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Fundamental Understanding and Development of Low-Cost, High-Efficiency Silicon Solar Cells

Annual Progress Report: Sept. 1997 – Aug. 1998

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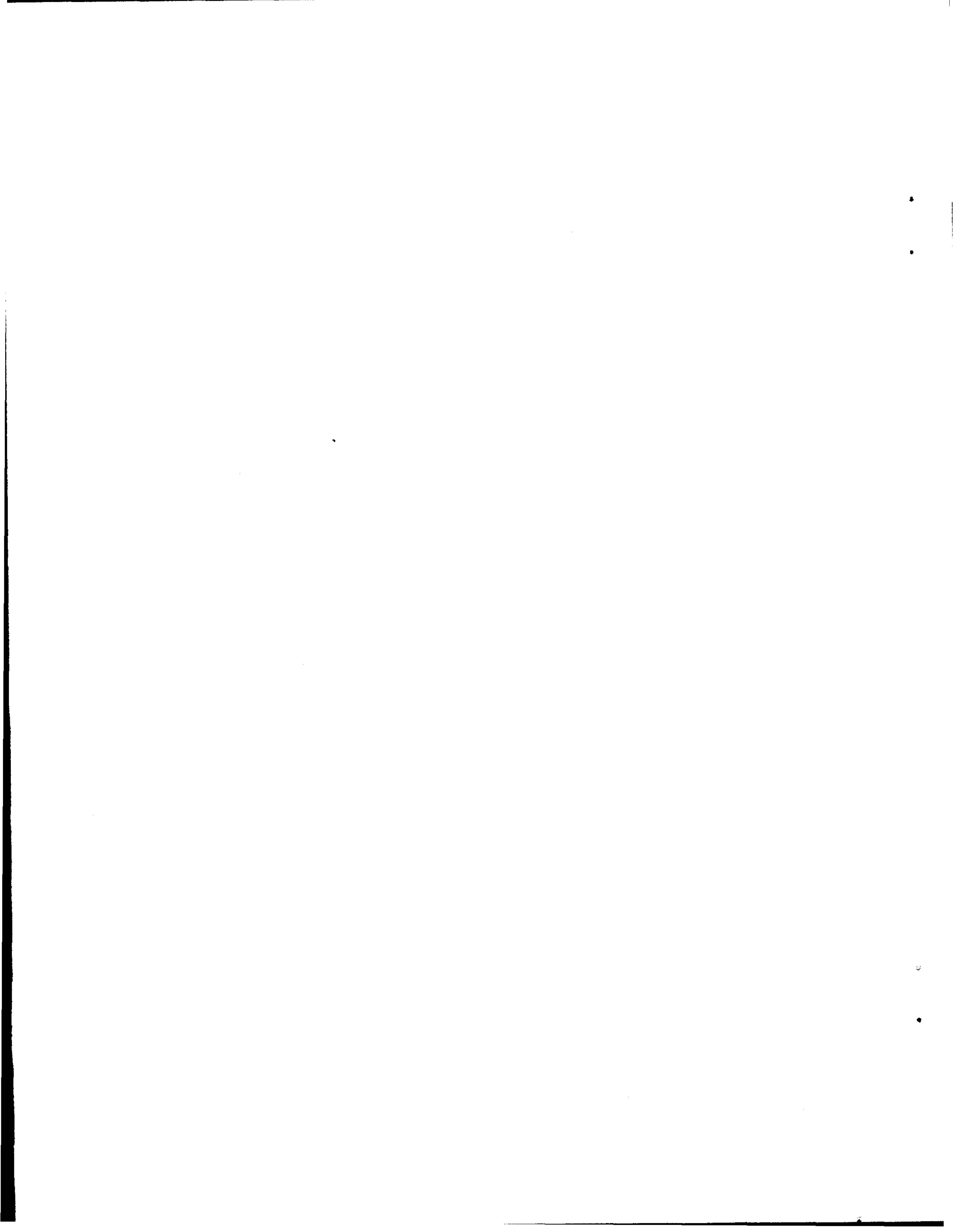
ABSTRACT

The overall objective of this program is 1) to develop rapid and low-cost processes for manufacturing that can improve yield, throughput, and performance of silicon photovoltaic devices, 2) to design and fabricate high-efficiency solar cells on promising low-cost materials, and 3) to improve the fundamental understanding of advanced photovoltaic devices. Several rapid and potentially low-cost technologies are described in this report that were developed and applied toward the fabrication of high-efficiency silicon solar cells.



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SUMMARY

Overall objective of this program is threefold. First, to develop rapid and low-cost manufacturable processes that can improve yield, throughput and performance of silicon photovoltaic devices; second, to design and fabricate high efficiency solar cells on promising low-cost photovoltaic materials and third, to improve the fundamental understanding of advanced photovoltaics devices. In this report several rapid and potentially low-cost technologies are developed and applied toward the fabrication of high efficiency silicon solar cells.

One of the most difficult aspects of large scale solar cell production is forming low-cost, high-quality front contacts. Screen-printing (SP) offers a simple, cost-effective contact method that is consistent with the requirements for high-volume manufacturing. The current problem with SP, however, is that the throughput gains are attained at the expense of device performance. Literature shows considerable scatter in the fill factor values of SP solar cells. In addition there are no clear guidelines for achieving high fill factors. Therefore, a methodology for optimizing SP metallization is developed, recognizing the fact that fill factor can be degraded by gridline resistance, contact resistance, and contact formation induced junction leakage and shunting. Systematic optimization of the firing cycle and junction depth, coupled with a post contact forming gas anneal, resulted in fill factors in excess of 0.78 on monocrystalline silicon. Preliminary results on multicrystalline silicon cells indicate that firing cycle and junction depth may need to be optimized for each multicrystalline silicon material due to the possible role of defects in causing junction shunting underneath the gridlines.

A comprehensive and systematic investigation of low-cost surface passivation technologies is presented for achieving high-performance silicon devices such as solar cells. Most commercial solar cells today lack adequate surface passivation, while laboratory cells use conventional furnace oxides (CFO) for high-quality surface passivation involving an expensive and lengthy high-temperature step. This investigation tries to bridge the gap between commercial and laboratory cells by providing fast, low-cost methods for effective surface passivation. This report demonstrates for the first time, the efficacy of TiO_2, thin (<10 nm) RTO, and PECVD SiN individually and in combination for (phosphorus diffused) emitter and (undiffused) back surface passivation. The effects of emitter sheet resistance, surface texture, and three different SiN depositions (two direct PECVD systems and one remote plasma system) were investigated. The impact of post-growth/deposition treatments such as forming gas anneal (FGA) and firing of screen-printed contacts was also examined. This study reveals that the optimum passivation scheme consisting of a thin RTO with a SiN cap and 730°C screen-printed contact firing anneal can (a) reduce the emitter saturation current density, J_{Oe}, by a factor >15 for a 90 Ω/sq. emitter, (b) reduce J_{Oe} by a factor of >3 for a 40 Ω/sq. emitter, and (c) reduce S_{back} below 20 cm/s on 1.3 Ωcm p-Si. Furthermore, this double-layer RTO+SiN passivation is relatively independent of the deposition conditions (direct or remote) of the SiN film and is more stable under heat treatment than SiN or RTO alone. Critical to achieving low S by the RTO/PECVD SiN stack is the use of a short, moderate temperature anneal (in this study 730°C for 30 seconds) after the stack formation. This thermal treatment is believed to enhance the release and delivery of

atomic hydrogen from the SiN film to the Si-SiO_2 interface, thereby reducing the density of interface traps at the silicon surface. Compatibility with this post-deposition anneal makes the stack passivation scheme attractive for cost-effective solar cell production where a similar anneal is required to form screen-printed contacts. Model calculations are also performed to show that the RTO+SiN surface passivation scheme may lead to greater than 17%-efficient thin screen-printed cells even with a low bulk lifetime of 20 μs.

Screen-printing and rapid thermal annealing have been combined to achieve an aluminum- alloyed back surface field (Al-BSF) that lowers the effective back surface recombination velocity (S_{eff}) to approximately 200 cm/s for solar cells formed on 2.3 Ω-cm Si. Analysis and characterization of the BSF structures show that this formation process satisfies the two main requirements for achieving low S_{eff}: 1) deep p^+ regions and 2) uniform junctions. Screen-printing is ideally suited for fast deposition of thick Al films which, upon alloying, result in deep BSF regions. Use of a rapid alloying treatment is shown to significantly improve the BSF junction uniformity and reduce S_{eff}. The Al-BSFs formed by screen-printing and rapid alloying have been integrated into both laboratory and industrial-type fabrication sequences to achieve solar cell efficiencies in excess of 19.0% and 17.0%, respectively, on planar 2.3 Ω-cm float zone Si. For both process sequences, these cell efficiencies are 1-2% (absolute) higher than analogous cells made with un-optimized Al-BSFs or highly recombinative rear surfaces.

Research was also conducted to achieve high efficiency cells on multicrystalline silicon materials. In this report, the effect of impurity gettering and defect passivation by hydrogenation was examined on 100 μm thick string ribbon silicon material from

Evergreen solar. Solar cells were fabricated with photolithography contacts as well as screen-printed contacts. Solar cells fabricated with phosphorus and aluminum gettering and FGA hydrogenation showed an increase in efficiency of 1.2% (absolute) over cells with the same gettering treatments but without FGA hydrogenation. Without the gettering treatments, FGA had little effect on the bulk lifetime. Cells processed with conventional furnace processing and photolithography contacts had an average efficiency of 14.6% with a maximum of 15.4%. A lifetime study of the optimization and application of beltline gettering and passivation techniques indicates that lifetimes over 50 μs are achievable even though the as-grown lifetime values are only about 1 μs. The first 100 μm thick fully screen-printed cell with a beltline diffused emitter (BLP) of 45 Ω/ produced efficiencies as high as 10.9%. The main loss components of the screen-printed devices are in the blue response and low shunt resistance. The shunt resistance of screen-printed devices was increased from 200 $\Omega\text{-cm}^2$ to over 5000 $\Omega\text{-cm}^2$ by implementing a spike in the contact firing profile. An increase in the red response resulted in cells that were spike fired and may be due enhanced bulk hydrogenation from the SiN film. Cell efficiencies as high as 14.9% were achieved on 250 μm substrates using beltline processing and screen-printing.

A novel simultaneous boron and phosphorus diffusion technique is presented to produce simple, high efficiency $n^+ pp^+$ silicon solar cells in one thermal cycle. This technique uses boron and phosphorus spin-on dopant films to fabricate limited solid doping sources out of dummy silicon wafers. This approach results in the delivery of a fixed dose of P_2O_5 or B_2O_3 to the diffused sample. The resulting diffusion glass is extremely thin (~60 Å) which allows for the *in-situ* growth of a passivating thermal oxide

without increasing the solar cell reflectance. J_o measurements show that the *in-situ* oxide passivation for a light boron and phosphorus diffusion provides excellent passivation properties, resulting in J_o values in the 100 fA/cm^2 range. Measurements of the bulk minority carrier lifetime show that by fabricating separate boron solid sources, trace impurities in the spin-on dopant film are not transported to the diffused sample. This filtering action is shown to result in bulk lifetimes in excess of 1 ms for silicon doped indirectly from the source wafers, but gives much lower lifetimes (~6 μs) for the wafers on which the boron spin-on film was directly applied. This process was validated by fabricating, *in-situ* oxide passivated, $n^+ pp^+$ solar cells in one high temperature cycle incorporating several high efficiency features including surface texturing and a Back Side Reflector (BSR), resulting in confirmed efficiencies in the 19-20% range.

Finally, the individual rapid and potentially low-cost processes are integrated to form high efficiency devices. RTP solar cell efficiencies of 17% and >19% are achieved on monocrystalline silicon with screen printed and photolithography contact, respectively. Rapidly formed screen printed cells in a commercial beltline machine also resulted in 17% efficient cells on monocrystalline silicon and 14.9% efficient cells on multicrystalline string ribbon material.

1. Fundamental Understanding and Development of Screen-Printed Metallization for Monocrystalline Si Solar Cells

One of the most difficult aspects of large scale solar cell production is forming high-quality front contacts. The metallization techniques used in laboratory settings (which involve vacuum evaporation, lift-off photolithography, and plating) are too time consuming and impractical for large scale application. On the contrary, screen-printing (SP) offers a simple, cost-effective contact method that is consistent with the requirements for high-volume manufacturing. The problem with SP, however, is that the throughput gains are attained at the expense of device performance. The losses associated with SP metallization fall into three categories: 1) increased minority carrier recombination in the required heavily doped n^+ regions, 2) increased shading due to wide grid fingers (> 100μm), and 3) fill factor degradation due to poor contact quality. The purpose of this section is to provide a detailed study of the third issue: *contact quality*. This is important because contact quality determines the device fill factor, and therefore, affects the overall cell efficiency ($\eta=V_{OC}\cdot J_{SC}\cdot FF$). Though high fill factor performance has been demonstrated in the past with SP [1], most commercial solar cell processes which implement this technology result in relatively low fill factors (≈ 0.750) [2]. No comprehensive study has been conducted to isolate the causes for low fill factor in SP cells and relate them to specific process conditions.

In this study, the SP process is closely analyzed and developed so that high fill factors (≈ 0.785-0.790) can be reproducibly achieved on monocrystalline Si solar cells. The requirements on emitter junction depth and contact firing schedules are established in a systematic manner. For the first time, the beneficial effect of a *post-fire* forming gas anneal on contact resistance is demonstrated. By achieving high fill-factor response, device efficiencies of 17.0% (4 cm^2) are demonstrated for fully screen-printed, planar, single layer AR coated solar cells fabricated on FZ Si substrates.

1.1 Fill Factor Loss Mechanisms

The *primary* fill factor loss mechanisms associated with SP metallization are shown in Fig. 1.1. The losses arise from excess: 1) gridline resistivity, 2) contact resistance, and 3) junction leakage and shunting. The *gridline resistivity* and the *contact resistance* both depend on the

contact firing cycle and the material qualities of the conductor paste. If the overall resistance becomes excessive, then the solar cell fill factor will be lowered. The *junction leakage* and *shunting behavior* depend primarily on the junction design and the contact firing cycle. If the junction is compromised during the firing cycle, the lowered shunt resistance and increased junction leakage will cause severe fill factor degradation.

The impact of series resistance (R_{series}), shunt resistance (R_{shunt}), and junction leakage (J_{02} and n_2) on device fill factor can be simulated numerically using the solar cell equivalent circuit model shown in Fig. 1.2. (The J_{o2} diode and its corresponding ideality factor model the effect of junction leakage via depletion region recombination.) This equivalent circuit was employed together with a device simulator (*PC1D-4*) to model the fill factor change as a function of R_{series}, R_{shunt}, and J_{o2}. The results (Fig. 1.3-Fig. 1.5) can be used to formulate the following guidelines for attaining high fill factor: R_{shunt}>1000 Ω-cm^2, R_{series}<0.50 Ω-cm^2, and J_{o2}<10^{-8} A/cm^2. In the following sections, the experimental behavior of screen printed metallization in the context of these parameters is presented. Different characterization techniques, such as diode (dark) IV, solar cell lighted IV, contact resistance, and conductivity analysis, are used to extract the parameters which govern fill factor response.

1.2 Effect of SP Firing Treatment on Conductor Paste Resistivity

The conductor paste used in this work was made by Ferro Corporation (*3349 Ag Conductor*). After printing, the following procedure was used to form the contacts. First, the solvents were removed by baking on a hotplate at 150°C for 2 minutes. This was followed by firing in a 3-zone IR-belt furnace in which the lengths of zones 1,2, and 3 were 7.5", 15", and 7.5", respectively. The first two zones were set to 425°C and 580°C and used to burn off organic materials in the printed paste. The *hotzone* (zone 3) temperature was varied to suit the particular investigation. The overall firing time was determined by the beltspeed through the furnace. Beltspeeds of 15"/min and 40"/min were implemented in this study, which correspond to hotzone dwell times of 30 seconds and 11 seconds, respectively.

First, the Ag resistivity was determined so that basic model calculations could be performed. (It is instructive to note that the resistivity of pure Ag is 1.6 μΩ-cm.) As shown in Fig. 1.6, this parameter is a function of hotzone firing temperature. In fact, the resistivity changes by more than a factor of 2 (from 5.3 to 2.2 μΩ-cm) for a hotzone temperature swing of 300°C and a dwell

time of 30 seconds. The data also shows the effect of varying the beltspeed through the furnace. Two points are important to note when considering the effects of beltspeed on a process. The first issue is obvious: a higher beltspeed reduces the overall process time. Additionally, for a fixed temperature setting, a higher beltspeed will result in the sample moving deeper into the furnace before it is brought to temperature. To compensate for these effects, the temperature setpoints must be increased when a faster beltspeed is implemented. This behavior is evident in Fig. 1.6.

The data in Fig. 1.6 was used to model and compare the power loss expected for solar cells with pure Ag contacts (1.6 μΩ-cm) and SP Ag contacts (3.5 μΩ-cm, 700°C hotzone, 30 sec dwell time). The following device parameters were used for simulation purposes: solar cell active area of 2 cm by 2 cm, 8 grid fingers, a single tapered bus bar, and a 40 Ω/sq emitter sheet resistance. The width and height of each finger were fixed at 130 μm and 8 μm, respectively (typical values for screen-printed solar cells). The simulations show that the increased metal resistivity of SP Ag compared to pure Ag leads to an R_{series} increase of 0.12 $\Omega\text{-cm}^2$ and an *additional* power loss of 0.14 mW/cm^2. In other words, SP fill factors are inherently lower than those of a pure Ag metallization by approximately 0.010 due to higher ρ_{metal} and R_{series}.

1.3 Effect of Junction Depth on the FF of Monocrystalline Si Solar Cells

As discussed in Section 2, most conductor pastes contain a small amount of glass frit. The frit serves to improve adhesion to the substrate by conforming to the surface topology. Additionally, for Si substrates, the frit *etches* a small distance into the Si material. If the firing process is too aggressive, the glass frit along with the metal particles will begin to encroach on the n^+p junction. This encroachment manifests itself as decreased R_{sh} and increased J_{o2}. As indicated by the modeling results in Fig. 1.2, low R_{sh} and high J_{o2} can destroy the device fill factor.

In this section, the importance of junction depth on the quality of SP contacts is explored. A set of phosphorus diffusions was carried out using cerium pentaphosphate solid sources. The diffusion time was fixed at 30 minutes, and in each case the peak temperature was varied. The resulting sheet resistances were in the 40-90 Ω/sq range, and the junction depths are shown in Fig. 1.7.

Screen-printed solar cells were formed on each emitter. (Throughout this study, all devices were 4 cm^2 in area, and the front contact coverage was roughly 7%). To fire the contacts, an

intermediate beltline firing cycle (hotzone temperature of 730°C and beltspeed of 15"/min) was selected based on Fig. 1.6. After firing, the contacts were annealed in forming gas at 400°C. (This FGA plays an important role in reducing contact resistance, and will be discussed in detail in a following section.) A histogram of fill factor versus emitter sheet resistance is shown in Fig. 1.8. For comparison, the high fill factor of a device formed with photolithography (PL) contacts is also shown. The same data is presented as a function of junction depth in Fig. 1.9.

As shown in Fig. 1.9, the highest fill factor was measured for the deepest junction (40 Ω/sq, x_j of 0.38μm). Yet even for this case, there is a noticeable fill factor spread (0.740-0.780) which is unacceptable for reliable, high-efficiency devices. As the emitter junction depth decreases, the fill factor drops off sharply. This behavior suggests two possibilities: 1) with reduced junction depth the cells suffer from lowered R_{sh} and high J_{o2}, or 2) with increased emitter sheet resistance the devices experience higher R_{series} from contact resistance effects. In order to precisely determine the cause for the fill factor drop, the non-illuminated I-V responses for the cells were measured and analyzed. Plots of these IV curves are shown in Fig. 1.10. For comparison, the IV response for a cell with contacts formed by lift-off PL is also shown. It is immediately evident that the lift-off PL cell has a large R_{sh} and low leakage current. Fitting this IV curve to the equivalent circuit model in Fig. 1.2 reveals in an $R_{sh}=6\times10^3$ Ω-cm², $J_{o2}=1\times10^{-8}$ A/cm² (with $n_2=2$), and $R_{series}=0.35$ Ω-cm². These parameters are consistent with the high fill factor (0.792) exhibited by the cell. On the contrary, the R_{sh} behavior for all the screen-printed devices is significantly worse. Analysis of these devices reveals R_{sh} values less than 1000 Ω-cm² in all cases and J_{o2} values greater than 0.5 μA/cm² ($n_2=2.2$). Moreover, the junction leakage worsens with increasing emitter sheet resistance and decreasing junction depth. These effects are responsible for the fill factor degradation and scatter shown in Fig. 1.8 and Fig. 1.9.

It is interesting to note that for all the n^+ emitters shown in Fig. 1.10, which exhibit surface concentrations between 2×10^{20}-5×10^{20} cm^{-3}, the R_{series} for all SP contacts is essentially the same. This observation is important because R_{series} is often presumed to be the cause of fill factor degradation when in fact the problem stems from the compromised junction.

1.4 Reducing Leakage and Shunting with Deeper n^+ Emitters

Deeper emitters were attained by diffusion from a $POCl_3$ liquid source at a diffusion temperature of 900°C. An appropriate gas flow condition and diffusion time were established so that a 35-40 Ω/sq emitter with 0.5 μm junction depth was achieved. The n^+ region profile is

shown in Fig. 1.11 along with the first set of emitters formed by solid source diffusion. Initial SP solar cells were fabricated on this new emitter using the same process detailed above (hotzone of 730°C and beltspeed of 15"/min). Average fill factors of 0.785 were consistently achieved. It is evident from Fig. 1.12 that the problems of excess shunting and leakage are eliminated.

Table 1.1. Junction depth requirement for screen printed contact formation to monocrystalline Si solar cells.

Junction Depth	R_{shunt} Value	Junction/FF Quality
< 0.25 μm	low	Completely shunted/Low FF
0.30-0.40 μm	< 1000 Ω-cm^2	Onset of leakage/Moderate FF
> 0.50 μm	≈ 10,000 Ω-cm^2	No shunting or leakage/High FF

By consolidating the data in Fig. 1.8 through Fig. 1.12, the following guidelines for emitter junction depth are established for SP contact formation.

1.5 Effect of Firing Conditions and Post-Firing Forming Gas Anneal on the Contact Resistance and Fill Factor

In addition to R_{sh} and J_{o2}, the quality of SP contacts depends critically on the overall R_{series}. This was shown in the modeling results of Fig. 1.4 and Fig. 1.5. R_{series} is comprised of different resistance components (metal resistivity and contact resistance, among others). The metal resistivity issue was discussed in Section 4.2.2. In this section, the contact resistance (ρ_c) associated with SP metallization is investigated. In a novel application, a low-temperature FGA is shown to be effective in lowering ρ_c *after* the SP contacts have been fired in the IR-belt furnace.

The investigation of peak firing condition on fill factor was extended for large temperature variations. The response is shown in Fig. 1.13 for beltspeeds of 15"/min and 40"/min. Immediately after the firing treatment, the fill factors are prohibitively low (≈0.500-0.600). However, the fill factors drastically improve after the samples are annealed in forming gas at 400°C. For the hotzone dwell time of 30 sec (beltspeed of 15"/min), there exists at least a 60°C range in acceptable peak firing temperature (690°C to 750°C) in which final fill factors of 0.785 are attained. For the 40"/min beltspeed, a similar range exists, though higher process temperatures are required to offset the reduced dwell time and increased ramp-up distance. These

results indicate that, in contrast to conventional thinking on the topic, the range of acceptable firing temperatures is relatively broad.

In order to verify that the FGA specifically acts to improve ρ_c, non-illuminated IV measurements were conducted for a typical device before and after the FGA treatment. The result in Fig. 1.15 shows that after annealing, the curve changes in the high-current regime where the response is most sensitive to R_{series}. It was determined separately that the FGA has no effect on the gridline resistivity of the fired metal. This clearly shows that the only parameter altered by the FGA is ρ_c. Additionally, *transmission line model* (TLM) based contact resistance measurements were performed for the SP metallization (Fig. 1.14). These results also provide clear support of ρ_c reduction as a result of the FGA treatment.

It is believed that the FGA initiates an oxidation-reduction (redox) reaction at the interface between the printed metal and the Si surface. The question is why should such a reaction be important for SP contacts? The Ag paste used in this study contains a lead borosilicate glass frit. At the time of printing, the Ag and frit particles are packed together within the organic vehicle. When firing is initiated, the organic vehicle is burned away leaving behind the metal-frit combination. As the temperature is raised further, the metal particles begin to sinter which serves to expel or "squeeze out" the frit from the interior of the printed feature. (This process is also referred to as glass "bleedout" [3].) The glass frit is forced to migrate to the metal surface and the Si-metal interface. Since the firing is done in air, some of the lead content in the frit becomes oxidized. This creates an insulating layer and a large ρ_c at the metal-Si interface. The hydrogen in the ensuing FGA is believed to reduce this species back to Pb, bringing about the measured improvement in the ρ_c.

In order to provide a degree of verification for this model, a similar contact anneal at 400°C was conducted in N_2 instead of forming gas. The results in Fig. 1.16 show that the N_2 anneal in *no way* improves the contact quality. However, subjecting the same samples to a subsequent FGA treatment improves the fill factor to a high level. This provides clear evidence that hydrogen is the active species in this process, and it supports the theory that a reduction reaction is occurring at the Si surface to lower ρ_c.

1.6 Effect of Peak Firing Temperature on Solar Cell Shunting Behavior and Fill Factor

It is instructive to analyze the results of Fig. 1.13 in greater detail to ascertain the effect of peak firing temperature on contact quality. As indicated in this figure, there is a relatively large firing window (>60°C) which can be implemented to form high quality contacts. The question arises as to precisely what effect (if any) the process temperature within this range has on the contact quality. The average dark IV responses for certain devices are shown in Fig. 1.17. The corresponding R_{sh} values, extracted from numerical analysis of the IV curves, are shown in Fig. 1.18. The analysis reveals that increasing the hotzone temperature by as little as 10°C results in a measurably reduced R_{sh}. A 60°C increase in hotzone temperature reduces R_{sh} by over one order of magnitude, from $2x10^4$ Ω-cm² at 690°C to 10^3 Ω-cm² at 750°C. However, as shown in Fig. 1.3, an R_{sh} value of 10^3 Ω-cm² essentially marks the cutoff between high and low fill factor response for solar cells. Since all cases in Fig. 1.17 have R_{sh} values are higher than 10^3 Ω-cm², all devices exhibit high fill factors (≈0.785).

Fig. 1.6 and Fig. 1.17 illustrate the fundamental competition in the SP process. Higher temperatures are needed to achieve low gridline resistivity, whereas lower temperatures are desirable to avoid shunting. The highest fill factors are achieved only when both R_{series} and R_{shunt} values fall within acceptable ranges.

Table 1.2. Reproducibility of the SP process developed in this study. Each entry represents an average value over multiple (≈ 9) cells. All devices are planar, 4 cm² in area, with single layer AR coatings.

Run ID	Cell Type	Voc (mV)	Jsc (mA/cm²)	Fill Factor	Eff. (%)
1	1.3Ω-cm Si (850°C beltline Al-BSF)	624	34.5	**0.791**	17.0
2	1.3Ω-cm Si (850°C beltline Al-BSF)	623	33.8	**0.789**	16.6
3	1.3Ω-cm Si (850°C RTP Al-BSF)	626	34.4	**0.783**	17.0
4	0.65Ω-cm Si (no BSF)	621	32.8	**0.785**	16.0
5	0.65Ω-cm Si (900°C beltline Al-BSF)	635	33.7	**0.796**	17.0

In order to determine the reproducibility of this contact formation method, many solar cells were fabricated with the above developed process. By implementing the 0.5 μm deep $POCl_3$ emitter, a hotzone temperature of 700°C-730°C with a dwell time of 30 seconds, and a 10 min FGA after firing, fill factors between 0.785-0.795 were achieved in a consistent manner on monocrystalline Si. Some of these results are listed in Table 1.2.

1.7 SP mc-Si Solar Cells

The SP process has been applied to various mc-Si substrates including Solarex, HEM, and Eurosolare. The fill factors as a function of junction depth are shown in Fig. 1.19. The results show that for highest FF response, deeper junctions are required for mc-Si substrates than for (100) single crystal Si. The increase in junction depth required, and the relative fill factors achieved, are material specific. It has been observed [4] that the etch reaction between the frit and Si is more aggressive for certain crystalline orientations (preference for <111> over <100>). Since mc-Si grains exhibit random orientations across a wafer, the reaction of the frit with various grains will be different. Some regions will have a greater tendency to react, and therefore, decrease the R_{shunt}.

1.8 Conclusions

An effective SP methodology has been developed which yields high-quality contacts and fill factors in the 0.785-0.795 range on single crystal Si solar cells. These values approach those achieved by intricate lift-off photolithography procedures. In achieving these results, multiple device related effects have been established. It has been shown that a critical junction depth (0.5 μm in the present case) is required to avoid fill factor degradation due to device shunting and excessive leakage. For this optimal emitter design, a relationship between peak firing temperature and the resulting R_{shunt} has been determined. Additionally, a novel post-firing FGA process has been shown to dramatically improve fill factor by lowering the contact resistance. It is believed that the hydrogen exposure during this treatment induces a redox reaction at the interface between Si and the SP contacts. This contact formation methodology has been used to achieve 17% efficient fully screen-printed, planar, single layer AR coated devices (4 cm^2 area) on FZ substrates. Other important aspects of these high-efficiency devices are discussed in the upcoming sections.

1.9 References

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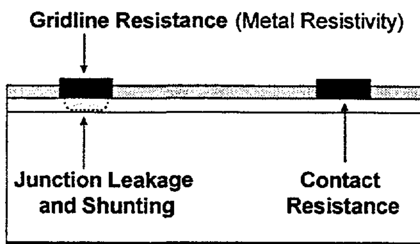

Fig. 1.1. Fill factor loss mechanisms associated with screen printing.

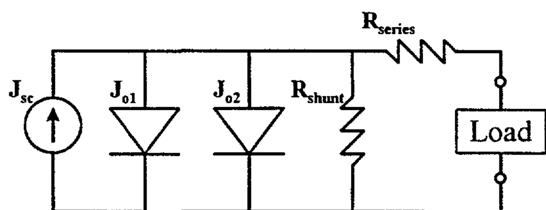

Fig. 1.2. Solar cell equivalent circuit. Fill factor is influenced by J_{o2}, R_{shunt}, and R_{series}.

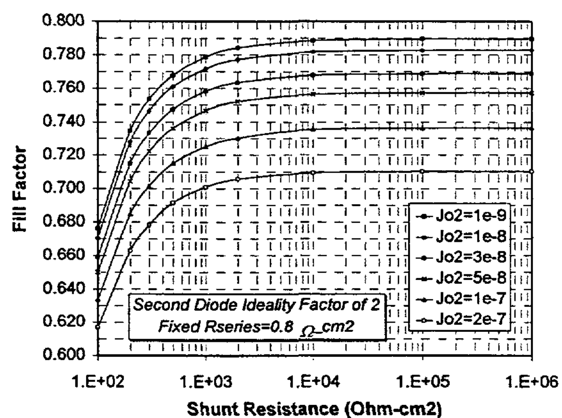

Fig. 1.3. Effect of R_{shunt} and J_{o2} on fill factor response. (R_{series} fixed at 0.8 Ω-cm²).

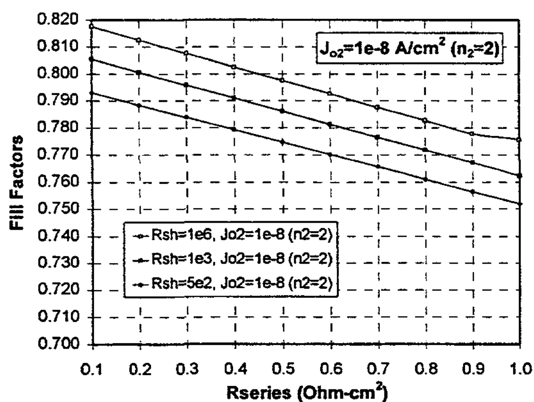

Fig. 1.4. Effect of R_{series} and R_{shunt} on fill factor response. (J_{o2} fixed at 10^{-8} A/cm².)

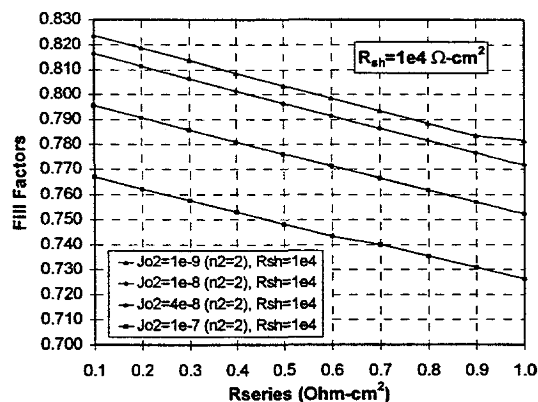

Fig. 1.5. Effect of R_{series} and J_{o2} on fill factor response. (R_{shunt} fixed at 10^4 Ω-cm².)

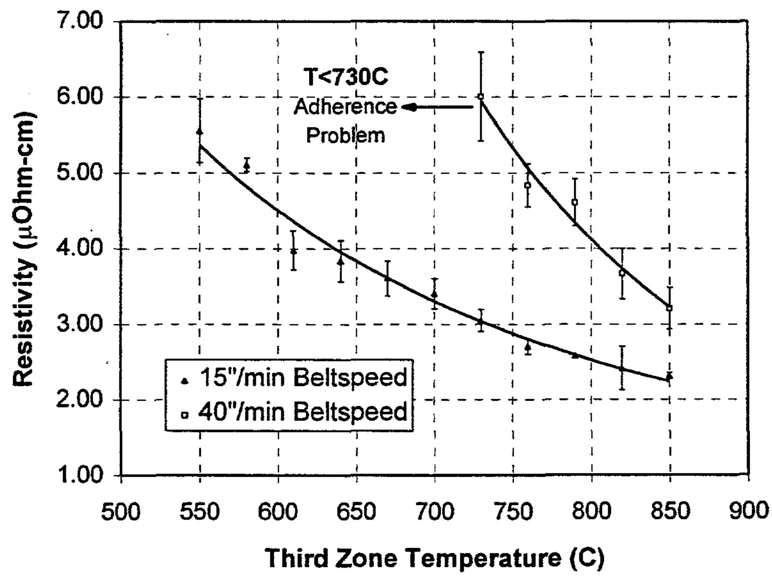

Fig. 1.6. Effect of beltline firing temperature and beltspeed on metal conductivity. The corresponding hotzone dwell times are 30 sec (15"/min) and 11 sec (40"/min).

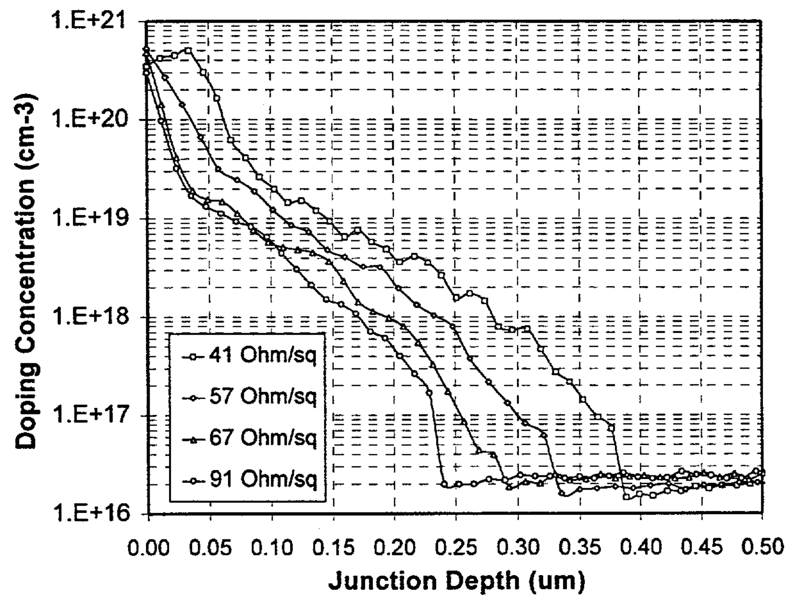

Fig. 1.7. Solid source diffusion profiles measured by the spreading resistance technique. The diffusion time was fixed at 30 min, and the highest temperature used was 850°C.

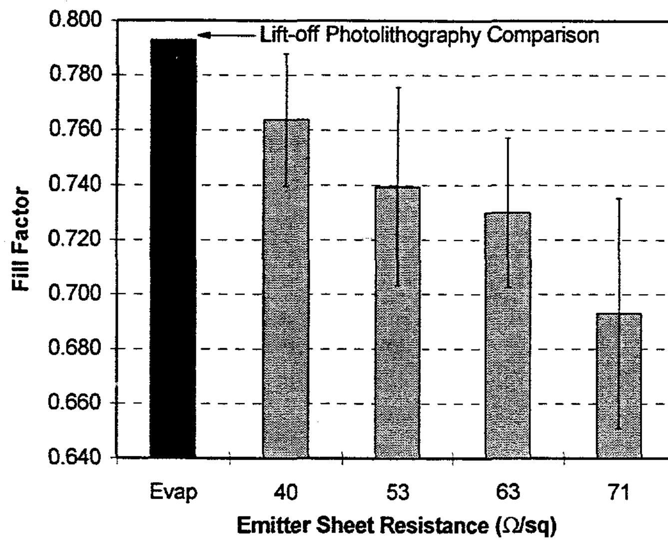

Fig. 1.8. Fill factor versus emitter sheet resistance.

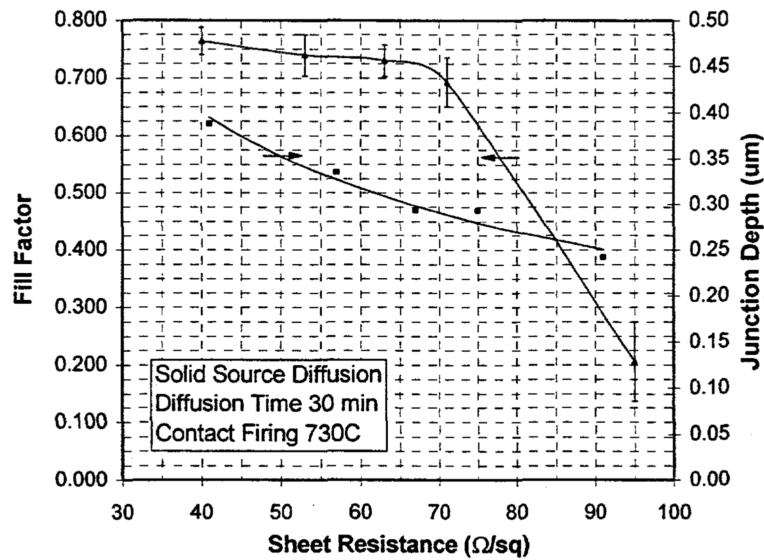

Fig. 1.9. Relationship between screen-printed fill factor and junction depth.

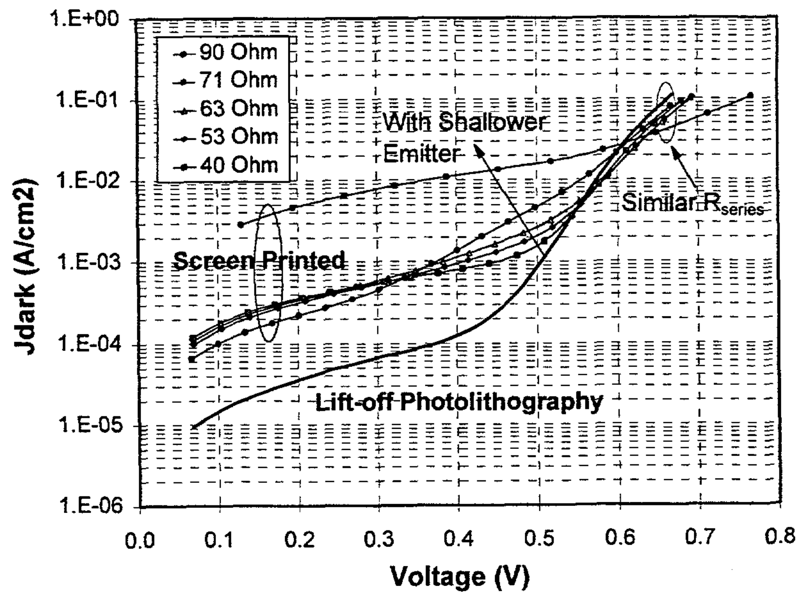

Fig. 1.10. Shunt and junction leakage effects on solar cell dark IV response.

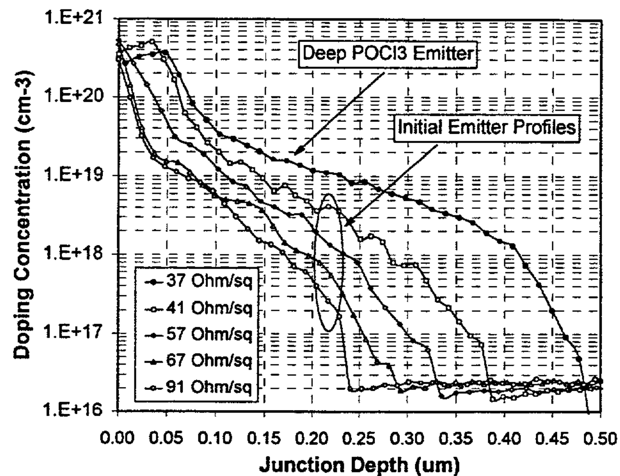

Fig. 1.11. Deeper $POCl_3$ emitter as compared to original solid source diffusion.

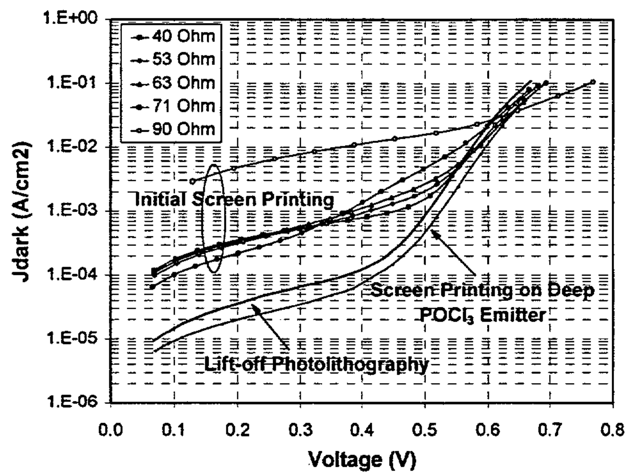

Fig. 1.12. Dark IV response when printing is done on deeper emitter.

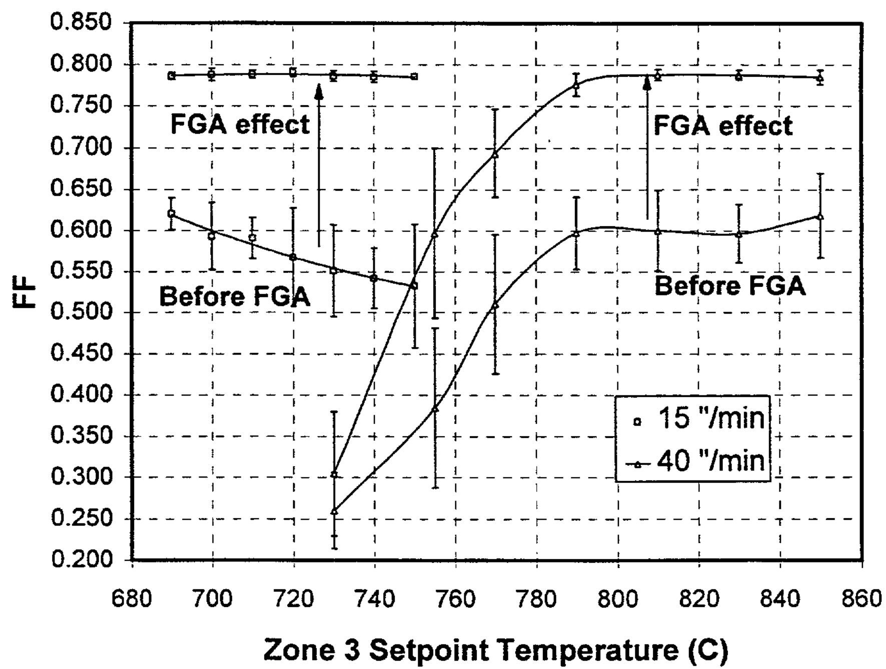

Fig. 1.13. Fill factor response as a function of hotzone temperature and dwell time.

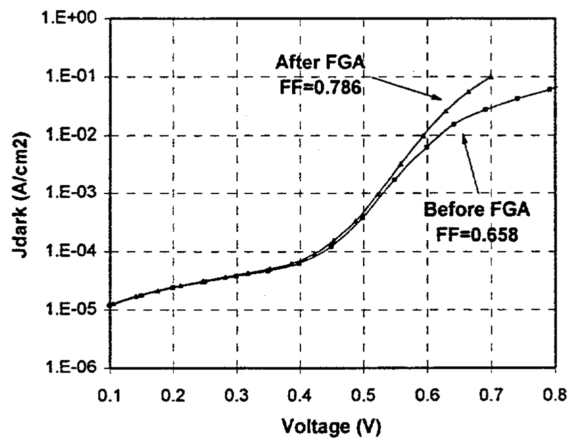

Fig. 1.14. The effect of a 400°C FGA on the series resistance of fired SP contacts.

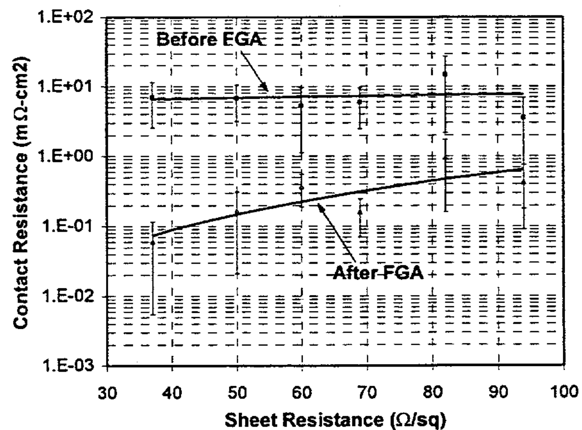

Fig. 1.15. The effect of the FGA on the ρ_c of SP contacts to n^+ emitter regions.

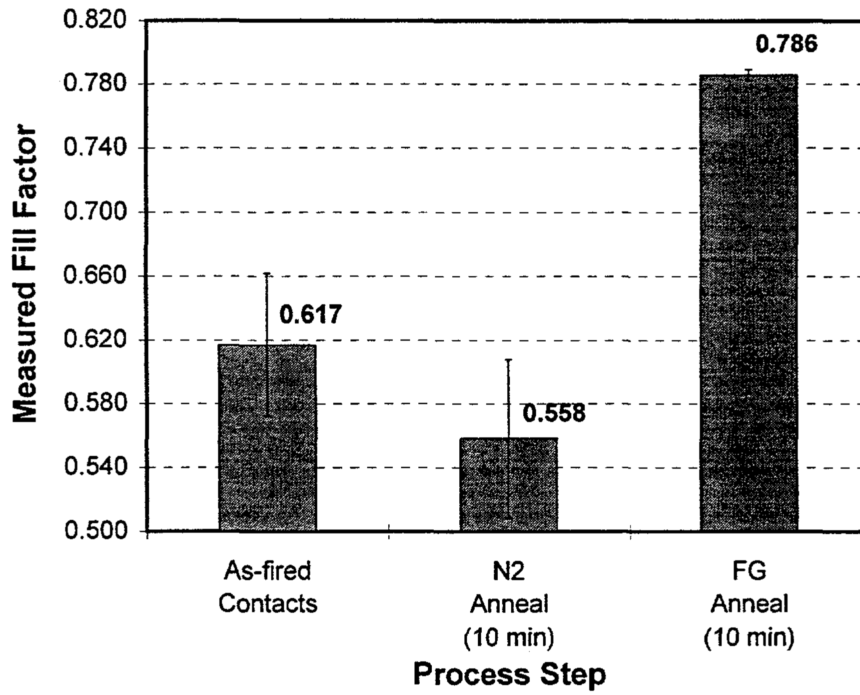

Fig. 1.16. Effect of post-firing contact anneal in non-reducing (N_2) and reducing (FG) ambients. The anneal temperature was 400°C.

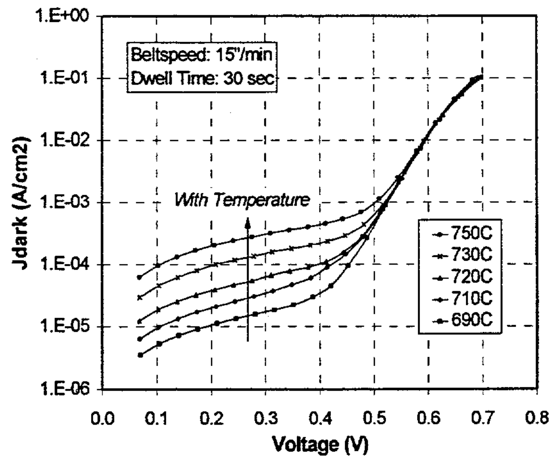

Fig. 1.17. Effect of hotzone firing temperature on the ensuing dark IV response of solar cells.

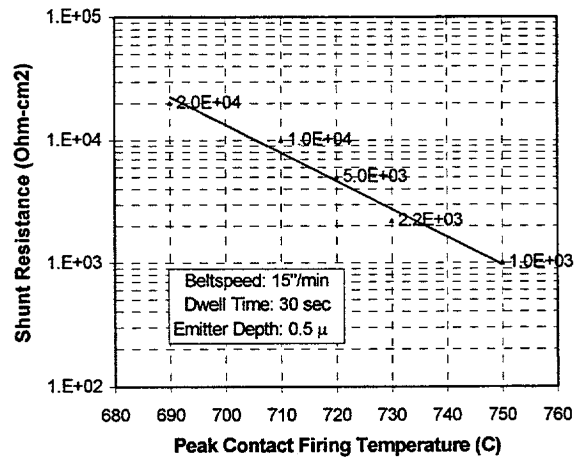

Fig. 1.18. Effect of hotzone firing temperature on R_{sh} value.

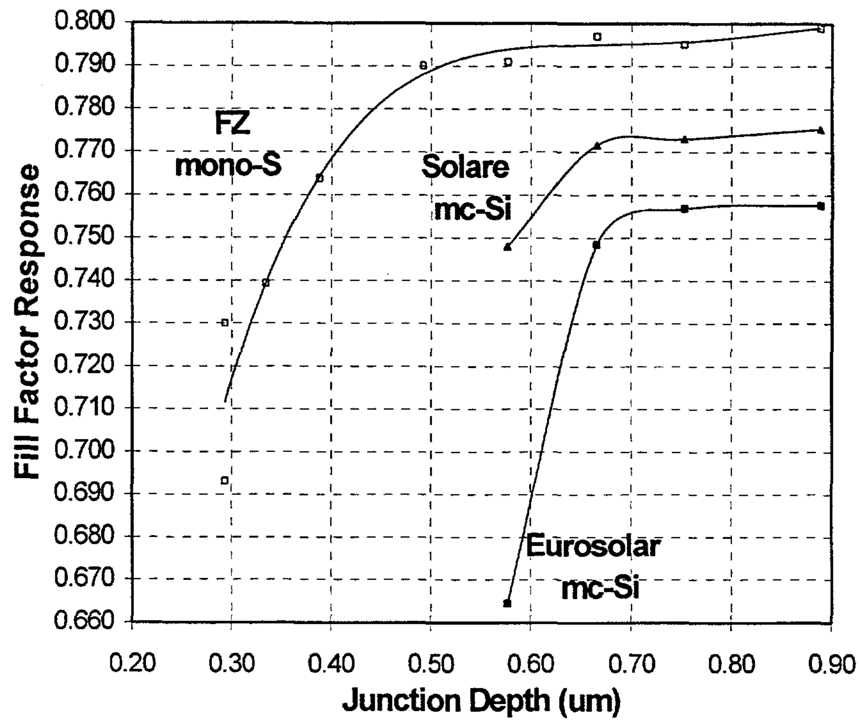

Fig. 1.19. The effect of junction depth on fill factors for SP mc-Si solar cells.

2. Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies

A comprehensive and systematic investigation of low-cost surface passivation technologies is presented for achieving high-performance silicon devices, in this case for photovoltaic devices. Most commercial solar cells today lack adequate surface passivation. In contrast, laboratory cells use conventional furnace oxides (CFO) for high-quality front and/or back surface passivation but at the expense of a lengthy, high-temperature step. This investigation tries to bridge the gap between commercial and laboratory cells by providing fast, low-cost methods for effective surface passivation. As an alternative to CFO, rapid thermal oxides (RTO) can give comparable passivation in a much shorter time. Additionally, plasma deposition of silicon nitride (SiN) has recently emerged as a low-temperature passivation technique, which simultaneously provides a good antireflection coating for silicon solar cells. In this work, we demonstrate, for the first time, the efficacy of TiO_2, thin (<10 nm) RTO, and PECVD SiN passivation individually and in combination for (diffused) emitter and (non-diffused) back surface passivation. The effects of emitter sheet resistance, surface texture, and three different SiN depositions (two using a direct PECVD system and one using a remote system) were investigated. The impact of post-growth/deposition treatments such as forming gas anneal (FGA) and firing of screen-printed contacts was also examined. This study reveals that the optimum passivation scheme consisting of a thin RTO, SiN, and 730°C screen-printed contact firing anneal can (a) reduce the emitter saturation current density, J_{0e}, by a factor of >15 for a 90 Ω/sq. emitter, (b) reduce J_{0e} by a factor of > 3 for a 40 Ω/sq. emitter, and (c) reduce S_{back} below 20 cm/s on 1.3 Ωcm p-Si. Furthermore, this double-layer RTO+SiN passivation is independent of the deposition conditions (direct or remote) of the SiN film and is more stable

under heat treatment than SiN or RTO alone. Model calculations are also performed to show that the RTO+SiN surface passivation scheme may lead to 17%-efficient thin screen-printed cells even with a low bulk lifetime of 20 μs.

2.1 INTRODUCTION

Minimizing recombination of minority-carriers at the surfaces of silicon is crucial for the performance of many Si devices including solar cells, BJTs, CCDs, power devices. The objective of this paper is to provide a comprehensive and systematic study of different surface passivation technologies available for diffused and non-diffused silicon, planar (flat) and chemically textured surfaces. The information is immediately applicable for junction devices such as solar cells, which typically have a n^+p structure. For such devices, surface passivation is the key to higher performance especially because the trend is towards thinner substrates, which bring the surface closer to the collecting junction.

The passivation schemes investigated include evaporated films of TiO_2, thin SiO_2 films grown in a conventional furnace (CFO) and in a rapid thermal processor (RTO), plasma-deposited (PECVD) SiN, and selected combinations of RTO, TiO_2, and SiN. RTO films are of particular interest because thin 8-10 nm films can be grown in an extremely short time. Films like TiO_2 and SiN are investigated because they provide silicon antireflection properties, which are essential for photovoltaic devices. Since SiN depends strongly upon deposition conditions and the type of PECVD equipment used, SiN films from three different sources were compared.

In this study, rapid, low-cost technologies like RTO and PECVD SiN are focused upon. These low-cost methods can provide effective surface passivation in short time and with a much lower thermal budget than a CFO. Individually, their effectiveness for solar cell passivation has been demonstrated previously [1,2,3]. However, their combined effect and their ability to

withstand subsequent thermal treatments necessary for complete solar cell fabrication has never been studied. Therefore, the impact of solar cell fabrication steps like forming gas anneal (FGA) and screen-printed contact firing on the surface passivation quality of individual and double-layer stacks of dielectrics has also been quantified.

2.2 EXPERIMENTAL

To assess the surface passivation of p-type silicon, effective minority carrier lifetime (τ_{eff}) measurements were performed on 1.3 Ωcm p-type <100> FZ silicon wafers coated with various passivating films. The investigation of n^+-emitter passivation was performed by J_{oe} measurements by the photoconductance decay (PCD) technique on diffused, high-resistivity (750 Ωcm), high bulk lifetime (> 1 ms) FZ Si wafers. Some of the wafers were subjected to a chemical random surface texturing before processing. Surface texturing is commonly used for solar cells to help optically confine and antireflect more light. Samples for the emitter passivation experiment were diffused on both sides in an RTP system using spin-on dopant sources. We investigated emitters with sheet resistances of 40 and 90 Ω/sq., which correspond to emitters that can accommodate screen-printed and evaporated contacts, respectively. After removal of the residual phosphosilicate glass, part of the diffused and non-diffused p-type samples were oxidized in the same RTP system used for the diffusions. This rapid thermal oxidation at 900°C for 150 s resulted in an oxide thickness of approximately 6 nm. The oxidized low-resistivity samples were then annealed in forming gas at 400°C for 15 min. After this, depositions of passivating films were performed in three different laboratories. The thickness of these films was approximately that of a single-layer antireflection (AR) coating (~60 nm). The refractive indices of these films measured at at 632.8nm were between 2.15 and 2.27, which is in the optimum range for single-layer AR coatings under glass, or the first film of double-layer AR coatings in air [4].

The deposition of TiO_2 was performed by evaporating titanium in an oxygen atmosphere under a low pressure of 15 mPa. For the deposition of SiN, three different PECVD systems were used. Two of these systems have a parallel plate reactor and high frequency excitation, with deposition temperatures of 300°C and 350°C, respectively. The third system is a remote PECVD system with microwave excitation and a deposition temperature of 400°C [5]. Table 2.1 summarizes the differences in key parameters of these systems. The plasma deposition systems vary in a number of other aspects, such as the reactor geometry, and the plasma power and pressure. However, all three SiN films are used as a standard in the respective laboratories.

After film deposition, the effective minority carrier lifetime (τ_{eff}) was measured on all samples. Subsequently, a forming gas anneal (FGA) at 400°C was performed on all samples. As a final step, the samples were subjected to a short temperature cycle with a maximum temperature of 730°C, which is typically used as a firing cycle for screen-printed contacts. This step was performed in a beltline furnace with tungsten-halogen lamp heating.

The minority carrier lifetime was measured after each step using a commercially available inductively-coupled PCD tester. From these data, the emitter saturation current J_{0e} (for diffused samples) and the surface recombination velocity S_{eff} were calculated. The PCD measurement of J_{0e} is discussed in Kane and Swanson [6] and S_{eff} was calculated using the following two equations [7]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \beta^2 \cdot D_n \qquad (1)$$

$$\tan\left(\frac{\beta \cdot W}{2}\right) = \frac{S_{eff}}{\beta \cdot D_n} \qquad (2)$$

In this study, an infinite bulk lifetime ($\tau_b \rightarrow \infty$)was assumed so the calculated S_{eff} actually represents the worst-case (maximum) value.

2.3 RESULTS AND DISCUSSION

The passivation of solar cell front surfaces was investigated on both 40 Ω/sq. and 90 Ω/sq. emitters. On relatively opaque 40 Ω/sq. emitters (which is generally needed to accommodate screen-printed contacts), the surface is largely decoupled from the bulk, because of the high surface doping concentration and depth of the doping profile. Thus, the introduction of RTO or SiN passivation resulted in a moderate decrease in J_{0e} of about a factor of two to three, as can be seen from Fig. 2.1. While TiO_2 showed hardly any passivation, SiN 1 was clearly inferior to RTO or SiN 3, which, in combination, resulted in the best passivation. Note that the high-temperature treatment during RTO growth changed the doping profile and lead to a lower surface doping concentration, which allowed for better surface passivation. The J_{0e} values for textured samples were about 1.5 to 2 times higher than those for planar surfaces, which resembles the 1.73 times increase in surface area resulting from regular pyramidal texturing.

On the relatively transparent 90 Ω/sq. emitters, (which are generally used for evaporated contacts) the difference in the degree of passivation for various schemes was more apparent, as shown in

Fig. 2.2. Again, TiO_2 does not provide any appreciable reduction in J_{0e}. For the planar surface, RTO growth reduced J_{0e} by more than a factor of ten to below 100 fA/cm^2, as does the deposition of SiN 3. However, on the textured surface, RTO is not as effective, resulting in a moderate J_{0e} value of 400 fA/cm^2. Here, SiN 3 and the RTO+SiN double layers were clearly superior.

As-deposited double layers of RTO and SiN were better than the nitrides alone in all cases, resulting in low J_{0e} values of 50 fA/cm^2 for planar and 100 fA/cm^2 for textured emitter surfaces (see Fig. 2.2). A subsequent forming gas anneal did not change the surface passivation appreciably. The same applies for the contact firing cycle on the 40 Ω/sq. emitters. This indicates that double layer passivation with a SiN cap preserves the passivation quality of heavily-doped silicon during contact firing. For comparison, thin conventional furnace oxides (CFOs) and double layers of CFO and SiN were grown on the same emitters. This passivation resulted in identical or only slightly lower J_{0e} values than the RTO-based schemes.

On the undiffused surface of 1.3 Ωcm silicon, the deposition of TiO_2 again did not give any measurable surface passivation, nor did the growth of RTO or the deposition of SiN 1 (see Fig. 2.3). (Please note that S_{eff} values above 10^4 cm/s could not be measured reliably by the method used in this study.) However, both SiN 1 and RTO passivation improved considerably after FGA. While as-deposited SiN 3 already gave very good passivation, it tended to degrade slightly with the FGA. Double layers of RTO with all nitrides resulted in excellent S_{eff} values after FGA, possibly because of the release of hydrogen from the SiN which then reaches the interface, reducing the interface state density.

Fig. 2.4 shows that the same trend was observed for textured surfaces, with SiN 3 giving considerably better passivation than the other nitrides. After FGA, all RTO+SiN double layers showed good passivation, resulting in a very low S_{eff} value of 39 cm/s for RTO+SiN 3.

As a last step, the samples with SiN and RTO+SiN double layers were subjected to a screen-print contact firing cycle with a maximum temperature of 730°C. Fig. 2.5 indicates that the SiN passivation resulted in moderate to low S_{eff} values after this treatment, with SiN 1 and SiN 3 showing some degradation. This may be because of hydrogen escaping from the SiN films. In contrast, the RTO+SiN double layers provided exceptionally low S_{eff} values regardless of the type

of nitride used. After this treatment, the double layer with SiN 1 resulted in the lowest S_{eff} value of 12 cm/s on a planar surface. Note that this value gives the same value as the record low S_{eff} value of 4 cm/s resulting from SiN 3 passivation [5] which was calculated using a bulk lifetime of 1.7 ms. Since we used an infinite bulk lifetime in all of our calculations, we have reported the higher value of 12 cm/s corresponding to the *maximum* S_{eff}. Furthermore, Fig. 2.5 clearly shows the superior thermal stability of RTO+SiN in contrast to any of the SiN films alone, which degrade upon screen-printed contact firing.

2.4 IMPACT OF SURFACE PASSIVATION ON PHOTOVOLTAIC DEVICE PERFORMANCE

Model calculations were performed to predict the impact of the various promising surface passivation schemes on the performance of photovoltaic devices. For this, a one-dimensional modeling program, PC-1D version 5.1 was used to calculate the energy conversion efficiency. The results of these calculations can be seen in Fig. 2.6 which shows the calculated cell efficiencies as a function of front and/or back surface passivation and a two different values of cell thickness (W = 100 or 300 μm) and bulk lifetime (τ_b = 20 μs or 200 μs). The calculations were performed with a 40 Ω/sq. emitter, 6% grid shading factor, and fill factor of 0.77-0.78 to be consistent with typical commercial screen-printed solar cells. Highly-efficient commercial screen-printed cells are about 14-15% efficient today and do not usually have front or back surface passivation. Fig. 2.6 shows that up to about 0.5% (absolute) gain in efficiency can be derived from improving just the front surface passivation. A comparatively large improvement can be gained by employing high quality

back surface passivation as well. The calculations show that 17-18%-efficient screen-printed cells are possible with RTO+SiN front and back surface passivation even on materials with a bulk lifetime of only 20 μs. It is very important to note that the calculations assumed negligible contact recombination, which may not be valid especially for back contacts unless a highly effective local back surface field is employed. However, we, along with others, have demonstrated low S_{pp+} values of 200-300 cm/s using an optimized Al BSF [3,8,9]. Thus, the cells in Fig. 2.6 may be realized with the combination of high-quality RTO+SiN passivation and a gridded BSF. Fig. 2.6 also shows that thinner cells (with a bulk lifetime of only 20 μs), which consume less silicon and therefore reduce cost, actually improve in performance because of high-quality back surface passivation. These calculations are encouraging especially since cost limitations are forcing the trend to reduced cell thickness with lower qualities of silicon.

2.5 CONCLUSIONS

This study provides a thorough investigation of silicon surface passivation by RTO, TiO_2, different PECVD silicon nitrides, and double-layer combinations of these films. The deposition or growth of these films can be performed in a matter of minutes, and all of the passivation schemes used provide or allow for near-optimum antireflection properties. Thus, they can enhance the performance of current industrial solar cells significantly. We have found that both a RTO film and three different silicon nitride films can individually reduce surface recombination substantially. Three PECVD SiN deposition systems, differing in various aspects, were used, and the resulting passivation was evaluated. This study demonstrated that the double-layer of RTO+SiN can improve the surface passivation even further, resulting in exceptionally low J_{0e} values below 50 fA/cm^2 on 90 Ω/sq. emitters, 200 fA/cm^2 on 90 Ω/sq. emitters, and maximum S_{eff} values below 20 cm/s on a

planar 1.3 Ωcm Si surface. The combination of RTO and SiN also reduces the gap in passivation quality between the different nitrides allowing for a high degree of freedom in the SiN deposition conditions. Furthermore, this combination has been shown to enhance the stability of the surface passivation under thermal treatments such as screen-printed contact firing. Textured surfaces revealed a similar trend as planar surfaces but showed a greater amount of surface recombination. Therefore, effective RTO+SiN passivation is even more essential for textured surfaces since surface recombination can frequently limit performance. Finally, model calculations show that the combination of RTO+SiN double-layer passivation and standard screen-printed contact firing anneal can result in significant improvement of current industrial cells. Calculations show that this passivation on the front and back may lead to 17%-efficient screen-printed cells on thinner substrates (100 μm) with low bulk lifetimes (20 μs), resulting in considerable cost reduction of photovoltaic cells.

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Table 2.1: Plasma depositions used in this investigation.

System No.	Excitation mode	Deposition Temp. [°C]	Gases
SiN 1	direct, HF (13.6 MHz)	300	SiH_4, N_2, NH_3
SiN 2	direct, HF (13.6 MHz)	350	SiH_4 (5%) in He, N_2, NH_3
SiN 3	remote, 2.45 GHz	400	SiH_4, NH_3

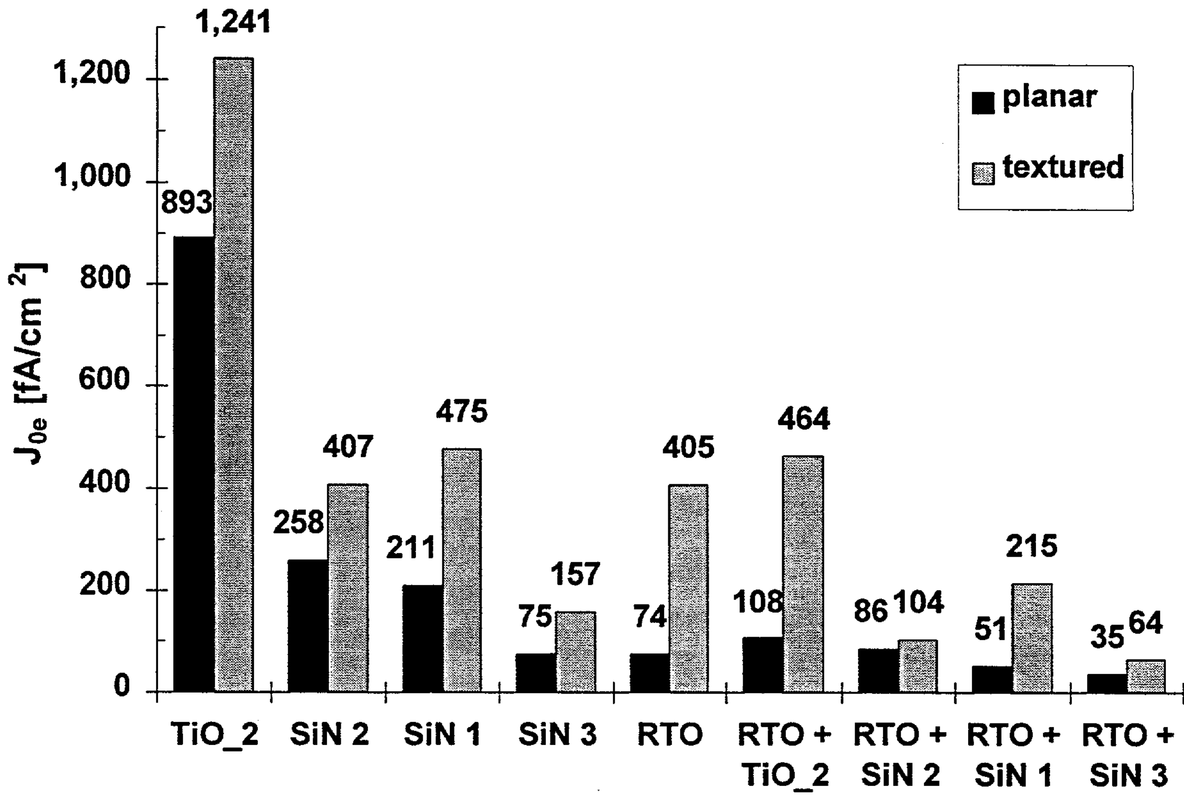

Fig. 2.1. Emitter saturation current densities for different passivation schemes on 40 Ω/sq. RTP emitters.

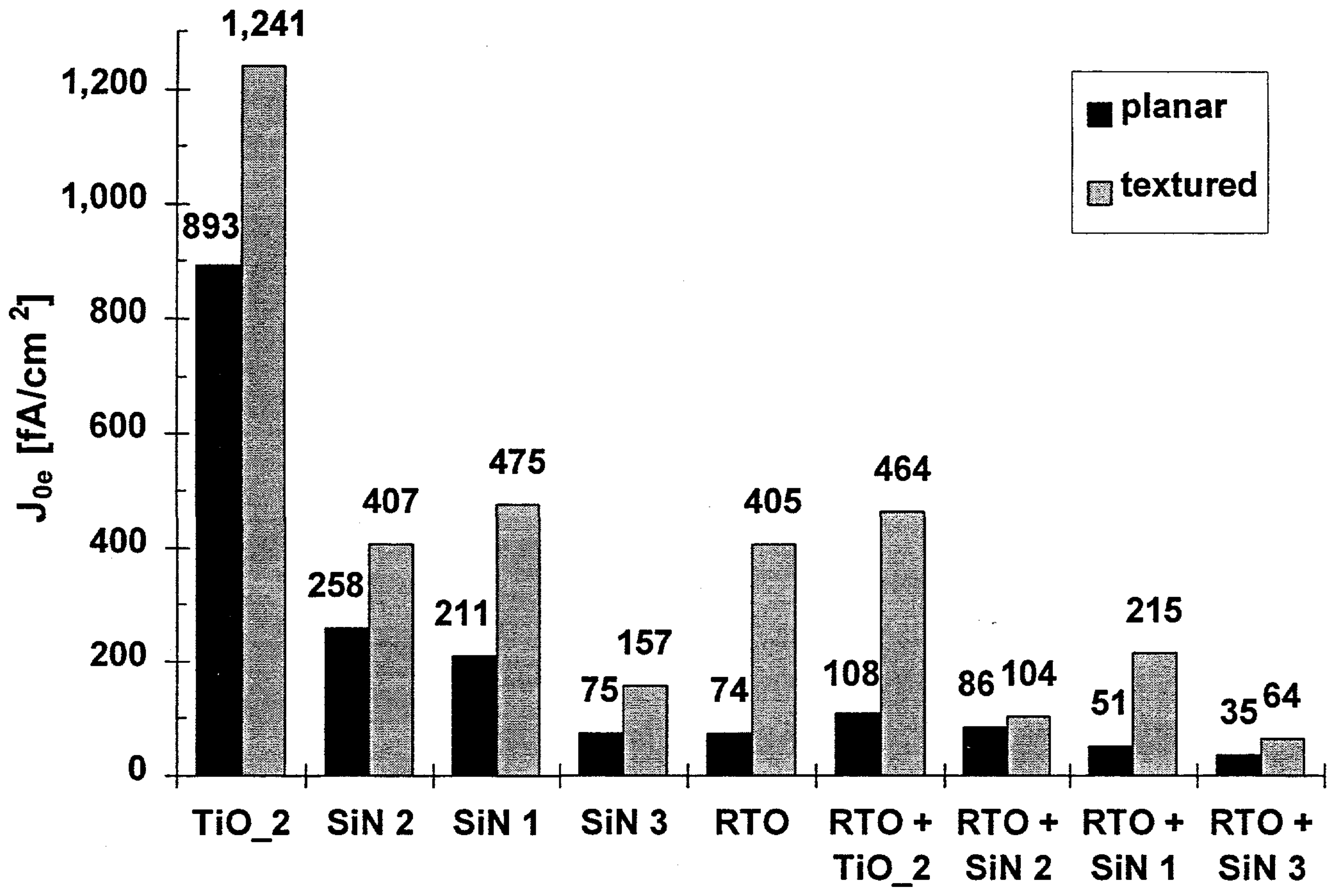

Fig. 2.2. Emitter saturation current densities for 90 Ω/sq. RTP emitters.

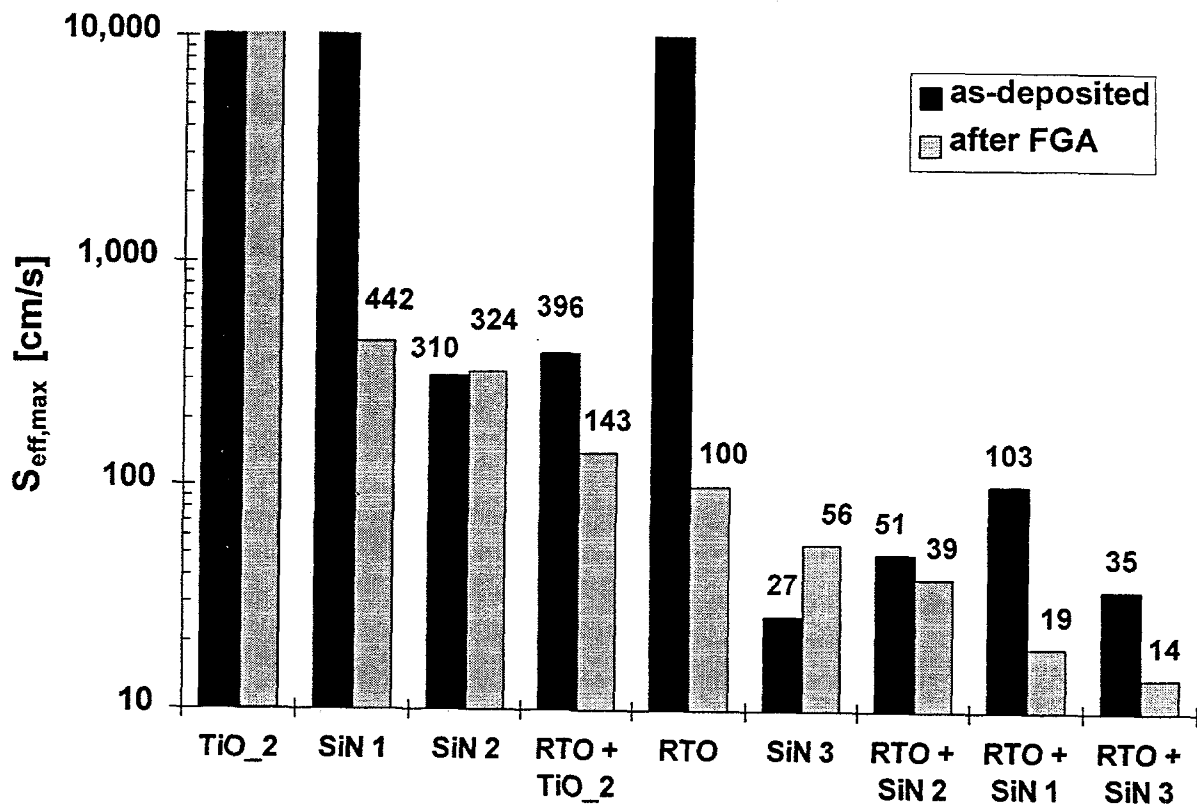

Fig. 2.3. Maximum surface recombination velocities for different passivation schemes on planar surfaces. S values above 10^4 cm/s cannot be resolved by the measurement technique used and are not shown.

3 Effective Passivation of the Low Resistivity Silicon Surface by a Rapid Thermal Oxide/Plasma Silicon Nitride Stack

3.1 Introduction

Low surface recombination velocity (S) is an important requirement for the performance of many semiconductor devices. For silicon solar cells, the recombination velocity at the front and rear surfaces (S_f and S_b, respectively) must be reduced in order to achieve high-efficiency. Moreover, the techniques by which S_f and S_b are reduced should be compatible with high-throughput, low-cost fabrication. S_b reduction is generally accomplished for p-type substrates by forming an aluminum or boron back surface field (BSF). Even though such BSFs can lead to low S_b,[1,2] there are disadvantages associated with each. For example, stresses imparted to the Si substrate during aluminum BSF formation preclude application to thin wafers, and lengthy diffusion times required to form deep boron BSFs reduce compatibility with high throughput processing.

Surface passivation by a dielectric film provides an alternative to BSF design. However, traditional methods of growing a high quality thermal SiO_2 layer in a conventional furnace are not consistent with low-cost solar cell fabrication.[3] Alternatively, silicon nitride (SiN) films deposited by plasma enhanced chemical vapor deposition (PECVD) have been shown to provide excellent passivation of the low resistivity p-type Si surface.[4] However, the passivation quality of SiN films can vary greatly with deposition conditions, plasma reactor design, and post-deposition annealing. For example, reports show that high frequency direct PECVD SiN deposited on low-resistivity Si at 300°C can result in S values as low as 30 cm/s[5] or as high as 20,000 cm/s.[6] The former films showed an increase in S after a low temperature post-deposition anneal in forming gas, whereas the later films showed an improvement in passivation after a similar treatment. Since industrial solar cells undergo a moderate thermal anneal in order to fire the screen-printed device contacts (>700°C and typically the final step in processing), it is imperative that a potential passivation scheme be compatible with this heat treatment.

In this paper, we report the use of a dielectric stack comprised of SiO_2 grown by rapid thermal processing (RTP) and SiN deposited by the PECVD technique for effective passivation of the low

resistivity p-type (100) Si surface. Not only does this passivation scheme withstand a moderate heat treatment (>700°C), it relies on such a treatment to achieve very low S values. Compatibility with post deposition annealing makes this passivation scheme attractive for high-efficiency, high-throughput solar cell fabrication.

3.2 Experimental

P-type (100), 1.25 Ω-cm, 300 μm thick, float zone (FZ) wafers were used in this study to monitor surface passivation. The as-received wafers were chemically polished (*not* mirror-mechanically polished). Prior to rapid thermal oxide (RTO) growth and/or SiN deposition, the wafer surfaces were prepared with the following chemical treatment: dip in 2:1:1 H_2O:H_2O_2:H_2SO_4 for 5 minutes, etch in 15:5:2 HNO_3:CH_3COOH:HF for 2 minutes, dip in 2:1:1 H_2O:H_2O_2:HCl for 5 minutes, and dip in 10:1 H_2O:HF for 2 minutes. Between each step, the wafers were thoroughly rinsed in deionized water. The RTO layers were grown in an RTP unit (AG Associates 610) at 900°C in less than 5 minutes. PECVD SiN films were deposited in a direct, high-frequency (13.5 MHz), parallel-plate reactor (Plasma-Therm) at 300°C in 6-7 minutes. Ensuing thermal treatments (simulating screen-printed contact firing) were carried out in beltline furnace (Radiant Technology Corp.) in which samples are heated by tungsten-halogen lamps. The total anneal time in the beltline was fixed at 2 minutes, and samples were exposed to a peak firing temperature of 730°C for only 30 seconds.

The passivation quality of each scheme was monitored by the transient photoconductance decay (PCD) technique. The effective lifetimes measured by PCD were converted to S values using a conventional analysis method.[7] In this paper, all S values are calculated assuming an infinite minority carrier bulk lifetime. The resulting S values are therefore maximum or "worst-case" limits.

3.3 Results and Discussion

The passivation quality of an RTO layer grown at 900°C is shown in Figure 3.1 as a function of injection level in the 10^{14}-10^{15} cm^{-3} range. The as-grown oxide results in S greater than 10,000 cm/s (not plotted in Figure 3.1) which is reduced to approximately 100 cm/s by an anneal in forming gas

at 400°C. However, an ensuing 730°C beltline anneal degrades the passivation and increases S to greater than 1000 cm/s.

A similar trend is observed in this study for the PECVD SiN film *alone* (Figure 3.2). The as-deposited SiN results in S greater than 10,000 cm/s which is reduced to less than 200 cm/s by an ensuing anneal in forming gas at 400°C. (The high S value for the as deposited film and the improvement after forming gas annealing are both consistent with the results of Refs. 6 and 8 in which a similar high-frequency, direct SiN was studied. However, there is a lack of agreement with the results of Ref. 5 in which the as-deposited SiN film results in very low S and subsequent low temperature forming gas annealing increases this value. Again, differences in the passivation behavior of seemingly analogous films are believed to arise from variations in reactor design and deposition conditions.) The effect of the 730°C beltline anneal is also shown in Figure 3.2. Again, the heat treatment degrades the interface quality, and increases S by roughly one order of magnitude.

Clearly, the two passivation schemes shown above (RTO alone or PECVD SiN alone) are not compatible with high-throughput solar cell fabrication since neither can effectively withstand a screen-printed contact firing cycle without significant degradation in S. However, contrary to the response of the individual films, annealing the RTO/PECVD SiN *stack* actually enhances the passivation quality. The effect of stacking PECVD SiN on top of the RTO layer and then annealing at 730°C is shown in Figure 3.3. The S value attained after the final anneal (Step 3 in Figure 3.3) is clearly superior to the RTO growth (Step 1) or the SiN deposition on top of the oxide layer (Step 2). The 730°C anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO_2 interface, thus reducing the density of states at the surface. Also evident is the weak injection level dependence of S within the measurement range (10^{14}-10^{15} cm^{-3}). This behavior is quite different than that reported for the highest quality remote SiN films where S increases by a factor of 5 as the injection level falls from 10^{15} to 10^{14} cm^{-3}.[4]

It is important to note that the final S value achieved after the 730°C firing of the stack is the same whether or not a forming gas anneal is used as an intermediate step following oxidation (Figure 3.4). This indicates that the SiN film is indeed supplying all the hydrogen needed to reduce S to such low levels. *Maximum* S values of 11 cm/s and 20 cm/s are achieved by the stack passivation on the surfaces of 1.25 Ω-cm and 0.65 Ω-cm material, respectively. These are among

the lowest S values ever reported for solid film passivation of the low-resistivity Si surface. Moreover, these S values are significantly lower than those attained by either the RTO or PECVD SiN alone, even after the individual films are annealed in forming gas (Figures 3.1 and 3.2).

The initial RTO growth temperature is observed to have an effect on the final S value of the annealed stack. In Figure 3.5, the stack progression is shown for RTO layers grown at 850°C and 900°C. In both cases, low S values (<40 cm/s) are attained after the 730°C anneal. However, the initial 900°C RTO SiO_2 growth clearly results in lower S (aforementioned 10-20 cm/s). In the past, higher RTO growth temperatures have been observed to improve the SiO_2-Si interface quality by limiting the interface width[9] and reducing the suboxide bonding arrangement.[10]

In conclusion, it is shown that an RTO/PECVD SiN stack, along with a short 730°C anneal, can be used to attain S values nearing 10 cm/s on the 1.25 Ω-cm p-type silicon surface. These S values are achieved by the stack even when passivation by the individual films degrades after annealing. Inability of the individual films to maintain low S values after moderate heat treatments precludes application to low-cost, high-efficiency solar cells which require effective surface passivation and screen-printed contact firing between 700°C-800°C. On the contrary, the stack passivation is ideally suited for high-throughput processing, and can be utilized to form cost-effective bifacial solar cells.

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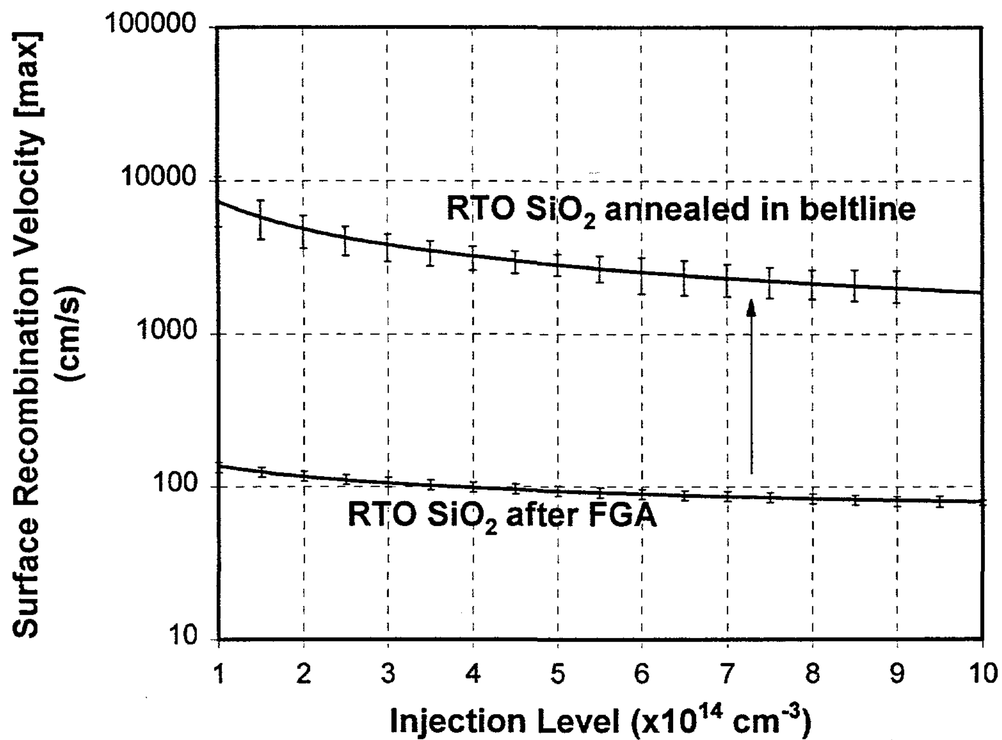

Figure 3.1. Passivation of the 1.25 Ω-cm p-type (100) Si surface by RTO SiO_2 alone. The RTO was done at 900°C in 5 minutes (≈ 79Å), and the ensuing forming gas anneal (FGA) was done at 400°C in 15 minutes.

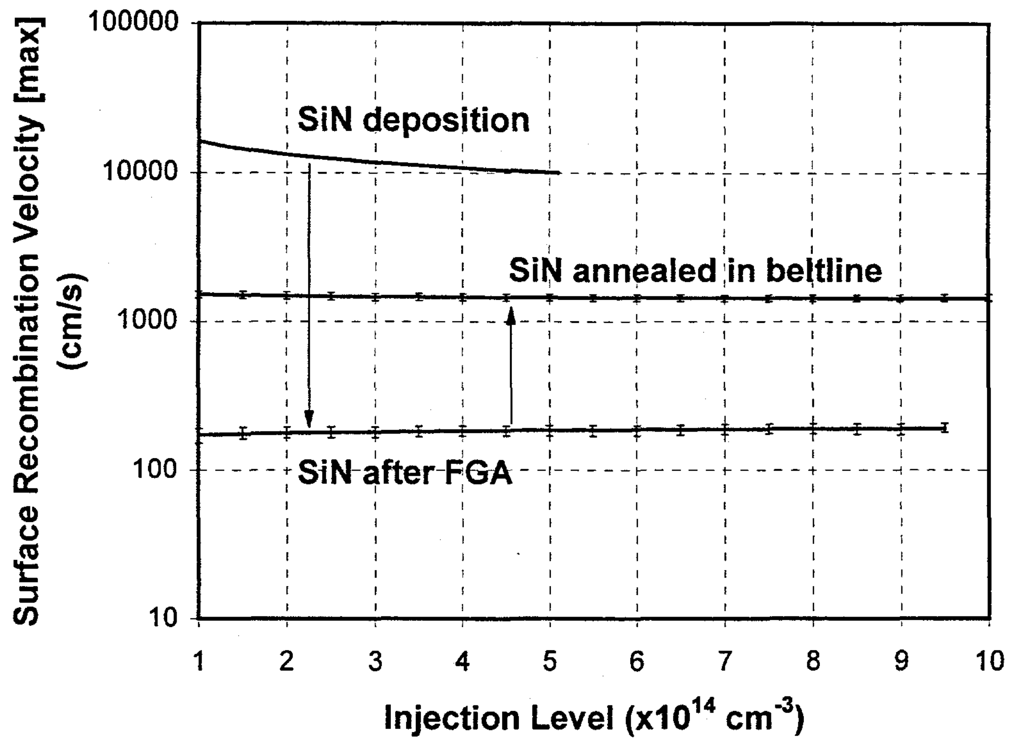

Figure 3.2. Passivation of the 1.25 Ω-cm p-type (100) Si surface by SiN alone. The FGA was done at 400°C in 30 minutes.

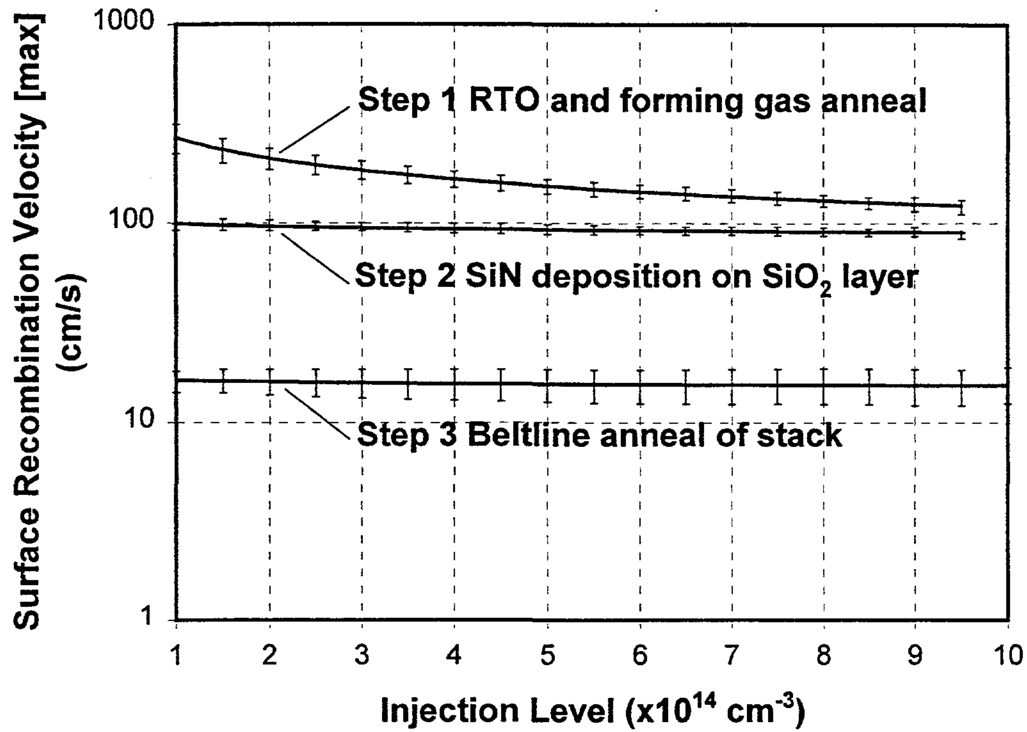

Figure 3.3. Progression of S values for passivation by the RTO SiO_2/PECVD SiN stack. SiO_2 films (≈ 57Å) were grown at 900°C in 2 minutes, and the ensuing FGA was done at 400°C in 15 minutes.

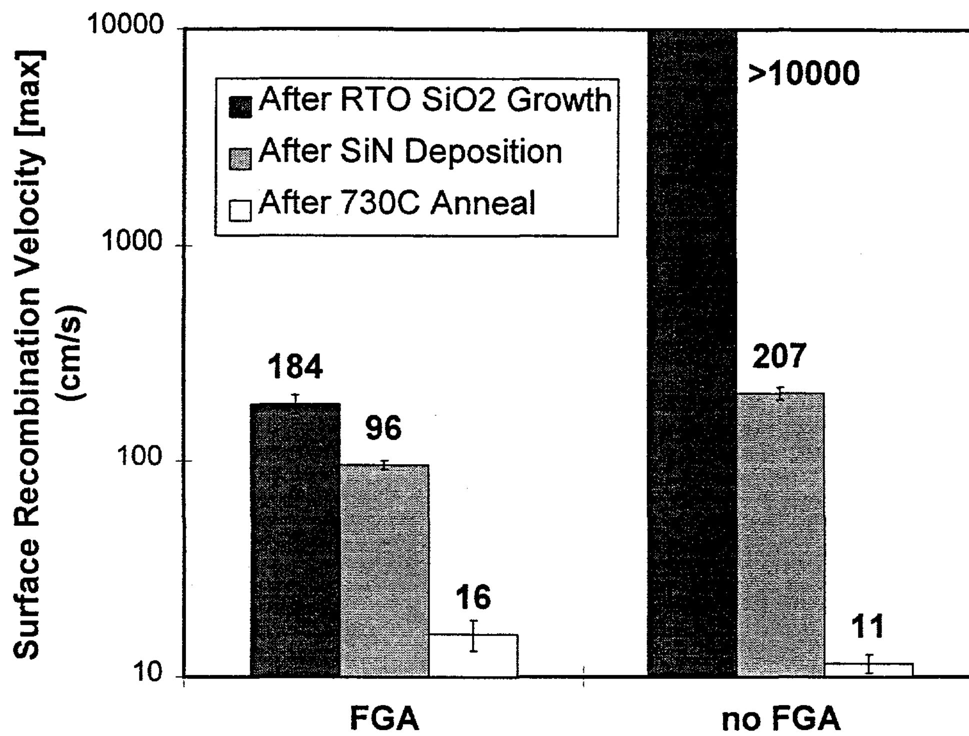

Figure 3.4. Effect of intermediate FGA (immediately after RTO growth) on the stack passivation. RTO films were grown at 900°C in 2 minutes, and the FGA was done at 400°C in 15 minutes.

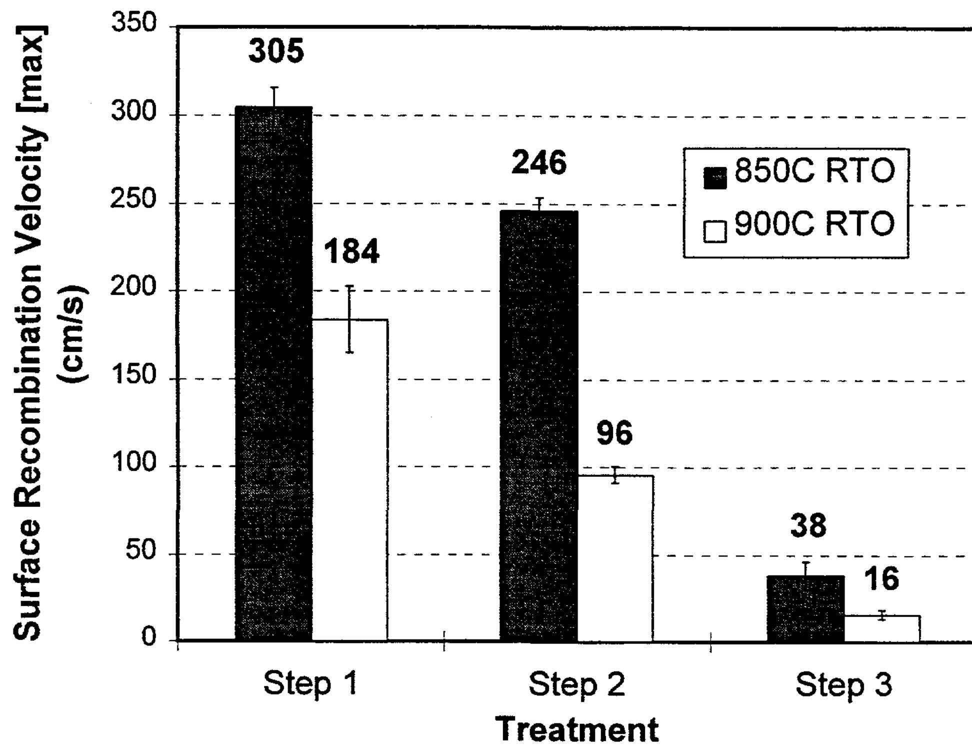

Figure 3.5. Effect of RTO temperature on the stack passivation. Step 1: 2 minute RTO growth (≈43Å at 850°C, ≈57Å at 900°C) followed by FGA at 400°C in 15 minutes, Step 2: SiN deposition on RTO layer, Step 3: 730°C anneal of stack.

4 An Optimized Rapid Aluminum Back Surface Field Technique for Silicon Solar Cells

4.1 Introduction

The back surface recombination velocity (S_b) begins to strongly influence solar cell performance when the ratio of minority carrier diffusion length to device thickness approaches or exceeds unity. Single crystalline Si typically falls into this category, and multicrystalline growth techniques have improved to the point where "cm-scale" grain sizes with long intragrain diffusion lengths are common. Furthermore, the cost-advantage associated with reduced Si consumption has led photovoltaic (PV) manufacturers to implement thinner substrates. When the solar cell thickness is reduced, the influence of S_b on device performance is felt more strongly. These observations emphasize the need to reduce S_b in commercially available solar cells.

A robust structure capable of reducing S_b is the back surface field (BSF), or high-low junction. This region acts to transform the true S_b into an effective recombination velocity (S_{eff}) at the BSF junction edge [1,2,3,4,5,6,7,8]. Commonly implemented on p-type substrates is the aluminum-alloyed BSF (Al-BSF). The Al-BSF is attractive because the p^+ region is formed by metal-Si alloying instead of dopant diffusion. As a result, BSF formation can be accomplished very quickly (within seconds or minutes) and at moderate temperatures (<900°C). This provides a distinct advantage over, for example, a deep p^+ boron BSF that requires a lengthy (≈ 1 hour), high-temperature (≈ 1000°C) diffusion step in order to achieve low S_{eff} [9,10].

In general, BSF action improves with increasing junction depth and doping level. A theoretical treatment of the Al-BSF based on the Al-Si phase diagram reveals that: 1) the junction depth is primarily determined by the amount of Al initially deposited onto the Si substrate, and 2) the doping level is determined by the peak alloying temperature [11]. The greater the thickness of deposited Al, the deeper the resulting BSF junction. Similarly, the higher the alloying temperature, the more heavily doped the p^+ region.

A limited number of experimental studies have attempted to quantify these theoretically expected relationships. In [11], del Alamo et. al. investigated the effect of peak alloying temperature (in the range of 650°C-825°C) on Al-BSF quality. While a weak relationship between S_{eff} and alloying temperature was observed, the lowest S_{eff}'s attained were not consistent with the

requirements for high-efficiency solar cells. The authors indicated that the limitation was due mainly to the deposition of thin Al films (≈ 1 m) prior to BSF alloying. In [12], Amick et. al. investigated the effect of the initial Al thickness on BSF action. Screen printing was used to deposit thick and (relatively) thin Al films onto solar cell samples. After alloying, the resulting BSF junction depths were measured by the spreading resistance technique to be in excess of 10 m. However, the impact of these deep p^+ regions on solar cell V_{oc} was minimal, increasing V_{oc} by only ≈ 5mV for 2 Ω-cm substrate Si. Moreover, the cells were not characterized to determine the impact of the Al thickness on S_{eff}. In [13], Lolgen et. al. used photoconductance decay analysis to measure S_{eff} values below 200 cm/s (on 3 Ω-cm Si) for screen-printed Al layers alloyed in a belt furnace. However, when the same Al-BSFs were applied to cells, efficiency improvements concomitant with the expected S_{eff} reductions were not evident [14]. This was partly attributed to the use of substrates with low minority carrier diffusion lengths. It is evident from these studies that the effects of basic BSF formation conditions have not been established to a high degree of confidence.

Another important factor that affects Al-BSF electrical quality, one that is not considered in the studies mentioned above, is junction uniformity. In [15,16], Roberts and Wilkinson discussed the factors that influence the uniformity of alloyed metal-Si junctions. They indicated that the ramp-rate used to reach the peak alloying temperature should have a significant impact on the resulting smoothness of the interface. This effect was later observed, in qualitative terms, for the Al-Si system in [17]. However, no study has analyzed the effect of junction uniformity on Al-BSF electrical quality and the resulting solar cell efficiency.

The goal of this work is therefore to: 1) understand the impact of Al-BSF uniformity on S_{eff} and cell performance, and develop processes that suppress junction non-uniformity, 2) establish from fundamental considerations an effective, high-throughput Al-BSF formation process, and 3) integrate this optimized Al-BSF into solar cell formation sequences to demonstrate high-efficiency. The main Al-BSF formation parameters (Al deposition quantity, alloying temperature, and furnace ramp-rate) are considered in detail. Industrially viable process techniques such as screen-printing, rapid thermal processing (RTP), and beltline alloying are analyzed in terms of their impact on BSF quality and cell performance.

4.2 Al-BSF Formation Issues

4.2.1 Theoretical Modeling: Effects of Temperature and Al Deposition Quantity

Al-BSF formation occurs in four steps: 1) Al deposition onto the rear Si surface, 2) alloying above the Al-Si eutectic temperature (577°C), 3) cooldown and epitaxial regrowth of the p^+ BSF, and 4) final solidification at the eutectic temperature. In general, the *opacity* of a BSF can be improved by increasing the junction depth and/or the p^+ doping level. A rudimentary analysis of the Al-Si binary phase diagram reveals that the Al-BSF *junction depth* is increased by either depositing thicker layers of Al onto the Si substrate or by alloying at higher temperatures, and the *doping level* is increased solely by raising the alloying temperature. The expected junction depth can be written explicitly in terms of process parameters:

$$W_{BSF} = \frac{t \cdot \rho_{Al}}{\rho_{Si}} \left(\frac{F(T)}{1 - F(T)} - \frac{F(T_o)}{1 - F(T_o)} \right) \qquad (1)$$

where t represents the thickness of the deposited Al layer, ρ_{Si} and ρ_{Al} are the densities of Si and Al, *F(T)* represents the Si atomic weight percentage of the molten phase at the peak alloying temperature, and $F(T_O)$ represents the Si atomic weight percentage at the eutectic temperature (≈ 12.2% for the Al-Si binary system) [11]. Applying this phase diagram analysis, the characteristic retrograde profile of an Al-BSF can be constructed and analyzed numerically to determine the change in S_{eff} expected for variations in Al deposition quantity and alloying temperature. The results of such an analysis are plotted in Fig. 4.1 for Al-BSFs on 2.3 Ω-cm Si. The model predicts that increasing the alloying temperature in intervals of 50°C (between 800°C-1000°C) should only reduce S_{eff} by a modest factor of 1.5 per interval. In contrast, increasing the Al deposition quantity from 1 to 10 μm should reduce S_{eff} by nearly one order of magnitude. Clearly, S_{eff} reduction can be achieved more readily by going to thicker Al deposition instead of higher alloying temperatures. It must be noted, however, that this simplistic treatment offers only general guidelines for Al-BSF design. It fails to consider another aspect of the BSF structure that has a significant impact on the electrical performance: *junction uniformity*.

4.2.2 *Effect of Ramp-Rate on Al-BSF Uniformity*

The uniformity of an Al-BSF is controlled to a large extent by the ramp-up rate used to reach the alloying temperature. Under slow ramp conditions, alloying between Al and Si can occur at certain sites before others (a form of *local wetting*), which leads to non-uniformities in the resulting Al-BSF [15]. These non-uniformities can include variations in junction depth, loss of surface planarity, spiking, and even non-formation of the p^+ region. Under fast ramp conditions, the sample goes through the eutectic point and reaches the process temperature very quickly. At typical process temperatures (≈ 800-900°C), the Al layer becomes molten and readily wets the entire Si surface. This promotes uniform alloying, and in turn, leads to more uniform Al-BSF regions.

Fig. 4.2 shows SEM micrographs of Al-alloyed p^+ junctions formed under slow ramp and fast ramp conditions. In both cases, 10 μm of Al was thermally evaporated onto the Si substrates before alloying at 850°C. The sample undergoing the slow ramp process was pushed into a conventional furnace below the Al-Si eutectic temperature and ramped-up at a rate of 5°C/min. The sample undergoing the fast ramp procedure was processed in an RTP unit (AG Associates 610) and ramped-up at a rate of 1200°C/min. After processing, the p^+ regions were delineated by etching the samples in an acid solution [18].

As evident from Fig. 4.2, the slow ramp process results in an extremely non-uniform, discontinuous p^+ junction. On the contrary, the sample alloyed under fast ramp conditions shows a higher degree of junction uniformity and planarity. It is important to note, however, that while BSF uniformity is promoted by fast ramp alloying, the creation of non-uniformities can not be totally suppressed. Even under fast ramp conditions, Al-BSF junction depth variation can be significant (as high as 50% across the wafer). This effect has also been observed in a previous study on rapid Al-Si alloying [17]. Furthermore, it has been suggested that junction uniformity can be influenced by the type of heating element (halogen lamp versus graphite heater) used in the RTP unit [19]. These observations call into question the accuracy of relying on measured p^+ junction profiles to calculate S_{eff}. A more accurate method would be to analyze a finished solar cell and extract S_{eff} by a combination of internal quantum efficiency (IQE) measurements and device simulation.

The effects shown in Fig. 4.2 have a profound impact on the performance of solar cells formed on materials in which the minority carrier diffusion length exceeds the cell thickness. Fig. 4.3 shows the resulting V_{oc} change for solar cells fabricated on 2.3 Ω-cm FZ Si with Al-BSFs formed under

slow and fast ramp conditions. For each case except the *baseline* cell, 10 μm of Al was evaporated onto the back of the sample prior to alloying at 850°C. (The baseline BSF process refers to evaporation of 0.5 μm of Al followed by fast ramp alloying at 850°C. As a result of this thin deposition, an ineffectual BSF is formed, and the V_{oc} approaches the value limited by high S_b.) Each data point in Fig. 4.3 represents the average of nine 4 cm^2 cells fabricated from a 100 mm diameter wafer. All wafers were selected from the same ingot of float zone (FZ) Si. In order to minimize experimental variation, non-comparative process steps (i.e. emitter formation, emitter surface passivation, contact formation, and AR coating application) were done simultaneously. A detailed process sequence for these high-efficiency laboratory cells is given in Section 4.1.

Predictions based solely on the Al-Si phase diagram would require all cells in Fig. 4.3 to exhibit the same S_{eff} (and therefore the same V_{oc}) since the Al deposition quantity and peak alloying temperature are the same for each. Clearly this is not the case as Al-BSFs formed with differing ramp-rates exhibit significantly different device performance. IQE plots in Fig. 4.4 reveal that the change in V_{oc} observed for varying ramp-rates is indeed due to differences in S_{eff}. Long wavelength IQE in this spectral range (800-1100 nm) is a function of both bulk lifetime (τ_b) and S_{eff}. For high-lifetime material, such as the 2.3 Ω-cm FZ Si used in this study, the IQE is invariant to small perturbations in τ_b and responds only to changes in S_{eff}. Also shown in Fig. 4.4 are long wavelength IQE simulations generated using *PC1D-4* [20] for an analogous device with S_{eff} values ranging from 10^4 cm/s to 10^2 cm/s. By simple comparison, it is clear that the S_{eff} of the Al-BSF is reduced by nearly one order of magnitude by changing from slow to fast ramp process conditions.

4.2.3 Effect of Al Deposition Thickness and Alloying Temperature on Al-BSF Quality

Fig. 4.5 shows that the positive effect of increased Al deposition thickness on BSF quality (predicted theoretically by Al-Si phase diagram analysis) occurs only when fast-ramp alloying is implemented. Under such conditions, V_{oc} improvements in excess of 25 mV can be achieved by increasing the Al deposition thickness from 1 to 10 μm for 2.3 Ω-cm FZ Si. Under slow ramp alloying conditions, the same correlation between deposition quantity and BSF action is severely diminished.

The other variable in the Al-BSF formation process is the alloying temperature. As the BSF alloying temperature is increased, it is expected that both the p^+ region doping level and junction

depth also increase. Again, the analysis in Fig. 4.1 indicates that S_{eff} should drop by a factor of 1.5 for every 50°C increase in alloying temperature between 800°C and 1000°C. To verify this prediction, p^+ Al alloyed junctions were formed and profiled using the electrochemical CV measurement technique. The junctions were formed by thermally evaporating 10 μm of Al onto p-type Si and then alloying by RTP at temperatures between 800-1000°C. The results (Fig. 4.6) are consistent with the theoretical *trend* expected for the alloying temperature effect.

To determine whether the same trend is observed for solar cells, a series of devices was fabricated with Al-BSFs alloyed at 850°C, 900°C, and 950°C in the RTP unit. The results in

show that the temperature variation actually has little effect on cell performance. Furthermore, IQE measurements of the same devices reveal almost no variation in the long wavelength response which indicates nearly the same S_{eff} behavior for all samples. This apparent discrepancy between CV profiles and cell performance can be understood on the basis of the microscopic non-uniformities (etch pits, Al inclusions, etc.) present in even Al-BSFs formed under fast ramp conditions. SEM analysis of the BSF surfaces reveals their existence. The BSF effect is strongly tempered by these features, and the relatively small V_{oc} variation in

is attributed to their presence. On the contrary, the CV technique measures across a fairly large sample area (≈ 7mm^2). The profiles are therefore not significantly affected by the microscopic non-uniformities in the p^+ region.

4.3 Assessment of Screen-Printed Thick Al Films for BSF Application

As shown in Fig. 4.5, thick film Al deposition is a critical requirement for effective Al-BSF formation. However, thick Al deposition by evaporation is inappropriate for large scale cell production. Screen-printed (SP) Al has been widely implemented in Si photovoltaics as a low-cost, high-throughput precursor to Al-BSF formation [21,22].

The Al quantity deposited onto a wafer during screen-printing depends on the rheology of the conductor paste as well as the Al content. In this study, a commercially available Al conductor paste (*FX-53-038* from Ferro Corp.) was used. Printing was accomplished using a screen with 325 wires per inch, wire diameter of 0.9 mil, and emulsion thickness of 1 mil. With these conditions, a typical print results in the deposition of 4.10 mg/cm^2 of Al (corresponding to an *effective* Al thickness of 15 μm). SEM analysis of samples printed with Al and alloyed at 850°C in an RTP unit (Fig. 4.7)

reveals cleanly formed, deep BSF junctions (≈ 6 μm) with a noticeable variation in junction depth. In spite of this junction depth variation, the deep p^+ regions are consistent with the requirement for effective BSF action.

The primary concern associated with screen-printing is possible contamination introduced into the wafer by the Al paste during high temperature alloying. Unlike the high purity Al used for the thermal evaporation studies (99.999%), the conductor paste is formed from lower purity Al (99.7%) in which the chief contaminant is Fe. At elevated process temperatures, a fast-diffusing impurity like Fe can segregate into the bulk and degrade τ_b throughout the device [23].

The effect of contamination was monitored by measuring the performance of cells with SP Al-BSFs alloyed between 850°C-1000°C. The results (Fig. 4.8) indicate that the cell performance degrades at temperatures above 850°C. V_{oc} reduction is most severe when the alloying temperature is raised to 1000°C. Long wavelength IQE analysis of these cells shows that the degradation is primarily due to a drop in τ_b. However, at 850°C there is no appreciable sign of bulk contamination in these FZ wafers, and the resulting high IQE response in the long wavelength (≈ 90% at 1000 nm) is indicative of low S_{eff}.

4.4 Incorporating the Screen-Printed/RTP Alloyed Al-BSF into Solar Cell Processes

In order to quantify the effects on solar cell performance, the optimal Al-BSF process conditions discussed above (thick film deposition by screen-printing, RTP fast ramp alloying, and the maximum tolerable alloying temperature) were integrated into two solar cell processes: 1) a high-efficiency laboratory process and 2) a high throughput industry-type process. The results are presented in the following two subsections.

4.4.1 High-Efficiency Laboratory Process

The high-efficiency laboratory process is listed in **Error! Reference source not found.**. The key features are a light emitter diffusion (90 Ω/sq), thin thermal oxide emitter passivation, front contact formation by vacuum evaporation and lift-off, and double layer AR coating application. Various Al-BSF structures were implemented on the rear surface. The effect of both Al deposition thickness and

heating rate were examined. The trend in performance (Table 4.3) is entirely consistent with the results in Fig. 4.5. Thick film Al deposition and fast ramp alloying are *both* required to achieve the highest cell performance. Moreover, the data shows that the lengthy 10 μm Al evaporation step can be completely replaced by high-throughput screen-printing without any loss in cell performance. Noteworthy efficiencies of 19%-20% are shown for 2.3 Ω-cm Si by utilizing the SP/RTP Al-BSF. This represents an efficiency improvement of ≈1.5% (absolute) over cells with Al-BSFs formed inappropriately by either slow ramping or thin Al deposition.

4.4.2 High-Throughput Industry-Type Process

The SP/RTP Al-BSF was next incorporated into a high-throughput, industry-type process sequence. The key features of this process are a heavier emitter diffusion (45 Ω/sq), plasma SiN emitter passivation (which also serves as a single layer AR coating), and front contact formation by screen-printing. A step-by-step comparison of this sequence to the high-efficiency laboratory process is given in **Error! Reference source not found.**. In addition to RTP alloying, beltline furnace alloying was also applied to BSF formation. Beltline processing is widely used in the commercial PV sector for various solar cell processes (i.e. for emitter diffusion, contact firing, and Al-BSF formation) [24]. In this study, the effects of specific beltline alloying treatments on S_{eff} and cell performance have been analyzed quantitatively.

A schematic of the 3-zone beltline furnace (Radiant Technology Corp.) used in this study is shown in Fig. 4.9. In each zone, the energy source for heating is provided by a bank of tungsten-halogen lamps. Three different beltline thermal cycles (also depicted in Fig. 4.9) were investigated for their ability to form Al-BSFs. These were: 1) a step-up in temperature from 425°C in Zone 1 to 730°C in Zone 3, 2) a step-up in temperature from 550°C in Zone 1 to 850°C in Zone 3, and 3) all zones set to 850°C. The relevance of each cycle is explained below.

Cycle 1 represents a typical front contact sintering recipe. It was included to determine the feasibility of co-firing the Al-BSF with the screen-printed front Ag contact. *Cycle 2* is a variation of Cycle 1 in which the temperature is ramped up to 850°C, a more appropriate setting for Al-BSF alloying. In *Cycle 3*, all three zones were set to 850°C so the sample could be exposed to high temperature immediately upon entering the furnace. As such, Cycle 3 most closely simulates the RTP fast ramp condition. In all experiments, the beltspeed was fixed at 15 inches/minute to

maintain a total process time of 2 minutes. The effect of each thermal cycle on cell performance and long-wavelength IQE was measured, and the results are shown in Table 4.4 and Fig. 4.10.

Application of Cycle 1 results in the poorest long-wavelength IQE response corresponding to an S_{eff} of $>10^4$ cm/s and the lowest device efficiency of 15.2%. (As in Section 2.2, S_{eff} extractions were made by fitting the measured IQE response to theoretical spectra calculated using *PC1D-4*. In all cases, the τ_b required to accomplish the simulation was assumed to be very high. This assumption yields conservative or "worst-case" S_{eff} value.) The poor response of Cycle 1, expected due to the slow ramp temperature profile and low peak alloying temperature, indicates that an effective Al-BSF is difficult to form simultaneously during the front contact sintering cycle. This result is significant since many PV manufacturers choose to co-fire the Al-BSF with the front Ag contacts. Similar results are observed for Cycle 2 because of the slow ramp condition. However, application of Cycle 3, which most closely simulates an RTP fast ramp condition, results in a significant performance improvement over the other two treatments. The S_{eff} for this process is reduced to 10^3 cm/s, and the average device efficiency is improved to 16.3%. In spite of this improvement, Fig. 4.10 shows that the RTP process still results in the best long-wavelength IQE corresponding with an S_{eff} of 200 cm/s and a device efficiency of 17.0%. This result is noteworthy considering the simplicity of the fabrication process (no high temperature oxidation for surface passivation, front and rear metallization by screen-printing, and a single layer AR coating only).

Additional increases in cell efficiency were achieved by incorporating improved light trapping features into the device design. Cell efficiencies of 17.5% (V_{oc}=623mV, J_{sc}=35.4 mA/cm^2, FF=0.793) and 17.6% (V_{oc}=616mV, J_{sc}=37.3 mA/cm^2, FF=0.770) have been officially verified for planar and textured devices, respectively, on 2.3 Ω-cm FZ Si with a SiN/MgF_2 double layer AR coating. These efficiency values clearly demonstrate the beneficial effect of optimally formed Al-BSFs on device performance.

4.5 Conclusions

The conditions required to form optimal Al-BSF regions have been established by a combination of theoretical modeling and detailed experimentation. For the first time, treatment of the Al-BSF has been extended to include the effects of junction uniformity on BSF action. Model calculations indicate that the S_{eff} of an Al-BSF is more readily improved by increasing the initial Al deposition

thickness (from 1μm to 10μm) rather than increasing the alloying temperature (by 50°C between 800-1000°C). Experimental results show that this theoretical prediction is accurate only when RTP fast ramp rates are used to promote BSF uniformity. By combing thick film Al screen-printing and fast ramp RTP alloying at 850°C, Al-BSFs exhibiting S_{eff} as low as 200 cm/s have been achieved on 2.3 Ω-cm Si. Integrating this SP/RTP Al-BSF into a high efficiency laboratory fabrication sequence has resulted in Si solar cell efficiencies of 19-20%. The same BSF process applied to a high-throughput, industrial-type sequence has resulted in 17.0% efficient single layer (silicon nitride) AR coated cells and 17.5% efficient double layer (SiN/MgF_2) AR coated devices. Al-BSF alloying in a beltline furnace, though somewhat less effective than RTP alloying, can still results in reasonable BSF action if: 1) an appropriate alloying temperature (≈850°C) is used and 2) the fast-ramp condition is properly simulated.

4.6 References

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Table 4.1. Effect of alloying temperature on Al-BSF solar cell V_{oc}. All samples (except the baseline case) were formed by 10μm Al evaporation followed by RTP fast ramp alloying. Each data value represents the average of nine 4 cm^2 cells taken from a wafer.

Alloying Temperature	V_{oc} **(mV)**
Baseline Process	606
850°C	632
900°C	632
950°C	636

Table 4.2. Process sequence comparison: high-efficiency laboratory process and high-throughput industry-type process. *SP* represents screen-printing.

Step	Lab Process	Industrial Process
1	n^+ Diffusion (90 Ω/sq)	n^+ Diffusion (45 Ω/sq)
2	Thermal Oxide Passivation	PECVD SiN Pass. and SLAR
3	SP or Evap Al/ RTP Alloy	SP Al/ RTP or Beltline Alloy
4	Contacts (Photolithography)	Contacts (Screen Printing)
5	Double Layer AR	

Table 4.3. Al-BSF solar cells formed using a high-efficiency, laboratory fabrication sequence. All results have been officially verified at Sandia National Labs. (Cell area: 4 cm^2)

BSF Formation	Res. (Ω-cm)/ Surface	V_{oc} (mV)	Jsc (mA/cm^2)	Eff (%)
Baseline	2.3 Planar	606	36.4	17.4
10μm Evap Al Slow Ramp Alloy	2.3 Planar	612	35.9	17.4
10μm Evap Al RTP Alloy	2.3 Planar	632	37.6	19.0
Screen Printed Al RTP Alloy	2.3 Planar	637	37.4	19.1
Screen Printed Al RTP Alloy	1.3 Textured	634	38.5	19.8

Table 4.4. Average performance of Al-BSF solar cells formed using a high throughput, industry-type fabrication sequence. (Cell area: 4 cm^2)

Cell Type	Res. (Ω-cm)	V_{oc} (mV)	Jsc (mA/cm^2)	Eff (%)
Beltline Alloying Cycle 1	2.3 Planar	597	32.7	15.2
Beltline Alloying Cycle 3	2.3 Planar	614	34.2	16.3
RTP Alloying Fast Ramp 850°C	2.3 Planar	625	35.1	17.0

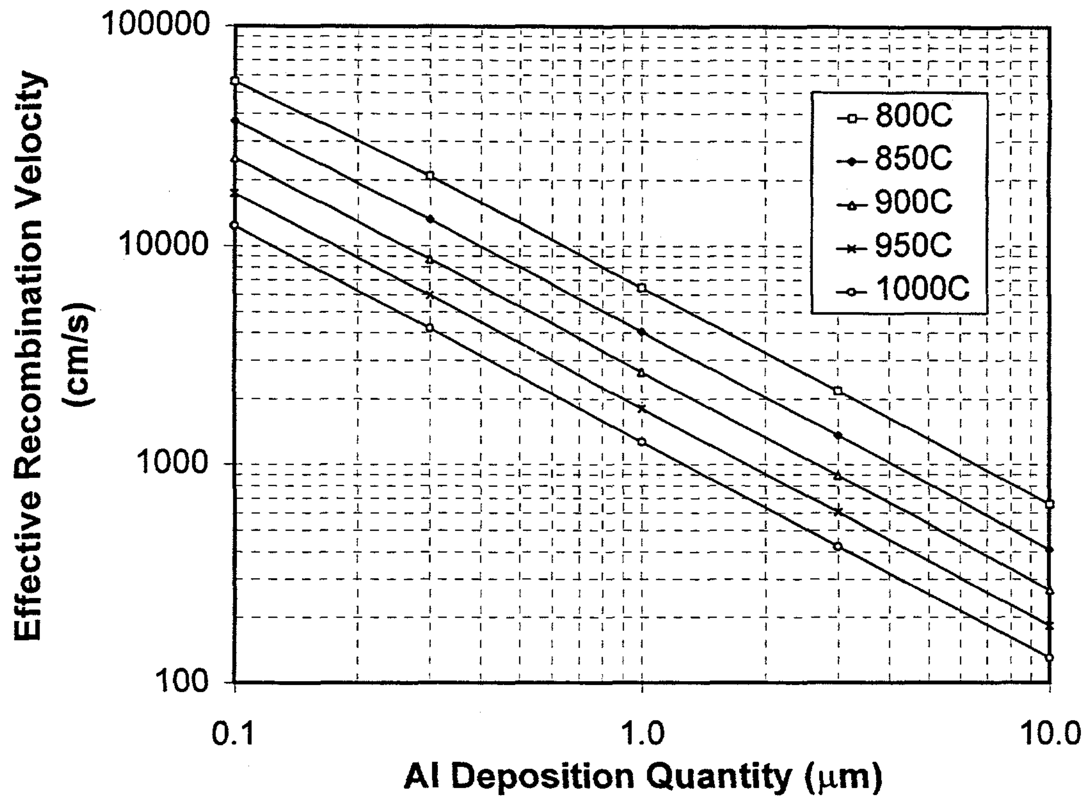


Fig. 4.1. Simulations relating the S_{eff} achieved by the Al-BSF on 2.3 Ω-cm Si to the Al deposition quantity and alloying temperature.

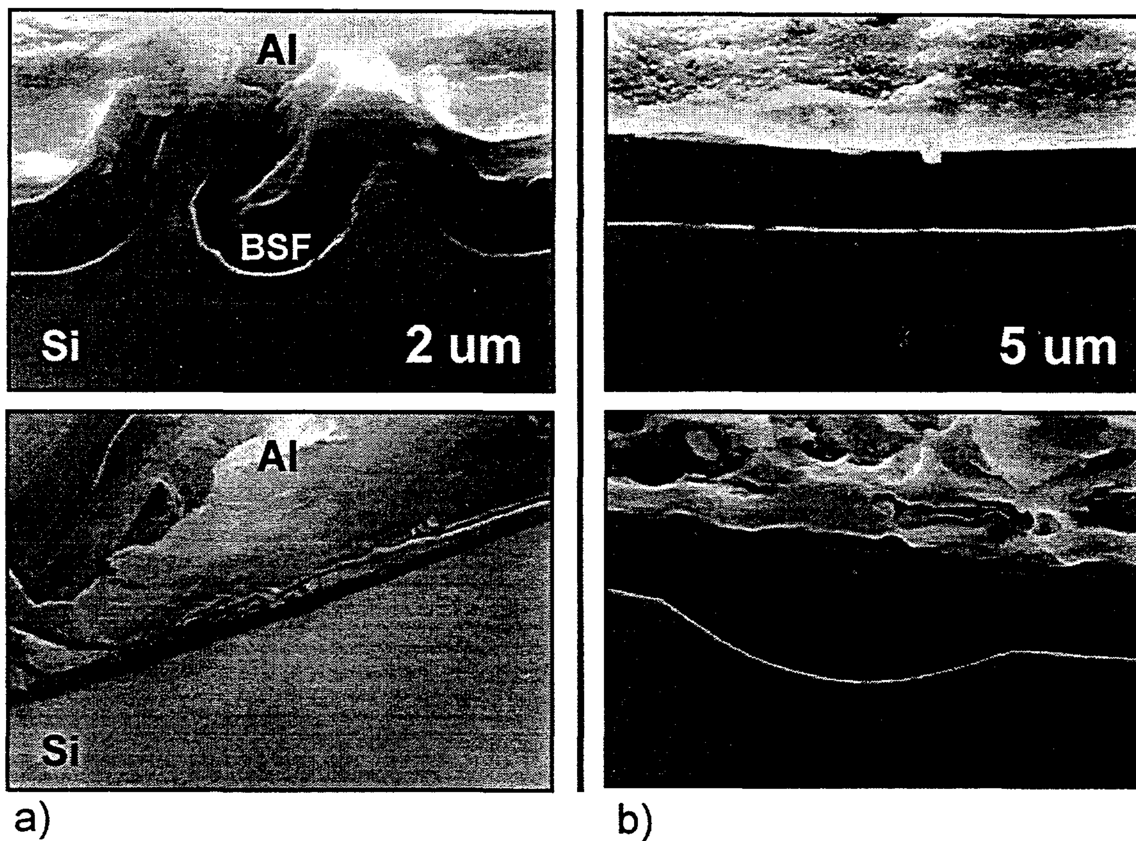


Fig. 4.2. BSF regions formed under a) slow ramp conditions (top shows severe junction non-uniformity, bottom shows non-formation) and b) fast ramp conditions (both top and bottom show clean formation and improved uniformity).

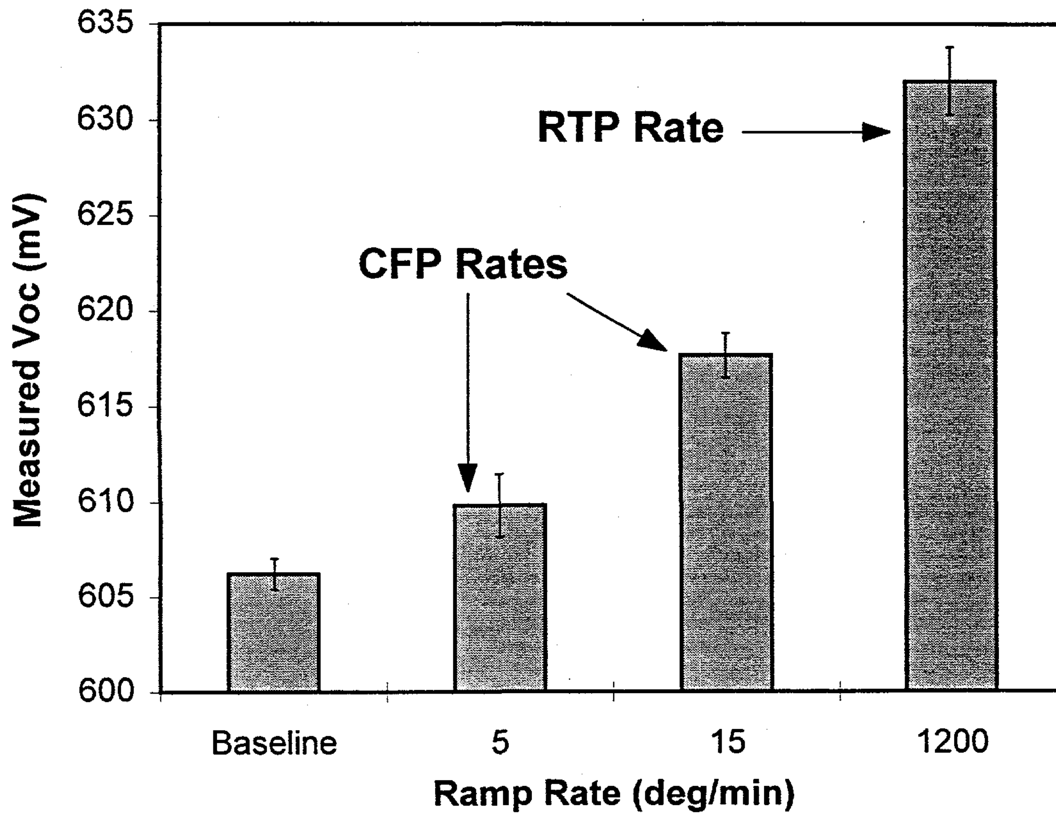


Fig. 4.3. The effect of ramp rate used during Al-BSF alloying on solar cell Voc (2.3 Ω-cm FZ Si substrate). The peak alloying temperature was 850°C. CFP indicates conventional furnace processing.

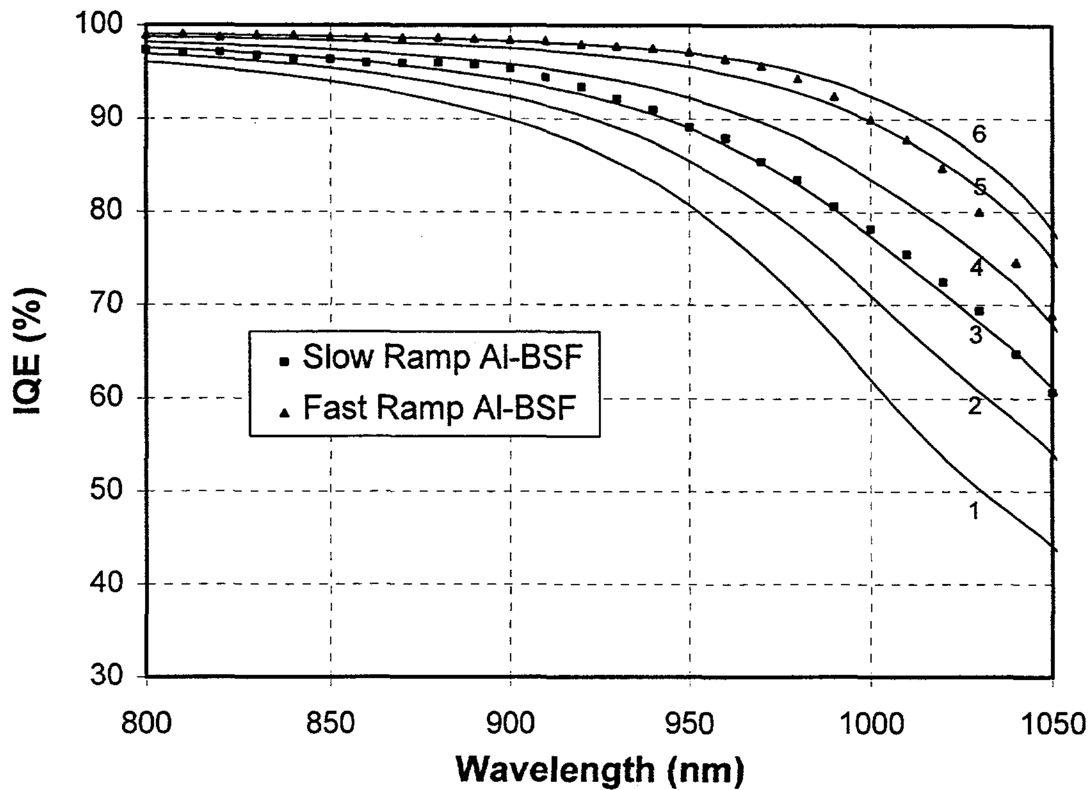


Fig. 4.4. Effect of ramp rate used during alloying on long wavelength IQE response (fast ramp: 1200 °C/min, slow ramp: 5 °C/min). The solid lines represent simulated IQE curves for an analogous cell with different S_b. Lines 1-6 represent S_b values of 10000 cm/s, 2000 cm/s, 1000 cm/s, 500 cm/s, 200 cm/s, and 100 cm/s, respectively.

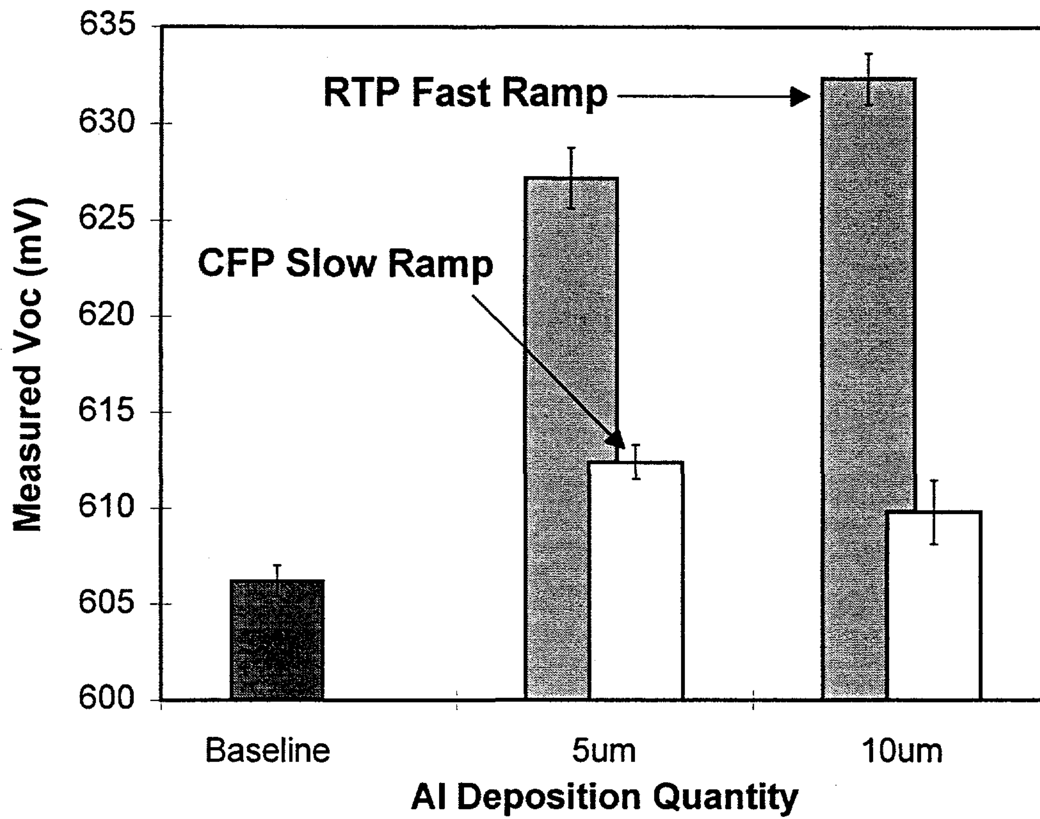


Fig. 4.5. The effect of Al deposition thickness and ramp-rate on solar cell V_{oc} (2.3 Ω-cm FZ Si). The CFP and RTP ramp rates were 5°/min and 1200°/min, respectively, and the peak alloy temperature was 850°C. Each data bar represents the average of nine 4 cm² cells taken from a wafer.

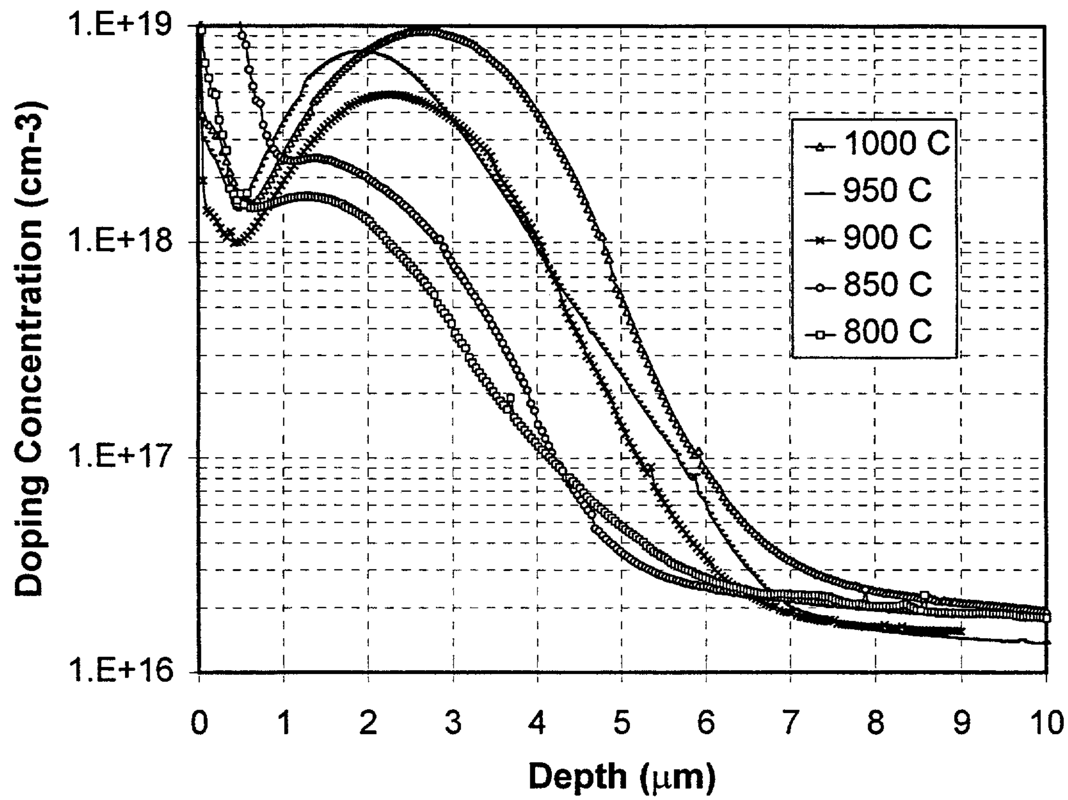


Fig. 4.6. Effect of increased alloying temperature on Al-BSF doping and junction depth as determined by electrochemical CV profile measurements. Each measurement was taken from an area of ≈7 mm^2.

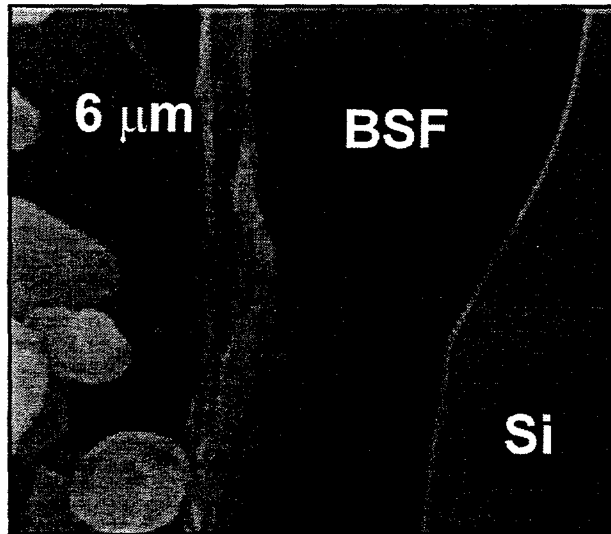


Fig. 4.7. SEM image of a p^+ region formed by screen-printing Al paste and alloying at 850°C in an RTP unit.

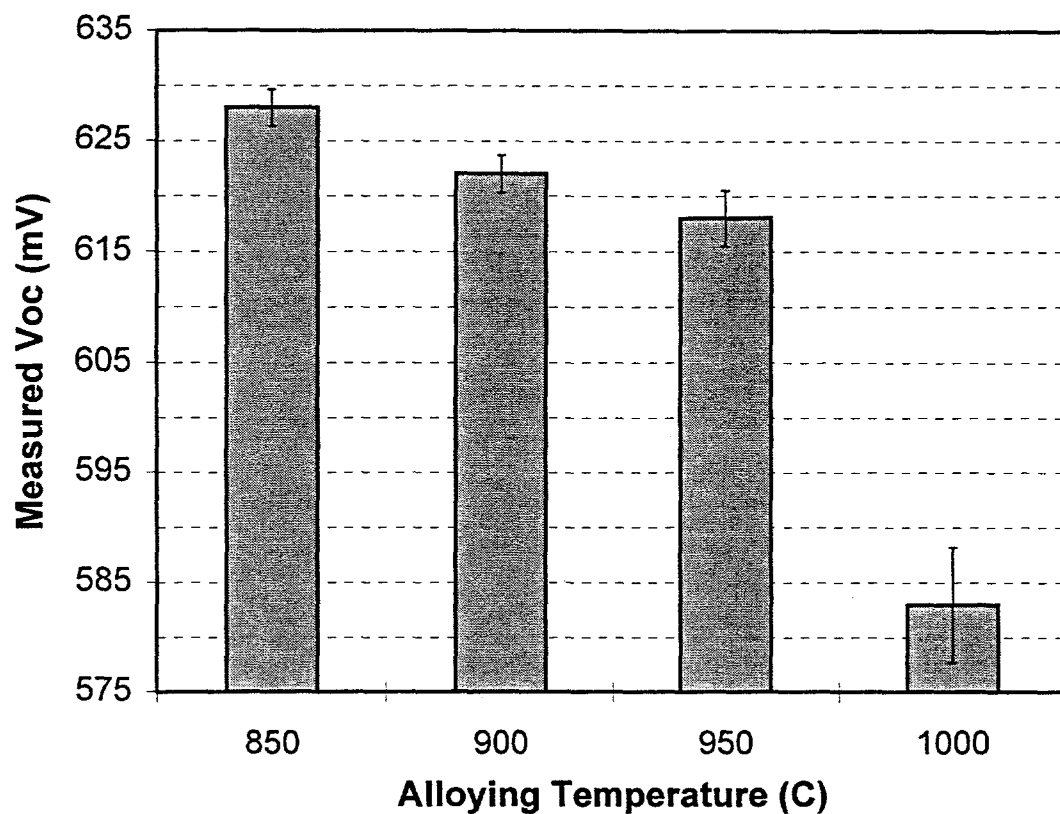
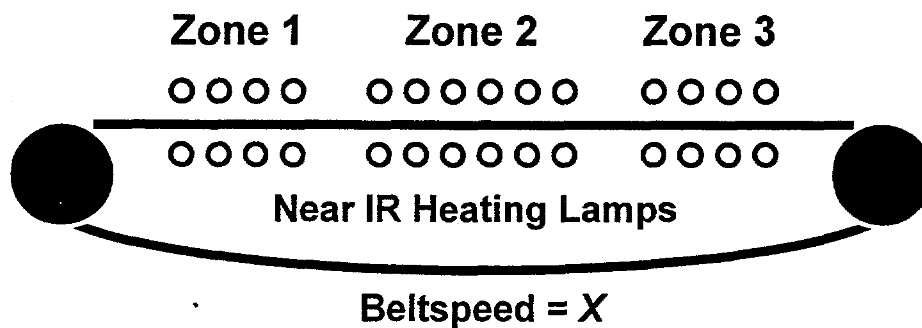


Fig. 4.8. Effect of alloying temperature on contamination in SP Al-BSF solar cells. The V_{oc} values were measured without AR coatings (2.3 Ω-cm FZ Si). Each data bar represents the average of nine 4 cm^2 cells taken from a wafer.



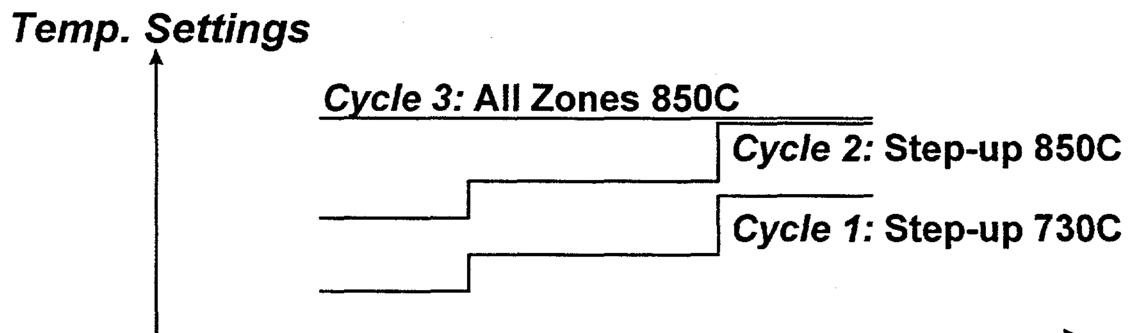


Fig. 4.9. Schematic of the beltline furnace used in this study, and the temperature settings used to investigate Al-BSF formation.

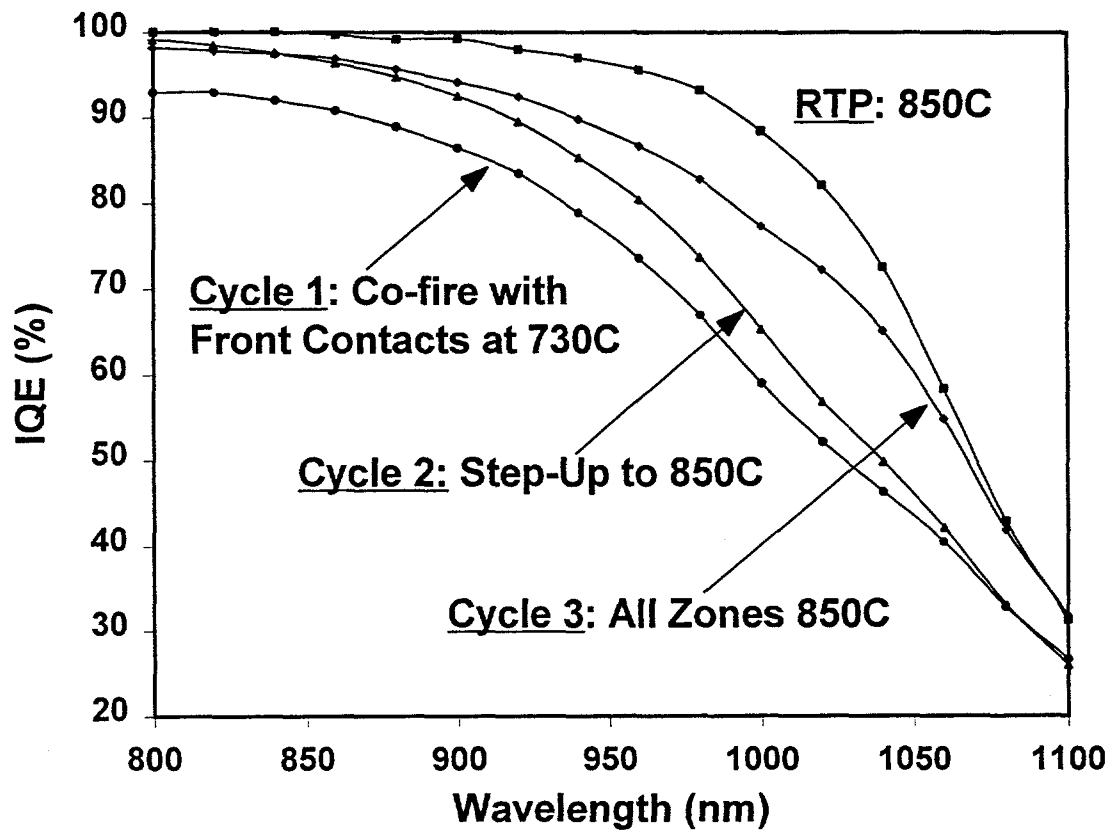


Fig. 4.10. Long wavelength IQE difference for solar cells with Al-BSFs alloyed in a beltline furnace and an RTP unit (2.3 Ω-cm FZ Si).

5.0 Introduction

The overall goal of the research on Evergreen String Ribbon silicon is to fabricate high efficiency solar cells through process development and a fundamental understanding of defect activity. The response of the material to gettering and passivation treatments has been studied in conventional furnace processing (CFP) cells in order to fabricate high efficiency cells. The CFP gettering and passivation treatments were then adapted to the rapid thermal beltline processing (RT-BLP) fabrication sequence along with screen-printing to produce high efficiency RT-BLP cells.

Four major experiments were performed to meet the objectives outlined above. This report is divided into four sections that describe each experiment and their results. Section 1 of the report has the following three objectives: investigation of the effect of the thickness of the evaporated aluminum for the back surface field (BSF), effect of hygrogenation after aluminum gettering, and the evaluation of rapid thermal processing steps on photolithography cells. Section 2 describes the development of an RT-BLP with screen-printing fabrication sequence on 100 μm String Ribbon silicon. Part 3 of the report is a minority carrier lifetime study of the synergistic effect of phosphorous and aluminum gettering and hydrogen passivation using RT-BLP and screen-printing. The objectives of the experiment in Section 4 of this report are to investigate the effect of contact firing, Al-BSF formation time and temperature, emitter doping, and forming gas contact anneal on solar cell performance. These experiments have yielded the highest efficiency screen-printed String Ribbon solar cell.

5.1 High Efficiency 100 μm Thin String Ribbon Silicon Solar Cells Fabricated by Conventional Furnace Processing

5.1.1 Objective

The primary objective of this section is to establish the potential of photovoltaic devices fabricated on the string ribbon material grown by Evergreen Solar using conventional furnace processing. This polycrystalline material is a promising candidate for low-cost silicon photovoltaics because of the ability to grow thin wafers (100-125 μm), with no kerf loss, lack of strict temperature control during growth, and high throughput (5 cm x 10 cm per min). This section of the report examines the following:

1. **The effect of Al BSF thickness:** It has been shown that 1 μm of evaporated Al gives very poor BSF and 5 μm of evaporated Al causes the thin material to warp upon alloying. The effect of a fast ramp in the aluminum-silicon alloying profile is also investigated in this study.
2. **Fabrication Photolithography (PL) Cells using the following three different cell technologies:**
   - **2.1.** Technology A: Conventional Furnace Processing / Conventional Furnace Oxide (CFP/CFO or SBLC)
   - **2.2.** Technology B: Conventional Furnace Processing/ Rapid Thermal Oxide (CFO/RTO)
   - **2.3.** Technology C: Rapid Thermal Belt Line Processing / Conventional Furnace Oxide (RT-BLP/CFO).
3. **The effect of a forming gas anneal (FGA) at** different stages of processing. Some cells were subjected to an additional 2 hour FGA at 400°C following the Al-BSF formation and

oxide growth in the furnace. For comparison, other cells were annealed for 2 hours in N_2 at 400°C after the Al-BSF formation and oxide growth.

5.1.2 Experimental Approach

Phosphorus Diffusion by Conventional Furnace Processing (CFP).

Some wafers in this experiment were diffused in a conventional tube furnace from a $POCl_3$ liquid source at 845 ^{0}C. The wafers were loaded into the furnace at 800^0 C then ramped up to 845^0 C and finally ramped down to 800^0 C before being pulled. After removal of phos glass in HF, a sheet resistance of ~ 80-85 ohm/sq was measured.

Phosphorus Diffusion by Rapid Thermal Belt Line Processing Diffusion (RT-BLP).

Selected wafers were diffused by the application of a phosphorus spin on dopant source (6% P_2O_5) at spin speed of 2500 rpm for 30 sec. This was followed by a thermal cycle in a IR heated beltline furnace. This resulted in sheet resistance of 85-90 Ohm/sq.

Conventional Furnace Oxide Growth (CFO).

The SBLC process involved Al BSF formation by deposition 2 μm of Al on the back surface of all wafers. The wafers were inserted in furnace at 400 ^{0}C in N_2 and ramped at 25 ^{0}C/min to 850 ^{0}C and alloyed for 10 minutes in O_2 and 25 minutes in N_2. This resulted in oxide thickness of ~115-125 A on the front surface of the samples. Selected samples were then ramped down to 400 ^{0}C and subjected to a 2 hour forming gas anneal (FGA) in an attempt to improve surface and bulk defect passivation by hydrogenation. Other samples were ramped down to 400 ^{0}C after oxide growth and BSF formation and annealed in N_2 for 2 hours.

Rapid Thermal Oxide Growth (RTO).

After evaporation of 2 μm of Al, selected wafers were alloyed in a single wafer, UV-

RTP system at 850 ^{0}C 150 seconds in O_2 for the simultaneous formation of the Al-BSF and RTO growth. The ramp rate was 20^{0} C/sec from room temperature and the cooling rate was 1^{0}C /sec to 800°C and 10^{0}C /sec to 500 ^{0}C followed by natural cooling. The ramp-up and ramp-down was performed in a N_2 ambient to prevent any oxide growth at low temperatures. This cycle resulted in an oxide thickness of 95-120 ^{0}A on 80-100 Ω/sq. emitters.

Metallization and Anti-Reflection Coating

The back contact was formed by the evaporation of Al-Ti-Pd-Ag on the back surface of all samples. The front metal grid was formed by photolithography, evaporation, and lift-off of 40 nm Ti, 60 nm Pd, and 100 nm Ag. The cells were then mesa etched to isolate 1cm x 1cm or 2cm x 2cm cell areas and plated with silver under illumination to achieve ~5 μm line height. Finally, a ZnS-MgF_2 double layer antireflection coating was deposited . The processing was finished with 15 min contact anneal in FGA at 400^{0}C. The cells were measured by Light and Dark IV and analyzed at different stages of processing.

5.1.3 Results and Discussion

Table 5.1 shows a summary of the best cells after ZnS/MgF2 ARC and 15 minutes of FGA contact anneal. The best cell gave an efficiency of 15.4%, with Voc of 589, Jsc of 33.61, and a fill factor of 0.778 on the thin Evergreen material (100-125 μm). Figure 5.1 shows a histogram of the improvement in cell efficiency resulting from AR coating and contact annealing in forming gas. Table 5.2 shows the two best cells for each processing technology at different stages of cell processing: before AR coating, after AR coating, and after contact anneal in forming gas. Figure 5.2 is perhaps the most important data because it shows the positive effect of the 2 hour FGA immediately following Al BSF formation oxide growth in a furnace on cell

performance. Table 5.4 shows the efficiency distribution of greater than 14% efficient cells fabricated in several runs on thin Evergreen ribbon material by three different technologies.

A.Effect of Fast Ramp Al BSF

The best cell gave an efficiency of 15.4%, with Voc of 589mV, Jsc of 33.6 mA/cm^2 and a fill factor of 0.778 with fast ramp-up rate (25°C/min) in the aluminum BSF formation thermal profile even with only 2 μm Al BSF. In previous runs a thicker Al BSF (5 μm) showed an improvement in Jsc and Voc but caused warpage of material resulting in non-uniformity in efficiency distribution and difficulty during photolithography processing. Based on the average cell efficiencies of several runs as shown in Table 5.4, evaporating only 2 μm with the fast ramp-up (25°C/min) of the conventional furnace yields similar performance as a slow ramping with 5 μm. Thus, the warpage resulting from the combination of the thick deposited Al layer and slow rap-up rate (10°C/min) can be avoided. Previous experiments have shown that increasing the thickness of the deposited aluminum layer has increased the thickness of the Al-BSF, improving the BSRV of float zone and HEM mc-Si solar cells. A similar decrease in BSRV is expected in String Ribbon silicon. To see the effect of reduced BSRV, the bulk minority carrier diffusion length must be high enough (L >= W) for carriers to see the back surface. PCD measurement of the bulk minority carrier lifetime of finished devices is necessary to determine if the alloying of a substantially thicker Al layer (10 μm) would increase the performance of String Ribbon cells. However, the heat treatment of a thicker aluminum layer (10 μm) on thin String Ribbon (100μm) may cause the material to warp and prohibit further fabrication steps. Unlike the thick Al-BSF passivation scheme, the high quality RTO/SiN stack passivation scheme in conjunction with gridded back contacts may not cause the thin ribbon material to warp upon thermal cycling. If

the lifetime is sufficient to benefit from back passivation, gridded back contact solar cells on string ribbon will be investigated.

B. Effect of FGA anneal

Table 5.2 shows the effect of the 2 hour FGA performed immediately after the Al-BSF/CFO formation on thin Evergreen cell performance. The average efficiency of cells with FGA (CFP/CFO cells) was about 1% (absolute) higher than those that were either annealed in N_2 for 2 hours (CFP/CFO cells) or not annealed following the BSF formation step at all (CFP/RTO cells). Note the significant trend in Voc shown in Table 5.2. Cells without any FGA at all had an average Voc of 549 mV. Applying the AR coating and annealing in forming gas for 15 min. resulted in an average Voc of 570 mV. Cells which initially had a 2 hour FGA gave an average Voc of 573 mV prior to AR coating which improved to 585 mV after AR coating and the 15 minute contact anneal in forming gas.

Figure 5.3a illustrates the difference in IQE of a cell with the 2 hour FGA and a cell annealed in N_2 for 2 hours. The higher quantum efficiency of the cell with the 2 hour FGA is attributed to a larger effective diffusion length. Two theories that explain the difference in the long wavelength IQE can be stated: 1) the 2 hour FGA improved the effective diffusion length of minority carriers by the passivation of bulk defects; and 2) the as grown material quality of sample ETN22 (w/ 2-hour FGA) was better than ETN7 (w/ 2-hour N_2) resulting in a larger effective diffusion length in the finished device. Evidence of material non-uniformity is seen in Figure 5.3b in which the two cells compared (ETN11-8 and ETN 11-11) were processed *identically* on the *same* piece of ribbon. The difference in the long wavelength IQE of the two cells is due to the variation of material quality on the same ribbon, not a variation in the

processing. This observation makes the analysis of the IQE of two String Ribbon silicon solar cells inconclusive. Figure 5.2 suggests that the material may respond very favorably to hydrogenation from a low temperature forming gas anneal. However, because of the possibility of a variation of material quality from sample to sample, the experiment must be repeated on a larger scale with random material to isolate the passivation effect of the 2-hour FGA from the as-grown material quality.

C. *Improvement in cell performance after ARC and FGA Contact anneal*

Table 5.3 shows the effects of ARC and contact anneal in forming gas on the cell performance. It is interesting to note that the cells with RTO passivation, which had no FGA anneal after the Al BSF formation and oxide growth showed remarkable improvements, on the order of 60 to 70%, in efficiency after the ARC and FGA contact anneal. The CFO cells with FGA anneal during the BSF formation showed an improvement of 48 to 55% in efficiency after the ARC & FGA contact anneal and the cells annealed only in N_2 improved by 48 to 66%. This improved is attributed to reduced surface reflection and defect passivation from the contact anneal in forming gas. The thick (250 μm) Evergreen material also showed similar trends.

5.1.4 FUTURE DIRECTIONS

Further characterization and repetition of the cells produced in this run is necessary. When the effects of the 2-hour FGA and back surface passivation schemes have been reproduced, model calculations will be performed to gauge the impact of bulk lifetime, back surface recombination velocity, and thickness on cell performance. Further improvements including optimized phosphorus and aluminum gettering, FGA and PECVD hydrogenation, high-quality RTO+SiN surface passivation, and clever cell designs can produce greater than

16%-efficient thin Evergreen ribbon silicon cells. Further improvement will make this material a significant competitor to thin Si film cells since only 100 μm of material is consumed to yield stable efficiencies on such inexpensive silicon.

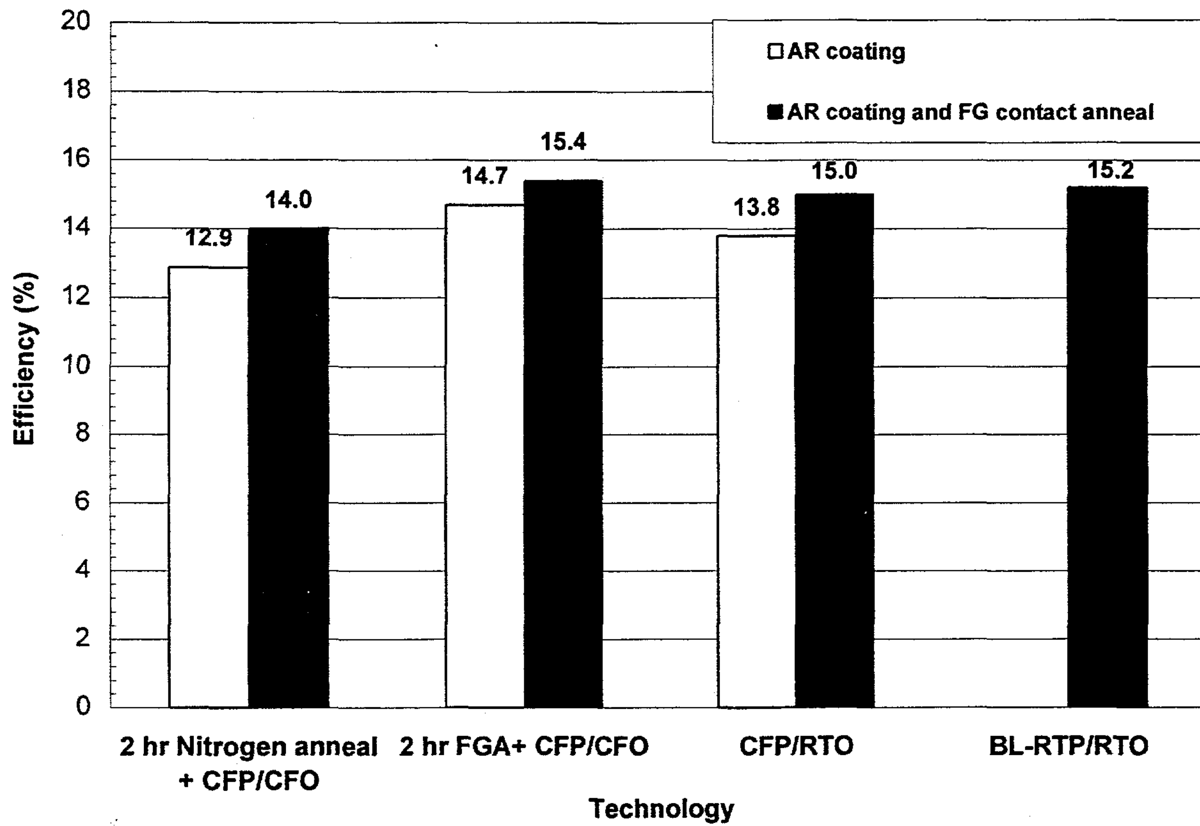


Figure 5.1 Histogram of Improvement in Cell Efficiency

1 cm² thin Evergreen cells WITH 2 hr. FGA									
		Before AR & FG Cont. Anneal				After AR & Cont. Anneal in FG			
Cell ID	Technology	Voc (mV)	Jsc (mA/cm2)	FF	Eff (%)	Voc (mV)	Jsc (mA/cm2)	FF	Eff (%)
ETN8-1	CFP/CFO	574	23.10	0.763	10.1	587	33.20	0.765	14.9
ETN8-6	CFP/CFO	566	21.19	0.784	9.4	578	32.49	0.777	14.6
ETN3-6	CFP/CFO	573	22.40	0.762	9.8	585	33.46	0.772	15.1
ETN3-7	CFP/CFO	577	22.53	0.773	10.0	589	33.61	0.778	15.4
	Average	**573**	**22.30**	**0.771**	**9.8**	**585**	**33.19**	**0.773**	**15.0**

1 cm² thin Evergreen cells WITHOUT 2 hr. FGA									
		Before AR & FG Cont. Anneal				After AR & Cont. Anneal in FG			
Cell ID	Technology	Voc (mV)	Jsc (mA/cm2)	FF	Eff (%)	Voc (mV)	Jsc (mA/cm2)	FF	Eff (%)
ETN7-2	CFP/CFO	550	21.54	0.745	8.8	564	32.63	0.758	14.0
ETN7-3	CFP/CFO	542	20.90	0.727	8.2	559	31.80	0.748	13.3
ETN7-7	CFP/CFO	551	20.11	0.767	8.5	577	31.37	0.780	14.1
ETN9-2	CFP/CFO	555	22.34	0.737	9.1	576	31.58	0.756	13.8
ETN9-3	CFP/CFO	545	21.29	0.742	8.6	563	29.86	0.746	12.5
ETN9-5	CFP/CFO	540	20.88	0.746	8.4	555	30.09	0.749	12.5
ETN9-6	CFP/CFO	555	21.96	0.734	8.9	581	30.75	0.756	13.5
ETN9-8	CFP/CFO	551	21.45	0.743	8.8	565	29.38	0.751	12.5
ETN2-6	CFP/RTO	559	21.28	0.764	9.1	582	33.22	0.765	14.8
ETN6-1	CFP/RTO	561	21.92	0.756	9.3	578	33.48	0.774	15.0
ETN6-5	CFP/RTO	544	20.61	0.745	8.4	569	32.31	0.763	14.0
ETN6-7	CFP/RTO	539	20.13	0.736	8.0	566	32.21	0.756	13.8
ETN6-9	CFP/RTO	551	20.81	0.758	8.7	570	31.76	0.772	14.0
ETN6-10	CFP/RTO	549	21.03	0.748	8.6	570	32.62	0.763	14.2
ETN4-1	CFP/RTO	553	20.60	0.758	8.6	578	32.64	0.778	14.7
ETN5-1	CFP/RTO	543	20.69	0.737	8.3	567	33.16	0.751	14.1
	Average	**549**	**21.10**	**0.746**	**8.6**	**570**	**31.80**	**0.760**	**13.8**

Figure 5.2 Effect of 2-hour Forming Gas Anneal on String Ribbon Solar Cells

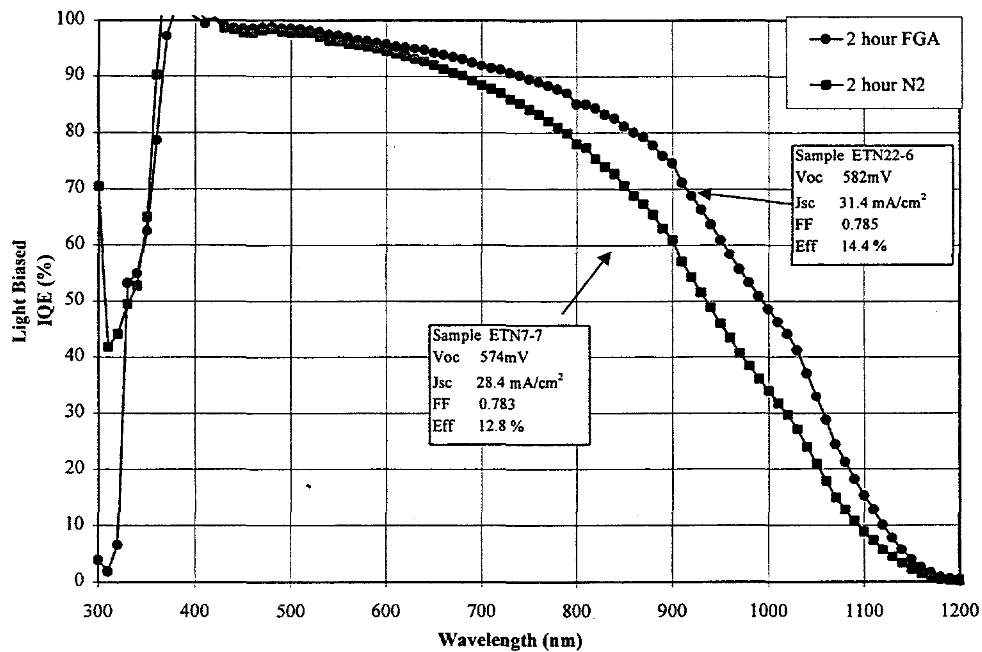


Figure 5.3a Effect of 2-hour FGA on long wavelength IQE

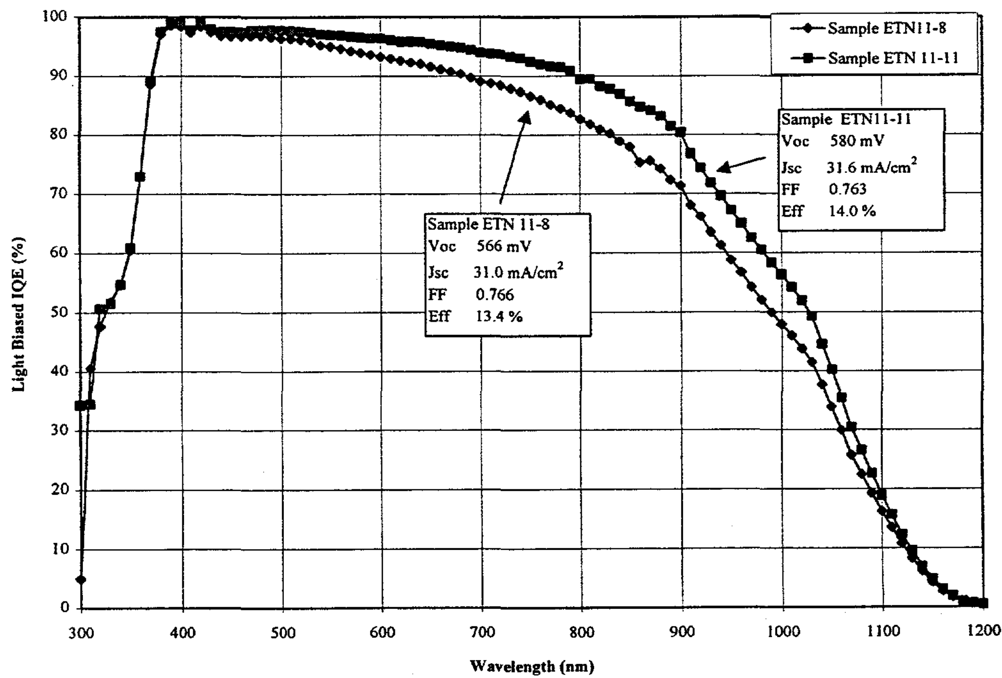


Figure 5.3b Evidence of variation in bulk lifetime of samples

Table 5.1: Best Cell Performance After ARC & 15 minutes FGA Contact Anneal on Evergreen Material with Various Technologies

Process	FGA/N2	Jsc	Voc	FF	Eff %
Thin Evergreen					
CFP/CFO	N2	31.37	577	780	14.1
CFP/CFO	FGA	33.61	589	778	15.4
CFP/RTO	N2	33.48	578	774	15.0
BLP/CFO	FGA	31.77	589	756	14.1*
Thick Evergreen					
BLP/CFO	FGA	32.90	588	774	15.0

**2x2*

Table 5.2: Effect of FGA at Various Stages of Processing on the Performance of Evergreen String Ribbon Solar Cells fabricated by Different Technologies

(Best Cells)

Technology A : BLP/CFO

Processing	Jsc	Voc	FF	Eff %
THIN EVERGREEN				
FGA anneal on CFO & No FGA Contact Anneal (ETN1-1 & ETN1-2)	**22.69** **22.14**	**578** **574**	**745** **753**	**9.8** **9.6**
FGA anneal on CFO & ZnS/MgF2 ARC only (ETN1-1 & ETN1-2)	**30.33** **29.70**	**580** **576**	**743** **759**	**13.1** **13.0**
FGA anneal on CFO & ZnS/MgF2 ARC + 15 min FGA Contact Anneal (ETN1-1 & ETN1-2)	**31.77** **31.17**	**589** **581**	**756** **765**	**14.1** **13.9**
THICK EVERGREEN				
FGA anneal on CFO & No FGA Contact Anneal (ETH1-10 & ETH1-11)	**23.58** **23.68**	**580** **581**	**761** **774**	**10.4** **10.7**

FGA anneal on CFO & ZnS/MgF2 ARC only (ETH1-10 & ETH1-11)	31.52 31.48	581 583	767 773	14.0 14.2

Table 5.2 cont.

FGA anneal on CFO & ZnS/MgF2 ARC + 15 min FGA Contact Anneal (ETH1-10 & ETH1-11)	32.40 32.35	586 586	756 774	14.4 15.0

Technology B : CFP/CFO

Processing	Jsc	Voc	FF	Eff %
THIN EVERGREEN				
N2 anneal on CFO & No FGA Contact Anneal (ETN7-2 & ETN9-2)	21.54 22.34	550 555	745 737	8.8 9.1
FGA anneal on CFO & No FGA Contact Anneal (ETN3-6 & ETN3-7)	22.40 22.53	573 577	762 773	9.8 10.0
N2 anneal on CFO & ZnS/MgF2 ARC only (ETN7-2 & ETN9-2)	31.18 30.01	553 556	747 737	12.9 12.3

FGA anneal on CFO & ZnS/MgF2 ARC only (ETN3-6 & ETN3-7)	**32.51** **32.67**	**578** **582**	**772** **776**	**14.5** **14.7**

Table 5.2 cont.

N2 anneal on CFO & ZnS/MgF2 & ARC 15 min FGA Contact Anneal (ETN7-2 & ETN9-2)	**32.63** **31.58**	**564** **576**	**758** **756**	**14.0** **13.8**
FGA anneal on CFO & ZnS/MgF2 & ARC 15 min FGA Contact Anneal (ETN3-6 & ETN3-7)	**33.46** **33.61**	**585** **589**	**772** **778**	**15.1** **15.4**

Technology C: CFP/RTO

Processing	Jsc	Voc	FF	Eff %
THIN EVERGREEN				
N2 anneal on RTO & No FGA Contact Anneal (ETN6-1,ETN4-1 & ETN5-1)	**21.92** **20.60** **20.69**	**561** **553** **543**	**756** **758** **737**	**9.3** **8.6** **8.3**

N2 anneal on RTO & ZnS/MgF2 ARC only (ETN6-1,ETN4-1 & ETN5-1)	32.42 30.50 31.0	564 555 545	757 758 740	13.8 12.8 12.5
N2 anneal on RTO & ZnS/MgF2 & ARC 15 min FGA Contact Anneal (ETN6-1,ETN4-1,ETN5-1)	33.48 32.64 33.16	578 578 567	774 778 751	15.0 14.7 14.1

Table 5.3 : The effect of ZnS/MgF2 ARC & FGA Contact Anneal for Photolithography Solar Cells on Evergreen Ribbon Material

Before = No FGA Contact Anneal & No ZnS/MgF2 ARC.
After = ZnS/MgF2 ARC & 15 min FGA Contact Anneal.

a) BLP/CFO

THICK EVERGREEN WITH FGA ANNEAL ON CFO

Ribbon ID # ETH1

Best cell # 11

Condition	Jsc	Voc	FF	Eff %
Before	23.68	581	774	10.7

After	32.90	588	774	15.0
Improvement %	*40*	*1.4*	-	*40*

Average (12 Cells)

Condition	Jsc	Voc	FF	Eff %
Before	23.08	577	764	10.2

Table 5.3 contd.

After	31.75	588	761	14.2
Improvement %	*38*	*1.9*	*- 0.4*	*39*

THIN EVERGREEN WITH FGA ANNEAL ON CFO

Ribbon ID # ETN1

Best Cell# 1

Condition	Jsc	Voc	FF	Eff %
Before	**22.69**	**578**	**745**	**9.8**
After	**31.77**	**589**	**756**	**14.1**
Improvement %	*40*	*1.9*	*1.5*	*44*

Table 5.3 cont.

Average (2 Cells)

Condition	Jsc	Voc	FF	Eff %
Before	**22.40**	**576**	**749**	**9.7**

After	**31.47**	**585**	**761**	**14.0**
Improvement %	*41*	*1.6*	*1.6*	*44*

B. CFP/CFO

THIN EVERGREEN WITH FGA ANNEAL ON CFO

Ribbon ID # ETN8

Cell# 1

Condition	**Jsc**	**Voc**	**FF**	**Eff %**
Before	**23.10**	**574**	**0.763**	**10.1**

Table 5.3 cont.

After	**33.20**	**587**	**0.765**	**14.9**
Improvement %	*44*	*2.3*	*0.3*	*48*

Average (6 & 5 cells)

Condition	Jsc	Voc	FF	Eff %
Before	**22.22**	**571**	**750**	**9.5**
After	**32.68**	**581**	**733**	**13.9**
Improvement %	*47*	*1.8*	*-2.3*	*46*

Ribbon ID # ETN3

Cell # 7

Condition	Jsc	Voc	FF	Eff %
Before	**22.53**	**577**	**773**	**10.0**
After	**33.61**	**589**	**778**	**15.4**

Table 5.3 cont.

Improvement %	*49*	*2.1*	*0.7*	*54*

Average (2 Cells)

Condition	**Jsc**	**Voc**	**FF**	**Eff %**
Before	**22.46**	**575**	**768**	**9.9**
After	**33.53**	**587**	**775**	**15.3**
Improvement %	*49*	*1.7*	*0.9*	*55*

THIN EVERGREEN WITH N2 ANNEAL ON CFO

Ribbon ID # ETN7

Cell# 7

Condition	**Jsc**	**Voc**	**FF**	**Eff %**

Table 5.3 cont.

Before	**20.11**	**551**	**767**	**8.5**
After	**31.37**	**577**	**780**	**14.1**
Improvement %	*56*	*4.7*	*1.7*	*66*

Average (5Cells)

Condition	Jsc	Voc	FF	Eff %
Before	**20.39**	**547**	**741**	**8.3**
After	**31.62**	**567**	**736**	**13.2**
Improvement %	*55*	*3.7*	*-0.7*	*59*

Table 5.3 comt.

Ribbon ID # ETN9

Cell# 2

Condition	Jsc	Voc	FF	Eff %
Before	**22.34**	**555**	**737**	**9.1**
After	**31.58**	**576**	**756**	**13.8**
Improvement %	*41*	*3.8*	*2.6*	*52*

Average (10 & 7 Cells)

Condition	Jsc	Voc	FF	Eff %
Before	**21.30**	**547**	**738**	**8.6**
After	**30.10**	**565**	**746**	**12.7**

Improvement %	*41*	*3.3*	*1.1*	*48*

Table 5.3 cont.

c) CFP/RTO

THIN EVERGREEN WITH N2 ANNEAL ON RTO

Ribbon ID # ETN2
Cell 6

Condition	**Jsc**	**Voc**	**FF**	**Eff %**
Before	**21.28**	**559**	**764**	**9.1**
After	**33.22**	**582**	**765**	**14.8**
Improvement %	*56*	*4*	*0.1*	*62*

Ribbon ID # ETN6

Cell # 1

Condition	**Jsc**	**Voc**	**FF**	**Eff %**

Before	**21.92**	**561**	**756**	**9.3**
After	**33.48**	**578**	**774**	**15.0**

Table 5.3 cont.

Improvement %	*53*	*3.0*	*2.4*	*61*

Average (6 cells)

Condition	Jsc	Voc	FF	Eff %
Before	**21.47**	**555**	**752**	**9.0**
After	**32.37**	**570**	**764**	**14.1**
Improvement %	*51*	*2.7*	*1.6*	*57*

Ribbon ID # ETN4

Cell 1

Condition	Jsc	Voc	FF	Eff %
Before	20.60	553	758	8.6

Table 5.3 cont.

After	32.64	578	778	14.7
Improvement %	*59*	*4.5*	*2.6*	*71*

Ribbon ID # ETN5

Cell 1

Condition	Jsc	Voc	FF	Eff %
Before	20.69	543	737	8.3
After	33.16	567	751	14.1

Improvement %	*60*	*4.4*	*1.9*	*70*

Table 5.4: Above 14% Efficient PL Solar Cells Fabricated on Ribbon Thin Evergreen Material.

(Thickness=~125 micron; Resistivity=1 - 2 ohm-cm, cell area= 1 sq cm)

Cell ID #	Voc	Jsc	FF	Eff %
CFP/CFO (Slow Ramp, 1 micron Al BSF)				
9639E7-1	594	33.0	775	15.2
9639E6-1	585	32.9	756	14.5
9639E5-1	585	31.4	792	14.6
9639E5-3	576	31.3	786	14.2
9639E5-6	581	30.9	792	14.2
9639E5-7	579	30.9	792	14.2
9639E5-8	579	31.1	785	14.1

Table 5.4 cont.

9639E8-3	**577**	**31.5**	**787**	**14.3**
9639E8-8	**577**	**30.7**	**789**	**14.0**
9639E9-1	**580**	**31.7**	**763**	**14.0**
Average	**581**	**31.5**	**782**	**14.3**
CFP/CFO (Slow Ramp, 5 micron Al BSF)				
9641G3-1	**585**	**33.5**	**762**	**14.9**
9641G3-2	**588**	**33.7**	**761**	**15.1**
9641G1-3	**566**	**33.3**	**747**	**14.1**
9641G1-11	**568**	**34.1**	**773**	**15.0**
9641G4-3	**584**	**32.6**	**774**	**14.7**
9641G4-2	**570**	**33.0**	**732**	**15.0**
Average	**578**	**32.9**	**762**	**14.6**
CFP/CFO (Fast Ramp, 2 microns Al BSF)				
98ETN3-7	**589**	**33.6**	**778**	**15.4**
98ETN3-6	**585**	**33.5**	**772**	**15.1**

98ETN8-1	587	33.2	765	14.9

Table 5.4 cont.

98ETN8-6	578	32.5	777	14.6
98ETN7-2	564	32.6	758	14.0
98ETN7-7	577	31.4	780	14.1
Average	578	32.8	765	14.7
CFP/RTO (2 micron Al BSF)				
98ETN6-1	578	33.5	774	15.0
98ETN6-5	569	32.3	763	14.0
98ETN6-9	570	31.8	772	14.0
98ETN6-10	570	32.6	763	14.2
98ETN4-1	578	32.6	778	14.7
98ETN5-1	567	33.2	751	14.1
Average	573	32.5	768	14.4
BLP/CFO (Fast ramp, 2 micron Al BSF)				
98ETN1-1	589	31.8	756	14.1*

***4 sq cm cell**

5.2 High Efficiency 100 μm Thin String Ribbon Solar Cells Fabricated by Rapid Thermal Beltline Processing and Screen-Printing

5.2.1 Introduction

In an attempt to fabricate fully screen-printed cells on 100 μm string ribbon, considerable effort went into learning how to handle the ribbon and into developing appropriate conditions for screen printing on such thin material. The first attempt was to make a screen printed full Al back fired at 850°C to form a BSF. While the screen printing of the Al was successful, firing the metal in a beltline furnace at 850°C caused stressed-induced warping of the sample. As a result, we developed a gridded back contact cell with metal coverage of less than 10%. To reduce the back surface recombination velocity and serve as an AR coating, PEVCD SiN was deposited on the back and front surfaces. The back and front grid patterns were printed on top of and fired through the SiN layer. A schematic of the cell design is shown in Figure 5.4.

5.2.2 Solar Cell Processing of Screen Printed Gridded Back Contact Cells

Scribing Samples

Each sample was carefully scribed with a diamond tip pen.

Sample Cleaning

Samples were cleaned in the following series of solutions:

1. Rinse in H_2O for 5 min
2. 10:1 $HF:H_20$ for 1 min
3. Rinse in H_20 for 2 min
4. 2:1:1 $H_2O:H_2SO_4:H_2O_2$ for 5 min
5. Rinse in H_2O for 3 min
6. 15:5:2 $CH_3COOH:HNO_3:HF$ for 2 min

7. Rinse in H_2O for 3 min

8. 2:1:1 H_2O:HCl:H_2O_2 for 5 min

9. Rinse in H_2O for 3 min

10. 10:1 HF:H_2O for 4 min

11. Rinse in H_2O, dry with N_2 gun

Rapid Thermal Beltline Diffusion

Diffusion was performed with phosphorous spin-on dopant in a beltline furnace to achieve sheet rho of 45Ω/.

Phos-Glass Removal

Removal of phos-glass was done in 10:1 H_2O:HF.

PECVD SiN Deposition

A SiN layer of index of refraction of 2.0 was deposited to a thickness of 600 A. SiN is deposited on both sides in the gridded back contact design.

Rear gridded Contact Printing

A grid pattern was printed using a thinned Ag-Al paste. Samples were then baked on a hot plate at 175°C for 2 minutes.

Front Contact Pattern

A front contact pattern for 2-cm x 2-cm cells was printed using Ag-paste. Samples were then baked on a hot plate at 175°C for 2 minutes.

Contact Firing

Contact firing was done in the beltline furnace at 730°C for 30 seconds.

Isolation

Cells on each sample were isolated with dicing saw cuts of 2.5 mils in depth. The 2.5-mil deep cuts were made because they can be resolved visually and are continuos across the surface of the sample. Shallower cuts were not continuous at grain boundaries. Deeper cuts significantly compromised the strength of the samples. Even the samples isolated with 2.5 mil deep cuts were prone to fracture, but safely along the cut lines.

Forming Gas Anneal

Samples were placed in forming gas anneal furnace at 400°C for 20 minutes.

Measure

Light and dark I-V characteristics were measured.

Evaporation of full aluminum rear contact

A full rear contact of aluminum of thickness 1.9 μm was formed by evaporation. A full rear contact was necessary because it could not be determined if our I-V tester was making electrical contact to the Al-Ag grid. The contact was not fired or annealed. The series resistance and efficiency of the cells improved after evaporating the full rear contact.

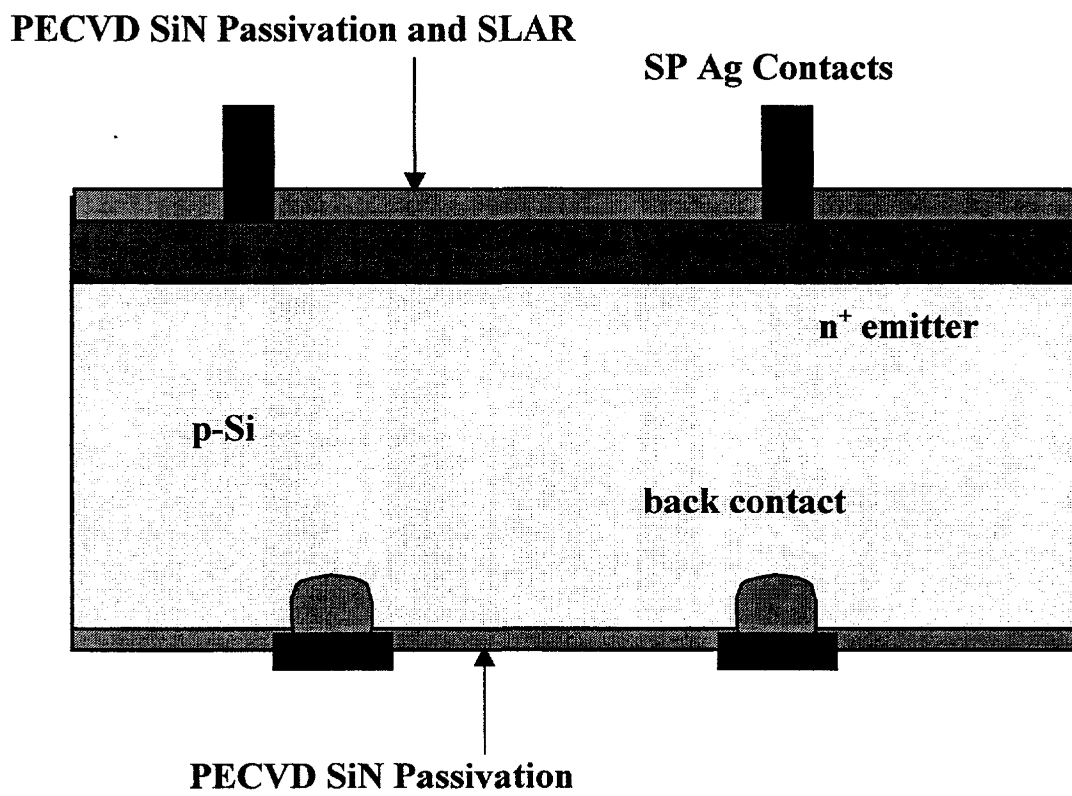


Figure 5.4 Schematic of Gridded Back Contact String Ribbon Cell

5.2.3 Results

Table 5.5 : Fully Screen Printed 100 μm Evergreen Cells

		Gridded Back Contact only				
Cell ID	V_{oc}	J_{sc}	FF	Eff	Rs	Rsh@-1
	(mV)	(mA/cm2)		(%)	(W-cm2)	(W-cm2)
evg1	529	26.15	0.627	8.7	1.53	814
evg2-1	518	24.01	0.635	7.9	1.35	316
evg2-2	375	25.63	0.522	5.0	2.38	855
evg3-1	548	28.61	0.488	7.6	1.84	881
evg3-2	561	28.28	0.639	10.1	1.29	1,601

	After evaporation of full Al back on top of gridded back					
Cell ID	V_{oc}	J_{sc}	FF	Eff	Rs	Rsh@-1
	(mV)	(mA/cm2)		(%)	(W-cm2)	(W-cm2)
evg1	523	26.51	0.68	9.4	0.53	748
evg2-1	519	24.28	0.661	8.3	0.53	748
evg2-1	518	24.27	0.662	8.3	0.56	315
evg2-2	375	25.84	0.572	5.5	3.55	742
evg3-1	546	28.83	0.496	7.8	1.34	649
evg3-2	557	28.56	0.666	10.6	0.72	1,655

Table 5.6 : Highest Evergreen Cell Efficiency Achieved by Photolithography

V_{oc}	J_{sc}	FF	Eff
(mV)	(mA/cm2)		(%)
594	33.00	0.775	15.2

5.2.4 Discussion

Attempts to fabricate screen printed cells with full metal backs and BSFs did not succeed due to stress-induced warping of the thin ribbon during BSF formation. However, we were successful in making the gridded back contact cells on 100μm string ribbon. Screen printing on the thin material required significant process development including the thinning of the Ag/Al

paste to achieve the proper paste viscosity. More effort is needed to improve the yield of the printing steps. The PECVD SiN film deposited on the front serves as an AR coating, while SiN on the back reduces surface recombination velocity between the grid.

First run cells have efficiencies approaching 10%. In this run, the fill factors of less than 0.67 were unusually low. The identical process on float zone cells gives fill factors of 0.76. There was a concern that our cell tester was not making good contact to the grid pattern on the back of the cells. Therefore, we decided to evaporate Al metal to provide full coverage of the back. The results show that, while the series resistance did improve after the Al evaporation, the shunt resistance remains low contributing to the low fill factors. In addition discontinuous front contact patterns were observed on the cells that still have a high series resistance. It is believed that using a Ag paste with the proper viscosity on the front pattern can solve this problem. The low current may explained by the improper index and thickness of SiN and the lack of a second layer AR coating of MgF_2. The photolithography cell has a double-layer AR coating.

5.3 Gettering and Passivation of Bulk Defects in String Ribbon Silicon with Beltline Rapid Thermal Processing, Screen-Printing, and PECVD SiN

5.3.1 Introduction

String Ribbon silicon is an attractive material for photovoltaics because it can be grown thin (100 μm) without incurring a kerf loss. However the as-grown bulk minority carrier lifetime of the material, as measured by photoconductance decay, is less than 1 μs. For high efficiency solar cells, the diffusion length to thickness ratio must greater than one. Therefore in order to fabricate high efficiency solar cells on String Ribbon silicon the diffusion length, or the lifetime, of the material must be increased. To maintain the cost-effectiveness of String Ribbon silicon, procedures that improve the lifetime of the material must be in-line with the industrial fabrication processes of beltline furnace processing and screen-printing.

Phosphorus and aluminum gettering have been shown to improve the lifetime of multicrystalline silicon materials. The synergistic affect of phosphorous and aluminum gettering has been shown to improve the bulk lifetime of ribbon multicrystalline silicon. In addition, hydrogenation from a PECVD SiN thin film has been shown to improve the bulk lifetime of ribbon multicrystalline silicon. The purpose of this experiment is to quantify the effects of :

1. Hydrogen passivation from a PECVD SiN film on the bulk minority carrier lifetime of String Ribbon silicon
2. The synergistic effect of phosphorous, aluminum gettering and hydrogentation from a PECVD SiN film.

5.3.2 Experimental

To investigate the effect of hydrogen passivation from a PECVD SiN film on the bulk minority carrier lifetime of String Ribbon silicon, a PECVD SiN layer was deposited and heat treated in screen-printing anneals. The SiN layer was then etched and the bulk lifetime was measured using transient photocondutance decay (PCD) and chemical passivation (0.001 M I_2 in methanol). .

To investigate the synergistic effect of phosphorous, aluminum gettering and hydrogentation from a PECVD SiN film a combination of rapid thermal beltline processing (RT-BLP), PECVD, and screen-printing was used. The bulk lifetime of samples was measured using quasi-steady state PCD (QSS-PCD) and chemical passivation (0.001 M I_2 in methanol) after removing any aluminum metal and n+ and p+ diffusions. A description of Processes A-D in this experiment is listed below:

Process A – Phosphorous diffusion using RT-BLP at 965°C for 6 minutes

Process B – Phosphorous diffusion using RT-BLP at 965°C for 6 minutes
PECVD SiN, peak temperature of 700°C anneal in beltline furnace for 30 seconds

Process C - Phosphorous diffusion using RT-BLP at 965°C for 6 minutes
PECVD SiN, aluminum screen- printing, peak temperature of 700°C anneal in beltline furnace for 30 seconds

Process D - Phosphorous diffusion using RT-BLP at 965°C for 6 minutes
PECVD SiN, aluminum screen- printing, 850°C anneal in beltline furnace for 2 minutes

5.3.3 Results

Figure 5.5 illustrates the effect of the annealing of the SiN layer on the and bulk lifetime of String Ribbon.

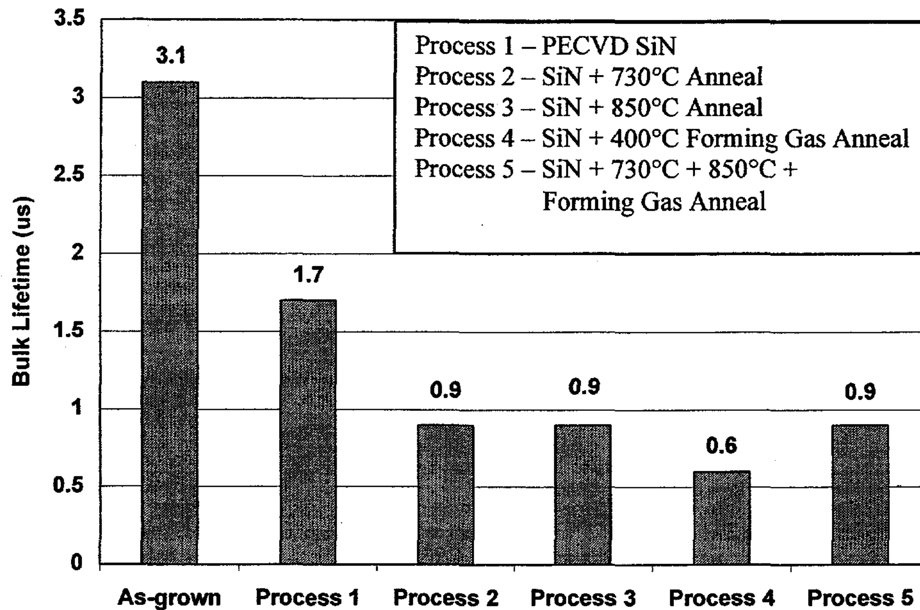


Figure 5.7 Effect of Hydrogenation alone on bulk lifetime of String Ribbon

The results indicate that the bulk lifetime of String Ribbon silicon does not change significantly from the as-grown value of 3 μs. This result leads to the conclusion that hydrogenation from the PECVD SiN film alone is not effective in improving the bulk lifetime of String Ribbon silicon.

The synergistic effect of phosphorous and aluminum gettering with hydrogenation was investigated in the beltline furnace with liquid source dopant, screen-printed aluminum and a PECVD SiN film. Figure 5.6 indicates that the bulk minority carrier lifetime of String Ribbon silicon improves after each processing step. The greatest improvement in the minority carrier lifetime was seen after phosphorus gettering and hydrogenation from the SiN film. This increase after phosphorous gettering and

hydrogenation is very significant in comparison to the small change in lifetime after hydrogenation alone of the he as-grown material. This results indicates that hydrogenation of String Ribbon silicon is effective after phosphorus gettering. The bulk lifetime increased slightly after phosphorous gettering, hydrogenation, and aluminum alloying at 700°C for 30 seconds, but increased significantly to 59 μs after phosphorous gettering, hydrogenation, and aluminum alloying at 850°C for 2 minutes. While the bulk lifetime of String Ribbon silicon did not change after hydrogenation alone, the synergistic effect of phosphorous and aluminum gettering and hydrogenation increased the bulk lifetime from 1 μs to 59 μs.

5.3.4 Conclusions

String Ribbon silicon can be a cost-effective photovoltaic material if the bulk minority carrier lifetime can be increased so that the L/W >1. To maintain the cost-effectiveness of String Ribbon silicon, the solar cell fabrication steps must be low cost. The objective of this experiment was to investigate the effect of commercially viable technologies such as rapid thermal beltline furnace processing, screen-printing, and PECVD SiN on the bulk lifetime of String Ribbon silicon.

The results of the experiment indicate that hydrogenation from a PECVD SiN source alone is not effective in increasing the lifetime from the as-grown value of 1 μs. However, with phosphorous pre-gettering, hydrogenation increases the bulk lifetime to 38 μs. The addition of aluminum gettering increases the bulk lifetime to 59 μs. The effect of defect passivation by hydrogenation may not be seen in the as-grown material because the lifetime may be dominated by a lifetime limiting impurity level. Only after

gettering these impurities can the effect of defect passivation be seen in the minority carrier lifetime.

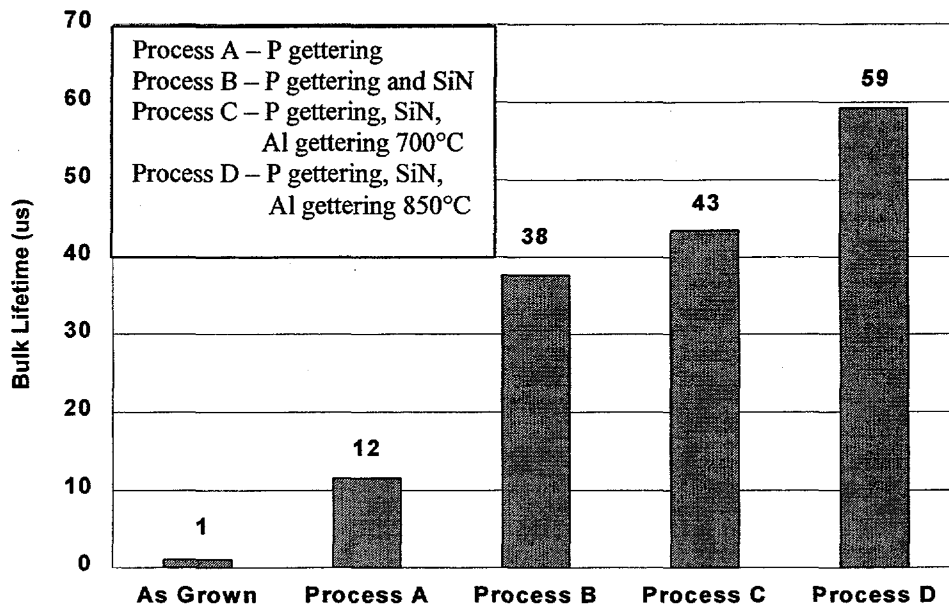


Figure 5.6 Bulk Lifetime of String Ribbon silicon after gettering treatments

5.4 High Efficiency 250 μm Thin String Ribbon Solar Cells by Rapid Thermal Beltline Processing and Screen-Printing

5.4.1 Introduction

The aim of this experiment is to simulate the CFP gettering and passivation techniques using the RT-BLP and screen-printing fabrication sequence and produce high efficiency screen-printed String Ribbon solar cells. The objectives were to investigate the effect of contact firing, Al-BSF formation time and temperature, emitter diffusion profile, and forming gas contact anneal on solar cell performance.

5.4.2 Experimental Procedure

Table 5.7 describes how the samples were prepared to investigate the objectives outlined above. Samples for each group were made in triplicate with each sample having four 4-cm2 solar cells.

Group	Emitter Sheet Rho	BSF	Front Contact Firing
A	25	850°C/2min	GT
B	25	co-fired GT	GT
C	45	850°C/2min	GT
D	25	850°C/2min	EG
E	25	co-fired EG	EG
F	45	850°C/2min	EG

Table 5.7 Experiment Matrix

Sample Cleaning

Samples were cleaned in a modified RCA acid clean and etched in 9:1 HNO_3:HF for 1 min at 15°C and in 100:1 HNO_3:HF for 3 min at 25°C.

Emitter Diffusion by RT-BLP

Samples were diffused to achieve a sheet resistance of 25 and 45 Ω/sq using a spin-on liquid dopant (*Filmtronics P507 6 %*) and RT-BLP. After emitter diffusion, the phos-glass was removed and the sheet resistance was measured. Samples were then cleaned in a modified RCA acid clean.

PECVD SiN deposition

SiN was deposited on the front surface of all samples to provide surface passivation, anti-reflective coating, and to serve as a source of hydrogen for bulk defect passivation.

Rear surface aluminum printing and firing

Aluminum paste (*Ferro 53-038*) was printed and baked on the back surface of all samples. Samples from groups A, C, D, and F were fired at a setpoint temperature of 850°C for 2 min in the beltline furnace. Samples from groups B and E were printed and baked, but not fired.

Front contact printing and firing

Silver paste (*Ferro 3349*) was printed and baked in a four-cell pattern on the front surface of all samples. Samples from group A, B, and C were fired at Georgia Tech at a peak setpoint temperature of 700°C for 30 seconds. Samples from groups D, E, and F were fired at Evergreen Solar.

Cell Isolation

Cells on all samples were isolated using a dicing saw.

Pre-FGA light IV measurement

FGA

All samples were annealed in forming gas for 15 min at 400°C.

5.4.3 Results and Discussion

Forming Gas Contact Anneal

Table 5.8 and Table 5.9 list the average solar cell efficiency before and after FGA respectively.

Group	V_{oc}	J_{sc}	FF	Eff
A	562	26.1	0.394	6.1
B	554	26.29	0.449	6.7
C	571	30.3	0.448	7.8
D	570	30.3	0.721	12.4
E	557	28.9	0.692	11.1
F	585	31.9	0.67	12.5

Table 5.8 Pre-FGA Average Light IV Data

Group	V_{oc}	J_{sc}	FF	Eff
A	556	27.8	0.689	10.7
B	546	27.5	0.691	10.4
C	566	30.6	0.603	10.5
D	561	29.7	0.751	12.5
E	556	28.7	0.741	11.9
F	582	31.9	0.736	13.7

Table 5.9 Post-FGA Average Light IV Data

The results indicate that the contact firing performed at Evergreen Solar yielded higher voltage and current response as well as higher average fill factors in comparison to those fired at Georgia Tech. Groups C and F were processed identically with the exception of the front contact firing step. Cells in Group F (fired at Evergreen Solar) were on average 6.4 % (absolute) higher than those in Group C (fired at GT). This large difference in cell

performance is attributed to the front contact firing time and temperature. However it is possible that the material in Group F was of a higher quality than that in Group C.

Contact Firing

Table 5.10 contains the results of five parameter fits of the dark IV curves of a cell fired at Evergreen and a cell fired at Georgia Tech to extract J_{o1}, J_{o2}, n_2, R_{sh}, and R_s. The

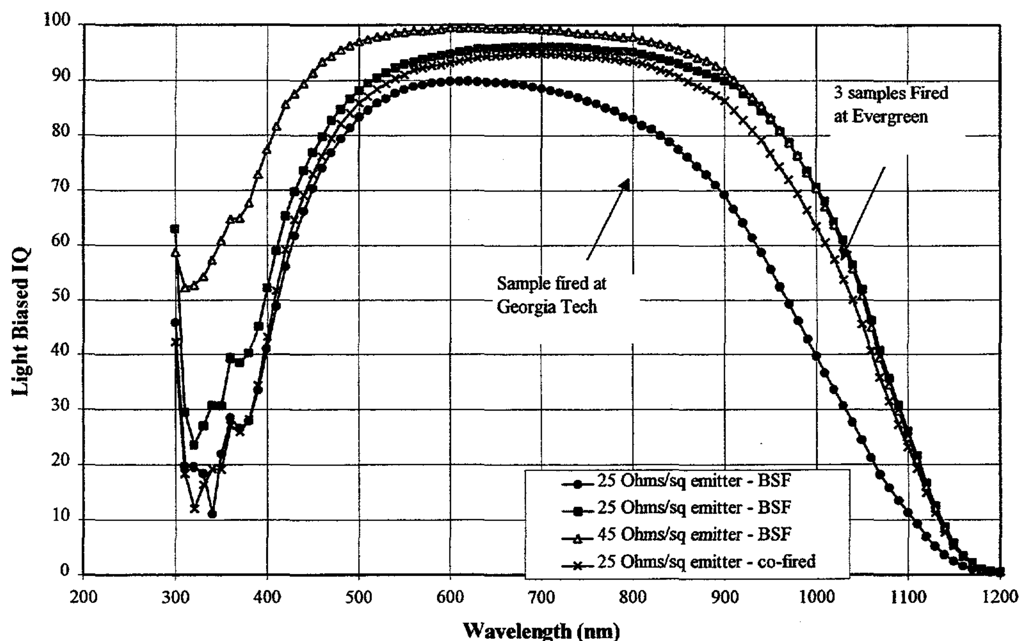


Figure 5.8 Light Biased IQE of Cells fired at Georgia Tech and Evergreen Solar

fits reveal that the higher fill factor of the cell fired at Evergreen is due to a higher shunt resistance, lower series resistance, n_2, J_{o1}, and J_{o2}. Identification of a single parameter responsible for the difference in fill factor is difficult. A contact resistance study of the contact firing at Evergreen and Georgia Tech before and after FGA should indicate if the difference is in the quality of the contact. The effect of the contact firing profile is not only seen in the fill factor of the cells, but also in the voltage and current. This result

indicates that there may be an improvement in the bulk lifetime of the samples fired at Evergreen Solar.

Figure 5.8 indicates that there may be an improvement in the long wavelength response of string ribbon cells from the combination of PECVD SiN and the spike firing contact anneal. While this observation is supported by cell IV data, it is not yet known if the variability in material quality may be responsible for the difference in the long wavelength response. Experiments to reproduce the observation that cells fired with a spike firing profile have an increased long wavelength response are underway.

The cells that were fired at Georgia Tech showed an increase in efficiency after the forming gas contact anneal. Cells fired at Evergreen Solar also improved after the forming gas anneal step, but not as dramatically. The efficiency improvement of the cells after FGA is mainly due to an increase in the fill factor. It has been shown at Georgia Tech that the contact resistance of cells fired at GT decreases after FGA, increasing the fill factor. The IV data of cells after forming gas contact anneal (in Table 5.9) is used to illustrate the remaining results of the experiment.

Firing	J_{o1}	J_{o2}	n_2	R_{sh}	R_s	FF
	(mA/cm^2)	(mA/cm^2)		(Ω-cm^2)	(Ω-cm^2)	
Georgia Tech	8.00E-12	4.00E-07	2.5	7000	0.8	0.653
Evergreen	2.00E-12	4.00E-08	1.9	13000	0.45	0.751

Table 5.10 Dark IV Five Parameter Fit Results

Emitter Doping

The effect of emitter doping on cell performance can be seen in the comparison of Group F (45 Ω/sq) and Group D (25 Ω/sq). Figure 5.8 suggests that the cells with the 25 Ω/sq emitter have a lower average efficiency due to increased recombination in the emitter resulting in a lower short wavelength response. While the fill factor of Group D is higher than that of Group F, the current loss in the heavily doped emitter decreases cells performance.

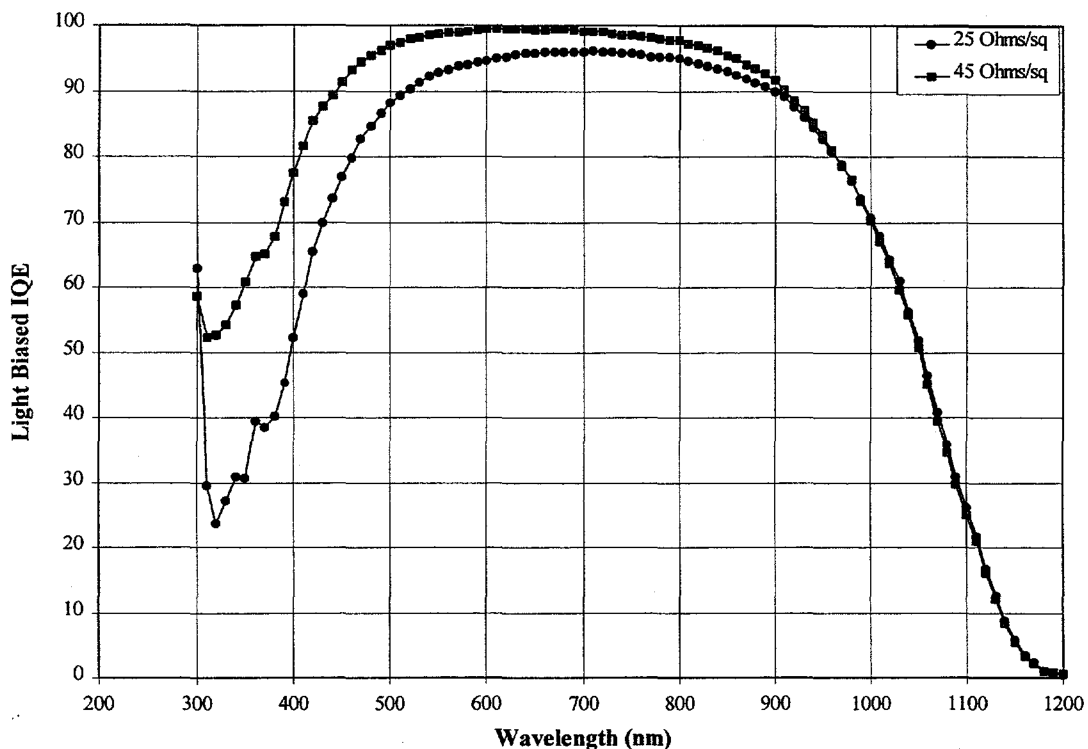
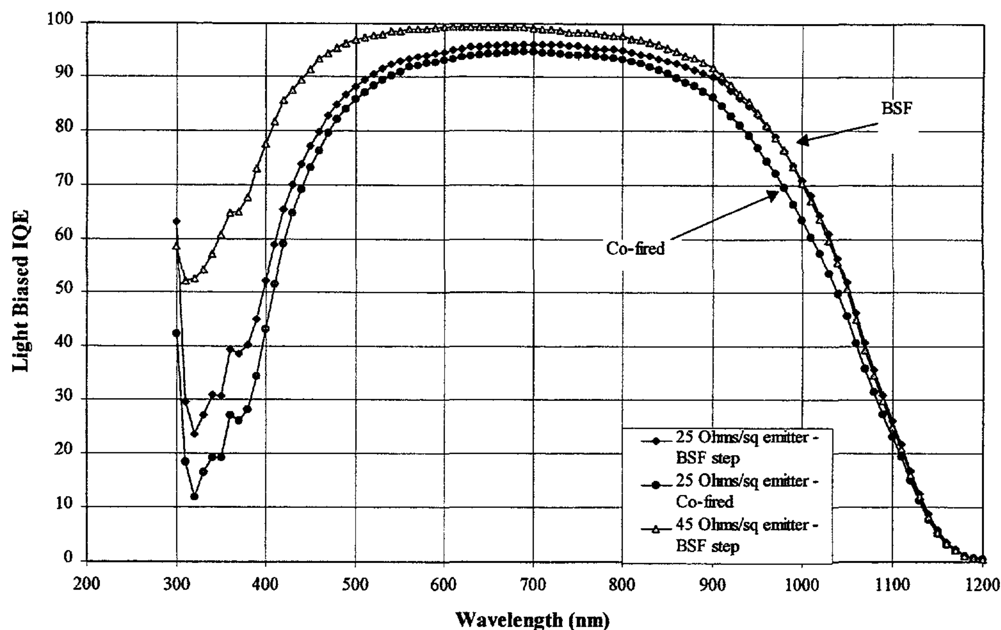


Figure 5.9 Effect of Emitter Doping on Short Wavelength Response

Al-BSF formation

To investigate the effect of Al-BSF formation time and temperature on cell performance, Groups D and E are examined. The back surface of samples of Group D was formed by screen-printing aluminum and alloying at a setpoint temperature of 850°C



for two minutes in the beltline furnace. Samples from Group E were co-fired at Evergreen Solar, and therefore did not see the BSF formation step. The overall efficiency of cells from Group D was greater than that of Group E.

Figure 5.10 Effect of BSF alloying on long wavelength IQE

Figure 5.10 illustrates that there may be in increase in the long wavelength response of string ribbon solar cells with the addition of a dedicated BSF formation step in the process sequence. Again, non-uniform material quality may be responsible for the observed difference in long wavelength IQE. Further experiments to reproduce this effect are necessary to reproduce the effect of the addition of a dedicated BSF formation step.

If the effect of the BSF step can be reproduced, the back surface recombination velocity of the two passivation schemes can be measured using the combination of IQE and bulk lifetime measurements. The effective minority carrier diffusion length (L_{eff}) of both passivation schemes can be determined from the long-wavelength IQE. The back

surface recombination velocity (S_{back}) can be determined by measuring the bulk lifetime and fitting the long wavelength IQE with different values of S_{back}. A comparison of L_{eff}, S_{back}, and bulk lifetime for the two different back passivation schemes will more clearly indicate if the improvement in cell performance is due to a difference in the back surface passivation or the material quality.

Solar Cell Efficiency Confirmation

The highest cell efficiency achieved was 14.87% (confirmed by SNL) with a combination of RT-BLP, PECVD, and screen-printing. The IV data of the cells measured by Sandia National Labs is listed in Table 5.11. A total of four cells were measured above 14.0% at Georgia Tech.

Cell	Voc (V)	Jsc (mA/cm^2)	FF	Eff (%)
A2-2	0.543	26.66	0.710	10.27
D2-4	0.579	29.73	0.765	13.19
E1-4	0.585	30.43	0.759	13.51
F3-1	0.592	31.24	0.773	14.33
F3-2	0.600	32.75	0.743	14.58
F3-3	0.595	32.50	0.770	14.87
F3-4	0.590	32.30	0.775	14.75

Table 5.11 Light IV Data of cells measured by Sandia National Labs

5.4.4 Conclusions

The purpose of this experiment was to investigate the 1) effect of contact firing, 2) Al-BSF formation, 3) emitter doping, and 4) forming gas contact anneal on solar cell performance. The average fill factor of cells fired at Evergreen Solar had a higher fill

factor and a higher efficiency than those fired at Georgia Tech. Unexpectedly, the voltage and current of the cells fired at Evergreen Solar was also higher than those fired at Georgia Tech indicating that the firing cycle at Evergreen not only improved the contacts, but may have improved the bulk lifetime of the samples. The enhanced long wavelength response of cells fired Evergreen Solar suggest that there may be a form of defect passivation in the spike firing of contacts in the presence of a PECVD SiN film. Further investigation is necessary to separate the effect of the material quality and this defect passivation in the contact-firing step on cell performance. A low temperature anneal in forming gas improved the performance of cells fired at Georgia Tech and at Evergreen Solar, possibly due to an improvement in contact resistance. The average efficiency of cells with an additional Al-BSF formation step was higher than those that were co-fired. However, proper comparison of the back passivation schemes required that the bulk minority carrier lifetime, L_{eff}, and S_{back} be determined for both schemes. The cells with the heavily doped emitter (25 Ω/sq) had a lower efficiency that those with a more lightly doped emitter (45 Ω/sq) due to increased emitter recombination. The highest cell efficiency was 14.9 % (confirmed by SNL) using an RT-BLP emitter, PECVD SiN single layer anti-reflective coating, screen-printed Al-BSF alloyed at 850°C, screen-printed contacts fired at Evergreen Solar, and a low temperature anneal in forming gas.

5.5 Final Conclusions

The primary objectives of the research on Evergreen String Ribbon silicon in the past year have been to fabricate high efficiency solar cells with conventional furnace processing (CFP) and high efficiency solar cells with rapid thermal beltline processing (RT-BLP). The response of the material to gettering and passivation treatments has been studied in CFP cells in order to fabricate high efficiency cells. The results from the experiment in Section 1 show that the fast ramp Al-BSF formed in the RTP furnace with 2 μm of evaporated Al gave an efficiency of 15.4 %, similar to the efficiency of cells with 5 μm of evaporated Al and conventional furnace processing. This high efficiency cell also included hydrogenation from a 2-hour low temperature forming gas anneal.

A minority carrier lifetime investigation using RT-BLP, PECVD, and screen-printing was performed to evaluate the response of String Ribbon to potentially low-cost gettering and defect passivation techniques. The results of the experiment indicate that hydrogenation from a PECVD SiN source alone is not effective in increasing the lifetime from the as-grown value of 1 μs. However, with phosphorous pre-gettering, hydrogenation increases the bulk lifetime to 38 μs. The addition of aluminum gettering increases the bulk lifetime to 59 μs. The gettering and passivation treatments were then adapted to the RT-BLP fabrication sequence along with screen-printing to produce high efficiency RT-BLP cells.

The highest efficiency cells fabricated by RT-BLP and screen-printing was 10.9 % (confirmed by SNL) on 100 μm and 14.8 % on 250 μm thick String Ribbon. In this year, considerable effort has gone into the adaptation of RT-BLP and screen-printing for

thin String Ribbon. An important result was that cells fired at Evergreen Solar outperform cells fired at Georgia Tech. An attempt to modify the contact firing profile at Georgia Tech is now underway.

A Novel Processing Technology for High-Efficiency Silicon Solar Cells

Introduction.

For widespread implementation of silicon photovoltaics, the cost as measured in dollars/watt must be reduced from the current level of $4/Watt to about $1/Watt to be competitive with fossil fuels [1]. Of the many components contained in a silicon solar cell module, the processed solar cells account for nearly 70% of the total cost. Thus it is imperative to reduce solar cell material and processing costs, while improving device performance to achieve a cost/Watt competitive with conventional energy sources. A typical n^+pp^+ silicon solar cell fabrication process incorporating a phosphorus emitter, boron (or aluminum) Back Surface Field (BSF), and thermal oxide surface passivation, requires anywhere from 2-5 high temperature furnace steps for the growth of masking and passivating oxides and dopant diffusions. Each high temperature step adds cost in terms of processing time and resources. In this paper we present a novel simultaneous boron and phosphorus diffusion technique capable of producing simple high-efficiency n^+pp^+ silicon solar cells in one furnace step. This process incorporates many significant efficiency -enhancing features, and is completely compatible with the current PV manufacturing technology base.

Historically, the simultaneous diffusion of boron and phosphorus in silicon has been implemented in several ways. For example, using boron and phosphorus Spin-On Dopants (SOD) films, boron and phosphorus can be simultaneously diffused in a rapid thermal processor [2] or in a conventional diffusion furnace [3], without significant cross doping. The drawbacks of this approach are that the wafers are left with a thick diffusion glass which in most cases must be removed in order to apply an effective antireflection coating, thus eliminating any potential for *in-situ* oxide surface passivation. In addition, our experience has been that it is often difficult to obtain high minority carrier lifetimes in processed wafers using commercially available boron spin-on dopants, due to residual impurities in the films. An alternative approach towards simultaneous boron and phosphorus diffusion is to deposit B and P-doped oxides on opposite sides of a silicon wafer using Chemical Vapor Deposition (CVD) techniques [4], prior to a high temperature diffusion. A major drawback of using CVD-doped oxides in a solar cell fabrication line is the costs associated operating and maintaining a CVD system, which typically uses the highly toxic gasses PH_3, B_2H_6 and SiH_4. While this process has been used to produce high performance solar cells [4], again one is still left with a thick diffusion glass which needs to be removed and a passivating oxide re-grown, requiring an additional high temperature cycle.

The approach used in our work is to simultaneously diffuse phosphorus and boron in a conventional diffusion furnace using solid doping sources containing extremely low concentrations of boron and phosphorus oxides. The solid doping sources are fabricated from dummy silicon wafers coated with phosphorus and boron spin-on dopants, containing controlled amounts of the volatile dopant species. It is shown in this paper that by using *limited* solid doping sources fabricated in this way, in one furnace step one can independently tailor the

phosphorus and boron diffusion profiles to be compatible with high efficiency solar cell designs. It is also shown that by using this approach the resulting diffusion glass is extremely thin (~60 Å), allowing for the growth of a high quality *in-situ* thermal oxide for surface passivation, without appreciably increasing the device reflectance. A model is presented to describe the dependence of sheet resistance on the dopant source concentration, and is used to explain the observed sheet resistance dependence on surface morphology. In addition to demonstrating flexibility in process design as well as *in-situ* oxide surface passivation, a powerful contamination filtering action is observed in the case of boron diffusions. This filtering action is used to obtain extremely high bulk minority carrier lifetimes in excess of 1 ms for wafers facing a boron SOD-coated source wafer, which in itself had a processed lifetime as low as 6 μs after a typical diffusion/oxidation cycle. Finally, we present typical results for devices fabricated from the described simultaneous diffusion and *in-situ* oxidation process, where 19-20% efficient solar cells are produced in one furnace step.

This paper is organized as follows: In the following section we present the experimental procedure for the simultaneous boron and phosphorus diffusion technique. Next, a model is presented which describes the reaction pathways for the limited diffusion sources developed in this work. This model is used to explain two unique attributes of this process dealing with *in-situ* oxide surface passivation and the dependence of sheet resistance on surface morphology. Next, we demonstrate a powerful impurity filtering action obtained through implementing a separate source/sample arrangement, resulting in high minority carrier lifetimes from a relatively impure boron spin-on dopant source. Finally we apply this knowledge to the fabrication of silicon solar cells with resulting conversion efficiencies in the 19-20% range, demonstrating the potential of

this novel processing technique to produce simple, high efficiency n^+pp^+ silicon solar cells in one high-temperature step.

II Experimental

Figure 6.1 shows the furnace stacking arrangement for the described boron and phosphorus simultaneous diffusion technique. The boron and phosphorus solid doping sources, B and P respectively, are interleaved with the solar cell sample wafers, S, with the back side of the solar cell wafers facing the boron sources and the front side facing the phosphorus sources. The boron and phosphorus sources are fabricated from 100 mm diameter dummy silicon wafers, coated with 1-2 ml of phosphorus or boron spin-on dopant film containing a controlled concentration of the volatile dopant compound. The phosphorus and boron SOD's used in this work were supplied by Filmtronics Incorporated and were found to be of consistently high quality. After applying the SOD to the sources, the wafers were spun on a clean delrin plastic chuck and baked on a clean quartz sheet on top of a 150 °C hotplate for 3 min (boron) or for 10 min (phosphorus), and loaded directly into the furnace. A typical simultaneous diffusion cycle is to load the wafers at 800 °C in N_2, ramp up to 900-1000 °C and diffuse in N_2 or Ar_2 for 60 minutes. If an *in-situ* oxide is required, a low O_2 flow is added to the N_2 ambient for 5-60 min depending on the desired oxide thickness, and the furnace ramped down to 700 °C at a rate of 4 °C /min, and the wafers pulled in a high N_2 flow. The source wafers are recycled (as sources) after each diffusion cycle, following a brief dip in 10% HF and re-application the phosphorus or boron SOD. It should be noted that the source wafers are depleted of the dopant compounds

after one diffusion cycle, and need to be re-fabricated as doping sources prior to each diffusion step. This is not a significant drawback of

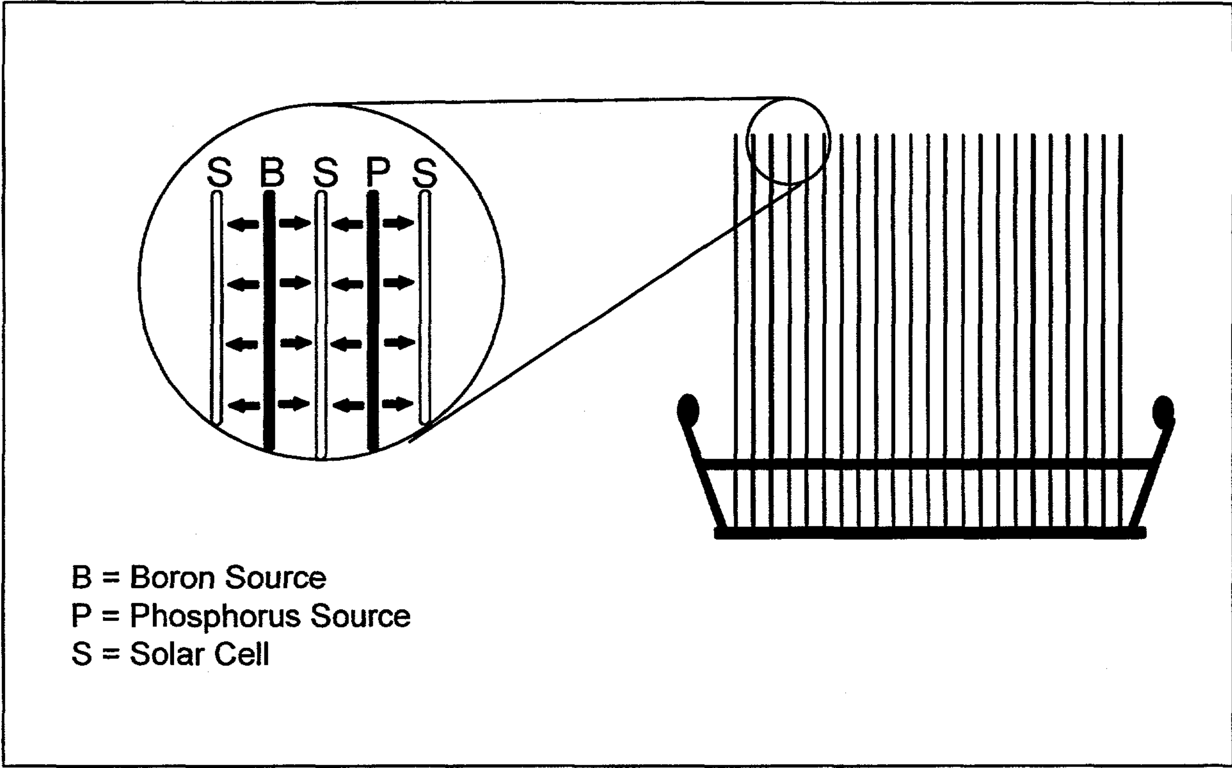


Figure 6.1. Furnace stacking arrangement, with the solar cell wafers (S) interleaved with the Boron (B) and Phosphorus (P) solid sources developed in this work.

this technique since the source wafers can be fabricated by high throughput techniques such as spray coating or dip-coating full wafer cassettes. As shown below, the limited nature of the solid doping sources enables several high efficiency features to be realized in one furnace step using this simultaneous diffusion technique. It is noted that this process is similar to a previous approach [5] in which we had fabricated the boron and phosphorus sources by growing a doped oxide on the source wafers using $POCl_3$ and BBr_3. From a practical point of view the implementation of this process using SOD's has several advantages over $POCl_3$ and BBr_3, such as the elimination of separate $POCl_3$ and BBr_3 diffusion furnaces and the precautions associated with handling these pyrophoric chemicals, and the ability to reproducibly obtain high minority carrier lifetimes using a boron SOD in place of BBr_3 to fabricate the boron sources.

III Results and Discussion

A. Process Flexibility

To simultaneously form the emitter and BSF diffusions for a high efficiency cell design, it is important to have the flexibility of independently tailoring the resulting boron and phosphorus diffusion profiles for a given thermal budget. Figure 6.2 shows the flexibility in diffused sheet resistance ($?_s$) as a result of tailoring the concentration of dopant compounds in the SOD films applied to the source wafers. Measurements were made on 100 mm diameter, 500-1000 Ω-cm n-type, (100) float zone silicon wafers, with the error bars representing 1 standard deviation for 16 measurements across a 49 cm^2 area. It is noted that all the samples in figure 6.2 were diffused using the same 1000 °C/60 min diffusion cycle, with the only variable being the

concentration of dopant compounds in the SOD's applied to the source wafers. The dopant compound in the phosphorus

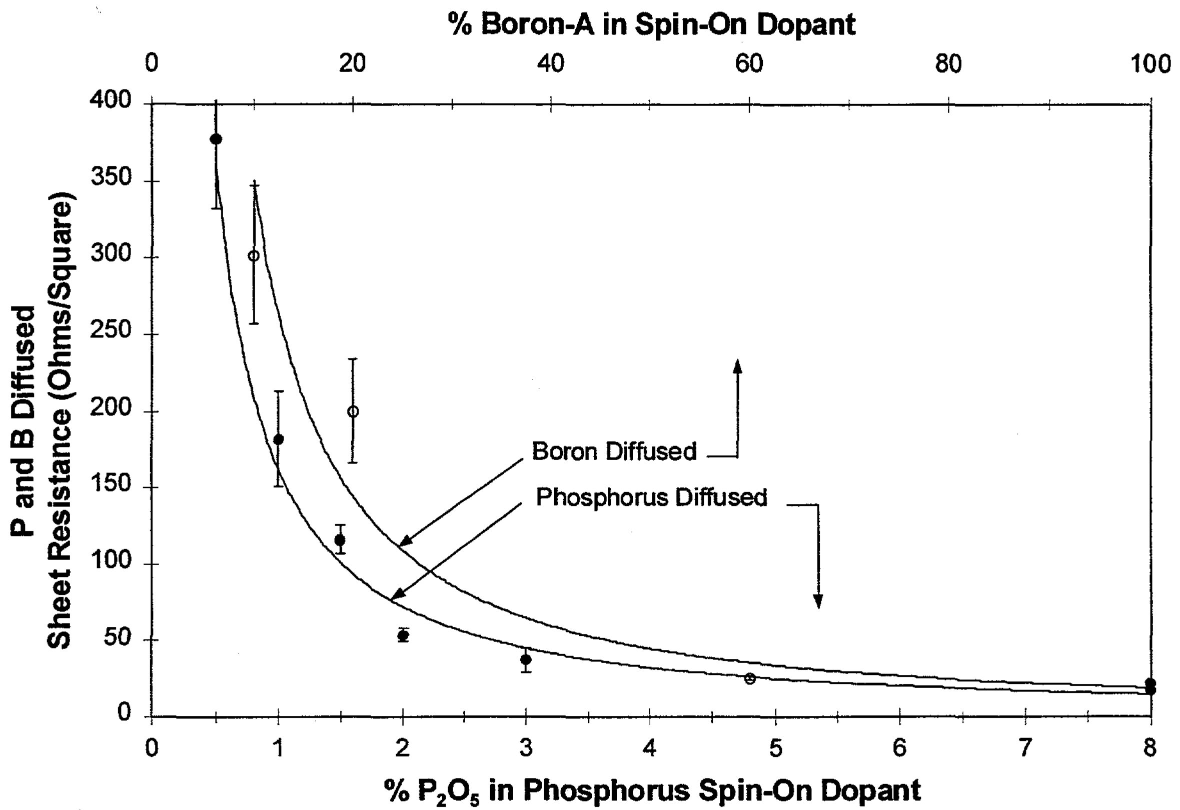


Figure 6.2. Dependence of phosphorus and boron-diffused sheet resistance on source fabrication conditions for a 1000 °C/60 min process. The phosphorus sources were tailored by adjusting the concentration of P_2O_5 in the SOD film, while the boron sources were tailored by diluting the 100% Boron-A SOD film with toluene.

SOD is P_2O_5, which was varied to obtain a wide range of diffusion profiles ranging from 17 to 378 Ω/□. The boron SOD, sold under the product name Boron-A, is made from a proprietary boron polymer dissolved in cyclohexane, and was diluted by the manufacturer using semiconductor grade toluene. The % listed on the top x-axis is the % by volume of the Boron-A SOD sold by Filmtronics. As was the case with phosphorus, a wide range of boron diffusions, ranging from 22 to 302 Ω/□ can be obtained by diluting the boron SOD applied to the source wafers. Thus based on the data in figure 6.2, one can easily obtain a boron BSF having a low sheet resistance in the 20 Ω/□ range, and a phosphorus emitter compatible with either screen printing metallization requiring ~ 50 Ω/□ or photolithography-based metallization where ~ 85 Ω/□ is optimal, using a 1000 °C 60 min diffusion cycle.

The dependence of sample sheet resistance on the concentration of dopants on the source wafers observed in figure 6.2 is quite different than what is observed with conventional solid doping sources. Commercially available solid sources, such as silicon pyrophosphate (SiP_2O_7)-based solid sources [6,7] and boron nitride solid sources [8] are designed to be used for hundreds of hours, and essentially deposit infinite amounts of P_2O_5 and B_2O_3 respectively, so that the surface concentrations approach the dopant solid solubility at a given diffusion temperature. Using data from reference [7], if conventional phosphorus solid sources were used under conditions required for a deep boron BSF (~1000°C/30 min), the sheet resistance would be approximately 4 Ω/□. If solar cells were made using this emitter profile, heavy doping effects would result in low quantum efficiencies for UV and visible radiation absorbed near the surface, thus lowering the cell efficiency. In addition, the residual oxide thickness deposited from the SiP_2O_7 solid sources would be on the order of 750 Å for a 30 minute diffusion at 1000 °C [7],

which would result in a high optical reflectance if incorporated into a module. For this reason, most manufacturers remove the phosphorus diffusion glass and deposit an appropriate anti-reflection coating prior to encapsulating the solar cells, thereby eliminating any passivating effects of the diffusion glass.

B. Residual Oxide Thickness

Figure 6.3 shows the residual oxide thickness for boron and phosphorus diffused samples resulting from the limited solid doping sources developed in this work. The three sets of data are for boron and phosphorus diffusions at 1000 °C for 60 min in N_2, at which point the wafers were cooled to either 700 °C (open and closed circles for B and P respectively), or to 100 °C for a second set of phosphorus diffusions, and pulled into a cleanroom ambient. In comparing the B and P diffused samples pulled at 700 °C, it appears that the residual glass thickness is approximately the same value for both dopants, for sheet resistance ($?_s$) values greater than about 30 Ω/□. For $?_s$ values below about 30 Ω/□, the glass thickness rises sharply with decreasing $?_s$, and the differences in glass thickness between boron and phosphorus diffused samples becomes more pronounced. One plausible explanation for the same glass thickness being measured on B and P diffused samples pulled at 700 °C is that a native silicon oxide is growing while the wafers are pulled into the cleanroom ambient. To investigate this idea, selected phosphorus diffusions were repeated, with the wafers cooled in N_2 and pulled at 100 °C so that any native oxide grown would be much thinner than if pulled at 700 °C. Figure 6.3 shows that the residual glass thickness for wafers pulled at 100 °C is essentially the same value than if pulled at 700 °C, and therefore that the 50-60Å of residual glass is a by-product of the (limited) diffusion sources.

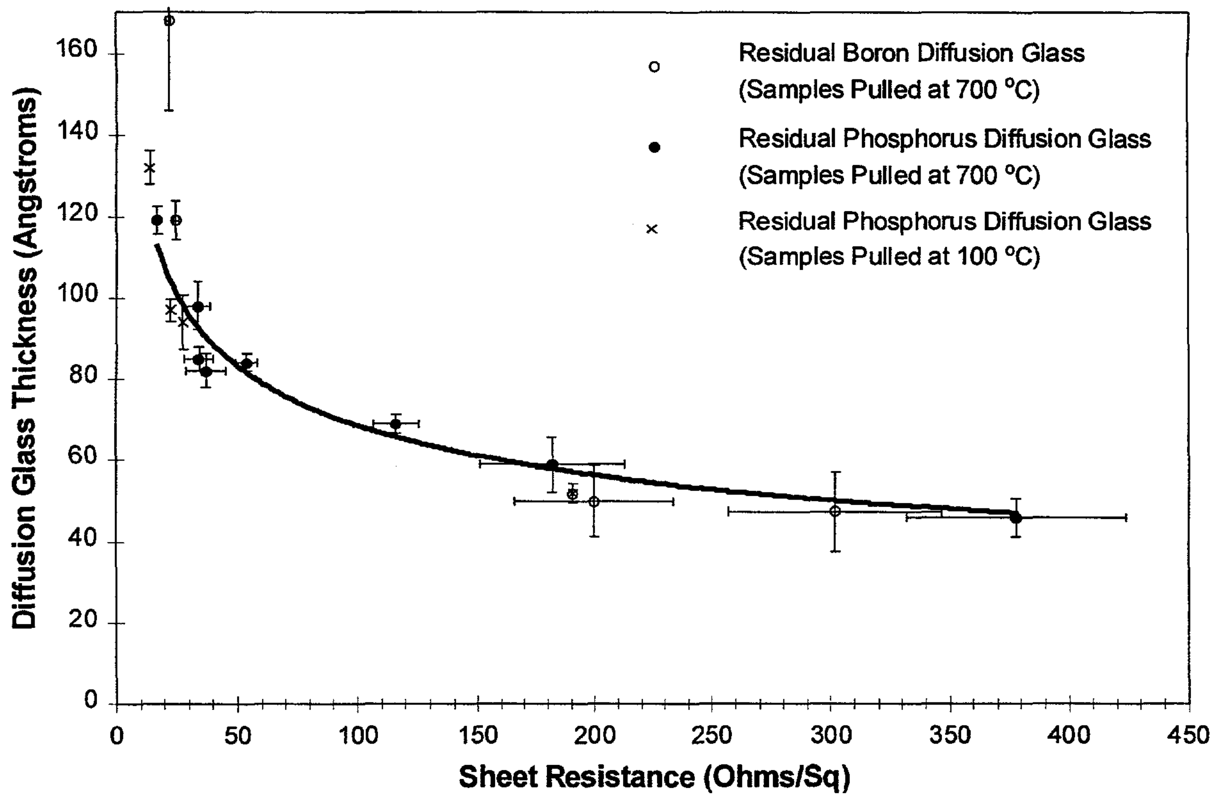
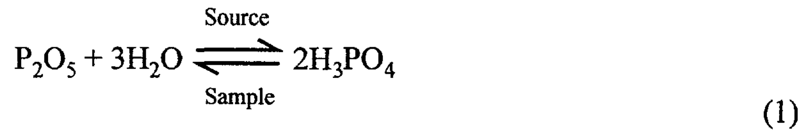


Figure 6.3. Residual diffusion glass thickness vs. sheet resistance for a 1000 °C/60 min process in N_2 for phosphorus and boron diffusions, with no *in-situ* oxidation.

C. Proposed Model

The results of the above experiments could be interpreted in several ways. One explanation is that below 700 °C, the partial pressure of the phosphorus species liberated from the source wafer is negligible, therefore no additional dopant is deposited below 700 °C to increase the residual glass thickness (fig 3). If that were true, then the phosphorus sources would be re-useable for additional diffusion cycles, which we have found not to be the case. A more likely situation is that the dopant sources used for lower surface concentrations (i.e. $?_s$>30Ω/□) deposit a limited dose of volatile dopant species which is *consumed* by the intended sample instead of piling up on the silicon surface, which would lead to the formation of a thick glass layer.

The phosphorus SOD used in this work is an industry-standard solution of P_2O_5, H_2O, tetraethylorthosilane (TEOS), and ethanol. The hotplate bake prior to diffusion serves to drive off the ethanol solvent leaving a glassy phosphosilicate film (PSG). As temperatures are increased toward the target diffusion temperature (900-1000 °C), the PSG film polymerizes to form SiO_2, H_2O and C_2H_4 [9,10]. It is well known that P_2O_5 is extremely hygroscopic, and will react with H_2O in the SOD film, as well as with trace amounts of moisture in the process gasses, to form the volatile species H_3PO_4 (phosphoric acid), which is weakly bonded to the PSG structure. It is assumed that this is the phosphorus containing species transported from the source to the sample wafer. On the sample surface, the reverse reaction takes place whereby H_3PO_4 reacts to form P_2O_5, with H_2O as a byproduct; a process which was shown to occur during the direct vaporization of H_3PO_4 at elevated temperatures [12].



$$P_2O_5 + 3H_2O \underset{\text{Sample}}{\overset{\text{Source}}{\rightleftharpoons}} 2H_3PO_4 \qquad (1)$$

The pentoxide of phosphorus, P_2O_5, deposited on the sample surface proceeds to react with silicon to form SiO_2 and P, which preferentially diffuses into silicon:

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P \qquad (2)$$

For the case of limited doping sources, we propose that the starting thickness of P_2O_5 formed on the sample surface is extremely thin, and is limited by the dose of H_3PO_4 from the source. During the diffusion cycle reaction (2) is essentially driven to completion, resulting in a thin layer of SiO_2 rich glass on the sample surface, and the surface concentration of P below the solid solubility. Thus by controlling the concentration of P_2O_5 in the SOD film, we can limit the dose of H_3PO_4, and thus the thickness of P_2O_5 on the sample, allowing the underlying silicon to consume virtually all of the available phosphorus for surface concentrations below the solid solubility. As the P_2O_5 content in the SOD is increased, resulting in a greater dose of H_3PO_4, the residual P_2O_5 layer on the sample exceeds what can be consumed during the diffusion cycle. At this point, the sources used in our process behave like conventional phosphorus solid sources in which the P_2O_5 supply exceeds what the sample can consume, resulting in a fixed surface concentration which is limited by the diffusion temperature (i.e. solid solubility). This concept is shown schematically in figure 6.4, in which the surface concentration increases with P_2O_5 thickness on the sample until the supply of phosphorus exceeds the solid solubility, at which

point the surface concentration is fixed by the phosphorus solid solubility for increasing P_2O_5 thickness.

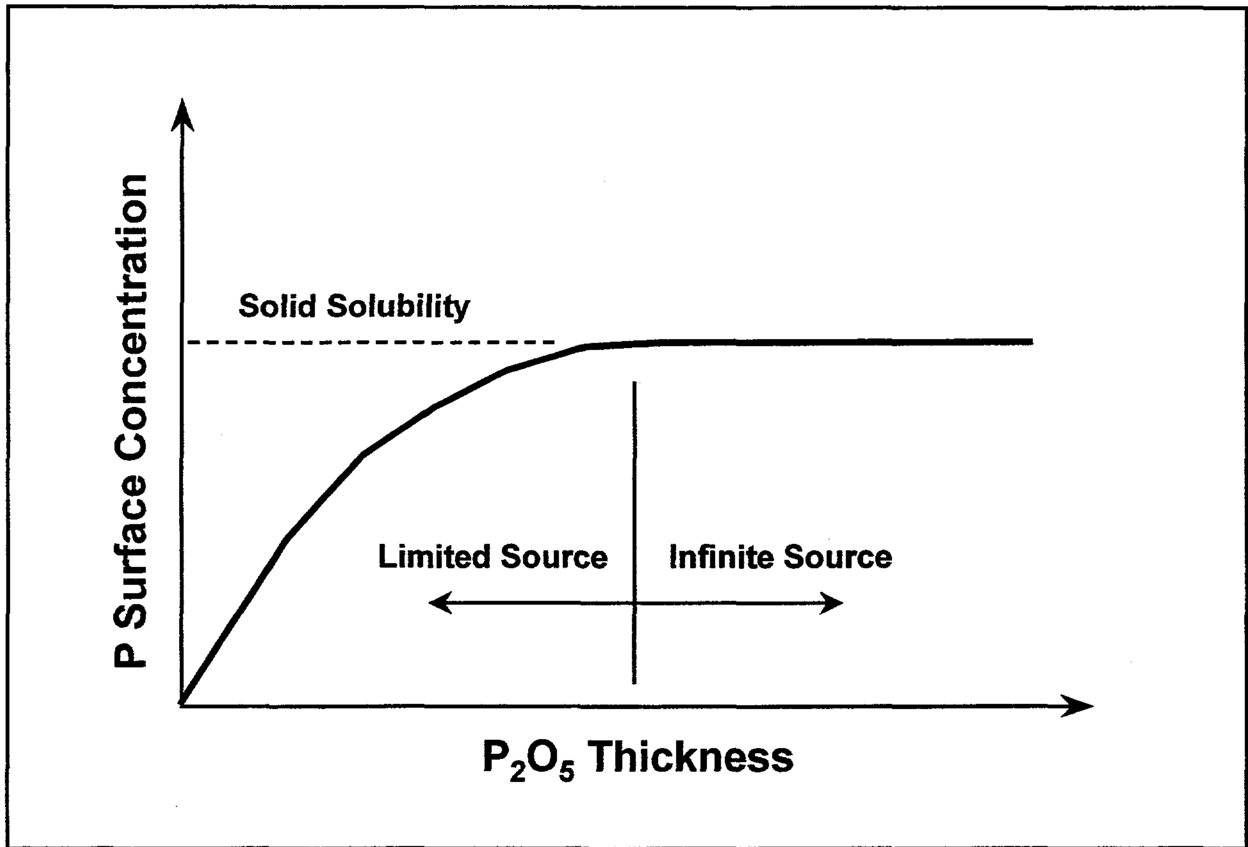


Figure 6.4. Proposed reaction pathway for phosphorus diffusions using solid sources fabricated from a spin-on dopant film.

This result is notably different than conventional SiP_2O_7-based solid sources which are designed to be reused for hundreds of hours. These conventional solid sources continually deposit a stream of P_2O_5 on the sample wafers, which results in a thick layer of diffusion glass on the surface [7], and thus provides a supply of phosphorus which exceeds the solid solubility. In this case the surface concentration is ultimately limited by the solid solubility of P in Si, and thus the only degrees of control is the diffusion temperature and time. But by fabricating solid doping sources in the limited source regime we can now control the (diffused) surface concentration by controlling the SOD source concentration.

The situation for boron diffusions is analogous to phosphorus. The Boron-A film used in these experiments is a proprietary boron-based polymer dissolved in cyclohexane and diluted with toluene, which converts directly to B_2O_3 at about 450 °C. It is likely that B_2O_3 is directly transported from the source to sample wafer, although HBO_2 which has a much higher vapor pressure than B_2O_3 is known to form in the presence of even trace amounts of moisture [13, 14]. For the case of limited boron diffusions, the reactions on the sample surface proceed as in the case of phosphorus:

$$2B_2O_3 + 3Si \rightarrow 3SiO_2 + 4B \qquad (3)$$

resulting in a thin SiO_2-rich glass layer and a boron concentration below the solid solubility and a thick borosilicate glass layer for surface concentrations above the solid solubility. As explained below, an important advantage to using separate boron sources as fabricated in our process is the

ability to filter out impurities contained in the boron SOD film, resulting in very high processed bulk minority-carrier lifetimes.

The assertion that the doping sources fabricated in our simultaneous diffusion process results in a limited thickness of P_2O_5 or B_2O_3 onto the intended sample was tested by examining the dependence of sheet resistance, ?$_s$, on surface morphology. Figure 6.5 shows the resulting sheet resistance for the case of textured and planer sample wafers each facing the same phosphorus source, for a range of P_2O_5 concentrations in the SOD films. Surface texturing was achieved by etching upright pyramids with [111] oriented facets in the (100) silicon surface, using a weak alkaline solution at 80 °C for 30 min. Sheet resistance measurements were made by the four point probe technique, in which the sheet resistance is independent of the absolute probe spacing and is therefore assumed to be independent of the surface morphology [15]. All the planer and textured samples in figure 6.5 were diffused at the same time using a 925 °C diffusion cycle in N_2 for 60 min, followed by a 15 min *in-situ* oxidation. As the data in figure 6.5 shows, for low concentrations of P_2O_5 in the SOD films used to fabricate the sources, the textured wafers have a higher sheet resistance than the planer wafers by a factor of about 2 when facing the same sources. As the % P_2O_5 in the SOD film is increased, the difference in ?$_s$ is reduced until the ?$_s$'s for the textured and planer wafers approach the same value for the "infinite" P_2O_5 case, which corresponds to that of conventional solid sources. For comparison, diffusions were carried out using $POCl_3$ and conventional SiP_2O_7 - based solid sources, with textured and planer wafers diffused simultaneously. As shown in Table 1, the values of ?$_s$ for textured and planer wafers is nearly identical when using $POCl_3$ and conventional solid sources. However, in the case of

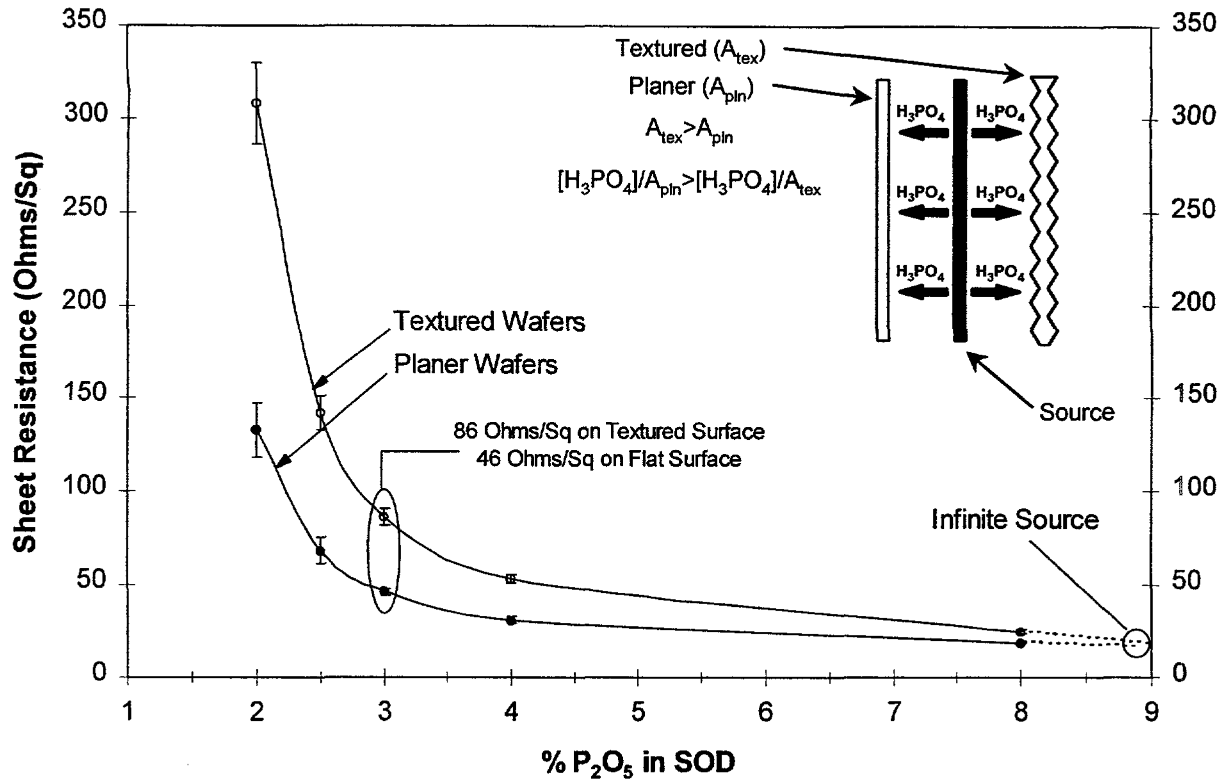


Figure 6.5. Dependence of sheet resistance on % P_2O_5 in phosphorus SOD film for a 925 °C/60 min process, for planer and pyramid-textured surfaces.

	Conventional Solid Sources	**$POCl_3$**	***Limited* Solid Sources**
Textured Wafer Sheet Resistance	101 Ω/□	82 Ω/□	*86 Ω/□*
Planer Wafer Sheet Resistance	98 Ω/□	88 Ω/□	*46 Ω/□*

Table 1. Comparison of conventional SiP_2O_7-based solid sources, $POCl_3$ and the limited solid sources developed in this work, to form light phosphorus diffusions on planer and textured silicon wafers.

limited solid sources used in this technique, the same source can produce an 86 Ω/□ textured emitter and a 46 Ω/□ planer emitter. This is because a fixed dose of H_3PO_4 impinging on a textured surface (with a larger surface area), results in a thinner P_2O_5 layer, which in turn results in a lower surface concentration and higher sheet resistance. Thus it appears that the limited solid sources used in this work are unique in their ability to deposit a fixed, relatively thin dose of dopant oxide, resulting in a clear dependence of sheet resistance on surface texturing.

The dependence of sheet resistance on surface morphology displayed in figure 6.5 using limited solid sources is a significant result because it offers a way of obtaining a selective emitter for screen-printed based metallization, which requires heavy diffusions under the metal grid contact, while maintaining a light diffusion in the textured field region with a well passivated surface. This could be achieved by patterning a suitable texture mask, such as PECVD SiN, to obtain a flat grid region and a textured field. For example, the data set in figure 6.5 shows that using a phosphorus SOD film containing 3% P_2O_5 to fabricate the sources, one can obtain 86 Ω/□ on a textured surface, which is ideal for high efficiency cell designs, and 46 Ω/□ on a flat region which is suitable for screen printing.

D. In-Situ Oxide Surface Passivation

Since the residual diffusion glass is thin for light phosphorus and boron diffusions formed using limited doping sources, a passivating thermal oxide can be grown *in-situ* thus eliminating the need for a diffusion glass removal step and additional high temperature oxidation cycle. To examine the passivating qualities of this thin *in-situ* thermal oxide, measurements were made of the emitter saturation current density (J_o) using the Photo-Conductance Decay (PCD) technique

[16] for both phosphorus and boron diffusions. By plotting the inverse effective lifetime 1/?$_{eff}$, as a function of injection level *n*, for a sample with identical diffusions and passivation on each side, the slope is proportional to the saturation current density, J_o according to the relation:

$$\frac{1}{\tau_{eff}} - C_n n^2 = \frac{1}{\tau_{bulk}} + \frac{2J_0}{q n_i^2 W_{bulk}} n \quad (4)$$

where C_n is the Auger coefficient, ?$_{bulk}$ the bulk minority carrier lifetime, W_{bulk} the bulk wafer thickness and n_i the intrinsic carrier concentration (at 25 °C). Table 2 shows the results of J_o measurements for 80-90 Ω/□ boron and phosphorus diffusions on un-textured 500-1000 Ω-cm n-type float zone wafers. The resulting J_o values for light boron and phosphorus diffusions are quite low, giving a value of 118 fA/cm^2 and 67 fA/cm^2 respectively for the case of *in-situ* oxide surface passivation. After removing the *in-situ* oxide in dilute HF and allowing a native oxide to form, the J_o's increased substantially to 404 fA/cm^2 in the case of boron and 809 fA/cm^2 for the case of phosphorus, thus demonstrating the superb passivating qualities of the *in-situ* oxide provided by this simultaneous diffusion technique.

E. Impurity Filtering

Boron diffusions are not widely used in the photovoltaic industry, which is due in large part to the difficulty in obtaining high minority carrier lifetimes, and forming the boron diffusions in a straight-forward, cost-effective way. Several groups have been successful [17, 18] at producing record high efficiency solar cells using BBr_3 as a boron source, but in our experience with BBr_3 it has proven to be difficult to reproducibly obtain high bulk lifetimes without extensive

Dopant	Sheet Resistance	Surface Passivation	J_o
Boron	83 Ohms/Sq	In-Situ Oxide	118 fA/cm^2
Boron	83 Ohms/Sq	Un-Passivated	404 fA/cm^2
Phosphorus	90 Ohms/Sq	In-Situ Oxide	67 fA/cm^2
Phosphorus	90 Ohms/Sq	Un-Passivated	809 fA/cm^2

Table 2. Saturation current density (Jo) measurements for in-situ oxide passivated and un-passivated 80-90 Ω/□ boron and phosphorus diffusions.

furnace gettering cycles prior to diffusion. In addition, the use of BBr_3 requires a masking oxide be grown prior to diffusion thus requiring an additional high temperature step which increases processing costs and complexity. Several groups have reported similar lifetime problems using boron nitride solid sources [19, 20]. In this work it was discovered that by fabricating boron solid sources out of silicon wafers, one could reproducibly obtain high bulk minority carrier lifetimes from a relatively impure boron SOD film. Figure 6.6 shows the results of PCD bulk lifetime measurements for boron diffused samples, in which the diffusions were etched and the surfaces passivated in 20% HF [21] during the measurement. High quality p-type (2.3 Ω-cm) float zone silicon was used in these experiments, and special care was taken at all stages to insure cleanliness of the diffusion process. In the first case, a 100% Boron-A film was a applied to a float zone wafer, which was subsequently boron diffused directly from the SOD film in a 60 min, 1000 °C thermal cycle in N_2. A second float zone wafer adjacent to the first was doped indirectly by the transport of B_2O_3 from *this* SOD film. From the inset of figure 6.6, at an injection level of $5(10)^{14}$ cm^{-3}, the minority carrier lifetime was 227 ?s for the wafer on which the boron SOD was directly applied (i.e. the source wafer), while the *adjacent* sample wafer had a much higher bulk lifetime of 1306 ?s. A more dramatic difference in bulk minority carrier lifetime is seen from the second set of samples in which a thick *in-situ* oxide was grown for 66 min at 1000 °C after the 60 min diffusion process in N_2 at 1000 °C. It is noted that the same lot of boron SOD film was used for the source wafers in figure 6.6. For the thick oxide case, the wafer which had the boron SOD directly applied had a low bulk lifetime of only 5.91 ?s, while the adjacent sample wafer had a bulk lifetime of 1010 ?s, corresponding to a factor of 171 higher. We have observed this behavior numerous times using 5 different lots of boron SOD

film manufactured over the course of three years. The mechanism responsible for impurity filtering can be understood conceptually

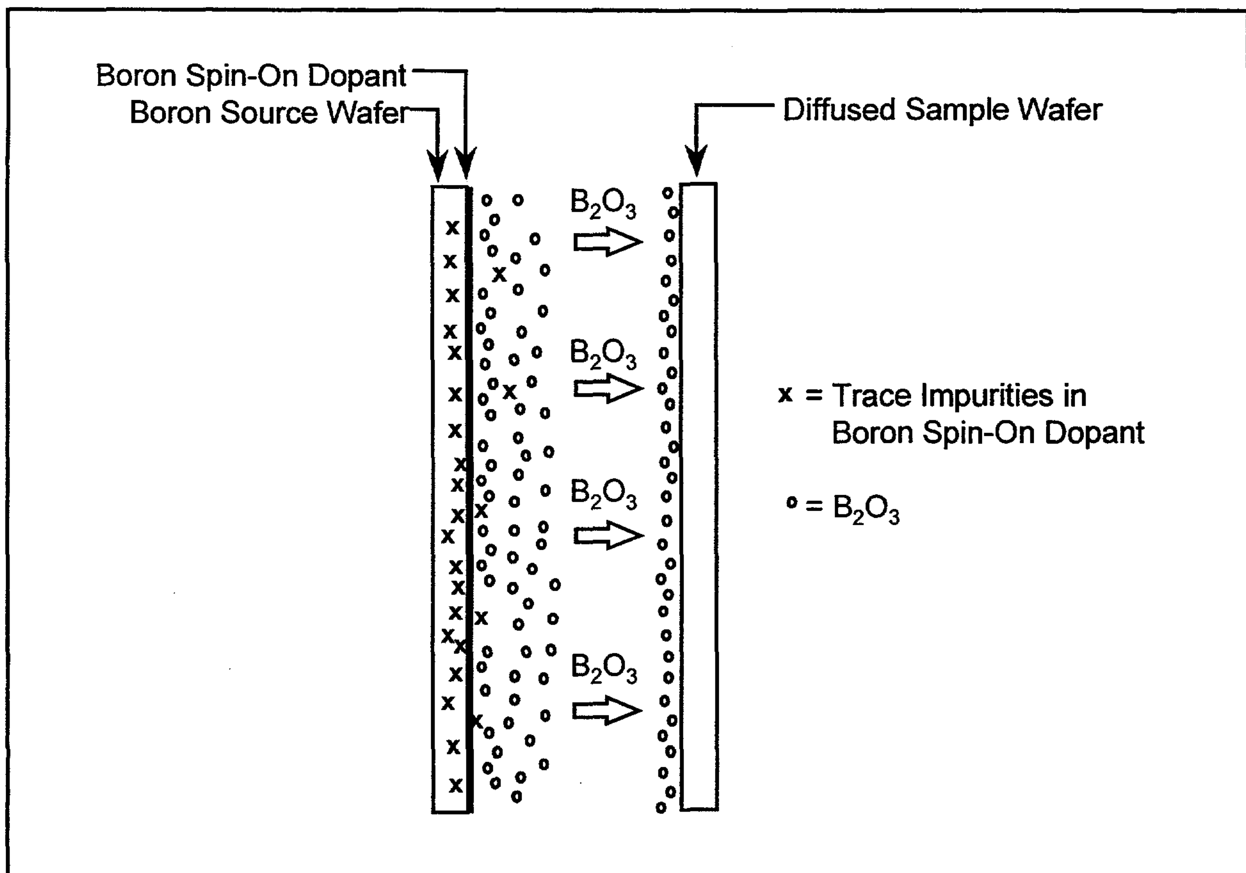


Figure 6.6. Demonstration of high minority carrier lifetimes due to impurity filtering from boron SOD-coated solid sources. Source 1 wafer on which the boron SOD was applied was facing Sample 1 in a 1000 °C/60 min process with no *in-situ* oxidation, while the Source 2 wafer was facing Sample 2 in a 1000 °C/60 min process with an additional 66 min *in-situ* oxidation at 1000 °C.

from figure 6.7. The impurity level in the Boron-A SOD used in this work is relatively high for achieving very high minority carrier lifetimes, containing levels of Fe, Cu, Ni, Cr, Mn in the 10 ppb range [22]. This is why it is generally difficult to obtain high lifetimes in excess of 1 ms using boron SOD sources. At diffusion temperatures of 1000 °C, the partial pressure of these trace metals is extremely low [23], so that in our diffusion scheme only the volatile B_2O_3 is transported from the source to sample wafer, leaving the impurities in the source wafer. Thus by simply fabricating boron sources out of silicon wafers using a commercially available boron SOD film, one can obtain clean boron diffusions and in the process benefit from the *in-situ* passivating oxide which from Table 2 resulted in J_o values in the 100 fA/cm^2 range.

F. Boron Gettering

Transition metals such as Fe, Cr, Cu and Ni are fast diffusing elements in silicon, and if present in the boron SOD film in 10 ppb levels will certainly degrade the lifetime of the p-type silicon float zone silicon wafers used in this work [24]. Thus it is interesting to note that the sample which was oxidized for an additional 66 min at 1000 °C had a substantially lower bulk lifetime than the sample diffused in a N_2 ambient for 60 minutes at 1000 °C. For fast diffusing metallic impurities such as Fe, Cu and Mn it is assumed that the diffusion lengths, $\sqrt{D_{metal}t}$, during a 60 min 1000 °C thermal cycle, is greater than the 300 ?m wafer thickness [25]. This type of lifetime dependence on oxidation was recently reported for p^+ diffusions formed using boron nitride solid doping sources [19], and was attributed to the re-injection of impurities from the p^+ region into the wafer bulk during a subsequent oxidation step. By growing an oxide on the p^+ diffused surface, the boron is preferentially segregated into the oxide [13], thus lowering

the diffused boron surface concentration. Recently, workers at Bell Laboratories [25] and elsewhere

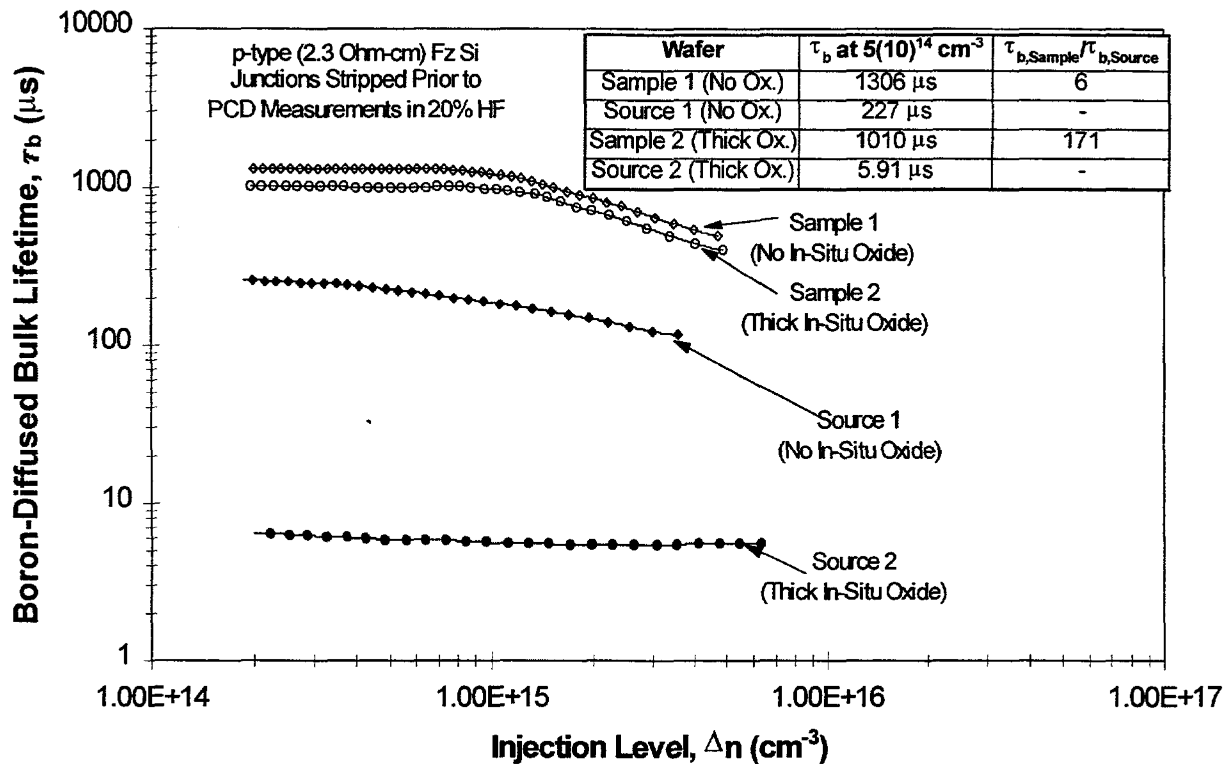


Figure 6.7. Schematic of impurity filtering action commensurate with boron SOD-coated source wafers: The impurities (X) in the SOD film are diffused into the source wafers while the volatile dopant species, B_2O_3, (O) is transported to the sample wafer, resulting in a high-purity boron diffusion.

[26] have shown that boron is effective at gettering transition metals such as Fe, Cr and Mn through the formation of metal acceptor pairs, and in the case of iron have shown a clear dependence of the gettering efficiency on the boron concentration in the gettering region [25]. Figure 6.8 shows the spreading resistance profiles for two boron diffused samples, in which one was diffused for 60 min at 1000 °C in N_2, and the other diffused for 60 min at 1000 °C in N_2, and *in-situ* oxidized for an additional 66 min at 1000 °C. A possible explanation for the lower bulk lifetime for the oxidized source wafer (fig 6) is the reduction in the *gettering efficiency* of impurities introduced by the boron SOD film, as a result of lowering the boron surface concentration (shown by the hatched are in figure 6.8) during the *in-situ* oxidation. It is noted that although no attempt has been made in this work to identify the lifetime limiting impurities or quantify the gettering effectiveness of boron, our results are consistent with those reported in the literature for boron gettering of the metallic impurities present in the Boron-A SOD film [25, 26]. This work demonstrates that one can obtain clean boron diffusions in a simple way (via impurity filtering), which makes this an ideal materials system for studying the gettering effectiveness of boron, and possibly boron and phosphorus co-gettering phenomena [27], in a process which is compatible with commercial solar cell manufacturing technology.

G. High Efficiency Silicon Solar Cells

Textured n^+pp^+ solar cells have been fabricated by this simultaneous boron and phosphorus diffusion process, and has reproducibly given over 19% efficiencies on float zone silicon for a variety of bulk resistivities. Figure 6.9 shows the results of light IV, internal quantum efficiency and reflectance measurements provided by Sandia National Laboratories.

The 4 cm^2 devices were fabricated from textured 2.3 Ω-cm (p-type) float zone silicon by simultaneously

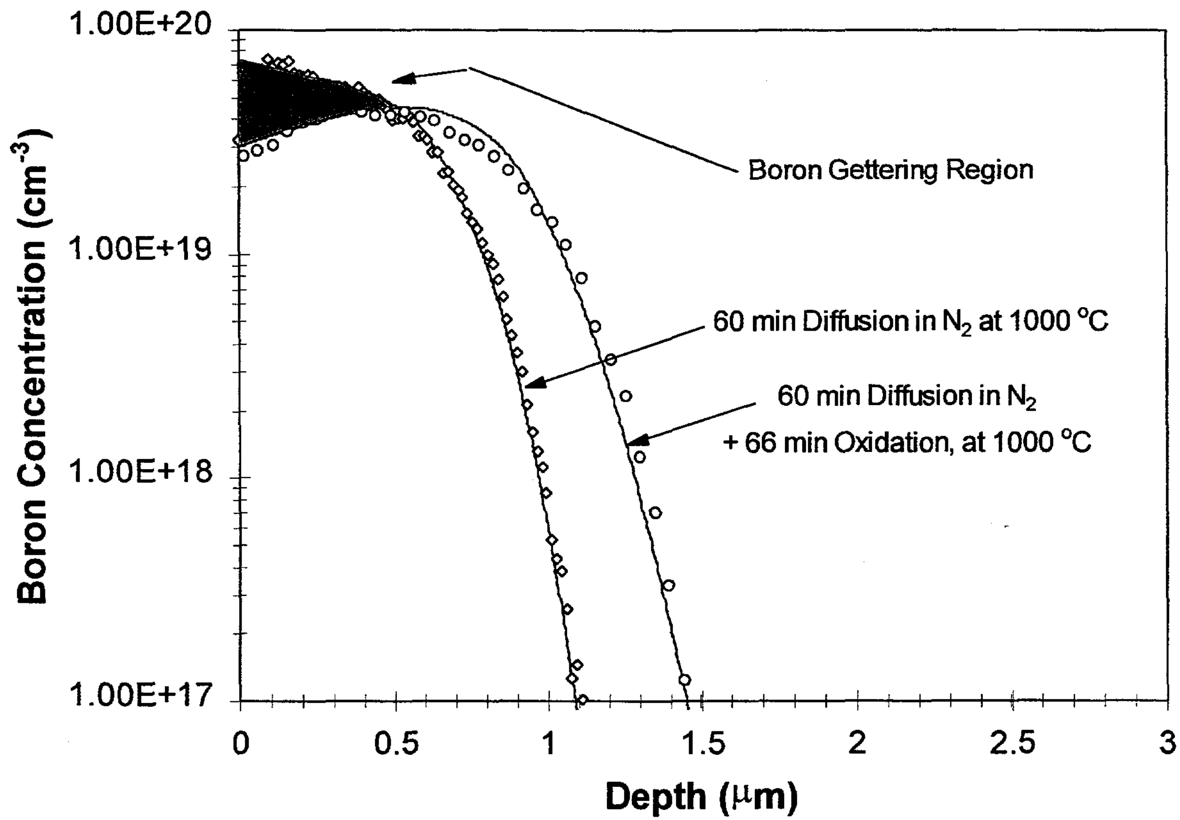
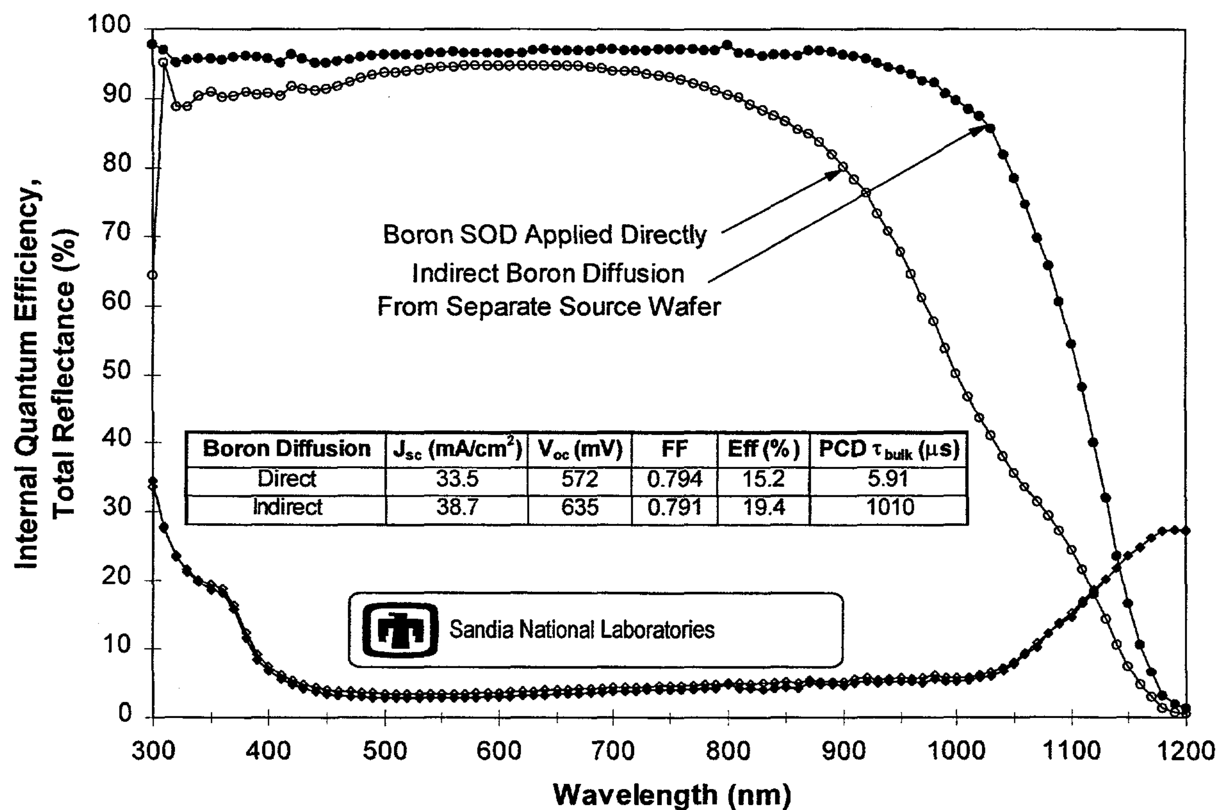


Figure 6.8. Spreading resistance measurements for boron diffusions formed in a 1000 °C/60 min process, with and without *in-situ* oxidations. The reduction in boron surface concentration for the oxidized case is believed to reduce the gettering effectiveness of the diffused region relative to the non-oxidized case.

diffusing a 100 Ω/□ phosphorus emitter, 35 Ω/□ boron BSF, and growing a thick (~1070 Å) *in-situ* thermal oxide for surface passivation and as a rudimentary anti-reflection coating. In addition to providing excellent surface passivation and anti-reflection properties, the *in-situ* oxide on the back was used as a dielectric for a $Si/SiO_2/Al$ Back Side Reflector (BSR), to improve the light trapping capabilities of the devices. This device structure, referred to as a Simultaneously diffused, Textured, *in-situ* passivating oxide **AR**-coated solar cell (**STAR** cell), has produced efficiencies as high as 20.1% [29] in a single thermal cycle, using photolithography-based metallization. Figure 6.9 shows the results for two STAR cells, in which the first had a boron SOD film directly applied to the backside, which was used as a boron source for the second cell in figure 6.9. The benefits of impurity filtering are clearly shown in figure 6.9, in that the cell which had the boron SOD directly applied has a low efficiency of only 15.2%, whereas the cell doped indirectly from the boron film on the 15.2% cell had a much higher efficiency of 19.4%. These results demonstrate the ability of this novel simultaneous boron and phosphorus diffusion technology to provide several efficiency-enhancing features, (optimal profiles, *in-situ* oxide surface passivation, *in-situ* SiO_2 AR-coating, BSR), in a single thermal cycle.



Boron Diffusion	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	Eff (%)	PCD τ_{bulk} (µs)
Direct	33.5	572	0.794	15.2	5.91
Indirect	38.7	635	0.791	19.4	1010

Figure 6.9. Internal Quantum Efficiency and Reflectance vs. Wavelength measurements for a solar cell wafer on which the boron SOD was directly applied (source wafer) and the adjacent solar cell (sample wafer) that was facing this source in the diffusion furnace. The 4.2% increase in absolute efficiency for the sample wafer is attributed to impurity filtering, resulting from the separate source/sample arrangement in the diffusion furnace.

IV Conclusion

In conclusion, we have presented a novel simultaneous boron and phosphorus diffusion technology that is well suited for the production of simple, but high efficiency silicon solar cells. In addition to providing the flexibility to simultaneously obtain a wide range of emitter and BSF profiles, this process also allows for the *in-situ* growth of a thin passivating thermal oxide. Measurements of the emitter saturation current density, J_o, have shown that the passivatingqualities of the *in-situ* oxide is excellent, producing J_o values in the 100 fA/cm^2 range for light phosphorus and boron diffusions. A physical model is presented to explain the behavior of the limited solid doping sources developed in this work. It is proposed that by fabricating solid sources out of silicon wafers using spin-on dopant films, the resulting sources deposit a *limited* dose of dopant oxide which is consumed by the intended sample. Thus for surface concentrations below the solid solubility, the surface concentration is controlled by the thickness of P_2O_5 or B_2O_3 deposited from the sources and absorbed by the sample wafers. This model was used to explain two unique attributes of this process, namely the ability to obtain an extremely thin layer of residual oxide on the diffused surface, and the dependence of sheet resistance on surface texturing, where it was shown that one could obtain $86\Omega/\square$ on a random textured surface, and $46\Omega/\square$ on a flat surface, using the same phosphorus source.

During the course of this work it was shown that by fabricating separate boron solid sources using a boron SOD film, that one could filter-out trace impurities present in the SOD film and obtain high minority carrier lifetimes in the adjacent sample wafers. Bulk minority carrier lifetimes in excess of 1 ms were obtained on boron-diffused 2.3 Ω-cm float zone wafers doped

indirectly by separate source wafers. The 2.3 Ω-cm float zone source wafers to which the boron SOD was directly applied had lifetimes as low as 5.91 ?s after a prolonged *in-situ* oxidation step. The impurity filtering action commensurate with separate boron sources was used to fabricate high-efficiency n^+pp^+ solar cells. It was shown that the cell which the boron SOD film directly applied had a low efficiency of 15.2%, while the adjacent cell doped from the same SOD film had a much higher conversion efficiency of 19.4%.

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7. Integration of Rapid Process Technologies for High Efficiency Silicon Solar Cells

7.1 Introduction

In the previous chapters we demonstrated a methodology for achieving high fill factors for screen-printed solar cells, rapid and improved formation of emitter and back surface field, and development of a novel and very effective RTO/SiN stack passivation for front and back surfaces which can also withstand screen-printed firing. In this chapter we show the integration of these rapid technologies for achieving high efficiency cells on mono-crystalline silicon.

Figure 1 shows the fabrication sequence of a baseline cell using conventional furnace processing (CFP) and photolithography contacts. In this process phosphorous diffusion, Al back surface field formation, and front oxide passivation was done in conventional furnace, resulting in about 5½ hours of high temperature processing. Metal evaporations and photolithography took another 7½ hours, resulting in a total cell processing time of about 16 hours with mono-crystalline cell efficiencies of about 18% (Fig.1) without any surface texturing.

The above process was modified by replacing furnace processing by rapid thermal processing (RTP) in which phosphorous diffusion, screen printed Al BSF formation, and oxide passivation was done in a single wafer RTP system from AG Associates. Front and back contacts were formed by evaporation and photolithography. Figure 2 shows the detailed process sequence and the corresponding cell performance. Phosphorous diffusion was performed in about 3 minutes by heating the silicon wafers, coated with appropriate

spin-on film, under the tungsten halogen lamps. Al back surface field was formed by screen printed Al on the back followed by RTP in an oxygen ambient. Besides forming a very effective and deep BSF, this step also produced a high quality rapid thermal oxide on the front simultaneously. Thus, this RTP process sequence reduces the total high temperature processing time from 5½ hours (furnace processing in Fig. 1) to less than 10 minutes (Fig. 2). In addition to reducing the total processing time from 16 hours to 8½ hours, this RTP process produced higher efficiency cells compared to conventional furnace processing. The RTP cell efficiencies of 19.1% were achieved compared to 18% for the CFP cells. This is primarily due to the superior and more uniform RTP SP Al back surface field. As shown in chapter 4, 1 μm evaporated Al BSF formed in conventional furnace, using typical slow ramp up rate, is not uniform and effective.

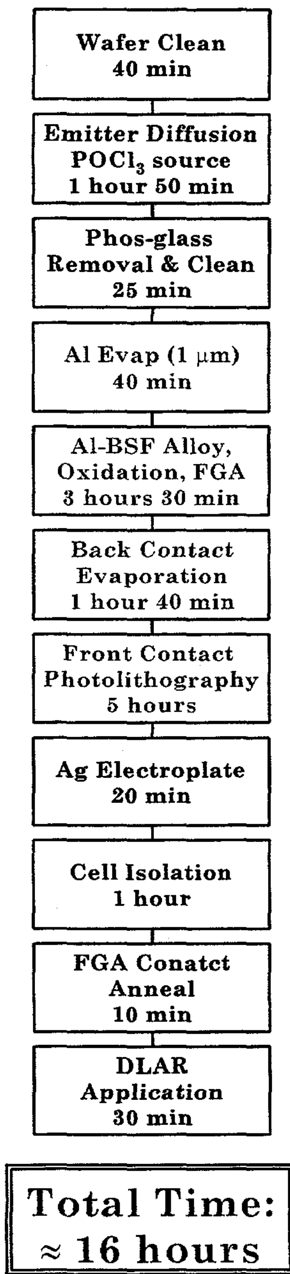
The above process was modified again by replacing evaporation and photolithography contacts by screen-printed contacts. As indicated in chapter one, we had to reduce the sheet resistance from 80 Ω/□ to 40 Ω/□ to achieve good contacts and high fill factors. Figure 3 shows the modified process sequence along with the cell performance. This RTP/SP process reduced the cell processing time from 8.5 hours to less than 2 hours and produced a cell efficiency of 17% without any texturing on mono-crystalline silicon. Notice that we were able to achieve a fill factor of 0.798 on this screen-printed cell. The 2% reduction in absolute efficiency (19% to 17%) is largely attributed to heavy doping effects in the emitter, increased shading and reflectance, and somewhat inferior front surface passivation due to higher surface doping concentration. We are investigating the formation of selective emitter (≤ 40 Ω/□ underneath the grid

and ≥ 80 Ω/□ between the grid lines) for SP cells which should be able to recover majority of the 2% loss in efficiency.

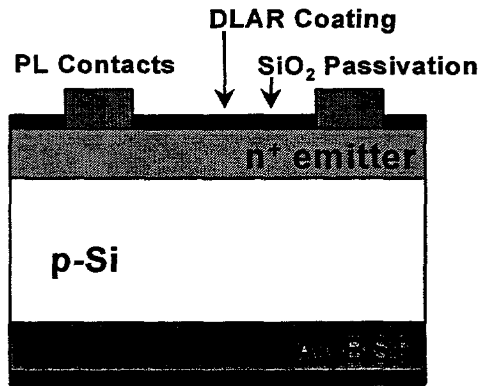
Above cells were fabricated in a single wafer RTP system. Since there is no continuous RTP system available today, we have started modifying continuous belt line processing (BLP) to bridge the gap between RTP and BLP cells. Our initial results look quite encouraging. Figure 4 shows that phosphorous diffusion in belt line furnace is slower than in RTP. This is probably because of the reduced number of high-energy photons in the BLP. A 965°C/12-min phosphorous diffusion in belt furnace gave a junction depth of 0.4 μm as opposed to 0.9 μm in the single wafer RTP system. Therefore, an attempt to keep the phosphorous diffusion time to about 6 min, we had to raise the diffusion temperature from 890°C to 925°C to achieve 45 Ω/□ emitter in BLP. We also gave up RTO for emitter passivation and decided to use direct PECVD SiN on top of the emitter for passivation as well as AR coating. Screen-printed Al BSF was formed in 2 min in the belt furnace at 860°C. Finally the SP silver contacts on the front were fired through the SiN layer. Figure 5 shows the detailed belt-line process sequence and corresponding cell efficiency on mono-crystalline silicon. Total belt line processing time was less than 2 hours, which resulted in a cell efficiency of 17% on float zone silicon. This is virtually identical to what we obtained by single wafer RTP (Fig. 3).

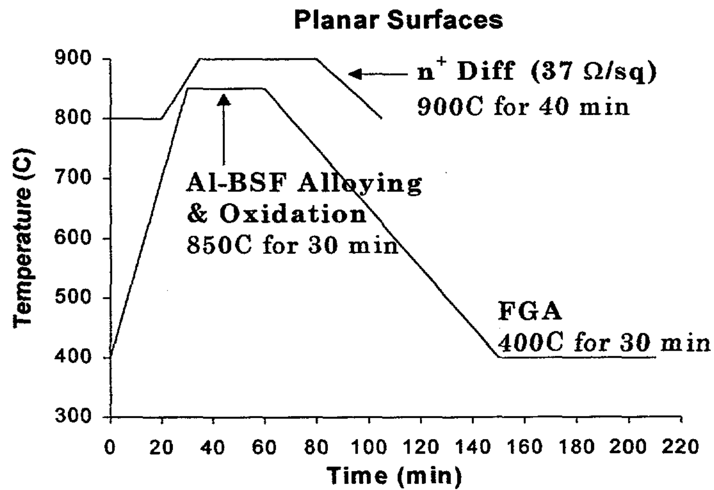
In an attempt to exploit the full potential of the stack passivation, which gives surface recombination velocity of less than 20 cm/s on bare silicon surface, we have started investigating bifacial cells. Figure 6 shows the opportunity and challenge in fabricating gridded back screen-printed cell. Gridded back screen printed cells can simplify cell processing by permitting co-firing of contacts on both sides, prevent wafer

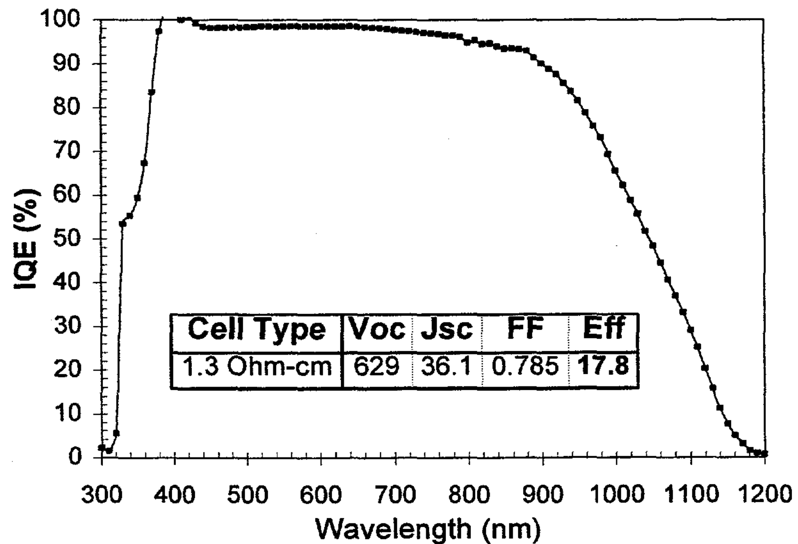
warping due to full Al BSF if thin material (≅ 100 μm) is used, offer hydrogenation of defects from both sides due to the presence of SiN, and enhance the cell efficiency due to lower BSRV. The challenge is keep the series resistance and contact recombination small. Model calculations in Fig.7 show that 100 μm thick cell with a bulk lifetime of 20 μs can produce 17% efficient screen-printed cells without surface texturing, if the back surface recombination velocity is reduced to 100 cm/s. This approach can transform 12-15% efficient industrial cells on 300 μm thick Si today to greater than 17% cells on 100-200 μm thick silicon in the future.



17.3% on FZ 2.3 Ω-cm
17.8% on FZ 1.3 Ω-cm
18.2% on FZ 0.65 Ω-cm

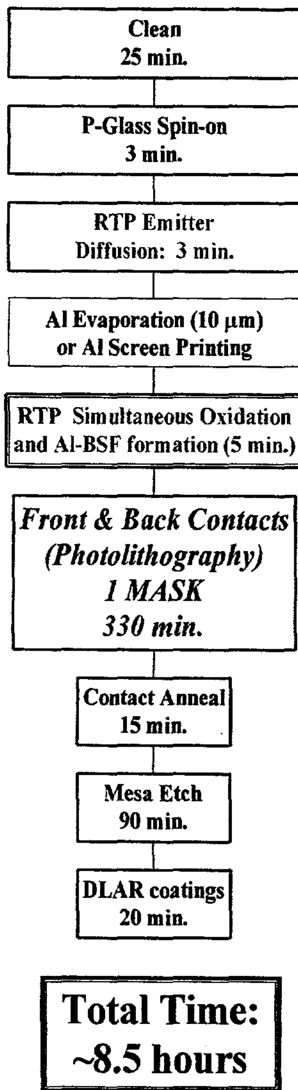


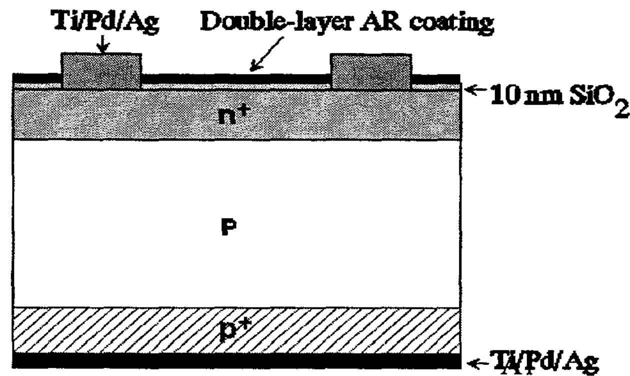


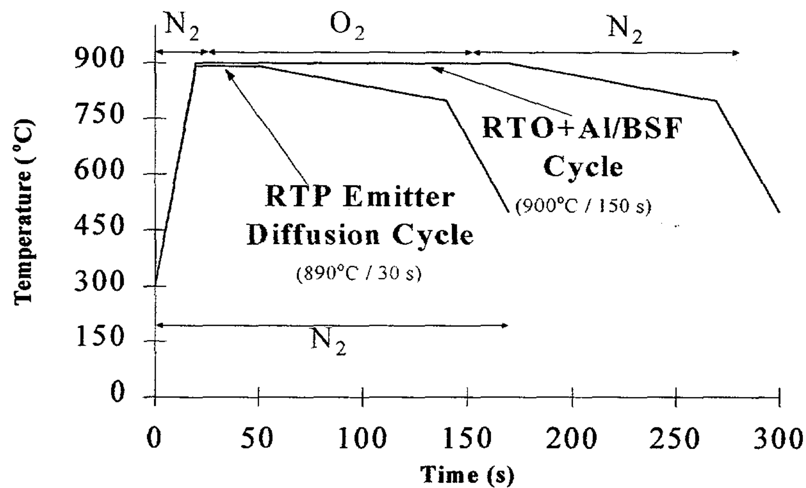


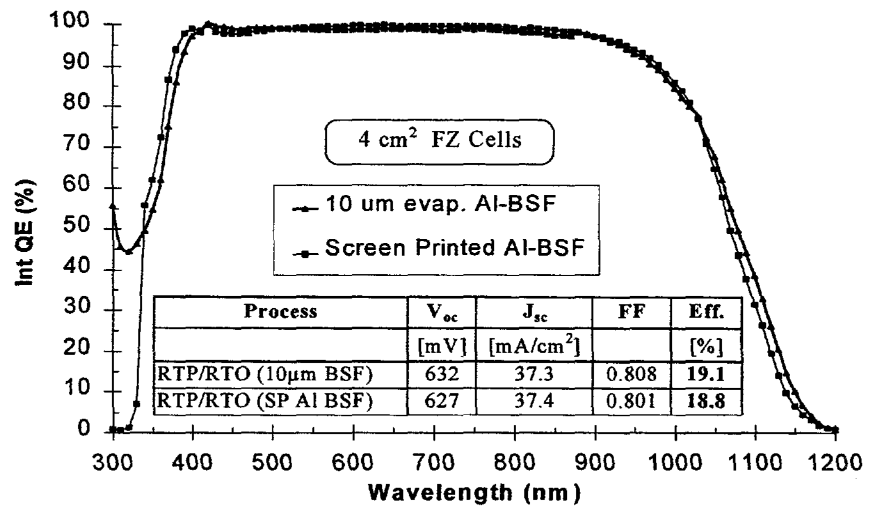
Cell Type	Voc	Jsc	FF	Eff
1.3 Ohm-cm	629	36.1	0.785	**17.8**

Figure 7.1: Baseline cell process sequence by conventional furnace processing and photolithography.



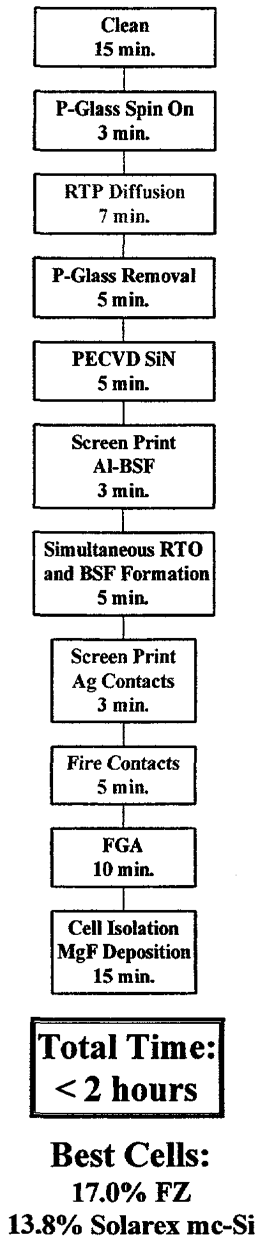


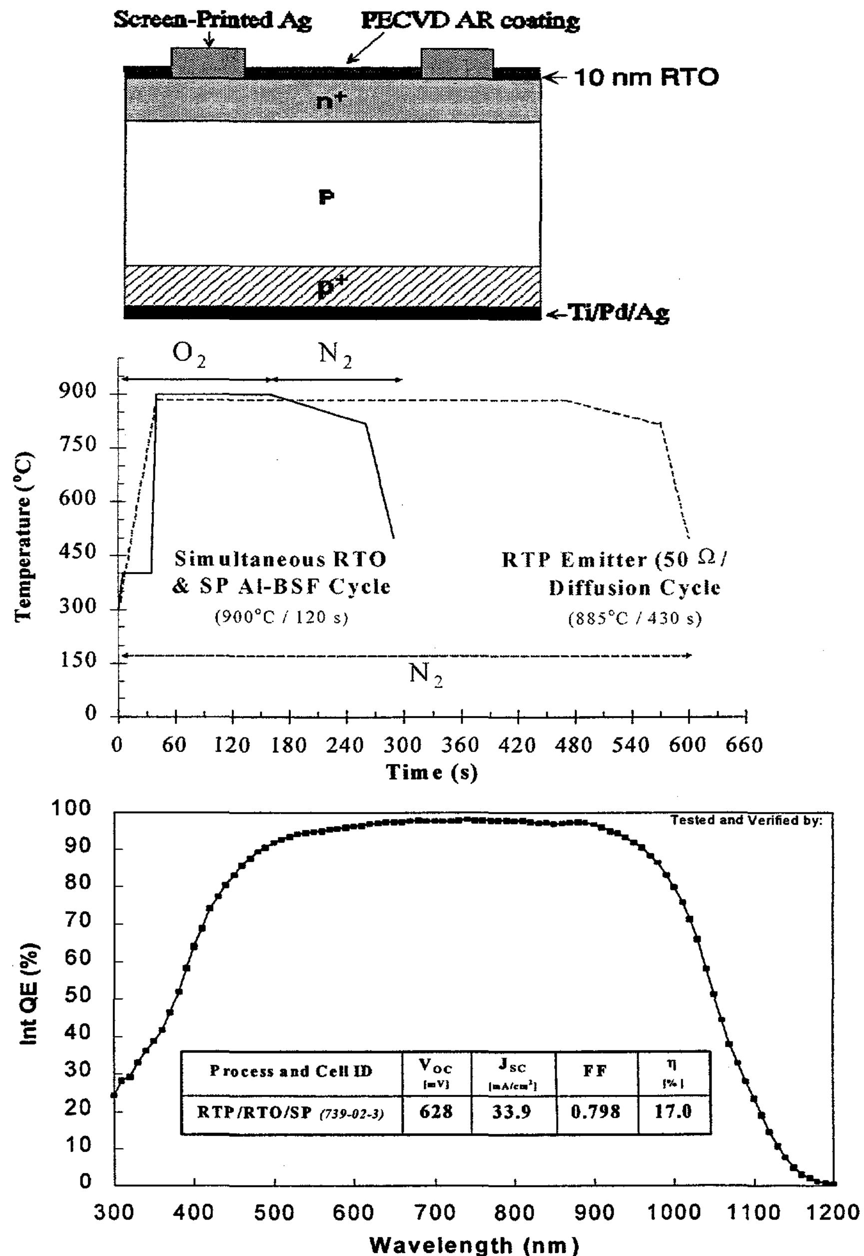




Process	V_{oc}	J_{sc}	FF	Eff.
	[mV]	[mA/cm²]		[%]
RTP/RTO (10μm BSF)	632	37.3	0.808	**19.1**
RTP/RTO (SP Al BSF)	627	37.4	0.801	**18.8**

Figure 7.2: Rapid Thermal Processing (RTP) of cells with photolithography contacts





Process and Cell ID	Voc [mV]	Jsc [mA/cm²]	FF	η [%]
RTP/RTO/SP *(739-02-3)*	628	33.9	0.798	17.0

Figure 7.3: Rapid Thermal Processing of Cells with Screen-Printed Contacts

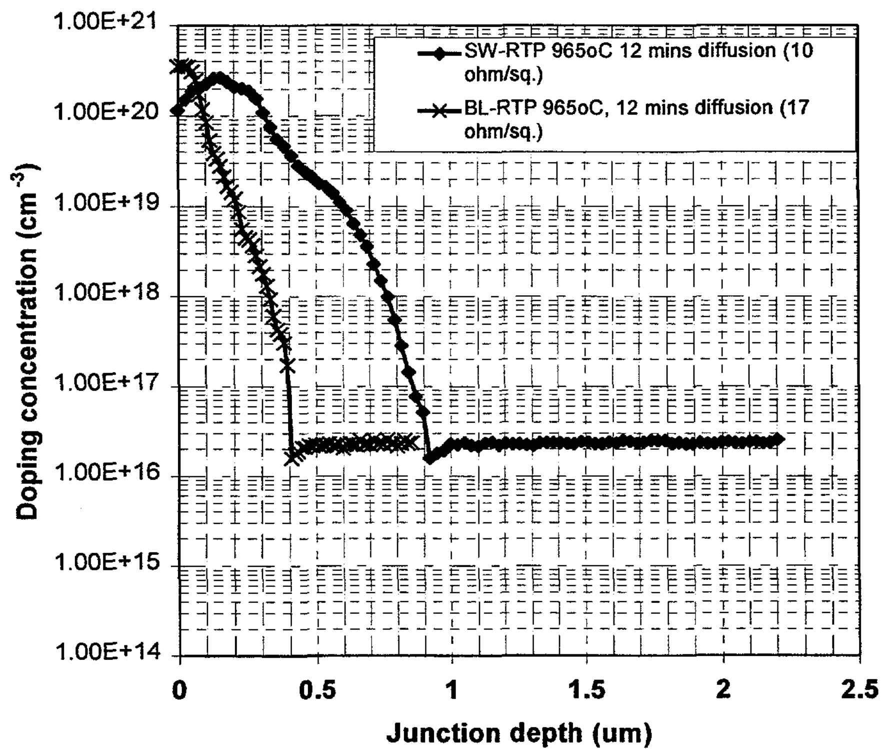
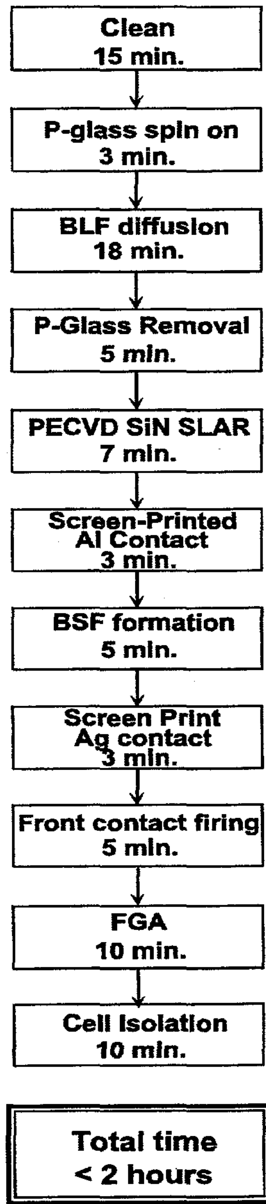
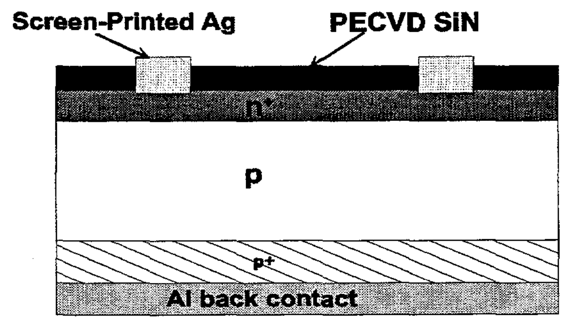
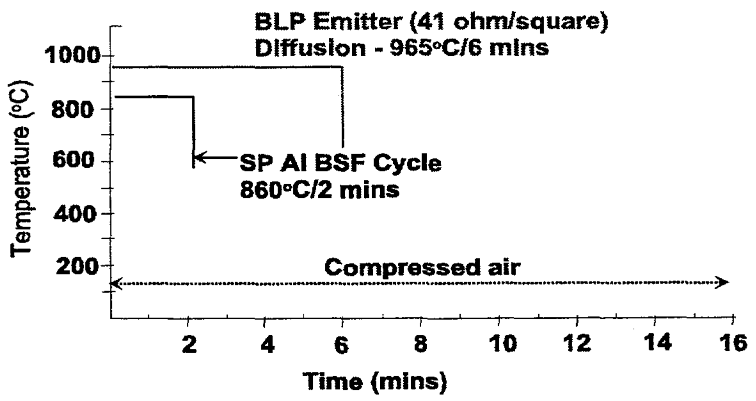


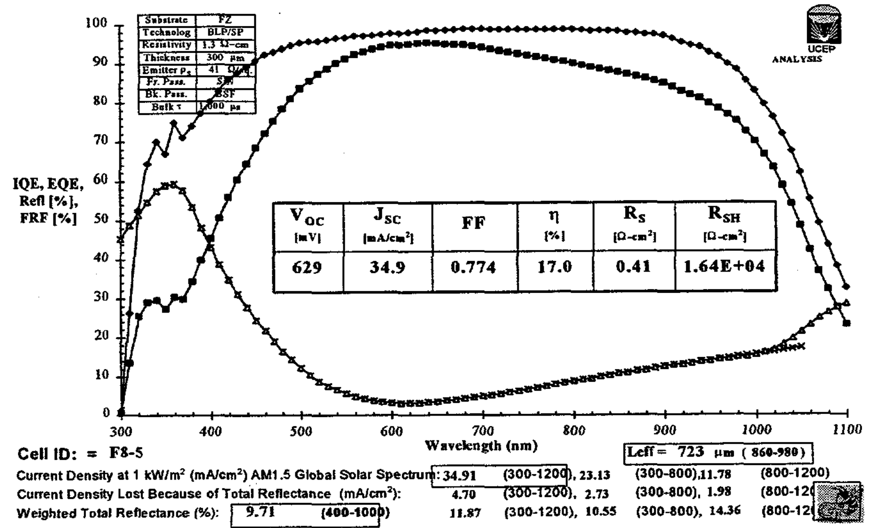
Figure 7.4: Comparison of the effective diffusivity of phosphorous in single wafer and BLP emitters at 965oC for 12 minutes.



Best Cells:
17.0% FZ

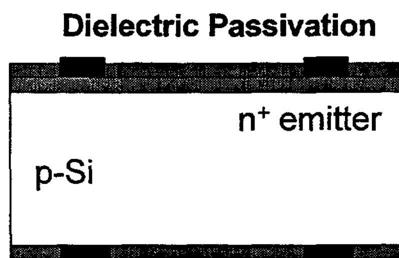


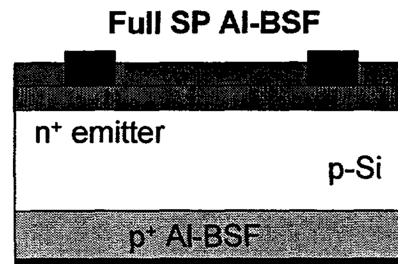




V_{OC} [mV]	J_{SC} [mA/cm²]	FF	η [%]	R_S [Ω-cm²]	R_{SH} [Ω-cm²]
629	34.9	0.774	17.0	0.41	1.64E+04

Figure 7.5: Belt line Processing of cells with screen-printed contacts





Advantages:

- No warping for thin wafers
- Lower surface recombination velocity
- Possibility of hydrogenation from the SiN on the back side
- Bifaciality

Challenges:

- Series resistance
- Contact recombination

Figure 7.6: Dielectric Passivation with Gridded Back Contacts vs Full Screen-Printed Al BSF.

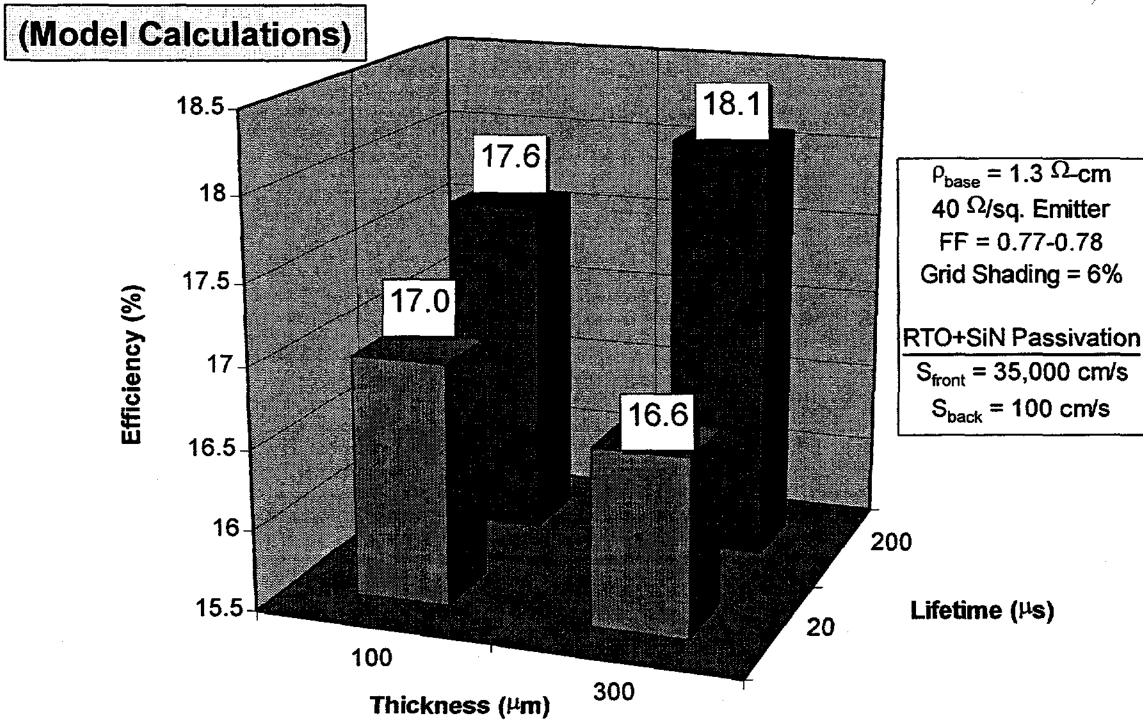


Figure 7.7: Modeling of Screen-Printed solar cells as a function of thickness and lifetime with S_{back} of 100 cm/s

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