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High-Frequency Operation of 0.3 μm GaAs JFETs for Low-Power Electronics

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GaAs Junction Field Effect Transistors (JFETs) have attracted renewed attention for low-power, low-voltage electronics. JFETs have a significant advantage over MESFETs for low-power operation due to their higher gate barrier to current flow resulting from the p/n junction gate. In this paper we report on recent advances in an all ion implanted self-aligned GaAs JFET with a gate length down to 0.3 μm. By employing shallow SiF implants next to the gate, dielectric sidewall spacers, and 50 keV source and drain implants, JFETs with a f_t up to 49 GHz with good pinchoff and sub-threshold characteristics have been realized. In addition, the JFET benefits from the use of shallow Zn or Cd implantation to form abrupt p^+/n gate profiles.

INTRODUCTION

GaAs Junction Field Effect Transistors (JFETs) have attracted renewed attention for aaplication to low-power, low-voltage electronics due to their higher gate barrier to current flow, as compared to MESFETs, resulting from the p/n junction gate. Although some JFET structures suffer a degradation in high-frequency performance due to the added gate-to-source capacitance (C_{GS}) of the junction gate and due to the gate length broadening associated with formation of the p^+-gate region, we have previously demonstrated a self-aligned GaAs JFET technology that minimizes C_{GS} and closely aligns the p^+-gate with the gate contact [1]. In our earlier work, JFETs with a 0.7 μm gate length were reported with an f_t of 26 GHz and f_{max} of 42 GHz [2].

In this work, we present results for all ion-implanted GaAs JFETs with gate lengths down to 0.3 μm. To reduce short channel effects in an all ion implanted device, the doping profiles must be significantly modified as compared to a longer gate transistor. In particular, we employed shallow SiF implants, sidewall spacers, a photolithographically defined lightly doped drain (LDD) region, and low energy Si n^+-implants. This lateral doping profile is critical to minimizing output conductance and achieving good channel pinch-off characteristics. In addition, the p^+-gate region has been made extremely shallow by using the heavy acceptor species Zn or Cd implanted at 45 keV to achieve junction depths of 70 nm and 35 nm, respectively.

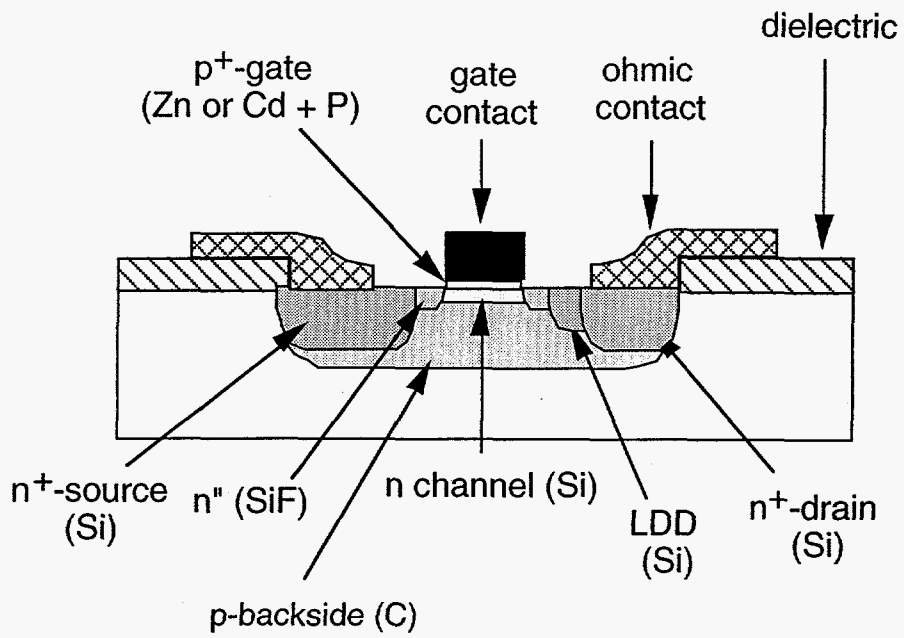

Fig 1. Schematic of self-aligned GaAs JFET showing the seven implanted regions.

JFET PROCESSING

Figure 1 shows a schematic representation of the ion-implanted, self-aligned GaAs JFET. The device requires a total of seven implantation steps which represents the most sophisticated compound semiconductor device formed by ion implantation. The implants are: 1) p^+-gate (Cd or Zn), 2) P co-implant overlaying the p^+-implant to reduce diffusion, 3) ^{29}Si for the n-channel, 4) ^{12}C for the buried p-region [3], 5) self-aligned ^{47}SiF at 40 keV for the n"-region next to the gate contact, 6) ^{29}Si in a photolithographically define lightly doped drain (LDD) region, and 7) ^{29}Si implant at 50 keV to form the source and drain regions. The gate contact is sputter deposited tungsten or a tungsten/tungsten silicide bilayer defined by electron beam lithography and patterned in a subtractive RIE-based etch. Realization of a near vertical gate profile is critical since the gate contact feature acts as a self-aligning mask for the initial n-type implants. Figure 2 shows a scanning electron microscopy image of a W/Si_x 0.3 μm length gate contact demonstrating the vertical profile [4]. After definition of the gate contact, the p^+-GaAs implanted with either Zn or Cd is removed from the source and drain regions using a citric acid based wet etch. This process results in a slightly undercut profile at the edge of the gate contact as seen on a 0.8 μm gate length device in Fig 3. At this point the n" implant is performed self-aligned to the gate contact. Next a SiN sidewall spacer is defined by a deposition and etchback process and the LDD implant is done with a photolithograpically defined LDD region. Finally, the source and drain implant is performed and all the implants are activated in one annealing step at 800 to 850 °C for 15 s. The device is completed with Ge/Au/Ni/Au ohmic contact definition and alloying.

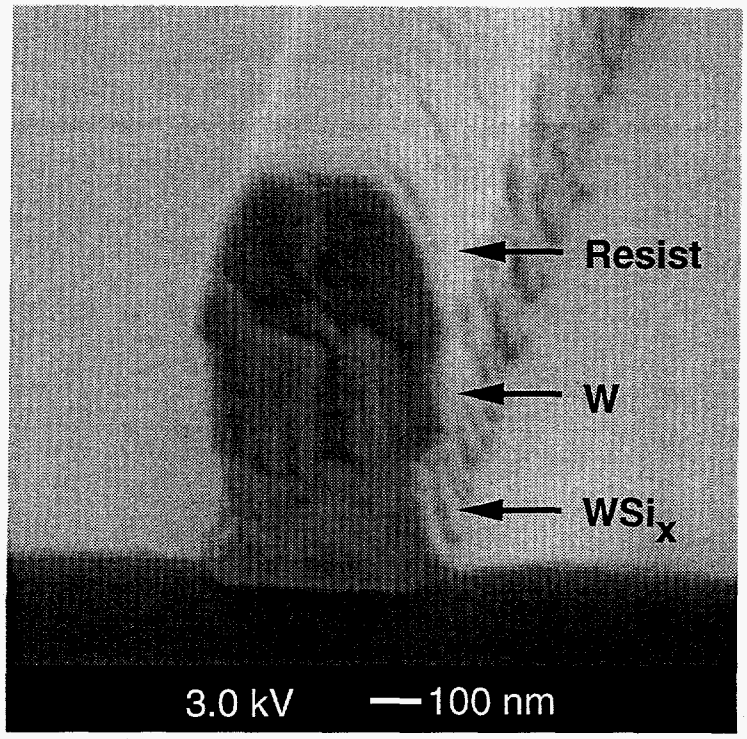

Fig 2. SEM image of 0.3 μm W/WSi$_x$ bilayer gate contact.

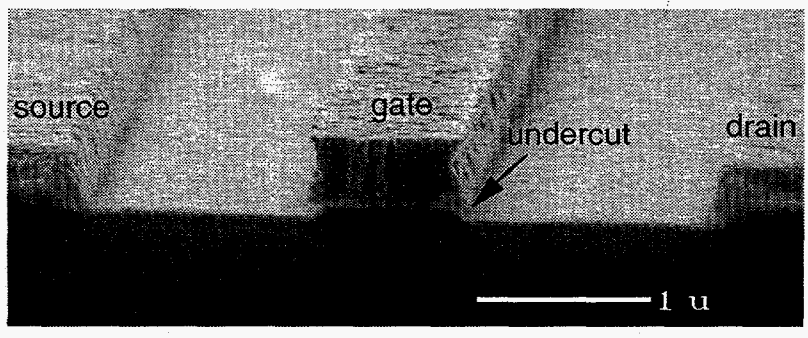

Fig 3. Scanning Electron Microscope micrograph of a 0.8 μm gate length GaAs JFET after the source and drain wet etch showing the undercut of the gate contact.

DEVICE RESULTS

Figure 4 shows the DC characteristics (I_{DS} and g_m versus V_{GS}) of an all ion-implanted 0.3 μm x 20 μm GaAs JFET with a Cd-implanted gate region. The gate diode has a forward turn on voltage of 1.0 V at 1 mA/mm of gate current, allowing the JFET to operate at low-power with a 1 V power supply. For 1 V gate bias and V_{DS} = 1.5 V the transconductance is 235 mS/mm with a saturation current of 160 mA/mm. The output conductance (g_{DS}) between V_{DS} = 1.5 to 2.5 V is 17 mS/mm and the sub-threshold slope, as seen in Fig 5, is 110 mV/decade. Both of these values are comparable to previous longer gate length implanted GaAs JFETs and are the result of the optimized doping profiles in this device.

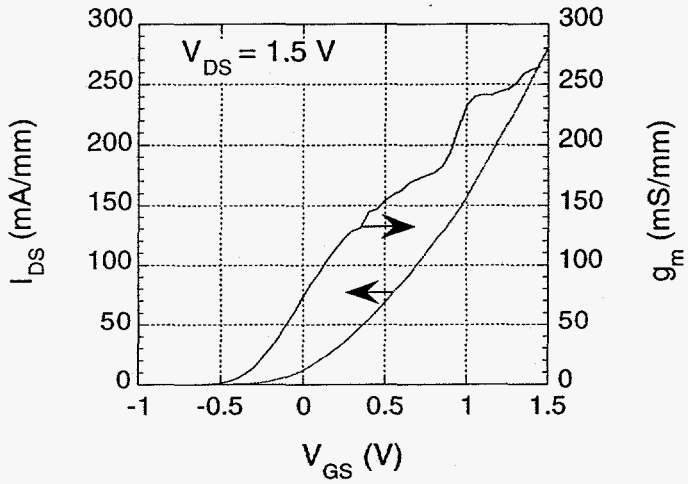

Fig 4: I_{DS} and g_m versus V_{GS} at V_{DS} = 1.5 V for a 0.3x20 μm^2 GaAs JFET.

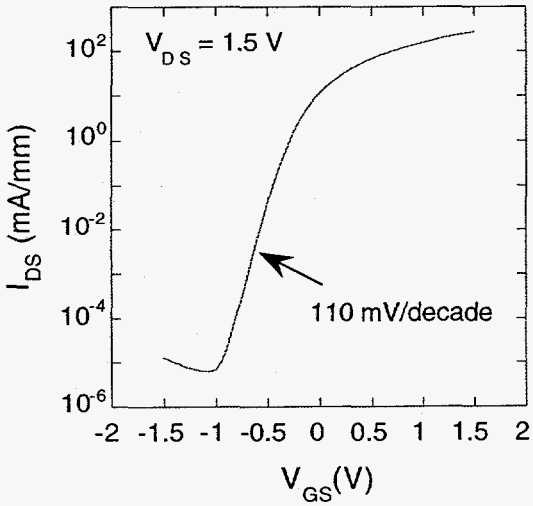

Fig 5. Plot of I_{DS} versus V_{GS} showing a sub-threshold slope of 110 mV/decade for a 0.3x20 μm^2 GaAs JFET.

Figure 6 shows the high frequency performance versus gate bias (for V_{DS} = 2.5 V) for a 0.3 μm x 40 μm JFET with a Zn-implanted gate region. When corrected for pad capacitances, we obtain an intrinsic unity current gain cut-off frequency (f_t) of 45.8 GHz and an extrinsic maximum oscillation frequency (f_{max}) of 58.6 GHz for the Zn-gate device. JFETs made with a Cd-gate implant had a slightly higher f_t of 49 GHz with an f_{max} of 56 GHz. This frequency performance is comparable to a similar gate length GaAs MESFET.

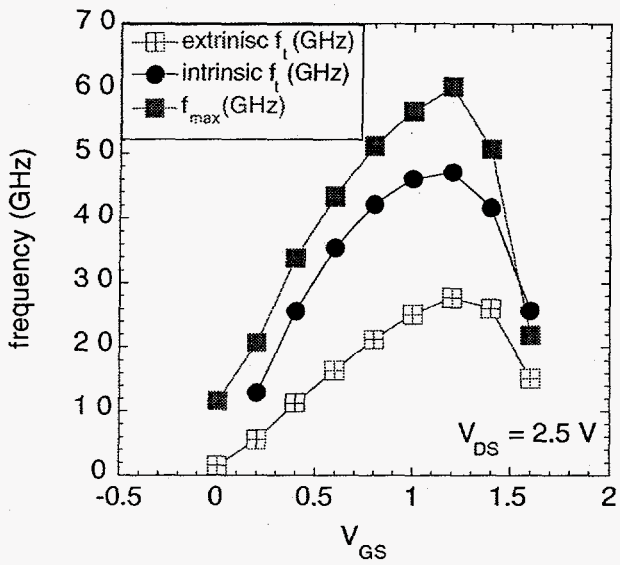

Fig 6. Frequency performance versus gate bias (V_{DS} = 2.5 V) for a 0.3x40 μm^2 Zn-gate GaAs JFET.

CONCLUSION

We have demonstrated 0.3 μm gate length all ion-implanted GaAs JFETs with V_{GS}(on) = 1 V with DC and rf performance (f_t = 49 GHz, f_{max} = 58 GHz) comparable to a similar gate length GaAs MESFET with V_{GS}(on) ~ 0.6 V. In addition, by optimizing the implant conditions, this short gate length device displays output conductance and sub-threshold performance equivalent to longer gate length implanted JFETs. Since this JFET is based solely on ion implantation it should be readily manufacturable. In addition, this device should be very attractive for low-power, low-voltage, high-frequency operation.

ACKNOWLEDGMENT

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