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ICP Etching of GaAs Via Hole Contacts

R. J. Shul, A. G. Baca, R. D. Briggs, and G. B. McClellan
Sandia National Laboratories, Albuquerque, New Mexico 87185-0603

S. J. Pearton
University of Florida, Gainesville, Florida 32611

C. Constantine
Plasma-Therm Inc., St. Petersburg, Florida 33716

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Deep etching of GaAs is a critical process step required for many device applications including the fabrication of through-substrate via holes for monolithic microwave integrated circuits (MMICs). The use of high-density plasmas, including inductively coupled plasmas (ICP), offers an alternative approach to etching vias as compared to the more conventional parallel plate reactive ion etch (RIE) systems. In this paper, we report ICP etching of GaAs vias at etch rates of approximately 5.3 µm/min with via profiles ranging from highly anisotropic to conical.

INTRODUCTION

Via hole contacts are essential to many GaAs electronic and photonic device applications. Monolithic microwave integrated circuits (MMICs) require backside via holes for low inductance grounding and increased circuit complexity. Interest in through-substrate via holes has also increased for photonic devices and packaging applications. It is often necessary to etch deep GaAs features to fabricate photonic devices designed to emit through the substrate since GaAs often absorbs at the wavelength of operation. Smooth, anisotropic GaAs via holes may also have potential use in photonic packaging where optical fibers can be inserted into a via hole for self-alignment to photonic devices.

GaAs via holes are typically etched in chlorine based reactive ion etch (RIE) plasmas at rates ≥1 µm/min.[1-7] The patterned via holes are normally 100 µm in diameter on wafers thinned to approximately 100 µm. The etched via profiles are generally easy to metallize (conical profiles), however the sidewalls and bottoms can be rough, decreasing long-term reliability and yield. Furthermore, as via diameters are decreased to increase circuit complexity, etch rates decrease due to poor transport of reactants and etch products into and out of the via.[4] Pearton *et al.* have used high density plasma electron cyclotron resonance (ECR) etching to etch small diameter (≤30 µm) GaAs via holes.[7] Due to enhanced plasma density and low process pressures (≤20 mTorr), etch rates remained relatively high (0.5 to 1.5 µm/min) despite transport issues associated with high aspect ratio features. Inductively coupled plasma (ICP) etching, which is also expected to yield high etch rates at low process pressures, offers an attractive alternative high-density dry etching technique. It may also be easier to scale-up than ECR sources and more economical to operate in terms of cost and power requirements.

ICP plasmas are formed in a dielectric vessel encircled by an inductive coil into which rf-power is applied. A strong magnetic field is induced in the center of the chamber which generates a high-density plasma due to the circular region of the electric field that exists concentric to the coil. At low pressures (≤10 mTorr), the plasma diffuses from the

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generation region and drifts to the substrate at relatively low ion energy. Etch profiles may be contoured by superimposing a rf-bias on the sample to independently control ion energy. We report ICP etch results for GaAs vias as a function of pressure, plasma chemistry, rf-power, and ICP power.

EXPERIMENTAL

Semi-insulating GaAs wafers were used to determine etch rates for 150 μm diameter vias patterned with Shipley STR-1110 photoresist. A single application of STR-1110 resist was used to obtain an approximate 12 μm resist thickness. Vias were patterned using a Karl Suss MJB-3 contact aligner. An oxygen plasma was used to descum the samples prior to GaAs etching to remove any excess resist in the via hole. Prior to exposure to the plasma, the samples were placed on a hotplate for 5 minutes at 150°C to create a sloped resist profile. Plated Ni masks and AZ-4903 photoresist masks were used for deep via etching (>50 μm). The patterned via diameters ranged from 20 to 70 μm. The Ni mask was approximately 2 μm thick. A sacrificial polyimide release layer was used to strip the Ni mask in hot (90°C) n-methyl-2-pyrrolidinone (NMP) after etching. The AZ-4903 was approximately 24 μm thick and was exposed to a series of hotplate bakes at 90, 120, and 180°C fro 7 minutes each to obtain a sloped resist profile.

The ICP reactor used in this study was a load-locked Plasma-Therm SLR 770 etch system with a Plasma-Therm 2 MHz ICP source. Ion bombardment energies were modified by superimposing a rf-bias (13.56 MHz) on the sample. Samples were mounted with a low vapor pressure thermal paste on an anodized Al carrier that was clamped to the cathode and cooled with He gas. Etch gases were introduced through an annular region at the top of the chamber. Unless otherwise mentioned the ICP etch parameters used in this study were: 8 sccm Cl_2, 32 sccm BCl_3, 10°C electrode temperature, 5 mTorr total pressure, 750 W of ICP power, and 150 W rf-power with a corresponding dc-bias of -350 ± 25 V.

GaAs etch rates were calculated from the depth of the etched feature measured with a Dektak stylus profilometer following removal of the masking material. The etch rates represent maximum values for the given set of plasma conditions since they were calculated for 5 minute exposures to the plasma and therefore were not affected by transport issues. Each sample was approximately 1 cm^2 and depth measurements were taken at a minimum of three positions. Error bars for the etch rates represent the greater of either the standard deviation across the sample or the standard deviation from run-to-run. Selectivites were reported as GaAs etch rate/resist etch rate. The resist etch rate was calculated from the depth of the resist measured with the profilometer before and after exposure to the plasma. Via hole profile, surface, and sidewall morphology were evaluated with a scanning electron microscope (SEM).

RESULTS AND DISCUSSION

GaAs via etch rates and selectivities to STR-1110 photoresist are shown in Figure 1 as a function of pressure . During these runs the rf-power was held constant at 150 W which resulted in an increase in dc-bias (-250 to -465 V) as the pressure was increased (1 to 20 mTorr). Higher dc-biases were attributed to increased collisional recombination which decreased the plasma density at higher pressures. The etch rate increased monotonically as the pressure was increased from 1 to 20 mTorr suggesting a reactant limited regime. As observed in ECR etching of GaAs vias [7,8], the GaAs etch rates

increased as the available concentration of reactive chlorine increased and the sputter desorption (dc-bias) increased at high pressures. At 50 mTorr, the GaAs etch rate decreased by more than 50% while the dc-bias decreased to approximately -360 V. The decrease in etch rate may have been due to less efficient sputter desorption or redeposition on the etch surface. The decrease in dc-bias at 50 mTorr may have been due to less efficient coupling of the ICP power at high pressure. Under these high pressure conditions, the ICP plasma may have been operating under RIE-like conditions where the collisional frequency increased and the ion energies decreased at 50 mTorr. The GaAs to STR-1110 selectivity increased to approximately 11 at 50 mTorr possibly due to the lower dc-bias.

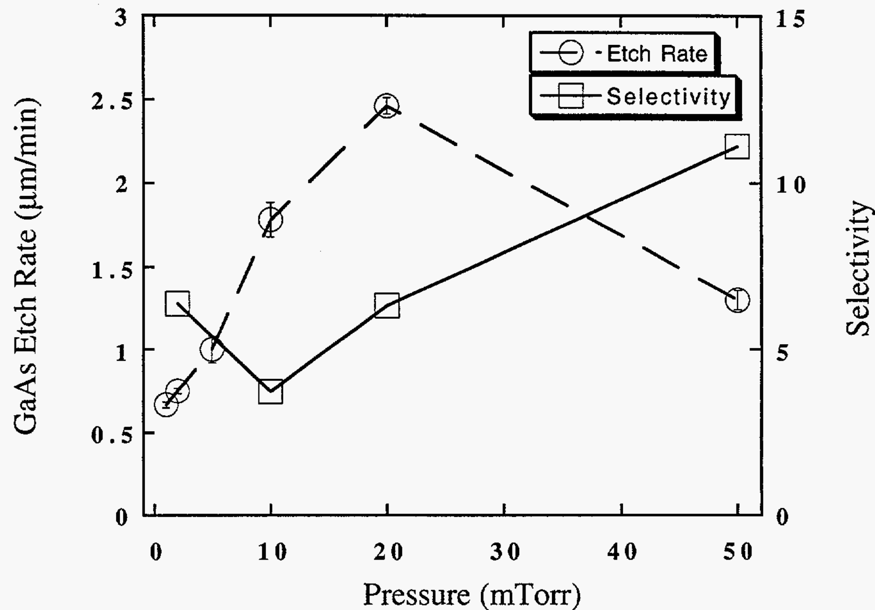

Figure 1: GaAs via etch rates and selectivity of GaAs to STR-1110 photoresist as a function of pressure.

In Figure 2, GaAs etch rates and selectivities to resist are plotted as a function of percent Cl_2 flow in a Cl_2/BCl_3 plasma. The etch rate increased monotonically up to 80% Cl_2, however decreased in a pure Cl_2 plasma. This trend showed the chemical nature of the etch, which increased as the concentration of reactive Cl increased. Lower etch rates observed in pure Cl_2 may be attributed to less efficient sputter desorption as well as a longer incubation period required to sputter through the surface oxide in the absence of BCl_3. The selectivity remained relatively constant (3.5 to 5) with a slight increase as the Cl concentration increased.

The GaAs etch rate and selectivity to resist are plotted as a function of rf-power in Figure 3. The etch rate increased by approximately a factor of 3 as the rf-power was increased from 1 to 350 W possibly due to improved sputter desorption of the etch products from the surface. The etch rate showed a decrease at 150 W. Selectivities remained relatively constant independent of rf-power. The GaAs etch rate data was somewhat scattered as a function of ICP power as shown in Figure 4. Following an initial

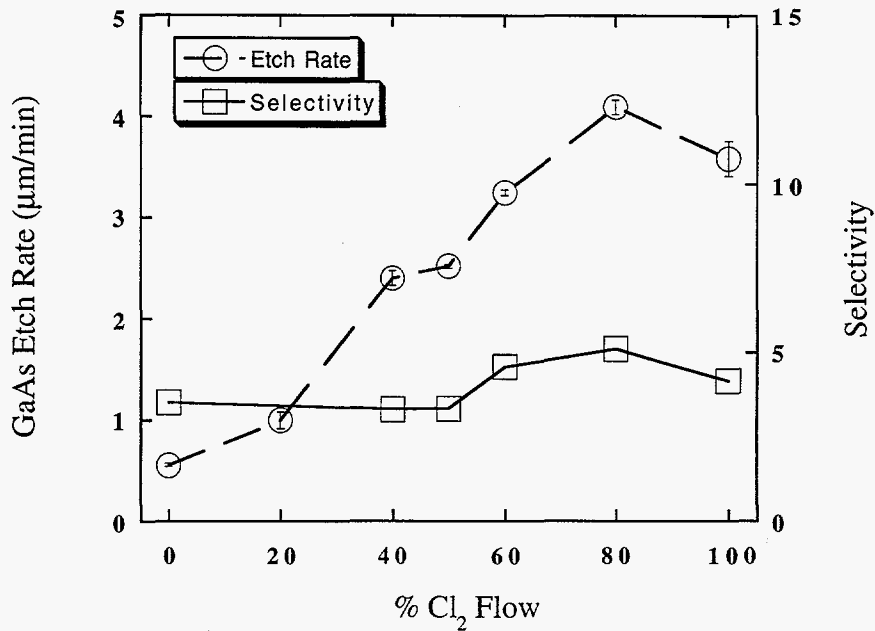

Figure 2: GaAs via etch rates and selectivity of GaAs to STR-1110 photoresist as a function of %Cl_2 in a Cl_2/BCl_3 plasma.

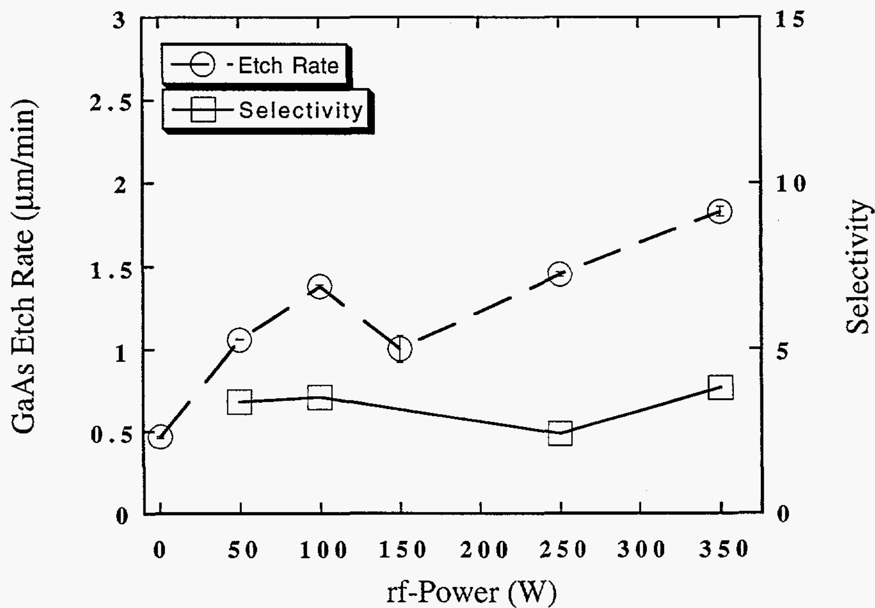

Figure 3: GaAs via etch rates and selectivity of GaAs to STR-1110 photoresist as a function of rf-power.

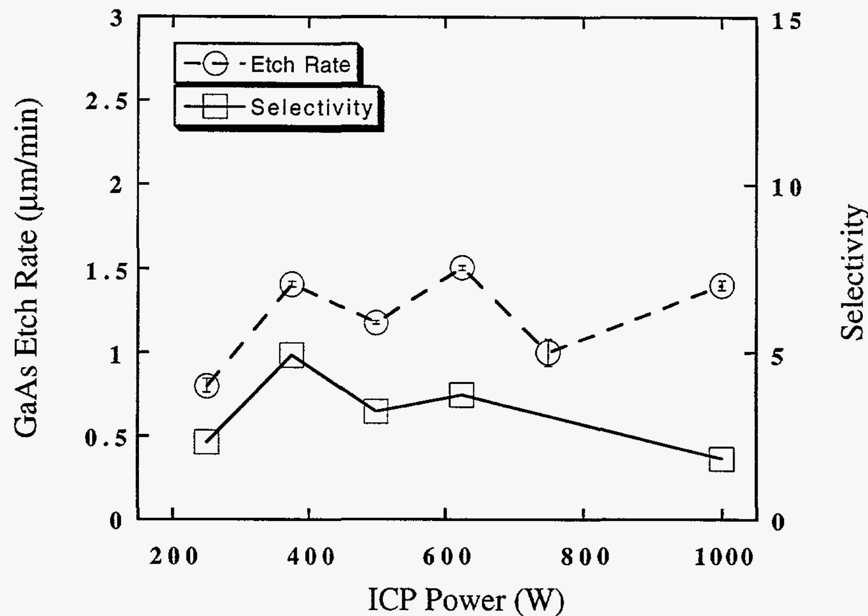

Figure 4: GaAs via etch rates and selectivity of GaAs to STR-1110 photoresist as a function of ICP power.

increase in etch rate with ICP power (plasma density), the etch rates remained relatively constant at 375, 625, and 1000 W ICP power and were lower at 500 and 750 W. The selectivity ranged from approximately 2 to 5.

By flowing the STR-1110 resist to create a sloped profile, we observed highly conical etched GaAs via profiles under most etch conditions with no sign of a lip at the top edge of the via or concave wall profiles. The sidewall roughness did vary as a function of plasma conditions, however trends were not obvious and the roughness was minimal. Figure 5 shows a SEM micrograph of a via etched at 5 mTorr pressure, 750 W ICP power, 350 W rf-power, 8 sccm Cl_2, and 32 sccm BCl_3 with the resist removed. The patterned via was 150 µm in diameter. The via was etched to an approximate depth of 9 µm at a rate of 1.8 µm/min. The via profile was conical with very smooth sidewalls and surfaces; however, the selectivity was 3.8 and therefore required more than 25 µm of resist to etch a 100 µm deep GaAs via.

In Figure 6, SEM micrographs are shown for 70 µm diameter vias patterned with AZ-4903. The via shown in Figure 6a, was approximately 50 µm deep (GaAs etch rate was approximately 1.67 µm/min), conical, and showed a roughened texture on the sidewalls. The etch conditions were 10 mTorr pressure, 750 W ICP power, 150 W rf-power, 8 sccm Cl_2, and 32 sccm BCl_3. The resist was left in place to show the sloped profile used to obtain conical etched GaAs via profiles. For the via shown in Figure 6b, the plasma conditions were changed to increase the etch rate and were; 10 mTorr pressure, 750 W ICP power, 250 W rf-power, 32 sccm Cl_2, and 8 sccm BCl_3. The etch rate increased to approximately 5.33 µm/min for an 80 µm deep via. The via profile was conical and had very smooth sidewalls. The higher etch rate was probably due to higher %Cl_2 flow which resulted in a higher concentration of reactive Cl and higher rf-power

which resulted in improved sputter desorption. Despite the more aggressive etch conditions, the GaAs to AZ-4903 selectivity remained approximately 5. These processes yield via profiles which are applicable to backside metallization for MMIC applications.

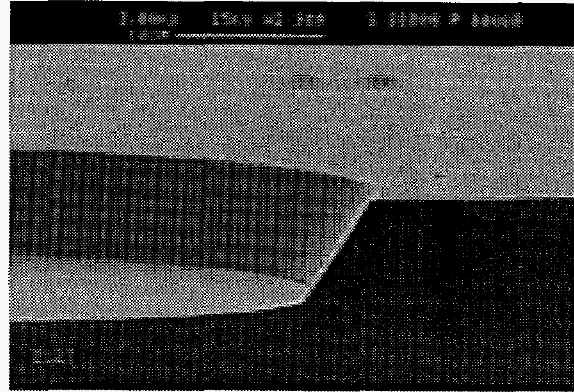

Figure 5: SEM micrograph of a 150 μm via etched at 5 mTorr pressure, 750 W ICP power, 350 W rf-power, 8 sccm Cl_2, and 32 sccm BCl_3 with the STR-1110 resist removed. The etch rate was approximately 1.8 μm/min (9 μm deep).

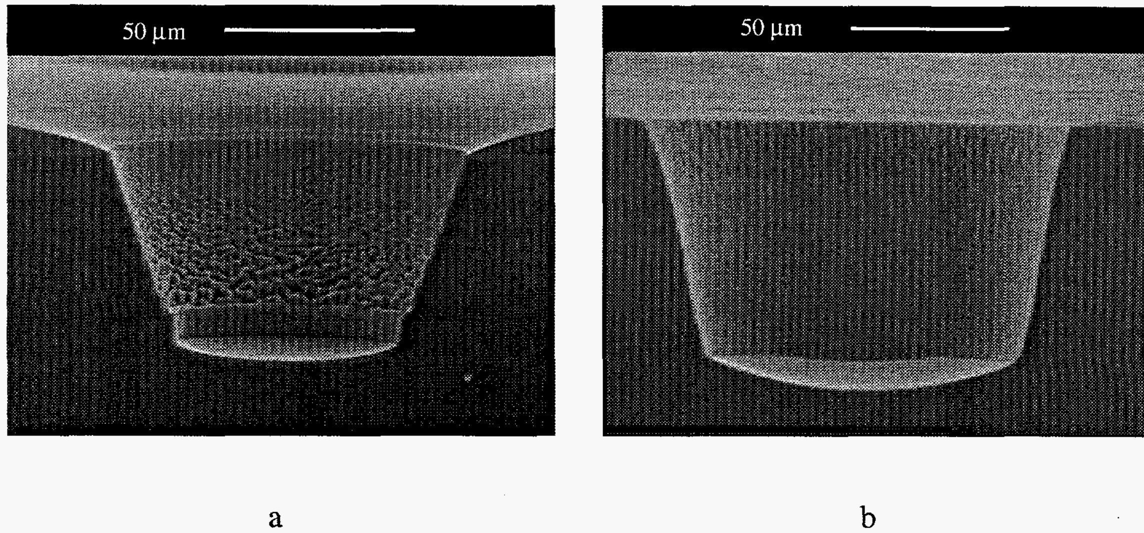

Figure 6: SEM micrographs of 70 μm wide vias etched at (a) 10 mTorr pressure, 750 W ICP power, 150 W rf-power, 8 sccm Cl_2, 32 sccm BCl_3 and (b) 10 mTorr pressure, 750 W ICP power, 250 W rf-power, 32 sccm Cl_2, and 8 sccm BCl_3.

Using a Ni mask, we obtained highly anisotropic GaAs vias which were very smooth, as shown in Figure 7. The etch conditions were identical to those used for the via shown in Figure 6a. The etched via was 105 μm deep (GaAs etch rate was approximately 3.50 μm/min), highly anisotropic, and smooth. The patterned via was 60 μm in diameter which accounted for the lower etch rate than that obtained for the via displayed in Figure 6b. We also observed the effect of "RIE lag" as shown in Figure 8. The etch depth was approximately 12 μm less for the 20 μm diameter via as compared to the 60 μm diameter via. As the patterned via diameters were decreased, the etch rates decreased due to

transport effects in high aspect ratio features. Highly anisotropic vias can be used for photonic devices, packaging applications, and GaAs micromachining applications.

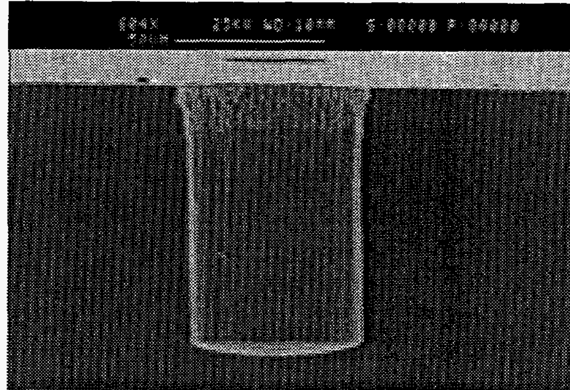

Figure 7: SEM micrograph of GaAs via etched with a Ni mask at) 10 mTorr pressure, 750 W ICP power, 250 W rf-power, 32 sccm Cl_2, 8 sccm BCl_3

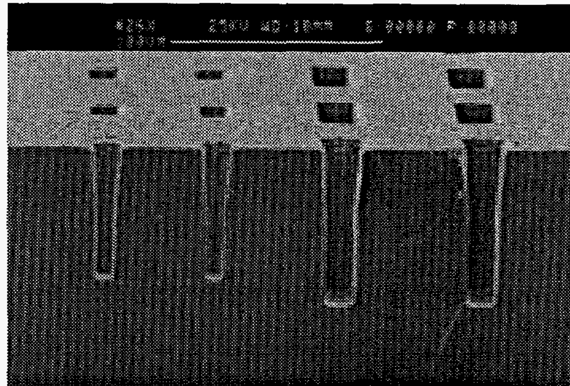

Figure 8: SEM micrograph of 20 and 60 μm vias patterned with a Ni mask showing the effect of RIE lag.

CONCLUSIONS

High rate etching for GaAs through substrate via holes are reported in an ICP etch system. Etch rates of approximately 5.3 μm/min were observed for patterned vias 70 μm in diameter for depths up to 80 μm. Conical via profiles, well suited for backside metallization, were obtained using a sloped photoresist profile. The selectivity of the GaAs to photoresist remained relatively low (≤5) requiring a resist thickness >20 μm for standard MMIC applications (100 μm deep vias). The via profile tended to widen at the top due to the flowed resist profile thus limiting the density of features and circuit complexity. With the application of a Ni mask, the vias were much more anisotropic and showed virtually no widening, thereby increasing circuit complexity. The anisotropic profiles however were more difficult to metallize. RIE lag was an issue for ICP etching. ICP appears to be a worthy technique to fabricate small diameter, deep GaAs features at high etch rates.

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