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E. M. Chow, H. T. Soh, A. Partridge, J. A. Harley,
T. W. Kenny, C. F. Quate, S. Abdollahi-Alibeik,
J. P. McVittie, A. McCarthy

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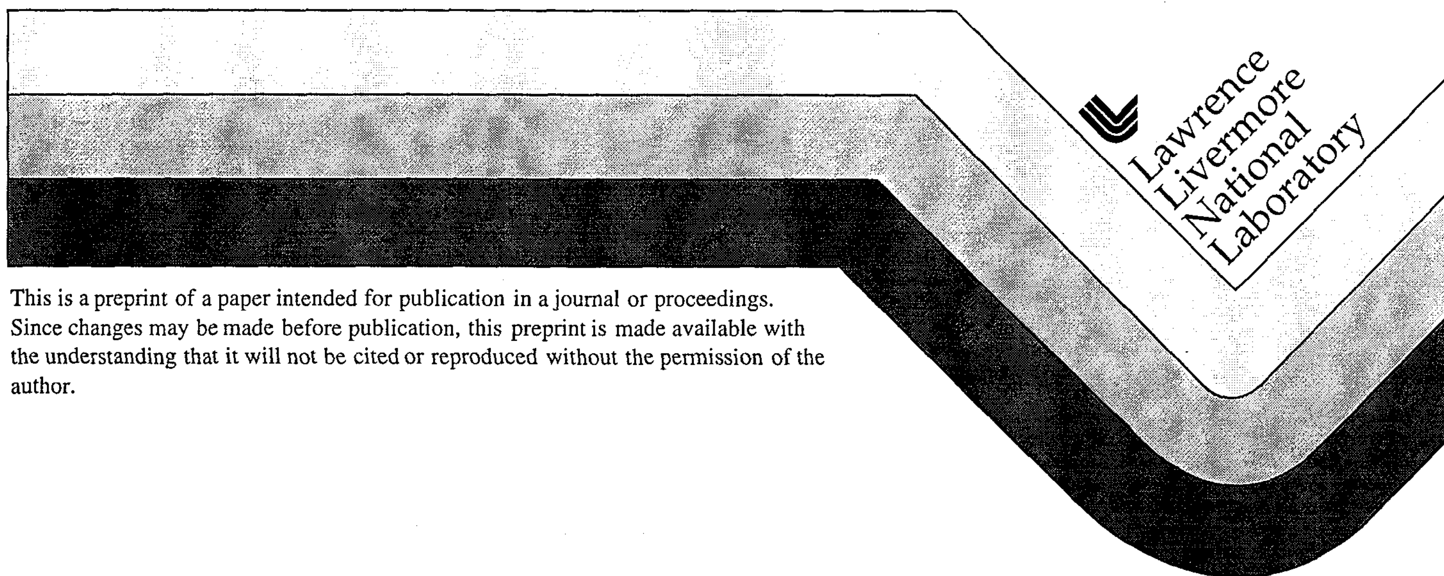

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FABRICATION OF HIGH-DENSITY CANTILEVER ARRAYS AND THROUGH-WAFER INTERCONNECTS

Eugene M. Chow, Hyongsok T. Soh, Aaron Partridge, Jonah A. Harley, Thomas W. Kenny, and Calvin F. Quate
E. L. Ginzton Laboratory, Stanford University
Stanford, CA 94305-4085

Shahram Abdollahi-Alibeik and James P. McVittie
Center for Integrated Systems, Stanford University
Stanford, CA 94305

Anthony McCarthy
Lawrence Livermore National Laboratory
Livermore, CA 94551

ABSTRACT

Processes to fabricate dense, dry released microstructures with electrical connections on the opposite side of the wafer are described. A 10 × 10 array of silicon and polysilicon cantilevers with high packing density (5 tips/mm^2) and high uniformity (<10 μm length variation across the wafer) are demonstrated. The cantilever release process uses a deep SF_6/C_4F_8 plasma etch followed by a HBr plasma etch to accurately release cantilevers. A process for fabricating electrical contacts through the backside of the wafer is also described. Electrodeposited resist, conformal CVD metal deposition, and deep SF_6/C_4F_8 plasma etching are used to make 30 μm/side square vias each of which has a resistance of 50 mΩ.

INTRODUCTION

Since the invention of the atomic force microscope [1], micromachined cantilevers have found applications in surface science [2], lithography [3,4], data storage [5], and biological sensors [6,7]. While scanning probe devices have proven their importance in many areas of science and engineering, they suffer from slow speeds and long scan times, because the scanning probe is inherently a serial device. Parallel operation of an array of scanning probes will address this problem as system bandwidth, scan area, and reliability (through redundancy) are increased.

Specific requirements for an array of scanning probe devices vary with application, but generally include: 1) fabrication of cantilevers with high yield and density and, 2) a method of addressing each cantilever electrically for sensing and/or actuation. Also, if circuitry is to be integrated on the same chip, the fabrication process must conform to standard CMOS processing techniques.

High densities and yields, however, are not easily achievable with conventional processing. Cantilevers are typically released by etching through the entire wafer from the backside. Because etch profiles are restricted to crystallographic planes, potential cantilever density is severely limited, as demonstrated in Fig. 1. Also, process yields are often low because of front side protection. Protecting a front-side metal layer, which is necessary for a one-sided etch in liquid, is difficult for the long durations and elevated temperatures needed for etchants such as TMAH and KOH. Stiction, especially for thin and long cantilevers, is another source of yield reduction for wet processes.

The requirement for electrical connections is particularly challenging for two-dimensional arrays. Interconnects for each cantilever are needed when piezoresistive or piezoelectric effects are utilized. Addressing all of these elements is complicated by the need to keep bonding wires out of the scanning region, which could be only a few microns above the sample. Hence, it is important to be able to place the array element on the front side of the wafer, while electrically connecting them to the bond pads on the backside of the wafer. Such through-wafer contacts have been demonstrated with wet etching, but this exacerbates the density problem depicted in Fig. 1 [8].

Figure 1. Drawing of a wet released cantilever and its through wafer electrical contacts (with four leads.) For a 100 μm × 500 μm release region with one cantilever per release region, using a 500 μm thick wafer, tip densities are limited to < 0.3 tips/mm^2.

To address these issues, we have developed high-yield fabrication processes to release dense cantilever arrays, and create small, through-wafer interconnects. A key advance is to replace wet etches with deep, anisotropic etching with high density low pressure (HDLP) plasmas [9]. Cantilever densities more than an order of magnitude greater than that possible with wet etching are achieved, implying that significantly shorter scan times (Fig. 2) are now possible.

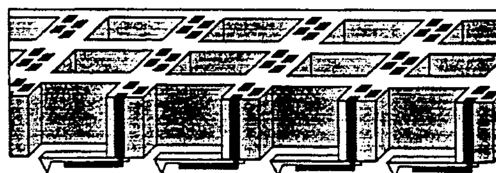

Figure 2. Cross section drawing of anisotropic released cantilevers with through wafer electrical contacts. For a 100 μm × 500 μm release region with one cantilever per release region, and using a 500 μm thick wafer, tip densities of >20 tips/mm^2 are achievable.

The cantilever release process uses a two part etch, a deep SF_6/C_4F_8 plasma etch followed by a well controlled HBr plasma etch. The process is uniform and capable of releasing thin cantilevers which are CMOS compatible and applicable to other structures. Dense arrays of cantilevers (5 tips/mm^2) with high yields and uniform mechanical properties (< 10 μm length variation) across the wafer are demonstrated.

Through-wafer vias (TWV) which are 30 μm/side and with a resistance of 50 mΩ/via have also been fabricated. This resistance is significantly less than that of typical piezoresistor sensors used in cantilevers (~1 kΩ.) In addition to benefiting cantilever technology, this process can be applied to circuits (i.e., ground connections in mixed signal circuits), packaging (i.e., multi-chip stacking) and MEMS (i.e., 3D structures.) Critical steps include HDLP etching, conformal metallization by CVD, and patterning of high-aspect ratio holes using electrodeposited resists.

CANTILEVER ARRAYS

The cantilever dry release process, summarized in Fig. 3, starts with a 4" silicon-on-insulator (SOI) wafer or a layer of polysilicon on silicon dioxide. First the cantilevers are patterned into the device layer. At this time piezoresistive sensors and/or on-chip CMOS circuitry can be integrated. For the process demonstrated, simple optical detection cantilevers (200-400 μm long, 5-50 μm wide and 1-3 μm thick) without integrated sensors were fabricated.

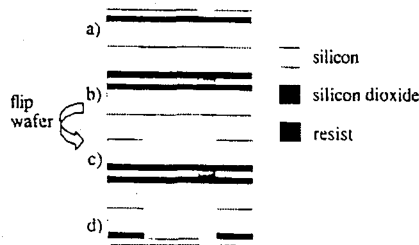

Figure 3. Cantilever Process. a) Pattern cantilevers into device layer. b) Coat with support resist. c) Pattern backside and HDLP etch through wafer stopping on buried oxide layer. d) HF vapor etch oxide and plasma etch the resist for final release.

The cantilevers are then coated with photoresist which will be used as a sacrificial support layer for the final release. Next, the backside of the wafer, polished or unpolished, is patterned with a backside release mask of 8 μm photoresist (Shipley AZ4620). A two part anisotropic HDLP etch is then performed to release the underside of the cantilevers. An aggressive SF_6/C_4F_8 based plasma etch is used to etch through the entire wafer (~500 μm) until the buried oxide layer is reached. Another HDLP etch is then performed using an HBr dominated chemistry to complete the etch in a controlled manner. These HDLP etches will be discussed in detail later.

Then the buried oxide layer is etched in a concentrated hydrofluoric acid (HF) vapor, performed at room temperature and pressure. With the absence of surface tension effects, vapor reaches the bottom of high aspect ratio holes easier than wet etchants. Brief heating of the wafer prior to etching reduces water condensation on the wafer, making more exotic HF vapor etching techniques unnecessary [10]. The thick support resist above the cantilevers enabled a water rinse, which was necessary to remove silicon shards left from the backside etch. Finally the top layer photoresist is stripped in an oxygen plasma to free the cantilevers.

The deep part of the two part etch is performed in a commercial high density low pressure (HDLP) plasma etcher, which uses separate RF sources for the plasma generation (coil) and ion acceleration (substrate platen) [11]. The anisotropy is obtained by alternating between etching and passivating processes. The etch part employs a 600 watt coil, 120 watt platen, 130 sccm SF_6 flow, and 15 mTorr chamber pressure. The passivation is performed at identical plasma power and pressure, but uses 85 sccm of C_4F_8 with no platen power. A repeating cycle of etching for 11 seconds alternating with passivation for 8 seconds resulted in near vertical walls and an etch rate of 4.5 μm/min.

The cantilever release pattern consists of a die with a 10 × 10 array of 100 μm × 500 μm areas. Carefully measuring the etch rate for this pattern enabled consistent stopping on the oxide without overetching. Figure 4 shows a completed deep etch through the wafer, which has stopped on the buried oxide layer. The etch was uniform and selective enough to fully etch die throughout the wafer with only 3800Å of thermally grown silicon dioxide (a common SOI thickness) as an etch stop layer.

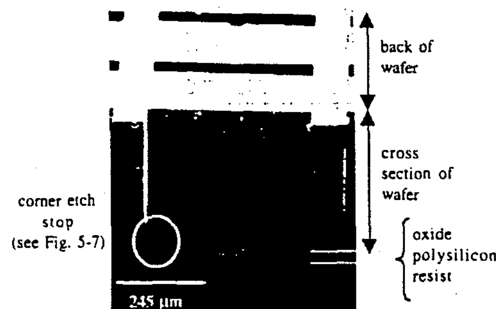

Figure 4. Cross section of a cantilever release region after a deep SF_6 etch through the backside of the wafer. The etch proceeded downward in the picture until reaching the oxide and device layer. The oxide and device layers are supported by thick photoresist. The cantilever is not in the picture.

Critical to the effective length of the cantilevers is the accuracy of the backside etch. The definition of the cantilever base needs to be consistent over a die so that the mechanical characteristics of the cantilevers are uniform throughout the array, facilitating plans for individual cantilever controller and sensor design [4]. Wafer scale uniformity is important for increasing functional device yields. Unfortunately, the uniformity of the etch is such that overetching on the order of minutes is required to clear die throughout the wafer. Using the fluorine based HDLP etch, however, causes extreme lateral silicon etching at the oxide interface, as depicted in Fig. 5.

This can be minimized at a certain radius of the wafer by near perfect timing, but neighboring die will exhibit lateral etching. This is likely because fluorine has the ability to etch silicon spontaneously, without ion bombardment [12]. When the etch reaches the oxide there is a sudden increase in fluorine radicals as the vertical silicon etching has stopped. This increased fluorine etches through the sidewall passivation at the base of the hole, and etches into the silicon. Thus the aggressive SF_6/C_4F_8 works well for etching anisotropically and quickly, but does not consistently define the cantilever base throughout the wafer.

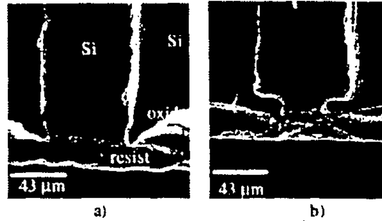

Figure 5. The aggressive SF_6/C_4F_8 based HDLP etch can be carefully timed for a well defined stop in the middle of the wafer (a), but the edge of the wafer still experiences severe lateral silicon etching. These views have the same orientation as figure 4, with the device layer beneath the oxide.

To control the oxide stop, an HBr based HDLP etch is used to finish the backside etch. First the deep etch is stopped early so that silicon feet, shown in figure 6, are left at the cantilever bases throughout the wafer. Then another commercial HDLP etcher, also with separate coil and platen RF sources, but without the sequential etch/passivate ability, is used [13]. Operating at 10 mTorr, with an RF coil power of 250 watts and platen power of 60 watts, HBr (150 sccm flow) and O_2 (15 sccm flow) are simultaneously used to etch the remnant silicon feet. The chemistry of this etch does not permit rapid lateral silicon etching at the oxide interface, as ion bombardment is necessary for activation of the silicon etch [12]. Combined with a high silicon-to-oxide etch selectivity (>200:1), controllable rates (3000 Å/min for Si), and high anisotropy, this etch is ideal for clearing out the remnant silicon feet in a controlled manner. Since overetching can be tolerated, the cantilever bases can be well defined throughout the wafer (Fig. 7).

A completed cantilever array is shown in Fig. 8. A density of 5 tips/mm^2 is demonstrated here, though higher densities are possible with this process. Near perfect yields were obtained, as out of 45 die per wafer, typically 2-3 of the die had single defects. As shown in Fig. 7, the two part etch results in a silicon foot length deviation of 5 µm or less, which is a significant improvement over the 20 µm variations typical of the SF_6/C_4F_8 etch stop. With longer HBr etching, this variation between the center and edge of the wafer could be reduced, especially since the chemistry of the etch tolerates overetching.

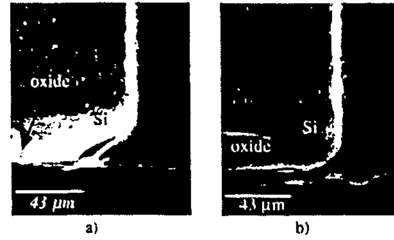

Figure 6. The deep etch is timed to leave a silicon foot in the center (I) and edge (b) of the wafer. The oxide and device layer is supported by thick photoresist.

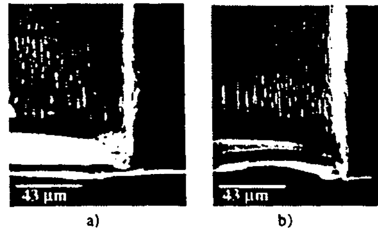

Figure 7. The HBr based HDLP etch clears out the remnant silicon foot in a controlled manner in the middle (a), and edge (b) of the wafer.

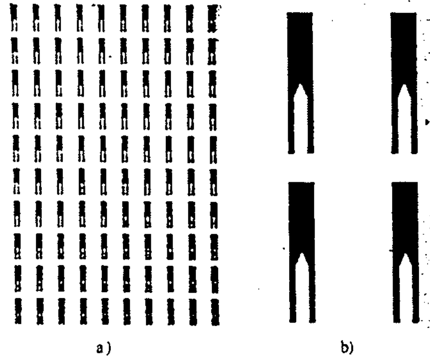

Figure 8. a) Optical photographs of a finished 10 × 10 array of cantilevers, with release regions of 100 µm × 500 µm each. b) Close up of the same array. These cantilevers are made of polysilicon, and are 50 µm wide, 200 µm long, and 1.6 µm wide.

More work needs to be done to improve the absolute accuracy of the etch profile, which is important for this application. The etch profiles are currently slanted out (getting larger as they proceed down) by 1 to 1.5 degrees. Over the thickness of the wafer this generates about a 10 μm absolute error in effective opening area, with a variation of 5 μm. Thus the profile and lateral etch effects combined give less than 10 μm variation in effective cantilever length over the wafer. Further tuning of the etch to passivation time ratio should help rectify the deep profiles.

Another issue is the observation of severe lateral silicon etching at the oxide interface along the longer side (500 μm side) of the cantilever release region. The current uniformity of the deep SF_6/C_4F_8 etch make this unavoidable because the etch rate is slower along the short side of a release region (100 μm side.) This lateral etching on the long side, similar to that pictured in Fig. 5b, does not effect these cantilevers because the cantilever base is only along the short side. However, unless it can be controlled, this phenomena suggests that architectures with multiple cantilevers along the same side in a release region will be difficult to release with the precision demonstrated in this work.

THROUGH-WAFER INTERCONNECTS

In addition to fabricating a high-density array, we have developed techniques to create electrical connections through the wafer. We report here on the fabrication of through-wafer vias (TWV) with small size, ultra-low resistance, and CMOS processing compatibility.

The TWV process consists of three main steps: 1) etching of a high-aspect ratio trench through the wafer, 2) electrical isolation and conformal metallization of the high aspect ratio trench, and 3) patterning of the top and bottom sides of the wafer while protecting the metallized via. The process is outlined in Fig. 9. The substrate is a p-type, 4-inch, 525 μm thick, 10 Ω-cm, double-polished silicon wafer. First, the square vias are patterned using 16-um thick photoresist (Shipley AZ4620). Then vias are etched with the same deep HDLP etcher described in the previous section. Since the vias are 30 μm/side and their depths are 525 um, the aspect ratio of the vias is 17.5:1 (Fig. 9a). The etch rate of the vias is 2.2 μm/min.

To isolate each via electrically, a 1 μm thick thermal oxide is grown at 1100°C. Then, a 1.5 μm thick undoped polysilicon layer is deposited using low pressure chemical vapor deposition (LPCVD) (Fig. 9b). Both the thermal oxide and LPCVD polysilicon are completely conformal on the sidewalls of the vias. The polysilicon serves as the sticking layer for the 250 nm thick CVD copper since the adhesion of the CVD copper is poor on thermal oxides. To decrease the resistance of the vias, a 6 μm thick copper layer is electroplated on top of the CVD copper (Fig. 9c). The resulting sheet resistance is 2.8 mΩ/□. The electroplated copper has good sidewall coverage on the high aspect-ratio vias as shown by the low resistance.

Photolithography over widely varying topography is difficult using a conventional spin-on type photoresist, unless the surface is planarized. Direct application of a spin-on resist over deep trenches or tall mesas creates streaks which cause serous problems during exposure. In addition, it does not coat the inside of the vias where the metal must be protected. To overcome this problem, we used an electrodeposited photoresist (Shipley PEPR 2400)[14]. The resist was 7 μm thick on both the top and the bottom sides of the wafer, and it coated the walls of the vias so that the metal is protected. The resist was then exposed on a standard mask aligner (Fig. 9d). Finally, the copper layer is wet etched in (Fig. 9e) and the polysilicon is dry etched in a conventional SF_6 plasma (Fig. 9f). A finished TWV, depicted in Fig. 10, had a resistance of 50 mΩ.

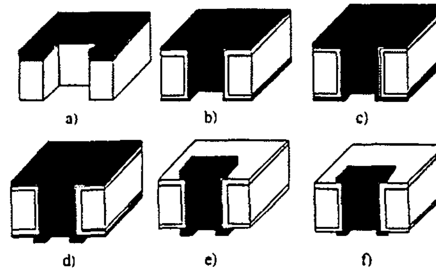

Figure 9. Through wafer via process. a) Etch via through the wafer. b) Isolate vias with thermal oxide and deposit LPCVD polysilicon sticking layer. c) CVD and then electroplate copper. d) Electrodeposit and pattern resist. e) Wet etch copper and f) plasma etch polysilicon to complete TWV.

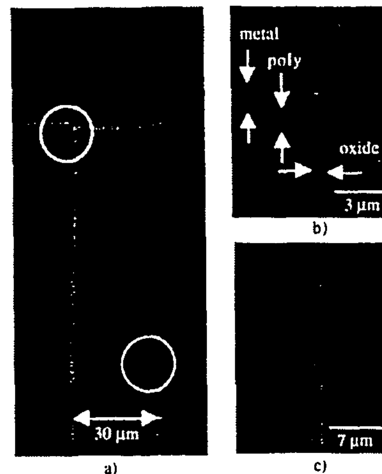

Figure 10. Cross sectional SEM micrographs of a through wafer via. a) The via is 30 μm wide and 525 μm deep. Deposited films have good step coverage at b) the corners and at c) the sidewalls.

CONCLUSION

The ability to fabricate high density, two-dimensional arrays of micromachined cantilevers with backside contacts is critical to the continued advancement of scanning probe technologies. We have reported here on CMOS compatible fabrication techniques which accurately release structures throughout an entire wafer, and form small, ultra-low resistance electrical contacts between the front and back side of the wafer.

Precise HDLP etching with SF_6/C_4F_8 and then HBr are key steps in the cantilever release process, which produces cantilevers with good uniformity (< 10 µm length variation) and high yields throughout the wafer. Probe densities of 5 tips/mm^2 are demonstrated with a 10 x 10 array of cantilevers, though higher densities are possible with this process. Small (30 µm/side), through wafer vias with ultra-low resistance (50 mΩ/via) have also been demonstrated. HDLP etching, CVD copper, and electrodeposited resist result in interconnects with a resistance well below that necessary for piezoresistive cantilever sensing.

Current work includes integrating the two processes and adding integrated piezoresistive cantilevers and tips. Further profile optimization of the deep HDLP etch is also ongoing.

ACKNOWLEDGEMENTS

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