SAND96-2309C
CONF-9609274--1

Lowering of Intralevel Capacitance Using Air Gap Structures

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SEP 26 1996
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ABSTRACT

Interconnect delays, arising in part from intralevel capacitance, are one of the limiting factors in the performance of advanced integrated circuits. In addition, the problem of filling the spaces between neighboring metal lines with an insulator is becoming increasingly severe as aspect ratios increase. We address these problems by intentionally creating a air gap between closely spaced metal lines. The ends of the air gap and reentrant features are then sealed using a spin on dielectric. The entire structure is then capped with silicon dioxide and planarized . Simple modeling of mechanical test structures on silicon predicts an equivalent dielectric constant of 1.9 on features similar to those expected for 0.25 micron technologies. Metal to metal test structures fabricated in a 0.5 micron CMOS technology show that the process can be readily integrated with chemical mechanical polishing and current standard CMOS processes.

INTRODUCTION

As device dimensions continue to shrink, system performance is becoming limited by the interconnect delay. This is a major unresolved challenge to the semiconductor industry. A major component of this delay results from intralevel capacitance [1]. A variety of different techniques have been pursued to address this problem. The use of inorganic spin-on materials for example, hydrogen silsesquioxane (HSQ), is probably the most advanced. However, HSQ only reduces the dielectric constant to ~3.0 [2]. Fluorinated silicon dioxides (FSG) can be deposited by chemical vapor deposition (CVD) through the addition of a fluorine containing species to the reactive gas flow. However, film stability appears to limit the reduction in the dielectric constant to ~3.5 [3]. Spin on organic materials demonstrate low dielectric constants but they suffer from a number of problems. Among these are, poor adhesion and thermal stability, low thermal conductivity and high thermal expansion, low dielectric strength and high leakage currents. Via etch integration problems can also be significant. (see for example ref. 4). Organic dielectrics can also be deposited by CVD, however, the deposition processes are not well developed. Another proposed approach is the use of Xerogels [5]. These materials consist of a porous silicon dioxide network. Since a large fraction of the material is air, these materials can have a very low dielectric constant. However, it is clear that these materials face severe process integration issues.

A second problem being encountered is that the metal thickness is not scaling down as fast as the metal pitch is shrinking. This results in an increasing aspect ratio between metal lines. This trend has driven interlevel dielectric oxide deposition systems to become increasingly more complex, evolving from thermal CVD to plasma enhanced CVD, CVD/SOG (spin on glass) sandwich structures, deposition/etch/deposition systems, O_3/TEOS processes, and now to high density plasma deposition systems. This trend has increased process complexity and cost per wafer. The process we propose exploits the trend towards higher aspect ratio trenches between closely spaced metal lines using simple techniques to lower intralevel capacitance and fill gaps between the metal lines. This is done by intentionally creating an air gap between closely spaced metal lines.

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THE AIR GAP PROCESS

The process is schematically shown in Fig.1. It starts with the intentional formation of a air gap between closely spaced metal lines. During this step a simple, high throughput, high sticking coefficient, poor step coverage process is used. It is important to realize that this step of the process benefits from shrinking dimensions and increasing aspect ratios. Figure 2 shows examples of test structures coated with oxide deposited by plasma enhanced CVD using SiH_4 and N_2O. The presence of the void between high aspect ratio metal lines greatly reduces the dielectric constant between the lines. However, as the air gaps were being formed between closely spaced metal lines, reentrant openings form between lines with slightly wider spacing. Also the ends of the air gaps can remain open where the closely spaced metal lines diverge. All of these features can trap chemicals from down stream processing and are therefore unacceptable. To address this problem we use a spin on material with excellent gap fill characteristics, HSQ (Dow Corning trade name FOx). HSQ is inorganic and contains only Si, H and O. It is thermally stable at the temperatures encountered during back end processing, and has been integrated into standard integrated circuit processing [2]. We have found that this material can seal the ends of the air gaps and any other unfilled or reentrant features, Fig. 3. The HSQ itself also has a relatively low dielectric constant, ~3 and is quite effective at planarization [2]. The remaining processing is relatively standard. We cap the HSQ with plasma enhanced CVD oxide and then globally planarize the wafer using CMP.

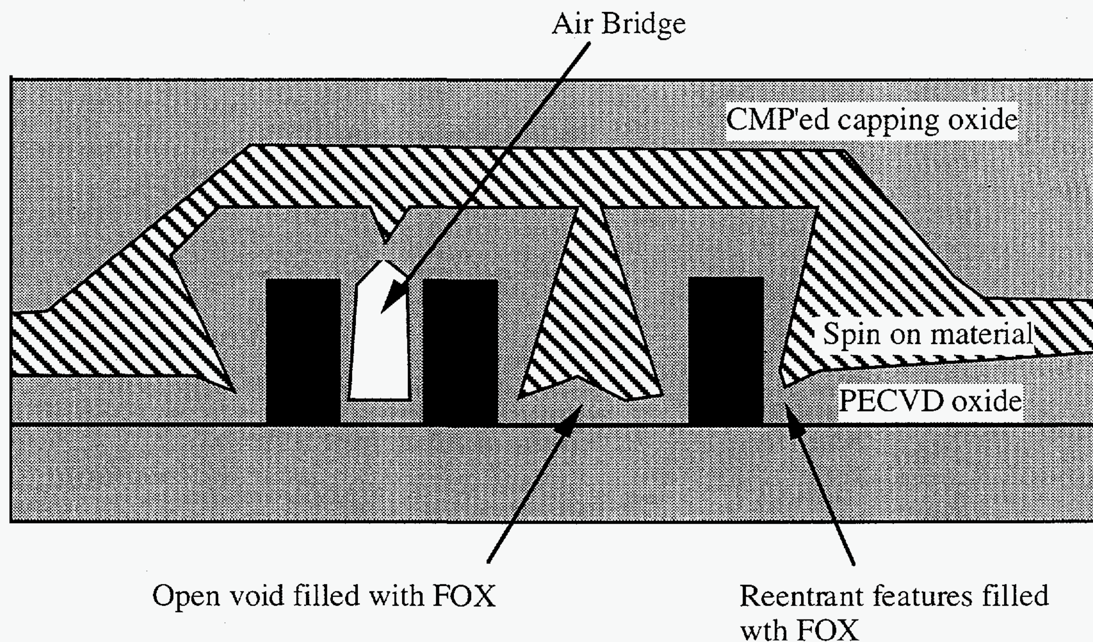


Fig. 1
Schematic of the air bridge process, a void is intentionally formed between closely spaced metal lines using a process with poor step coverage such as plasma enhance CVD. A spin on material is then used to fill reentrant features and regions where the lines were too widely spaced to from an air bridge. The spin on material is then capped with more CVD oxide, which in our case is then chemically mechanically polished.

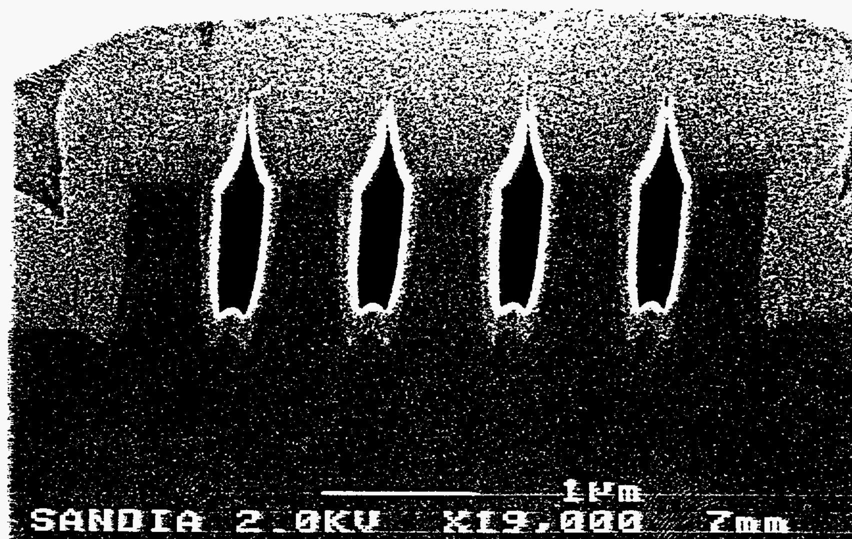


Fig. 2
Example of a mechanical test structure showing the void formed by the CVD process. The spin on material can also be seen on the edges and in the dimples on top.

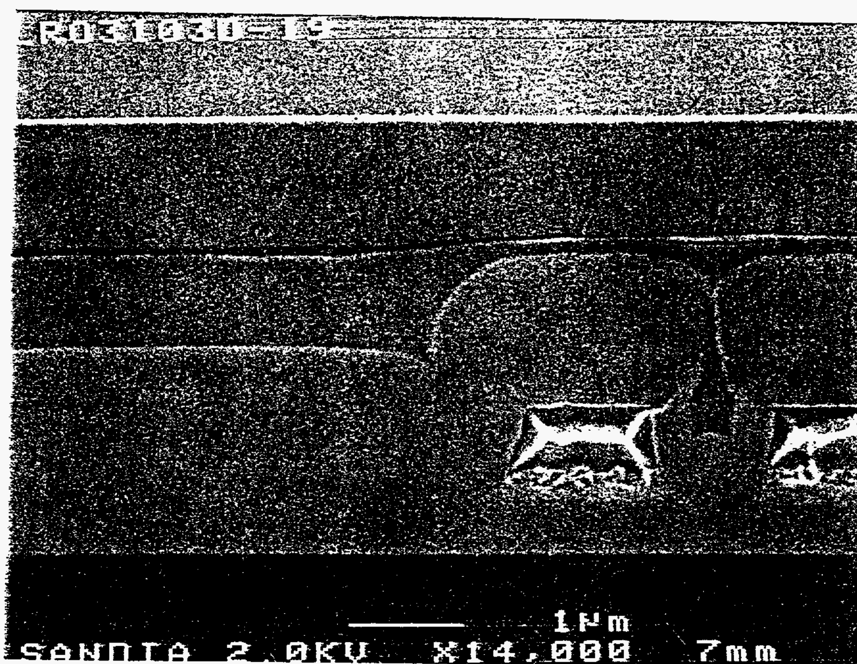


Fig. 3
Example of the gap filling properties of the FOx material. The slight opening remaining between the lines is sufficient to allow the filling of the voids and the reettant corners at the edges. In this exmple the lines are metal and a capping oxided has been added and CMPed planar.

EXPERIMENTAL

In this preliminary work we have investigated two types of test structures. The first consists of purely mechanical test features etched into silicon, the finest having spacings of 0.4 microns. We investigated a range of different aspect ratios. Plasma enhanced CVD oxide was deposited on these structures using an Electrotech Delta system and a SiH_4/N_2O chemistry. Examples of the structures formed are given in Fig. 2.

In the second set of samples, the air bridge approach was integrated into metal-via-metal test structures. These structures were created using a 0.5 micron technology in which the aspect ratio between metal lines is only ~0.7, Fig. 4.

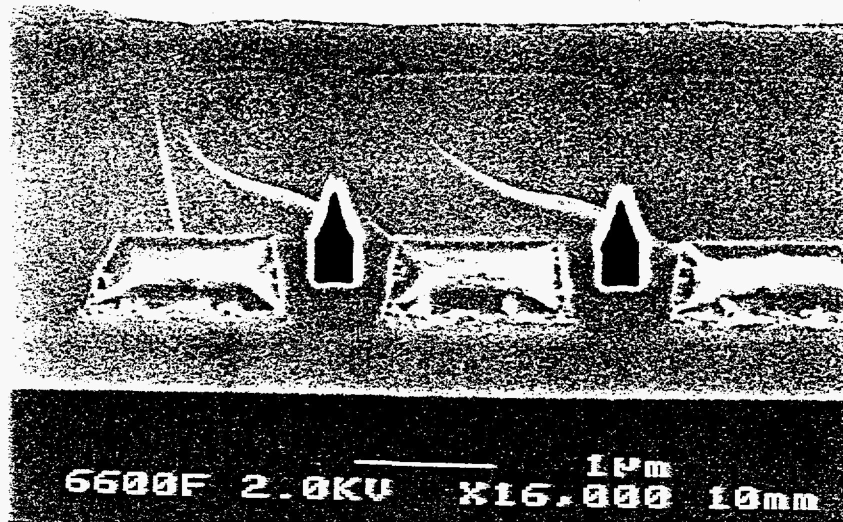


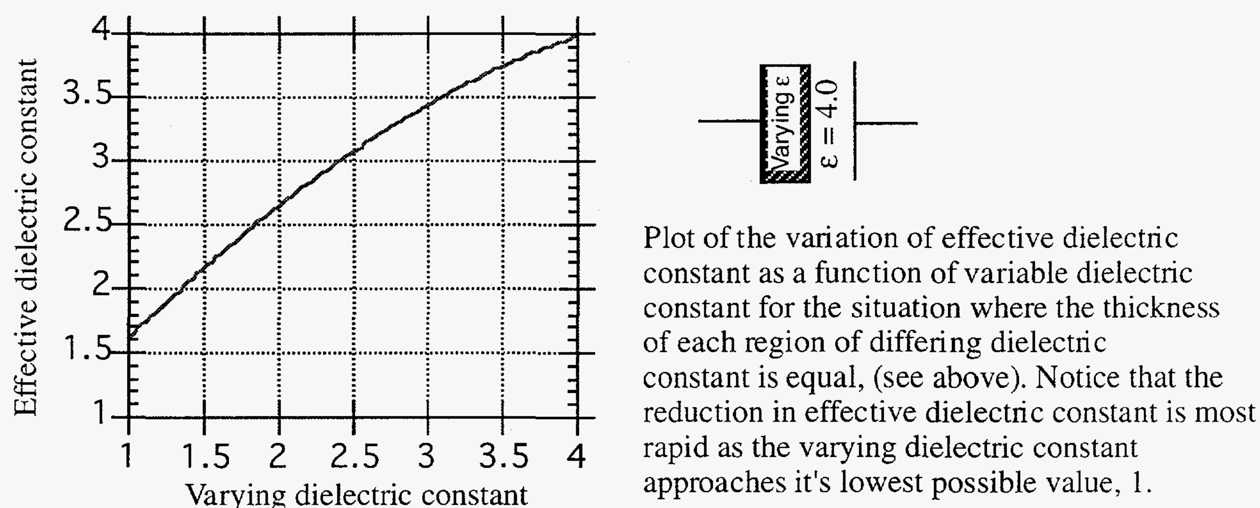
Fig. 4
Example of the process demonstrated on a two level metal test structure. The void was formed dispite the relatively low aspect ratio and sloping walls of the trench. After deposition of the CVD oxide. The FOx material was deposited. This was then capped by further CVD oxide. The whole structure was then planarized by CMP. Vias were then cut to the first level of metal. Tungsten plugs (not shown) were formed by Ti/TiN sputtering and CVD W. Excess tungsten was removed by CMP. This was followed by the deposition of metal 2. We found no evidence of CMP slurry in the voids. Nor any cracking or other problems after W CVD and CMP. The first oxide layer is roughly 0.5 micron thicker than necessary but we were still able to etch the vias and obtained acceptable via contact resistivities.

This experiment was run to ensure that the ends of the voids and reentrant features were in fact sealed and that the process could be integrated into a relatively standard CMOS process. After forming the air gap, HSQ deposition and capping oxide deposition, the wafers were run

through CMP. There was no indication of any problems at CMP such as the infiltration of slurry or liquid into the voids. Nor was there any indication of cracking of the ILD during subsequent processing, the highest temperature encountered was a ~430°C CVD tungsten deposition to form the via plug. The only problem encountered was a significant increase in the ILD thickness. This is due to the relatively wide spacing between lines which necessitated a thick oxide deposition in order to form a void. As dimensions shrink, this situation will improve since the dielectric thickness is not scaling at the same rate as the reduction in line spacing. Even though not optimal, this test clearly shows that the HSQ material can be used to seal the ends of the air gaps and the approach can be integrated into standard fabrication processes.

RESULTS AND DISCUSSION

In Fig. 5 we plot the relative dielectric constant of a sandwich structure with the gap between the oxide layers filled with materials of different dielectric constant. Notice that the relative dielectric constant is falling faster than would be expected from simply the volume fractions of the two components filling the gap. The reason for this is that the capacitance of capacitors in series is the inverse sum of the inverse of the separate capacitances. This is one of the benefits of using effectively the lowest possible dielectric constant material between the metal lines.



Plot of the variation of effective dielectric constant as a function of variable dielectric constant for the situation where the thickness of each region of differing dielectric constant is equal, (see above). Notice that the reduction in effective dielectric constant is most rapid as the varying dielectric constant approaches it's lowest possible value, 1.

Fig. 5

The results obtained on one of the mechanical test structures is schematically rendered in Fig. 6. Electrically, the capacitance of the system can be modeled as three capacitors in series, in parallel with a fourth capacitor. The three capacitors in series are the two oxide films along the walls and the air gap between them. The fourth capacitor is formed by the presence of the oxide deposited into the bottom of the trench. In our simple analysis we ignore the contribution of fringing fields. The effective dielectric constant of the structure in Fig. 6 is calculated to be 1.9. This predicted performance is superior to all materials except the lowest reported organics and xerogel type materials. Test features with an aspect ratio of 3 predict a dielectric constant of 1.5, which is surpassed only by xerogels and foams. Even the metal line example given in Fig. 4 in which the formation of the void is hindered by the low aspect ratio of the feature and the tapered walls, the calculated dielectric constant is found to be 2:8. This is considerably lower than if the entire space between the lines was filled with FGS.

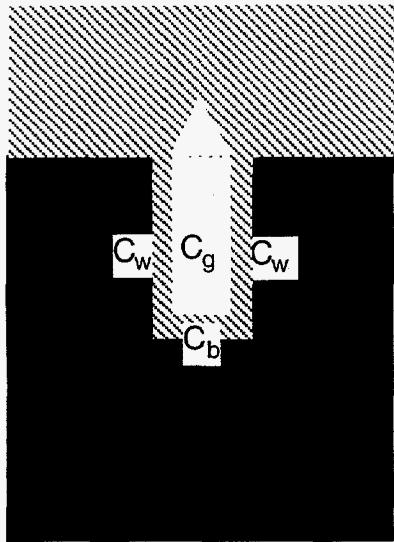
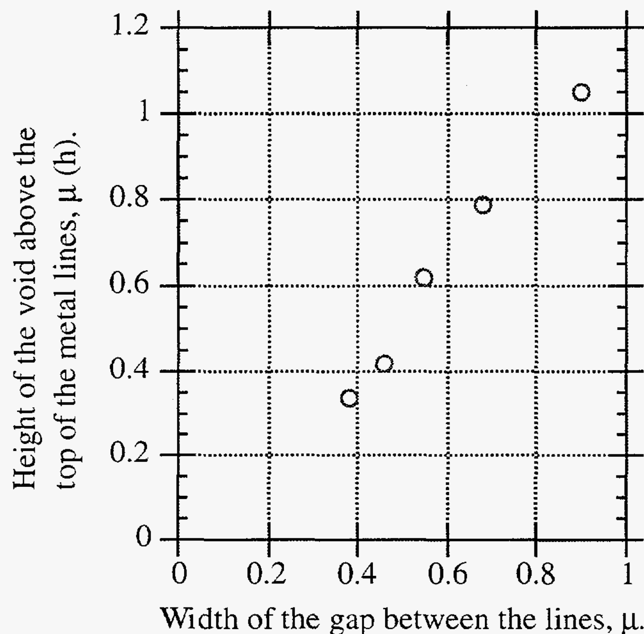


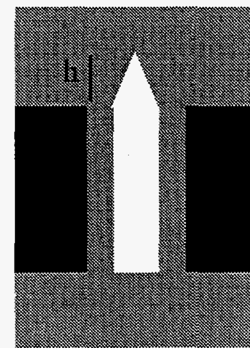
Fig. 6

$$C_t = C_b + \frac{1}{\frac{1}{C_g} + \frac{1}{C_w} + \frac{1}{C_w}}$$

Schematic representation of the result expected for metal lines with aspect ratio of three, based on the results obtained using the mechanical test structures. Above is the simple electrical model we used to determine the effective dielectric constant, 2.3 in this case.

As yet we have not optimized the deposition process to have a poor sticking coefficient, nor have we optimized the HSQ deposition process. Using our current plasma enhanced CVD SiH_4/N_2O process we have found the height of the peak of the void above the lines to be roughly equal to the space between the lines, Fig. 7. More exotic approaches to the gap fill oxide such as sputtering or e-beam deposition are expected to greatly reduce side wall coverage and void height. In our experiments the thickness of the HSQ on planar structures was 0.2 to 0.3 microns. It should therefore be readily possible to keep the interlevel dielectric thickness at close to 1 micron for 0.25 and 0.18 micron technologies. We find that the HSQ material plugs the first 3 to 5 microns of 0.6 micron wide trenches with an aspect ratio of 2 capped with 1.1 microns of oxide.





Height of the top of the void above the top of the metal line (h above) as a function of line spacing. For the un-optimized process used in this work the two are roughly equal.

Fig. 7

There are many potential advantages to this approach. Firstly it becomes easier to implement and more effective in lowering the dielectric constant as the dimensions shrink and aspect ratios increase, since it becomes easier to form the void. Secondly, the air gap forms only where it is most needed, the bulk of the rest of the ILD is SiO_2, with its superior thermal conductivity. Thirdly, the metal lines are completely encapsulated in excellent quality SiO_2 and since there are no organics used, all the materials display excellent thermal stability. Finally, the tools needed to execute this scheme are extremely simple, inexpensive and have the potential for high throughput.

CONCLUSIONS

We have demonstrated the feasibility of using an air gap approach to reduce intralevel capacitances and deal with high aspect ratio features. We have integrated the approach into a relatively standard 0.5 micron design rule CMOS process. Simple analysis of mechanical test structures fabricated in silicon indicate that it should be possible to achieve significant reductions in intralevel capacitances and solve the gap fill problem using this simple approach.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the support of Sandia's Microelectronics Development Laboratory, especially, Dale Hetherington for CMP support and Patrick Shea for SEM support. Sandia National Laboratories is supported by the U.S. Department of Energy under contract number DE-AC04-94AL85000.

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