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Low Resistivity Ohmic Contacts to Moderately Doped n-GaAs with Low Temperature Processing

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A low-temperature process for forming ohmic contacts to moderately-doped GaAs has been optimized using a PdGe metallization scheme. Minimum specific contact resistivity of 1.5×10^{-6} $-cm^2$ has been obtained with a low anneal temperature of 250 C. Results for optimizing both time and temperature are reported and compared to GeAu n-GaAs contacts. Material compositions was analyzed by X-ray photoelectron spectroscopy and circuit metal interconnect contact resisitivity to the low-temperature processed PdGe contacts is reported. For the lowest temperature anneals considered, excess Ge on the ohmic contact layer is suspected of degrading interconnect metal contacts, while higher temperature anneals permitted interconnect metal formation with negligible contact resistivity. Atomic force microscopy measurements showed that the PdGe surface morphology is much more uniform than standard GeAu contacts.

I. Introduction

Low temperature ohmic contact processing is required for a variety of novel material systems that are grown at temperatures as low as 300 C which limits processing temperatures to maintain material layer integrity. In addition, for some photonic device applications where free carrier absorption is deleterious to device performance, device growth on low-to-moderately doped substrates is desirable. Significant work has been reported to optimize contact schemes for heavily-doped GaAs and with higher temperature processing, while much less processing optimization has been performed in the regime of moderate doping and low-temperature processing.

The standard GeAu n-GaAs contact is unsuited for low-temperature processing because relatively high anneal temperatures are required to achieve low contact resistivity with acceptable uniformity. In addition, contact-spiking is a problem and the contact is of questionable reliability due to high current densities at Ge-rich islands.[1] As an alternative contact metal, a PdGe contact formed by solid phase epitaxy was recently reported.[2] On n^+-GaAs, excellent specific contact resistance for anneal temperatures above 300 C are reported; however, high-temperature thermal stability is uncertain.[2] Most work on this metallization scheme has focused on improving thermal stability to make the contact suitable for subsequent high-temperature processing.[3,4]

In this study we optimized the anneal temperature and time for low-temperature processing of PdGe contacts to n-GaAs substrates doped to ~2.5 $x10^{17}$ cm^{-3}. Anneal temperatures from 200 to 400 C and times from 5 to 30 minutes were investigated. Excellent contact resistivity of 1.5 x 10^{-6} $-cm^2$, comparable to our standard GeAu n-GaAs contact, was obtained. The material composition profile was analyzed by X-ray photoelectron spectroscopy (XPS) in order to avoid the spectral interference encountered for Auger emission from the Ga, Ge, As (LMM) series. The result suggests that the mechanism for ohmic contact formation is heavy-doping of the GaAs at the metallurgical junction. Surface morphology was characterized by atomic force microscopy (AFM).

The PdGe contact has much lower RMS roughness without evidence of contact spiking which is characteristic of GeAu alloyed contacts.

In addition to optimizing a low-temperature process for actual ohmic contact fabrication, issues related to applying this contact scheme to integrated circuits applications were investigated. For circuit applications it is not sufficient that the ohmic contact specific resistivity be low. The interconnect metal-to-ohmic metal specific contact resistivity must also be low; however, this property has not been reported. In the temperature range investigated for ohmic contact optimization, we also report the PdGe alloy sheet resistance and interconnect specific contact resistance as a function of anneal temperature where ohmic metal anneals were performed prior to interconnect metal deposition.

II. Experimental

Ohmic contacts were deposited by electron-beam evaporation and patterned by standard photolithographic liftoff technique. First, our standard GeAu contact metal was deposited and annealed at 400 C for 90 sec to realize a blanket-coverage, backside contact on the silicon-doped (2.5×10^{17} cm^{-3}) n-type 100-GaAs substrates that were used in this study. Following a wet etch to expose a pristine surface, frontside contacts with 50 nm of Pd followed by 136 nm of Ge were patterned and deposited. After contact metal patterning, a low-temperature (150 C) silicon-dioxide dielectric was deposited by PECVD. Via holes through the dielectric were opened by standard RIE SF_6 etching. Device samples were then annealed for various temperatures (200-400 C) and times (5-30 min) to determine optimum anneal conditions. Anneals were performed in a tube furnace and nitrogen ambient. Sample loading consisted of placing the device sample on a quartz boat that was approximately at the anneal temperature which precluded tightly controlled temperature ramping during anneals. To insure uniform current distribution during testing, 50 nm of titanium for adhesion followed by 300 nm of Au was deposited as a pad metal. Analysis was performed with the Cox and Strack technique[5] with the following diameter contacts: 6, 8.5, 10, 15, 20, 26, 30, 37, 40, 50 and 100 m. Four-point probe resistance measurements consisted of sweeping the

current density through the PdGe contact from 1000A/cm^2 to verify linear current-voltage (I-V) characteristics and determining the resistance from linear regression of the I-V curve.

Chemical analysis was performed with XPS in the sputter depth profile mode. Al(Kα)-induced photoelectron emission from the Pd(4p), As(3d), Ge(3d) and Ga(3d) core level transitions were used to quantify element composition at the surface. Sputtering conditions were 3 keV Ar^+ ion sputtering at a current density of 2 A/cm^2. The ion beam was rastered over an area larger than that used for analysis to eliminate the possibility of incorporation of signal from the crater sidewall. Sputtering rates for Ge and Pd were 0.94 nm/min and 0.71 nm/min respectively. Surface morphology was measured by AFM. Both electrical characteristics and morphology for the optimized process were compared to our standard n-GaAs, alloyed GeAu contacts that were rapid thermal annealed at 400 C for 90 seconds.

The PdGe ohmic metal sheet resistance and interconnect metal-to-ohmic metal specific contact resistivity was investigated by employing the transmission line model (TLM) and devices with 50 x 100 m^2 contacts spaced 3, 5, 9, 13 and 20 m apart. PdGe metal conduction channels were patterned, deposited and annealed as described for ohmic contact processing. The TLM-devices were fabricated on undoped, semi-insulating 100-GaAs wafers. After annealing the PdGe conduction channel, Ti/Au (50 nm/300 nm) contact pads were patterned by liftoff. Four-point probe resistance measurements with the current density through the PdGe metallic layer swept from 1000A/cm^2 were performed and the resistance was determined from linear regression of the I-V curve. In the TLM-analysis, the sheet resistance under the contact was assumed to be equal to the sheet resistance between the contacts, which is a valid assumption because the TiAu interconnect metal to PdGe conduction layer was not annealed and alloying was minimized.

III. Results and Discussion

The I-V characteristics measured between two large area PdGe contacts fabricated with 30 minute anneals in nitrogen at 200, 225 and 250 C are shown in Fig. 1. Probe resistance is included in these data since the measurements were made with only two probes. Unannealed samples and samples annealed below 225 C showed highly non-linear I-V characteristics. A

dramatic change from back-to-back Schottky diode characteristics to highly linear, ohmic contact behavior occurred at 225 C and persisted to the highest anneal temperature considered which was 400 C. This change to ohmic behavior is attributed to enhanced Ge diffusion at the higher temperatures through the Pd-layer to the GaAs-Pd interface. Our result is consistent with reports of reactions of Ge with Pd occurring at temperatures as low as 200 C.[2]

Two mechanisms for ohmic contact formation have been proposed. The first mechanism presented is solid-phase epitaxial growth of a Ge-layer at the metal-semiconductor interface which results in a barrier lowering due to the heterojunction formed at the wide-bandgap GaAs and the narrow-gap Ge layer. Evidence of this mechanism has been presented for samples annealed at much higher temperatures (425 C) where Auger analysis showed a distinct Ge-layer between the PdGe alloy and the GaAs semiconductor interface.[6] The second mechanism, which we believe to be responsible for the low contact resistivity obtained in this work, is Ge-doping of the GaAs to form a low-resistance tunneling-contact. This conjecture is supported by XPS analysis of samples annealed at the low anneal temperature of 250 C which did not show a distinct Ge-layer, but rather a high Ge-content in the GaAs at the semiconductor-metal interface.

Specific contact resistivity versus anneal temperature is shown in Fig. 2. The data was measured with the Cox and Strack method. All anneals were 30 minute anneals in a nitrogen ambient. For unannealed samples and samples annealed below 225 C the contacts are non-ohmic. Excellent contact resistivity was obtained for anneals at and above 225 C. The minimum specific contact resistivity of 1.5×10^{-6} Ω-cm^2 was obtained at 250 C. This value is comparable to the results obtained by Marshall *et al.* for 30 minute anneals at 325 C.[7] Our results show that excellent contacts to moderately doped n-GaAs can be fabricated at much lower temperatures than previous investigations considered at this doping level. This low-temperature minima in resistivity for contacts to moderately doped GaAs contrasts with results for degenerately doped material where the specific contact resistance minimum is at 350 C.[2] Later we show that the higher resistivities for anneals below 350 C may have been influenced by the actual metal resistivity in addition to changes in the specific contact resistivity to the GaAs. As the anneal temperature was

increased to 400 C, we found slightly higher resistivities in the range 2-3 x 10^{-6} -cm^2. These results at higher temperature anneals are comparable with previously reported results for moderately doped GaAs.[3,7] The important new results is that excellent contacts can be formed at much lower anneal temperatures than were previously investigated and are often required to maintain material structure in new material systems. For comparison, our standard GeAu contact process yielded 2.9 0.6 x 10^{-6} -cm^2 specific contact resistivity.

In addition to optimizing a low-temperature anneal, the anneal time was optimized as well. We investigated anneal times from 5 to 30 minutes for 250 C anneals. With only the 30 minute anneals were uniform, consistently low-resistivity contacts realized. A 5 minute anneal greatly improved the I-V behavior from highly non-linear to slightly non-linear ohmic and ten minute anneals further improved the contact with the best results being within a factor of ten of the optimized contact but the consistency between processing lots was poor. Twenty minute anneals actually degraded the contact while 30 minute anneals yielded uniform, repeatable contacts with a specific contact resistivity of 1.5 x 10^{-6} -cm^2.

The contact-metal compositions of as-deposited samples and with optimum anneal conditions were profiled with XPS analysis. In Fig. 3a atomic concentration versus sputtering time is shown for the unannealed sample. The data clearly show the Ge- and Pd-layers on GaAs with ~2 atomic-% of Ge at the GaAs-metal interface. This implies significant Ge-diffusion through Pd under common electron beam evaporation conditions; our evaporator does not provide sample cooling. Although the Ge-concentration is high for unannealed samples, as shown earlier, non-ohmic I-V characteristics were observed. In Fig. 3b atomic concentration versus sputtering time is shown for the annealed sample. The Ge-concentration at the GaAs-metal interface is much greater (~20 atomic-%) after the 250 C 30 minute anneal; however, a Ge-layer indicative of solid-phase epitaxial growth of Ge at the GaAs interface was not found. The high Ge-concentration at the interface is believed to be the mechanism that is responsible for the low contact resistivity. With the high concentration of Ge found at the surface, only a small fraction would be required to be active donors to form a heavily-doped contact layer that yields a low-resistance tunneling contact.

The profiles in Fig. 3 also demonstrate a significant penetration of Pd and Ge into the GaAs. Penetration could be due to ion-beam knock-on or thermal diffusion. We believe that the origin of the tailing concentration profile is diffusion dominated based on the following argument. The annealed sample showed an increased Ge concentration and a decreased Pd concentration at the GaAs-interface when compared to the as-deposited sample. The expected effects on knock-on due to the changes in concentration would be an increase in Ge knock-on and a decrease in Pd knock-on during analysis of the annealed sample. However, sufficiently deep in the GaAs where knock-on effects are minimized the concentration profiles of the as-deposited and annealed samples indicate opposite trends. These results demonstrate there is coupled Pd and Ge diffusion. Significant diffusion of both Pd and Ge is consistent with previous reports of other contact metal schemes on GaAs.[8,9] If Pd and Ge does diffuse to significant depths in to the GaAs, the high impurity level could greatly impact device performance and contact reliability. More work is underway to accurately characterize the depth of Pd and Ge diffusion.

The XPS results show that a relatively uniform PdGe compound with roughly 3:2 Pd:Ge composition was formed during the anneal. This ratio is roughly maintained in the GaAs bulk. Due to the Pd and Ge initial relative layer thicknesses, all of the Pd has been consumed in the PdGe formation and an excess of Ge remains on the contact surface after annealing. The distinct interface between excess Ge and the PdGe alloy shows a limited solubility of Ge in Pd. Excess Ge on the surface may degrade interconnect metal contact resistivity to the PdGe contact, hence, for circuit applications the Ge layer thickness should be reduced from thicknesses that were considered here.

Electrical characterization of Ti-Au metal interconnects to the PdGe ohmic contact revealed both high-sheet resistance and high metal-to-metal contact resistance for low temperature anneals. As shown in Fig. 4, below 300 C both the specific contact resistivity and the variation in resistivity between devices and lots increased as the anneal temperature was decreased; below 250 C the interconnect metal contact resistivity became the dominant component. With lower temperature anneals, incomplete PdGe formation with excess Ge on the surface is suspected of degrading the

interconnect metal contacts. Above 250 C, the interconnect metal specific contact resistivity was negligible relative to the semiconductor-contact resistivity. Consistent resisitivities with small variations between samples were realized for anneals above 300 C. Sheet resistance of 3.4 and 3.1 per square were obtained for anneals at 300 and 350 C respectively. The conclusion for circuit applications is that the PdGe contact anneal temperature must be sufficiently high to yield a low-resistivity interconnect metal interface.

These results are certainly important for circuit applications, but also must be considered for contact characterization. Such high sheet resistance can be important with measurements of contact resistance. As an example, errors will result in four-point TLM measurements if the current is not uniformly distributed across the contact because the voltage measurement will be low and because the one-dimensional transmission line model used to extract the specific contact resistivity is not valid. To eliminate these problems, a highly conducting probe-pad must be deposited over the PdGe contact metal. In this study we used a TiAu probe pad to insure uniform current distribution.

An additional issue in circuit fabrication is the device ohmic contact metal morphology which was characterized by AFM. The morphology of the optimized contact with low-temperature processing was compared to the standard GeAu contact. The as-deposited contacts have comparable surface morphology with RMS roughness of 0.378 nm for the PdGe and 0.893 nm for the AuGe. Shown in Fig. 5 is the AFM contour plot for both contacts after anneals. RMS roughness increased slightly for the PdGe contact to 1.3 nm, while the roughness of the GeAu contact increases to 4.0 nm. In addition, the PdGe contact is much more uniform while the AuGe contact shows evidence of spiking.

IV. Summary

A low-temperature process for forming PdGe ohmic contacts to moderately-doped GaAs has been optimized. Minimum specific contact resistivity of 1.5×10^{-6} Ω-cm^2 was realized with a low anneal temperature of 250 C. Post-anneal XPS analysis showed a high concentration of Ge at the ohmic metal/semiconductor and preliminary results indicate that a significant amount of Ge has

diffused into the GaAs which may impact device reliability. Characterization of TiAu interconnect metal to the annealed PdGe contact shows that annealing above 250 C permits interconnect metal formation with negligible resistance. Surface morphology of the PdGe contacts was shown to be more uniform than standard GeAu contacts. The contact has been successfully applied to a II-VI reflectance modulators fabrication process which required low-temperature processing and should prove useful for both device research and circuit fabrication.

Acknowledgments

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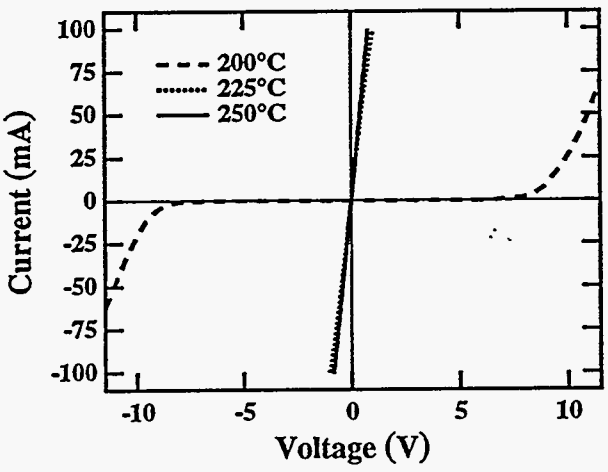

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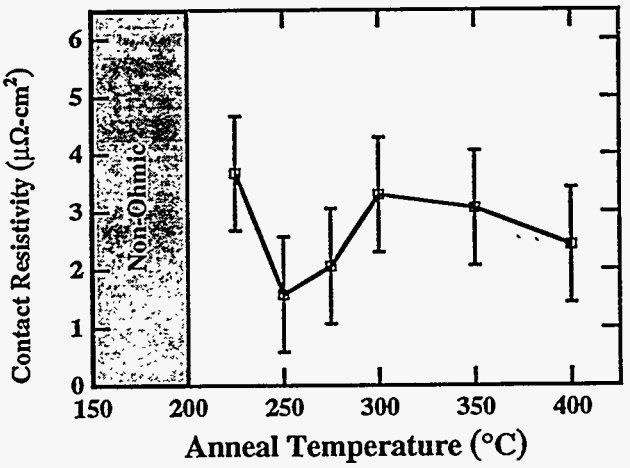

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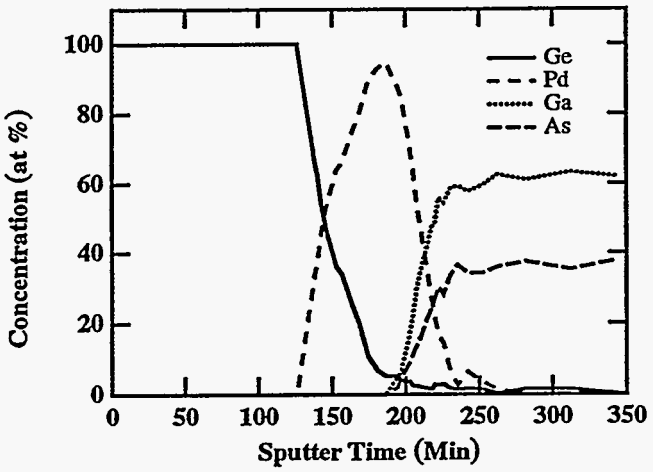

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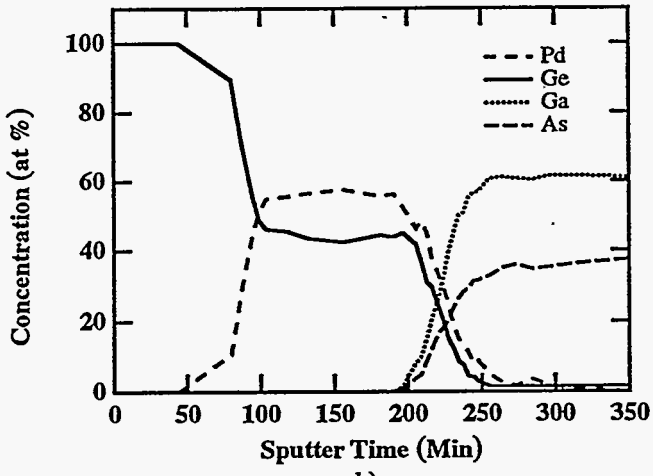

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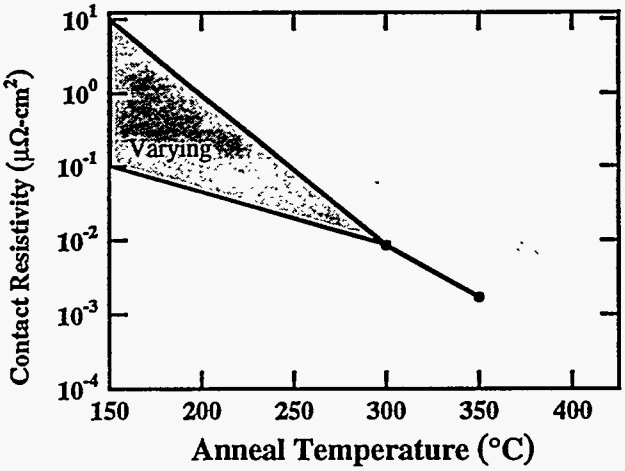

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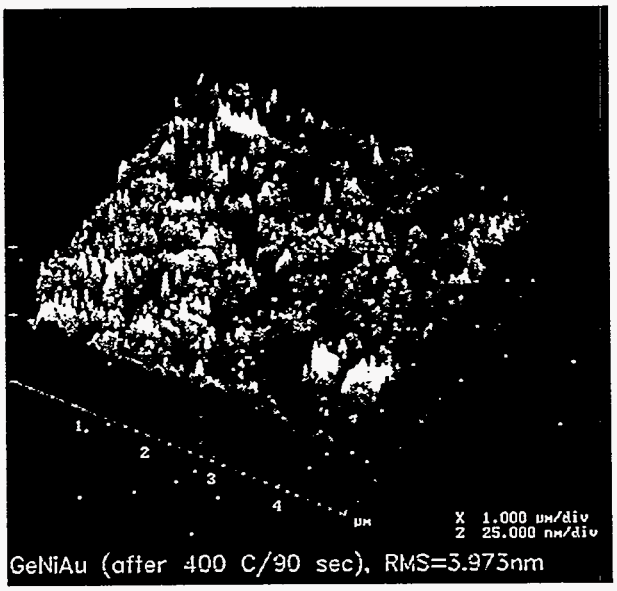

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Figure 5.
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