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High-Efficiency One-Sun Photovoltaic Module Demonstration Using Solar-Grade Cz Silicon

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HIGH-EFFICIENCY CELL STRUCTURES AND PROCESSES APPLIED TO PHOTOVOLTAIC-GRADE CZOCHRALSKI SILICON

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ABSTRACT

We performed a detailed study to examine the limiting performance available using "photovoltaic-grade" Cz silicon. Photovoltaic-grade silicon refers to silicon produced by the photovoltaic industry, which may differ from the silicon used in the semiconductor device industry in impurity and defect concentrations. The study included optimization of fabrication processes, development of advanced device structures, and detailed model calculations to project future performance improvements. Process and device optimization resulted in demonstration of 75-μs bulk lifetimes and 17.6%-efficient large-area cells using photovoltaic-grade Cz silicon. Detailed calculations based on the material and device evaluation of the present work project efficiencies of 20% for photovoltaic-grade Cz silicon with properly optimized processing and device structures.

INTRODUCTION

The requirements for achieving high efficiencies are now well established for crystalline-silicon (c-Si) solar cells [1]. High-efficiency c-Si cells feature long injected-carrier lifetimes and well-passivated surfaces in order to minimize intrinsic loss mechanisms (recombination). High-efficiency c-Si cells also feature sophisticated grids and antireflection coatings to minimize extrinsic loss mechanisms (series resistance and reflectance). Efficiencies of 24% and 21% have been demonstrated with float-zone-refined (FZ) and high-purity Czochralski (Cz) c-Si substrates, respectively [2,3]. These cells required several high-temperature process steps and several photolithography steps with precise alignments for device fabrication, and used high-quality processing and high-purity "semiconductor-grade" c-Si substrates to ensure long bulk lifetimes.

The photovoltaic industry typically uses c-Si substrates ("photovoltaic-grade") with possibly higher metallic impurity concentrations, higher oxygen and/or carbon concentrations, or higher microdefect densities due to non-optimal crystal growth and to uncontrolled impurities in the silicon feedstock. For example, crystallographic defects are believed responsible for low-lifetime regions in multicrystalline-silicon (mc-Si) substrates, while high-lifetime regions are limited by Fe-related recombination sites [4]. Similarly, recombination that is possibly related to FeB pairs has been recently implicated in photon degradation in photovoltaic-grade single-crystal solar cells [5]. In our experience, the bulk lifetime of photovoltaic-grade c-Si degrades more easily with thermal processing and some photovoltaic-grade c-Si materials degrade continuously with multiple high-temperature furnace steps [6]. On the other hand, Cz substrates used for ULSI integrated-circuit fabrication are sufficiently free of impurities and defects that residual recombination is due to intrinsic oxygen-related recombination centers [7]. The net result is that process optimization may be different for photovoltaic-grade c-Si materials than for semiconductor-grade c-Si materials.

We recently reported on development of high-efficiency cells using low-oxygen photovoltaic-grade mc-Si substrates grown by the Heat Exchanger Method™, which included the demonstration of a 15%-efficient mc-Si module [8]. In this paper, we report results of a detailed study to develop high-efficiency c-Si solar cells using photovoltaic-grade Cz silicon. The purpose of this study is to determine the limiting performance available from such materials. The study included optimization of the fabrication process to maintain and/or upgrade the bulk lifetime, and development of advanced device structures. A recent report provides a more complete description of this work [9]. A key result of this work is the projection that efficiencies of 20% are possible using solar-grade Cz silicon.

EXPERIMENT

All processing was performed at Sandia National Laboratories in a Class 100 cleanroom (Photovoltaic Device Fabrication Laboratory) with high-purity chemicals and extensive process controls [10]. Many of the experiments used statistical experimental designs, which is a very efficient experimental procedure for process optimization [10]. Many of the experiments also used microwave-detected photoconductance decay (PCD) to measure the effective lifetime of injected carriers [11]. The effective lifetime measured by PCD is a well-known function of both the bulk lifetime (τ) and the surface recombination velocity (S). Other experiments fabricated complete cells. Cell fabrication used photolithography, evaporated metallizations, and evaporated antireflection coatings in order to minimize extrinsic loss mechanisms. We used a relatively simple single-mask high-efficiency sequence that can fabricate either nine 4.6-cm^2 cells or one 42-cm^2 cell per 100-mm diameter wafer [12]. This cell fabrication sequence can be completed with only a single high-temperature furnace step, although most sequences used two high-temperature steps (phosphorus diffusion followed by aluminum alloy).

The photovoltaic-grade Cz silicon was obtained from a commercial c-Si fabrication line (Siemens Solar Industries - SSI) that is currently the world's largest photovoltaic manufacturing plant. The material was not specially selected for this project. This material is p-type (boron) with a bulk resistivity around 1 Ωcm, has an interstitial oxygen concentration around 30 pmma (ASTM F121-80), uses a variety of excess silicon feedstocks from the integrated-circuit industry, and is grown with a

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diameter of 5.3 inches. This study complements previous work that examined several advanced back-surface structures with photovoltaic-grade Cz silicon and used commercial fabrication processes [13].

PROCESS OPTIMIZATION

The purpose of process optimization is to achieve the desired device structure while maintaining long bulk lifetimes. The bulk lifetime in c-Si frequently changes during high-temperature steps when impurities and defects become mobile. Hence, we performed a number of experiments that examined the effect of the major high-temperature steps (phosphorus diffusion and aluminum alloy) on the bulk lifetime.

The first experiment evaluated the bulk lifetime of photovoltaic-grade Cz silicon as a function of phosphorus-diffusion temperature (Fig.1). The phosphorus diffusion parameters for each temperature were selected to yield similar diffusion profiles that are also typical of high-efficiency cells (i.e., a sheet resistance around 100 Ω/□ and surface concentration less than 10^{20} cm^{-3}). These phosphorus diffusions also provide excellent surface passivation (estimated surface recombination velocity less than 300 cm/s), so that the effective PCD lifetime is a good indication of bulk lifetime. This evaluation is performed on each new set of SSI Cz silicon slices received at Sandia, so the experiment was performed on materials from a variety of ingots and over a span of several years.

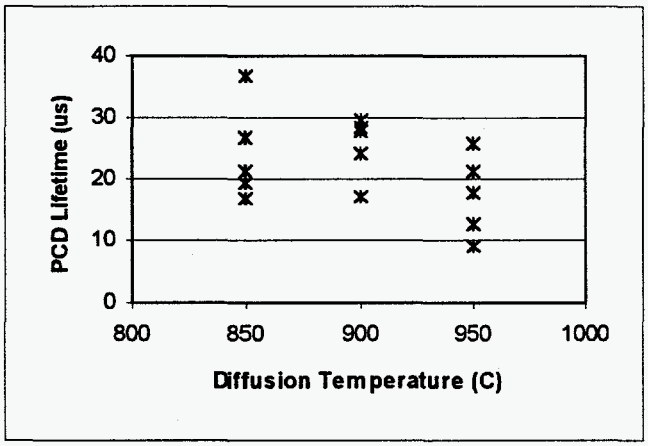

Fig. 1. PCD lifetime of phosphorus-diffused samples as a function of diffusion temperature. Each data point represents average of 10 measurements.

This experiment found a preference for lower diffusion temperatures, with a PCD lifetime around 30 μs for 850°C-diffused samples (Fig. 1). Due to the similarity in surface passivations for the different diffusion conditions, the degradation in PCD lifetime with higher phosphorus diffusion temperature is primarily due to degradation in the bulk lifetime. The bulk lifetime can be calculated using the measured PCD lifetime if there is an independent estimate of S. S was calculated for the phosphorus-diffused surfaces in this experiment using the measured bulk resistivity and the measured emitter saturation current density (J_{oe}). J_{oe} is measured independently on intrinsic FZ wafers, and is between 100 and 300 fA/cm^2. The effective PCD lifetime of 30 μs therefore corresponds to an estimated bulk lifetime between 50 and 100 μs, which agrees with an independent measurement of 75 μs by Narasimha and Rohatgi [14]. This bulk lifetime is comparable to the bulk lifetime limited by intrinsic oxygen-related recombination centers for the resistivity and oxygen concentration of SSI Cz material [7]; hence, this material approaches semiconductor-grade silicon in quality when processed optimally.

While the best results approach semiconductor-grade silicon, the majority of evaluations found lower lifetimes (Fig. 1). There are a large number of variables associated with high-temperature processes (ramp rates, time, temperature, furnace ambient, etc.) and with surface preparation (clean, etch, etc.) that might affect the bulk lifetime through a high-temperature process. Hence, we performed a series of experiments that examined several variables associated with the phosphorus-diffusion process and with the aluminum-alloy process.

Knobloch *et al.* report that the temperature ramp rates are important parameters for processing Cz silicon [3]. We therefore examined the effect of temperature ramp rate on SSI Cz silicon. The largest change in temperature occurs during the insertion (push) or removal (pull) of the wafers from the furnace, so the experiment examined the effect of several push/pull temperatures and boat insertion rates on the diffusion length and on the performance of cells using photovoltaic-grade Cz silicon (Fig. 2). The low-temperature push with slow ramp rate produced the lowest PCD lifetime and lowest cell performance. The preference for a high push/pull temperature and rapid ramp rates agrees with previous studies using high-oxygen-content silicon, and is believed to be related to the kinetics of oxygen precipitation and/or agglomeration [7,15]. There was little difference between various splits with the faster effective ramp rates, so we used the PDFL standard ramp rates (push/pull temperature of 800°C and temperature ramp rates of 5°C per minute) for all other experiments.

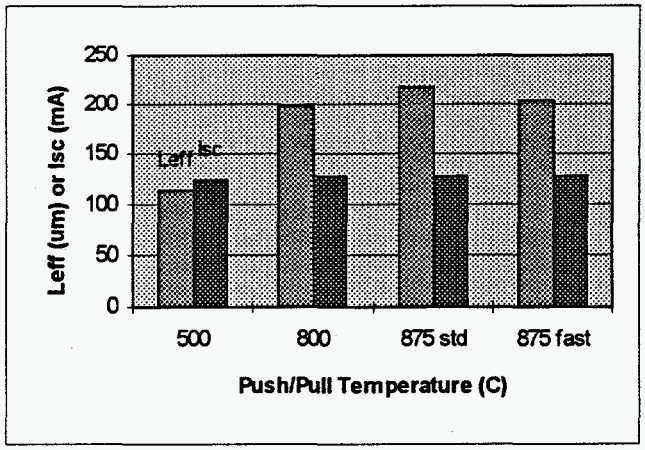

Fig. 2. Effect of push/pull temperature on effective diffusion length and on I_{sc} of 4-cm^2 planar cells. *Std.* and *fast* refer to speed of wafer insertion.

We next examined the effect of various surface preparation and phosphorus diffusion parameters on the bulk lifetime using a statistically based experimental design (Fig. 3). The PDFL $POCl_3$ diffusion process consists of a phosphorus-glass deposition step, an inert soak, and an oxygen soak; a wide variety of diffusion profiles can be obtained with this $POCl_3$ diffusion process [16]. The experiment examined the effect of six different parameters (material, texture etch time, isotropic etch time, inert soak time, oxygen soak time, and diffusion temperature) on PCD lifetime and on finished cell parameters (effective diffusion length -- L_{eff}, V_{oc}, J_{sc}, FF, and η). The most significant factors for PCD lifetime and cell performance were associated with the phosphorus diffusion; lower diffusion temperature, longer inert soaks, and shorter oxygen soaks were preferred for longer lifetime and better cell performance (Fig. 2). We performed a similar experiment using a statistically based

experimental design to examine the effect of various parameters (aluminum thickness, alloy time, and alloy temperature) associated with aluminum-alloy process. For this experiment, best cell performance was achieved with short high-temperature (15 minutes, 1000°C) alloys or with long low-temperature (12 hour, 800°C) alloys.

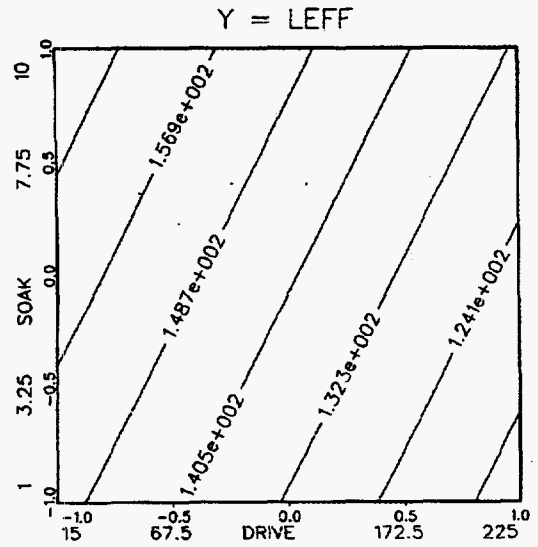

Fig. 3. Sample of an experiment that examined the effect of six different $POCl_3$ diffusion and surface preparation parameters on material quality and cell performance using a statistical experimental design. *Soak* and *Drive* refer to inert and oxygen soak times (minutes) of $POCl_3$ diffusion process, respectively. Contours are the effective diffusion length (L_{eff}) in μm, and the 95% confidence interval is around 16 μm.

Important observations from these experiments include the following [9]:

- Textured and planar surfaces produce similar bulk lifetimes.
- It is difficult to maintain bulk lifetime through an oxidation. For example, lifetime is improved during the inert soak in our $POCl_3$ diffusion process while there is further phosphorus diffusion, but is degraded during the *in situ* oxidation when further phosphorus incorporation from the phosphorus diffusion glass is ceased (Fig. 3). We have also observed lifetime degradation due to *ex situ* post-diffusion oxidations; this lifetime degradation did not occur when aluminum was present on the back surface during the oxidation [17].
- Aluminum alloys have much wider process latitude compared to phosphorus diffusions, and can be performed at temperatures up to 1000°C with no lifetime degradation.
- It was highly beneficial to have a gettering agent (phosphorus or aluminum) present during high-temperature steps to avoid bulk lifetime degradation.

The results from these experiments collectively suggest that impurities or microdefects are gettered by heavy phosphorus diffusions, but are re-released during a subsequent oxidation. This observation is potentially very important because there are several steps with temperatures above 700°C after the phosphorus diffusion in most commercial fabrication sequences.

CELL RESULTS

The results of the process optimization were used to fabricate high-efficiency cells. Besides the process evaluation

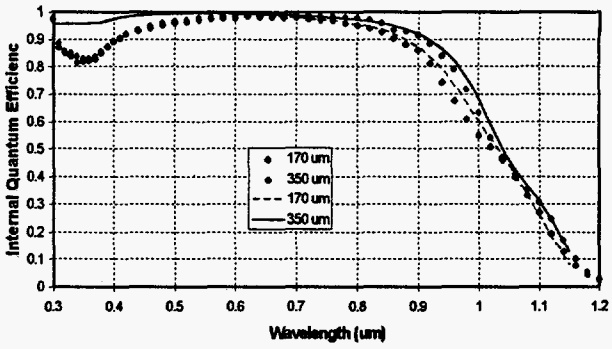

Fig. 4. Model fit (lines) and measured data (points) for cells using photovoltaic-grade Cz silicon. See Table 1 for details of the model.

Table 1. Comparison of measured and modeled data for 4-cm^2 cells with two substrate thicknesses. The model fit used a bulk resistivity of 1 Ωcm, a bulk lifetime of 36 μs, and a back-surface recombination velocity of 10,000 cm/s. These particular cells have a very thin aluminum-alloyed back-surface field. The model calculations used a numerical device simulator (PC1D [18]).

Cell ID (Thickness)	Parameter	Eff %	V_{oc} volts	FF	J_{sc} mA/cm^2
19-4D	Measured	16.9	0.613	0.795	34.6
(350 μm)	Modeled	17.1	0.615	0.805	34.6
19-2C	Measured	16.2	0.605	0.794	33.8
(170 μm)	Modeled	16.4	0.605	0.804	33.7

described previously, we used extensive device modeling to help guide our cell development. In an early experiment, we fabricated cells on two different thicknesses to help model our cells and determine areas of research to emphasize. Detailed analysis of the spectral and current-voltage data found that these cells were limited by recombination in the base (Fig. 4 and Table 1). Base recombination has components due to bulk and to back-surface recombination. Approximately 80% of the base recombination at open circuit occurred at the back surface for the thin (170 μm) cell! Improvements in performance therefore require novel back surfaces to reduce back-surface recombination.

Several high-efficiency device structures were examined, including aluminum-alloyed back-surface field (BSF), boron-doped BSF, and emitter wrap-through (EWT) cells [9]. Details of the work are presented in Ref. 9. Some of the highlights of this work include the following:

- Efficiencies of 18.3% (V_{oc} of 634 mV, J_{sc} of 35.9 mA/cm^2, FF of 0.803, and f_g of 2.9%) and 17.6% (V_{oc} of 617 mV, J_{sc} of 35.5 mA/cm^2, FF of 0.806, and f_g of 6.7%) were demonstrated for moderate- and large-area (4.6- and 42-cm^2) cells with aluminum-alloyed BSF's, respectively. 21-out-of-23 large-area cells had efficiencies above 17%, and the overall average for the large-area aluminum-alloyed cells was 17.25 ± 0.25%. Cell performance was limited by recombination at the back surface due to the relatively high S values (around 1000 cm/s) of aluminum-alloyed BSF's using furnace anneals of evaporated aluminum films. In separate experiments, we determined that Al-alloyed BSF's using paste aluminum had S values as low as 200 cm/s.

- Back-surface recombination velocity of around 350 cm/s was demonstrated with a boron-doped BSF using a boron-phosphorus codiffusion process. Cell performance was limited by degradation of bulk lifetime, which is only partially related to the higher diffusion temperatures. Average for 12 large-area boron-doped BSF cells was 14.1 ± 1.1%.
- A 42-cm^2 bifacial-contact EWT cell was demonstrated with an efficiency of 15.7% (V_{oc} of 613 mV, J_{sc} of 34.9 mA/cm^2, FF of 0.731, and f_g of 6.2%) using photovoltaic-grade Cz material. Cell performance was limited by a high series resistance, which is related to a non-optimal base contact geometry.

The ultimate performance potential of photovoltaic-grade Cz silicon was projected based on the material evaluation and advanced device development tasks in this project. The excellent match of model and experimental results (Table 1 and Fig. 4) gives us confidence in the validity of the projections. Two types of devices were considered: thin BSF cells and EWT cells. The calculations used the following parameters: a bulk lifetime of 75 μs, a bulk resistivity of 1 Ωcm, a series resistance of 0.5 Ωcm^2, a well-passivated emitter (N_s=3•10^{19} cm^{-3}, sheet resistance of 108 Ω/□, junction depth of 550 nm, and surface recombination velocity of 5000 cm/s), a solar-weighted extrinsic reflectance of 5%, an internal back-surface reflectance of 90%, and an internal front-surface reflectance of 92%. These values are considered appropriate, if aggressive, targets for advanced c-Si cells. PC1D was used for the calculations (Fig. 5) [18]. Efficiencies of 20% are projected for thin cells with excellent BSF's (S<300 cm/s), or for EWT cells for nearly all the thicknesses considered. Because the best BSF demonstrated to date only has an S around 300 cm/s, the EWT cell has about 0.5% absolute higher efficiency potential compared to thin BSF cells. The superior projected performance of the EWT cell is due to (1) a high V_{oc} that is roughly equivalent to a BSF cell with an S of 100 cm/s, and (2) a J_{sc} that is higher than any of the BSF cells.

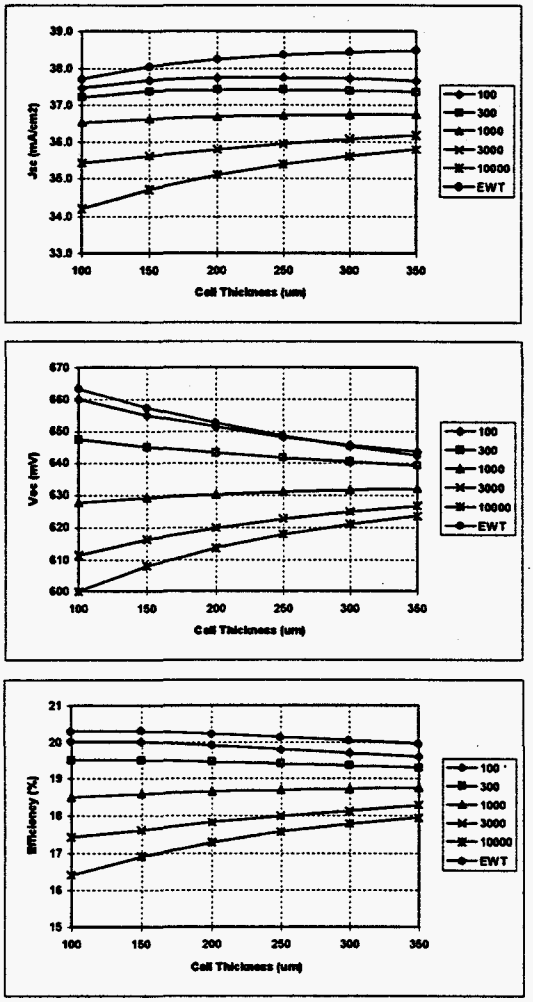

Fig. 5. Projected performance of optimized cells using photovoltaic-grade Cz silicon. Legend is back-surface recombination velocity in cm/s.

CONCLUSIONS

This paper presented a brief summary of a detailed process and device development study using photovoltaic-grade Cz silicon [9]. Photovoltaic-grade silicon requires a different process and device optimization compared to semiconductor-grade c-Si materials. With proper optimization, we project efficiencies of up to 20% are possible for photovoltaic-grade Cz silicon.

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