SAND 96-2511C

Presented at the 6th *International Workshop on Moisture in Microelectronics*, Oct. 15-17, 1996, Gaithersburg, MD.

SAND--96-2511C
CONF-9610143--2

POROUS SI STRUCTURE AS MOISTURE SENSOR†

D.W. PETERSON*, L.T. NGUYEN**
*Sandia National Laboratories, P.O. Box 5800, M/S 1082, Albuquerque, NM, 87185-1082
**National Semiconductor Corporation, 3875 Kifer Rd, M/S 19-100, Santa Clara, CA, 95051

ABSTRACT

Development and characterization of a capacitive moisture sensor made from porous Si is presented. The sensor development was in support of the DoD funded Plastic Package Availability program and was intended for the detection of pinholes and defects in moisture barrier coatings applied to ICs during fabrication or during the plastic encapsulation assembly process.

INTRODUCTION

Interest in non-hermetic IC (integrated circuit) packaging on the part of the DoD and DOE has resulted in a number of studies of moisture induced IC failure mechanisms. The recently completed DoD funded Plastic Package Availability (PPA) program was aimed at providing a better understanding for the potential use of plastic encapsulated microcircuits (PEMs) in military systems. The principle objective of the PPA program was to provide the data necessary for the DoD to revise its specification concerning the use of plastic ICs in military systems. To this end, National Semiconductor assembled a team consisting of Dow Corning, Honeywell, Plaskon Electronic Materials, and Sandia National Laboratory. Each team member made contributions based on their own area of unique expertise. Honeywell reported on system considerations for the replacement of hermetic with plastic ICs based on field experience with commercial products. Plaskon reviewed current commercial state-of-the-art materials and processes and developed a preliminary specification for military-grade epoxy molding compounds. Dow Corning demonstrated improvements in reliability of plastic packaged ICs through the use of a proprietary ceramic moisture barrier die coat technology. The role of Sandia National Laboratory in this program was development of a moisture and corrosion test chip that could be used to validate and possibly even qualify the materials and processes generated by the other team members. This paper describes the development and characterization of the porous Si moisture sensor part of this test chip.

THEORY

The NAT-01 test chip is comprised of a moisture sensor and a corrosion detector. The corrosion detector is a conventional triple track corrosion structure similar to that used in previous ATCs (Assembly Test Chips) designed and built by Sandia. In this application, the moisture sensor is required to detect pinholes or defects in a moisture barrier coating and withstand processing temperatures of 300 °C for at least 4 hours. A capacitive sensor using a porous Si (PS) dielectric was selected to meet these requirements. PS is formed during the anodization of doped Si in a bath of hydrofluoric acid (HF). The density of PS can vary from 20–80% that of bulk Si. PS retains the crystalline structure of the starting material and has specific surface areas that can range between 40 and 400 m^2/g[1]. The porous microstructure depends largely on the dopant type and concentration of the starting wafer. PS films formed in *n*-type Si have columnar, non-connected pores similar in structure to Al_2O_3 porous films. PS films in *p*-type Si substrates contain finer pores with diameters in the 100 Å range. Lightly doped *p*-type Si substrates (< 1 Ω-cm), in particular, develop *interconnected* pores in a sponge-like matrix capable of supporting lateral (in-plane) diffusion or moisture. This characteristic is considered key to pinhole detection.

† This work was supported by the United States Department of Energy under Contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

MASTER

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

Anodization Process: The formation of PS through anodic etching of Si is illustrated in Fig. 1. The Beale[2] theory assumes the Fermi level is pinned at mid-gap, much like a Schottky barrier diode. Charge flows across the Schottky barrier by thermionic emission in lightly doped *p*-type Si substrates. Current flows preferentially down the electrolyte path of least resistance, concentrating at the pore tips due to local field enhancement. Local field enhancement is greatest during the onset of pore growth when the radius is smallest and decreases with time. The current flux at the a pore tip dissolves Si and "grows" the pore along the current path. The orientation of a given pore tip and its subsequent growth direction can vary from normal to the surface to perpendicular to the surface. The "off normal" pores eventually intercept other pores creating the interconnected pore morphology common to lightly doped *p*-type PS.

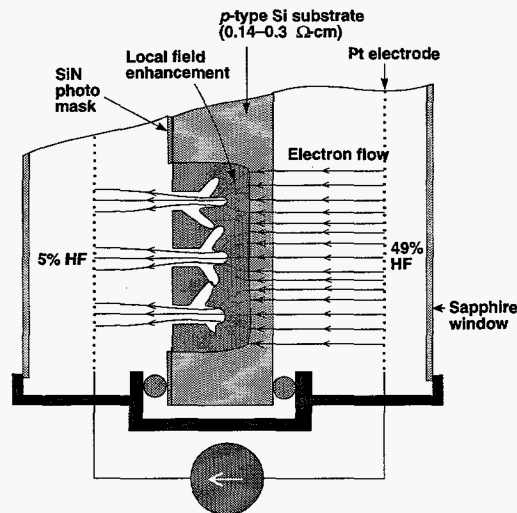

Fig. 1. Beale model for porous film formation in Si. The backside ohmic contact is achieved with a Pt electrode in a wet chemical cell using a 49% HF electrolyte solution.

The anodization process is carried out in a double-tank electrochemical cell, where both sides of the wafer are in contact with HF[3]. The cell is constructed of high density polyethylene with sapphire windows at each end to facilitate front and backside illumination with external light sources for carrier generation. A liquid-tight seal is obtained with a cam-type lever which compresses O-rings fitted in each half-cell against the wafer. The half-cells are cylindrical cavities; thus, the electrolyte volumes between the wafer and the two Pt mesh electrodes have the same cross-section as the exposed region of the wafer. This geometry minimizes current crowding at the wafer edge and optimizes the primary current distribution. Anodization parameters used for the NAT-01 sensors are 5 mA/cm^2 for 252 s in 5% HF by weight on 0.14 – 0.3 Ω-cm *p*-type 152 mm Si wafers. This process nominally results in a 0.9 μm film of 80% porosity.

Process optimization: Previous work successfully demonstrated lateral diffusion and pinhole detection in lightly doped PS films and led to the design and fabrication of a simple Al grid test chip to be used in process development. The test chip, shown in Fig. 2, contains four Al grid PS capacitors of varying surface area, each with 5μm wide lines and spaces. The chip was used to optimize the interlevel dielectric and passivation etch steps over PS films. After some experimentation, it was determined that a 1200 Å film of TEOS (Tetraethylorthosilicate – a low temperature decomposition resulting in SiO_2) could be used to protect the PS layer during subsequent processing steps and would also act as an etch stop during the final passivation plasma etch. The film also corrected a problem with delamination of fine line Al conductors during DI (deionized) water rinse cycles by enhancing the adhesion between the PS and Al layers.

Besides process optimization, the Al grid test chip was used to demonstrate pinhole detection. Wafers were passivated using a number of inorganic barrier coatings including 7 kÅ of PECVD SiN (Si_3N_4 NH_3 - based plasma

enhanced low temperature SiN typically used for chip passivation). The results of a wafer level diffusion experiment are shown in Fig. 3, where all 300 of the 2.54 mm square PS sensors on a SiN passivated wafer were measured using an LCR meter before and after a 12 h soak in DI water. The graph shows the ratio of C/C_0 as a function of sensor location. A ratio of 1 signifies a "non-leaker" and ratios of greater than 1 represent "leakers" where the magnitude of the ratio is functionally dependent on the diffusion rate and therefore also on the defect cross-section. The sensors are sealed during the SiN CVD (chemical vapor deposition) process in a vacuum devoid of moisture, so the capacitance measurements of the non-leakers represent a "dry" capacitance. Leakers respond not only to the highly concentrated moisture source present during DI water immersion, but also to the partial pressure of water vapor in the room ambient (~ 35% RH in our facility). Therefore, a leaker will eventually reveal itself even during storage in ambient conditions.

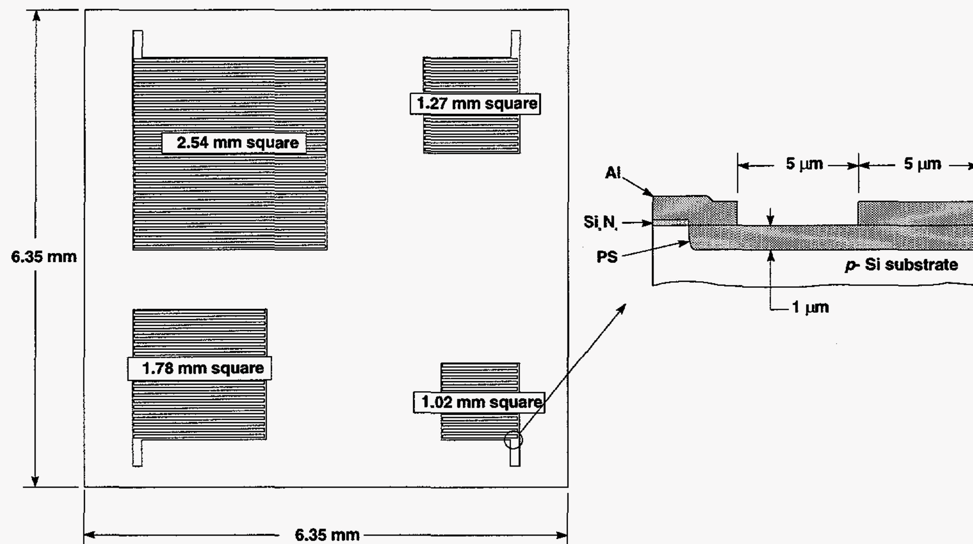

Fig. 2. Porous Si technology demonstration test chip. This chip was used in a number of experiments to demonstrate pinhole or defect detection and optimize the fabrication process of an Al grid device fully compatible with standard CMOS processing.

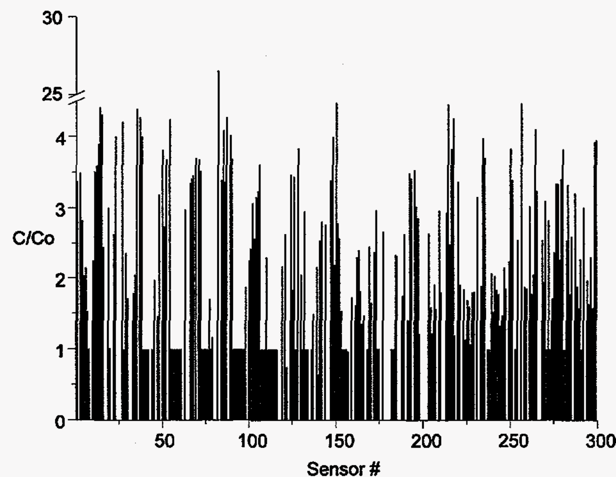

Fig. 3. Wafer level pinhole detection experiment using the test chip shown in Fig. 2 coated with 7 kÅ of PECVD Si_3N_4. Capacitance readings were taken before (C_0) and after (C) a 12 h soak in deionized water on each of the 2.54 mm square sensors. Total surface area represented by the 300 sensors ~ 11%. Measurements greater than 1 indicate leakers.

Test chip layout: For the final design, a 2 μm minimum feature size was chosen for the Al grid electrode covering the PS sensors. Corrosion triple tracks were laid out using the same design rules. The layout maximizes the surface area of four sensing regions within the space available in a 2.54 mm design area after allowing for a perimeter string of 120 μm bondpads. Two of the sensors are Al triple track corrosion structures, one passivated with PECVD SiN and the other unpassivated. The other two sensors have the same layout except that the triple tracks are tied together at the end to form the upper electrode of a PS capacitor MS (moisture sensor). Unused bondpads are connected to the substrate, which serves as the lower electrode of the PS capacitors. This layout is shown in Fig. 4.

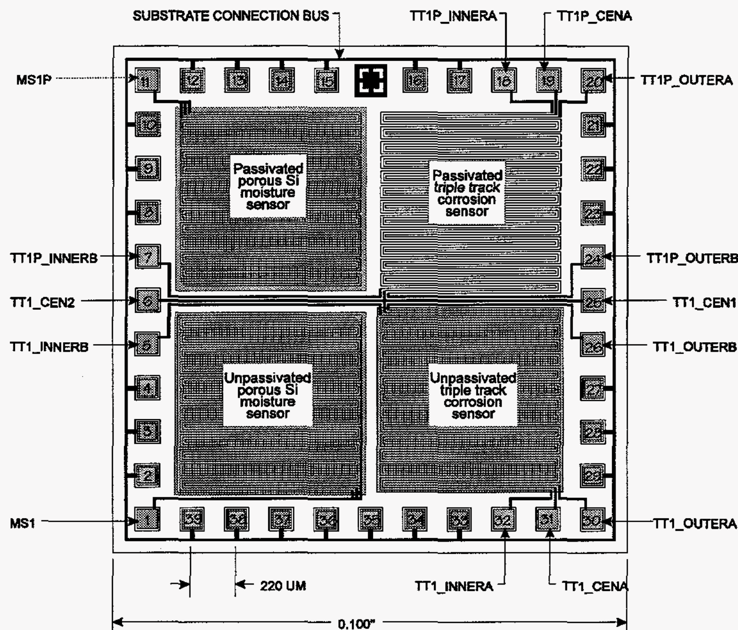

Fig. 4. Layout for the NAT-01 moisture and corrosion test chip. Al triple tracks are 2 μm wide lines and spaces and each of the four sensing regions are ~ 1 mm square.

Process Steps: The fabrication flow of NAT-01 is shown in Fig. 5. Starting material is 0.14 – 0.30 Ω-cm *p*-type [100] Si wafers. A 1400 Å high temperature densified SiN layer is deposited and patterned photolithographically to form the anodization mask. High temperature SiN has a relatively slow etch rate in the HF anodization bath. The anodization process is carried out in a two-sided electrochemical cell, as described earlier. After anodization, the PS layer is protected during subsequent processing with 1200Å of TEOS, which also acts to prevent backetching and delamination of the Al metal grid during later processing. The *p*+ substrate contacts are implanted and annealed. Al is deposited and plasma etched. The TEOS layer protecting the PS acts as an etch stop during this step. The remaining TEOS between the Al grid lines is removed. The final step is deposition and etch of 7 kÅ PECVD SiN for chip passivation.

RESULTS

Changes in the concentration of vapor phase moisture at the chip surface are detected by measuring the change of capacitance across the moisture sensitive PS dielectric using a common LCR or capacitance meter before and after exposure to a moisture source. Typical "dry" capacitance readings for both MSs are ~25 pF at 1 kHz using a 1 V signal. Readings are often normalized by calculating fractional changes in capacitance, $(C-C_0)/C_0$. The passivated MS should not exhibit measurable changes in capacitance at room temperature after the initial post-fabrication readings as long as the SiN passivation film remains intact. The intrinsic sensitivity of the passivated MS is greater than the unpassivated MS because it is protected during and after the fabrication process from exposure to organic contaminates. Contaminates on the pore walls can significantly affect hydrophilicity of the surfaces. Experimental measurements show order of magnitude differences in sensitivity.

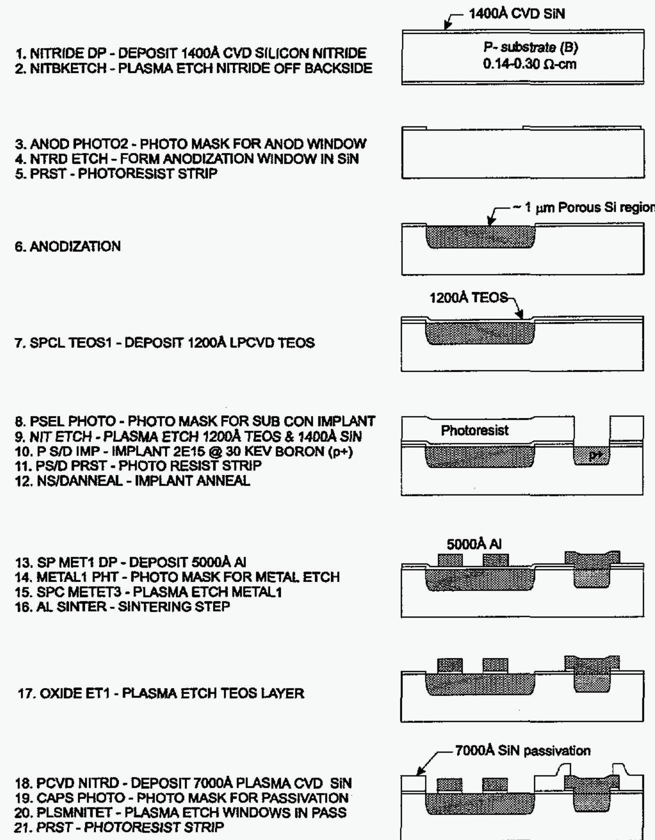

Fig. 5. Processing flow for NAT-01 test chip.

Fig. 6 illustrates four experimental conditions possible with the two moisture sensors in a molded package. The first case is for the *unpassivated* MS. The permeability of the epoxy molding compound (or glob-top) to vapor phase moisture is estimated by measuring the change in capacitance as a function of time of a previously dried out part during exposure to a known moisture concentration at a controlled temperature. Changes in weight corrected for non-absorptive package components (lead frames, die) are also recorded. This process is carried out until both measurements indicate the package has reached equilibrium conditions with the external moisture source. Using the gravimetric data, a diffusion coefficient can be obtained from the linear part of a plot of mass uptake, M_t, against root time using Eq. (1)[4].

$$\frac{M_t}{M_\infty} = \frac{4}{l}\left(\frac{Dt}{\pi}\right)^{1/2} \tag{1}$$

Solving Eq.(1) for the diffusion constant in terms of the slope, the diffusion coefficient is calculated by,

$$D = \pi\left(\frac{kl}{4M_\infty}\right)^2 \tag{2}$$

where k is the slope of the linear portion of the plot of M_t vs. $t^{1/2}$.

It should be noted that Eqs. (1) and (2) assume Case I ("Fickian") diffusion in the polymer. Fickian diffusion is characterized by sorption and desorption curves with initial parabolic time dependency. This is generally the case with epoxy molding compounds, but estimates of the diffusion coefficient based on experimental weight gain measurements assume one-dimensional penetration along two surfaces, and thus are done on thin strips of material. A molded part will have edge effects that can possibly skew the M_t vs. $t^{1/2}$ curve such that it is not linear in the initial stage of diffusion. The fractional change in capacitance of the unpassivated MS will reflect the moisture flux at the chip surface during the diffusion process.

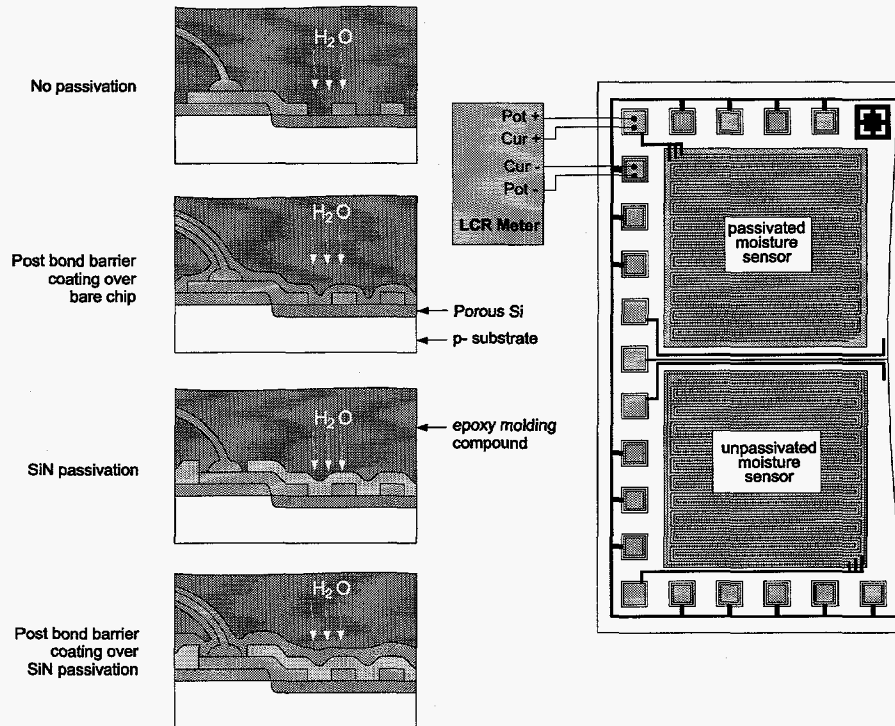

Fig. 6. Test set-up and possible experimental conditions for the NAT-01 porous Si MS (moisture sensor).

The second experimental condition uses the unpassivated MS coated with a post bond moisture barrier coating, as shown in Fig. 6. These coatings are normally applied in a vacuum using a plasma CVD process, and therefore a sensor protected with a defect free coating would be expected to exhibit "dry" capacitance readings of ~25 pF at all times. If there is variation from this measurement, particularly as a function of time, it could be concluded that a defect exists in the coating. The rate of change in capacitance of an unencapsulated sensor during exposure to a step change in ambient moisture concentration is related to defect characteristics, such as cross-section, crack vs. pinhole, etc. Assuming that "non-leakers" were encapsulated with epoxy molding compound or liquid encapsulant, subsequent changes in capacitance from the baseline would indicate packaging-related damage to the post bond barrier coating. Exposure of encapsulated parts to extremely high moisture concentrations in a HAST or pressure cooker system would help accelerate the detection of small defects with low effective diffusion rates.

The third and fourth experimental conditions illustrated in Fig. 6 involve the *passivated* MS with and without a post bond barrier coating. The former is a measure of the protective properties of the SiN passivation film applied during fabrication of the sensor, and the latter reflects the combined protection offered by both coatings. HAST or pressure cooker tests would aid in rapid isolation of leakers. At the onset of his program, the Dow Corning post bond barrier coating (SPEC) was to be evaluated using the MS, however, this was not possible due to programmatic difficulties. The MS characterization results described in following paragraphs are based on the Sandia SiN passivation acting as

a moisture barrier. This coating has not been optimized for moisture protection and offers a rich variety of defects suitable for detection.

High Temperature Performance: A series of experiments were performed to determine the sensitivity of the NAT-01 MS to elevated temperature cycles in various ambients. The original requirement was the need for the MS to survive the Dow Corning post bond moisture barrier coating process, which had a cure schedule that reached 275 °C. The high temperature exposure used air, N_2, and vacuum ambients. Results from the vacuum test are shown in Fig. 7. The unpassivated MS decayed approximately 35% for air, 30% for N_2, and 28% for vacuum ambients, respectively, after temperature exposure and ambient storage. The experiment demonstrated that the MS can survive high temperature exposures for extended periods of time without loss of functionality.

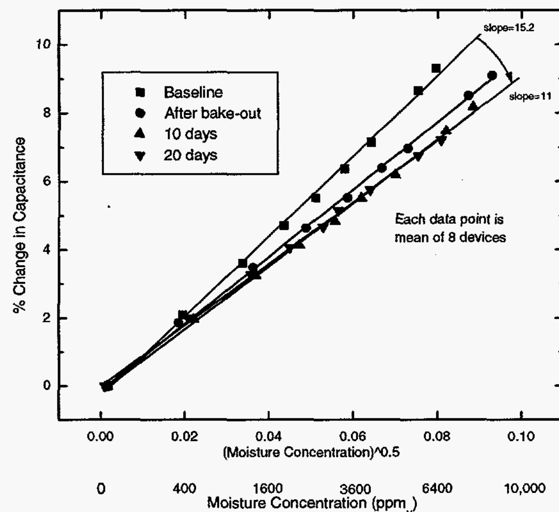

Fig. 7. NAT-01 *unpassivated* MS calibration data after exposure to vacuum at 300 °C for 4 h. Plot is in % change of capacitance vs. square root of moisture concentration. Lower legend is in ppm_v for reference.

Moisture Diffusion Experiments: The purpose here was to demonstrate the use of the passivated and unpassivated MS during conditions of package dry-out and moisture ingress. The dry-out condition was 100 °C at 10^{-4} Torr. Moisture ingress experiments were performed using a Thunder Scientific Model 2500 humidity generator at 50 °C and 85% RH (~118,000 ppm_v). Results for this experiment are shown in Fig. 8 for a group of NAT-01 test chips molded in 14-lead DIPs (dual in-line packages) using Plaskon 3400 epoxy molding compound. The unpassivated MS data track the ambient moisture concentration, and the passivated MS data split into two apparent groups. One group roughly tracks the ambient humidity, suggesting defects or pinholes in the passivation, while the other group is essentially unaffected, with a gradual trend toward increasing readings. The latter could be due to changes in fringe field capacitance due to moisture build-up on the molding compound side of the passivation.

Moisture ingress was also monitored during HAST conditions using NAT-01 test chips molded in 68-lead PLCCs (plastic leadless chip carriers) with Plaskon ULS12H and ULS12H-X ultra-low stress molding compounds (-X containing ionic getters). A control group of hermetically sealed 68-lead CQJP (ceramic quad J-bend) parts were also included. The *unpassivated* MSs were measured before and at predetermined off-line intervals during HAST at 159 °C and 85% RH. These data are shown in Fig. 9 plotted as fractional changes in capacitance vs. time. The first off-line measurement interval was at 20 h, and it can be seen that the unpassivated MS data indicate a state of equilibrium moisture concentration at the chip. The ceramic control parts were non-responsive with the exception of one leaker. At approximately 200 h, the response of some of the MSs dropped off toward negative fractional changes. The capacitance readings of these parts ranged from 7 pF to 15 pF (open circuit readings). Failure analysis results showed that the Al electrodes in these devices had decomposed due to corrosion. This occurred only on the ULS12H parts. The ULS12H-X parts containing ionic getters remained functional throughout the HAST experiment.

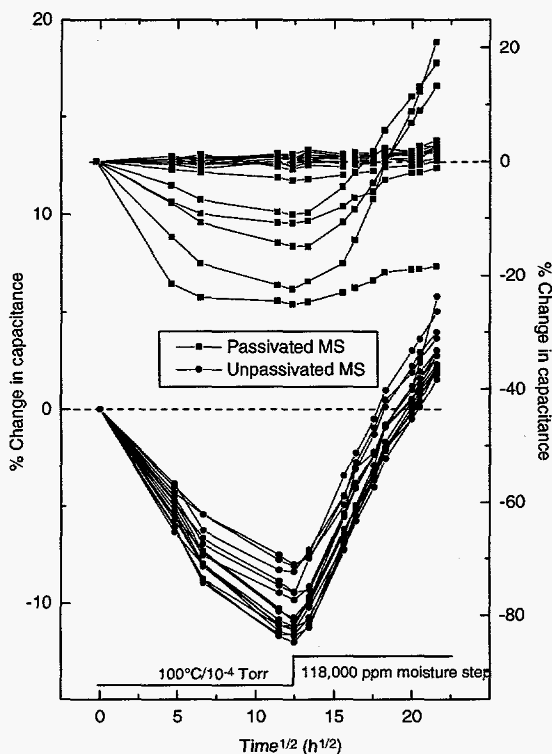

Fig. 8. MS response as a function of time during dry/wet cycle of NAT-01 parts encapsulated in 14-lead DIPs. Passivated sensors (filled square - right ordinate) show two trends: "leakers" that appear to follow the swing in ambient moisture concentration, and "non-leakers" that are relatively unresponsive. Unpassivated sensors (filled circle - left ordinate) track the swing in ambient moisture concentration.

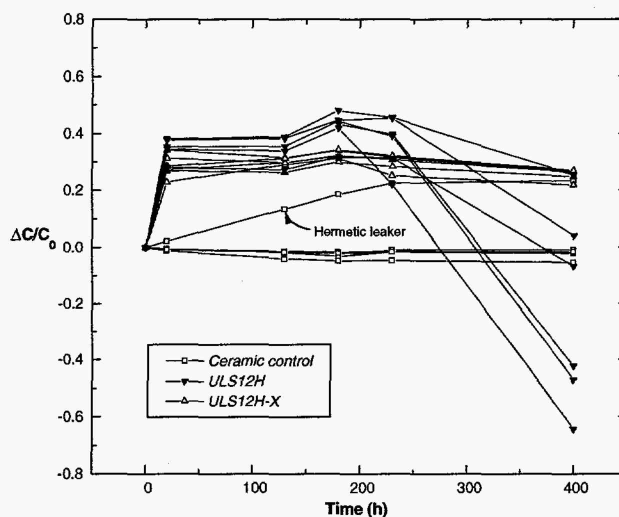

Fig. 9. NAT-01 *unpassivated* MS response during HAST at 159 °C and 85% RH. Two groups were molded in 68-lead PLCCs using Plaskon ultra-low stress compounds ULS12H (filled triangle) and ULS12H-X (open triangle), and a control group (open square) was packaged in 68-lead CQJPs. Plot is fractional change in capacitance as a function of time. One "leaker" is evident in the control group. The drop-off in response of some of the molded parts is due to corrosion of the Al electrode.

Moisture Penetration Though Passivation Experiments: The capacitive responses of the passivated MS in HAST fall into two groups: non-leakers with essentially straight line response, and leakers with very high readings at the first off-line measurement interval followed by a drop off to open circuit readings between 100 h and 200 h. (Refer to Fig. 10) Failure analysis indicated the drop off was associated with corrosion of the Al grid. HAST conditions were 159 °C and 85% RH.

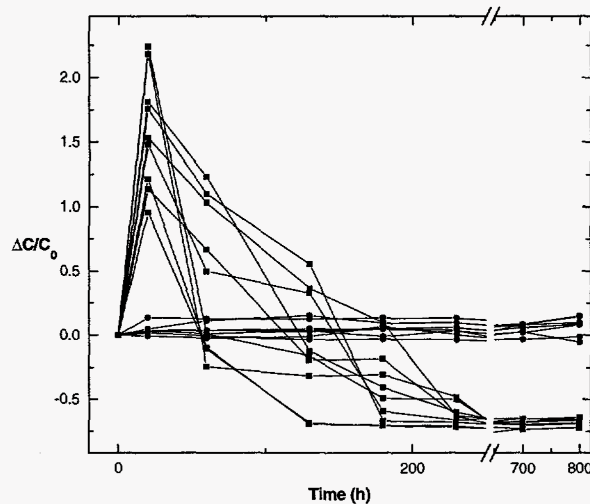

Fig. 10. NAT-01 *passivated* MS response during HAST at 159 °C and 85% RH. Devices were molded in 14-lead DIPs using different Plaskon molding compounds. Plot is fractional change in capacitance as a function of time. Data are grouped by devices showing leaks (filled square) and devices showing no leaks (filled circle) irrespective of molding compound. First measurement is at 20 h. (Note break in time axis.)

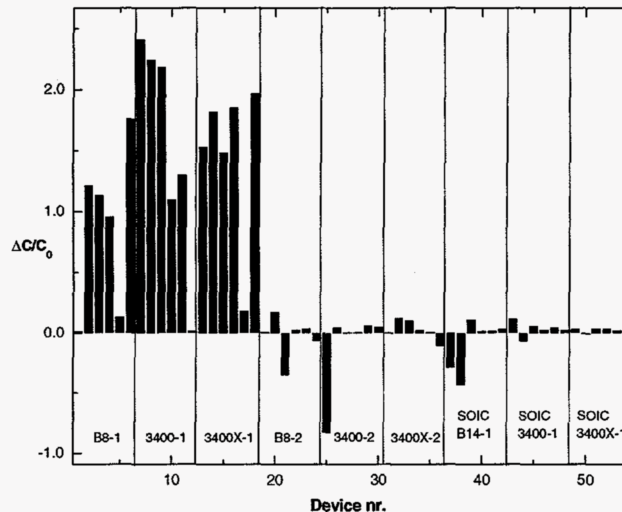

Fig. 11. NAT-01 MS response of *passivated* sensors at first (20 h) off-line measurement interval during HAST at 159 °C and 85% RH. Each bar represents fractional change in capacitance of an individual part molded in a 14-lead DIP, unless specified as SOIC, using the Plaskon molding compound indicated at the bottom. The parts are further divided into "not preconditioned" (-1), and "preconditioned" (-2).

Fig. 11 shows the *passivated* MS response across all of the molding compounds at the first measurement interval (20 h). Groups annotated with a -2 were preconditioned by National Semiconductor prior to shipping to Sandia for further testing. Preconditioning simulates worst-case surface mount operations through a series of temperature cycles and moisture exposure followed by two simulated vapor phase reflow temperature profiles. In this plot, small bars mean passivation layer with little or no moisture leak rate. Negative responses could possibly be due to Al grid corrosion, suggesting leaks through the passivation layer. The preconditioned group underwent thermal cycles and thermal shock that would potentially damage the passivation layer, and it would seem likely that they would exhibit more and bigger leaks than the non-preconditioned parts. However, the data show early failures mostly in the non-preconditioned parts.

CONCLUSIONS

A porous Si moisture sensor was developed for the purpose of evaluating CVD moisture barrier coatings for IC protection. Sensitivity to pinholes, or "point" moisture sources, was demonstrated, along with robustness to elevated temperatures associated with CVD processes. Experimental data were taken during a range of environmental test conditions from room temperature at 35% RH to 159 °C at 85% RH on both passivated and unpassivated MSs molded in several package configurations using a number of special molding compounds made by Plaskon. These data show that the unpassivated MS can be used for moisture diffusion measurements and the passivated MS is effective in detecting defects in PECVD SiN protective coatings. Although not demonstrated in this work, it is logical to assume that post fabrication or post bond protective coatings could be similarly evaluated using the unpassivated MS.

REFERENCES

[1] T. R. Guilinger, M. J. Kelly, and S. S. Tsao in *Silicon-on-Insulator and Buried Metals in Semiconductors*, edited by J. C. Sturm, C. K. Chen, L. Pfeiffer, and P. L. F. Hemment, Material Research Society Proceedings **107**, 455-458 (1988).

[2] M. I. Beale, J. D. Benjamin, M. J. Uren, N. G. Chew, A. G. Cullis, "An Experimental and Theoretical Study of the Formation and Microstructure of Porous Silicon," *J. Crystal Growth*, **73**, 622 (1985).

[3] M. J. Kelly, R. R. Guilinger, V. E. Granstaff, D. W. Peterson, J. N. Sweet, and M. R. Tuck, *in Proceedings of the Symposium on Electrochemical Microfabrication*, 180th Meeting of Electrochemical Society, edited by M. Datta, K. Sheppard, and D. Snyder, Phoenix, AZ, (1991).

[4] M. T. Goosey, "Permeability of Coatings and Encapsulants for Electronic and Optoelectronic Devices," in *Polymer Permeability*, edited by J. Comyn, Elsevier Applied Science Publishers, New York, (1985).