CONF-961040--4 SAND96-2006C SAND--96-2006C

COMPLEMENTARY HFET TECHNOLOGY FOR WIRELESS DIGITAL AND MICROWAVE APPLICATIONS

A. G. Baca, J. C. Zolper, D. F. Dubbert, V. M. Hietala, L. R. Sloan, R. J. Shul, M. E. Sherwin,* and M. J. Hafich
Sandia National Laboratories, P. O. Box 5800, Albuquerque, NM 87185-0603
*present address: Microwave Signal, 22300 COMSAT Drive, Clarksburg, MD 20871

Development of a complementary heterostructure field effect transistor (CHFET) technology for low-power, mixed-mode digital-microwave applications is presented. The digital CHFET technology with independently optimizable transistors has been shown to operate with 319 ps loaded gate delays at 8.9 fJ. The power consumption of this technology is dominated by leakage currents of the p-channel FET, while performance is primarily determined by the characteristics of 0.7 µm gate length devices. As a microwave technology, the nJFET forms the basis of low-power circuitry without any modification to the digital process. Narrow band amplification with a 0.7 x 100 µm nJFET has been demonstrated at 2.1-2.4 GHz with gains of 8-10 dB at 1 mW power. These amplifiers showed a minimum noise figure of 2.5 dB. Next generation CHFET transistors with sub 0.5 µm gate lengths have also been developed. Cutoff frequencies, f_t of 49 GHz and 11.5 GHz were achieved for n- and p-channel FETs with 0.3 and 0.4 µm gates, respectively. These FETs will enable enhancements in both digital and microwave circuits.

RECEIVED
AUG 15 1996
OSTI

INTRODUCTION

Portable electronics provides a large driving force for low power electronic components and continued miniaturization of systems. GaAs complementary logic, known as CHFET when heterostructure field effect transistors are employed, offers the potential for greatly reducing the power consumption of digital integrated circuits while offering high performance [1-6]. Power consumption of complementary logic circuits is much lower than other digital logic families because they consume very little static power. Dynamic power consumption becomes an important concern for high speed circuits because of the relation $P_d = C_L(V_{DD})^2f$, where P_d is the dynamic power, C_L is the load capacitance, V_{DD} is the power supply voltage, and f is the frequency. An important consideration of all complementary logic technology is that dynamic power is reduced dramatically at lower power supply voltages. The performance of FETs that work well at higher voltages (3-5 V) can degrade as the power supply voltages drop. Therefore technology development of smaller gate length FETs is required to maintain performance at lower supply voltages. At these lower power supply voltages, compound semiconductor FETs still achieve acceptable performance at reasonable gate lengths because of superior electron transport properties, whereas CMOS technology is driven towards very small gate lengths that are even sub 0.1 µm [7]. At the present time leakage currents in compound semiconductor CHFET technology are not as low as CMOS and preclude its use where VLSI technology is required because they result in high static power consumption. The current niche for CHFET technology is medium size circuits with high speed and low power consumption, especially if radiation hardness is required.

On the other hand, low-power microwave technology is increasingly important for wireless applications. Because there is no fundamental circuit approach to reduce power consumption of microwave technology, device biasing and device size are the main approaches to lower operating power and this usually results in some sacrifice in performance [8]. When circuits are biased for low power consumption, the devices may

To be published in a proceedings volume of the Fall 1996 Electrochemical Society Meeting

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED
MASTER

not be fully turned on and do not operate at maximum gain. Intrinsically high gain devices such as GaAs FETs have margin to sacrifice some gain at lower frequencies, in addition to other commonly cited microwave advantages of low noise and semi-insulating substrates suitable for low loss monolithic integration.

In this work, we present compatible low power digital and microwave GaAs-based technology suitable for mixed-mode applications where low power, high speed, and system miniaturization are desired. Monolithic integration of digital and microwave functions is generally desirable for performance enhancement, increased reliability, and cost reduction in packaging and system assembly. Applications such as electronic tags can benefit from low power and system miniaturization, especially at higher frequencies, where the antennas can be made smaller.

A complementary logic digital technology with self-aligned JFETs has been described previously [9] and will be briefly reviewed. Then the same digital n-channel JFET is characterized for low-power microwave operation and is demonstrated in a hybrid microwave circuit. A complete integrated process for monolithic digital and microwave circuits is presented. Finally, higher performance n- and p-channel FETs with shorter gate lengths are demonstrated. These devices form the basis for future technology improvements.

TECHNOLOGY DESCRIPTION

The GaAs complementary logic technology integrates an epitaxial design, p-channel HFET and a fully ion implanted n-channel JFET [9], as illustrated in Fig. 1. This approach permits the independent optimization of the p- and n-channel devices, including the ability to independently set threshold voltages. An all-implanted self-aligned n-channel GaAs JFET allows any epitaxial pHFET design that is process compatible with the nJFET, particularly regarding the high temperature annealing required. In this way pHFET designs other than the HIGFET can be employed for high performance. Since pHFET performance is approximately 6-8 times worse than nFET performance, even incremental improvements in pHFET design are worthwhile. In our approach, epitaxial doping, material composition, and layer design can all be varied to optimize the p-channel device, since none of these

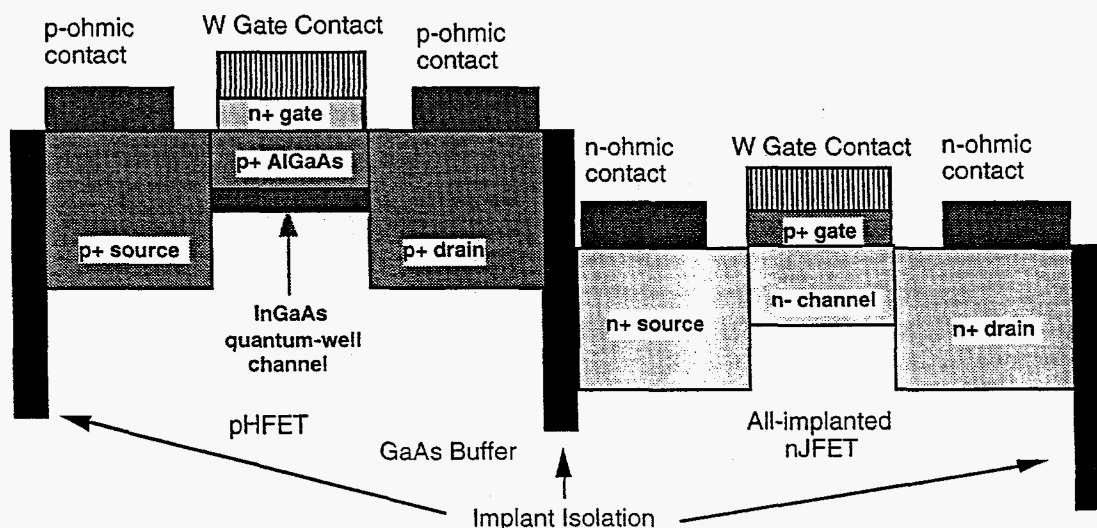

Figure 1. *Schematic device cross sections of the first generation complementary nJFET and pHFET devices. These devices are independently optimizable.*

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

layers will be shared with the n-channel device. A drawback of this approach is that n-channel performance will be sacrificed relative to n-channel HFET designs, but it is expected that overall performance improvement will more that compensate for this shortcoming.

The self-aligned n-channel JFET [10,11] fabricated in the epitaxially grown GaAs buffer allows operation with low gate leakage up to 1 V, which is important in minimizing static power. In addition to the usual benefits of self-aligned processing, the self-aligned JFET eliminates excess gate capacitance present in the conventional JFET from metal overhang as well as junction broadening. This typically leads to a rf-performance penalty in the conventional JFET compared to MESFETs of the same gate length. The self-aligned JFET with a coincident or slightly undercut junction gate region has shown comparable rf performance to a MESFET of the same gate length with the added advantage of a higher gate turn-on voltage [10].

A self-aligned refractory gate process based on tungsten or tungsten silicide gate metal was used to fabricate the complementary circuits. A 13 mask process with the following steps was employed: 1) pHFET active area definition by wet chemical etching, 2) nJFET active area implants (gate, channel, and backside) [11], 3) a thermally stable isolation implant based on oxygen ions [12], 4) gate definition with tungsten or tungsten silicide refractory gate deposition, patterning, reactive ion etch in SF_6:Ar [13-15], and a wet etch to remove the heavily-doped junction-gate semiconductor regions, 5) the n^+ source and drain implants with Si, 6) the p^+ source and drain implants with Zn followed by a capless rapid thermal anneal, 7) the p-ohmic metal definition and alloy using AuBe, 8) n-ohmic metal definition and alloy using GeAuNiAu, 9) first via definition with silicon nitride dielectric, 10) first metal interconnect with TiPtAu, 11) second via with silicon nitride, 12) second metal interconnect with TiPtAu, and 13) passivation with silicon nitride. Minimum feature dimensions of 3 µm lines, 2 µm spaces, 0.7 µm gates, and 1.5 µm vias were used. A junction-gate pHFET simplifies the processing of step 4) since the wet etch definition of the junction gates is simultaneous for n- and p-channel FETs. This process sequence is slightly modified for the short gate FETs presented in a later section. It is important to note that for the JFETs the electrical gate is the pn junction region. The metal-semiconductor contact is fabricated to be a non-alloyed ohmic contact to a heavily doped semiconductor region [16], Zn-implanted GaAs for the nJFET and Si-doped InGaAs for the pHFET.

Both nJFET and pHFETs are enhancement-mode devices. The nJFET shows a maximum transconductance (g_m) of 230 mS/mm. At a 1.0 V gate and drain bias typical of circuit operation, the g_m and I_{DS} are approximately 170 mS/mm and 90 mA/mm, respectively with f_t of 19 GHz, f_{max} of 28 GHz, and a subthreshold slope of 90 mV/decade. Likewise, the pHFET shows a maximum g_m of 43 mS/mm, but g_m of 29 mS/mm and I_{DS} of 20 mA/mm under operating conditions of 1.0 V on gate and drain. The pHFET shows an f_t of 3.5 GHz and poor subthreshold characteristics due to soft turn-on.

The CHFET technology demonstrated loaded ring-oscillator delays of 319 ps/stage at 8.9 fJ with a power supply of 0.8 V [9]. The loading was provided by 200 µm of wire in second metal which was interdigitated with grounded first metal to provide a capacitive load between each stage. The power consumption was predominantly static power caused by a soft turn-on of the pHFET. Faster gate delays up to 179 ps were obtained at higher power supply voltages, but gate current caused an increase in power consumption. Since that work FET performance has been improved and pHFET leakage has been reduced, as presented in the section on short gate devices.

MICROWAVE TECHNOLOGY

An nJFET fabricated in the digital CHFET process was evaluated as a microwave device. A narrow-band amplifier was selected as a test vehicle since its successful implementation demonstrates the feasibility of most monolithic microwave integrated circuit

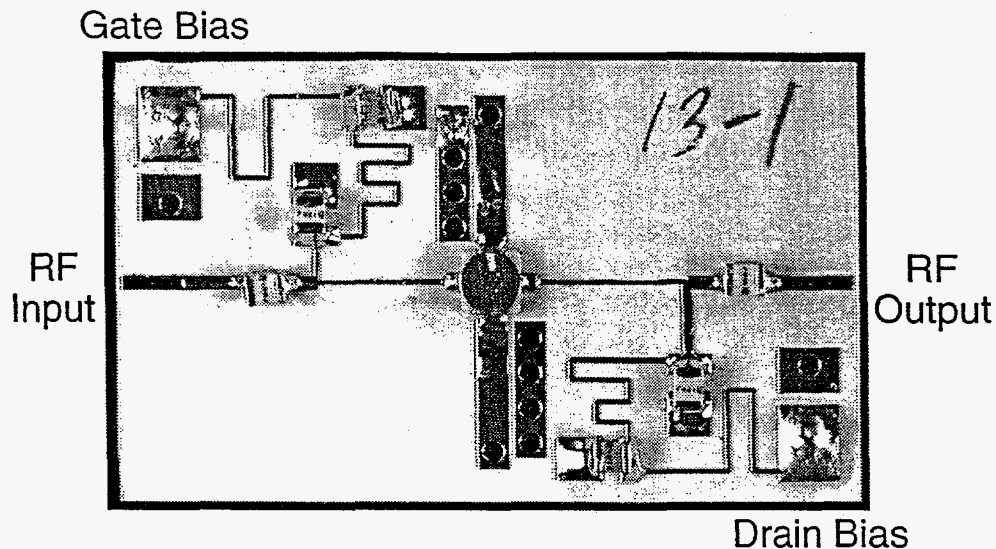

Figure 2. Photograph of a narrow-band CHFET amplifier using a packaged nJFET.

(MMIC) functions. The approximate gate length used was 0.7 μm and the gate width was 100 μm. The low power digital applications require low bias voltages ($V_{DS} \approx 1$ V), a small positive gate threshold, and large gate turn-on voltages (>1 V). These design parameters are also ideal for low-power microwave applications. The voltages are very suitable for battery operation on a single cell and the positive gate threshold along with the large positive gate turn-on voltage, eliminates the need for a negative supply as commonly required with MESFETs. Though not explicitly designed for microwave operation, the device's microwave properties are impressive with $f_t > 13$ GHz, $f_{max} > 20$ GHz and a minimum noise figure of about 1.6 dB (with a 12 dB associated gain) all measured at a 1 mW DC bias level.

S-parameters were measured at wafer level and used to design a narrow-band 2.4 GHz microstrip based amplifier. The wafer was then thinned to 100 μm and amplifiers were fabricated from both standard 100 mil stripline packaged parts as well as a chip and wire assembly. The amplifier was fabricated on Rogers TMM-10 25 mil thick substrate, shown in Figure 2 for an amplifier with a packaged part. Tests were performed using an HP 8510C network analyzer and, for selected parts, using an HP 8971 noise figure meter. The measured gain vs. frequency is plotted in Figure 3 for four amplifiers using packaged parts and three amplifiers with chip and wire assemblies. Peak gains between 8 and 10 dB were measured. The matching circuits accurately centered the frequency about 2.4 GHz for the chip and wire parts. Package parasitics were not adequately accounted for and are responsible for the shift in frequency for packaged parts. The measured gain and noise figure for a packaged part are plotted in Figure 4. The minimum noise figure was about 2.5 dB and occurred at a frequency higher than the gain's peak. This is not surprising as the amplifier was designed for maximum gain and not minimum noise figure. A minimum noise figure design should achieve a value more consistent with the on-wafer measured value of 1.6 dB, although some gain would be sacrificed. The amplifier gain and input and output return loss are plotted in Figure 5.

Because the digital CHFET process was used to fabricate the transistor, addition of MMIC passive elements that are compatible with the digital process will provide a mixed-mode technology. The passive elements needed are: 1) a thin film resistor, 2) thin film capacitors, 3) inductors, 4) transmission lines, 5) airbridges, and 6) backside vias. The CHFET via process will be used to etch dielectric back to the substrate in the MMIC areas

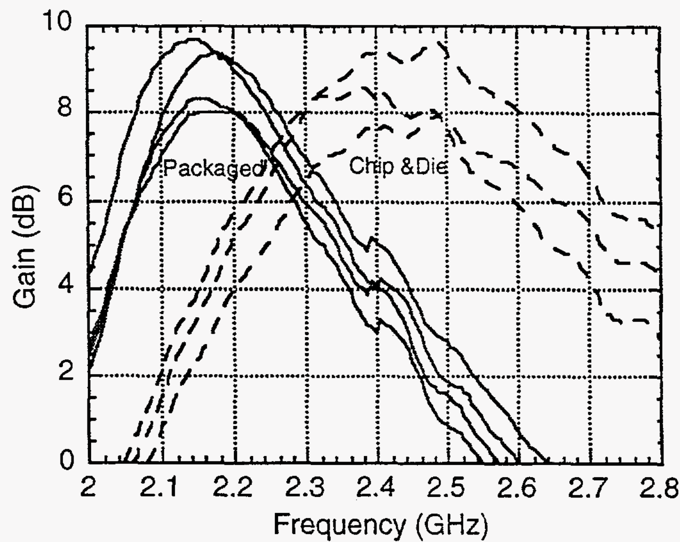

Figure 3. Gain characteristics of four packaged and three chip and die narrow-band amplifiers operating at 1 mW power.

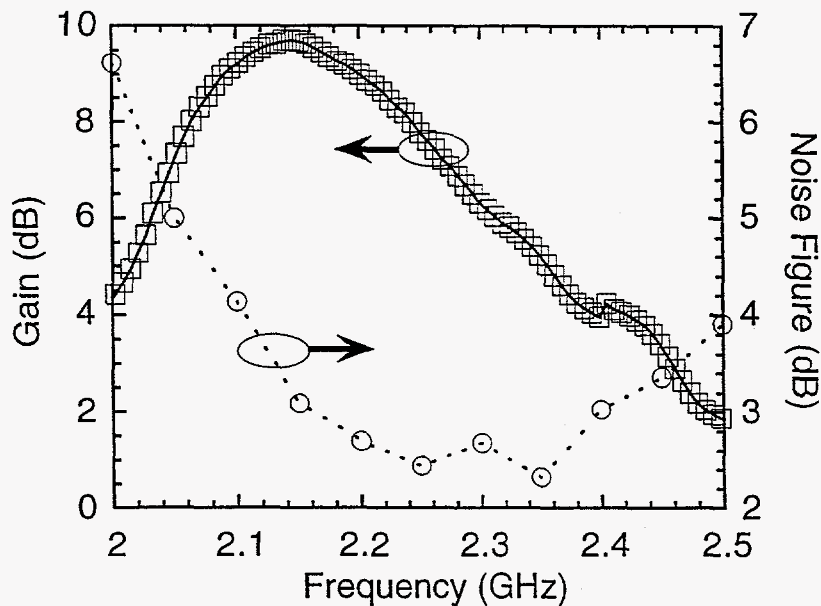

Figure 4. Plot of measured gain and noise figure versus frequency for a packaged narrowband amplifier operating at 1 mW power.

and the CHFET first metal process will be used for capacitor bottom electrodes and the base of transmission lines (including spiral inductors). The following new process steps will provide for the rest of the MMIC passive elements: 1) thin film resistor, 2) capacitor dielectric, 3) capacitor top metal, 4) airbridge post, 5) airbridge and plated metal, and 6) backside via. A full CHFET-MMIC process will require up to 19 mask levels and is currently being implemented in our laboratory.

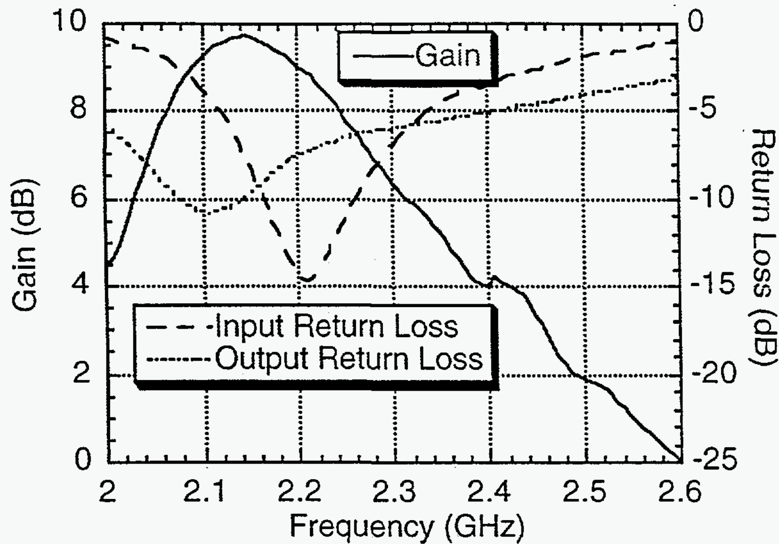

Figure 5. Amplifier gain and input and output return loss for a packaged narrowband amplifier operating at 1 mW power.

SHORT GATE CHFET DEVICES

While demonstration of the digital and microwave technologies has been made, performance improvements by reducing the gate length is desired. We have reduced the gates from optically patterned 0.7 µm lengths to the 0.3 - 0.4 µm range by the use of e-beam lithography. Both W and W/WSi_x bilayer gates have been patterned. While the W gates are preferable for the non-alloyed ohmic contacts to JFETs because of its greater conductivity, WSi_x gates make superior Schottky contacts for $0.4 \leq x \leq 0.5$ [17]. The Schottky contacts are better for conventional pHFET structures (i.e. non JFETs) and for these FETs the W/WSi_x bilayer gate provides both a good Schottky contact and low gate resistance. Good anisotropic profiles with low plasma damage and sub 0.5 µm W/WSi_x bilayer gates have been obtained with negative electron-beam resist and reactive ion etching in a SF_6/Ar chemistry [15]. A short gate W process works well with the same etch conditions as the W/WSi_x bilayer gates. The short gate processes have been used to fabricate self-aligned nJFETs and pHFETs.

0.3 µm nJFET

In addition to short gate definition, the process must be designed to address short channel effects as with self-aligned MESFETs. The channel's active region should be made more shallow and steps must be taken to prevent buffer conduction and associated threshold voltage shift from the source and drain implants. The nJFET p^+ gate implant was changed from Zn to Cd to maintain a high surface doping level greater than 10^{19} cm^{-2} while moving the pn junction closer to the surface [18]. The channel active region utilizes the same Si channel and C backside confinement implant as prior JFETs [11]. The Si dose was adjusted to keep the threshold voltage the same. The lateral short channel effects were addressed by implementing a sidewall process with a shallow 40 KeV SiF implant under a

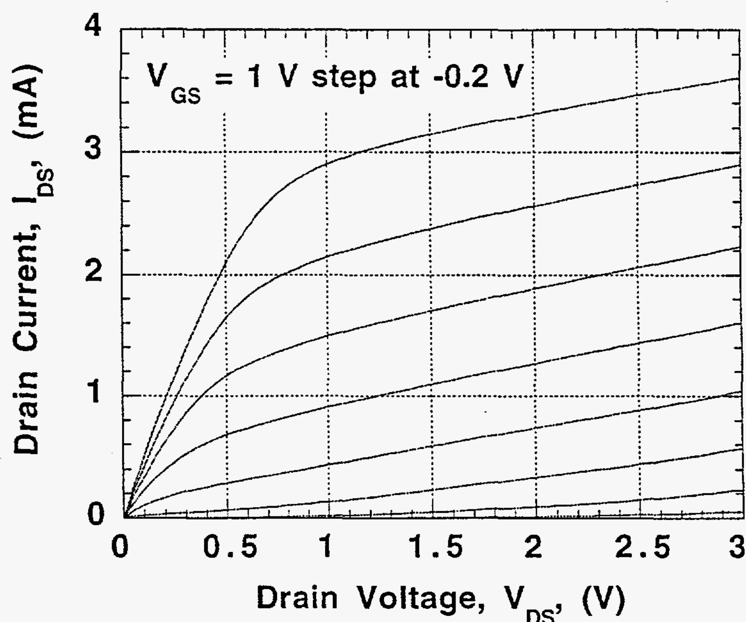

Figure 6. I_{DS}-V_{DS} characterictics for a self-aligned 0.3x20 μm^2 nJFET.

0.1 µm wide SiN sidewall [19] and a deeper 50 KeV Si implant spaced from the gate by the sidewall in the source and drain regions.

Using this process a high performance 0.3 x 40 µm JFET with W gates was fabricated. The drain I-V characteristics are shown in Figure 6. A maximum transconductance of 265 mS/mm, f_t of 49 GHz, f_{max} of 58 GHz, and a subthreshold slope of 110 mV/decade were measured. The proportionate increase in f_t with inverse gate length as well as the excellent subthreshold slope indicate that short channel effects have been suppressed. This nJFET needs a slight threshold voltage shift for enhancement-mode operation.

0.4 µm pHFET

In addition to the new short gate process, the pHFET structure was completely redefined. As mentioned previously, process simplicity was one factor in choosing junction gates for both pFET and nFET, but low pFET performance compels another approach. A doped-channel GaAs/AlGaAs pHFET was chosen for the current work. A 100 Å Be-doped GaAs channel with a 50 Å GaAs spacer, a 150 Å $Al_{0.75}Ga_{0.25}As$ undoped barrier layer, and a 100 Å cap layer form the active layers of the pHFET. This structure is similar to conventional HIGFETs [20], except that the doped GaAs channel allows for threshold voltage adjustment. This pHFET is still process compatible with the GaAs self-aligned nJFET with only minor modifications to the gate process. It is only process compatible with an nHFET if stacked epitaxial layers or small area, selective epitaxial regrowth is used. Lateral short channel effects are especially severe in compound semiconductor pFETs. They have been addressed in this work with a 0.1 µm wide SiN sidewall process using 50 KeV Zn implants under the sidewalls and 125 KeV implants in the source and drain regions.

pHFETs with gate lengths ranging from 1.0 to 0.3 µm was fabricated and characterized. The transistors scaled well down to 0.5 µm gate length. The output

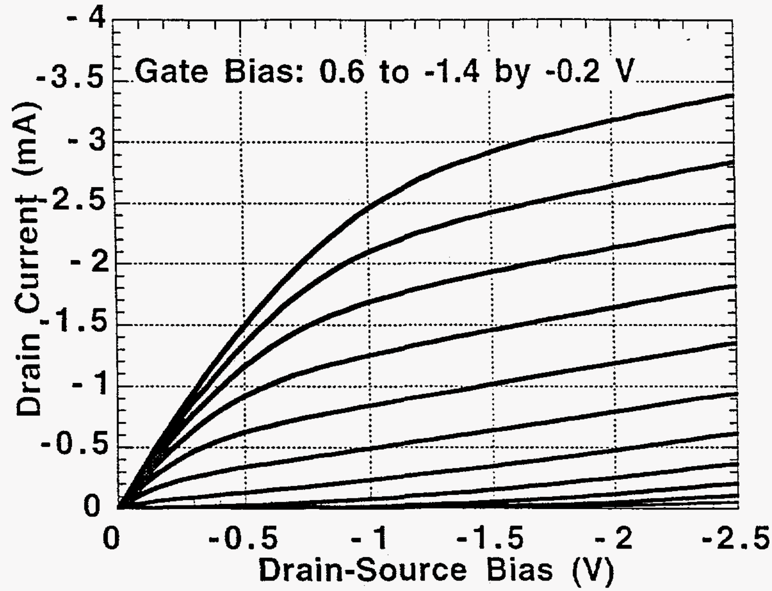

Figure 7. I_{DS}-V_{DS} characteristic for a self-aligned 0.4 x 40 μm^2 pHFET.

conductance and subthreshold slope degraded noticeably at 0.4 µm gate length and severe short channel effects were observed at 0.3 µm. Nevertheless, good rf characteristics were observed down to 0.4 µm gate lengths. Drain I-V characteristics for a 0.4 x 20 µm pHFET are shown in Figure 7. A maximum transconductance of 62 mS/mm was measured, as seen in Figure 8, with f_t of 11.5 GHz and f_{max} of 13 GHz. The subthreshold slope ranges from 130-170 mV/decade for gate lengths 0.5 µm and longer, as seen in Figure 9. At 0.4 µm gate length the subthreshold slope increases to 310 mV/decade. These subthreshold slopes are still not as good as nJFET values but are clear improvements even at long gate lengths from our previous pHFETs [9]. The transconductance decreases only slightly to 54 mS/mm for operating biases of 1.0 V on gate. A slight threshold voltage adjustment will be necessary to get enhancement-mode operation for use in CHFET circuit designs.

A summary of the FET characteristics (1V drain and gate bias for currents transconductance) is given in Table 1 to compare first generation CHFET devices with the new short gate devices.

Table 1. A summary of the FET characteristics for first generation and current CHFET devices.

Device Parameter	nJFET		pHFET	
	current	1st gen.	current	1st gen.
Lg (µm)	0.3	0.7	0.5	0.7
g_m maximum (mS/mm)	265	230	62	43
g_m @1V (mS/mm)	240	170	54	29
I_d @ 1V (mA/mm)	150	90	37	20
f_t (GHz)	49	19	8.8	3.5
Subthreshold slope (mV/decade)	110	90	170	n/a

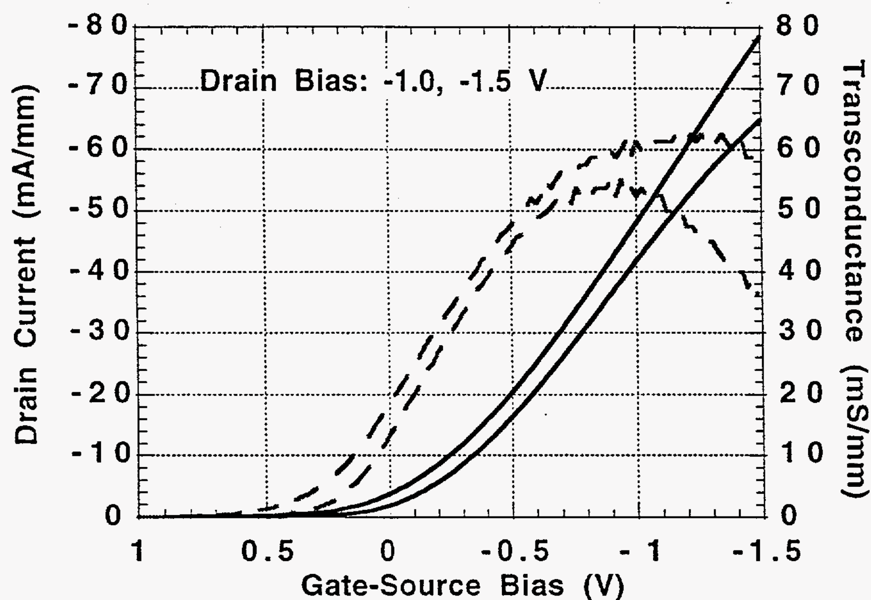

Figure 8. I_{DS}-V_G and g_m-V_G characteristics at drain biases of -1.0 and -1.5 V for a self-aligned 0.4x20 μm^2 pHFET.

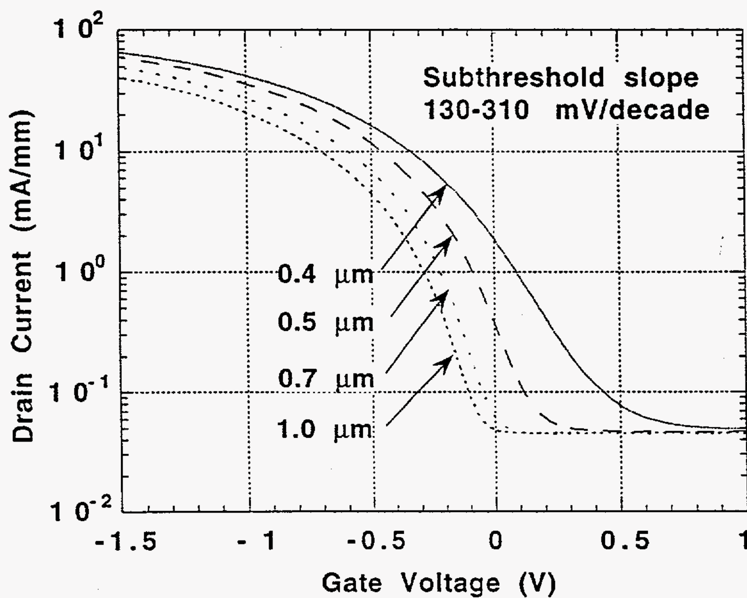

Figure 9. I_{DS}-V_G characteristics at a drain bias -1.0 V for a self-aligned pHFET.

CONCLUSION

CHFET technology development for low-power, digital and microwave mixed-mode applications has been described. The first generation digital CHFET technology operated with 319 ps loaded gate delays at 8.9 fJ. The digital nJFET device was used as a low-power microwave transistor in a hybrid microwave amplifier without any modification to the digital process. A narrow band amplifier with a 0.7 x 100 μm nJFET as the active element was designed, constructed, and tested. At 1 mW operating power, the amplifier showed 8-10 dB of gain at 2.15 GHz for packaged parts and 2.4 GHz for chip and wire assemblies. In addition, next generation CHFET transistors with sub 0.5 μm gate lengths were demonstrated. Cutoff frequencies, f_t of 49 GHz and 11.5 GHz were achieved for n- and p-channel FETs with 0.3 and 0.4 μm gates, respectively. These FETs will enable both digital and microwave circuits with enhanced performance.

ACKNOWLEDGMENTS

The authors would like to thank Geraldine Lopez for device fabrication. This work was supported by the Department of Energy under contract number #DE-AC04-94AL85000.

REFERENCES

[1] D. E. Grider, P. P. Ruden, J. C. Nohava, I. R. Mactaggart, J. J. Stronczer, and R. H. Tran, "0.7 Micron Gate Length Complementary $Al_{0.75}Ga_{0.25}As$/GaAs HIGFET Technology for High Speed/Low Power Digital Circuits," *IEDM Technical Digest*, pp. 331-334, 1992.

[2] J. K. Abrokwah, J. H. Huang, W. Ooms, C. Shurboff, J. A. Hallmark, R. Lucero, J. Gilbert, B. Bernhardt, and G. Hansell, "A Manufacturable Complementary GaAs Process," *IEEE GaAs IC Symposium Technical Digest*, pp. 127-130, 1993.

[3] R. A. Kiehl, J. Yates, L. F. Palmateer, S. L. Wright, D. J. Frank, T. N. Jackson, J. F. Degelormo, and A. J. Fleischman, "High-Speed, Low-Voltage, Complementary Heterostructure FET Circuit Technology," *IEEE GaAs IC Symposium Technical Digest*, pp. 101-104, 1991.

[4] K. Matsumoto, M. Ogura, T. Wada, T. Yao, Y. Hayashi, N. Hashizume, M. Kato, N. Fukuhara, H. Hirashima, and T. Miyashita, "Complementary GaAs SIS FET Inverter Using Selective Crystal Regrowth Technique," *IEEE Electron Device Letters*, vol. 7, pp. 182-184, 1986.

[5] T. Mizutani, S. Fujita, and F. Yanagawa, "Complementary Circuit with AlGaAs/GaAs Heterostructure MISFETs Employing High-Mobility Two-Dimensional Electron and Hole Gases," *Electronics Letters*, vol. 21, pp. 1116-1117, 1985.

[6] R. Zuleeg, J. K. Notthoff, and G. L. Troeger, "Double-Implanted GaAs Complementary JFETs," *IEEE Electron Device Letters*, vol. 5, pp. 21-23, 1984.

[7] B. Davari, W. H. Chang, K. E. Petrillo, C. Y. Wong, D. Moy, Y. Taur, M. R. Wordeman, J. Y. C. Sun, C. C. H. Hsu, and M. R. Polcari, " A High-Performance 0.25 μm CMOS Tehcnology: II-Technology," *IEEE Transactions on Electron Devices,* vol. 39., pp. 967-975, 1992.

[8] D. Scherrer, J. Kruse, J. Laskar, M. Feng, M. Wada, C. Takano, and J. Kasahara, "Low-Power Performance of 0.5 μm JFET for Low-Cost MMIC's in Personal Communications," *IEEE Electron Device Letters,* vol. 14, pp. 428-430, 1993.

[9] A. G. Baca, J. C. Zolper, M. E. Sherwin, P. J. Robertson, R. J. Shul, A. J. Howard, D. J. Rieger, and J. F. Klem, "Complementary GaAs Junction-Gated Heterostructure Field Effect Transistor Technology," *IEEE GaAs IC Symposium Technical Digest*, pp. 59-62, 1994.

[10] M. E. Sherwin, J. C. Zolper, A. G. Baca, R. J. Shul, A. J. Howard, D. J. Rieger, J. F. Klem, and V. M. Hietala, "An All Implanted Self-Aligned Enhancement Mode n-JFET with Zn Gates for GaAs Digital Applications," *IEEE Electron Device Letters,* vol. 15, pp. 242-244, 1994.

[11] J. C. Zolper, M. E. Sherwin, A. G. Baca, R. J. Shul, J. F. Klem, and V. M. Hietala, "Enhanced High Frequency Performance in a GaAs, Self-Aligned, n-JFET Using a Carbon Buried p-Implant," *IEEE Electron Device Letters,* vol 15, pp. 493-495, 1994.

[12] J. C. Zolper, A. G. Baca, and S. A. Chalmers, "Thermally Stable Oxygen Implant Isolation of p-type $Al_{0.2}Ga_{0.8}As$," *Applied Physics Letters,* vol. 62, pp. 2536-2538, 1993.

[13] R. J. Shul, D. J. Rieger, A. G. Baca, C. Constantine, and C. Barratt, "Anisotropic Electron Cyclotron Resonance Etching of Tungsten Films on GaAs.," *Electronics Letters,* vol. 30, pp. 84-85, 1994.

[14] R. J. Shul, A. G. Baca, D. J. Rieger, and A. J. Howard, "Anisotropic Etching of WSi Films on GaAs," *Electronics Letters,* vol. 31, pp. 317-318, 1995.

[15] R. J. Shul, M. E. Sherwin, A. G. Baca, J. C. Zolper, and D. J. Rieger, "Short Gate Etching of W/WSi Bilayer Gates," *Electronics Letters,* vol 32, pp. 70-71, 1996.

[16] J. C. Zolper, A. G. Baca, R. J. Shul, A. J. Howard, D. J. Rieger, M. E. Sherwin, M. L. Lovejoy, H. P. Hjalmarson, B. L. Draper, J. F. Klem, and V. M. Hietala, "An All-Implanted, Self-Aligned, GaAs JFET with a Non-Alloyed W/p^+-GaAs Ohmic Contact.," *IEEE Transactions on Electron Devices,* vol. 41, p. 1078 (1994).

[17] A. G. Lahav, C. S. Wu, and F. A. Baiocchi, "WSi_x Refractory Metallization for GaAs Metal-Semiconductor Field Effect Transistors," *J. Vac. Sci. Technol.*, vol. B6, pp. 1785-1795.

[18] J. C. Zolper, A. G. Baca, M. E. Sherwin, and R. J. Shul, "High Performance GaAs JFET with a Shallow Implanted Cd-Gate," *Electronics Letters,* vol. 31, pp. 923-924, 1995.

[19] A. G. Baca, A. J. Howard, R. J. Shul, and M. E. Sherwin, "Trenching Observed During Sidewall Formation in GaAs Self-Aligned Refractory Gate FETs," *Electronics Letters,* vol 32, p. 74-75, 1996.

[20] P. P. Ruden, M. Shur, D. K. Arch, R. R. Daniels, D. E. Grider, T. E. Nohava, "Quantum-Well p-Channel AlGaAs/InGaAs/GaAs Field Effect Transistors," *IEEE Trans. Elect. Devices,* vol. 36, pp. 2371-2379, 1989.

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.