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Verification of Three Dimensional Charge Transport Simulations Using Ion Microbeams

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Abstract

Optically targeted, ion microbeams provide a useful means of exposing individual structures within an integrated circuit to ionizing radiation. With this tool, calibrated, low damage, charge collection spectra can be measured from specific circuit structures without preceding ion damage to the structure or surrounding circuitry. This paper presents comparisons of calibrated, low damage, ion microbeam-based charge collection measurements and three-dimensional, charge transport simulations of charge collection for isolated n- and p-channel field effect transistors under conducting and non-conducting bias conditions.

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1. Introduction

Single event upset is the disruption of a circuit's normal operation, caused by the passage of an ionizing particle through an integrated circuit (IC). In space-based systems, the sources of ionizing radiation can be galactic cosmic rays, particles emitted by solar activity, or protons trapped in the earth's magnetic fields. Terrestrially, energetic ions arise from naturally occurring, alpha-emitting transuranic impurities in IC manufacturing materials, products of cosmic ray showers or neutron-induced Si-recoils. When such particles lose energy transiting an IC, electron-hole pairs are created. The magnitude of this electrical charge is referred to as the particle's linear energy transfer (LET); it is the electronic portion of the stopping power (dE/dx) measured in units of $MeV/mg/cm^2$. High electric field gradients present in a circuit can enhance separation and collection of this electrical charge before recombination occurs. If the magnitude and duration of the charge collection transient is greater than a critical value for the circuit, upset may occur. Since the generation of charge within an IC is the underlying physical process which causes upset, the amount of charge generated and collected at specific circuit nodes is an important point of comparison between experiment and computer simulations of circuit response to ionizing radiation.

Using 14 MeV carbon ion microbeams, calibrated, low-damage, charge collection spectra have been recorded from isolated circuit test structures and compared with charge transport simulation results in order to test the predictive capability of

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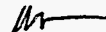

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simulation codes for future IC designs. The experimental and circuit simulation charge collection results presented here are all based on the Sandia-designed TA670 16K static random access memory test chip. The TA670 was designed in 1987 as a total dose and SEU rad-hard test chip using 2 μm design rules and fabricated on a 1 μm process line. Since we have access to the complete circuit design masks, vertical layout, doping concentrations, and other circuit parameters, the TA670 has been a valuable test-bed for evaluating microbeam radiation testing techniques.

Charge collection measurements of a transistor imbedded in surrounding circuitry can yield quite different results than those obtained for the same transistor irradiated in isolation. Differences arise from the introduction of external loading, capacitive coupling, and additional charge conduction paths or biasing conditions enforced by neighboring circuit structures. Without explicit control or measurement of this chorus of external influences, the conditions of a measurement can differ significantly from those assumed in a simulation. Therefore, as a first step toward validation of the simulation code for the entire circuit, we have begun by comparing the charge collection predicted by simulation, and measured by experiment, for isolated p-channel and n-channel field effect transistors (FET). Present on the TA670 die are a number of isolated, large area, test FETs which are normally left unwired for the IC's operation. However, we have wired and packaged the TA670 to allow measurement of charge collection from these isolated test FETs. A cross-sectional view of these FETs is shown in figure 1, along with vertical dimensions and biasing conditions for the conducting ("on") and non-conducting ("off") states.

2. Computer Simulation

2a. Numerical Simulation of Charge Collection

The charge–collection characteristics of Si junction diodes and transistors in response to an ion strike can be computed using semiconductor device simulation codes [1]. These codes solve Poisson's equation and the current continuity equations in one, two, or three dimensions, using finite element techniques. The simulations model the physics of carrier transport under potential and carrier concentration gradients, giving detailed microscopic information such as transient electron and hole densities throughout the simulated device. In this work, we have used a commercially–available, three–dimensional device simulator [2] to model charge collection in n– and p–channel transistors in both the "on" and "off" bias states. The simulations reported here typically require 6–12 CPU hours to execute on a Hewlett–Packard J210 workstation.

Input parameters required for these three dimensional simulations include structural information and doping profiles of the test circuit, as well as the charge generation characteristics of the incident ion. Since the simulation results can sometimes

depend critically on these values, the input parameters have either been independently measured or a range of values has been examined in order to determine the severity of the dependence.

Vertical and horizontal circuit dimensions were obtained directly from the circuit design masks. Doping profiles were obtained from process simulations and spreading resistance measurements of the TA670 fabrication technology. The charge collection in the p-drain has been modeled in the absence of the adjacent p-source and gate, since these regions do not contribute significantly to charge collection. P-drain charge collection is dominated by drift and diffusive collection from the epi and substrate, respectively. (We will use the term 'epi', from here on, to refer to the lightly n-doped epitaxial layer which lies between the n- or p-well and the n-type substrate.) Omitting the p-source and gate from the p-drain simulations was further justified by the fact that initial simulations which included the entire transistor were seen to produce identical results to those which included only the p-drain. This streamlining of the model produced a significant savings in computation time. For the n–channel simulations, however, it was necessary to model the entire transistor, since lateral charge flow between the source and drain can be induced by ion strikes [3].

The charge generation profile (LET *vs.* depth) of the normally–incident 14 MeV carbon ion strikes to the center of the n- and p-drains was computed using TRIM-90 [4]; a uniform ion track radius of 0.1 μm was assumed. By calculating the electron–hole generation in the device and the ensuing drift, diffusion, and recombination of free carriers in three dimensions, the time-dependent current transients present at the device drain are computed by the DAVINCI code. The resulting terminal currents are integrated to yield the charge–collection characteristics of the circuit structure being simulated.

2b. Charge Collection Mechanisms

The simulated charge collection transients are shown in Figure 2 for each transistor type and bias condition. In each panel, the lower curve displays the computed current transient at the drain as a function of time after the ion strike; the corresponding upper curve displays the total integrated charge collection at the drain also as a function of time after the ion strike. While a comprehensive description of charge transport in each case is beyond the scope of this paper, a few comments may assist interpretation of the simulation results and their comparison to the experimental results.

Charge collection in n- or p-drains consists of contributions from the epi layer, the substrate regions, and any enhancement or reduction due to junctions. Charge deposited in the epitaxial layer is collected by the p-drain at short times ($t < 0.1$ nanosec) under the influence of electric fields (drift); charge deposited in the substrate is collected in the p-drain at later times ($t > 0.1$ nanosec) through simple diffusion. Because the p–channel transistor rests in an n-well which sits in an n-type epi layer on an

n-type substrate, there is negligible effect on charge collection due to the n-well/n-epi/n-substrate "junctions". Thus, the total charge collection in the p-drain depends mainly on the thickness of the epitaxial layer (from which charge is collected with nearly 100% efficiency) and the free carrier lifetime in the substrate (which governs how much substrate charge diffuses into the epi layer before recombination can occur). As a consequence of this, the total charge collection into the p-drain has little dependence on the p-drain bias condition and the results for the conducting and non-conducting states are very similar.

For the n–channel transistors, the charge collection mechanisms are considerably more complex because the n–channel transistors sit in a p–well on the n–epi/substrate. This can lead to a change of sign in the ion–induced current transient. For example, in the n–on case, at early times, ($t < 1.0$ picosec), the ion track shunts the n–drain to the n–substrate. Since these regions are at 5 volts of potential difference, an initial negative shunt current flows [5]. As the track disperses by diffusion, the shunt disappears and a different collection mechanism dominates the current response. Holes deposited within the p–well raise the well potential, thereby lowering the n-source/p-well junction barrier. This results in electrons being injected into the p-well by the source, which can be collected at the drain as a positive current [3]. Important for both n–channel cases, this mechanism is especially dominant in the n–off case because the 5–volt potential difference between the source and the drain aids collection of electrons at the drain. This mechanism results in a positive total charge collection for the n–off case, shown in Figure 2.

2c. Parameter Sensitivity in Simulation Results

The validity of the simulation results can be greatly affected by the accuracy of the device description and material parameters supplied to the simulation. For example, charge collection due to the shunt effect in the n–on case is very dependent upon the assumed doping profile. The written process specification indicates an abrupt n-epi/n-substrate transition at a depth of 2 μm; however, spreading resistance measurements on the fabricated device yielded doping profiles showing an additional 1.0 μm thick transition region between the epitaxial layer and the heavily–doped substrate. Using the abrupt epi/substrate transition, the computed n-on charge collection was less than 65% of that attained when the more accurate, measured doping profiles were used. But, in the absence of the shunting mechanism, as is the case for p-on and p-off drains, the simulated charge collection results were quite insensitive to changes in this input parameter. Thus, inaccuracies in the input parameters do not necessarily influence the results of each structure in the same manner, or to the same degree.

The energy loss of the ion in the circuit is also a parameter subject not only to the approximation of determining dE/dx, but also of determining the depth of the ion in the circuit when it is at a given energy. If the ion's energy loss in passive circuit

overlayers (e.g. passivation layers, metallization lines, oxide insulators) is neglected, or these overlayer thickness are inaccurately known, the charge generation characteristics of the ion which are provided the simulation will be in error. Overestimating the range of the ion within the device can considerably reduce the estimate of the amount of charge liberated within the active regions of the circuit, since the Bragg peak would be assumed to be deeper in the substrate. This effect is even more pronounced for rather low–energy ions where the change in stopping power with energy is greatest. In the case of 14 MeV carbon incident on an n-on transistor, if the ion's energy loss in the 5.3 microns of overlying passivation glass, metallization and oxide is neglected, the resulting simulated charge collection is only about 75% of that which is computed if ion energy loss from the overlying, non-active layers is included.

Lastly, though free carrier lifetimes in the epitaxial layer and substrate are generally expected to have a strong influence on the simulation results, the simulated charge collection results for the n-on case were insensitive to this parameter. Doubling the minority carrier lifetimes from 1 microsecond to 2 microseconds resulted in only a 1 fC increase to the 293 fC charge collection calculated for the n-on drain. This insensitivity to minority carrier lifetimes occurs because the dominant charge–collection mechanisms for this case (shunting at short times and lateral charge injection at later times) are not highly dependent on lifetime. We would expect to see a much greater dependence of total charge collection on lifetimes for the p-channel cases, where minority carrier lifetimes regulate the amount of substrate charge which reaches the drain before recombination can occur.

3. Experimental Measurement of Charge Collection

The experimental charge collection measurements are accomplished by directly recording the charge pulse height resulting from each ion strike. In direct analogy to the configuring of a surface barrier detector, a charge-sensitive pre-amp is connected to the bias pin (V_{dd}) of the IC package and normal operating bias is applied to the IC through the pre-amplifier. For the isolated test FET structures used in this study, the specific biasing and measurement connections to the test structures are shown schematically in figure 1.

It is well-known that damage effects play a dominant role in microbeam-based radiation testing, even at beam intensities of less than a thousand ions/second. Unlike analytical applications of the nuclear microprobe, in which samples are routinely exposed to picoamp beam currents for many minutes during ion beam analysis, the charge collection response of a device can degrade after only hundreds of ions per exposure location. This has been a prime motivation for implementing event-by-event

recording of data, and optical targeting of the ion beam using a front-viewing microscope. The "event" data file consists of a sequence of (x, y, z, t) entries which record the x and y position of the microbeam at the time each event occurred, the digitized height, z, of the event pulse, and the time, t, at which the event occurred (as derived from the computer's system clock).

The duration of the ion beam exposure at each point in the measured 512x512 scan is controlled by the data acquisition computer. All pixels in the scan are exposed for an equal period of time, and therefore to an equal average incident dose. The practical lower limit for exposure of a single pixel is dictated by the data conversion and storage time needed by the data acquisition system to process a single event; this value is 20 microseconds. Therefore, the average ion arrival rate must be less than 50,000 ions/sec, if single ion resolution is expected. Typically beam currents of only 500 to 2000 ions per second ($\cong$0.1 femtoamp) are used, providing on average a 500 microsecond period between ion arrivals. To improve display statistics, the data is normally binned to a resolution of 64x64x64 pixels, though the original data file retains the original 512x512x4096 resolution.

Since degradation of charge collection pulses can occur after exposures of only hundreds of ions/μm^2, the target IC was replaced with an unexposed part upon exceeding ion exposures of 200 ions/μm^2. Furthermore, the data files were examined after the measurement for evidence of any signal degradation during the irradiation. The experimental charge collection measurements were performed using a 14 MeV carbon beam, focused to 1 μm diameter as determined from STIM (scanned transmission ion microscopy) images of a 1000 mesh grid. The size of the beam scan was calibrated using the pitch of the 1000 mesh grid in the STIM image; the two dimensional charge collection images shown in figure 3 are 40 x 40 μm. The size of the test FET drains is 12 x 5 μm.

The dwell time used in the charge collection measurements was 50 microseconds per exposed pixel. The original 512 x 512 resolution of the scanned beam has been binned to produce a 64 x 64 pixel image; thus each image pixel has a cumulative dwell time of 3.2 milliseconds, (64 exposure pixels * 50 microseconds/exposure pixel). The ion arrival rate was measured in a PIN diode four times during the charge collection measurements, yielding an average of 775 ±144 ions/sec. This results in an average ion exposure per image pixel per scan of 2.5 ±0.5 ions.

The range of 14 MeV carbon in silicon is 14 μm, with an LET of 4.2 MeV/mg/cm^2 at the surface, a maximum LET of 5.5 MeV/mg/cm^2 at a depth of 10 μm, and dropping below 4.2 MeV/mg/cm^2 at a depth of 11.5 μm, as calculated using TRIM-90 [4]. Referring to vertical structure of the FET, shown in figure 1, the distance from the top of the encapsulation layer (not

shown) to the underlying silicon substrate is 7.3 μm. Thus the 14 MeV carbon beam has an LET in excess of 4.2 $MeV/mg/cm^2$ throughout the entire active device and 4 μm into the underlying substrate. The data collection electronics were calibrated by measuring charge collection spectra of this ion in a previously unexposed PIN diode, biased to form a depletion depth of 30 μm (twice the calculated range of the beam). The full charge collection peak of the resulting spectrum, shown in figure 3, was equated to the calculated maximum charge production of this ion in silicon, 622 femtoCoulombs

In order to minimize damage effects, the FET test structures were optically targeted using a front-viewing microscope and only then exposed to the scanned 14 MeV carbon beam. In this way, the effects of any initial beam-induced damage on the charge collection pulse height could be detected if present. From examination of the time-evolution of the charge collection pulse heights measured from different regions of the scanned image, it was seen that the collection of diffusive charge from outside of the drains was quickly suppressed, (presumably by the introduction of defect sites acting as recombination centers), but that for doses up to 200 ions/image pixel, charge collection pulses from the drains did not show any measurable degradation. The images and charge collection spectra shown in figure 3 were generated using events collected in the first 20 scans of the beam across the test structure, or an equivalent ion exposure of 50 ions/image pixel. The charge collection from the drains is therefore taken to be unaffected by damage for the ion exposures used, and representative of the charge collection under 14 MeV carbon irradiation. The boundaries of the drains, as specified in the design mask, are outlined with white dashed lines in the charge collection images in figure 3.

4. Discussion of 3-D Simulation and Charge Collection Measurements

The charge collection spectra extracted from within the outlined region of the n- and p-drains in the charge collection images are shown in the lower panel of figure 3. The experimentally measured and DAVINCI-simulated charge collection for the n- and p-drains in conducting and non-conducting states is summarized in Table I.

For the p-channel devices, the magnitudes of the charge collection determined from simulation and experiment for both biasing conditions are found to agree to within 2%. The roughly 15 fC difference in charge collection between the p-on and p-off drains is clearly resolved experimentally and predicted from simulation. In both biasing conditions, the simulation predicts charge collection which is only slightly lower than the experimentally measured result.

For the n-channel devices, however, simulation and experiment disagree by as much as 70%. The greater disparity in n-drain results has several causes, chief among which is the more complex charge collection mechanism inherent in an ion strike

to the n-drain. Unlike the p-drain in which charge is collected predominately via drift from the epitaxial layer and diffusion from the substrate, charge collection into the n-drain involves both these drift and diffusion processes, as well as enhanced collection from shunting of the drain to the substrate at short times and lateral injection of charge from the n-source after the shunt has dissipated. These additional mechanisms, which involve more regions of the circuit in the collection process, give rise to an increased sensitivity of the simulation to circuit design input parameters. This is in agreement with the observed higher sensitivity which the n-drain simulations exhibited to small changes in the input parameters of the simulation.

A remaining qualitative difference between the n- and p-drain charge collection processes can be seen from the charge collection images in figure 3. Both n-drain images are quite crisp and well defined , while the p-drain images are "fuzzy". The n-drain images are much sharper owing to the much smaller diffusive contribution to the charge collection mechanism; diffusion from the substrate is blocked by the p-well/n-epi junction. The edges of the p-drains are more "fuzzy" since charge collection in the p-drain has a much greater diffusive component, over a longer collection period, unimpeded by a well-epi junction.

5. Summary

One of the most beneficial applications of microbeam-based radiation testing may lie in the measurement of the charge collection response of specific, isolated circuit structures to ionizing radiation, and the verification of charge transport results from three-dimensional device simulations. Calibrated charge collection measurements made under very controlled dose conditions, and inspected for the presence of any damage effects, are found to agree with DAVINCI computer simulations to within 2% for the 'on' and 'off' p-channel FETs, to within 35% for 'on' n-channel FETs, and to within 70% for the 'off' n-channel FET. The relative differences in charge collection from the p-off and p-on drains conform to simulation predictions, as do the n-channel results, although with a greater difference between the absolute magnitudes of the results. The much larger disagreement between experiment and simulation observed in the n-channel results is attributed to the more complex nature of the n-channel charge collection mechanisms, and their greater dependence on simulation input parameters. In making such comparisons between experiment and simulation, the importance of being able to accurately describe both the device structure and its material properties can not be overemphasized.

Table I. Simulated and Measured Charge Collection Results

	P-Off Drain	P-On Drain	N-Off Drain	N-On Drain
Experiment	262 fC	245 fC	100 fC	445 fC
Simulation	257 fC	242 fC	31 fC	292 fC
% Difference	1.9%	1.2%	69.0%	34.4%

Figure Captions

Figure 1. Biasing and vertical structure of the isolated n- and p-channel FETs.

Figure 2. DAVINCI simulation results for charge collection during the first microsecond after 14 MeV C ion strikes into n- and p-channel FET drains under conducting ("on") and non-conducting ("off") biasing conditions. The lower curve in each set reflects the calculated instantaneous drain current after the ion strike, the upper curve is the integrated charge collected at the drain; both are plotted as a function of time after the ion strike.

Figure 3. Charge collection spectra and two dimensional charge collection images (above) for 14 MeV C ion strikes into n- and p-drains of the TA670 test FETs. The full charge generation of the 12 MeV carbon ions is indicated by the PIN diode measurement. In the charge collection images across the top of the graph, greater charge collection is indicated by greater brightness; the drains of the FET are outlined in white (12x5μm).

References

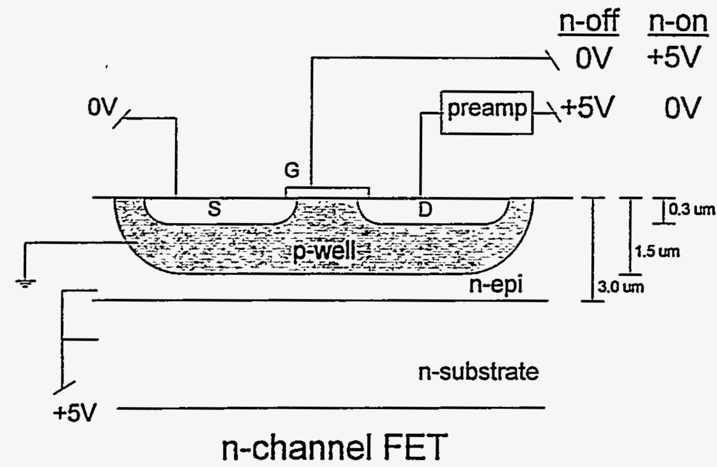
[1] P. E. Dodd, IEEE Trans. Nucl. Sci., 43, no. 2, 561 (1996).

[2] DAVINCI 3.1 (Technology Modeling Associates, Inc. 1995).

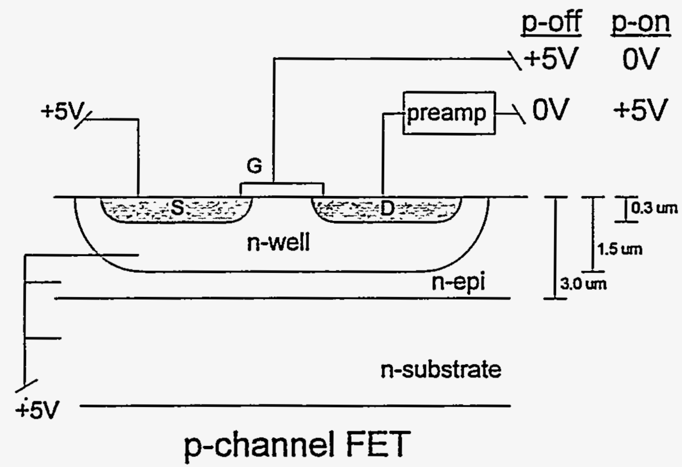
[3] J. S. Fu, C. L. Axness, and H. T. Weaver, IEEE Electron Dev. Lett., 6, no. 8, 422 (1985).

[4] J. F. Ziegler, J. P. Biersack, and U. Littmark, *The Stopping and Range of Ions in Solids,* New York: Pergamon Press, 1985.

[5] J. R. Hauser, S. E. Diehl–Nagle, A. R. Knudson, A. B. Campbell, W. J. Stapor, and P. Shapiro, IEEE Trans. Nucl. Sci., 32, no. 6, 4115 (1985).



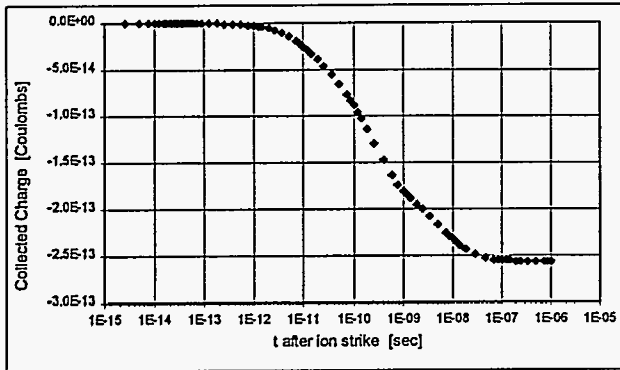
n-channel FET

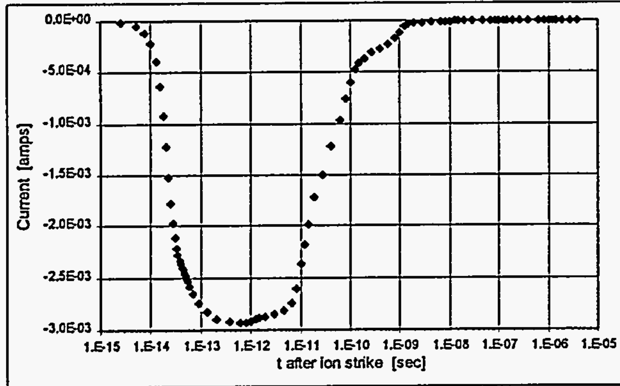


p-channel FET

Figure 1

P-Off Drain





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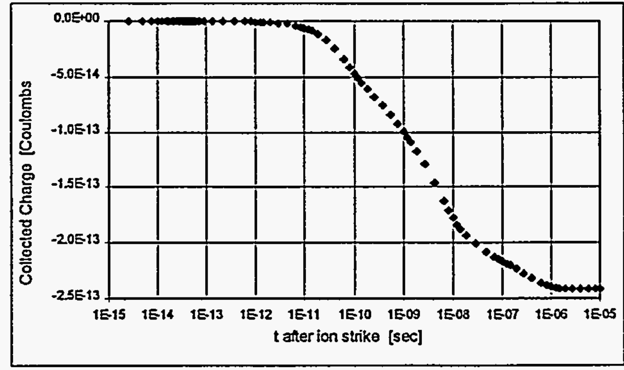
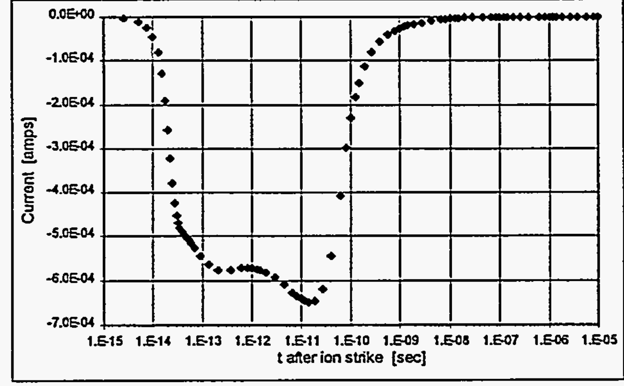
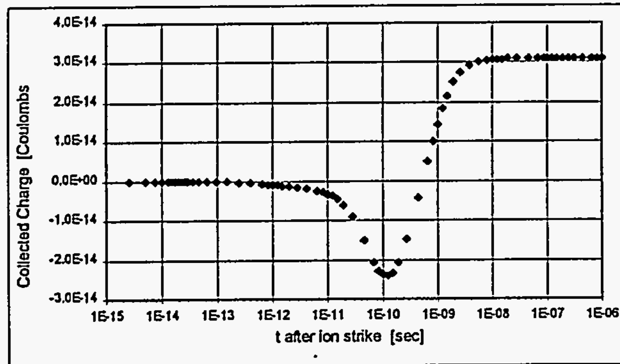
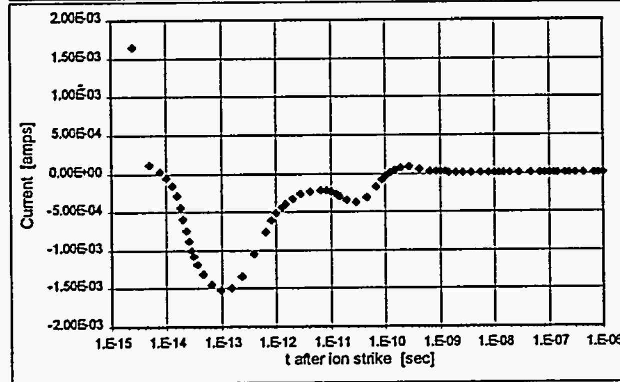


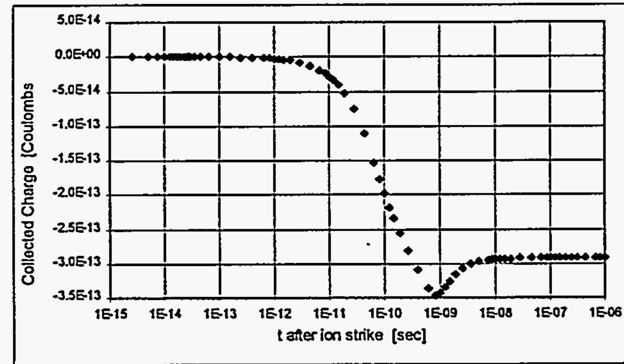


N-Off Drain





N-On Drain



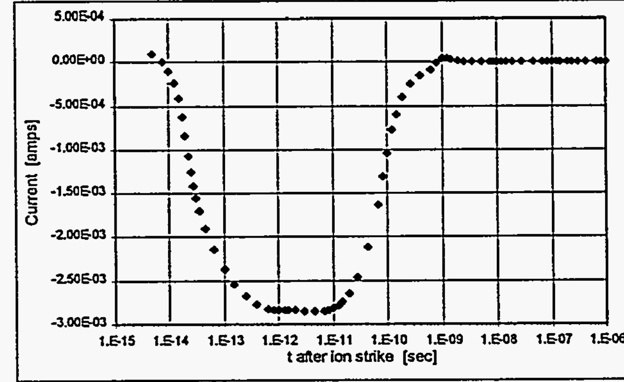


Figure 2

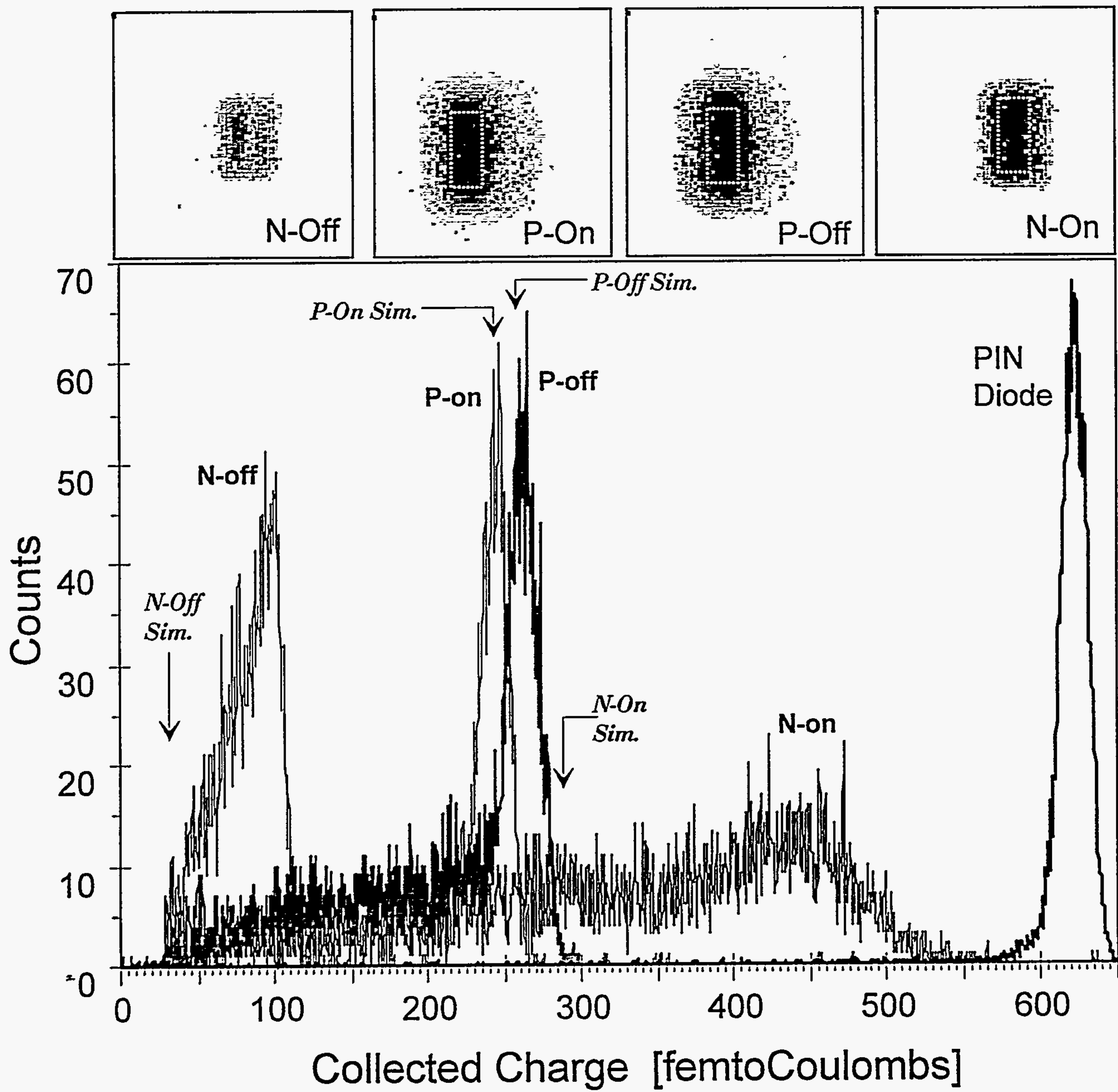


Figure 3