Mechanisms of Heavy-Ion Induced Gate Rupture in Thin Oxides

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Single event gate rupture (SEGR) is a catastrophic failure mode that occurs in dielectric materials that are struck by energetic heavy ions while biased under a high electric field condition [1-3]. SEGR can reduce the critical electric field to breakdown to less than half the value observed in normal voltage ramp reliability tests. As electric fields in gate oxides increase to greater than 5 MV/cm in advanced MOS technologies [4], the impact of SEGR on the reliability of space based electronics must be assessed.

Recent work has shown that the critical field to rupture increases with decreasing oxide thickness, and is correlated with the increasing dielectric strength of thin oxides [5]. The observed dependence of inverse critical field to rupture on ion LET and bias voltage has been described in terms of a physical model of the conductive path for discharge through the oxide [6]. This model relates the resistance of the conductive "pipe" through the oxide to the density of electrons injected from two sources: 1) those due to an applied voltage and 2) those due to energy deposition along the path of the heavy ion. The observed angular dependence of SEGR in thin oxides is well described by this model. This work also showed that SEGR is a true single ion effect and that the buildup of damage from high fluences of ions at biases below critical voltage to rupture, V_{CR}, does not affect breakdown. Also, the incorporation of nitrogen near the oxide-silicon interface, which increases the resistance to charge trapping [7] and the subsequent reliability of thin oxides [8], did not affect SEGR.

In this summary, we explore the nature of SEGR in oxides with thickness from 7 nm to less than 5 nm, where soft breakdown is often observed during traditional reliability tests. We discuss the possible connection between the present understanding of SEGR and voltage stress breakdown models.

Test devices used in this work were 5- and 7-nm patterned polysilicon gate capacitors from Lucent Technologies. To compare the effects of the incorporation of nitrogen on SEGR, oxides were grown in different ambients. One group of 7 nm oxides were grown in O_2, while a second group was grown in N_2O. The 5 nm oxides were grown on p-type wafers via two different processes. The first group of 5-nm oxides was grown via rapid thermal processing in O_2. The second group had dry oxides grown at 800°C followed by an 850°C NO anneal. Each test chip contained an array capacitors with areas of $2.5\text{x}10^{-5}$, $1\text{x}10^{-4}$, $4\text{x}10^{-4}$, and $2.5\text{x}10^{-3}$ cm^2. Devices were assembled into 24-pin ceramic dual-in-line packages.

SEGR tests were conducted at the Brookhaven National Laboratories tandem Van de Graaff accelerator using the following suite of ions: 1) 360-MeV Au, 2) 340-MeV I, and 3) 290-MeV Br. Linear energy transfer (LETs) of the ions were 80.6, 59.6, and 37.5 MeV-cm^2/mg, respectively. To characterize the oxide response to heavy-ion exposures, we measured capacitor gate leakage as a function of gate voltage using a HP4062 parametric analysis system.

A typical set of IV curves for 7-nm oxides is shown in Fig. 1 for a thermal oxide exposed to a flux of 360 MeV Au ions as a function of bias. A constant fluence of 10^6 ions/cm^2 was used for each exposure under constant bias. As irradiation bias increased with each exposure, a steady increase in leakage current was observed between gate voltages of 2 to 4 V. This is evidence that the oxide is being damaged by the heavy-ion flux. After exposure at a gate bias of 3.7 V (an electric field of 5.7 MV/cm, after correcting for work function), leakage current increased rapidly at a gate voltage of 0.2 V reaching a level that is four orders of magnitude higher than the leakage current measured at 3.6 V. This pronounced change in the IV curve between the 3.6 and 3.7 V exposures is the characteristic signature of SEGR. No significant difference was observed in critical voltage to rupture as a function of oxide treatment (O_2 vs. N_2O). Median charge to breakdown of the 7-nm oxides was 12.5 and 16.8 C/cm^2 for the thermal and nitrided oxides, respectively.

P-substrate capacitors with 5-nm oxides exhibited a mixed SEGR response. In a few cases, an SEGR characteristic similar to that seen in the thicker 7-nm oxides was observed. However, in most cases no SEGR characteristic was observed, and IV curves showed only damage buildup with biases up to 6 V (12.4 MV/cm) during exposure, as shown in Fig 2. The same behavior was observed in the thermal and NO-nitrided oxides used in this study. This response is similar to the observation that oxides at 5-nm and thinner do not consistently exhibit hard breakdown during electrical stress, but often show a "soft breakdown" [9].

In Fig. 3 we show inverse critical field to rupture, E_{CR}, as a function of ion LET for the 7 nm oxides of this study and 6, 12, and 18 nm oxides of Ref. [5]. It is clear that E_{CR} increases with decreasing oxide thickness at any given LET. The dependence of E_{CR} on LET at normal incidence has been described empirically by

$$\frac{1}{E_{CR}} = \frac{1}{E_0} + \frac{L}{E_0 B} \qquad (1)$$

where E_0 is the electrical breakdown strength of the oxide, L is ion LET, and B is a fitting parameter [2]. In the conductive pipe model [6], the breakdown strength of the oxide due to voltage stress is given by

$$E_0 = \frac{J_{CR}}{q\mu_V n(V)} \qquad (2)$$

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where J_{CR} is the critical current density to rupture, μ_V is the electron mobility during high electric-field transport, and n(V) is the electron density due to high-field injection of carriers in the pipe. A parallel expression describes the contribution of the heavy-ion generated electron density to conduction along the path of discharge.

At J_{CR}, thermal runaway results in destructive breakdown. Increasing resistance to SEGR with decreasing oxide thickness may simply be a result of an increase in J_{CR}. As oxide thickness decreases to ≤ 5 nm, the data of Fig. 2 suggest that the likelihood is reduced of carriers imparting sufficient energy to initiate thermal runaway [10]. Intriguingly, even a large buildup of precursor oxide defects does not lower the SEGR threshold significantly in Fig. 2, in contrast to expectations one may derive from recent models for "soft breakdown" [11, 12]. The lack of a dependence of SEGR threshold on oxide treatment for the 7 nm oxides also implies that the buildup of defects does not play a significant role in SEGR. These data suggest that SEGR depends on J_{CR} only.

At the SISC, we will discuss the implications of SEGR in thin oxides on the reliability of electronics in space. We will also compare and contrast the SEGR mechanisms with hard and soft electrical breakdown in thin oxides.

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1. T. F. Wrobel, IEEE Trans Nucl. Sci. **34**, pp. 1262-1268, 1987.
2. C. F. Wheatley, J. L. Titus, and D. I. Burton, IEEE Trans. Nucl. Sci. **41**, pp. 2152-2159, 1994.
3. J. L. Titus and C. F. Wheatley, IEEE Trans. Nucl. Sci. **43**, pp. 533-545, 1996.
4. *The National Technology Roadmap for Semiconductors*, the Semiconductor Industry Association, 1997, p. 46.
5. F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt, P. E. Dodd, and G. L. Hash, IEEE Trans Nucl. Sci. **44**, pp. 2345-2352, 1997.
6. F. W. Sexton, et al., "Precursor Ion Damage and Angular Dependence of SEGR in Thin Oxides," submitted to IEEE Trans on Nucl. Sci. **45**, 6, 1998.
7. D. M. Fleetwood and N. S. Saks, J. Appl. Phys. **79**, pp. 1583-1594, 1996.
8. M. Y. Hao, et al., Appl. Phys. Lett. **66**, pp. 1126-1128, 1995.
9. B.E. Weir, et al., IEEE IEDM Technical Digest, pp. 73-76, 1997.
10. D. J. DiMaria, E. Cartier, and D. A. Buchanan, J. Appl. Phys. 80, 1, pp. 304-317, 1996.
11. M. Houssa, et al., Appl. Phys. Lett. **73**, 4, pp. 514-516, 1998.
12. E. Miranda, et al., Appl. Phys. Lett. **73**, 4, pp. 490-492, 1998.

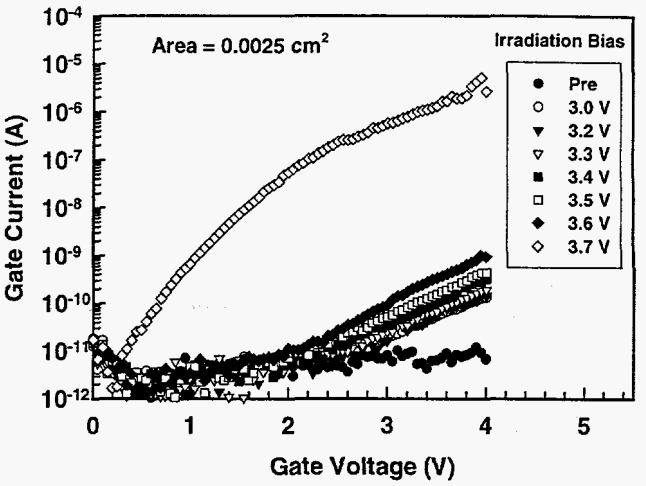

Figure 1: IV curves for a 7-nm SiO_2 capacitor as a function of exposure to a fluence of 360-MeV Au ions. Fluence per step was 10^6 ions/cm^2 and bias during each exposure is indicated.

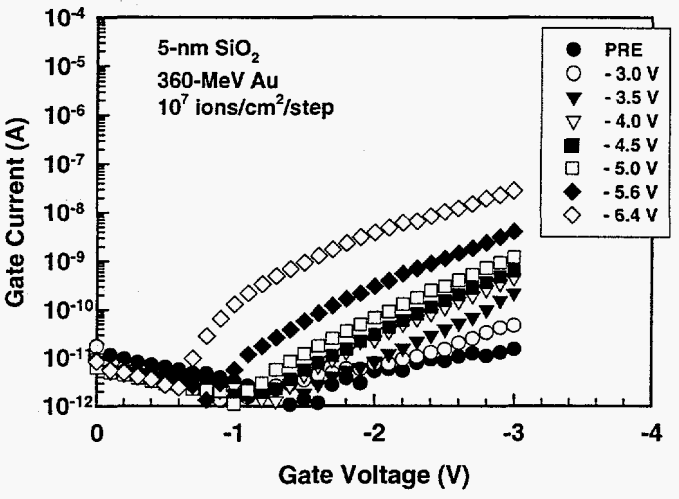

Figure. 2: Representative IV curves for a 5-nm oxide in which only damage was observed.

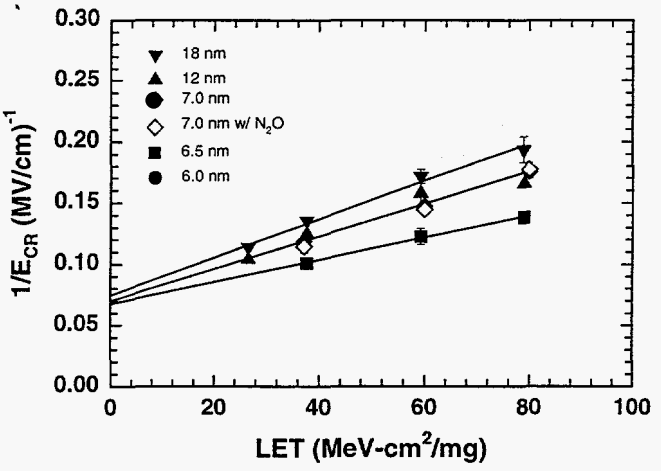

Figure 3: Inverse critical field to rupture as a function of ion LET and oxide thickness. Data for oxide thicknesses of 6, 6.5, 12, and 18 nm are from Ref [5]. Lines are fits to the data.