DEVELOPMENT AND INTEGRATION OF APPLIQUÉ DECOUPLING CAPACITORS

Terry J. Garino, D. Dimos and S. J. Lockwood
Sandia National Laboratories
Albuquerque, NM 87185-0333 USA

Abstract—For high-speed integrated circuit applications, it is important to interconnect decoupling capacitors and integrated circuits (ICs) as intimately as possible, to minimize parastic impedances. This can be achieved by mounting free-standing, thin film capacitors directly onto ICs as part of a chip-scale packaging approach. These "appliqué" capacitors utilize a chemically-prepared PLZT dielectric, which is nominally 1 μm thick. The small size and weight of appliqué capacitors can be used to improve packaging efficiency. Appliqué capacitors, which are initially fabricated on silicon wafers, have high permittivity ($\varepsilon \cong 1000$), low loss ($\tan\delta \cong 0.01$) and high breakdown strength ($E_B \cong$ 1 MV/cm) and leakage resistance ($\rho > 10^{14}$ Ω-cm @ 125°C). Various processes being developed to remove the capacitors from the silicon substrate and reattach them to ICs is described. In addition, a concept for interconnecting the capacitors using a repatterning process is discussed.

I. Introduction

Decoupling capacitors are essential elements in microelectronic circuits. They provide integrated circuits (ICs) with a nearby source of charge, which effectively decouples the IC from the power supply. This speeds up the circuit response and improves performance by lowering the interconnect inductance and, thereby, suppressing power line noise. In order to optimize the performance for high clock rate IC applications, it is necessary to minimize the interconnect distance between the decoupling capacitor and the IC. One approach to achieving this goal is to mount the capacitor directly onto the IC. To make such an on-die decoupling capacitor compatible with chip-scale packaging (CSP) approaches, the capacitor must be physically unobtrusive.

Thin films of ferroelectric perovskite materials have been developed for decoupling capacitor applications [1]. A thin film capacitor based on $Pb(Zr,Ti)O_3$ (PZT), with a single dielectric layer ~ 1 μm thick, can have a capacitance of 100 nF (a typical value for a decoupling capacitor) with an area of < 10 mm^2, due to its high dielectric permittivity (up to 1500). These films also maintain their high permittivities and low losses at frequencies above 1 GHz [2]. Furthermore, it has been shown that low leakage current densities (< 10^{-9} A/cm^2) and high breakdown strengths (>900 kV/cm) can be achieved at elevated temperatures (125°C) through donor doping with either lanthanum or niobium (~ 5 atom %) [3]. However, since thin film capacitors are fabricated on substrates (typically silicon wafers), the part thickness is much greater than the thickness of the active device, which is ~3 μm. To develop on-die decoupling capacitors, it is important to take advantage of this small active device thickness.

There are three possible ways to take full advantage of the compact size of thin film capacitors. First, the capacitor could be fabricated directly onto the IC. However, in the case of PZT, the minimum processing temperature of ~550°C exceeds the maximum processing temperature of a fully metallized IC (≤ 450°C). The situation is even worse for other perovskites, such as $(Ba,Sr)TiO_3$, which require higher firing temperatures. In addition, this type of process would only be appropriate for a 100% capacitor yield, since capacitor shorting would result in discarding the IC, which would be an expensive proposition.

The second way of optimally utilizing thin film decoupling capacitors is to fabricate them on very thin substrates. This approach was taken in earlier work, in which KOH back etching of silicon was used to form substrates with 25 μm thick membranes on which the capacitors were fabricated [4]. The substrates with etched membranes, which were significantly easier to handle than 25 μm thick Si substrates, yielded capacitor devices < 30 μm thick. However, for some packaging concepts, such as the one described below, 25-30 μm is still too thick.

Consequently, we have been developing a third approach to take advantage of the small, active device thickness. This approach uses standard Si micromachining techniques to enable the removal of thin film capacitors from the substrate after fabrication and the reattachment to a finished IC. This paper will describe several methods for fabricating these appliqué capacitors and a repatterning scheme for incorporating them with ICs in a CSP format .

II. Ferroelectric Film Fabrication

The decoupling capacitors were based on $(Pb,La)(Zr,Ti)O_3$ (PLZT) thin films, which were fabricated by chemical solution deposition [5]. The precursor solution was prepared by mixing the appropriate ratio of zirconium butoxide-

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butanol and titanium isopropoxide, and then adding acetic acid and methanol. Lead (IV) acetate (enough to give 10 mol % excess Pb to compensate for volatilization during heat treatment) and lanthanum acetate were then added. The solution was heated to 75°C to dissolve the acetates. Finally, water along with more methanol and acetic acid were added to give a 0.4 M solution.

The top and bottom electrodes consisted of platinum and were fabricated by sputtering. Both electrodes had to be relatively thick (~ 1 μm) to keep the equivalent series resistance and inductance to acceptable values. To improve adhesion and reduce hillock formation in these thick Pt films, sputter deposition was performed at elevated temperature (300°C) and a sputtered titanium adhesion layer was used for the bottom electrode [6]. Prior to metallization, a 0.3 μm layer of thermal oxide was grown on the wafers.

The capacitors were formed by spin coating the precursor solution onto the metallized wafers. Spinning was done at 3000 rpm for 30 seconds and the wafer was then heated at 300°C for 5 min to pyrolyze the film before repeating the process to deposit subsequent layers. Each layer had a thickness of about 0.1 μm after annealing at 650°C for 30 min where crystallization of the perovskite phase occurs. The high temperature anneal was done after every fourth layer was deposited until the film thickness reached 1 μm. Photolithography and wet etching were used to define the dielectric pattern following sputter deposition of the top electrodes through a shadow mask.

III. Appliqué Fabrication

To create free-standing thin film (appliqué) capacitors, the capacitors must be removed from the substrate, either by dissolving the substrate or by debonding the capacitor utilizing either a sacrificial layer or a mechanically weak interface. Methods based on each of these approaches have been explored. In addition, a fourth method that combines the first two approaches was also investigated. For all methods, the capacitors were fabricated on silicon wafers. This was done for three reasons. First, a process had already been developed and well understood for making PZT thin film decoupling capacitors on silicon. Second, polished silicon wafers of appropriate size are readily available at relatively low cost. Finally, and most importantly, "standard" Si micromachining techniques can be readily applied.

A. Substrate Dissolution Method

The first technique to fabricate appliqué decoupling capacitors involved simply etching away the substrate using a KOH etchant solution. The solution consists of 4 M KOH in deionized water at 85°C. During the etching process, the front side of the wafer is bonded to a silica plate using a special wax so that the capacitors are protected from the etchant solution. Wafers polished on both sides are required so that the etching takes place uniformly on the rapid etching (100) plane. However, it was found that complete dissolution of the substrate resulted in damage to the capacitors, presumably due to incomplete protection against KOH attack. Therefore, to obtain thin, functional capacitors, the etching time was carefully controlled to leave several microns of the Si substrate behind. However, precisely controlling the thickness of the remaining Si is difficult.

B. Sacrificial Layer Dissolution Method

The second method to make appliqué capacitors utilized the SiO_2 layer beneath the bottom electrode as a sacrificial etch layer. In this case, after fabricating the capacitors, the top surface of the wafer is bonded to a poly(methyl) methacrylate (PMMA) plate using cyanoacrylate. Individual capacitors are then cut out and placed in concentrated HF for ~30 min to dissolve the oxide, leaving the capacitors attached to the backing plate. The capacitors can then be bonded to a second substrate, which simulates an IC die, using an insoluble adhesive like epoxy or polyimide. The backing plate is then removed by dissolving the cyanoacrylate in acetone. This method requires handling lots of individual parts, but results in functional reattached capacitors.

C. Peel-Off Method

It is also possible to obtain marginal adhesion between the bottom electrode and the substrate, for example by eliminating the Ti adhesion layer. In this case, a sheet of metal foil can be bonded to the top of the thin-film capacitor wafer used a soluble, strong-bonding adhesive such as cyanoacrylate. Once the adhesive is set, the foil can be peeled from the wafer with the capacitors attached. The capacitors can then be individually cut out and bonded to an IC substrate using a insoluble adhesive such as polyimide or epoxy. Again, acetone is used to remove the backing foil.

D. Combined Dissolution Method

While each of the previous methods resulted in suitable free-standing thin film capacitors for on-die decoupling, a method more appropriate to batch handling and fabrication was desired. This method involves bulk etching of the Si substrate as well as the use of a sacrificial SiO_2 layer. In this method, 100 mm double polished (100) Si wafers with a 0.38 μm thick layer of buried oxide, which was located 3.2 μm below the top surface of the wafer, were used as the substrates (SIMOX, Ibis Technology Corp., Danvers, MA). The buried oxide layer served as both an etch stop for the Si

etching and as a sacrificial layer. Buried oxide wafers were used so that the capacitors would retain a few microns of Si on the back for added strength and protection.

The process flow for this method is illustrated in Fig. 1. The first step of this process was to etch a series of channels from the bottom surface of the wafer to the buried oxide layer using KOH solution (85°C). Silicon nitride is used as a hard mask for the KOH etching. For bulk micromachining, only Si_3N_4 formed by low-pressure CVD at ~ 800°C was acceptable. In contrast, reactively-sputtered Si_3N_4 (~ 500°C) exhibited significant damage during the time required to etch through the wafer thickness (~ 6 hr). However, sputtered Si_3N_4 may be suitable for the shorter etching times appropriate for surface micromachining. The pattern of channels was defined by a hexagonal array of square holes, which were formed in the bottom surface nitride layer using photolithography and plasma etching.

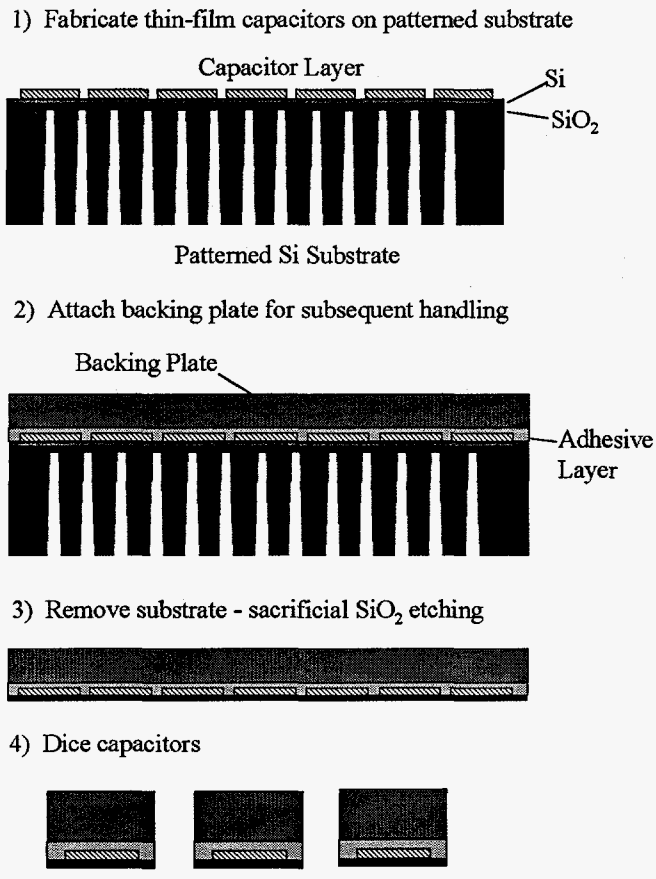

Fig 1. The process used to fabricate appliqué capacitors by combined etching of the substrate and the sacrificial oxide layer.

The size of the holes was calculated from the desired hole size at the buried oxide layer, the etching angle (~54°) and the thickness of the wafer. The desired hole size at the buried layer was estimated by determining the maximum size that a 3 μm thick membrane of silicon could be and still have the mechanical integrity to withstand the capacitor fabrication process. Calculations suggested that this size was roughly 0.2 mm, which requires a 0.87 mm hole in the nitride for a 0.475 mm thick wafer. The spacing of the holes is determined by the need for mechanical integrity and the desire to have the channels closely spaced to speed up the etching of the oxide. Therefore, to determine the optimal hole size and spacing, a design-study mask was made with the hole sizes from 0.8 to 0.96 mm and center-to-center spacings from 1.4 to 2.2 mm. Kinetic calculations indicated that the time needed to etch out the oxide from the channels for these dimensions should be comparable to that needed in method 2 to remove a single capacitor. Experiments are currently underway to optimize the etching conditions and determine the best hole sizes and spacings.

In these experiments, once the channels are etched into the wafer from the back side to the buried oxide layer, the capacitors will be fabricated on the wafer front side. A transparent polymeric backing plate such as PMMA will then be bonded to the front side using a soluble adhesive. The capacitors will then be diced and bonded to a substrate using polyimide (see Fig. 1). The soluble adhesive will then be dissolved to remove the backing plate leaving the capacitor upright on the second substrate. This technique will have several advantages. The capacitors will be removed at the wafer level and they should be well protected from the etchants by the 3 μm thick Si layer. However, it does require more steps and the fabrication of the capacitors on wafers that contain channels.

IV. Integration Scheme

One approach to incorporating thin film, appliqué decoupling capacitors into a CSP is by integrating them into a wafer repatterning process [7], as illustrated schematically in Fig. 2. The individual capacitors, which are tested prior to removal from the substrate, with their backing plates still attached, are bonded to the center of the top surface of an IC die using spun-on polyimide. The capacitor is bonded to the IC by partially curing the polyimide. The backing plate is subsequently removed with an appropriate solvent. A second layer of polyimide is then applied by spinning. Achieving good coverage of the capacitor with this polyimide layer dictates that the capacitor be no more than about 5 μm thick. The power and ground contacts for the die are connected to the capacitor as part of the repatterning process that redistributes the peripheral contacts into a 2-D array of solder bump contacts. The completed chip-scale package now contains an embedded capacitor but takes up no more space than a repatterned die without a capacitor.

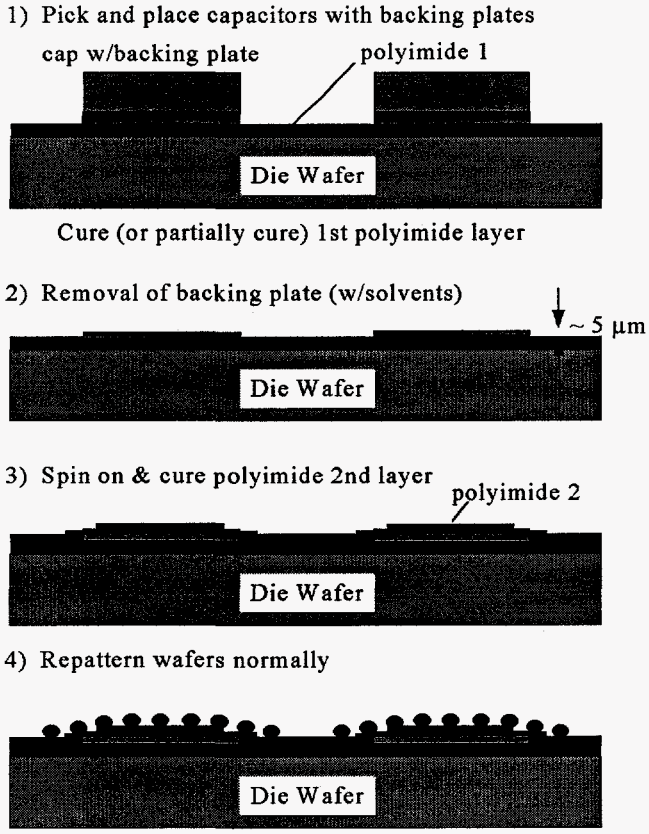

Fig. 2. A schematic depiction of a possible process for incorporation of appliqué capacitors on repatterned IC

V. Summary

Various techniques for fabricating ferroelectric thin-film appliqué decoupling capacitors have been investigated. The substrate dissolution method works, but is problematic since leaving a uniform and reproducible layer of Si a few microns thick was required, which was difficult to achieve. The sacrificial oxide method also worked, but the necessity of handling numerous small parts made the process somewhat awkward. The peel-off technique was a wafer level process and was, thus, more suitable to batch processing. However, this process relies on achieving controllably weak adhesion and has the further challenge that dicing the individual capacitors is difficult, since they are not visible when attached to the metal foil. The final technique of combined dissolution holds the most promise for commercial viability. However, additional work is still required to optimize the process steps and to address the costs of the process. Finally, a process for incorporating appliqué capacitors made by anyone of these techniques onto an IC die that meshes easily with the repatterning process has been described.

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