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IBM, ENDICOTT SECOND YEAR ANNUAL REPORT EXECUTIVE SUMMARY

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IBM Endicott, Assembly Process Design has completed the second year of development activity on DARPA TRP No. DE-FC-04094AL98817 for High Performance, Low Cost Interconnections for Flip Chip Attach. The second year of Endicott activity focused heavily on

1. Paste Deposition Process Development
2. Bonding Process Development

The bonding process development includes studies on flip chip encapsulation, thermal process modeling and reliability.

A brief summary of the objectives and key accomplishments follows for these two process efforts. Attached are detailed reports for deposition and bonding process development.

PASTE DEPOSITION PROCESS DEVELOPMENT

Summary

Objective: PMSP (Polymer Metal Solvent Paste) material must be deposited on a five inch wafer with 100% bump survival. The target geometry is 0.010" diameter, and 0.004" high with a flat surface.

Accomplishments: The photobumping process has been refined to yield bumps that are 0.010" in diameter and greater than 0.0035" high. The surface is flat and bonding results in a strong bond with no air entrapment between the chip bump and card pad.

Initial work with photobumping yielded a bump surface that was concave. In photobumping, 0.004" thick photoresist is imaged to create apertures. These apertures are filled with PMSP in two passes with a solvent drying process that occurs between the first and the second pass After the first pass filling, solvent from the PMSP interacted with the photoresist and caused the top surface, at the circumference of the aperture, to shrink. On the second pass filling, this slightly depressed surface fills up with PMSP. We call this blooming because the diameter of the bump is extended at the surface. When the photoresist is stripped, the thin surface extension of the bump diameter is folded over on top of the bump. This fold created a ridge at the circumference of the bump that would make initial contact with the card surface during bonding. The result was a high probability of air entrapment at the joint interface. The blooming problem was corrected by changing from an aqueous to a semiaqueous photoresist that was more solvent resistant. Flat surface bumps are made with 100% yield on five inch wafers. Double layers of 0.002" photoresist are used to define the nearly 0.004" high bumps. Work is in progress to use single layers of 0.003" and 0.004" photoresist. A single layer should eliminate perturbations from a straight side wall profile that exist near the interface of a double photoresist layup.

BONDING PROCESS DEVELOPMENT

Summary

Objective: The objective of the bonding process development effort is to identify the significant process variables that influence bond strength and fracture. Reliability tests will be used to verify electrical and mechanical integrity. Process optimization will use the Response Surface Analysis (RSA) experimental procedure to identify the fastest bond cycle that can be used to produce reliable joints.

The initial round of reliability tests of chips to cards demonstrated that it was possible to have PMC (polymer metal composite) interconnects survive reliability stress testing with stable contact resistance. However, unstable joints were also observed and were attributed to weak adhesive bonds that fail adhesively and air entrapment at the chip bump to card pad interface. The air entrapment was caused by the concave bump that was already described. Underfill material wicks into the weak interface between the bump surface and card, reducing contact area and mechanical strength. This problem is further compounded when air entrapment exists from the concave surface of the bumps. As mentioned, a semiaqueous photoresist is used to eliminate concave bumps and air entrapment. The weak adhesive interface was eliminated by making a PMSP/PMC material change. The adhesive fracture mode was changed to cohesive in tension and increased from 1000 psi to over 4000 psi. A second round of photobumped chips to cards was assembled for reliability tests. A fourth test was added to the three tests that were conducted during the first round:

1. 0 to 100 C, thermal cycle
2. 125 C, temperature age
3. 85 C/80% RH, temperature and humidity
4. -55 to 125 C, thermal cycle

No contact resistance failures have been observed after 1500 cycles, 1000 hours, 1000 hours and 1000 cycles respectively of the above stresses. These results are very encouraging. One more improvement to be made over these first two test sets is to increase the bondline of just less than 0.002" to greater than 0.003". The Universal Instrument prototype bonder will provide the necessary low level force control during bonding to achieve thicker bondlines that exceed 0.003". Previous work with finite element modeling of solder joints between flip chips and laminates indicated that the underfill begins to lose some of its benefit when joint thicknesses go below 0.003".

After demonstrating that a PMC bump design can survive the rigors of reliability tests, the focus moves to developing a fast bonding process suited to manufacturing. In addition to designing and building a fast prototype bonder, a thermal transient model has been developed and verified. This model can be used to predict temperature profiles given heat inputs to the card and chip. It has been shown that most of the heat needed to bond a bumped chip to a card can be driven in through the chip. Only a small volume of card is heated: the surface area of the chip site and only half of the card thickness. Preheating the card to a temperature of 120 C can have the effect of reducing the bond cycle as well as reducing the potential of card thermal gradients that would cause card warpage.

Future work for bonding will use the Universal Instrument prototype bonder along with the thermal transient model to optimize the responses of fracture mode, fracture strength, contact resistance, reliability and bond cycle duration.

BONDING PROCESS DEVELOPMENT

Material Properties

Objective: Mechanical testing is being used to quantify the bulk material strength as well as other properties which can be entered into finite element models for various simulations. Controlled experiments can also be run to study the effects of various bonding conditions.

Accomplishments: Testing consists of 0.125" diameter pegs which are bonded together with the electrically conductive paste using a rapid heating bonder from UIC as discussed in the earlier reports. A DOE was performed to investigate the effect of bonding temperature and pressure as well as the effect of surface roughness of the pegs, on the fracture strength of the ECA. Average failure stress was about 1100 psi. but a large standard deviation negated the possibility of statistically significant differences between the various sub-categories. Two observations were made. First, the failure mode was always adhesive (interfacial). This is not good news from the standpoint of stress intensity concentrations and fatigue failure. Second, there was a "starter crack" between the PMC material and the unscreened peg around the outside of the bond due to the slightly convex shape of the PMC as deposited on the screened peg. This gave a preferred failure site for the peg samples and probably resulted in the large standard deviation.

Subsequently, a modified version of the PMC, Paste C, was formulated by IBM Yorktown in order to increase the interfacial strength. This modified version performed much better than the earlier material with failure stress in tension of well over 4000 psi, and a tight (10%) standard deviation. In addition, the failure mode was cohesive in nature. This high failure stress is comparable to the 5000 psi failure stress of the solder. In addition to the PMC formulation change, improved cleaning methods, raising the bonding temperature (to 240°C from 220°C), and screening both pegs to eliminate "starter crack", contributed to the higher and statistically robust failure stress of the ECA.

To establish a failure envelope, the conductive adhesive was tested under different loading conditions, in tension/compression and shear. This was accomplished by screening the PMC on angled (15, 30, 45°) pegs and fracturing the bonded pegs either in pull or in compression. With increasing the loading angle from 0-45° the failure stress of the adhesive increased. Also, the failure stresses in compression were higher than in tension. The following table summarises the failure stresses and the modes, at the various loading conditions. The results are an average of 20 or more samples per test condition.

Phase (loading) Angle	Failure Stress (mode) in Pull, *psi*	Failure Stress (mode) in Compression, *psi*
0°	4,100 (cohesive)	N.A.
15°	3,985 (cohesive)	Not Evaluated
30°	4,140 (mostly cohesive)	10,096 (adhesive)
45°	5,093 (partial adhesive)	8,638 (adhesive)

This failure stress data is now being analyzed to construct the failure envelope for the conductive adhesive. In addition, displacement controlled fatigue tests will be carried out on the ECA bonded to the 0° pegs, at various loads and frequencies. The fatigue and the fracture data along with the bulk material properties of Young's modulus, % elongation, CTE of the material will be used to predict the long term reliability of the ECA interconnects.

Chip Bonding

Objective: The objective of chip bonding is to test the effect of various parameters such as bump height and encapsulant on the t-zero joint quality.

Accomplishments: Several test chips have been bonded, encapsulated to test cards, and are stressed in the reliability tests. A set of bonding parameters has been established for chip bonding to card, on Research Devices bonder at IBM and the UIC chip bonder. The initial card warpage during bonding was controlled by heating the card to 120°C (below it's T_g), and heating the chip to 240-260°C. A transient thermal model was also developed which verified the chip and the card heating during the bonding cycle. A very small volume of the card, under the chip, heats up to the bond temperature 225°C, while the rest of the card sets at 120°C. The heated volume is the size of the chip in area and about half the card thickness for a 2S0P card. The ability to heat this minimal volume to accomplish the bonding supports the concept of very rapid heating through the chip. Based on this localized heating predicted by the thermal model, and the rapid heating capability of the UIC chip bonder, we will be able to accomplish the short (10 second) bond cycles.

To investigate the effect of various bonding parameters, a DOE was performed with the following predictor variables: bump height, bonding pressure, "hole fill method" (either supplemental dispense or bump flatten), and encapsulation method (either no encapsulation, Matsushita, or Hysol 4511). Results showed that the encapsulation process was very destructive to joint integrity with the most damage produced by 4511. A second experiment with chips bonded to glass slides revealed that the encapsulants wicked into the interface between the bumps and glass slide producing damage. It is thus believed that any imperfect connection between the bump and pad (such as fissures, cracking, etc.) along with the weak interfacial strength of the material gives rise to the encapsulant wicking phenomenon and makes it very difficult to achieve consistently good joints. Also, the weak interfacial strength, even if it doesn't lead to encapsulant wicking, gives rise to an adhesive failure mode which would open the door to defect-driven catastrophic failure. Increasing the adhesion strength of the material in order to promote a "more forgiving" cohesive failure mode was therefore desired.

The need for improved (high) adhesive strength was addressed by the modified version of the PMC, Paste C, developed by IBM Yorktown. This new PMC formulation resulted in higher failure stresses and a highly desired "cohesive" failure mode as discussed in the earlier section. When the chips photobumped with the Paste C were bonded to glass and encapsulated with various encapsulants, no wicking of the encapsulants was observed. A group of cards was then assembled with Paste C bumped chips, encapsulated, and put on the reliability stress tests. No electrical failures have occurred in 1200 thermal cycles (-55 to 125°C), 1200+ hours of 85°C/85% RH, and thermal age at 125°C.

To yield a void-free and rapid encapsulation of flip chips, a bondline of 2.5 to 3 mils is desired. The ECA bonding parameters used in our study generally resulted in a 1.7 - 1.9 mil gaps for encapsulation. The higher encapsulation (bond) gaps, up to 2.4 mils, were achieved by decreasing the bond pressures from 150 psi to 75 psi on research devices. Lowering the bond pressure did not affect the ECA adhesive strength. When photobumped chips were bonded to Au plated Cu slugs at 75 psi and 150 psi, and stud pulled, the bond strength remained stable at around 7 lbs of pull force. Also, these chips exhibited cohesive failure of the bumps in the stud pull test, substantiating the failure mode of the new PMC on Au/Cu pegs discussed in the earlier section.

Reliability

Objective: The objective of the reliability testing is to investigate the overall joint stability of the PMC material as a function of time and in particular, to monitor the stability over time as a function of the t-zero joint resistance.

Accomplishments: Significant advances have been made since Spring 1996 in achieving high reliability conductive adhesive joints that exhibit no failures in 1200 thermal cycles (-55 to 125 °1200+ hours of 85°C/85% RH exposure, and thermal age at 125°C. The modified conductive adhesive paste, paste C, was used to photobump blanket (Au plated) chips, bonded to 2S2P cards, encapsulated with 2 different underfills, and tested in the reliability stress tests. The contact resistance (CR) of the assembled cards is monitored to assess the ECA joint stability as a function of stress test time/cycles and compared to the t-zero contact resistance. The actual changes in the contact resistance are less than 10 mΩ, most of which can be attributed to the variations in the ambient temperatures at the time of measurements. The table on the following page shows t-zero contact resistance, and the changes (delta) in the CR for representative, Dexter 4511 encapsulated cards, through the reliability stress tests.

In the past, our photobumped chips had a concave surface on the bumps. These concave bumps trapped air during bonding resulting in higher contact resistance values. The improvements in the screening process and the use of better photoresist materials coupled with bump flattening prior to assembly have now resulted in very uniform and flat conductive bumps.

The encouraging reliability performance of the ECA and the improved processing know how will be coupled to bond photobumped chips with a stitch pattern to cards and test in the reliability tests. Eight mil bumps with a 20 mil pitch chips will be bonded to 2S2P cards and stressed in the reliability tests.

Contact Resistance of the ECA bumped chips at t-zero, and the changes through stress tests

Card # 4

CR at t-zero	Delta CR (mOhms) at # temp. cycles (-55 to 125 C)					
mOhms	169	463	631	802	1021	1217
54.90	0.01	-0.21	-0.46	0.36	-0.03	-0.07
54.70	-0.22	-0.88	-0.95	-0.18	-0.64	-0.70
58.20	0.01	-0.56	-0.64	0.17	-0.60	-0.45
56.60	-1.02	-1.45	-1.58	-0.86	-1.48	-1.22
99.60	-0.64	-0.78	-0.31	1.19	0.29	0.40
107.50	0.07	-1.07	-1.45	-0.37	-1.46	-1.68
50.70	-1.60	-1.17	-1.24	-0.34	-0.45	-1.03
56.00	-1.02	-1.28	-1.48	-0.67	-1.45	-1.32
56.40	-1.01	-2.09	-2.57	-1.85	-2.74	-2.56
48.90	-0.47	-0.28	-0.53	0.26	-0.29	-0.34
95.60	-2.89	-3.36	-4.02	-2.87	-3.72	-3.96
103.60	-2.82	-4.69	-5.40	-4.91	-6.43	-6.70
58.00	-1.30	-0.66	-0.01	0.68	0.24	-0.58
103.40	-2.34	-3.40	-3.85	-2.79	-4.03	-4.65

Card # 7

CR at t-zero	Delta CR (mOhms) at hours in 85 C/85% RH			
mOhms	305	489	776	989
57.60	-0.69	-0.67	-0.23	-0.70
51.20	-1.20	-1.21	-0.87	-1.27
49.30	-0.48	-0.50	-0.11	-0.42
51.70	-0.73	-0.67	-0.30	-0.64
97.80	-1.57	-1.54	-1.06	-1.93
102.70	-1.52	-1.45	-0.93	-1.94
52.10	-1.07	-1.23	-1.25	-1.90
51.90	-1.88	-1.99	-1.71	-2.36
52.90	-0.52	-0.43	0.08	-0.43
51.80	-1.17	-0.88	-0.83	-1.32
97.00	-2.36	-2.61	-2.84	-4.35
107.40	-2.12	-2.03	-1.89	-3.30
50.80	-1.53	-1.50	-1.33	-2.11
97.70	-1.96	-2.30	-1.79	-3.13

Card # 10

CR at t-zero	Delta CR (mOhms) at hours in thermal age (125 C)			
mOhms	169	463	631	802
59.60	0.24	0.16	0.25	0.02
59.20	0.56	0.38	0.82	0.40
55.40	0.22	0.03	0.50	0.22
56.80	-0.20	-0.26	-0.09	-0.24
104.50	0.74	0.49	0.95	0.52
114.00	0.73	0.70	1.46	0.97
60.90	0.58	0.58	1.18	0.87
63.00	0.55	0.42	1.21	1.05
59.90	0.50	0.58	1.22	0.96
58.70	0.46	0.45	0.64	0.57
132.00	1.08	0.68	1.55	0.97
131.30	1.31	0.79	1.62	1.00
75.30	0.65	0.36	0.99	0.30
109.20	0.74	0.06	1.13	0.24

PASTE DEPOSITION PROCESS DEVELOPMENT

Objective: The objective of the paste deposition process effort is to identify the significant process variables as well as photoresists that influence deposit survival and flat PMC surface. Design-of-experiment (DOE) is the method used to determine the importance of each variable.

The IBM Corporation and Universal Instruments Corporation are collaborating on an ARPA contract to develop a high performance, low cost interconnect for flip chip using electrically conductive adhesive,(1). The scope includes four areas of focus:

1. Development of an electrically conductive adhesive material
2. Development of a process to deposit the conductive material and define chip bumps
3. Development of a process to bond a bumped chip
4. Development of a chip bonder to pick, align and bond the bumped chip to a carrier.

This research report will concentrate on development of a process to deposit the conductive material and define chip bumps. Process development is done at Assembly Process Design of IBM,Endicott. Thermoplastic electrically conductive adhesive is chosen as a solder replacement since it offers benefits in the areas of reworkability, low modulus, low joint stress, environmental and shelf-life stability. A novel approach using photoresist has been used to deposit the conductive material. The use of photoresist as a stencil can eliminate mechanical forces that impart mass variability as well as introduce air during stencil parting. Advantages of the photoprocess include better geometry definition and control of shape and height. Several deposition experiments have been completed with traditional stencil screening. The result was air entrapment in the deposits that was caused when the stencil was removed. The paste would stretch as the stencil was removed and eventually snap back. A pocket of air frequently was trapped as the adhesive snapped back. The novel isotropic electrically conductive adhesive paste used in this research project was developed at T. J. Watson Research Center,IBM. The paste is composed of thermoplastic binder, silver particles, and solvent. The filler concentration is approximately 80 weight%. The rheological behavior of the paste was determined using a cone-and-plate viscometer. The IBM-paste exhibits thixotropic and pseudoplastic behavior which is good for screening. Shear thinning is desirable for polymer flow during screening and the viscosity returns to a higher value when there is no shear force. The use of ECA as a solder replacement was first developed by screening IBM-paste on copper panels through a conventional stencil. The applied paste was dried at 70 degree C for 30 minutes. This technique yielded many empty holes, air voids and irregularly shaped deposits. Next, paste deposition process development was done using the photobumping process on a copper panel with a 6 x 6 chip matrix with dots ranging from 0.01" to 0.005" in 0.001" increments. This process made use of a photoimagable photoresist to form a via-hole. The dry-film negative-acting photoresist, CFI, was used as the imageable photoresist. The chemistry of this photoresist is well known in the literature(2). The thickness of photoresist was 0.003 inch obtained by double laminates of 0.0015 inch resist. The hole diameters varied from 0.005" to 0.01" on 0.020" pitch. The IBM paste was then screened into these holes and the applied paste was dried at 70 degree C for 30 minutes. Next, the photoresist was stripped. The result of this work was not satisfactory because of low deposit survival and a concave deposit surface. Air entrapment as well as high stress at the joint can be generated with a concave deposit surface during bonding.

Process enhancements were needed to achieve a 100% deposit survival and a flat deposit surface. Design-of-Experiment(DOE) was used to identify the significant process variables as well as photoresists that influence deposit survival and flat deposit surface. An 8 trial, 3 variable DOE was run on a silicon wafer that had blanket metal deposition of palladium using the photobumping process. Figure 1 shows the process flow of photobumping on the wafer(3). Dry film Riston 4720 photoresist was used. Riston 4720 is manufactured by Dupont. The thickness of photoresist was 0.004 inch and was obtained by double laminates of 0.002 inch resist. The 10X20 glass artwork was used. The hole diameters were 0.010" on 0.020" pitch. An expose level was 100 mJ/cm^2 (Tamarack machine). Sodium carbonate was used as a developing solution. The extrusion head used in the screening process is made of steel. It is driven by air pressure against a cylindrical piston. The IBM paste extrudes out of a slit formed by two thin metallic blades. The edge of the thin metallic blade is made at a certain geometry in order to conform to the surface topography of the photoresist. The blade contacts the photoresist directly. The screening process used 21 lbs of injection head downward force, 14-15 psi injection feed pressure and 0.15 inches/sec head speed. The variables included

1. Expose Dose: 1, 2 passes
2. Develop: 1, 2 passes
3. Baking Temperature: 25 degree C for 24 hrs, 50 C for 0.5 hrs.

The response after stripping photoresist was deposit survival. Some sensitivity was lost from the DOE because samples number 2 and 8 had to be canceled out. The resist stripper(NaOH) was too strong and completely removed the deposits and resist. Some observations were made:

1. The stripper, S-1100X, is compatible with Riston 4720. It gives 18%,23% and 27% yields on sample numbers 3, 5 and 6 respectively. Sample numbers 1, 4 and 7 had only 1-2 deposits missing. S-1100X is manufactured by Dupont and is composed of 10-30% Ethanolamine and 60-100% Butyl carbitol.
2. More deposits survived at baking temperature of 50 C for 0.5 hr. than at room temperature for 24 hours. Residual solvent after room temperature bake for 24 hours may be the reason for poor adhesion.
3. Expose dose and developing time seemed to be critical parameters for resist via formation.
4. Deposits had a slightly flatter surface rather than concave as was obtained in the previous DOE.

The result from DOE# 2(appendix 1) showed that baking temperature as well as expose-develop are the important parameters in achieving 100% deposit survival and flat deposit surface.

New types of photoresist with different chemistries were evaluated based on the results of DOE# 2: T168(solvent processed resist), AX(semi-aqueous resist), and GA40(aqueous resist). Solvent processed resist is typically used as an additive plating photoresist. It is developed in propylene carbonate and stripped in hot propylene carbonate. Semi-aqueous resist is more solvent resistant than aqueous photoresist. Semi-aqueous resist was evaluated for gold plating. Semi-aqueous resist is developed in Riston II developer(butyl cellosolve and sodium tetraborate) and stripped in S-1100X. Aqueous resist GA40 is similar to Riston chemistry based on HPLC data,(4). It needs to be developed in an aqueous system-sodium carbonate and stripped in S-1100X. Four types of thermoplastic isotropic electrically conductive adhesives included high filler and low filler version of IBM paste, Diemat and Staystik. The last two ECAs are commercially available adhesives. The results showed that photoresist AX2.0 and high

filler IBM paste(paste A) yielded perfect deposit survival and a flat deposit surface,(Fig. 3). GA40 photoresist gave similar results to Riston 4720.(Fig. 2) Low filler IBM paste, Diemat and Staystik paste did not perform well in either GA40 photoresist or AX photoresist. This may be caused by the residual solvent in the paste causing poor adhesion. The baking temperature needed to be optimized for these pastes. No deposits survived the T168 photoresist because of the strong alkaline stripping environment. Cross-sections were done on these samples(Fig.4). Photoresist AX gave the best result for side-wall profile. It showed slight undercut which is preferred to enhance adhesion of ECA to wafer.

Positive photoresist(Microposit SJR 5440) manufactured by Shipley Company was also evaluated. The difference between negative and positive photoresists is that in negative resists the irradiated areas are less soluble in the developer. In positive photoresists, irradiated areas are more soluble and are removed by the developer. Microposit SJR 5440 had 34% solid and the rest as propylene glycol methyl ether acetate. Positive photoresist was spin coated at 500 rpm to obtain 15 microns thickness. It was then baked at 80 C for 20 minutes to evaporate the solvent followed by expose using a Mercury Lamp at 500 watts. The positive photoresist was developed with 0.25 N KOH at 22-25 C, followed by rinsing with DI water. After the develop process, the sample was screened. Blanket expose without the artwork was done to prepare the photoresist for stripping in 1 N KOH(aq). The result showed all deposits survived. However, spin coating limits thickness buildup to less than 0.001". Therefore, a deposit height of 0.004" could not be achieved.

Photoresist AX was chosen as a candidate to further study the photobumping process because of 100% deposit survival and a flat deposit surface. Further experiments were done on AX photoresist to determine the range for expose dose. The result from DOE# 2 showed that expose, develop and baking temperature are critical parameters. Four levels of expose dose were 50, 75, 100 and 125 mJ/cm^2. Two levels of develop were 1 and 2 passes. The same ECA pastes used previously, were used except Diemat was replaced with a modified IBM-paste(paste C). Many conclusions can be made from this experiment. Both high level of expose dose(125 mJ/cm^2) and over develop(2 passes) give an excellent result in terms of deposit survival and flat deposit surface for the two IBM pastes. High levels of expose doses gave a straight sidewall profile in the photoresist and over develop gives a slight undercut. The low filler level and high polymer content may be the reason for difficulty in stripping of the IBM-paste with 60 weight% filler. A low level of expose dose gives deposits with poor shape due to an irregular sidewall profile in the photoresist. Riston 4820 was suggested by the supplier to have a better solvent resistance than Riston 4720. Riston 4820 which is in the same family of Riston 4720 was exposed and developed using the same condition as AX photoresist. The results showed that excellent deposit survival could be obtained with Riston 4820. A flat deposit surface could not be obtained, however based on the cross-section result of over developed AX and Riston 4820 photoresist(Fig. 4 & 5). Less stress concentration at the base of deposit can be obtained with AX photoresist because undercutting AX photoresist allows the ECA deposit to form a tree trunk like base.

Doe#3 was used to optimize expose dose and develop time and looked at the effects of plasma treatment. Two IBM pastes, A and C were evaluated. Deposit survival was the main response. A 4 trial, 2 variable Design-of-Experiment was run on a silicon wafer that had a blanket metal deposit of gold. Dry film AX was used as the photoresist. The thickness of photoresist was 0.004 inch, obtained by double laminates of 0.002 inch resist. The screening process had 21 lbs injection head downward force for IBM-paste

A, and 32 lbs for IBM-paste C with head speed of 0.15 inch/sec. The injection feed pressure was 14-15 psi. The expose level was 125 mJ/cm^2 with two pass develop.
The variables for DOE# 3 included:

1. Plasma treated, no and yes
2. IBM-paste type A and C

The response after stripping photoresist was deposit survival. These observations were made:

1. IBM-paste C is more viscous than IBM-paste A, and IBM-paste C drys faster than IBM-paste A.
2. Higher downward force is needed to screen IBM-paste C versus IBM-paste A.
3. An excess of pastes of A and C at the edge of wafers was caused by the difference in thickness of the wafers and the fixture. This lot of wafers was 3000 angstroms less in thickness than the previous lots, therefore the wafers are not at the same level as the fixture.
4. The dull surface of photoresist was caused by a low expose dose of photoresist.
5. The difficulty in stripping is caused by paste blooming at the surface. The extra paste film deposit can be removed with water wash.

The result of DOE# 3 shows that there is no difference in deposit survival between plasma treatment and no plasma treatment. IBM-paste C seems to perform better than IBM-paste A in terms of deposit survival. The level of the fixture and wafer is a very important parameter in screening. In order to obtain good screening, the wafer level has to be slightly higher than the fixture level. The percentage of deposit survival(80-90%) should be 100% if the wafer and the fixture are the same level. The deposits from DOE# 3 were sent to the mechanical testing department at IBM,Endicott to determine the deposit shear force. The result showed that IBM-paste C(1108 Psi) had a higher deposit shear force than IBM-paste A(567 Psi).

The result from DOE# 3 was satisfactory at this points, photoresist work was done on silicon wafers that had blanket metal deposition of palladium or gold. No photoresist work was done on polyimide. It is important to have the photobumping technique work on polyimide because polyimide is used as a passivation layer in a real chip. A silicon wafer that had a blanket metal deposition of gold was spin coated with adhesion promoter,Alpha-aminopropyl triethoxy silane(A-1100) at concentration of 5% in methanol at 3000 rpm for 1 minute. The wafer was baked at 110 C for 10 minutes. Then it was spin coated with polyimide 5878 at 3000 rpm for 1 minute. The sample was dried at 120 C for 10 minutes in conventional oven, then cured by baking at 360 C for 1.5 hours in nitrogen. Two layers of photoresist AX2.0 were double laminated on the wafer with blanket polyimide. The expose dose was varied from 75 mJ/cm^2 to 250 mJ/cm^2. After develop, IBM-paste C was screened, the resist was stripped and deposit survival examined. Some observations were made:

1. Sample with 75 mJ/cm^2 exposed level has a dull surface, and it was attacked by the developer.
2. Sample with 125 mJ/cm^2 exposed level also had a dull surface
3. Sample with 200 and 250 mJ/cm^2 exposed level has a shinny surface.
4. There is less paste blooming in the sample with the shinny surface

The result from this experiment showed that photoresist and ECA(IBM-paste C) adhere well to polyimide. Proper expose and develop level can yield 100% deposit survival. Expose levels in the range of 200 mJ/cm are preferred to obtain good screening.

Next, the stitch pattern wafer was used to determine the range of expose level in order to confirm the result of this experiment. A stitch pattern wafer was prepared in Yorktown with 10 mils diameter pads and four microns thick polyimide. Dry film AX was used as

the photoresist. The thickness of photoresist was 0.004 inch. The screening process had 32 lbs injection head downward with head speed of 0.15 inches/sec. The injection feed pressure was 14-15 psi. The wafer was divided into four quarters. The first quarter was exposed with 125 mJ/cm^2. The second quarter was exposed with 175 mJ/cm^2. The third quarter was exposed with 225 mJ/cm^2 and the last quarter was exposed with 300 mJ/cm^2. These parts were developed with two passes. Many observations were made:

1. It is very difficult to register the mask to the stitch pattern wafer because the color of photoresist is very dark. This causes misalignment between the pads and the vias.
2. Low expose level of 125 mJ/cm^2 and 175 mJ/cm^2 give a dul l surface.
3. High expose levels of 225 mJ/cm^2 and 302 mJ/cm^2 give a shinny surface.
4. There is less paste blooming on the shinny surface.
5. Low expose level samples are easily attacked by the developer.
6. Via opening decreases with higher expose levels.

Exposed level(mJ/cm^2)	Via opening(mils)
125	10.48
175	10.50
225	10.32
302	9.54

The results of this experiment are consistent with the results from the previous experiment. There is less paste blooming with a shinny surface. Figure 6 showed that deposits were larger than the pads at a low expose level and aligned well with the pad at high expose level.

Initial results for IBM Paste C showed drying during the screening process that prevented complete bump formation. IBM-paste D, is a modification of paste C. The trial run of paste D was done on a glass and a silicon wafer that had a blanket metal deposition of palladium. Dry film AX20 photoresist was used. The thickness of photoresist was 0.004 inch, obtained by double laminates of 0.002 inch resist. The 8x20 and 10x20 glass artworks were used. The hole diameters were 0.008" on 0.020" pitch and 0.010" on 0.020" pitch respectively. The expose level was 225 mJ/cm^2(Riston PC Printer 13 by Dupont). The screening process had 21-27 lbs injection head downward force with head speed of 0.15 inch/sec. The injection feed pressure was 14-15 psi. The orientation of fixture to screening direction was also studied in this experiment. The result showed no difference in 0.010" on 0.020" pitch with the screening direction of either 0 or 90 degree to fixture orientation. In the smaller feature, 0.008" on 0.020" pitch, the orientation of fixture to screening direction becomes critical. The zero degree orientation of fixture to screening direction gave a better result in terms of filling the via-hole. Overall, IBM-paste D has a better performance in terms of rheological behavior and screening than paste C. It does not dry before the completion of screening process.

Next, the expose range and develop for smaller feature(0.008" on 0.020" pitch) were studied. Dry film AX20 photoresist was used. The same lamination and screening processes as well as screening process were used as in 0.010" on 0.020" pitch feature. The expose levels were varied from 150 mJ/cm^2 to 300 mJ/cm^2. Many observations were made:

1. No difference in the shape of the via-hole between 0.008" on 0.020" pitch from 0.010" on 0.020" pitch.
2. Little change in shape of via-hole from 150 mJ/cm^2 to 300 mJ/cm^2.
3. Low expose level of 150 mJ/cm^2 gives a clean stripping with no residual left on the surface
4. There is less paste blooming on all samples.

The results of this experiment show that smaller features (0.008") do not require as high of an expose level as the 0.010" features. The cross-section of the chip shows that develop process needed to be optimized to obtain a tree trunk like base. A 100% deposit survival and a flat deposit surface were obtained from this experiment.

The stitch pattern wafer with 9 mils diameter pads (0.010" on 0.020" pitch 2 level design) was screened with IBM-paste D using the same process of lamination as in the previous experiment. The expose level of 150 mJ/cm was used. The result showed that in the first run, 100% deposit survival and a flat deposit surface were obtained. The experiment was repeated to confirm the result. The second run, less than 50% deposit survivals were obtained. Many observations were made:

1. Paste D did not flow nicely as in the first run. This may be caused by an increase in viscosity of paste D due to solvent evaporation.
2. Paste D did not come out from the squeegee uniformly, resulting in incomplete via hole filling.(see Fig. 7)

New photoresist PT30 was evaluated to solve the irregular sidewall profile problem. The desired result is a tree trunk like base and straight sidewall. PT30 photoresist has similar chemistry to AX20 photoresist. The only difference between the two is the thickness. PT30 photoresist is 0.003 inch thick therefore it does not need to be double laminated like AX20 photoresist which is 0.002 inch thick. PT30 photoresist is a semi-clear film. Therefore, it is somewhat difficult to detect the residual photoresist at the base of the via-hole after develop. PT30 photoresist has the same set-up of lamination only with single lamination. The expose level of 150 mJ/cm^2 was used. The results were no paste blooming on the surface, 100% deposit survival and a flat deposit surface. The cross-section showed a straightened sidewall profile with a tree trunk like base.(see Fig. 8) The problem with PT30 is that it may not give a bond line of 0.002 inch after bonding. Future work includes evaluating a new photoresist(solder mask) that is 0.004 inches thick and further refinement to the screening of 0.008 inches features on a stitch pattern wafer to get 100% deposit survival and a flat deposit surface.

References

(1) M. Gaynes, IBM-ARPA Technical Review, 1996

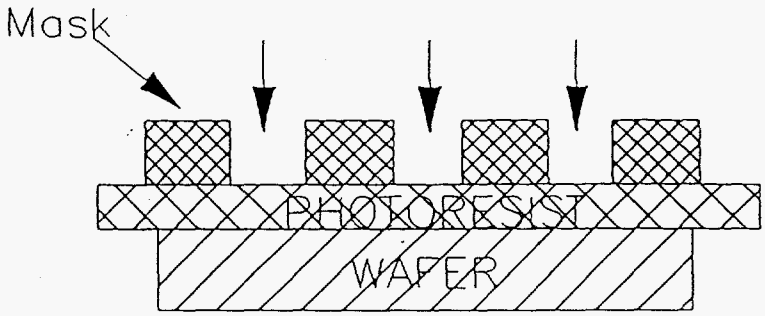
(2) A. Reiser,"Photoreactive Polymer: The Science and Technology of Resists", A Wiley-Interscience publication, NY., 1990, pp. 22

(3) M. Pierson, IBM-ARPA Technical Review, 1996

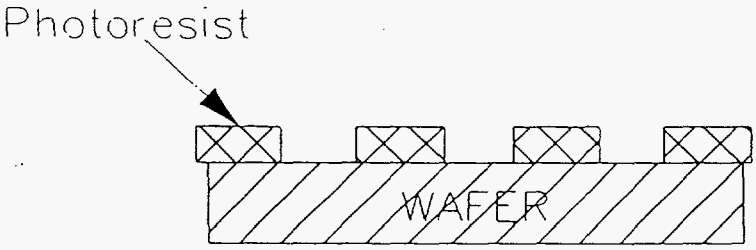
(4) S. Fuerniss, unpublished data, March 1996

1. Add Photoresist to Wafer

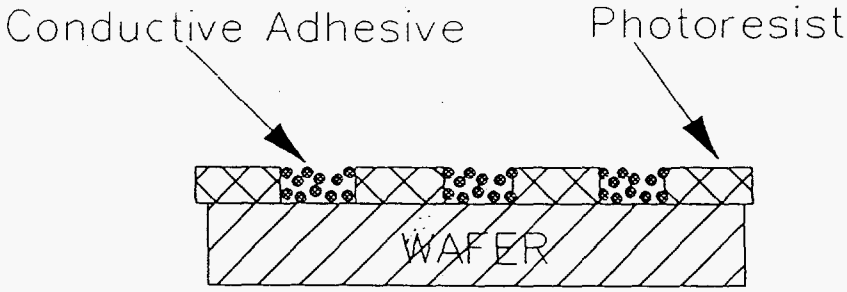
2. Place Photo Mask on Photo Resist & Align to Features on Wafer & Expose



3. Develop Photoresist



4. Screen on Conductive Adhesive & Dry Solvent (Until ECA is Solid)



5. Strip off Photoresist (Clean Surfaces)

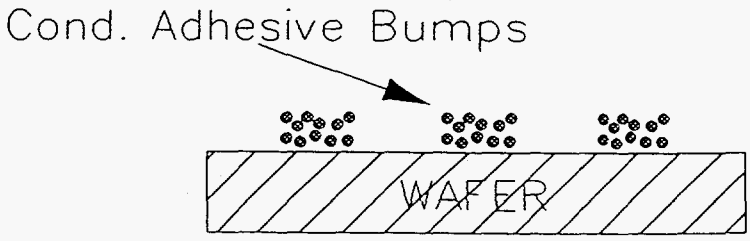


Fig. 1 Process Flow of Photobumping

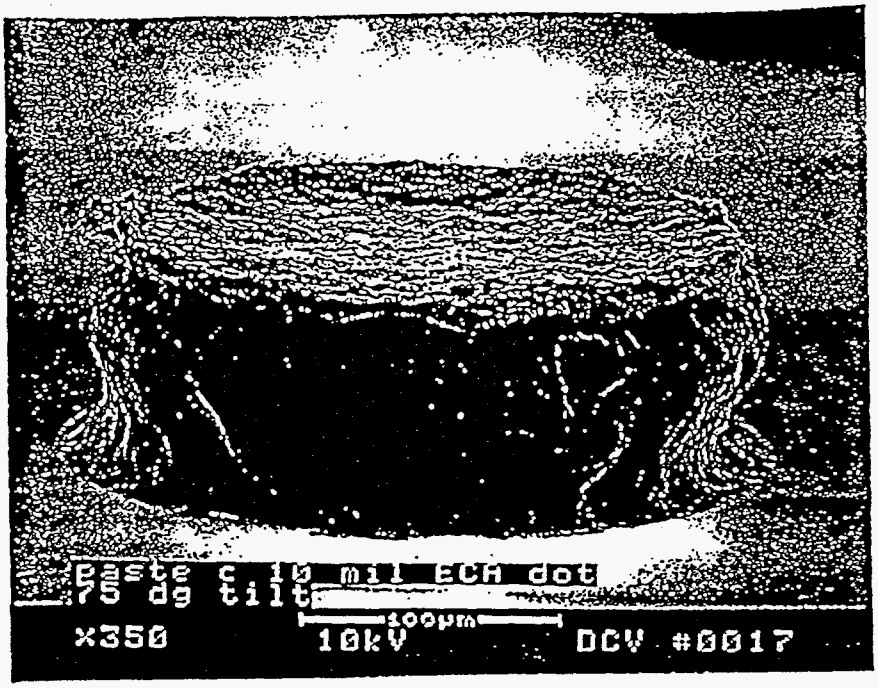


FIG. 2 SEM PICTURE OF DEPOSITS ON WAFER USING AX AS PHOTOIMAGABLE PHOTORESIST.

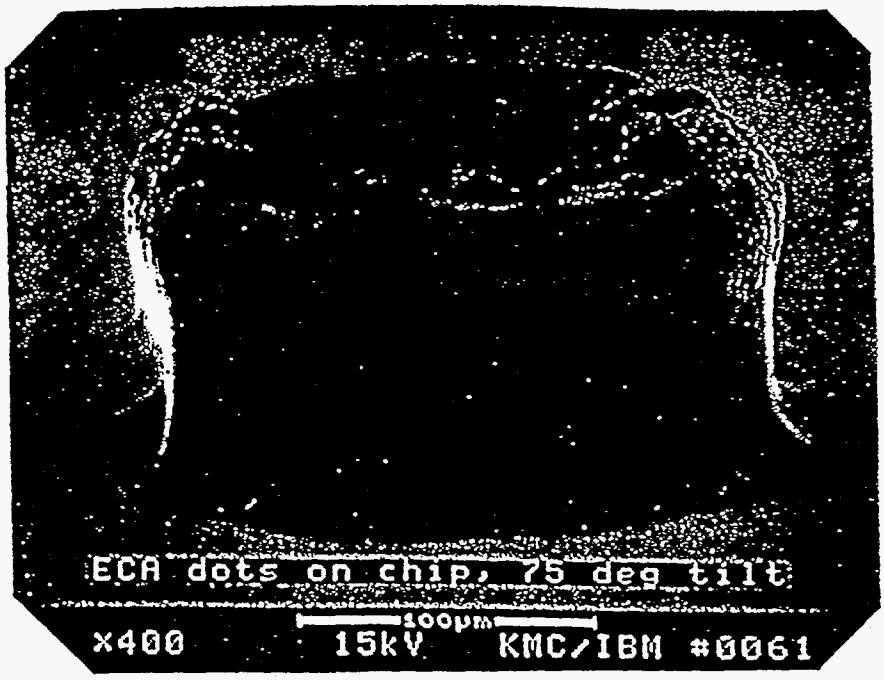


FIG. 3 SEM PICTURE OF DEPOSITS ON WAFER USING RISTON AS PHOTOIMAGABLE PHOTORESIST

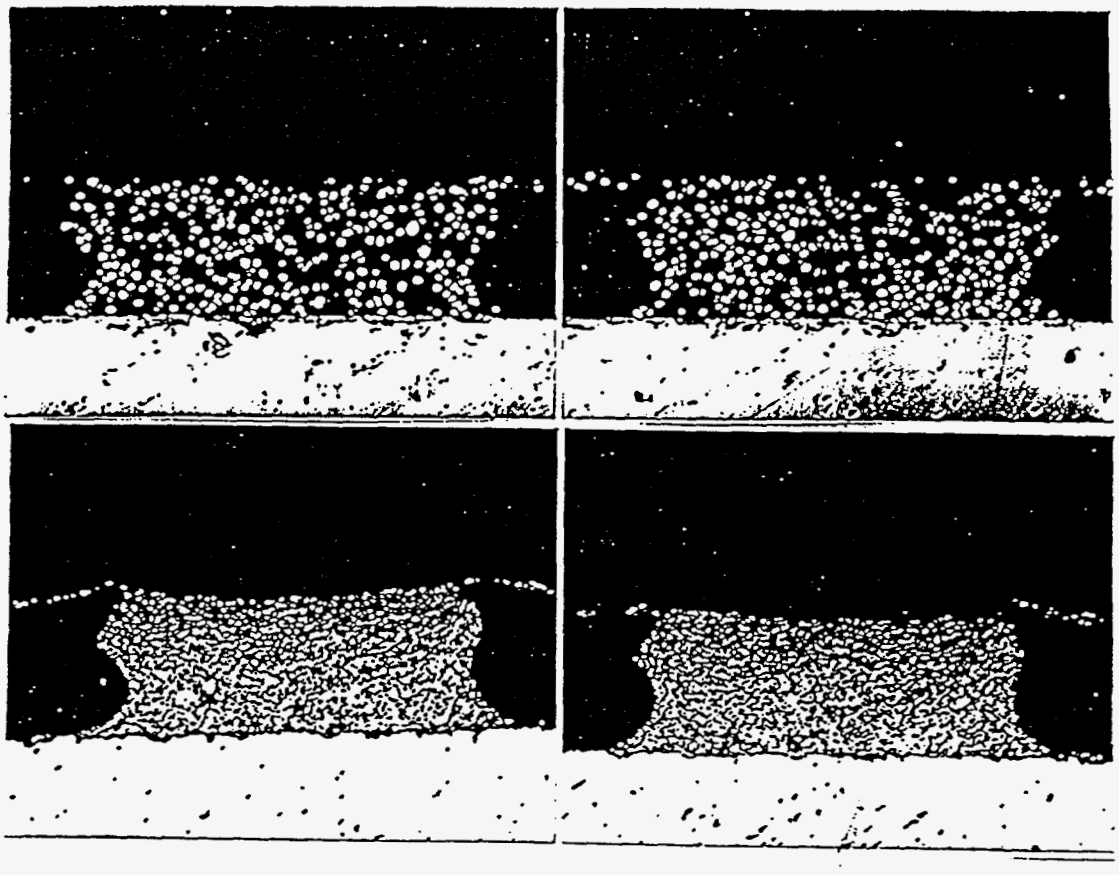


FIG. 4 THE CROSS-SECTION OF AX PHOTORESIST

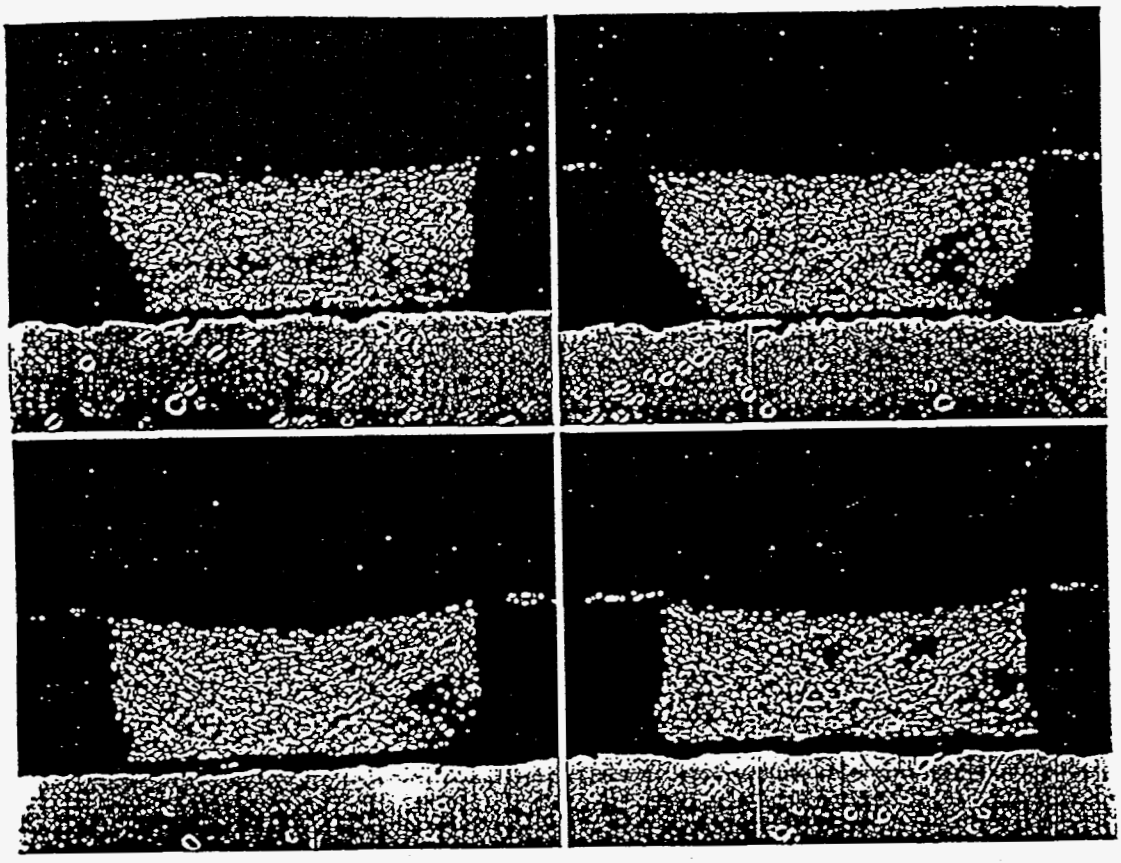


FIG. 5 CROSS-SECTION OF RISTON PHOTORESIST

EXPOSE 175 mJ/cm^2

EXPOSE 300 mJ/cm^2

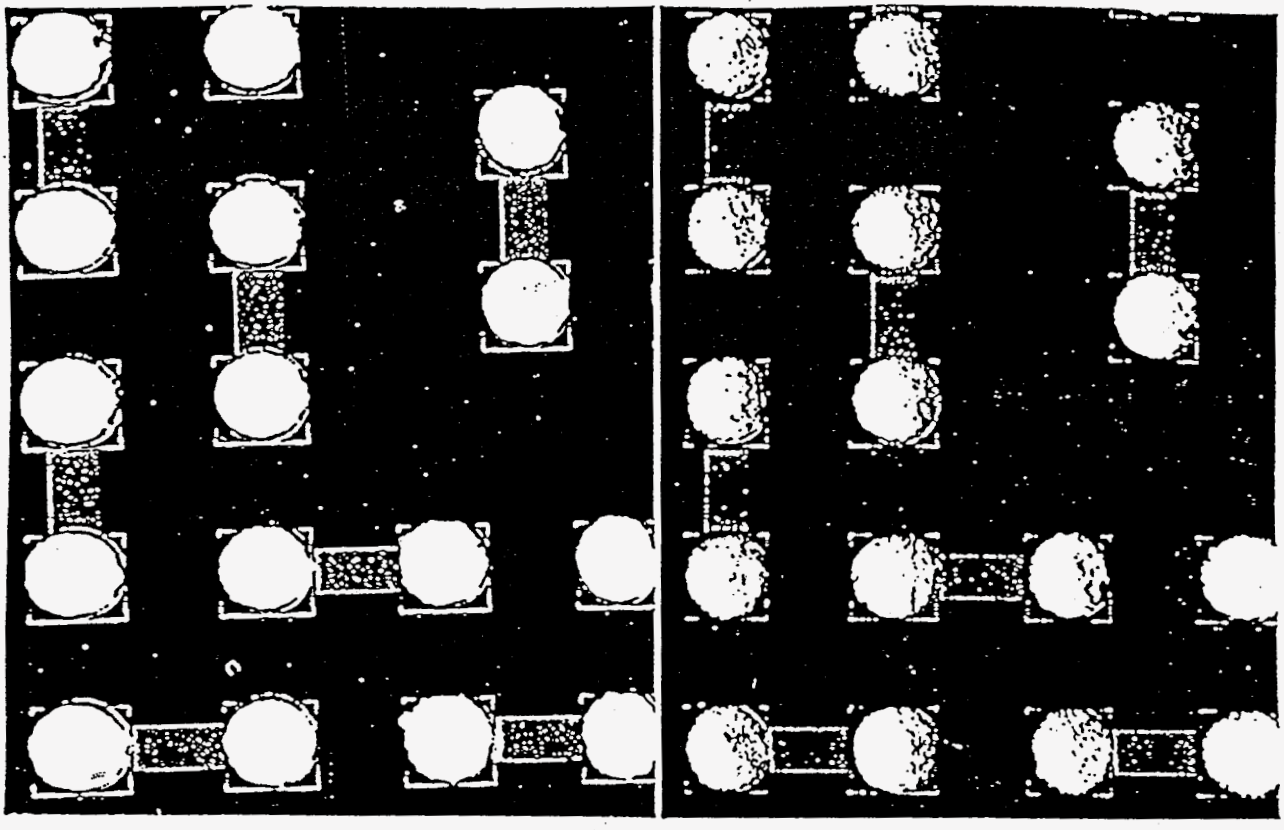


FIG. 6 ECA ON PAD

APPENDIX 1

EXPERIMENT WORKSHEET

NAME OF EXPERIMENT	: PHOTOBUMP
NUMBER OF FACTORS	: 3
NUMBER OF LEVELS	: 2
RESOLUTION	: FULL
NUMBER OF RUNS	: 8
DESIGN FRACTION	: FULL
BLOCKING	: NONE
NUMBER OF REPLICATIONS WITHIN BLOCK	: 1
NUMBER OF BLOCK REPLICATIONS	: 1
FACTOR CODES	: ABC

FACTOR LEVEL MATRIX

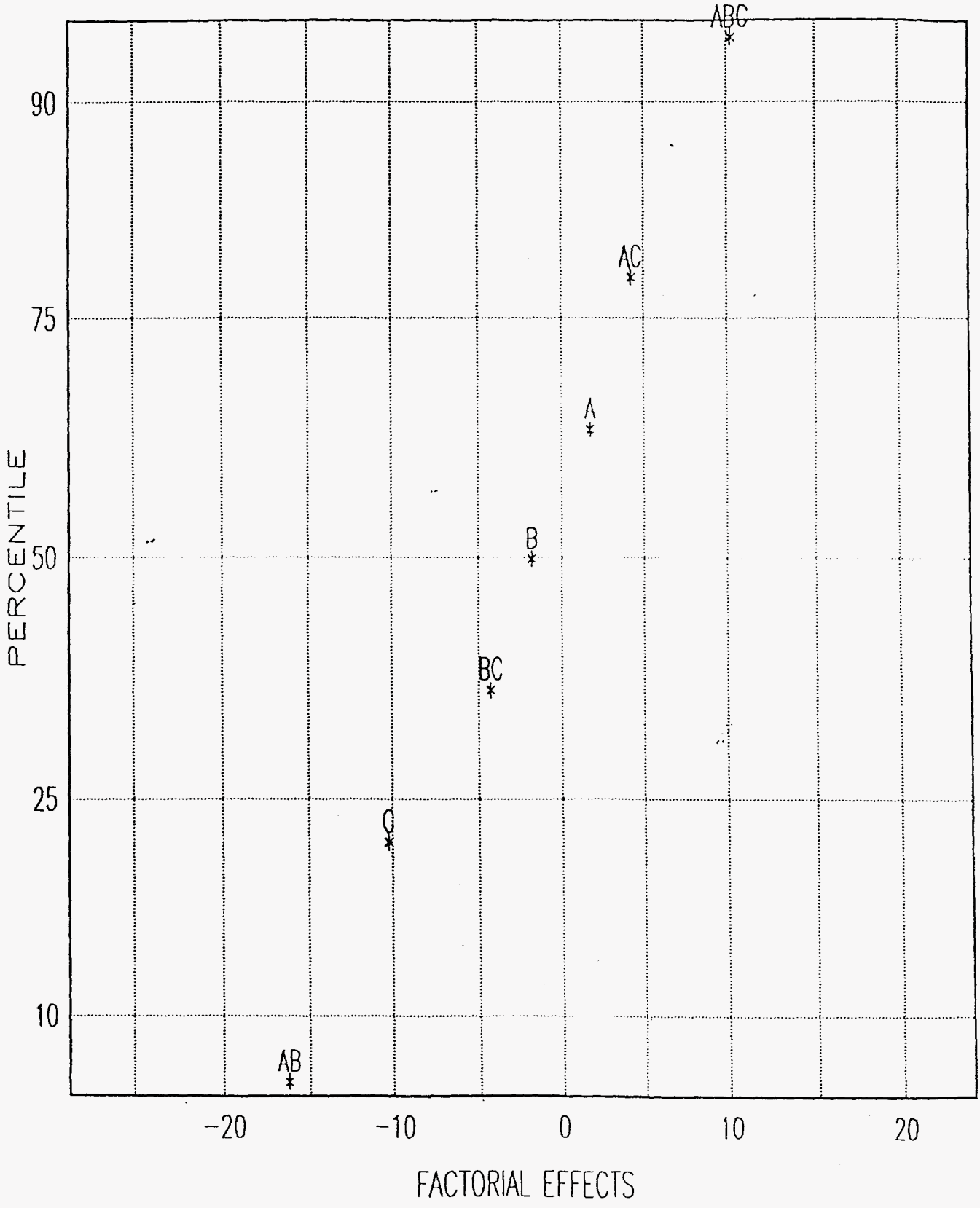
RUN	EXPOSE	DEVELOP	TEMP	SURVIVAL CHIP
1	HIGH	HIGH	HIGH	1
2	HIGH	HIGH	LOW	1
3	HIGH	LOW	HIGH	30
4	HIGH	LOW	LOW	1
5	LOW	HIGH	HIGH	25
6	LOW	HIGH	LOW	13
7	LOW	LOW	HIGH	1
8	LOW	LOW	LOW	1

```
                              TABLE OF COEFFICIENTS
8 OBSERVATIONS    R-SQUARED      = 1              STANDARD ERROR = 0
8 VARIABLES       ADJ R-SQUARED = UNDEFINED
  EFFECT     ESTIMATE    WITH 0 DEGREES OF FREEDOM, THE FOLLOWING ARE NOT DEFINED
MEAN           9.125          STANDARD ERRORS
 A EXPOSE      1.75           T STATISTICS
 B DEVELOP    -1.75           CONFIDENCE LIMITS
 C TEMP      -10.25
 AB          -16.25
 AC            4.25
 BC           -4.25
 ABC          10.25
--------------------------------------------------------------------------------
TABLE NAME   : -----AE1
DESTINATION  : ANS
ENTER=GO           PF:1=HELP      2=VIEW GRAPHICS      3=RETURN      4=SCROLL LEFT
CLEAR=DEFAULT         5=SCROLL RIGHT    6=ERASE    7=SCROLL UP     8=SCROLL DOWN
      RESPONSES       9=OUTPUT 10=STORE/RETRIEVE 11=INTO APL   12=ADD'L ACTIONS
                          PF13 TO PF24 ACT LIKE PF1 TO PF12
```

ANALYSIS OF VARIANCE

SOURCE	DF	SS	MS	F	SIG LEVEL
A EXPOSE	1	6.125	6.125	NOT	AVAILABLE
B DEVELOP	1	6.125	6.125		
C TEMP	1	210.13	210.13		
AB	1	528.13	528.13		
AC	1	36.125	36.125		
BC	1	36.125	36.125		
ABC	1	210.13	210.13		
TOTAL	7	1032.9	147.55		

TABLE NAME : -----AE2
DESTINATION : ANS
ENTER=GO PF:1=HELP 2=VIEW GRAPHICS 3=RETURN 4=SCROLL LEFT
CLEAR=DEFAULT 5=SCROLL RIGHT 6=ERASE 7=SCROLL UP 8=SCROLL DOWN
RESPONSES 9=OUTPUT 10=STORE/RETRIEVE 11=INTO APL 12=ADD'L ACTIONS
PF13 TO PF24 ACT LIKE PF1 TO PF12


ANALYSIS OF FACTORIAL EXPERIMENT: PHOTOBUMP
ABC
AC
A
B
BC
C
AB
90
75
50
25
10
PERCENTILE
-20
-10
0
10
20
FACTORIAL EFFECTS

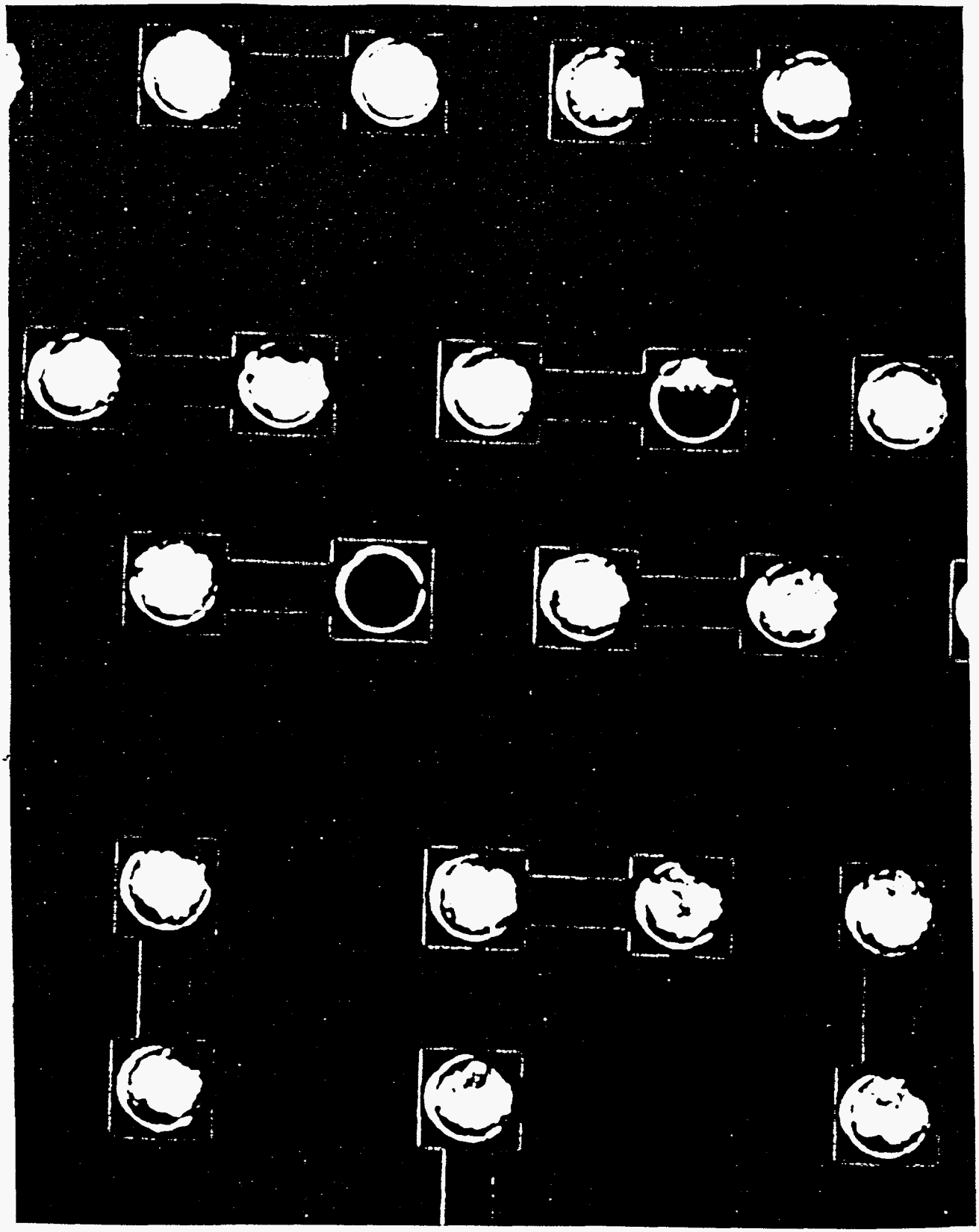


FIG. 7 INCOMPLETE VIA HOLE FILLING

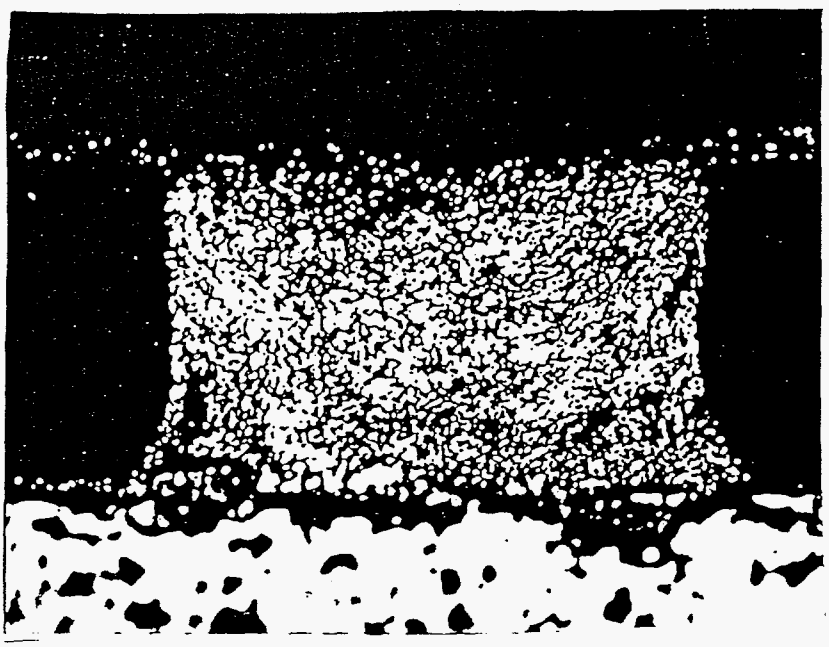


FIG. 8 A STRAIGHTENED SIDEWALL PROFILE WITH A TREE TRUNK LIKE BASE

Date: 10/8/96

To: Dr. Charles Woychik
From: Michael D. Snyder
Subject: Third Quarter 1996 Report on DARPA Project UIC J/N M919980 ID No. DE-FC-04094AL98817 Covering Universal Instruments Activities for the Timeframe 7/1/96 Through 9/30/96

Overview and Summary

The work by Universal during the 3Q96 timeframe continued to support the process and material property characterization testing being carried out by IBM, but the major Universal effort was again concentrated in two general areas:

- Refinement of the **Cost Estimation System for Flip Chip Attach Alternatives** activity being carried out with personnel from Binghamton University. The refinements allow an easier interface to the cost modeling tool and expand its usability in the cost comparison domain.
- Debug and characterization of the automated testbed and support of IBM in its use of the tool to characterize the ECA Flip Chip bonding process.

Work in these areas has progressively expanded the knowledge base and allow determination of the performance, cost and functional requirements needed to provide a salable production equipment solution to the Electronics Assembly Industry for the use of the IBM developed Electrically Conductive Adhesive material.

Work was carried out interactively between IBM, Endicott, IBM Yorktown and Universal using the automated testbed to bond Flip Chips. The work on the testbed included the bonding of chips to Silicon wafer material as well as laminate PWB. The focus of the effort was to verify the ability of the machine to correctly pick up, align, and carry out the bonding process under computer control. An additional focus of the activity was to inspect the bonded chips to determine if any detrimental influence of the bonding equipment on the creation of successful electrical ECA joints existed.

This iterative bonding and inspection showed that the thermal expansion properties of the bonding tool had an influence on the parallelism of the chip under surface to the substrate target surface. Lack of parallelism was evident qualitatively on post bond inspections. Subsequent quantitative inspection revealed that the chip standoff, as measured at each corner of the chip varied by approximately 0.0025 inches. Our desired result was a parallelism and standoff height of ≤ 0.0005 inches. As a result, two efforts were carried out to address this observation.

For the short term efforts, an iterative series of bond experiments were carried out, each experiment followed by an application of an alignment shim to alter the condition. The

final realignment leaves the chips bonded with parallelism of the chip underside to the substrate target surface to ≤ 0.0005 inch.

The root cause of the problem was determined to be an inability of the bonding tool to accurately maintain a uniform load distribution over the back surface of the chip during the temperature excursion and pressure application portion of the chip bonding process. Part of the early assumptions governing the bond tool suspension design was that the stiffness of the ECA bumps would minimize the effect of small variations in load distribution during bonding. Anticipated bonding loads at that time were felt to be in the range of 50 pounds (bonding force).

Working together with IBM the bonding force has been reduced to the < 5 pound range, which facilitates simplification of board support issues within a production machine application. A side effect, however, is that small variations in applied loading over the back surface of the chip during bonding has a more significant effect on the chip standoff height being maintained constant over the chip to substrate interface.

This bonding parallelism "problem" is an important finding, and has an impact on the tool suspension design as it will finally be implemented in a production tool. Efforts are under way at present within Universal to create a bonding tool suspension allowing for compliancy in the tool which can maintain uniform load distribution during the bonding process. On the positive side, it is exactly these type of "problems" which the automated testbed has been designed to find so they can be addressed prior to production packaging efforts. The second iteration of the bond tool suspension design is anticipated to be fabricated and tested early in the following quarter.

In the meantime, additional chip bonding efforts are being carried out to assist in the identification of other "problems" which eventual production implementation must address.

In addition to the work being carried out on the automated testbed, work was done to improve the benchtop testbed to facilitate the investigation of the bulk properties of the ECA material. An additional support ring for the alignment of copper "pegs" was designed and fabricated to allow the bonding of copper "pegs" whose ends were cut at various angles. These bonded "pegs" allow pull tests to be done with the material in various degrees of tension and shear, adding to the knowledge base on the ECA material.

Expansion of the Cost Modeling Activity

The report on this phase of the activity is provided as an attachment at the end of this document.

Automated Testbed Debug and Characterization

Tests were carried out to characterize the testbed so as to guarantee that the study of the ECA bonding process could be accurately assessed. Included in the characterization tests were:

- Laser tests of the X and Y testbed positioning system axes
- Measurement of the programmable bond force accuracy and resolution
- Measurement of the thermal response of the thermode heating tip
- Vision system / optics calibration
- Orthogonality of the Z axis to the X - Y plane
- Orthogonality of the X and Y axes
- Rotational repeatability of the Theta axis
- Verification of pneumatic pressure and vacuum levels

Status Update on the Automated Testbed System

The progress towards completion of the Automated Testbed (See Figure 1) is presented below:

Element	Status
• Optical Bench Frame Structure	Complete, Integrated
• Electrical Cabinet	Design done, In fab
• Head Support & Overbeam Structure	Complete, Integrated
• One Micron X-Y Positioning System (12 X 12 Travel)	Complete, Integrated
• Positioning System and Head Controller	Complete, Integrated
• Upward Looking Camera Assembly	Complete, Integrated
• Upward Illumination System	Complete, Integrated
• Downward Looking Camera and Illumination	Complete, Integrated
• Vision Processor Engine	Complete, Integrated
• Y-Axis Positioning Slide for Upward Looking Camera	Complete, Integrated
• Board Support Thermode With Vacuum/Air Kiss	Complete, Integrated
• Board Support Actuator	Complete, Integrated
• Bonding Head With Automatic Theta Axis	Complete, Integrated
• Automatic Z-Axis for Bonding Head	Complete, Integrated
• Bonding Thermode With Vacuum/Air Kiss Capability	Complete, Integrated
• Capability for Forced Cooling of Bonded Chips	Underway
• System Software	Complete
• System Pneumatics	Complete

As reported in the last quarter update, the integration of the testbed into a functional entity suitable for debug was completed, and the major effort over this

quarter was to complete the debug. This effort led to discovery of areas where the testbed could be improved, and those improvements were made.

An example is the addition of software changes to allow visual and manual intervention in the location of "fiducial" targets used for chip and board location. In the early stages of supply of ECA bumped chips, the edge characteristics of the bump deposits had certain irregularities, leading to difficulty in automatically "finding" these bumps with an automatic vision system. To correct this problem, changes were made to allow the operator to visually observe the bump, jog the X - Y positioning system to locate a cross hair over the apparent center of the bump, and enter that location as the bump center. This not only allows use of irregular bumps for location, but also allows use of features not formally identified as "fiducials" to act as location features for bonding alignment.

An additional area of improvement was to increase the speed of the Z axis and to smooth out the motion at the region where contact of the chip by the bonding tool and the "touchdown" portion of the bonding cycle occurs.

Cleanup of the electronics packaging aspects of the testbed continues as an intermittent activity. Since this activity does not affect the overall performance of the testbed, it is being treated as a lower priority compared with testbed functional; improvements. The incorporation of forced air cooling, while provided for in the software and control system, has not yet been mechanically integrated. This too is underway but being treated as a lower priority than work to improve the more functional aspects of the testbed such as determining improvements to the bonding tool suspension.

Focus of Fourth Quarter Efforts by Universal

- Completion of Electrical Cabinet packaging
- Completion of Forced Cooling provision
- Completion of testbed system first level refinement
- Continuation of the Cost Model software activity
- Design and implementation of an improved bonding tool suspension.
- Continued utilization of the testbed for bonding process characterization

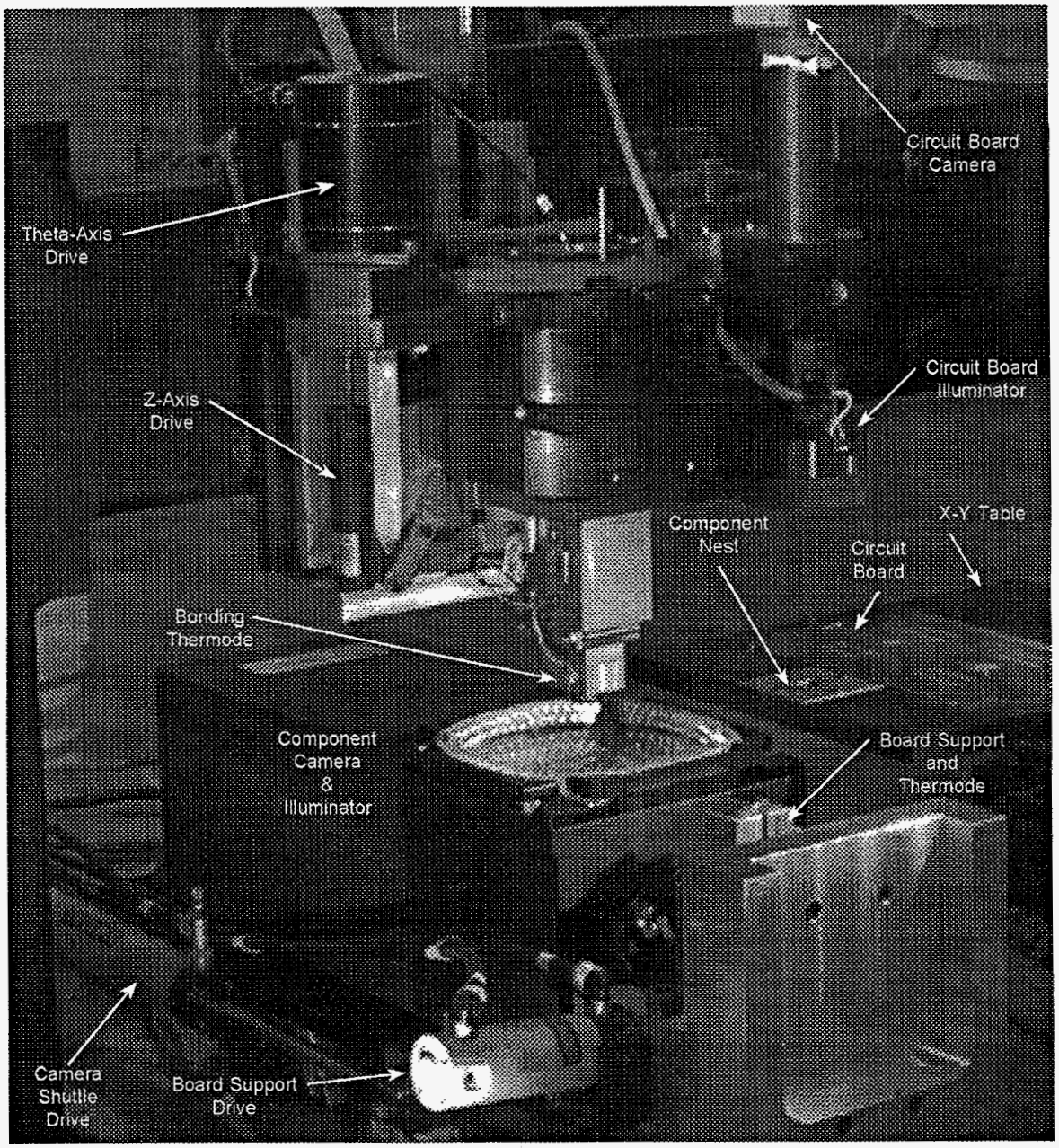


Figure 1. 2nd Generation Conductive Adhesive, Flip Chip Bonding Testbed

ECA-FCA Computer Aided Cost Estimation (CACE)

A Status Report Submitted To

Universal Instruments Corporation (UIC)
Advanced Technology Group
Binghamton, New York

October 1996

By

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This report is written to address the current and forthcoming efforts by the Binghamton University (BU) team in support of the sub-contractual effort accomplished under the auspices of a DARPA-sponsored grant being researched by Universal Instruments Corporation (UIC) and IBM. The purpose of the grant is to determine the viability of a recent IBM-developed thermoplastically electrically conductive adhesive (ECA) for use in the area of flip chip attach (a.k.a., FCA, DCA-direct chip attach, or COB-chip on board) in surface mount assembly. The sub-contractual effort undertaken by the BU team is specifically performed to help determine whether a nascent technology, namely ECA-FCA, can compete in the marketplace against the more traditional, solder-based attached methods. The thrust of the BU team's efforts is the development of a computer aided cost estimation (CACE) system to evaluate the alternatives of using ECA-FCA vs. solder-based-FCA. The descriptions below provide a summary of the status on the current version of the CACE and describe the newly undertaken efforts of the BU team for this sub-contractual effort.

Current Status

In the last quarterly report, we reported that the CACE system has, among others, attributes which allow the following:

- have the user input product-specific information (replete with volumes, number/types of components, etc.);
- estimate costs contributing from three important phases of FCA surface mount assembly (these are Wafer Preparation, Board Preparation, and PCB Assembly);
- generate estimates of equipment sets needed to support the production of the user-supplied information in the three aforementioned areas;
- analyze the costs of four different FCA methodologies (these are ECA vs. solder plating (SP), solder jetting (SJ), and solder-on-chip (SOC)).

During the June DARPA project-review meeting, it was presented that, for a particular product of a major camera and film manufacturer, ECA was a viable competitor (in terms of cost per board) among all the alternatives.

New & Forthcoming Efforts

The BU team has recently focused on new activities related to the betterment of the CACE tool. The activities being undertaken are divided into three areas: i) User-Interface Enhancements to the CACE tool; ii) Product Identification; iii) Animated Computer Simulation.

User-Interface Enhancements

The first activity is being performed to facilitate the use of the CACE by developing a more "user friendly" interface replete with dialog boxes and output report generators (i.e., graphs, tables, etc.). While the CACE is multifaceted, it needs a user significantly knowledgeable in the use of Microsoft Excel (the platform in which it is developed). This part of the new effort is undertaken to ensure that a potential user does not necessarily need to be skilled in the use of MS Excel in order to perform cost comparisons of ECA-FCA vs. Solder-FCA.

Status: As demonstrated to Mr. Michael Snyder (UIC liason to BU team) on October 10, the dialog boxes and output report generators have been created to provide a tremendous increase in the "friendliness" of the system. While there is still some effort which must be addressed to validate the new system (in terms of verifying the underlying "user-hidden" cost calculations), this portion of the CACE system modification is nearing completion. We estimate the completion of this activity to be October 31.

Product Identification

As the CACE is product specific (i.e., cost estimates are generated as a function of an exact product/card to be assembled), this second activity is being focused on the search for other products/examples with which to perform the ECA vs. solder analyses (e.g., as was discussed for the camera product mentioned above). With more examples analyzed, a better understanding of ECA cost-justification can be obtained.

Status: This activity will be addressed upon completion of the previous "User Interface Enhancements" which, as above, is around October 31.

Animated Computer Simulation

The third activity is being devoted to developing computerized animated simulation models as a further validation/justification step for ECA usage. While it is one thing to estimate the different numbers of machinery required at different production stages (as does the CACE), it is another task to determine if these machines can actually function as an interconnected *system* to effectively manufacture a product. Computer simulation will not only help to verify that the system will function, but as an added benefit, the animation will allow these proposed systems to be developed and studied in a virtual environment without having to actually create an expensive testing facility replete with actual machines.

Status: This activity is being performed using a "best-in-its-class" software known as "Arena". While the BU team is skilled in simulation modeling and analysis, this software is a recent acquisition for us. As such, we are currently developing preliminary simulation models (e.g., PCB's being assembled on one machine stage) to familiarize us with the software. The learning curve is on our side and we will begin to develop a library of different PCB assembly line configurations beginning about November 1. The configurations will be different, primarily, due to different equipment sets (e.g., different numbers of placement machines, numbers of underfill dispensers, etc.). Outputs provided by the CACE system can be validated by simulating a representative model from the library.

As mentioned in the last quarterly report, all of the activities by the BU team are scheduled to be complete by January 1, 1997.