

CONF-961066--6

Design Specifications for Manufacturability of MCM-C Multichip Modules

Federal Manufacturing & Technologies

Roy Blazek,
Jay Desch,
David Kautz, and
Howard Morgenstern

RECEIVED

NOV 22 1996

OSTI

KCP-613-5770

Published October 1996

Approved for public release; distribution is unlimited.



MASTER

Prepared Under Contract Number DE-ACO4-76-DP00613 for the
United States Department of Energy

 **AlliedSignal**
AEROSPACE

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade names, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Printed in the United States of America.

This report has been reproduced from the best available copy.

Available to DOE and DOE contractors from the Office of Scientific and Technical Information, P. O. Box 62, Oak Ridge, Tennessee 37831; prices available from (615) 576-8401, FTS 626-8401.

Available to the public from the National Technical Information Service, U. S. Department of Commerce, 5285 Port Royal Rd., Springfield, Virginia 22161.

Copyright © 1996 by AlliedSignal Inc. The Government is granted for itself and others acting on its behalf a paid-up, nonexclusive, irrevocable worldwide license in this data to reproduce, prepare derivative works, and perform publicly and display publicly.

A prime contractor with the United States
Department of Energy under Contract Number
DE-ACO4-76-DP00613.

AlliedSignal Inc.
Federal Manufacturing
& Technologies
P. O. Box 419159
Kansas City, Missouri
64141-6159

Design Specifications for Manufacturability of MCM-C Multichip Modules

Federal Manufacturing & Technologies

Roy Blazek,
Jay Desch,
David Kautz, and
Howard Morgenstern

KCP-613-5770

Published October 1996

Approved for public release; distribution is unlimited.



Prepared Under Contract Number DE-ACO4-76-DP00613 for the
United States Department of Energy

 **AlliedSignal**
AEROSPACE

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade names, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Printed in the United States of America.

This report has been reproduced from the best available copy.

Available to DOE and DOE contractors from the Office of Scientific and Technical Information, P. O. Box 62, Oak Ridge, Tennessee 37831; prices available from (615) 576-8401, FTS 626-8401.

Available to the public from the National Technical Information Service, U. S. Department of Commerce, 5285 Port Royal Rd., Springfield, Virginia 22161.

Copyright © 1996 by AlliedSignal Inc. The Government is granted for itself and others acting on its behalf a paid-up, nonexclusive, irrevocable worldwide license in this data to reproduce, prepare derivative works, and perform publicly and display publicly.

A prime contractor with the United States
Department of Energy under Contract Number
DE-ACO4-76-DP00613.

AlliedSignal Inc.
Federal Manufacturing
& Technologies
P. O. Box 419159
Kansas City, Missouri
64141-6159

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

KCP-613-5770
Distribution Category UC-706

Approved for public release; distribution is unlimited.

**DESIGN SPECIFICATIONS FOR MANUFACTURABILITY
OF MCM-C MULTICHIP MODULES**

Roy Blazek,
Jay Desch,
David Kautz, and
Howard Morgenstern

Published October 1996

Paper submitted to International Society for Hybrid Microelectronics
29th International Symposium on Microelectronics
October 6-10, 1996
Minneapolis, MN

 **AlliedSignal**
AEROSPACE

Design Specifications for Manufacturability of MCM-C Multichip Modules

Roy Blazek, Jay Desch, David Kautz, and Howard Morgenstern
AlliedSignal Federal Manufacturing & Technologies*
P.O. Box 419159
Kansas City, MO 64141-6159
Phone: 816-997-4901; Fax: 816-997-3297
Email: rblazek@kcp.com

Abstract

A comprehensive guide for ceramic-based multichip modules (MCMs) [1] has been developed by AlliedSignal Federal Manufacturing & Technologies (FM&T) to provide manufacturability information for its customers about how MCM designs can be affected by existing process and equipment capabilities. This guide extends beyond a listing of design rules by providing information about design layout, low-temperature cofired ceramic (LTCC) substrate fabrication, MCM assembly, and electrical testing. Electrical, mechanical, packaging, environmental, and producibility issues are reviewed. Examples of three MCM designs are shown in the form of packaging cross-sectional views, LTCC substrate layer allocations, and overall MCM photographs. The guide has proven to be an effective tool for enhancing communications between MCM designers and manufacturers and producing a microcircuit that meets design requirements within the limitations of process capabilities.

Key Words: Multichip module, Multichip module ceramic (MCM-C), LTCC substrate, manufacturability

Introduction

The development of MCMs using LTCC substrates is a continuing effort by AlliedSignal FM&T to meet future microelectronic packaging designs. The complexity of these MCMs requires that concurrent engineering methods be used to decrease overall project flowtime. Future electronic systems will require the cofired ceramic MCM technology for the higher performance, smaller volume, faster speed, lighter weight, and higher density that cannot be provided by traditional hybrid microcircuit and printed wiring board technologies.

In order to meet a customer's electronic system design requirements, a close relationship must be developed between designers and manufacturers so that the microcircuits required for these electronic systems can be designed, packaged, and tested within the required cycle time, process yield, and cost constraints. Design guides had been developed for earlier hybrid microcircuit (HMC) production, but redesign and rework resulted when designers

stretched to incorporate functional characteristics that exceeded the HMC process equipment and technology limitations.

The developers of the MCM-C technology realized that a more comprehensive design guide was required to transform complex MCM designs into producible microcircuits. As a result, the *Design Specifications for Manufacturability of MCM-C Multichip Modules* was created as part of a Total Quality initiative. Six sigma manufacturing quality levels can be achieved only if six sigma designs are developed by focusing more attention at the front end of the design-manufacturing cycle.

The *Design Specifications for MCM-C Multichip Modules* is a 73-page document that includes electrical, mechanical, environmental, testing, packaging design, and MCM producibility requirements and considerations for ceramic MCMs. A review of deliverables includes drawings, documentation, and computer-automated design (CAD) files. Seven appendices include material

*Operated for the United States Department of Energy under Contract No. DE-AC04-76-DP00613

properties, CAD checklists, substrate, assembly, and testing effects on design, component procurement, and MCM-C design examples.

Customer Requirements

The MCM-C development process sequence includes the customer requirements, MCM design, LTCC substrate fabrication, MCM assembly, electrical and environmental testing, and delivery. The knowledge needed to define a complete MCM package may be provided by the customer, but more likely a concurrent effort between the MCM design team and the customer will be required to develop all of the necessary information. The type of ceramic MCM available at AlliedSignal FM&T is a microelectronic assembly composed of standard and custom-designed integrated circuits and surface mount components that are attached to a multilayer, high density, three-dimensional, interconnected substrate. Some of the electrical, mechanical, environmental, and testing requirements that will be required by the design team to manufacture this type of MCM include the following:

- ◆ Electrical requirements
 - functional block diagram,
 - schematic, and
 - electrical interfaces;
 - ◇ interconnect impedances, terminations, loads, and bandwidths.
- ◆ Mechanical requirements
 - size of the MCM,
 - heat transfer, and
 - mechanical interfaces;
 - ◇ pin or lead geometry and location,
 - ◇ attachment material composition and next assembly processing conditions,
 - ◇ encapsulation materials, and
 - ◇ location of thermal pathways.
- ◆ Environmental requirements
 - operational shock and vibration,
 - thermal,
 - hermetic,
 - atmosphere, and
 - storage and transportation.
- ◆ Testing requirements
 - electrical,
 - temperature,
 - burn-in, and
 - shock and vibration.

In addition to MCM performance, other customer requirements include documentation, cost, quantity, schedule, and quality. Since these items are interrelated and invariably require trade-offs, the design team can most effectively analyze and communicate such trade-offs by first understanding the customer's priorities in these areas.

Packaging Design Requirements

The success of an MCM project is directly related to the concurrent efforts between the customer and the design team. The design team includes representatives from electrical, LTCC substrate, MCM assembly, drafting, testing, quality, and manufacturing areas. Packaging design requirements include electrical design and testing, LTCC substrate fabrication, and MCM assembly. The design team and customer must have complete knowledge of the capabilities and interactions of all of these areas in order to obtain a manufacturable design. An MCM producibility assessment is performed before the design is committed to manufacturing.

Electrical Design and Testing

The electrical design of the MCM must produce the schematic definition inclusive of all component symbols, signal input/output (I/O) definitions, and signal timing relationships or event sequences. This design cannot be considered complete until some degree of design testing is successfully conducted, such as the use of simulation and analysis tools and/or actually breadboarding the design and testing for correct functionality.

Once the electrical design has been completed, implementation techniques must be identified that ensure the required electrical performance. Issues to be resolved include power distribution (voltage, current, grounding) and signal integrity (isolation, controlled impedance interconnects, dielectric effects, propagation delay, MCM I/O launch). The product of this effort should be layout and routing rules, a preliminary layer stackup, dielectric tape selection, and a concept for I/O interconnect to the user system. Module electrical testing and troubleshooting should be considered early in the design so that additional test points are incorporated.

A thermal analysis is always in order for any MCM design. The basic goal of thermal analysis is

to minimize the thermal impedance between the semiconductor die surface (where active, heat-generating junctions are located) and the outer surface of the MCM (where the heat transfer to the environment or to the user system occurs).

Before finalizing the LTCC substrate layout, the design team must verify the electrical and thermal management designs. This verification avoids increased cost and production delays that result from inaccurate definition. Table 1, which appears in the MCM-C manufacturability guide, provides the design team with a checklist to support the initial phase of the design.

Table 1. LTCC Substrate Pre-Routing Checklist

Verification
Schematic vs. draft schematic
Electrical netlist file vs. schematic
Components CAD definition vs. component definition
Considerations
Controlled impedance conductor lines
Propagation delay
High current conductor lines
Isolation, shielding and cross talk
Thermal management
Die backside metallization and potential
Printed resistors
Verify each resistor value
Power dissipation for each resistor
Low resistance paths to low value resistors
Probe pads for resistor trimming
Place all resistors for active trimming on one side of substrate
Provide opening in all resistor loops
Design definition
Electrical interface
Mechanical interface
LTCC layers (number, planes and XY runs)
LTCC cavity (features and components)
Manufacturability
Substrate considerations reviewed with engineer
MCM package considerations reviewed with engineer
Testability
Requirements reviewed with test equipment engineer
Test nodes defined for key signals

LTCC Substrate Fabrication

The substrate design/layout and assembly are the concluding processes in the MCM design where all of the customer requirements, the manufacturing process capabilities, and the remaining design trade-off options are merged together to create the final MCM package definition. The process of creating the package definition also defines the substrate features due to the nature of the technology. LTCC substrates can serve as both the interconnecting network and the module package.

MCM thermal characteristics are often dominated by the substrate characteristics. One factor impacting substrate thermal performance is the thickness of the substrate beneath the heat dissipating devices. By placing these devices in cavities, substrate thickness can be reduced. An illustration of the cavity layout is shown in Figure 1. The minimum and typical dimensions of the substrate and cavity are shown in Table 2. All substrate dimensions are post-fired conditions and are in mm except where noted. The substrate cavity parameters include cofired package thickness, LTCC thickness at the bottom of the cavity, cavity depth, ledge height, distance from die edge to cavity wall, seal ring height, cavity edge to seal ring, and cavity ledge length.

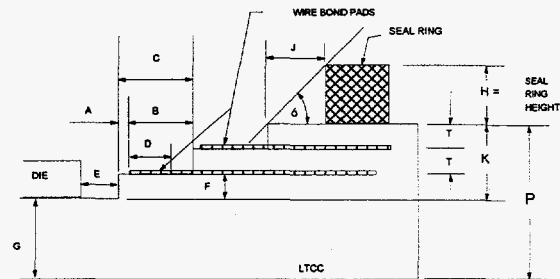


Figure 1. Cavity Layout Definition

Table 2. LTCC Substrate Cavity Parameters

	Minimum or Typical Dimension (mm)	Fig. 1 Item
Cofired package thickness	1.52 min	P
LTCC thickness at bottom of cavity	1.02 min	G
Cavity depth	NA	K
First ledge height = Die height ± 0.25 for single ledge or Die height -0.25 for multiple ledges	NA	F
Distance from die edge to cavity wall	0.25 min 0.50 typ	E
Wire bond pad length (FOR CAVITY DESIGN). $B=C-A$	0.38 min	B
Seal ring height (min) = Die height (max) $-K+M$ Where: M =Bond wire loop height $+0.25$ (min) for lid clearance	0.50 min	H
Bond wire loop height for 0.025 Au wire	0.25 typ	
Bond wire loop height for 0.127 Al wire	0.76 typ	
Cavity edge to seal ring (minimum) = $H/\tan\phi$	0.50 min 0.76 typ	J
Cavity bond pad ledge length $C=(A+D)+(T/\tan\phi)$	0.76 typ	C
Bond pad pull back	0.08 min	A
Bondable pad length	0.25 min	D
Bond ledge height = Number of LTCC layers • layer's post-fired thickness	NA	T
Tool Angle for wire bonder	70°	ϕ

The LTCC substrate thicknesses shown in Table 2 were established to ensure that the substrate will have adequate package strength. The tightest dimensional tolerance on the contour of the substrate can be held if the substrate is rectangular. Arcs, keyways, and irregular shapes are possible but not with tight tolerances because they are cut before firing. Substrate layer allocation is related to the designed thickness of the part and the electrical functionality assigned to each layer.

Voltages and grounds are distributed to the components by metal planes designed into specified substrate layers, one plane for each voltage and ground. Each plane is typically composed of metal printed on the specified layer in a cross-hatched pattern. An adequate number of substrate signal layers must be defined so that all of the MCM interconnections can be successfully routed. Signal layers are normally defined as a pair of two conductor layers where one layer is used to route traces primarily in an X direction while the traces on the other layer are routed primarily in the Y direction. This orthogonal routing technique tends to reduce coupling between layers and retain planar external surfaces.

The manufacturability guide provides a recommended width for internal traces. Wider traces are possible for unique signal properties, but the designer is advised that traces with lesser widths can reduce substrate yield. A recommended diameter for internal electrical vias is specified in the guide. Larger via diameters are possible, but the ratio of the via diameter to tape thickness becomes critical. Smaller via diameters are possible, but forcing the ink into the smaller via becomes more difficult, and the substrate yield is reduced. Guidance is provided for minimum spacing between electrical vias and for staggering vias every two layers. Thermal vias are treated separately from electrical vias, and spacing and diameter requirements are provided.

A six-page appendix in the MCM-C manufacturability guide provides LTCC substrate information and constraints on design. Information in this appendix includes a conceptual substrate cross-section and layer allocation; substrate dimensional and parametric information and constraints for a typical dielectric tape, typical paste properties, seal ring, braze pad, and lid definition; and a substrate specification summary.

MCM Assembly

A definition is required for each unique component to be used in the MCM design. The component characteristics which are essential for proper MCM design include the length, width, and thickness dimensions for each component. Information about bond pad dimensions, pitch, and material composition is required for layout and assembly. A die bond pad layout showing the location of all bond pads with meaningful names is required. This information could be in the form of a die photograph or a scaled drawing. Knowledge of the die technology is required to establish appropriate assembly, handling, and testing processes. Die technology includes semiconductor material, logic type, and information on die passivation.

Die attach techniques dramatically impact the thermal impedance between the semiconductor die and the LTCC substrate. Electrically conductive and nonconductive epoxies and thermoplastic adhesives are used for die attachment to provide MCM rework capability. Information regarding the semiconductor die backside metallization is required as it impacts die attach options. Knowledge of the semiconductor die backside potential is required so that the die attach pad may be connected to the proper voltage or allowed to float. As in the case of die attach, passive component attachment techniques and material selection can be critical to the thermal performance.

Die components should be placed on the substrate to provide adequate room for attachment and connection. Components should be placed and oriented for the shortest trace interconnect lengths. The interconnect length of high-speed signal traces requires particular attention. After each die has been attached to the substrate, it must be electrically interconnected to the substrate. This interconnect is accomplished with wires bonded between appropriate die and substrate bond pads. The manufacturability guide shows specific physical limitations for substrate bond pad size and spacing, wire lengths, current carrying capabilities, and rework procedures.

Surface mount components are usually leadless chip carriers, chip resistors, or chip capacitors. Interconnect traces for these components are typically located on internal layers of the substrate. The surface mount pads that are used for attaching these components must be triple-printed to prevent solder leaching. The solders selected for

attachment of surface mount components must be compatible with the substrate metallization and component termination materials. Solder can be applied to the substrate by screen printing, preforms, or automated dispensing. Component reflow soldering can be done by using convection or infrared belt furnaces or a vapor phase chamber.

Brazing (high-temperature soldering) is used to attach pins or leads and a seal ring to the substrate. The ability to braze a seal ring to the substrate allows a hermetic die cavity to be formed with the addition of a lid. Pins or leads are typically used for the electrical interface and mechanical support between the MCM and the user system. The dimensions of these parts must be defined. Several constraints and recommendations on the design of a seal ring, its braze pad, and the companion lid are shown in the manufacturability guide.

A 16-page appendix in the MCM-C manufacturability guide provides assembly information and constraints on design. Information in this appendix includes an assembly drawing checklist; cavity and component layout definition; surface mount layout definition; substrate pin, lead, and seal ring attachment; die attachment; wire bonding; gold ribbon bonding; sealing and leak testing; and surface mount assembly. Assembly and rework limitations are shown for each process with descriptions of materials, process times and temperatures, and available equipment.

MCM Producibility

When an MCM design is completed but before it is committed to manufacturing, a final assessment of the producibility must be conducted. This assessment is the culmination of an on-going producibility assessment which should have been occurring throughout the design process.

The producibility of the design can be influenced by the availability and quality of the pieceparts, particularly die components such as Application Specific Integrated Circuits (ASICs). Unlike packaged components, when a die is incorporated into the design, it is not readily replaceable with a functionally identical die from another supplier. Even if die quantities are expected to be available, additional die testing may be required to ensure die quality (known good die) prior to assembly; otherwise, excessive die replacement rework will be inevitable.

The ability to manufacture an MCM design must not only address the availability of those processes and equipment directly related to the assembly of the MCM but also the processes and equipment required to produce all parts of the MCM such as the LTCC substrate. While all processes and equipment may be available, acceptable producibility must also permit an achievable assembly sequence that provides die protection, cleanliness, and decreasing process temperatures with subsequent processing steps.

MCM Examples

The manufacturability guide includes three design examples; this paper will only describe two. The processor module (PM) is shown in Figure 2, which is a 5.08 X 5.08 cm package with 165 PGA pins for electrical interface. This module performs all the processing and decision-making functions as part of a controller system. A surface mount read only memory (ROM) provides capability to define the module's task.

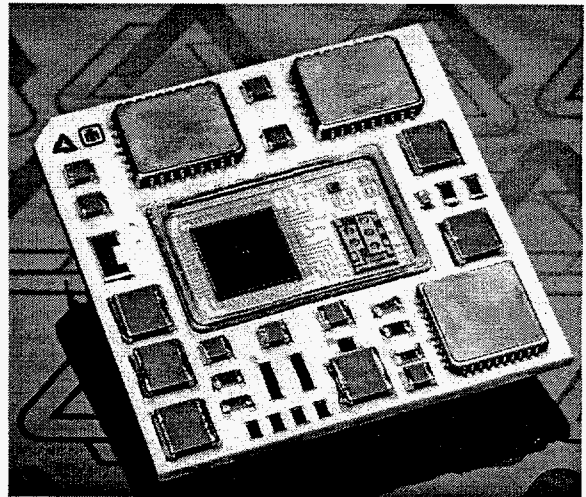


Figure 2. PM with Open Cavity

Figure 3 shows the cross-sectional view of the cavity area of the processor module. Some of the PM features are a two-tiered wire bondout cavity for the large digital ASIC, a sixteen-layer low temperature cofired ceramic substrate, and a high thermal conducting thick film aluminum nitride diode chip subcarrier with thermal vias.

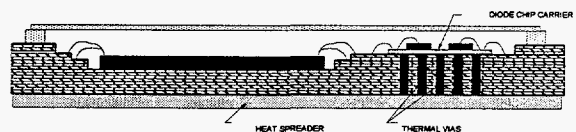


Figure 3. PM - Package Cross-Sectional View

Figure 4 shows PM layer allocation. The substrate thickness will be based on the mechanical requirements of the substrate and its physical features including those layers which form the die cavity. The electrical functionality of the substrate layers will be assigned based on the number of ground and/or power planes required and the electrical interconnect density of the signal layers.

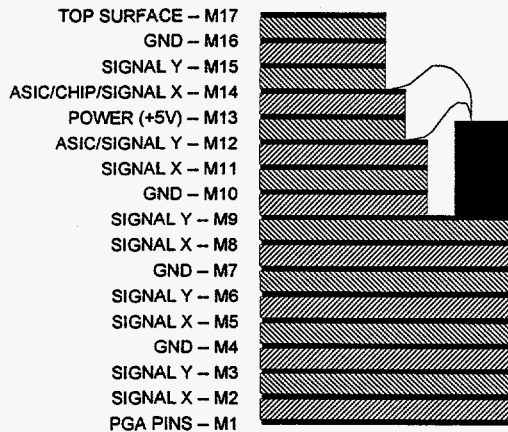


Figure 4. PM - Substrate Layer Allocation

The input/output module (IOM) is shown in Figure 5, which is a 5.08 X 5.08 cm package with PGA pins for electrical interface. This module performs the input level shifting for eight lines and provides output drives.

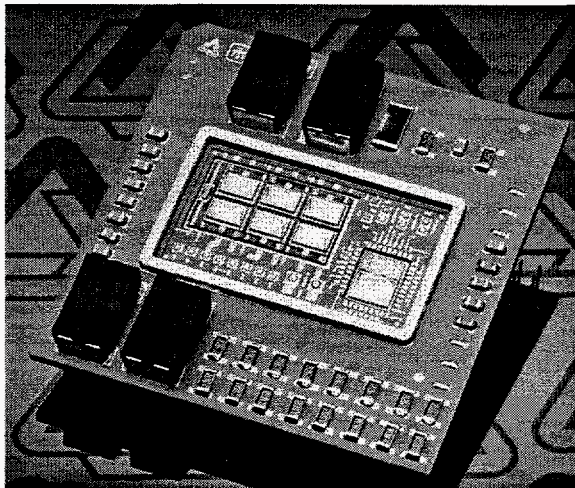


Figure 5. IOM with Open Cavity

Figure 6 shows the cross-sectional view of the cavity area of the input/output module. Some of the features are an analog ASIC, an eight-layer low temperature cofired ceramic substrate, and a high

thermal conducting thin film aluminum nitride FET subcarrier with staggered thermal vias.

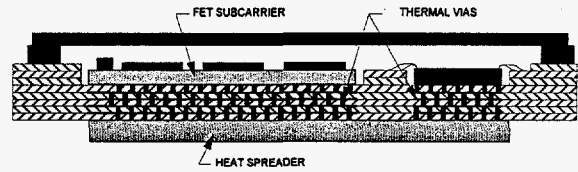


Figure 6. IOM - Package Cross-Sectional View

Conclusions

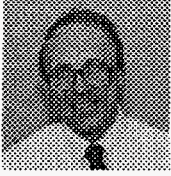
The development of *Design Specifications for Manufacturability of MCM-C Multichip Modules* resulted with an effective reference for creating complex ceramic MCMs within the limitations of the LTCC substrate fabrication, MCM assembly, and electrical testing capabilities. By improving the customer knowledge of the overall process and technology effects on design, the producibility of the MCM was increased before manufacturing was initiated. By involving the customer in the overall design-manufacturing process, design changes and rework could be reduced, and packaging and testing yields could be increased. Adherence to the design rules in the manufacturability guide is expected to produce MCM designs that lead to optimum substrate, assembly, and testing yields and MCMs that can be delivered on schedule at a reasonable cost. This manufacturability guide is expected to expand as the technology and more complex designs evolve, and as new, higher-capability packaging and test equipment develop.

Acknowledgment

The authors wish to express their gratitude to Sandia National Laboratories/New Mexico for their circuit designs.

Reference

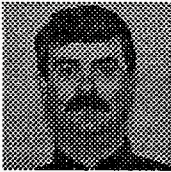
- [1] Chris Allen, Roy Blazek, Jay Desch, Jerry Elarton, David Kautz, Dick Markley, Howard Morgenstern, Ron Stewart, and Larry Warner, *Design Specifications for Manufacturability of MCM-C Multichip Modules*, AlliedSignal Federal Manufacturing & Technologies: KCP-613-5430, June 1995 (Available from National Technical Information Service, U.S. Department of Commerce, 5285 Port Royal Rd., Springfield, Virginia 22161).



Roy J. Blazek received a B.S. degree in electrical engineering from the University of Nebraska, Lincoln, and an M.S. degree in electrical engineering from the University of Missouri, Columbia. He is a Staff Engineer with AlliedSignal Federal Manufacturing & Technologies. He has worked with all phases of microelectronics and most recently has worked on a multichip module technology development team. He has presented several papers at both ISHM and IEEE conferences. Mr. Blazek is a member of ISHM and a Registered Professional Engineer in Missouri.



Jay K. Desch received a B.S. degree in Mathematics from St. Mary of the Plains College, Dodge City, Kansas and a B.S. degree in electrical engineering from Kansas State University. He is currently a Staff Engineer with AlliedSignal Federal Manufacturing & Technologies. He has worked with all phases of substrate fabrication including printed wiring boards, thick and thin film networks, and low temperature cofired ceramic. He has most recently worked on the qualification of assembly processes for multichip module technology.



David R. Kautz received a B.S. degree in electrical engineering from Kansas State University and an M.S. degree in electrical engineering from the University of Missouri, Columbia. He is a Staff Engineer with AlliedSignal Federal Manufacturing & Technologies. He has worked with all phases of electronic product development and production. He has most recently worked on a multichip module technology development team. Mr. Kautz is a member of the International Society of Hybrid Microelectronics.



Howard Morgenstern received a B.S. degree in Ceramic Engineering from Alfred University. He is presently a Staff Engineer with AlliedSignal Federal Manufacturing & Technologies. He has worked in all phases of microelectronics from production to advanced development. He has most recently worked on a multichip module technology development team. Mr. Morgenstern is a member of the American Ceramic Society, National Institute of Ceramic Engineers and International Society of Hybrid Microelectronics.