

CHEMICAL SOLUTION PROCESSING OF STRONTIUM BISMUTH TANTALATE FILMS

C.D.E. LAKEMAN*, T. J. BOYLE**

*Texas Instruments, Inc., P.O. Box 655012, Mail Stop 921, Dallas TX 75265

(Current Address TPL Inc., 3921 Academy Parkway North, NE, Albuquerque, NM 87109)

**Sandia National Laboratories, Advanced Materials Laboratory, 1001 University Blvd, SE

Albuquerque, NM 87106;

081

JAN 21 1999

RECEIVED

ABSTRACT

We describe Chemical Solution Deposition (CSD) processes by which Strontium Bismuth Tantalate (SBT) thin films can be prepared at temperatures as low as 550°C. In this paper, we will present strategies used to optimize the properties of the films including solution chemistry, film composition, the nature of the substrate (or bottom electrode) used, and the thermal processing cycle. Under suitable conditions, ~1700Å films can be prepared which have a large switchable polarization ($2P_r > 10\mu\text{C}/\text{cm}^2$), and an operating voltage, defined as the voltage at which $0.80 \times 2P_{r\text{max}}$ is switched, 2.0V. We also describe an *all-alkoxide* route to SBT films from which SBT can be crystallized at 550°C.

INTRODUCTION

The bismuth layered perovskites, such as $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT), have emerged as leading candidates for use as non-volatile memory elements owing to their remarkable polarization fatigue resistance [1-4]. Much research has been directed at tailoring processing conditions to optimize microstructure and properties for use in such devices [1,2,5]. Target parameters are: switchable polarization, $2P_r > 10\mu\text{C}/\text{cm}^2$; coercive voltage, $V_c < 1\text{V}$; and operating voltage (defined as the voltage at which 80% of the switchable polarization can be switched) $< 2\text{V}$. These parameters indicate the need for thin films ($< 2000\text{\AA}$) for device applications. In addition, to be compatible with standard CMOS circuitry, maximum processing temperatures should not exceed 700°C.

In order to test the feasibility of SBT for such applications, many researchers have turned to chemical solution deposition (CSD) as a straightforward, rapid method of preparing thin films [3, 6-9]. From the various deposition technologies available, several common features emerge: either complex solution preparation is required to dissolve all components, or high processing temperatures (800°C) are needed to remove all organic components and form the required layered perovskite phase. Recently, researchers at Sandia National Laboratories (SNL) have reported a simple process that employs readily available starting materials, and from which single phase, ferroelectric films can be formed on Pt/SiO₂/Si substrates at temperatures as low as 650°C [6,8].

In this paper, we describe experimental strategies to optimize the properties of SBT films prepared by CSD. In particular, details of process developments and optimization will be given, including:

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

- A process for pre-loading the substrate with bismuth which improves the squareness of the ferroelectric P-E hysteresis loops, through better control over stoichiometry in thin films while enabling the processing temperature to be lowered;
- Studies of processing variables, such as film composition, shadow mask top electrode (SMTE) annealing conditions; and
- An ALL ALKOXIDE route to SBT precursors which provides improved solution stability, and enables crystallization of *perovskite* SBT at temperatures *as low as 550°C*.

EXPERIMENTAL

A complete description of the processing route developed at Sandia National Laboratories appears elsewhere [6,8]. Briefly, bismuth acetate ($\text{Bi}(\text{OAc})_3$) was mixed and stirred with pyridine (Py). Separately, strontium acetate ($\text{Sr}(\text{OAc})_2$) and tantalum ethoxide ($\text{Ta}(\text{OEt})_5$) were mixed and dissolved in glacial acetic acid (HOAc). After stirring for ~10 minutes, the separate solutions were mixed together, whereupon the $\text{Bi}(\text{OAc})_3$ dissolved. All solvents used in the process were dried using standard procedures, and all manipulations were carried out in a glove box under a dry argon atmosphere. Prior to deposition of any solution, Pt/SiO₂/Si substrates were cleaned with methanol followed by heating to 400°C for 10 minutes in air. After further stirring of the precursor solutions to ensure complete dissolution, films were deposited by spin-coating at 3000 - 7000 rpm for 30s followed by drying on a hot-plate at 300°C for 5 minutes. After deposition of each layer the films were heated to the desired temperature (typically 700°C) for 30 minutes in flowing oxygen to crystallize the desired perovskite phase. Platinum top electrodes were sputter deposited through a shadow mask, and annealed in oxygen. Ferroelectric properties were measured using a Radiant Technologies RT-66A ferroelectric tester, and surface microstructures examined using a Digital Instruments Nanoscope II atomic force microscope (AFM) in contact mode. Film thickness values were measured using profilometry, and confirmed with scanning electron microscopy (SEM). Standard X-ray diffraction (XRD) was performed on thin films with Cu K_α radiation using a Siemens automated θ - θ powder diffractometer equipped with a diffracted-beam graphite monochromator and a scintillation detector. Parameters for standard scans were a 10-60° 2 θ range, 0.05° step-size and one second count-time. Grazing incidence X-ray diffraction (GIXRD) was also used to examine the phase assemblage of the films. *In situ* high temperature (HT-GIXRD) analysis was performed by using a film treated at 100°C on a hot plate and ramping through various temperatures (8 min/ °C) on a hot stage situated in the diffractometer.

RESULTS

Substrate

We have described the effects of different bottom electrode annealing conditions on SBT microstructures and properties elsewhere [10]. In essence, annealing the platinum at higher temperatures results in films with higher measured polarization values, though coercive voltage values are similar for the two films. XRD data did not show significant orientation or texture differences and the improved properties were attributed to the larger grain size observed in the films deposited on substrates pre-annealed at higher temperatures.

At the typical processing temperatures used for SBT films (~700 - 800°C), significant inter-diffusion between the electrode and film was found to occur (Figure 1). This diffusion caused a change the stoichiometry of the film and led to a deterioration of the properties of the

ferroelectric film, which could potentially compromised device performance. In addition, at high temperature, volatile heavy metal oxide components, such as Bi_2O_3 , can be lost via evaporation with similar consequences. Many researchers have compensated for these phenomena by loading the precursor solution composition with an additional 10 to 20% of the appropriate bismuth component.

In order to overcome these issues, we have developed a novel process to pre-load the platinized SiO_2/Si wafers with bismuth before deposition of SBT [11]. This was accomplished by spin-coating (3000rpm/30s) one coat of a 0.04M solution of $\text{Bi}(\text{OAc})_3$ in a mixture of Py:HOAc (1:2.9 by weight). After heating on a hot plate at $300^\circ\text{C}/5\text{min}$, the wafer was fired at $700^\circ\text{C}/60\text{min}$ in air. Residual Bi_2O_3 was removed using a basic oxide etch (BOE). Typically an entire wafer was Bi-loaded and etched, then cut into smaller pieces as needed. A comparison of P-E loops measured for films deposited onto loaded and not-loaded substrates is shown in Figure 2.

Composition

The SBT structure is flexible in that it allows stoichiometry variations for the Sr and Bi-sites. It has been demonstrated that Sr-deficiency can be compensated by additional Bi which occupies the vacant Sr sites [12]. This composition variation can affect the measured polarization and coercive field values, as shown in Figure 3 for $\sim 2200\text{\AA}$ SBT films. Values of switchable polarization, $2P_r$, reach a maximum for the 10% Sr-deficient composition (SBT 0.9/2.1/2.0), and the coercive voltage for 2200\AA films decreases almost monotonically over the entire composition range studied. However, even though the lowest value of V_c was measured for stoichiometric samples (SBT 1.0/2.0/2.0), the measured $2P_r$ value at this composition was too low for useful device application.

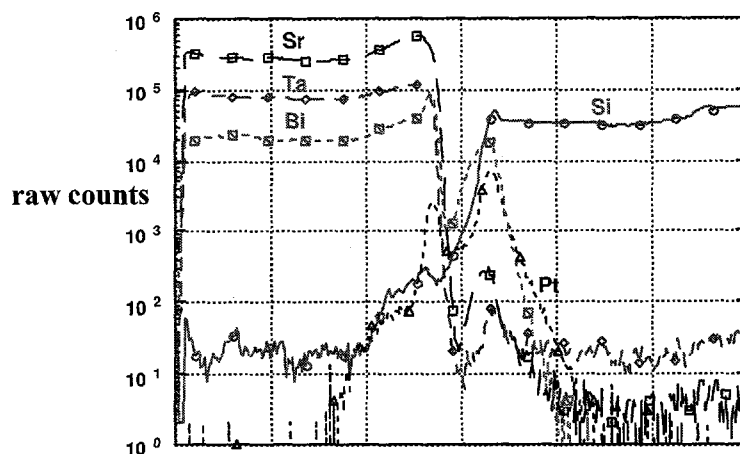


Figure 1 SIMS depth profile of SBT film on Pt/ SiO_2/Si

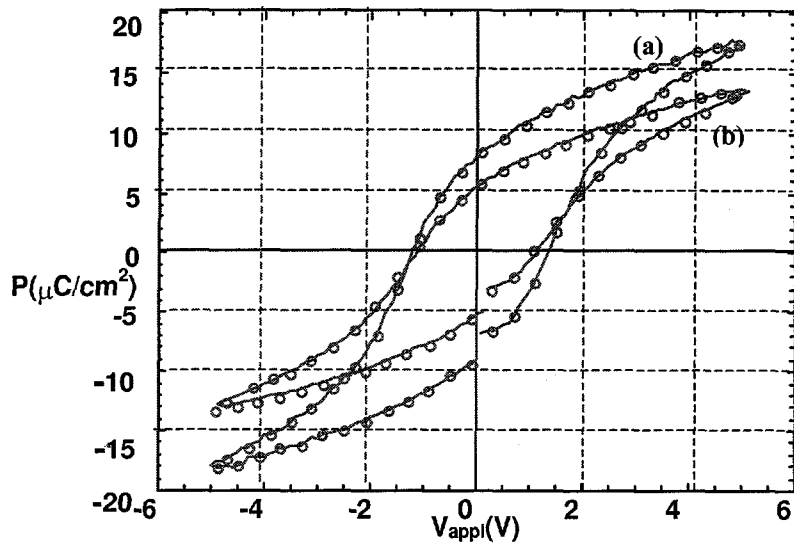


Figure 2 A comparison of P-E loops measured for films deposited onto (a) modified and (b) unmodified Pt/SiO₂/Si substrates.

Processing

Table I lists properties of films prepared with different SMTE annealing conditions, and figure 4 shows representative hysteresis loops. All films were annealed for 30 minutes in oxygen. Annealing at 700°C appears to improve the squareness of the loops, and give higher 2P_r values.

	550 C	600 C	700 C
P _s (μC/cm ²)	14.34	15.71	16.20
P _r (μC/cm ²)	7.41	7.98	9.67
V _c (V)	1.16	1.32	1.18
2P _r (μC/cm ²)	12.17	13.05	18.02

Table I Comparison of SMTE anneal temperature on ferroelectric properties of SBT films.

There are a number of accounts that describe the improvement of ferroelectric properties following a post-SMTE deposition anneal [13-15]. Spierings, *et al.* suggested that annealing following Pt top electrode deposition on PZT films reorients the polarization direction from parallel to perpendicular to the surface of the films, and attributed a marked improvement in switching behavior to this thermal poling process [13]. On the other hand, Noguchi *et al.* reported a decrease in the capacitor shorting rate after post-SMTE deposition annealing at 800°C (the same temperature as the crystallization treatment). They believed this was due to recrystallization of the Pt SMTE during the post-deposition annealing treatment, based on SEM analysis of the Pt layer and the Pt/SBT interface [14]. Watanabe and co-workers found that post-deposition heat treatment for Pt SMTE on SBT films resulted in more symmetric polarization reversal behavior (P-E hysteresis loops) and higher breakdown strength (>300kV/cm) [15]. They reported little difference between annealing at 450°C and 800°C.

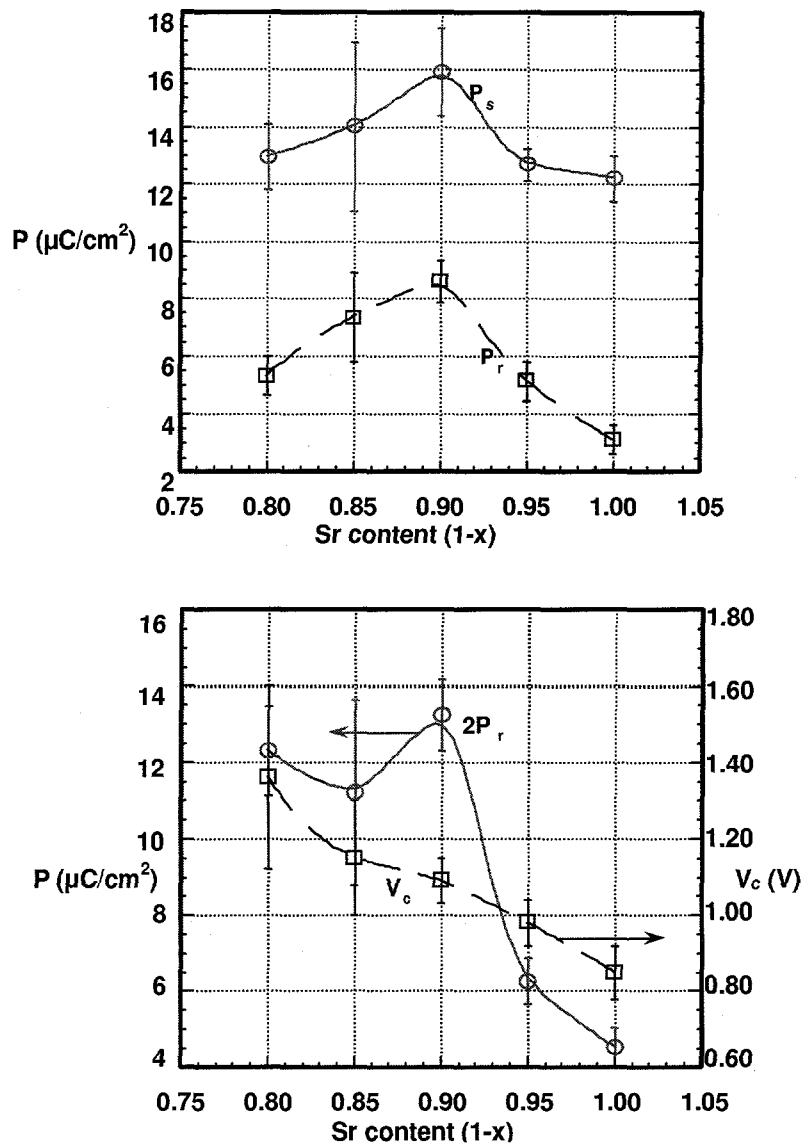


Figure 3 Measured polarization and coercive field values for $\sim 2200\text{\AA}$ SBT films on Pt/SiO₂/Si substrate

In situ measurements of stresses in the SBT films through SMTE anneals to 550°C and 700°C show that the behavior during the heating cycles for both films is quite similar. However, those films heated through 700°C undergo further stress relief at temperatures above 550°C. In other words, annealing to 550°C may not allow all stress relief processes to be completed [10].

In order to minimize the operating voltage, films should be as thin as possible. One of the difficulties associated with processing SBT films is the vermicular microstructure that inevitably leads to an increased probability of electrical shorting as film thickness decreases. The optimum P-V characteristics obtained for a film on a Pt/SiO₂/Si substrate are shown in Figure 5. With a thickness of $\sim 1700\text{\AA}$, $2P_r \sim 10\mu\text{C}/\text{cm}^2$, the applied voltage at which $0.80 \times 2P_r$ max. is switched is $\sim 2.0\text{V}$.

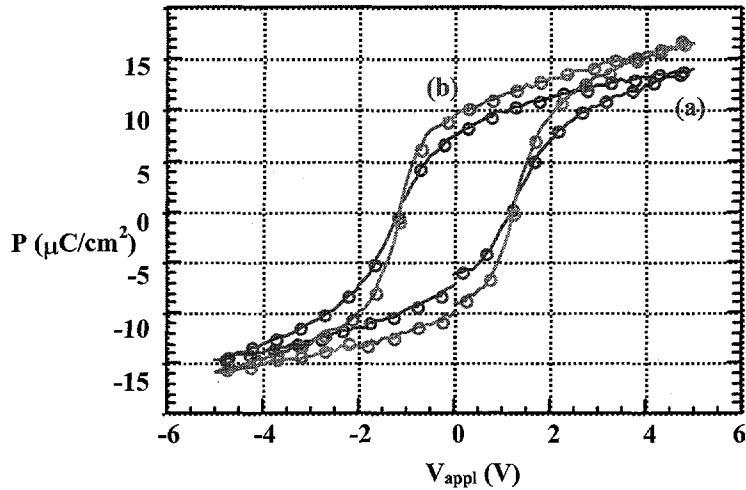


Figure 4 Properties of SBT films prepared under different SMTE annealing conditions: (a) 550°C and (b) 700°C.

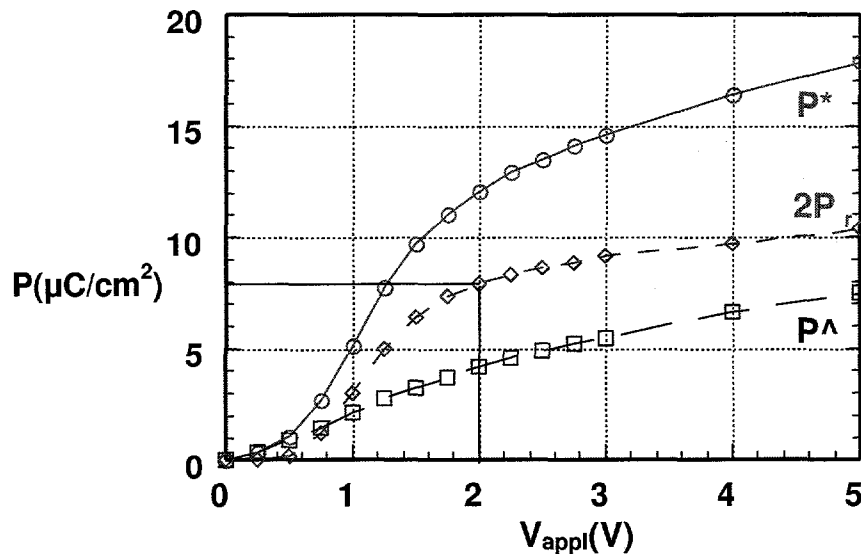


Figure 5 P-V characteristics for a 1700Å SBT film on a Bi-modified Pt/SiO₂/Si substrate.

All Alkoxide Precursor

One of the difficulties associated with this precursor system has been the relatively short shelf life of the precursors (3 days [6]). While this is offset by the ease of solution preparation, there is a need for solutions which display longer stability, and so, an all alkoxide system has been developed using novel, though readily synthesized, bismuth and strontium alkoxides.

$\text{Bi}(\text{OAr}')_3$ was prepared from bismuth amide, $\text{Bi}(\text{N}(\text{SiMe}_3)_2)_3$, and the alcohol ($\text{HOAr} = 2,6$ dimethyl phenol), and $\text{Sr}_5(\text{O})(\text{ONp})_8(\text{THF})_5$ was prepared by direct reaction of strontium metal and excess HONp in THF solvent. To prepare precursor solutions, $\text{Bi}(\text{OAr}')_3$ was slurried in pyridine, forming a pale yellow-green solution. Separately, $\text{Sr}_5(\text{O})(\text{ONp})_8(\text{solv})_5$ was slurried in the same volume of pyridine and stirred. The two solutions were mixed and the resulting green slurry was stirred for 10 min. $\text{Ta}(\text{OEt})_5$ dissolved in toluene was added to the Sr/Bi mixture and allowed to stir for 30 minutes or until translucent. The solution was then used without further modifications.

Films were deposited by spin-coating onto Bi-modified, Pt-coated SiO_2/Si substrates at 3000 rpm for 30 seconds. Between each SBT layer, films were inserted directly into a pre-heated furnace at 550°C for 20 minutes. After the final layer (typical film had 3 layers), the film was fired at the desired temperature for a predetermined amount of time.

HT-GIXRD experiments indicated that the perovskite phase formed as low as 600°C (Figure 6). Based on these data longer processing times at lower temperatures were also examined using *in-situ* HT-GIXRD at 575°C . After ~3 hours the perovskite phase was observed. Lower temperatures over the same time period only produced amorphous films. Using conventional furnace firing, it was determined that the perovskite phase was formed after 24 hours at 550°C (Figure 7).

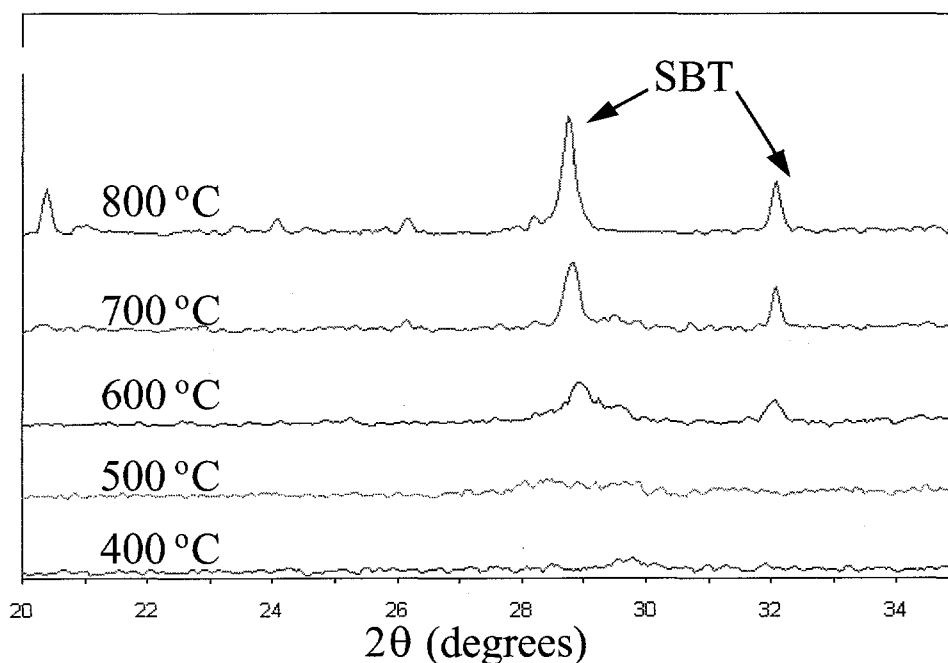


Figure 6 HT-GIXRD of all-alkoxide SBT films on Bi-modified Pt/ SiO_2/Si substrate

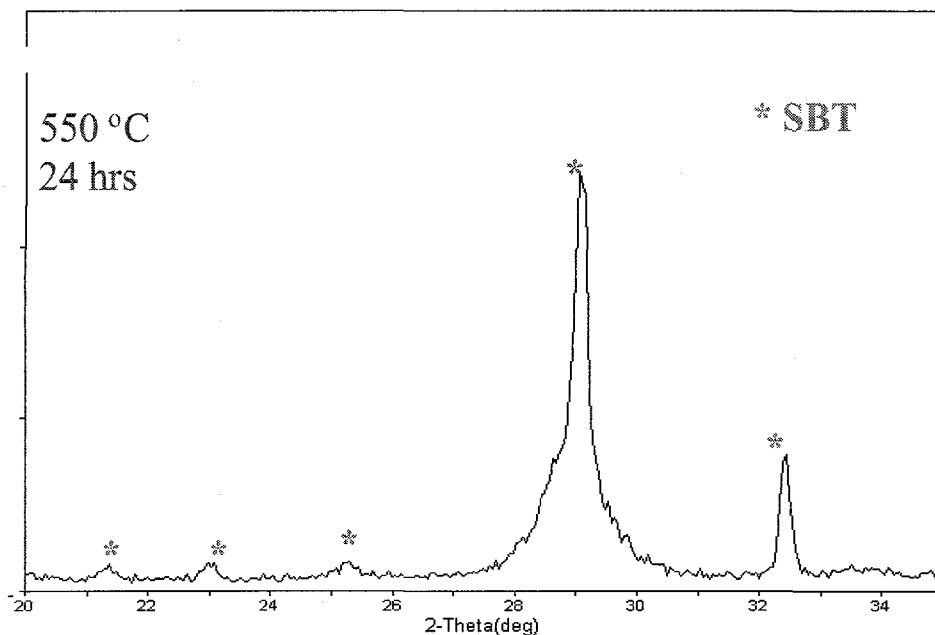


Figure 7 GIXRD of SBT film on Bi-modified Pt/SiO₂/Si. Note perovskite formation at 550°C.

SUMMARY

We have prepared (SBT) films using a chemical solution deposition. Substrate preparation and microstructure, film composition and control over post-SMTE thermal processing have been optimized to tailor film properties to meet parameters suitable for integration. Pre-loading Pt substrates with Bi before deposition of the SBT films helps to improve control over film stoichiometry, and can lead to improved properties. Precursors to enable an all-alkoxide process have been developed, from which perovskite films have been crystallized at temperatures as low as 550°C.

ACKNOWLEDGEMENTS

This work was supported by Texas Instruments, Inc. and the United States Department of Energy under contract DE-AC04-94AL85000. Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy. We would like to acknowledge the assistance of B.A. Hernandez, and C.D. Buchheit of Sandia National Laboratories, and Drs. S. Summerfelt, T. Moise, and S. Yamanaka of Texas Instruments.

REFERENCES

1. See for example, Ferroelectric Thin Films IV and V, Mater. Res. Soc. Symp. Proc., **361** and **433**, (1995, and 1996).
2. See also, Proc. IX ISIF, Santa Fe, NM, March 3 - 5, 1997, Eds. D.B. Dimos, and B.A. Tuttle, in *Integrated Ferroelectrics*, **17, 18**, (1997).

3. R.E. Jones, P. Zurcher, P. Chu, D.J. Taylor, Y.T. Lii, B. Jiang, P.D. Maniar, and S.J. Gillespie, *Microelectronic Engineering*, **29**, 3, (1995).
4. H.N. Al-Shareef, D. Dimos, T.J. Boyle, W.L. Warren, and B.A. Tuttle, *Appl. Phys. Lett.*, **68**, 690, (1996).
5. T. Noguchi, T. Hase, and Y. Miyasaka, *Jpn. J. Appl. Phys.*, **35**, 4900, (1996).
6. T.J. Boyle, C.D. Buchheit, M.A. Rodriguez, H.N. Al-Shareef, B.A. Hernandez, B. Scott, and J.W. Ziller, *J. Mater. Res.*, **11**, 2274, (1996).
7. K. Amanuma, T. Hase, and Y. Miyasaka, in Ferroelectric Thin Films IV, *Mater. Res. Soc. Symp. Proc.*, **361**, 21, (1995).
8. T.J. Boyle US Patent 5 683 614, (1997).
9. I. Koiwa, K. Tani, J. Mita, T. Iwabuchi, *Jpn. J. Appl. Phys.*, **37**, 192, (1998).
10. C.D.E. Lakeman, T.J. Boyle, J.A. Ruffner, *J. of Sol-Gel Sci.*, In Press, (1998).
11. A patent application by C.D.E. Lakeman and T.J. Boyle has been filed by Texas Instruments on this process (1998).
12. T. Noguchi, T. Hase, and Y. Miyasaka, *Integrated Ferroelectrics*, **17**, 57, (1997).
13. G.A.C.M. Spierings, G.J.M. Dormans, W.G.J. Moors, M.J.E. Ulenaers, and P.K. Larsen, *J. Appl. Phys.*, **78**, 1926, (1995).
14. T. Noguchi, T. Hase, Y. Miyasaka, *Jpn. J. Appl. Phys. Part 1*, **9B**, 4900, (1996)
15. K. Watanabe, M. Tanaka, N. Nagel, K. Katori, M. Sugiyama, H. Yamamoto, and H. Yagi, *Integrated Ferroelectrics*, **17**, 451, (1997).