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A DSP BASED DATA ACQUISITION MODULE FOR COLLIDING BEAM ACCELERATORS*

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Abstract

In 1999, the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory will accelerate and store two beams of gold ions. The ions will then collide head on at a total energy of nearly 40 trillion electron volts. Attaining these conditions necessitates real-time monitoring of beam parameters and for this purpose a flexible data acquisition platform has been developed. By incorporating a floating point digital signal processor (DSP) and standard input/output modules, this system can acquire and process data from a variety of beam diagnostic devices. The DSP performs real time corrections, filtering, and data buffering to greatly reduce control system computation and bandwidth requirements. We will describe the existing hardware and software while emphasizing the compromises required to achieve a flexible yet cost effective system. Applications in several instrumentation systems currently under construction will also be presented.

I. INTRODUCTION

Like other modern accelerators, RHIC will be well instrumented at commissioning[1][2]. This instrumentation consists of several thousand digitizers distributed over a 3.8 km tunnel and producing an aggregate data rate of nearly one gigabyte per second. Most of these channels sample filtered pulses with a 100MHz analog bandwidth, thus requiring the digitizers to be located near the signal source[3]. To deal with the resulting data rates, most instrumentation systems will include a digital signal processor followed by a memory buffer that is shared with a VME-based single board computer. In RHIC, the VME system is the first hardware layer in the distributed control system. The DSP in an instrumentation module provides the following functionality:

- Filtering that can decrease the data bandwidth to the control system
- Corrections and calculations that decrease the computational load on the control system
- Local circular buffer management to provide a flight recorder
- Software flexibility to present data from various I/O modules in a consistent manner

II. DSP BOARD DESCRIPTION

The DSP data acquisition module is physically incorporated on a single width 6U VME standard printed circuit board. It may be installed into a standard VME crate, or as one-half of a VXI module, as has been done for current applications. Figure 1 illustrates the block diagram of the design. Listed below are the highlights of the board which will be described in order.

- Motorola DSP96002
- VME/VXI interface
- 4Mbytes Static RAM
- 128Kbytes FLASH memory
- Accepts 4 Industry Pack (IP) Modules

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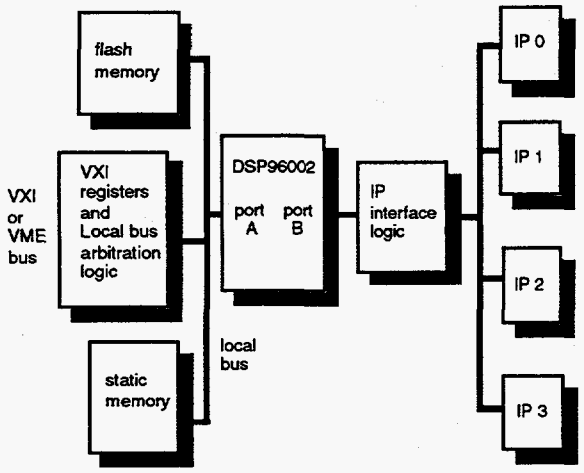

Figure 1. DSP Board Block Diagram

A. Architecture Overview

The centerpiece of this module is the Motorola 96002 32 bit floating point DSP. The 96002 boasts 16.5 million instructions per second (MIPS), and 49.5 million floating point operations per second (MFLOPS). In addition to its strong performance characteristics, it provides two 32 bit I/O ports, shown as port A and port B in Figure 1. These two ports permit independent handling of the raw data input from the Industry Packs (port B), and the post-processed data awaiting upload to the control system through VME in the static memory (port A).

The module provides a full 32 bit slave interface which conforms to the IEEE-1014-87 specifications. The necessary VXI registers have also been implemented for compatibility in a VXI environment. The interface to the VME bus is a simple memory map which provides easy data readout and control to the control system. The VME bus has full read and limited write access to the Static and FLASH memories. The memory map as seen from the VME bus is shown in figure 2. Arbitration for the local bus is performed between the DSP and VME bus with the DSP having higher priority. This priority scheme was chosen to allow the greatest overall DSP performance possible. Due to the asynchronous nature of VME transfers, it remains unaware of this arbitration and only its acknowledge signal is delayed until it can gain access to the local bus

The on-board memory consists of both static ram and flash memory. The static ram has multiple sources and is packaged in 64 pin zigzag JEDEC standard modules, permitting easy installation and upgrade. A maximum of four of these memory modules may be installed in sizes of 256kbytes, 512kbytes, or 1Mbyte each. Two size identifying pins on the memory modules themselves allow the hardware to automatically configure itself to the installed size. Since static memory can become expensive the DSP board allows installation of a single 64kbyte memory module for cost sensitive applications, or the installation of four 1Mbyte memory modules for more demanding applications. The on-board flash memory provides a nonvolatile area for program instructions and any necessary permanent coefficients, etc. It provides eight lockable sections, so that a core level program may be locked into a section to prevent inadvertent changes.

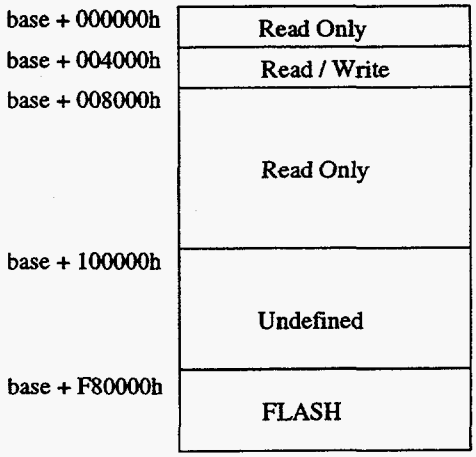

Figure 2. VME Memory map

What helps makes this board a versatile data acquisition board is its use of a mezzanine cards known as Industry Pack Modules. This interface was developed by Greenspring Computers, and provides a versatile, modular approach for implementing a wide range of I/O, control, interface, analog and digital functions. Up to four of these Industry Pack Modules may be installed on the DSP board while still occupying only one VME slot.

B. Performance Characteristics

The performance of the DSP board can be characterized by the performance of the DSP itself, along with its I/O throughput with both the SRAM and the Industry Packs. Some performance issues of the DSP itself were listed above, and now the I/O performances of the DSP that were accomplished will be mentioned. On port A of the DSP are the SRAM modules. They are accessed with a single wait state giving a maximum throughput of 42Mbytes/sec, and may have internal access times up to 45ns. On the other port are the Industry Pack Modules. The maximum throughput achieved with the Industry Packs at 8Mhz is 5.3Mbytes/sec. This can be doubled to 10.6Mbytes/sec with a double wide industry pack. The Industry Pack specifications also specifies (preliminary) a 32 Mhz interface, which has been implemented on two of the slots, giving a throughput of 12.8Mbytes/sec. (25.6Mbytes/sec for double wide Industry Pack).

C. Future Directions

The next step required for this data acquisition system is to provide a simple, cost effective way to off-load the processed data upstream to the control system for further analysis. The current implementation of the DSP board provides a VXI interface which is proving to be a restrictive and expensive packaging standard for the planned 600+ nodes. A possible alternate approach is the use of a high speed serial bus, which are quickly gaining popularity over parallel interfaces. One such serial bus currently being investigated and proves to be a likely candidate is IEEE-P1394. Some features of this bus are:

- 100, 200 or 400 Mbits/sec bandwidth
- asynchronous or isochronous data transfer
- simple memory mapped interface (64 bit address)
- inexpensive

A P1394 serial bus approach would eliminate the need for prohibitively expensive VXI crates which can only accommodate 12 nodes per crate. It will then be possible to locate the data acquisition hardware even closer to the signal sources, thus improving channel to channel phase match by reducing the length of costly signal transmission lines.

The evaluation of the P1394 serial bus is proceeding by implementing it as an Industry Pack Module. This permits the existing DSP boards to be used as the test bed. This Industry Pack interface, whose performance was described above can provide over 200 Mbits/sec throughput (32MHz, 32 bit-wide data configuration), enough to fulfill the current P1394 realization of 100Mbits/sec. If P1394 proves a viable alternative, it could then be directly built into the DSP boards in lieu of the VXI interface.

A backup approach to network these DSP boards to the control system is to use IEEE802.3 ethernet. Commercial Industry Pack modules with this interface currently exist as well as the software needed for the DSP to quickly obtain UDP/IP connections.

Another topic under consideration is the elimination of the general purpose DSP all together. With the advances in both logic synthesis and reprogrammable FPGA's, we are considering the possibilities of versatile, reconfigurable, hardware implementations of the signal processing and their viability for higher bandwidth applications using high level HDL's.

III. APPLICATION EXAMPLES

The number of digitizer channels serviced by a single DSP board depends on the digitizing rate and the complexity of the signal processing algorithm. Examples are summarized in Table 1. The Injection position monitor system is in production and will be commissioned beam in late 1995. A prototype of the collider ring position monitor module has been tested but production will not begin until 1997. A loss monitor module has not yet been constructed. The two variations of position monitor systems will be described. These two systems share the same sampling detector design, but use different digitizers, different timing system interfaces, and run different DSP software. Nevertheless, the results are presented to the control system in identical data structures.

Table 1: Typical Data Rates

Application	Digitizer Channels per Module	Peak Digitizer Sample rate (Sa/s)
Injection Line Position monitors	24	30
Ring Position Monitors	4	78k
Ring Loss Monitors	8	20k

D. The Injection Line Position Monitor

The electronics for this system consists of the two VXI modules shown in Figure 3. The beam position monitor (BPM) couples electromagnetically to packets (or bunches) of ions travelling in the vacuum chamber. This produces a pulse several volts in amplitude and a few nanoseconds wide that is then sampled by the analog front end. Because of the low data rate in the injection line, a single DSP board can service multiple analog VXI modules. Software for the injection line application can be summarized in the following routines:

- The acquisition routine runs upon interrupt from the 16 bit digitizer (about 30 Hz):
  - Raw values are corrected to 3rd order.
  - Position and amplitude for each bunch are calculated.
  - The buffer pointer and a bunch counter are updated.
  - Results are stored in a circular buffer residing in shared static memory.
- The housekeeping routine is run on interrupt from timing system:
  - Values of the buffer pointer and bunch counter are stored (part of scheme to synchronize buffers of geographically separated modules).
  - Changes to settings are read from shared memory and applied.
  - If the appropriate bit is set, a self calibration is performed.

E. Collider Ring Position Monitor

The ring system is very similar to the injection system except that each bunch in the ring returns to the same monitor at a 78 kHz rate. Because of the high data rates

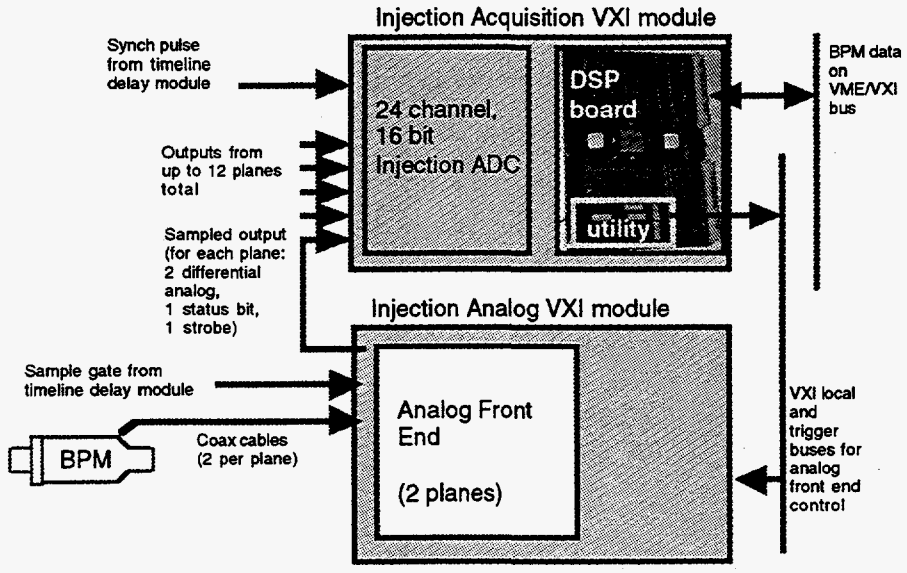

Figure 3. Block diagram depicting the 24 channel application

(turn by turn) of the ring system, a DSP board only services four digitizing channels. Also, the DSP software is synchronized to the beam synchronous timing system. This special timing interface resides on one Industry Pack while the 4 channel, 16 bit digitizer fits on another. The two planes of analog front end consist of two samplers each and reside in the front of the C-size VXI module. The DSP software for this module can be summarized as follows:

- The acquisition routine runs upon interrupt from the digitizer (about 78 kHz):
  - This routine is similar to injection line acquisition routine, but in addition, the calculated values and their squares are both accumulated.
- The statistics routine is run on interrupt from the timing system (usually at the synchrotron frequency - a few hundred Hz max.):
  - Average and variance of amplitude and position are calculated.
  - Results are stored in a separate circular buffer.
  - Pointers and counters relating to this circular buffer are updated.
  - The accumulators are cleared in preparation for the next averaging period.
- housekeeping routine is similar to the injection line version

IV. ACKNOWLEDGMENTS

The authors thank S. Rankowitz and the staff at the BNL Instrumentation Division for producing the DSP board.

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