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Integratible process for fabrication of fluidic microduct networks on a single wafer

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ABSTRACT

We present a microelectronics fabrication compatible process that comprises photolithography and a key room temperature SiON thin film plasma deposition to define and seal a fluidic microduct network. Our single wafer process is independent of thermo-mechanical material properties, particulate cleaning, global flatness, assembly alignment, and glue medium application, which are crucial for wafer fusion bonding or sealing techniques using a glue medium. From our preliminary experiments, we have identified a processing window to fabricate channels on silicon, glass and quartz substrates. Channels with a radius of curvature between 8 and 50 µm, are uniform along channel lengths of several inches and repeatable across the wafer surfaces. To further develop this technology, we have begun characterizing the SiON film properties such as elastic modulus using nanoindentation, and chemical bonding compatibility with other microelectronic materials.

Keywords: microduct, microchannel, microfluidic, integratible microchannel, sealed microchannel, microfabricated channel, MEMS microchannel, elastic modulus

1. INTRODUCTION

Fabrication of bulk microelectrical-mechanical systems (MEMS) involves advanced microelectronic processes to configure structures in three dimensions by thick resist photolithography, selective wet etching, deep plasma etching, and novel sealing techniques. Some advantages of MEMS are low fabrication cost, low power consumption, robustness, portability, and accessibility. Advanced fluidic MEMS sensors for applications in medical, biochemical, forensic, industrial, and environmental areas require processing to include a microduct network as well as electronics, transducers, and detectors to complete the working device. These sensor devices are sometimes referred to as 'micro-chemlab' on a chip. [1]

Networks for transporting fluids have been challenging to fabricate using established technologies due to the built-in processing issues of: 1) sealing fluidic networks, 2) chemical compatibility of fluids with microelectronic materials, 3) new technologies associated with fabrication of materials other than silicon, 4) voltage potentials that are significantly higher than IC's for operations like electrophoretic separations, 5) design and material optimization for thermal budgets, and 6) fluidic packaging integration. A common fabrication approach has been to etch the channel design in a substrate that is compatible with the application requirements followed by sealing the channel network with a second cover slip wafer. The relatively larger channel dimensions in the 10's of microns range that are required to accommodate sample volumes for detection are easier to configure in hybrid materials like glasses and quartz, and these larger features are also easier to align with the cover slip wafer, but larger features create severe aspect ratios that make post fabrication of IC's difficult using current technologies. IC fabrication is also difficult with two wafer sealing techniques. To alleviate many of the difficult issues associated with fabrication of a microfluidic system, we are developing a single-wafer thin-film technology inherently unlike the two wafer systems which we have also explored and briefly discuss.

2. TWO WAFER BONDING PROCESSES

Methods for sealing two wafers together involve either a glue medium or thermal fusion bonding. For the glue medium case, microvolumes of solution must be uniformly applied to all the sealing surfaces sized in the range of microns to mils. This application can be difficult due to interdependence of glue viscosity with surface tension and surface configuration. For simple bonding configurations, surface tension can be a useful driving force for applying a controlled volume of glue to the interface area between pieces in physical contact. Another approach to applying a glue medium, utilizes a photodefinable polyimide to pattern a seal bead around areas that require bonding. Application of polyimide seal beads near channels

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polyimide to pattern a seal bead around areas that require bonding. Application of polyimide seal beads near channels configured in the substrate or around via holes through a substrate, can be difficult due to nonuniformity in polymide film thickness that arises from spin coat application over severe topographies typical of MEMS. Although polyimide material is resilient. gaps due to seal-bead height differences are difficult to seal even when pressure is applied to the assembly.

Another polyimide sealing problem we encountered was outgasing of the patterned material during the cure, which created trapped gas and areas void of glue. These effects are shown in Fig.1a; the dark colored finger areas and the dark edge of the polyimide pattern at the channel edge are sealed areas. Profilometer measurements show that the patterned polyimide edges swell vertically by approximately 5% during heating, which we believe accounts for the preferential bonding at the pattern edges. Using these results, the narrow polyimide pattern shown in Fig.1b was designed to enhance bonding and minimize large areas that can trap gases. Although our modification pattern greatly enhanced channel sealing, global warp was a problem, alignment was difficult, and assemblies tended to be fragile.

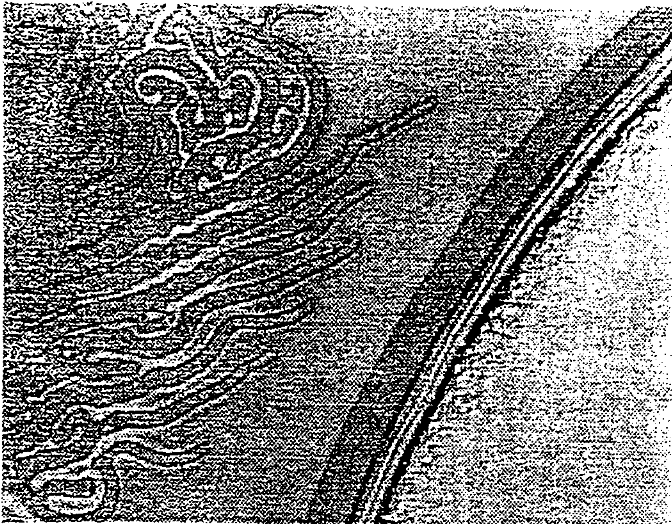

Figure 1a Wide area polyimide has trapped gases and sealed edges

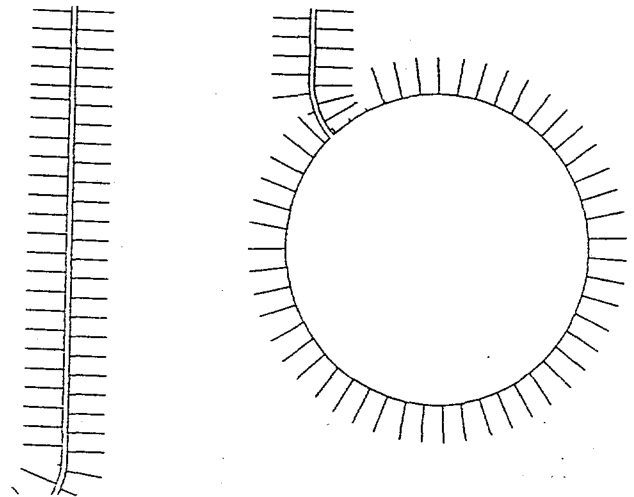

Figure 1b Narrow polyimide seal bead

We developed another glue medium process that utilized thin-film solder.[2] For this fabrication approach, indium solder film was patterned on one wafer and a gold film for wetting solder on a glass second wafer of the assembly. The process includes: a thin 200 Å gold film deposition after the solder film deposition to inhibit oxidation, a blanket metallization on the back of the glass wafer to adequately contact and enhance heat transfer to the assembly, and special fixtures in the vacuum bonding chamber, to ensure flatness, heat containment, and pressure contact. In addition to the factors mentioned, solder reflow optimization required characterization of solder film configuration, film thickness, bonding time, and bonding temperature. All of these issues made this bonding technique a complex process.

Fusion or thermal bonding is a high temperature process that produces chemical bond between wafers. Substrates to be bonded must have thermal coefficients of expansion (TCE) that are reasonably matched and materials that are preprocessed on the wafers must be thermally compatible. Fusion bonding of silicon is typically performed at 700C or higher[3] and for fused silica or quartz, bonding temperatures are from 1000C to 1200C.[4] For bonding like substrates of glass, fused silica and quartz, we have experimented with lower temperature fusion bonding at 600C for 4 hours. This heating schedule was adequate for soda lime glass and Pyrex, since assemblies fractured in the substrate rather than at the interface during pull testing. Although the pull test forces for fused silica and quartz samples were similar to those of the glasses, unlike the glasses, these samples failed at the interface. From these tests, we found that bonding does occur at lower temperatures for fused silica and quartz, but depending on the application, more aggressive heating schedules may be required to bond the interface area to the extent that it resembles the bulk. In addition to the thermal requirement, successful fusion bonding demands pristine surfaces that are free of particulates and are flat locally and globally. To alleviate the particulate issue. we utilized room temperature bonding similar to that reported by Bengsston[3] for our transparent substrates, to locate particulates, and if necessary, to pull the assembly apart and reclean surfaces, before permanent thermal bonding. We also configured our wafers by etching-back large areas that did *not* require bonding, to minimize pristine bonding areas. Finally, to address global warp, we used comparatively thin substrates (20

(20 mils thick). In utilizing these techniques, we were able to bond 3 inch assemblies of Pyrex and fused silica, but the inherent difficulties of fusion bonding limit its application.

Finally, anodic bonding is employed since bonding temperatures are relatively low from 200C to 400C and particulate cleanliness is somewhat relaxed. In this technique, an electric potential is applied across the aligned assembly that contains a glass wafer with mobile ions and a metal or semiconductor that has a reasonable TCE match to the glass. Static bonding occurs as the ions diffuse out of the glass forming a depletion region, and a secondary bonding mechanism is interfacial oxidation.[5] This bonding technique is widely used, but it has limitations due to material property specificity.

3. MICRODUCT FABRICATION PROCESS

Our microduct fabrication comprises benign processing steps that are compatible with preprocessed thin films and does not involve the two-wafer assembly. A photolithography step determines the size, shape and extent of the microduct system on the wafer. The channel design patterned in photoresist can be either on the wafer surface as demonstrated in our present experiments or in channels that have been previously etched into the wafer.[6] In either case, the subsequent channel formation replicates the entire resist pattern including any design provisions that may be included for packaging schemes to introduce fluids into the channel network.

The second processing step is a room-temperature blanket deposition of an electron-cyclotron-resonance (ECR) silicon oxynitride (SiO_xN_y) film, which forms the walls of the subsequent channel network. High density plasmas have electron, ion and radicals that are up to 10^3 times higher than in conventional rf low density plasmas, and the high degree of dissociation permits room temperature deposition of high quality films. The room temperature aspect of this plasma process is key to this technology, since heating of the sacrificial resist is minimized and, consequently, resist is easily removed in the subsequent process step.

To develop this technology, an array of test channels was fabricated on silicon, glass and quartz substrates. For the photolithography step, we chose AZ9260 photoresist to produce a relatively thick 30-μm film by a double spin process, and a photomask with nominal line widths from 5 μm to 500 μm. Small line patterns were difficult to hold on the transparent glass and quartz samples and only 50, 75, 100, 150, 200, and 500 μm wide lines remained on these surfaces. The silicon sample contained 25, 15, and 10 μm lines in addition to the wider line sizes. After development, resist was reflowed at 130C for a short (20 second) time period to minimize resist baking and to produce the hemispherical shape shown in Fig.2, that has reduced vertical surface areas and no corners, which are more difficult for uniform film coverage. The last resist step was a 4 minute oxygen plasma clean at 5 Watts to remove thin residual resist film from areas that are cleared in the develop step.

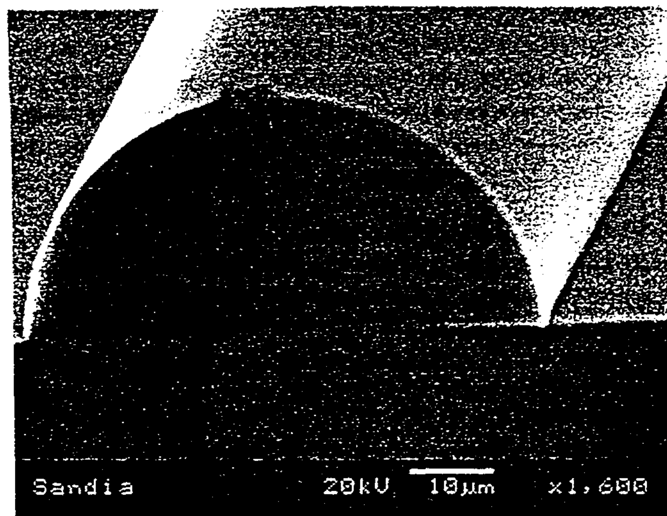

Figure 2. A resist pattern, that was initially 30 μm thick and 50 μm wide, was reflowed with gentle heating to form a near perfect hemispherical cross section, that has a 29 μm radius of curvature.

Samples were mounted on the ECR sample carrier using a thermally conductive material (MUNG II), and depositions were performed at rates of about 1 μm/15 minutes to produce films 2, 3, and 4 μm thick. After the deposition, samples were soaked in an acetone bath for about 6 hours to remove the resist through the ends of the channels at the wafer edges. Acetone

easily removes the resist and problems such as stiction were not noted. (Stiction is a problem associated with removing liquid from a narrow gap between large area surfaces.)

4. EXPERIMENTAL RESULTS

Critical processing parameters our for channel fabrication are extent of resist baking, cross sectional profile of patterned resist, ratio of resist cross-section to channel length, and substrate temperature during deposition. These parameters address two major issues inherent in our process: intrinsic film stress and radiative heating during plasma deposition. From our array of fabricated materials and channel sizes, we identified a processing window to fabricate channels that were uniformly shaped along the channel length, free of resist on the inside areas and repeatable across the wafer surface. These channels that extended across the wafer, were in the following width ranges. For silicon, channels were fabricated from nominal line widths of 10 to 100 μm (for example, the scanning electron micrograph (SEM) in Fig.3). For glass, channels were from 50 to 100 μm lines widths, and for quartz, one channel from a 50 μm wide line

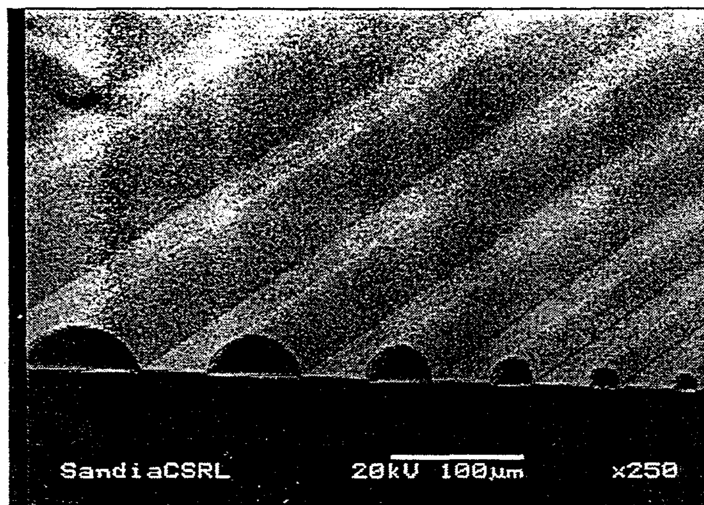

Figure 3 SEM of channels formed by deposition of 3 μm of room temperature SiON plasma film on patterned photoresist that was reflowed and subsequently removed.

Outside the processing window, channels were damaged by intrinsic film stress and resist heating. Resist heating was especially pronounced for: 1) channels on quartz and to a lesser extent channels on glass, that were heated more aggressively due to low thermal conductivity of these substrates; 2) larger channels that have greater resist volume per unit surface area of substrate; and 3) thicker 4 μm SiO_xN_y film that requires a longer film deposition time. We noted evidence of resist solvent outgasing and apparent bubble formation, that burst the SiON film as shown in Fig. 4 for a 75 μm wide channel on quartz. Process parameter changes to reduce the heat damage we observed for these channels could include: 1) backside metallization using E-beam evaporation to enhance contact of the substrate to the sample stage and thereby transfer heat away from the substrate, 2) increase the bake time of to the resist so solvents are outgased to a greater extent prior to SiO_xN_y deposition, or/and 3) increase the cooling rate of the sample stage in the chamber.

Channel size limitations with respect to intrinsic stress were clearly noted from the 150-μm and 200-μm channels on the silicon substrate. The SEM of one of these channels in Fig. 5, shows film stress damage by the regular pattern of breaks that occur along the channel length. From the configuration of these breaks, the film appears to be growing in a state of tensile stress and eventually fractures, since it cannot compress the underlying resist material. We did not see evidence of buckling which would indicate compressive stress failure. Stress degradation was not evident in the narrower channels, that have a cross section closer to that of a hemisphere as shown in Fig. 6a, 6b, 6c, and 6d. The channel in Fig. 6b with a 35-μm radius of curvature has a hemispherical cross section. The channel in Fig.6a is less than hemispherical and those in Fig. 6c and Fig. 6d are greater than hemispherical. For similar hemispherical shapes to form during the resist reflow step for wide channels, process characterization would be required for a thicker resist films.

For fabrication of narrower long channels, photoresist removal may the limiting process parameter. The narrowest channels in our test array (Fig. 6d) were 2 to 3 inches long, and resist removal was complete after the 6 hr. soak. Channels sized smaller than our array may be more useful to characterize resist removal.

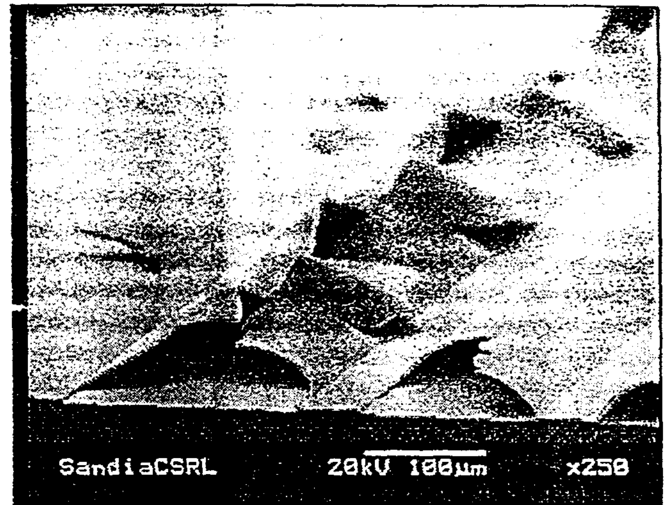

Figure 4. Channel damage due to photoresist heating on quartz wafer.

Figure 5. Wide channel on silicon with regular breaks in the stressed film

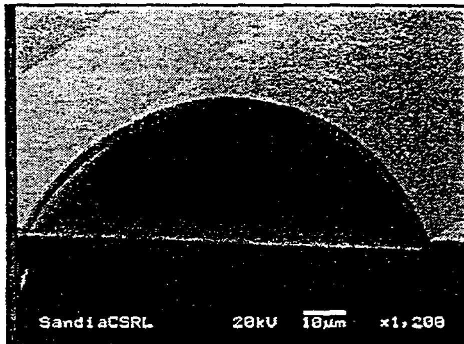

Figure 6a Radius is 52µm

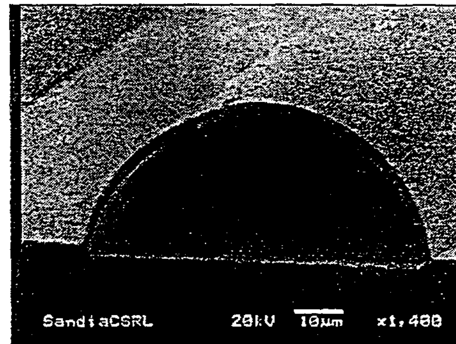

Figure 6b Radius is 35µm

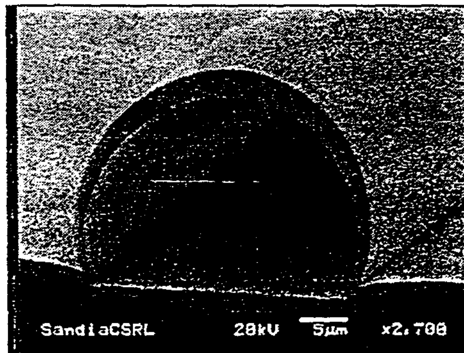

Figure 6c Radius is 15 µm

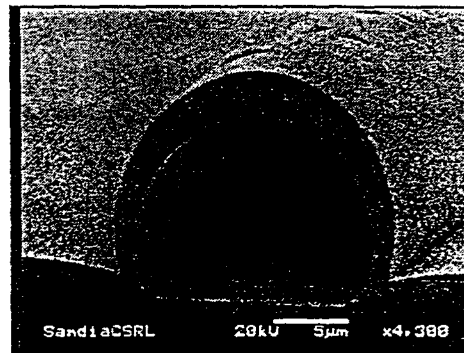

Figure 6d Radius is 8 µm

5. SiO_xN_y FILM MECHANICAL PROPERTIES

From recent reports, amorphous films can exhibit high strength and ductility.[7] Our wafer (fabricated with amorphous SiO_xN_y film) shown in Fig. 3 and 6 was notched then broken perpendicular to channels. Next, samples were dropped from a distance of about 1 ft. first face-up and then again face-down to test mechanical robustness. From close SEM inspections of the channels, film cracking was not noted as a result of the preparation treatment and these channels that are basically composed of film on three sides, appear to be quite robust. Mechanical durability is of interest for MEMS devices, and we have begun investigating the mechanical properties of the SiO_xN_y film by elastic modulus measurement.[8]

The elastic modulus of the SiO_xN_y film was measured by nanoindentation using interfacial force microscopy (IFM). These relatively new nanoindentation measurement techniques are ideal for microfeatures, since information about mechanical properties of materials can be provided at a very localized nanoscale, i.e. measurement of intrinsic material properties are apart from defects, in contrast to former bulk techniques, that averaged effects from inclusions, pores, etc. An additional advantage of the this particular IFM nanoindentation measurement technique is accuracy, since it is distinguished by an electrostatically driven force feedback system that eliminates mechanical instabilities inherent in all other compliance-based force sensor designs.[9]

To measure mechanical response, the sensor probe is pushed into the surface to get force vs. displacement information. Because we are interested in the elastic modulus, our measurement was of the simple elastic response that does not involve plastic flow (permanent damage) to the surface, and indeed elastic response is verified by the force profiles in Fig 7a and 7b, which do not have a hysteresis loop associated with plastic deformation. The silicon sample is included in our measurements in order to back calculation the SiO_xN_y elastic modulus. The silicon and SiO_xN_y samples were measured sequentially and then repeated to verify that the profiles were not changing due to probe tip wear. For our samples, the probe displacement for the SiO_xN_y film at 60 Å, is a small fraction of the total SiO_xN_y thickness of 2 mm (20,000 Å), and therefore the elastic response of the underlying silicon substrate is not included. For the case of the silicon, the thin native oxide (~20 Å thick) does not enter into the elastic response of that measurement.

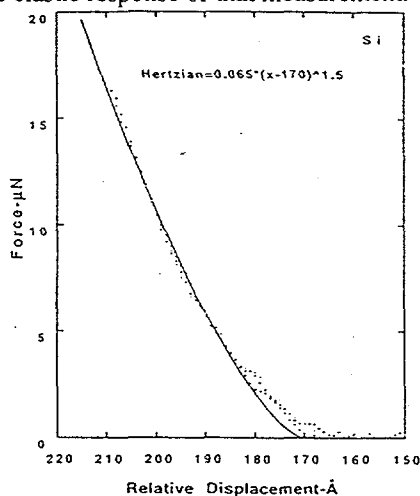

Figure 7a Force Profile of silicon with native oxide

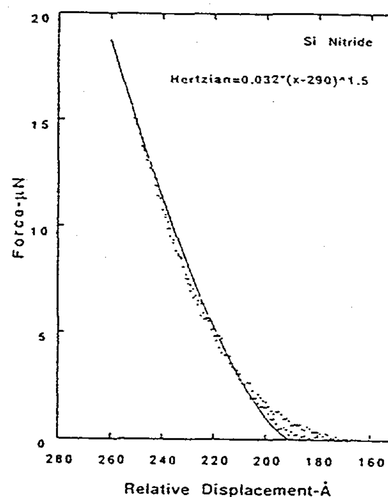

Figure 7b Force profile of SiON film

From the force profiles, Young's modulus of the SiO_xN_y film is calculated as follows.[9] The elastic force profiles are mathematically fit to the Hertz continuum elastic model of a sphere elastically contacting a flat surface.[10] The constant derived from the curve fit, referred to as the Hertzian (at the top of the Figs. 7a and 7b.), contains the radius of curvature of the probe, R, and the indentation modulus E*. The elastic response relationship of the curve is given in equation (1).

$$F = {}^4/_3\, R^{1/2} E^* d^{3/2} \quad (1)$$

where the Hertzian,

$$H = {}^4/_3\, R^{1/2} E^* \quad (2)$$

The indentation modulus, E*, contains mechanical properties of the tungsten probe and that of the sample, and is given by:

$$\frac{1}{E^*} = \frac{(1 - v^2_{Si})}{E_{Au}} + \frac{(1 - v^2_W)}{E_W} \quad (3)$$

where v_{Si} and v_W and E_{Si} and E_W are the Poisson's ratios and Young's moduli of silicon (or SiO_xN_y) and tungsten.

The probe radius of curvature, R, was calculated from the silicon data using equation (2). The Hertzian, H(Si), is known from the silicon profile curve fit and E*, the indentation modulus, for the silicon case can be calculated using equation (3) and the known mechanical properties of silicon and tungsten. (Table 1) From the calculation, the probe radius of curvature was 2600 Å, which is in the size range of probes measured using SEM.

Using the calculated radius of curvature, R, and the Hertzian for the SiO_xN_y measurement, $H(SiO_xN_y)$, the indentation modulus, E*, can be calculate for the SiO_xN_y measurement. The elastic modulus of SiON is finally back-calculated from equation (3), using the known mechanical properties of tungsten, and from our calculations this value is 51.

Mechanical property measurements of thin deposited films have been reported just in the past few years, and only a few values are available for comparison with our SiO_xN_y elastic modulus value. For pure materials like gold or silicon for example, the elastic moduli by bulk measurements are the same as for a surface nanoindentation measurement[11] and these materials are comparable to thin film material, but for materials like ceramic silicon nitride that is utilized as a tooling material, the bulk elastic modulus measurement averages in nonhomogeneities, and bulk modulus is quite different from that of thin films (Table 1). In comparison to elastic moduli of other CVD films (Table 1), the value of 51 for SiO_xN_y indicates that this material is softer. Interesting continued work in this area is variation of SiO_xN_y moduli with film thickness and annealing. Also, nanoindentation measurements of channel configurations to determine fracture dependence on shape is relevant.

Table 1

Material:		Elastic Modulus:	
Bulk:	Gold	74	CRC[12]
	Silicon	110 to 130	CRC[12]
	tungsten	340	CRC[12]
	SiO_2	73	Carlotti[13]
	Silicon nitride (ceramic)	280 to 320	Gogotsi[14]
Films:	PECVD TEOS	64±2	Carlotti[13]
	LPCVD TEOS	61±2	Carlotti[13]
	Thermal silicon oxide	66	Carlotti[13]
	SiO_2	70	Carlotti[13]
	CVD silicon nitride	E/(1-v)[15]: 370	Retajczyk[16]
	r.f. plasma silicon nitride	110	Retajczyk[16]

6. ADHESION OF SION FILM

Since this microduct fabrication is a low temperature process that utilizes only a few standard processing steps, it is an attractive addition to integrated circuit fabrication, and we tested SiO_xN_y film adhesion on several microelectronics materials. A 2 µm thick SiO_xN_y film was deposited on substrates or other films. Adhesion of the SiO_xN_y film to the underlying material was tested by pulling on a stub that was attached to the SiO_xN_y film, while the remainder of the sample was secured in a fixture. Failure occurred by either SiO_xN_y film delaminating from the substrate or by fracture of the substrate.

Adhesion results are shown in Table 2. Adhesion between SiO_xN_y films deposited on gold and GaAs samples results from weak Van der Waal's forces. Typically, oxides do not bond well to gold. However, PECVD silicon nitride films in the 4000Å thickness range are utilized for GaAs IC's. This suggests that with a thinner, less stressed SiO_xN_y film, or with a surface pretreatment to enhance bonding, the SiO_xN_y may bond adequately to GaAs substrates. The SiO_xN_y film, on the other hand, exhibited strong chemical bonding as expected to titanium, which has a high affinity for oxygen, and to the similar materials of silicon with native oxide, and thermal silicon dioxide. For these materials, the substrate fractured before the film delaminated.

Adhesion of SiO_xN_y to platinum gave mixed results, however the platinum film was only 500A thick and nonuniform island formation may be the cause for these results. Weak SiON film adhesion may occur to platinum and strong adhesion to titanium, could produce the mixed results reported in Table 2.

Table 2

SiON deposition on:	Pull test result:
Ti/Pt /Au	Film delaminated while cleaving the wafer
GaAs wafer	Film delaminated while cleaving the wafer
Ti/Pt	For 3 samples film delaminated before testing Other 3 samples: 1.00, 2.86, and 3.93 kg force
Ti	Excellent adhesion (substrate broke)
Silicon wafer (with native oxide)	Excellent adhesion (substrate broke)
Thermal dry SiO2 on Silicon	Excellent adhesion (substrate broke)

7. SUMMARY

We discuss a process that is compatible with microelectronic technologies, to fabricate a microfluidic network on a single wafer. This process avoids the more difficult integration of the two-wafer approach. Fabrication is comprised of a photolithography step that defines the entire fluidic network design either on the surface or in an etched channel, and a key room temperature SiON plasma film deposition that subsequently forms the channel walls after the photoresist is removed. From our test array of fabricated channels on silicon glass and quartz, we have identified a processing window that yields uniform repeatable channels (Fig.3 and 6) sized appropriately for fluidic microdevices that currently are of interest. Our processing results show that channel conformation is a result of a process design that can accommodate intrinsic film stress and radiative heat generation in the plasma.

We are in the process of further characterizations to determine mechanical properties of the SiON film and chemical compatibility to other microelectronics materials. From handling fabricated wafers, we find them surprisingly robust, and have begun mechanical characterization by measurement of the SiO_xN_y film elastic modulus using one of the latest nanoindentation techniques. Additional nanoindentation measurements of channel structures are relevant to film fracture dependence on channel shape and will assist us with further process development. To characterize film chemistry, we have performed pull tests to determine adhesion on the SiO_xN_y film to various materials commonly utilized in microelectronic fabrication. From results, the SiO_xN_y film that is deposited at room temperature is chemically similar to that of silicon oxides.

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