SANDIA REPORT

SAND95–2053 • UC–706
Unlimited Release
Printed August 1995

Characteristics and Development Report for the SA3871 Intent Controller Application Specific Integrated Circuit (ASIC)

Robert L. Simpson, Jr., Brent T. Meyer

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550
for the United States Department of Energy
under Contract DE-AC04-94AL85000

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

Available to DOE and DOE contractors from
Office of Scientific and Technical Information
PO Box 62
Oak Ridge, TN 37831

Prices available from (615) 576-8401, FTS 626-8401

Available to the public from
National Technical Information Service
US Department of Commerce
5285 Port Royal Rd
Springfield, VA 22161

NTIS price codes
Printed copy: A04
Microfiche copy: A01

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

SAND95-2053
Unlimited Release
Printed August 1995

Distribution
Category: UC-706

Characteristics and Development Report for the SA3871 Intent Controller Application Specific Integrated Circuit (ASIC)

Robert L. Simpson, Jr. and Brent T. Meyer
Digital ASICs Department
Sandia National Laboratories
Albuquerque, New Mexico 87185

Abstract

This report describes the design and development activities that were involved in the SA3871 Intent Controller ASIC. The SA3871 is a digital gate array component developed for the MC4396 Trajectory Sensing Signal Generator for use in the B61-3/4/10 system as well as a possible future B61-MAST system.

Contents

Figures

Characteristics and Development Report for the SA3871 Intent Controller Application Specific Integrated Circuit (ASIC)

1.0 Functional Description

1.1 Basic Function of Next Assembly

The SA3871 Intent Controller ASIC was designed for the MC4396 Trajectory Sensing Signal Generator (TSSG). The TSSG is an intent-enabled trajectory safety subsystem for the B61-3/4/10 weapon system that must receive an intent-unique signal (IUQS) from the aircraft before it will release the weapon. The reception of this unique signal establishes the human intent to arm the weapon system. The IUQS represents half the information needed by the TSSG to generate the unique signal required to drive the MC2935 or the dual stronglink assembly (DSA) in the B61-Multi-Application Surety Technology (MAST) system. The second half of the information is stored in the inclusion region of the TSSG.

Electronic access to the inclusion region is blocked by spin or retard rolamites. These rolamites allow access to the inclusion region only when a proper acceleration environment exists. The signal retrieved from the inclusion region is called the environmental unique signal (EUQS). The EUQS is then combined with a portion of the IUQS information to generate the trajectory unique signal (TUQS). The TUQS signal closes the trajectory stronglink thereby enabling the trajectory safety subsystem.

Figure 1 shows a single channel of the TSSG that interfaces with the aircraft monitor and control (AMAC) device. The TSSG is a dual-channel component to ensure weapon reliability, except for the single-channel aircraft interface.

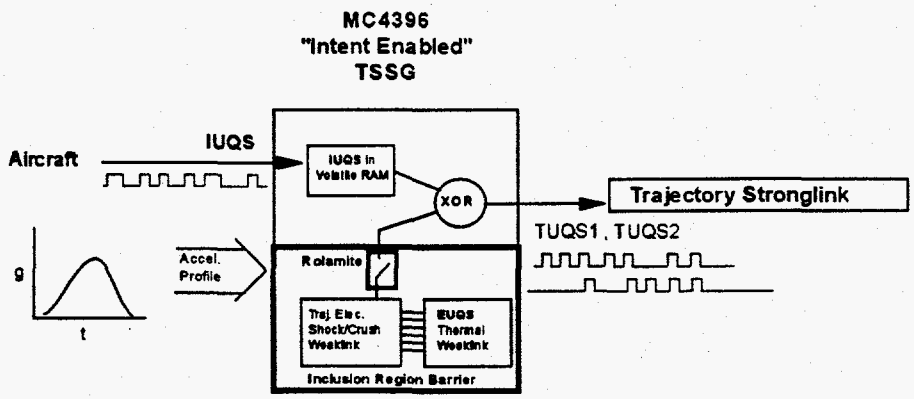


Figure 1. MC4396 Functional Block Diagram

1.2 SA3871 Circuit Description

The SA3871 was implemented in LSI Logic's 1.5 µm, two-layer metal LCA10000 CMOS technology. The design uses 31,391 gates, is placed in the LL10051C die, and is packaged into a 68-pin ceramic J-leaded chip carrier (LSI Logic package code CK45). This die was the largest available in the target package. Typical gate usage for the LL10051C die is < 25,000 gates (50% of the total gates), but since the layout for this ASIC was done in house by Department 2274, the usable gate count was extended well beyond the 50% mark. This prevented the design from being forced into a larger die and subsequently into a larger package size. A larger package would have presented significant constraints to the intent electronics board design. See Figure 2 for a block diagram of the SA3871 circuit.

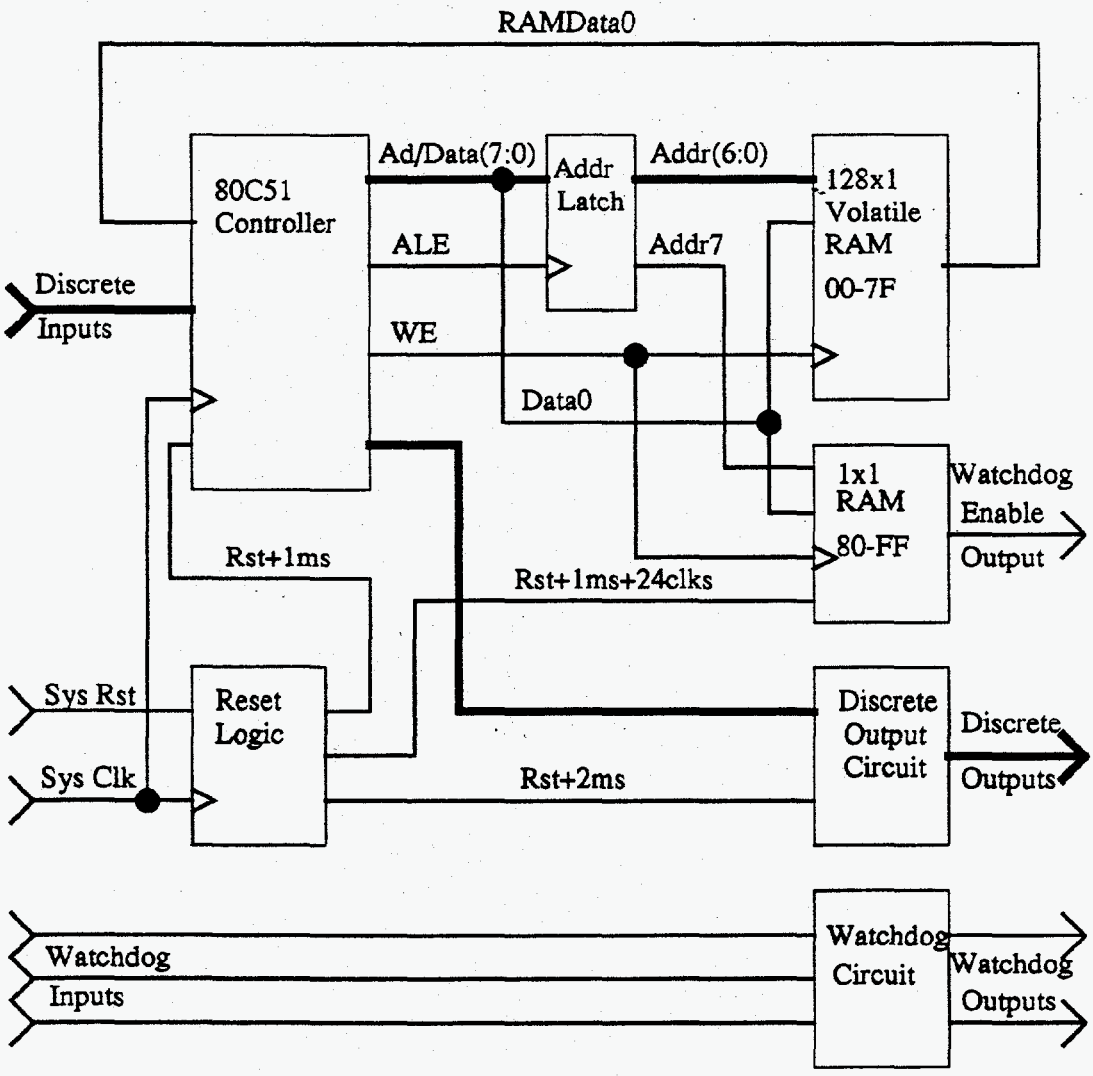


Figure 2. SA3871 Block Diagram

The 80C51 controller is LSI Logic's emulation of Intel's design. It includes a 4,096 x 8 ROM that contains the application program code. It also includes a 128 x 8 volatile RAM. Memory volatility is an integral part of this device and is discussed in Section 4.0. The reset logic holds the circuits in reset following the negation of system reset. The 80C51 is held in reset for an additional 1 ms to ensure that the oscillator is stable. The 1 x 1 RAM bit (a flip flop) is held in reset for 24 clocks after the controller's reset is negated in order to give the WE signal time to stabilize. The discrete outputs are held in the negated state for 2 ms to ensure that no erroneous data is output during reset and initialization of the microcontroller.

The 80C51 receives several "monitor" signals on the discrete inputs. These signals validate the external system condition. If the signals are correct, the program continues to execute. In addition, a powerdown interrupt input is received by the 80C51 to initiate a controlled powerdown sequence. This maintains the RAM contents, but the controller must be reset to exit from powerdown so the program state is lost.

The discrete outputs are used to control external circuitry. Several signals are used by the external monitor logic for enabling functions. Four signals are used to deliver stronglink drive information. Other signals retrieve the EUQS information, interact with the regulator for powerdown operation, and provide diagnostic information. Most of the critical output signals are "ANDed" with one of the reset logic outputs, so that they are held in the negated state until well after the 80C51 has stabilized and taken control of its output ports.

During operation, the IUQS is received one bit at a time on one of the discrete inputs. The controller moves each bit to the 128 x 1 Volatile RAM at external addresses 00-7F(hex). Bit 0 of the 80C51 address/data bus (Port 0) is used for the data signal during read and write operations. The EUQS is also received one bit at a time through one of the discrete inputs. It is combined with the stored IUQS and the resulting TUQS is transmitted on the discrete outputs.

The 1-bit watchdog flip flop is written by the controller at external addresses 80-FF (hex). Any address in this range will select the single flip flop for writing. The 80C51 will toggle the bit at a rate that is faster than the rate of the external watchdog timeout period. Toggling the bit will reset the watchdog timer. Should the external timer expire the watchdog inputs could cause the watchdog circuit to negate its outputs, effectively disabling the external circuitry.

Complete functional details are provided in SNL CD399258. Please refer to this document for further information.

2.0 Design Process

The design was created on a Mentor Graphics Corp. workstation using Version 7 software. Except for the reset counter, schematic capture was used to describe the logic. The reset counter was described in VHSIC Hardware Description Language (VHDL), synthesized using Synopsys Corp. software, and then a Mentor schematic was automatically generated from the synthesized design.

Considerable test logic was added to enable testing of the 128 x 1 RAM, the 4,096 x 8 ROM, the 80C51 microcontroller, and the reset counter. The counter was tested by using scannable flipflops to provide controllability and observability of each bit in the counter. The RAM, ROM, and 80C51 were tested by using all uncommitted pins and by adding internal multiplexers to provide controllability of all inputs and observability of all outputs. All remaining functions were tested by using the microcontroller to exercise the circuits. Appendix 1 contains a copy of the Mentor schematics. The test vectors that were developed for production testing are summarized below.

2.1 Test Vector Sets

Vector Set A: Writes all 1's to the 128 x 8 volatile RAM internal to the 80C51 megafunction and to the 128 x 1 volatile RAM external to the megafunction. Reads all locations back to verify the operation.

At this point in the test program the power supply is lowered to 2.0 V for 15 seconds and is then returned to previous levels.

Vector Set B: Reads the 128 x 8 RAM locations. The memory contents are expected to be all 1's as written by Vector Set A.

Vector Set C: Reads the 128 x 1 RAM locations. The memory contents are expected to be all 1's as written by Vector Set A.

At this point in the test program the power supply is lowered to 0.1 V for 15 seconds and is then returned to previous levels.

Vector Set D: Reads the 128 x 8 RAM locations. The memory contents are expected to be all 0's to validate the volatility of the RAM design.

Vector Set E: Reads the 128 x 1 RAM locations. The memory contents are expected to be all 0's to validate the volatility of the RAM design.

Vector Set F: Exercises the UART internal to the 80C51 megafunction. This test was explicitly included due to previous problems with LSI Logic's universal asynchronous receiver/transmitter (UART) module within the megafunction.

Vector Set G: Executes the 80C51 vector set supplied by LSI Logic.

Vector Set H: Executes the RAM test vector sets supplied by LSI Logic.

Vector Set I: Tests the reset counter by using scan techniques to check each stage for increment and hold operations without counting through all the possible states.

Vector Set M: Reads out the ROM contents from addresses 000-8FF (hex).

Vector Set N: Reads out the ROM contents from addresses 900-FFF (hex).

Vector Set P: Exercises the parametric NAND tree embedded in the I/O cells to determine input voltage thresholds. This test is required by LSI Logic.

Vector Set S: Tests the function of the watchdog circuitry.

Vector Set X: Used during Iddall testing, which measures the static current at the end of every test vector.

Vector Set Y: Used during Iddq testing, which measures the static current only once at the end of the vector set. This test is required by LSI Logic.

Vector Set Z: Used to test the tri-state function of the I/O cells. This test is required by LSI Logic.

2.2 The 80C51 Module Name

The 80C51 is a megafunction provided by LSI Logic. In order to exchange the standard internal 128 x 8 RAM for the volatile RAM design, the LSI-Logic-supplied netlist of the 80C51 (cfi0510) was edited manually to change the RAM module reference name (cmra220) to the volatile RAM module name (cmra221). This new 80C51 definition was called sfi0510 instead of cfi0510. The ASIC netlist was then manually edited to change the 80C51 module name to reference the edited megafunction module. The simulation models for both RAMs are identical.

2.3 Design Layout

The design layout was completed by Department 2274 in the C-MDE software tool set from LSI Logic. Following layout, actual wire delays were back annotated into the simulation database and all test vectors were re-executed. Each vector set was simulated with best-case timing models, and then again with worst-case models. The results of these simulations were compared cycle by cycle to ensure robust test vectors that were insensitive to process, temperature, and voltage variations. At this point the design layout and test vector files were sent to LSI Logic for validation and fabrication of the initial prototypes.

3.0 Test Results

Following receipt of the prototypes, testing of the SA3871 component by itself and in the next assembly began. The board level testing quickly uncovered a design flaw. Two of the outputs were crossed; the correct signals were being produced, but on the wrong pins. The problem was traced to a wiring mistake internal to the component. Because the paths had never been checked for functionality during simulation, the error went undetected until the product was inserted into the next assembly.

The design and layout files were updated and new prototypes were fabricated. This was accomplished in less than four weeks and included placing a new contract with LSI Logic. Board level testing of these devices uncovered a new problem. The ROM was fabricated with an outdated application code. Fortunately, the differences between the fabricated code and the desired code were cosmetic and the design did not need to be spun again. The root cause of the problem was that all versions of the application code were maintained in the same directory and when the design files were gathered together for layout and fabrication, an old version of the ROM code was selected accidentally.

Component testing on Sandia's HP82000 test hardware was initiated. The purpose of the tests was to determine the margin between the design requirements and the actual hardware. Results of the tests are summarized in Sections 3.1 through 3.3.8.

3.1 Static Leakage Current Requirement

Because of the powerdown retention mode requirement for the TSSG, the SA3871 has a static IDD leakage requirement of 30 μA at +100°C and 5.5 V. The initial static IDD 3σ data exceeded the CD requirement, but was taken at +125°C, 6.0 V. In an attempt to determine a realistic screen for production testing at LSI Logic (which would be done at +125°C, 5.5 V), the IDD data was plotted and values at +105°C were extrapolated. To provide a little more margin, +105°C was selected. The plots indicated that a screen of 75 μA at +125°C would provide a 2x margin for the 30 μA at +100°C requirement; thus, this limit was incorporated into the PS document.

Post-radiation testing was performed by Sandia on five SA3871 devices. The tests were performed at +25 °C, 5.0 V and +105 °C, 6.0 V. The total dose was 3 krad, 5 krad, 7 krad, 10 krad, 12 krad, and 15 krad. Only static IDD was recorded because this was the tightest requirement and because recording all parametric data would allow considerable time for annealing to occur. The devices were irradiated while bias was applied. The 3σ results indicated < 30 μA would be expected with a total dose of between 12 krad and 15 krad at +25 °C, 5.0 V and with a total dose of between 7 krad and 10 krad at +105 °C, 6.0 V.

Since a total dose of 15 krad was desired, additional testing was done on unbiased devices. These tests indicated that 10 krad of unbiased exposure would not significantly

increase IDD. Therefore a two stage test was incorporated into the product specification document. First, a biased 5 krad test would be performed with screening at +25 °C, 5.0 V for 30 μA. Then, an additional 10 krad unbiased (15 krad total dose) test would be performed under the same screening conditions.

3.2 Mechanical Shock Requirement

Mechanical shock testing was performed on four SA3871 devices. Even though the shock spectra required by the CD consisted of very low frequencies compared to the size of the SA3871 package, testing was still performed since the standard Group D qualification test uses 1,500 g/0.5 ms; this is radically different from that required of the SA3871. A single "enveloping" shock was applied in all six directions. Following the shock, all devices successfully passed electrical testing.

3.3 Characterization Data Summary

3.3.1 Maximum Operating Frequency. Figure 3 (a, b, c) shows the maximum operating frequency of the SA3871. These data can be somewhat misleading unless we remember that the frequency of operation depends on the particular vector set used to obtain the data. This vector set represents the operation of the SA3871 in the system, as well as we could simulate it. However, the maximum frequency of operation in the MC4396 TSSG may not be the same as shown here. The data were obtained by running the functional vector set at higher and higher clock frequency until a functional failure was detected. The maximum operating frequency is taken as the highest clock frequency attained before the functional failure was detected.

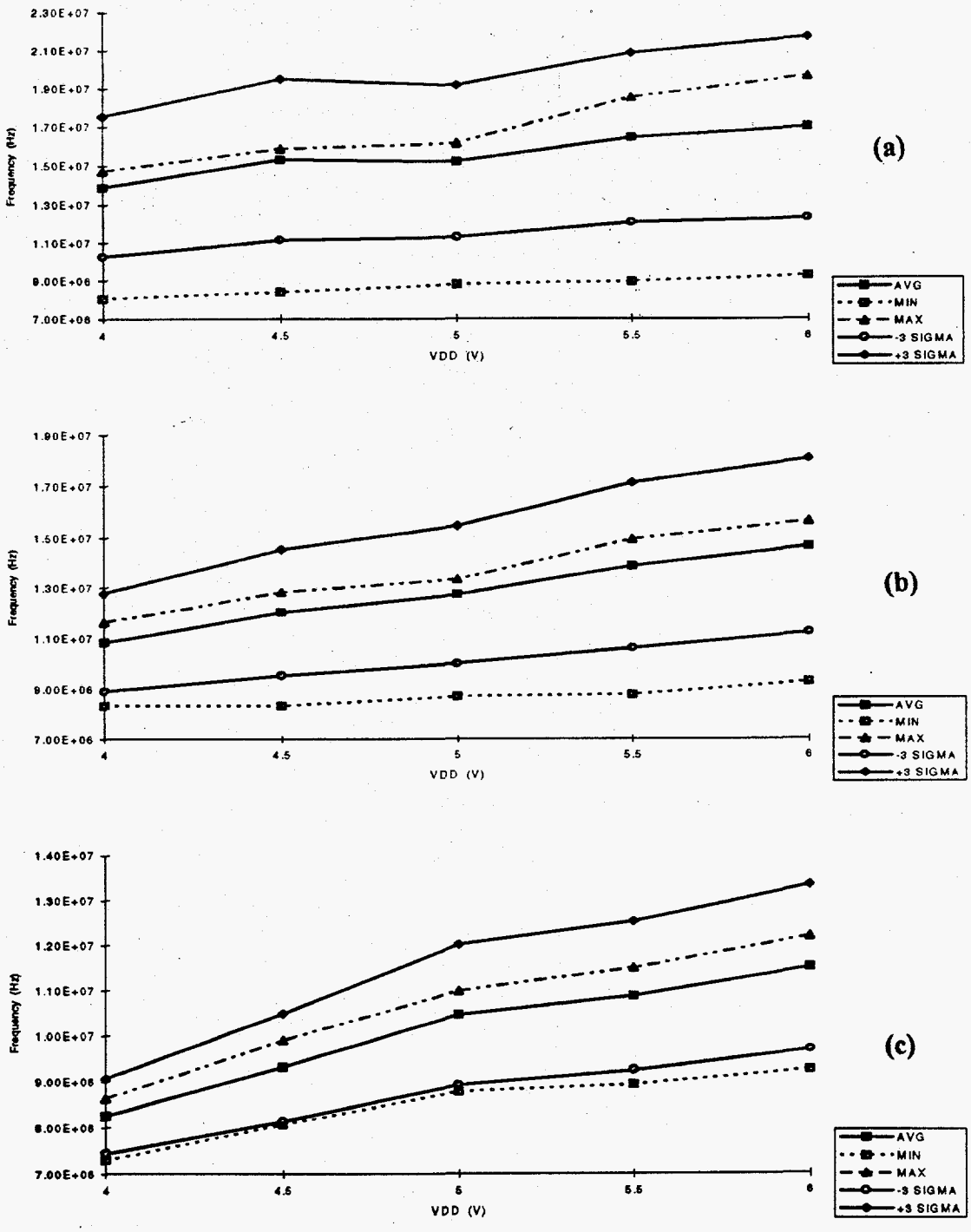


Figure 3. Maximum Operating Frequency of the SA3871
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

3.3.2 **Static IDD**. Static IDD (see Figure 4 a, b, c).is the current drawn by the SA3871 from the VDD power supply with the vector set stopped on a single vector.

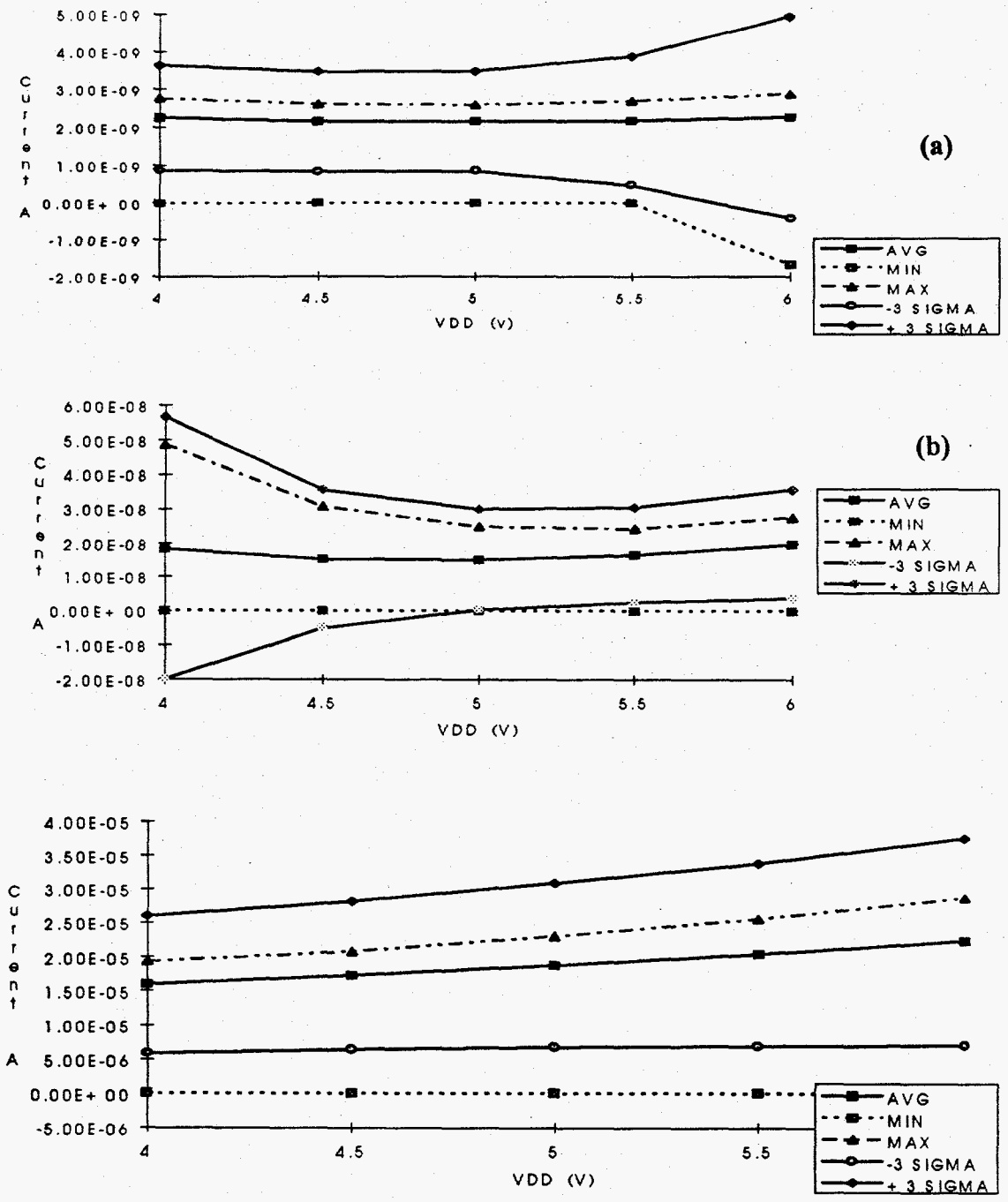


Figure 4. Static IDD (Current in Amps)
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

Figure 5 shows the static IDD for 5 parts and includes a data point at 105°C. Only the average current is shown.

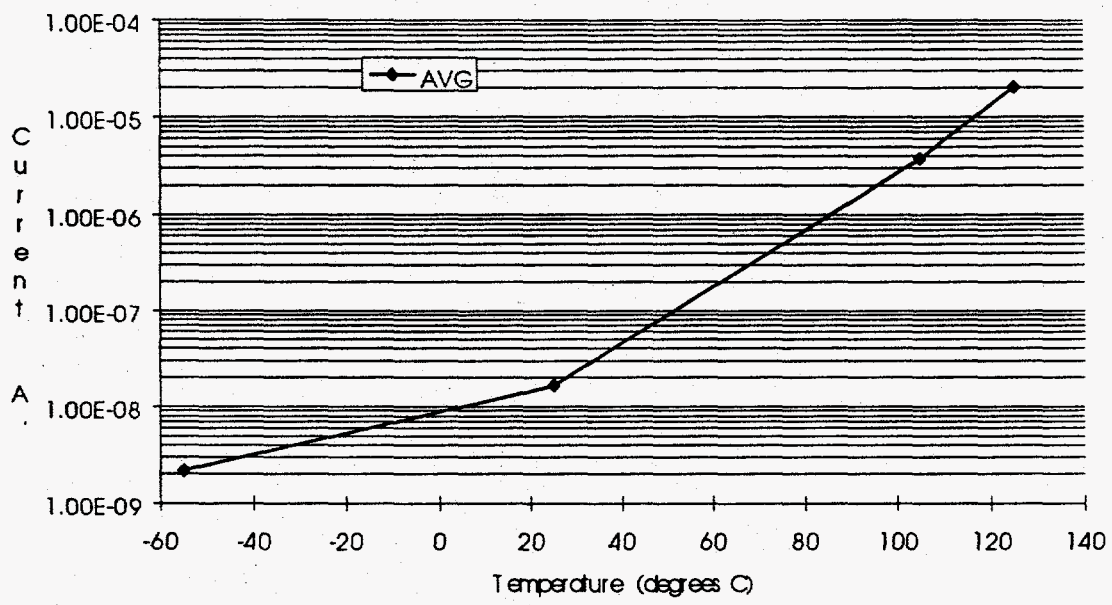


Figure 5. Average Static IDD for 5 Parts (Current in Amps)

3.3.3 Leakage Current of Input Pins. Figure 6 (a, b, c) shows the leakage current of input pins. The pin under test is held at VDD, while all other input pins are held at VSS (0 volts).

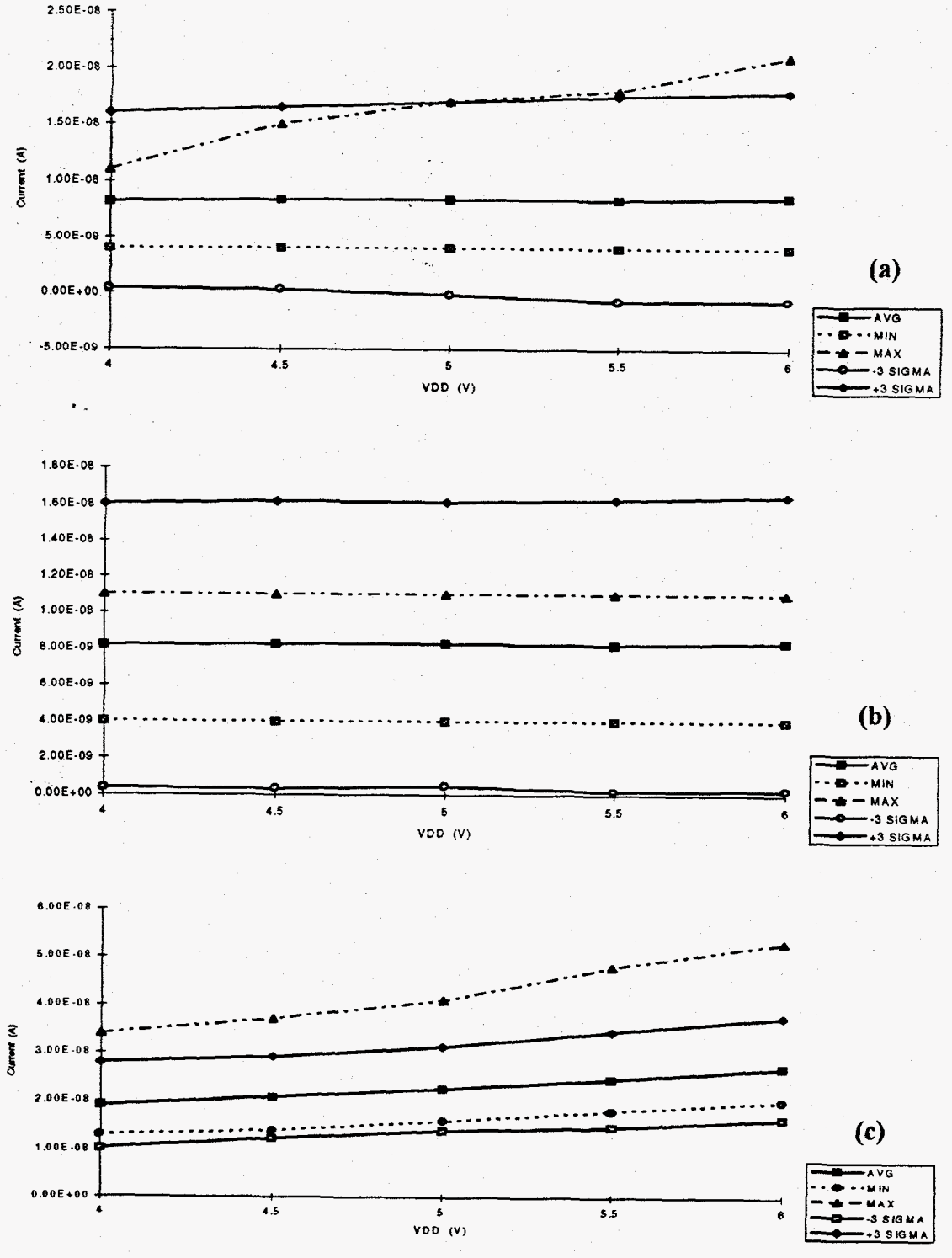


Figure 6. Input Leakage Current (IIH) With the Input Pin at VDD
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

Figure 7 (a, b, c) shows the leakage current at input pins with the pin under test held at VSS and all other input pins held at VDD.

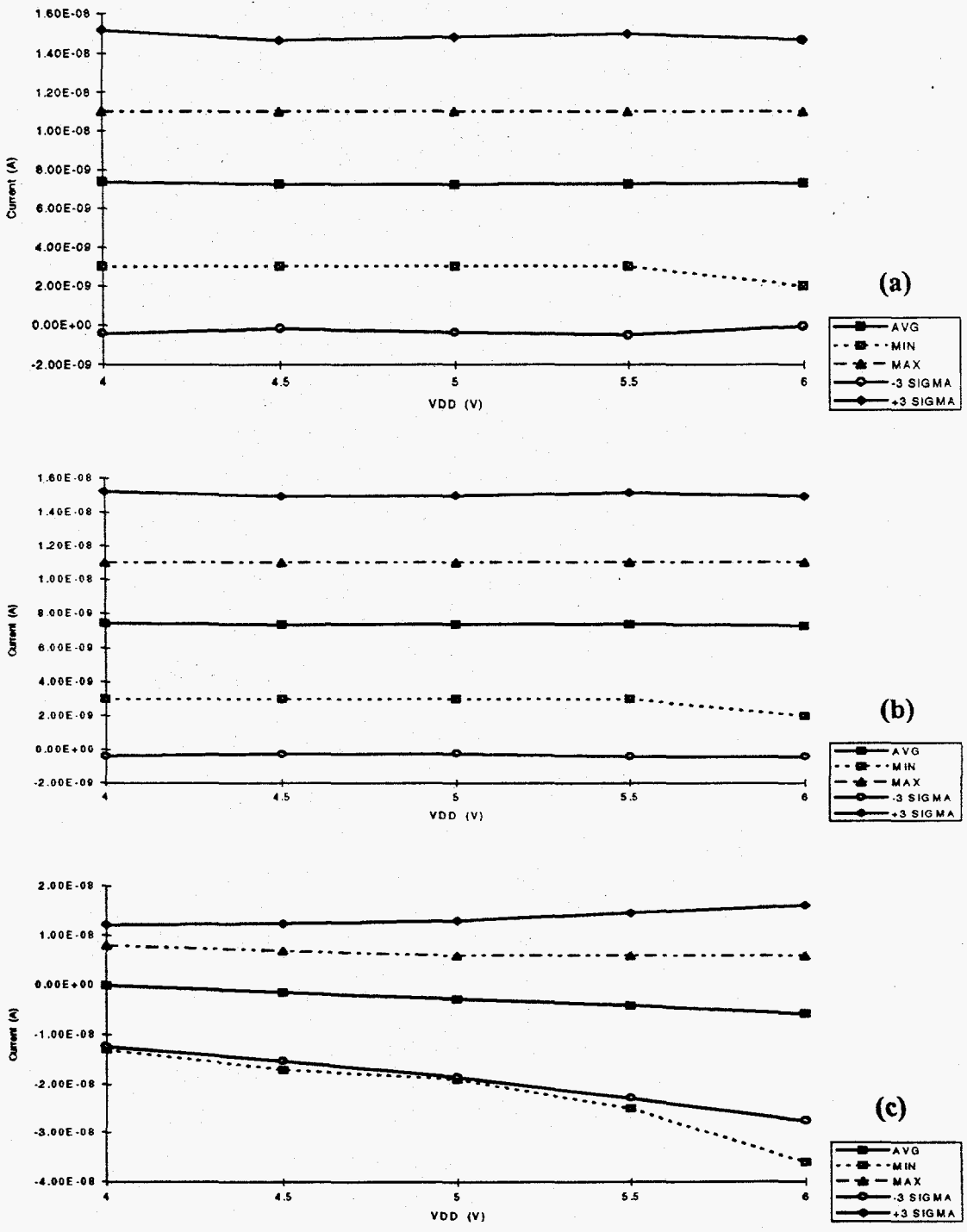


Figure 7. Input Leakage Current (IIL) With the Input Pin at VSS
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

3.3.4 Average Operating Current. Figure 8 (a, b, c) shows the average operating current drawn from the VDD power supply while the SA3871 is being operated at a clock frequency of 2 MHz. This is similar to the maximum operating frequency data that also depends on the particular operational vector set. Although the vector set simulated the MC4396 system operation to the greatest extent possible, it was not the actual operational vector set.

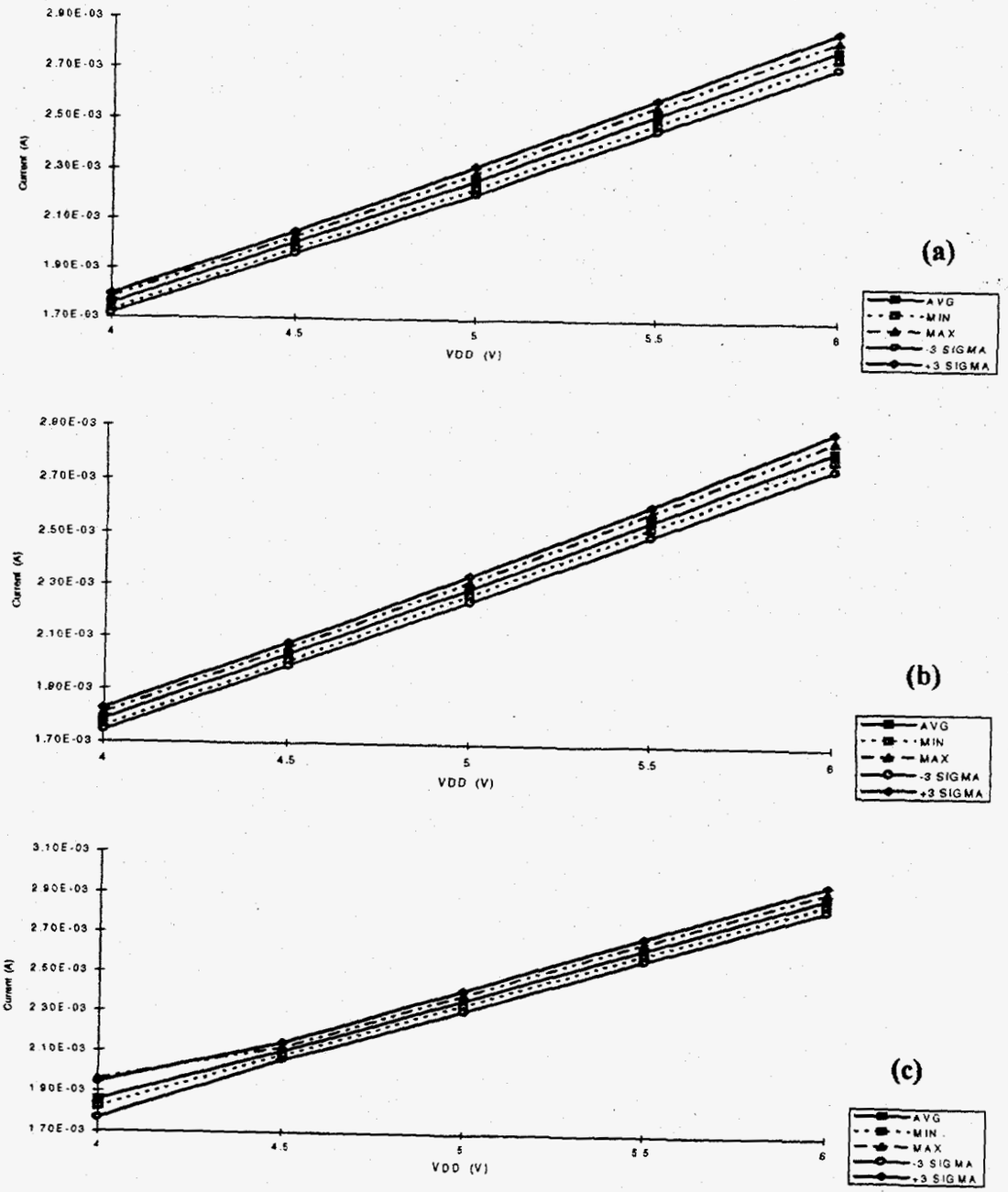


Figure 8. Average Operating Current at at 2 MHz Clock Frequency
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

Figure 9 (a, b, c) also shows the average operating current, but at a clock frequency of 8 MHz.

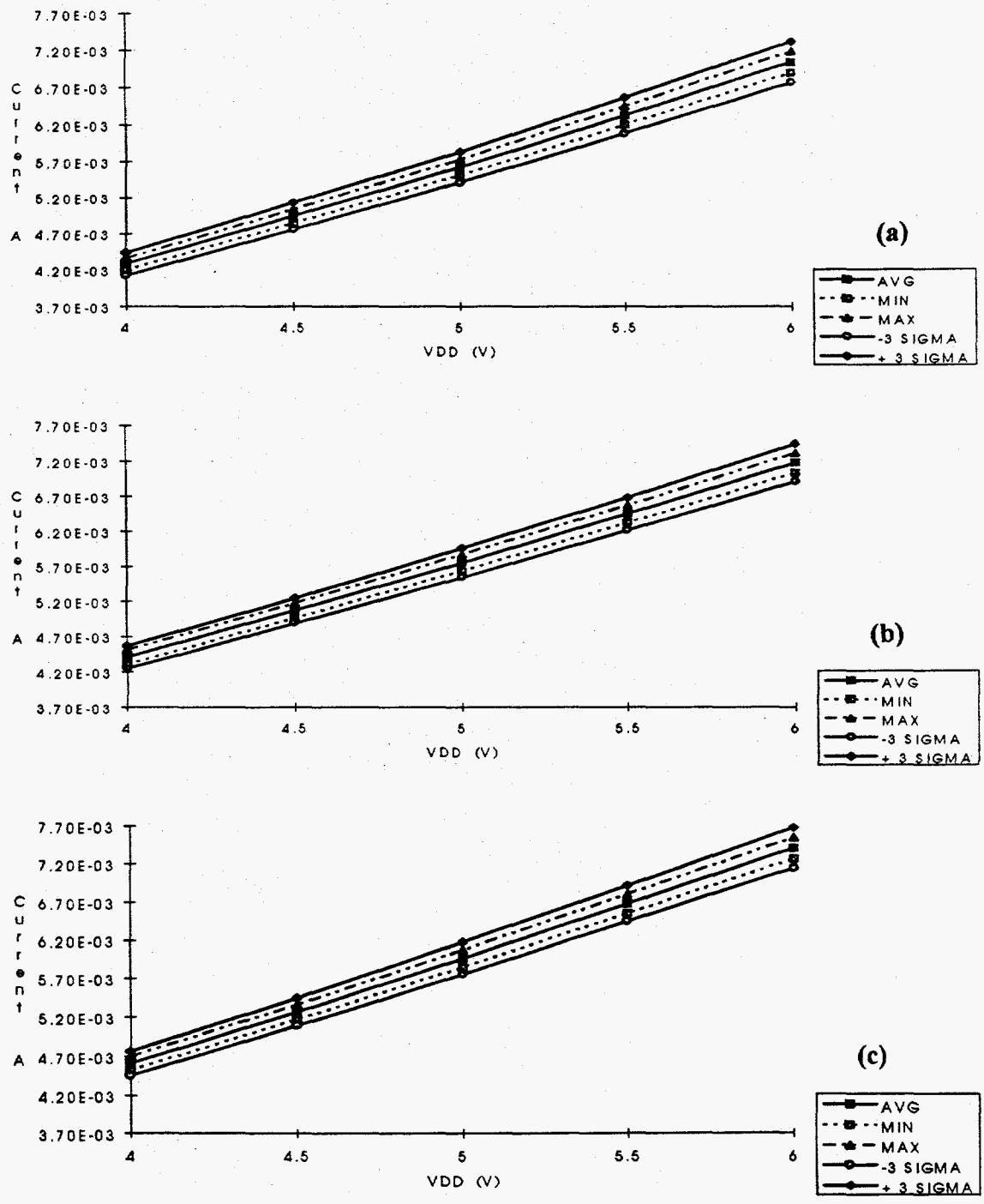


Figure 9. Average Operating Current at 8 MHz Clock Frequency
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

3.3.5 Tri-State Leakage Current. Figure 10 (a, b, c) shows the tri-state leakage current of the output pins that can be put into high impedance states. These pins include the combination I/O pins. The output drivers are set to the high impedance state and the leakage currents are measured in the same way the input leakage currents are measured on input pins. For IOZH, the pin under test is set at VDD.

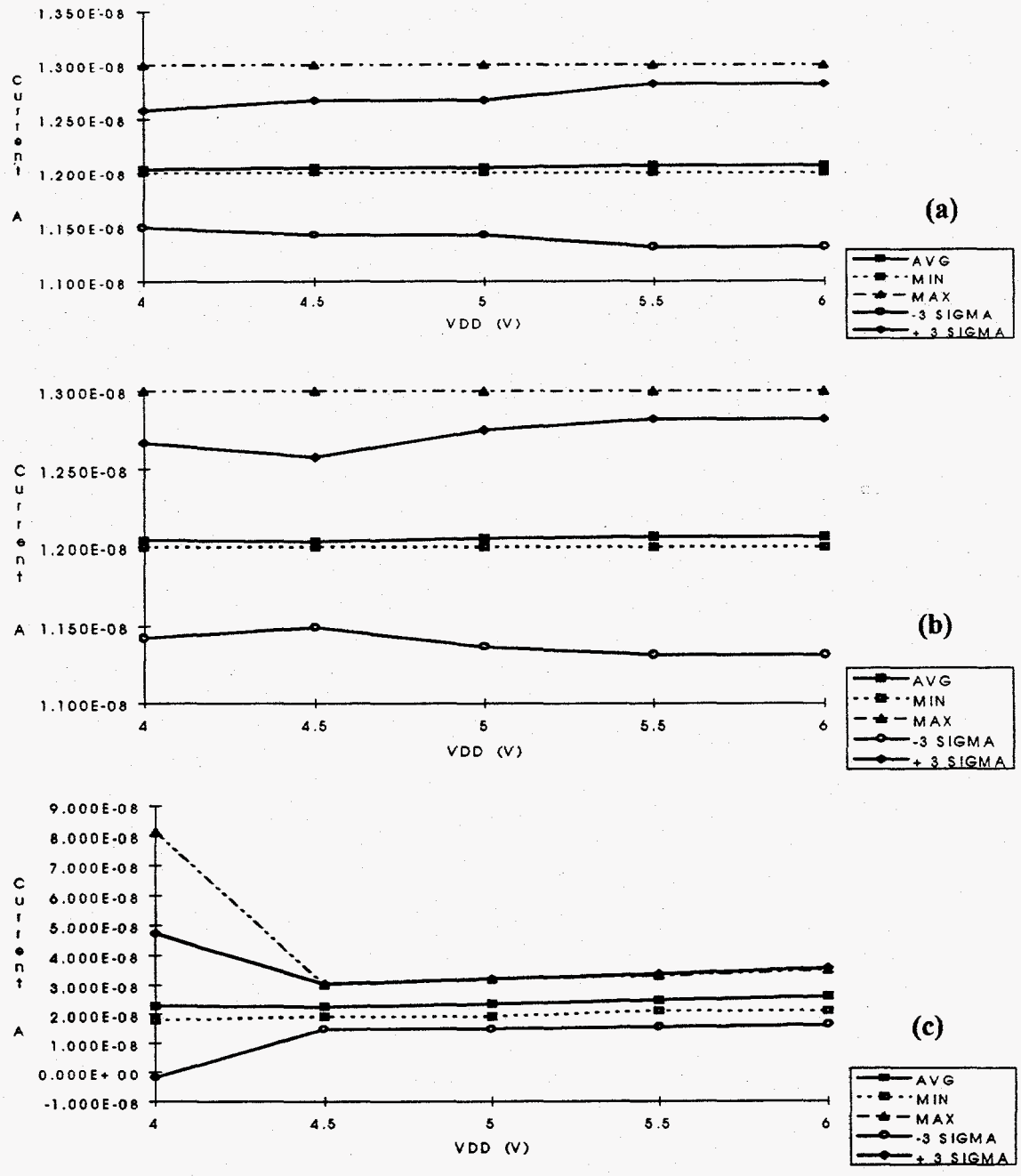


Figure 10. Tri-State Leakage Current With Output at VDD (IOZH)
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

Figure 11 (a, b, c) shows the Tri-State Leakage Current for the SA3871 high impedance pins with the pin under test set at VSS.

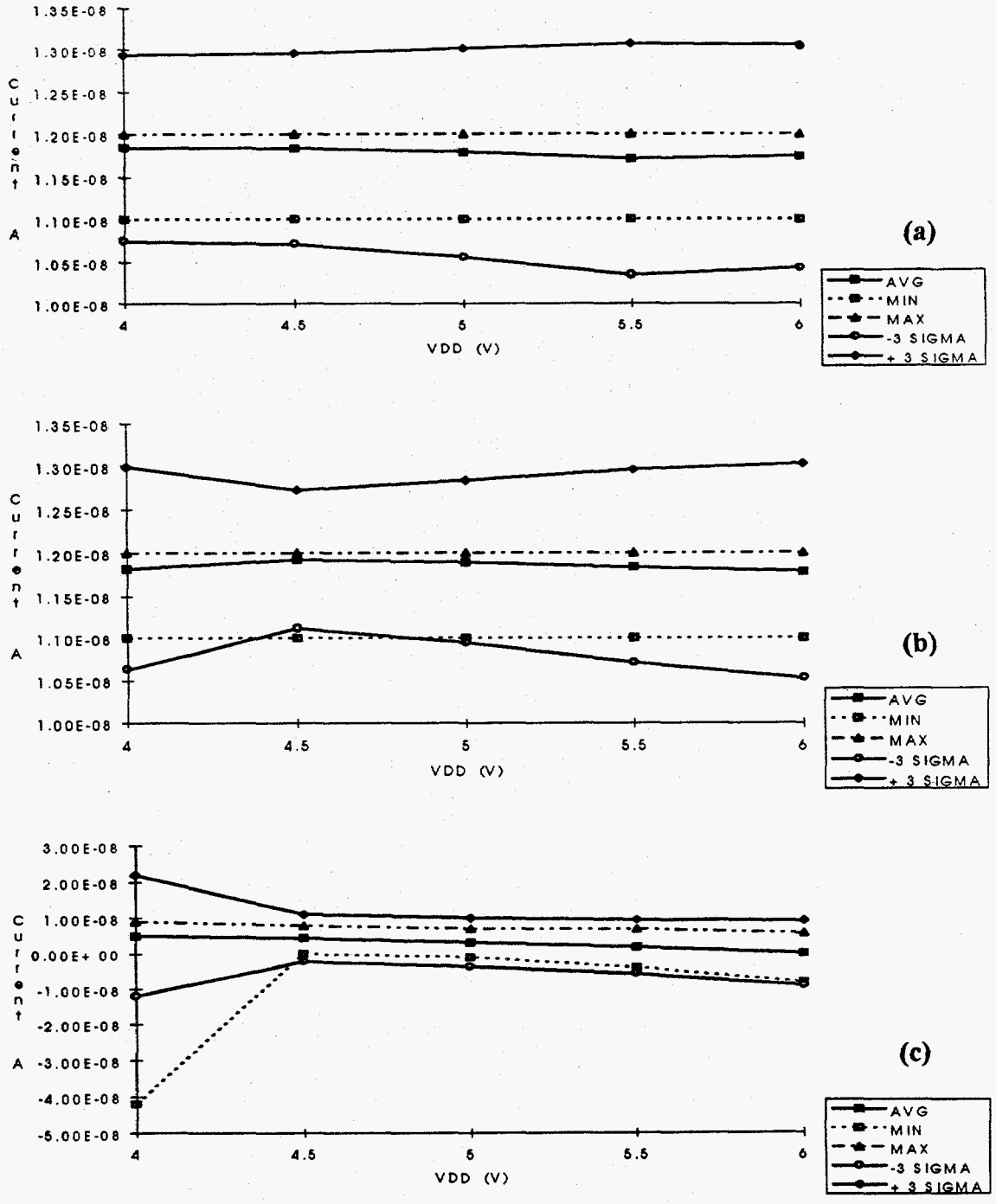


Figure 11: Tri-State Leakage Current at Output at VSS (IOZL)
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

3.3.6 Schmitt Trigger Input Cells. The input pins on the SA3871 device are all Schmitt trigger input cells (excluding the I/O pins). Figure 12 (a, b, c) shows the upper Schmitt trigger level for these input pins. To make the measurement, the voltage on the pin under test is set at a level that the device recognizes as a "0". The voltage is increased until the pin recognizes the voltage level as a "1". This value is recorded as VIH.

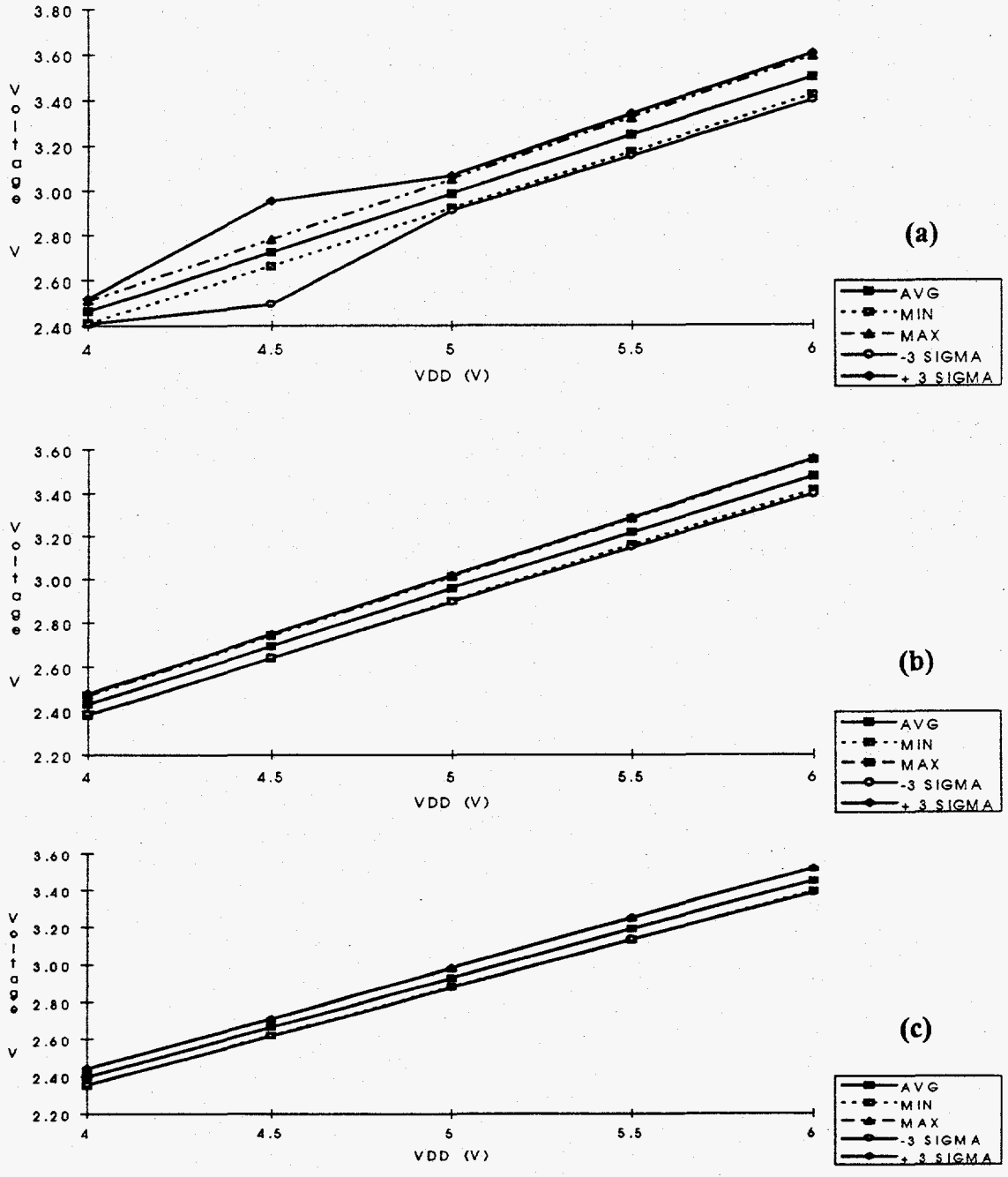


Figure 12: VIH (Upper Schmitt Trigger Level)
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

Figure 13 (a, b, c) shows the VIL for all the input pins (excluding the I/O pins) for the SA3871 device. VIL is the lower trigger level for the Schmitt trigger input cells. The data are obtained by setting voltage on the input under test at a voltage recognized as a "1". This pin voltage is decreased until the pin recognizes the level as a "0". This value is VIL.

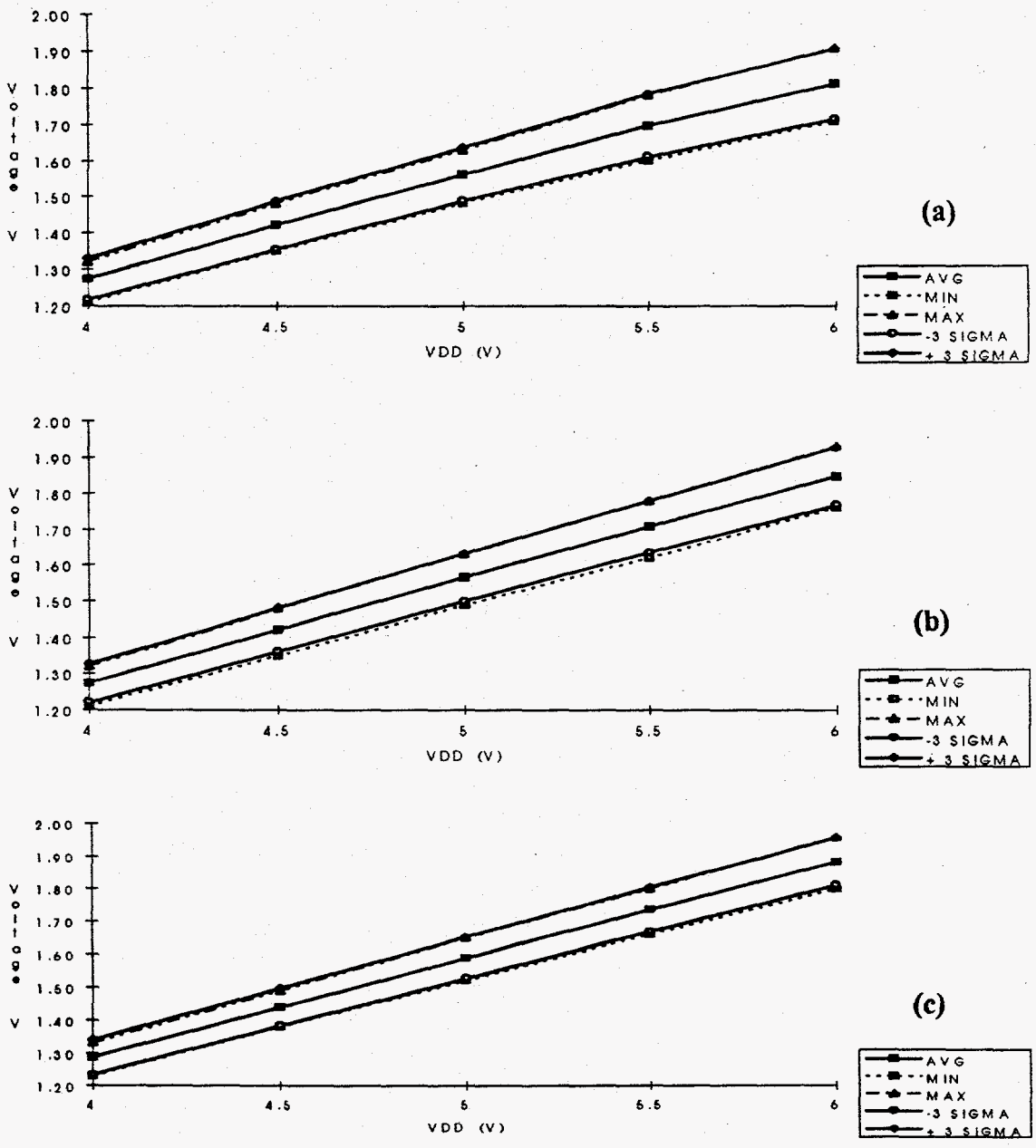


Figure 13. VIL (Lower Schmitt Trigger Level)
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

. **3.3.7 Output Driver Pins**. Figures 14 (a, b, c) shows VOH, the output voltage for output driver pins when the driver is set to a "1". The output drivers were sourcing 0.8 mA during the measurement.

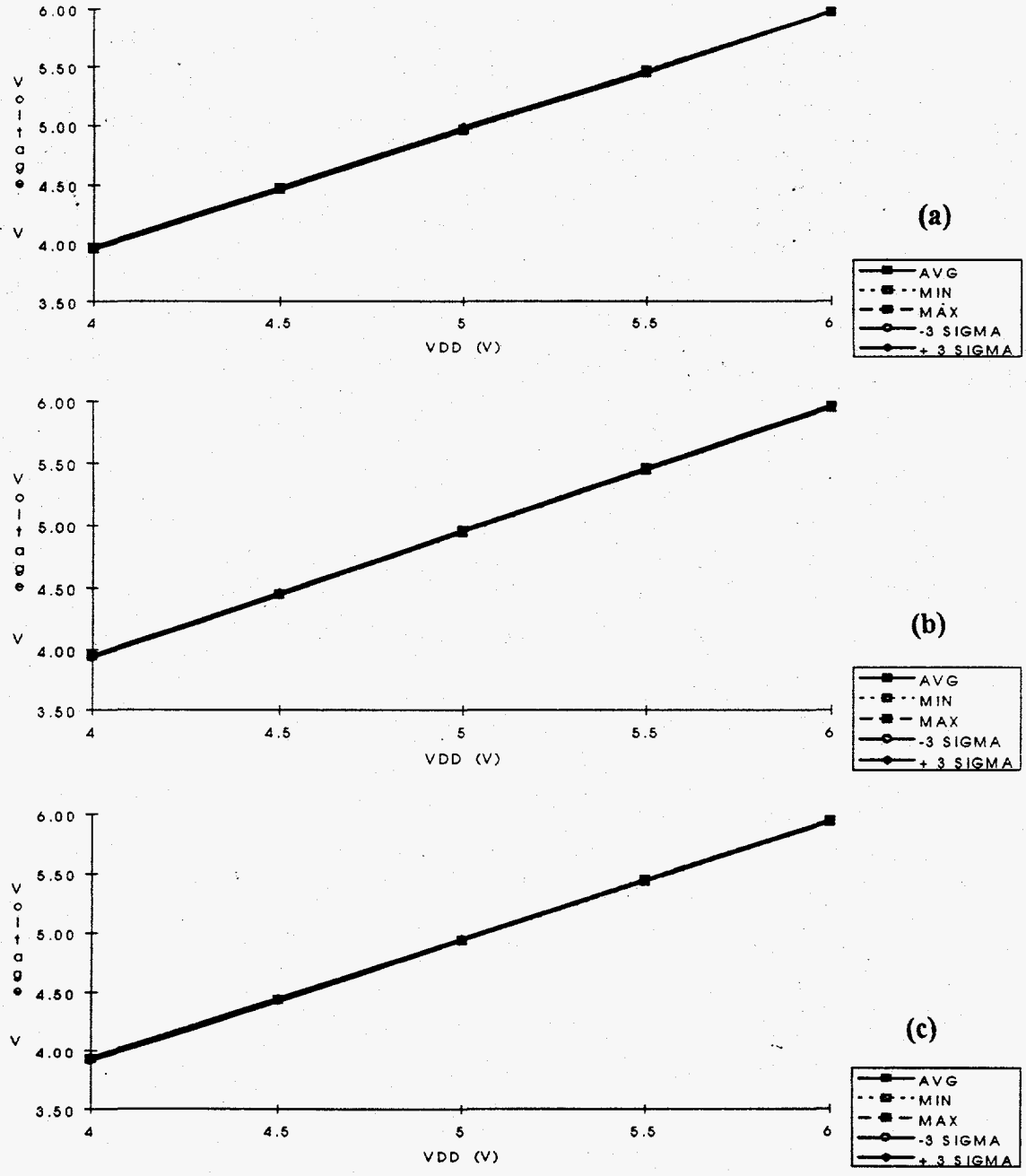


Figure 14. VOH (Voltage at Output Pin Driving "I")
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

Figure 15 (a, b, c) shows the voltage level at the output pins when driving a "0". The output drivers were sinking 3.2 mA during the measurement.

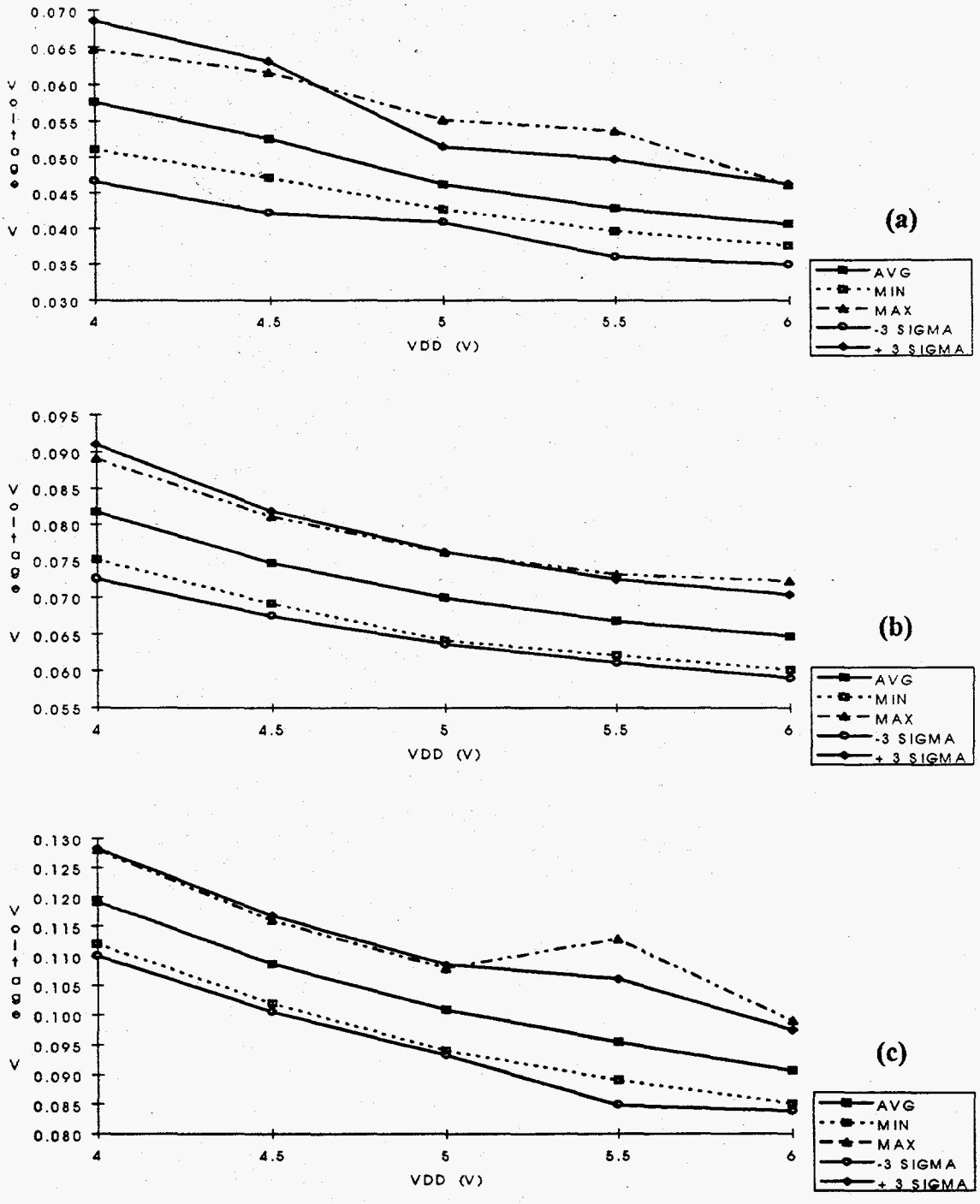


Figure 15. VOL (Voltage at Output Pin Driving "0")
(a) @ -55°C
(b) @ +25°C
(c) @ +125°C

3.3.8 Radiation Exposure. Figures 16 and 17 show the IDD drawn from the VDD power supply as a function of the total dose radiation exposure.

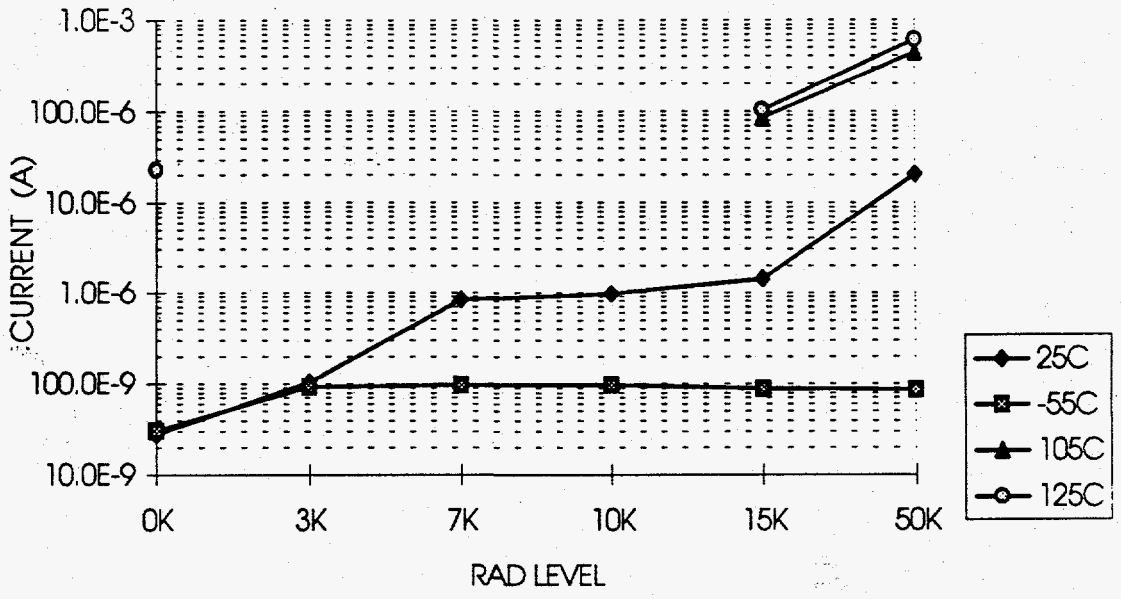


Figure 16. Static IDD Vs. Total Gamma Dose Level (Current in Amps) Device Serial Number 14

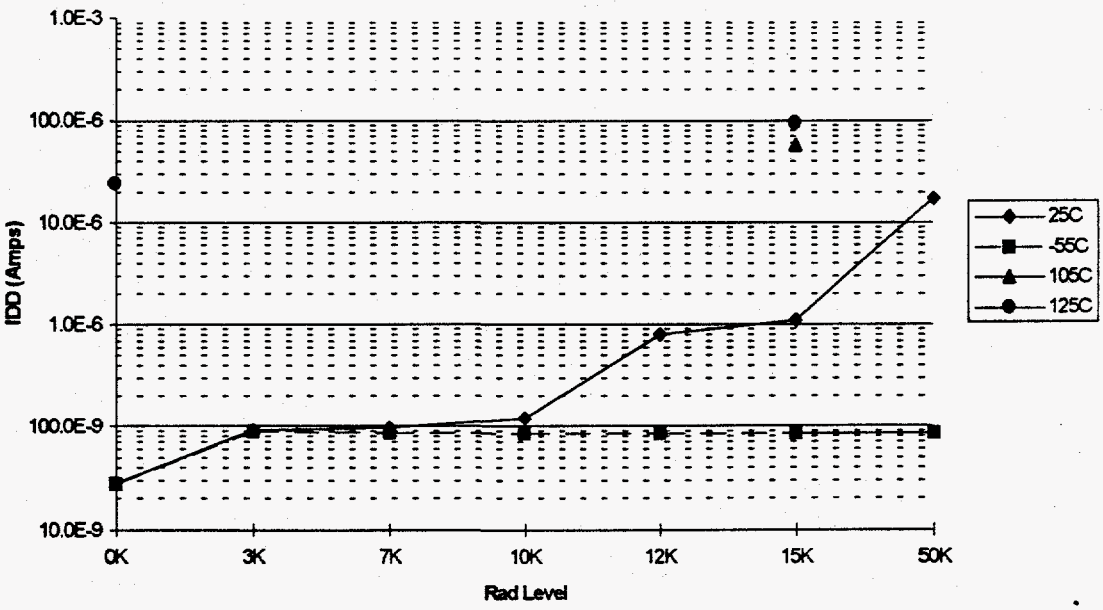


Figure 17. Static IDD Vs. Total Gamma Dose Level (Current in Amps) Device Serial Number 15

4.0 CMOS Static RAM Volatility

4.1 Volatile Memory Description

CMOS Static RAM (SRAM) devices are used in many different types of systems for temporarily storing data. They are called "static" because as long as the power source is supplying current, the memory contents are maintained. However, when the power source is removed, the contents are lost. The term "volatile" refers to this characteristic of a memory.

In most applications, volatility is a negative aspect of the memory. Following brief power failures or glitches, the contents of the memory are unreliable. However, in applications where the data being stored is critical to safety or security, volatility becomes a requirement. In these systems, the memory must return to a safe or secure state whenever power is removed.

During the development of previous TSSG subsystems, it was discovered that the commercial SRAM being used was almost nonvolatile. During testing at cold temperatures (-55°C), the contents of the memory was maintained for up to 24 hours after power was removed. At this point, an investigation into what was really affecting the volatility and what could be done to influence it was begun.

4.2 CMOS SRAM Operation

The standard six transistor (6T) CMOS SRAM memory cell is shown below in Figure 18. The basic structure is that of two cross-coupled inverters. The bit node serves as the output of Inverter 1 and the input to Inverter 2. The bit not node completes the feedback loop as the output of Inverter 2 and the input of Inverter 1. The access transistors allow data to be read or written.

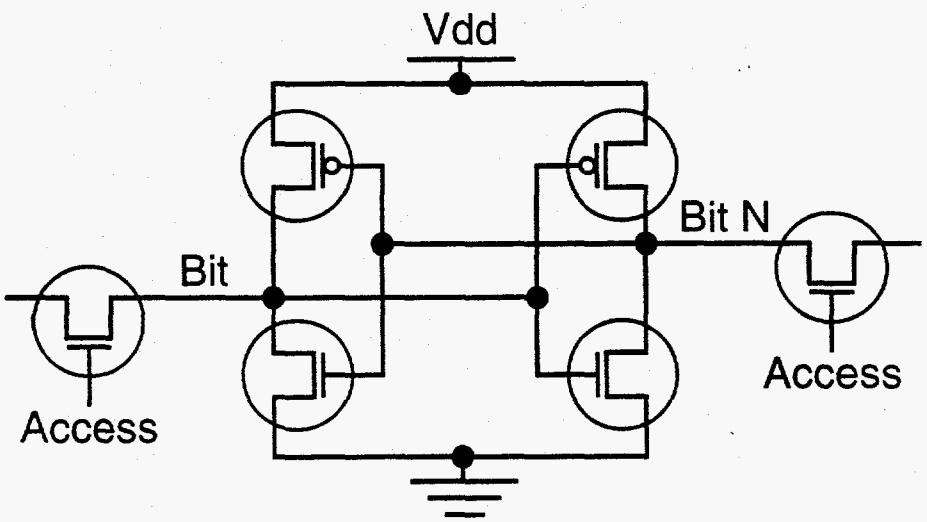


Figure 18. CMOS Static RAM Cell

Data in the cell is essentially maintained by the capacitance of the gate nodes. These structures are charged and discharged as the memory is written. As long as the power source is supplying current, the leakage from the nodes will be replaced by the power source and the memory will be static. When the power is removed, the leakage will drain the charge and therefore will drain the data.

In the ideal case, when power is reapplied to the cell, the two inverters will be perfectly balanced and the ultimate state of the cell will be random. This is analogous to placing a small ball on top of a larger ball. If they are balanced, the direction in which the small ball will ultimately fall is not deterministic. However, any disturbance or imbalance in the system will provide a bias to the outcome and the result will not be random.

4.3 Memory Volatility Principles

If there is still some residual charge in the cell when power is reapplied, this gives the cell a preference to power up in the previous state. The charge "leakage" rate when power is removed (subthreshold) is primarily a function of the reverse biased p-n junction recombination rate, which will determine the carrier lifetime. The slower the recombination rate, the longer the carrier lifetime, and the longer the cell maintains the charge. Numerous experiments validate that the recombination rate is the primary driver of CMOS memory volatility.

The equation that governs carrier lifetime is summarized as:

$$\tau \sim e^{E/T} .$$

The equation is a gross simplification, but effectively captures the dominant parameters. The numerator of the exponent is an energy term, related to the energy gap. The denominator is a temperature term. So as temperature decreases, carrier lifetime increases exponentially.

To positively affect, i.e. decrease, carrier lifetime, the energy term must be decreased. This can be accomplished by increasing the doping levels of the semiconductors, by introducing impurities into the material (such as gold), or by neutron irradiation. These methods provide additional recombination centers that reduce the carrier lifetime. Notice that a dirty fabrication process that introduces impurities into the material will create "leaky" transistors and will be quite volatile. On the other hand, a very clean process will produce very "tight" devices. They will be almost nonvolatile, as was the case for the TSSG subsystem that spurred this activity.

Unfortunately, the methods for decreasing the energy term are impractical. When procuring commercial silicon, the doping and impurities are not within our control. Exposing every device to neutrons would be time consuming and expensive, not to mention that the neutron effect can be annealed out of the silicon. Other methods of influencing the volatility must be found. At this time, two methods are being pursued.

4.3.1 First Method. The first method attempts to find a mechanism other than recombination for removing a charge. For example, in a 4T memory cell where the p-FETs are replaced by resistive loads (essentially an NMOS process), the volatility is controlled by the resistors. Experiments show that 4T cells have a much better volatility profile with less dependence on temperature. The main effect becomes thermionic emission instead of recombination. Since 4T cells consume considerable static power and are susceptible to single-event upset, a CMOS cell is still desirable. In CMOS technology, either polysilicon resistors or depletion-mode FETs could be used to "bleed" the charge off the nodes during powerdown times. However, because most CMOS processes do not implement these devices, this method requires access to a full custom-design process.

4.3.2 Second Method. The second method attempts to introduce an imbalance to the memory cell that overcomes the residual charge during powerup. The imbalance must not be so large that the cell becomes unstable in normal operation. But it must be large enough to overcome the charge at all temperature and process extremes. This method does not address the charge storage issue, it merely attempts to compensate for it. Of course, silicon foundries do not characterize their carrier lifetimes across all temperature and process variations, nor do they worry about subthreshold characterization. This makes it impossible to design the imbalance analytically; thus, an empirical approach must be used.

4.4 Implementation of an Unbalanced CMOS SRAM Cell

Since the TSSG subsystem was being developed, a solution had to be developed quickly. A custom design would take much longer than an unbalanced "standard" design. In addition, to preserve next assembly volumes, the solution needed to be integrated with the microcontroller. LSI Logic was the vendor providing the silicon and their process was for gate arrays and not for custom devices. This led us to provide an unbalanced memory cell that would greatly enhance the volatility of the data. The desired performance was for the cell to retain the data when power was dropped to 3.0 V, but to come up all zeroes when the power dropped to 2.0 V for 1 second. A contract was placed with LSI Logic to develop such a memory, which could be included in the SA3871 device. Their design is shown below in Figure 19.

The concept of this cell is that parallel transistors effectively reduce the net threshold voltage while series transistors effectively increase the net threshold. When power is applied, the 2 parallel transistors in each inverter will turn on before the three series transistors, so the cell will have a strong preference to come up with a '0' on the bit node and a '1' on the bit not node.

After the cell was fabricated, extensive testing was performed on the ten prototype devices. Results show that the cell was indeed volatile, but that the performance was much less than desired. Volatility was consistently achieved at -55°C when the power was dropped to 0.1 V for 10 seconds. While this was a tremendous improvement from the

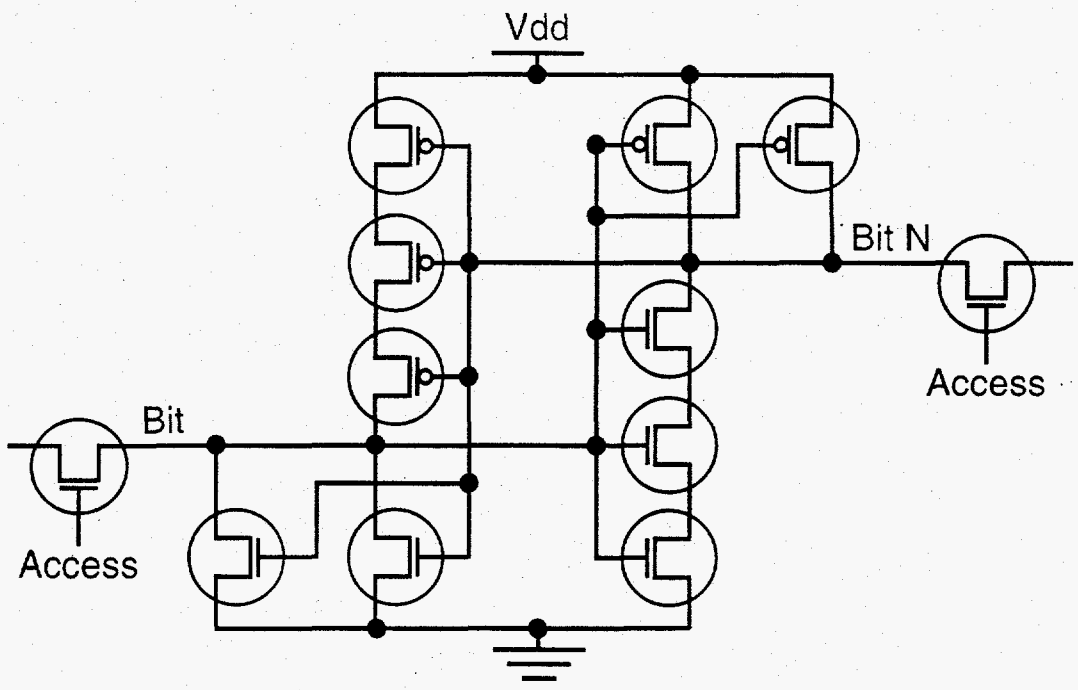


Figure 19. LSI Logic Volatile RAM Design

original devices (24 hours), it was far short of the design intent. Since time and budget were short, this design was accepted and put into production. A few minor changes to the read/write buffering external to the cell were made, but the basic cell as described above did not change.

For the production devices, tests were put in place at the vendor to screen devices for volatility. The most important test was at -55°C with a power cycle down to 0.1 V for 30 seconds. The time parameter accounted for process variations, even though the effect of the variations on volatility was unknown. When the test was run, all devices failed. It was determined that on the vendor's test equipment, a power cycle of ~5 minutes was required. The reason for this was never discovered, but it probably relates to parasitic current sources that provide additional charge to the nodes while the device is unpowered. This results in an extra residual charge for the imbalance to overcome and in less volatility than that measured on the prototype devices. Since a 5-minute test was unacceptable to the vendor, this test was removed. All testing of memory volatility at -55°C is at the subsystem level.

The test at the MC4396 TSSG level involved removing power and waiting for 3 minutes while at -55°C. The TSSG has considerable capacitance, and so a much longer time must elapse for the voltage to decay down to 0.1 V. The first development units were volatile in < 2 minutes, so the 3-minute parameter was selected to provide a testing margin. Once again, the margin was selected without extensive data to support the decision.

All but one development MC4396 passed the 3-minute test. The device that failed was removed and tested individually. The device was fully functional, but did have a reduced volatility characteristic. The device was volatile in 30 seconds if the temperature was increased by 2 or 3 degrees, or if the powerdown voltage was reduced by 35 or 40 mV.

4.5 Volatile Memory Aging Study

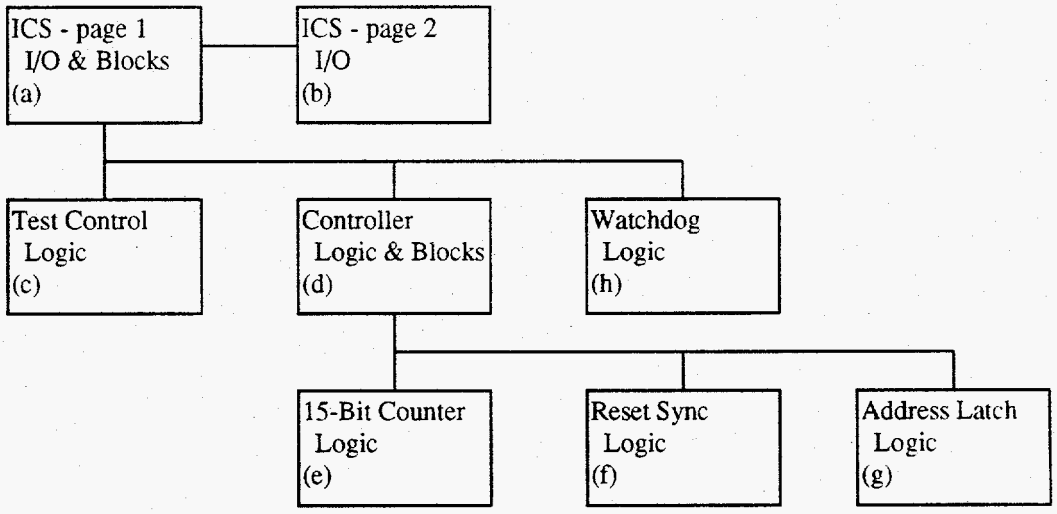
Since memory volatility was critical to the nuclear safety theme of the system and because this was the first attempt at controlling volatility, a detailed study of long-term aging effects was initiated. Duane J. Bowman (Department 2276) is currently performing the study and will issue a report once the study is completed. His preliminary report is included as Appendix 2.

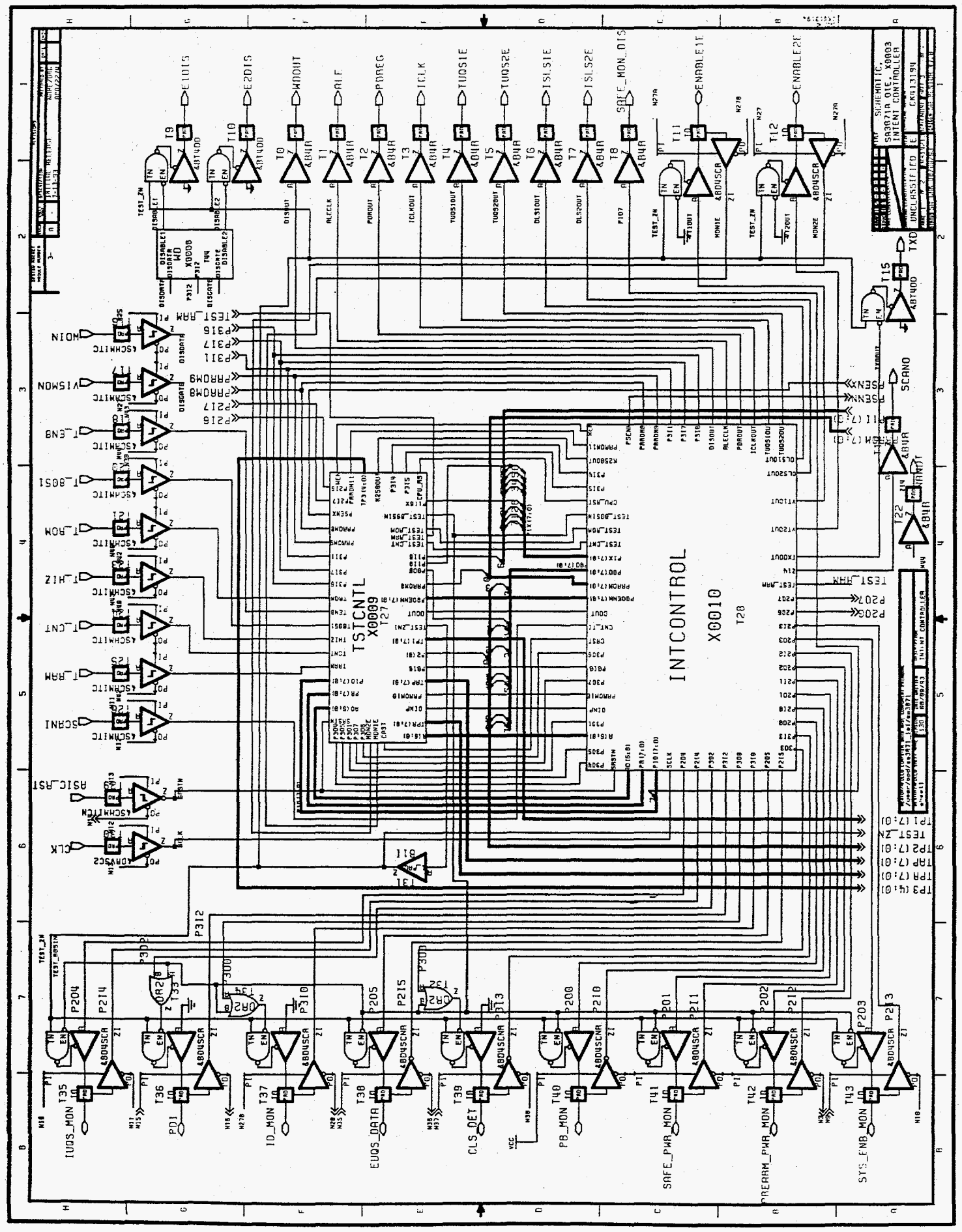
5.0 Summary and Conclusions

The SA3871 provided two significant challenges. Implementing a volatile memory and consuming less than 30 μA of static current in all environments. Both challenges caused considerable technical and programmatic problems. In the end, the volatile memory was accepted as better (but not ideal), and the static current was satisfied. In both cases, the fundamental problem was a lack of characterization data that would provide a high level of confidence that the requirements could be met. The ultimate test limits placed on the product to screen for both these requirements were the result of numerous revisions as the margin was cut each time the devices failed a test. At this point, the limits seem to be working. However, both parameters are very sensitive to process variations, so a future lot may fail the tests again.

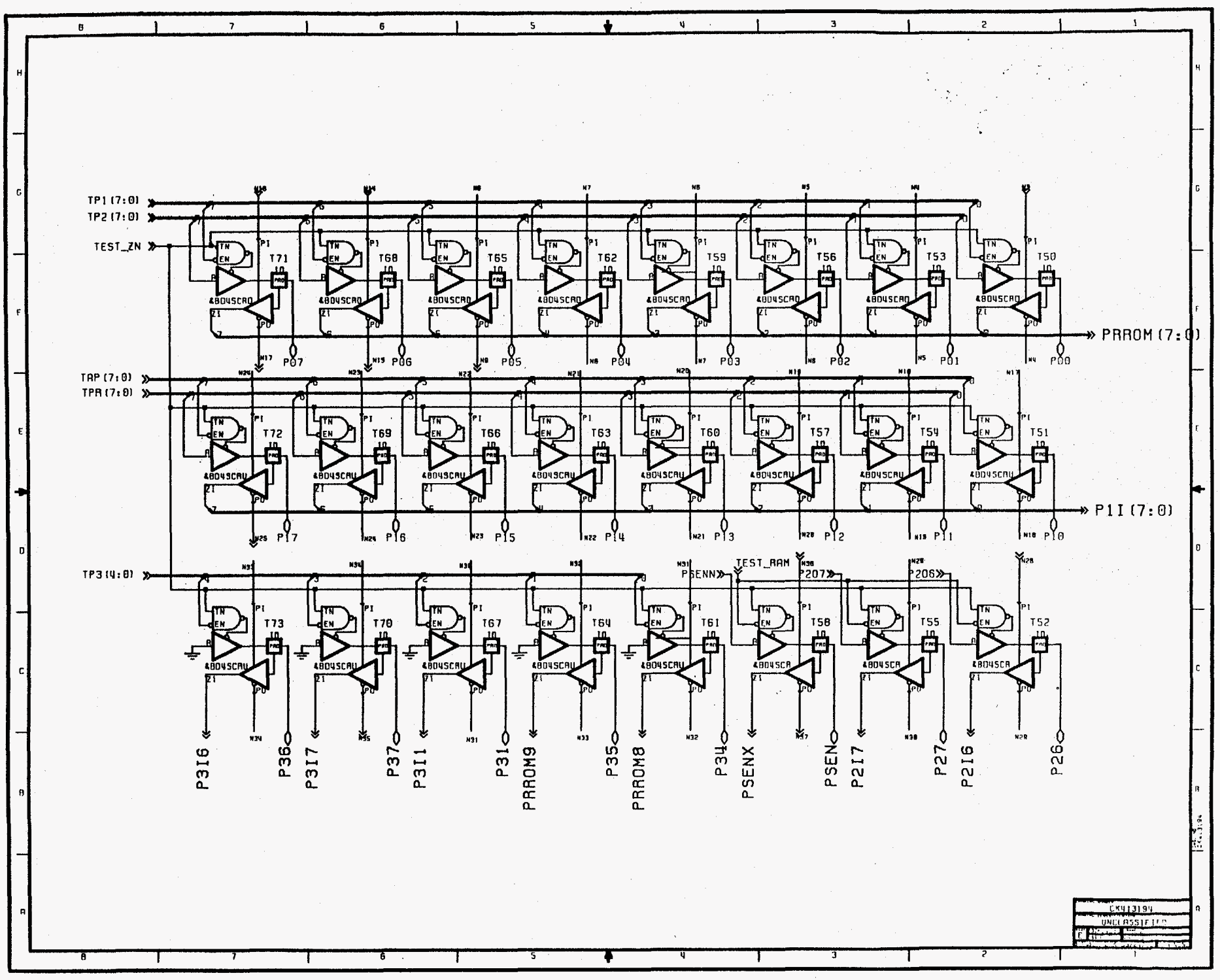
A business decision was made by LSI Logic to no longer support the LCA10000 process. Rather than risk opening up the design to new process variations from a new foundry, a life of program buy is being executed to support the remaining production requirements of the MC4396.

Appendix 1: SA3871 Intent Controller Schematic

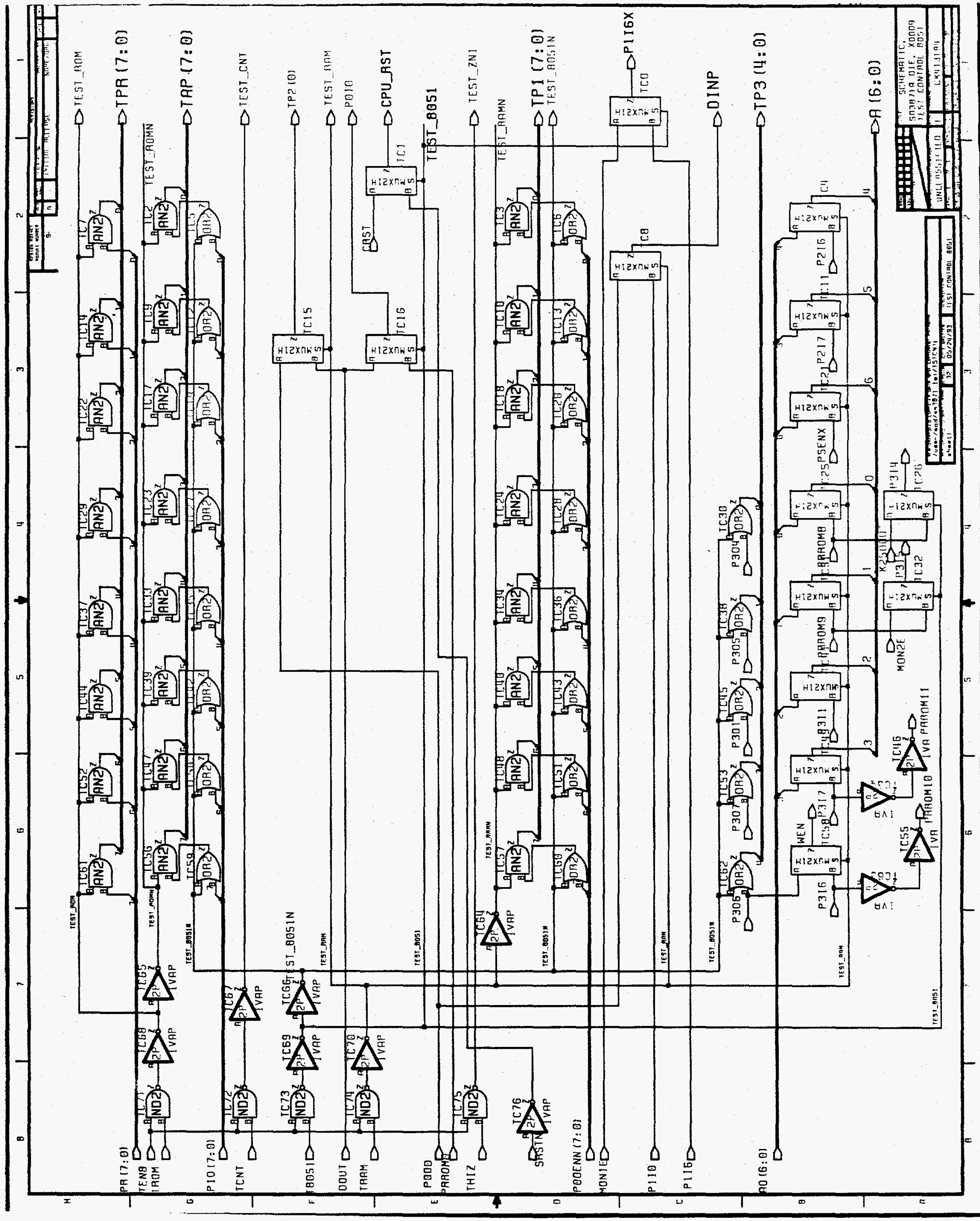



INTCONTROL
X0010
T28
TSTCNTL
X0009
T27
SCHEMATIC, SA3071A OIE, X0003
INTENT CONTROLLER
UNCLASSIFIED
E1DIS
E2DIS
WDOUT
AIF
PDREG
ICLK
TUOS1E
TUOS2E
ISLS1E
ISLS2E
SAFE_MON_DIS
ENABLE1E
ENABLE2E
TXD
SCANO
TEST_RAM
TEST_ZN
TP1(7:0)
TP2(7:0)
TP3(4:0)
IUOS_MON
PDI
ID_MON
EUOS_DATA
CLS_DET
PB_MON
SAFE_PWR_MON
PREARM_PWR_MON
SYS_ENB_MON
WDIN
VISMON
T_ENB
T_BOSI
T_BOM
T_HIZ
T_CNT
T_RAM
SCANI
RSIC_RST
CLK

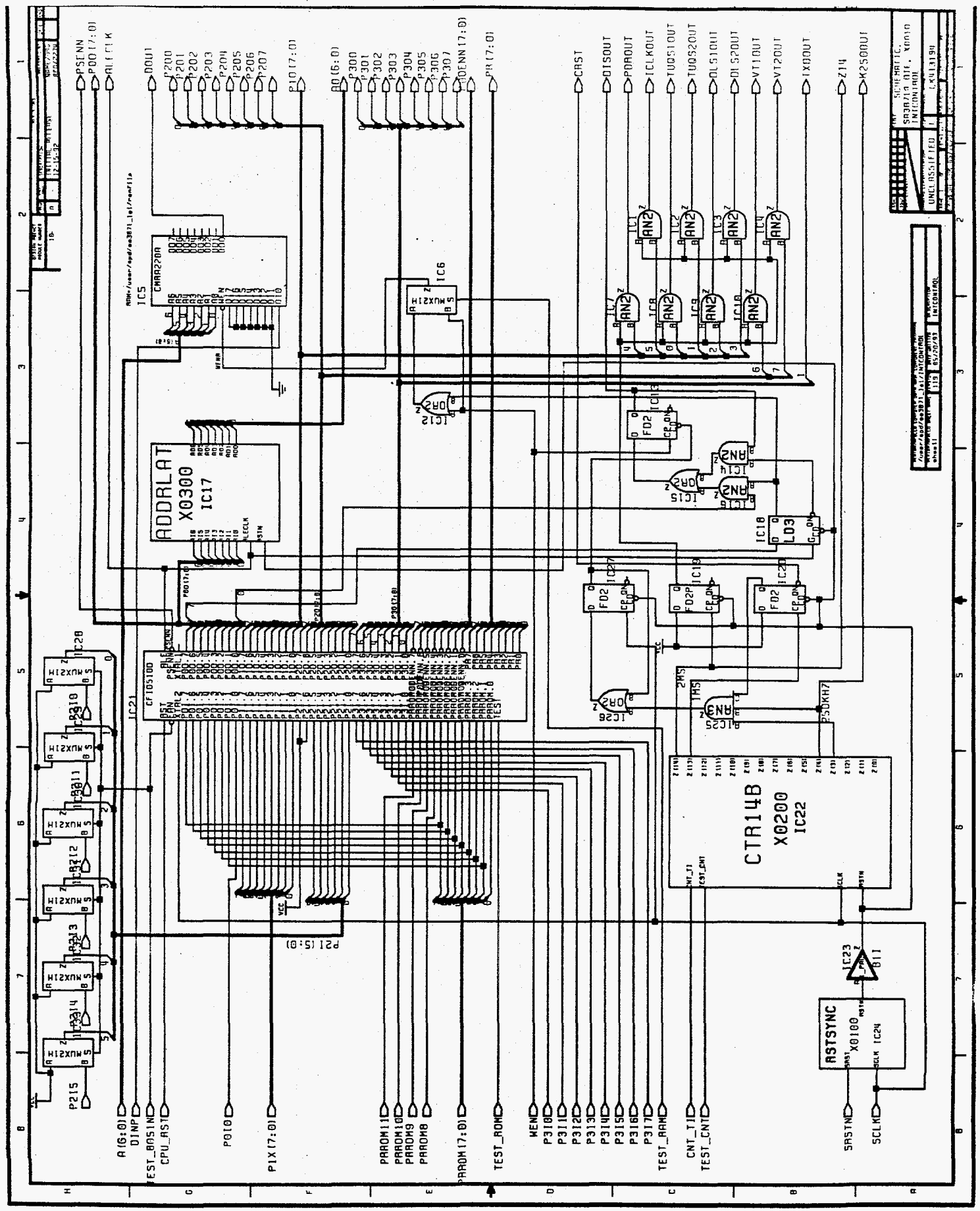
(a)


TP1(7:0)
TP2(7:0)
TEST_ZN
PRROM(7:0)
TAP(7:0)
TPR(7:0)
P1I(7:0)
TP3(4:0)
TEST_RAM
P6ENN
P207
P206
T71
T68
T65
T62
T59
T56
T53
T50
T72
T69
T66
T63
T60
T57
T54
T51
T73
T70
T67
T64
T61
T58
T55
T52
&8045CAU
&8045CA
P07
P06
P05
P04
P03
P02
P01
P00
P17
P16
P15
P14
P13
P12
P11
P10
P3I6
P36
P3I7
P37
P3I1
P31
PRROM9
P35
PRROM8
P34
PSENX
PSEN
P2I7
P27
P2I6
P26

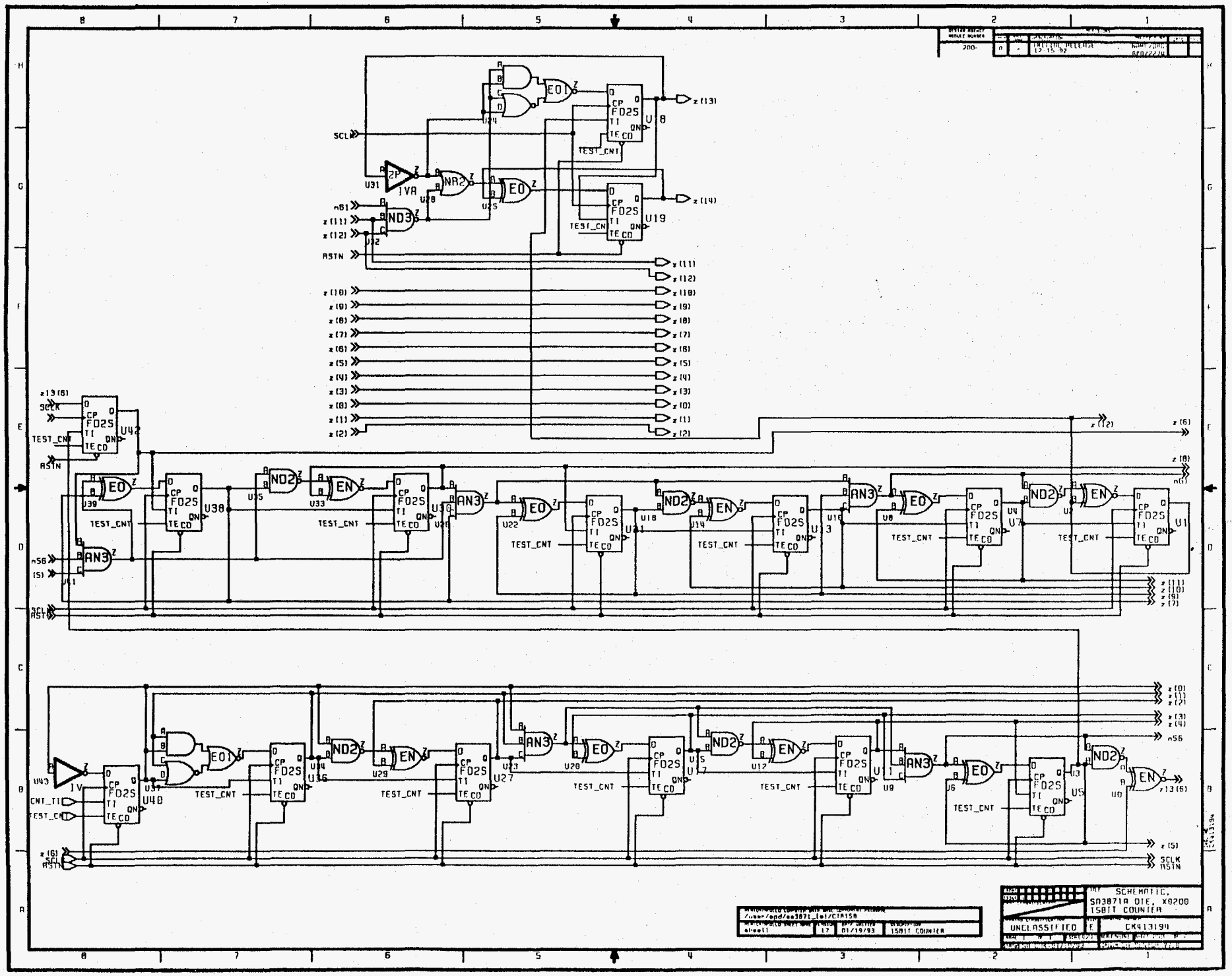
(b)


SCHEMATIC, SA3871A DIE, X0009 TEST CONTROL 8051
TEST_ROM
TPR(7:0)
TEST_ROMN
TAP(7:0)
TEST_CNT
TP2(0)
TEST_RAM
P010
CPU_RST
TEST_8051
TEST_ZN1
TEST_RAMN
TP1(7:0)
TEST_8051N
P116X
DINP
TP3(4:0)
A(6:0)
CRST
PA(7:0)
TEN8
TROM
P10(7:0)
TCNT
T8051
DOUT
TRAM
P000
PAROM
THIZ
SRSTN
P00ENN(7:0)
MON1E
P110
P116
A0(6:0)
MON2E
PAROM10
PAROM11
WEN
P216
P217
P5ENX
P314
P316
P317
P301
P304
P305
P306
P307
P311
K25000
TCRAROM8
TCRAROM9

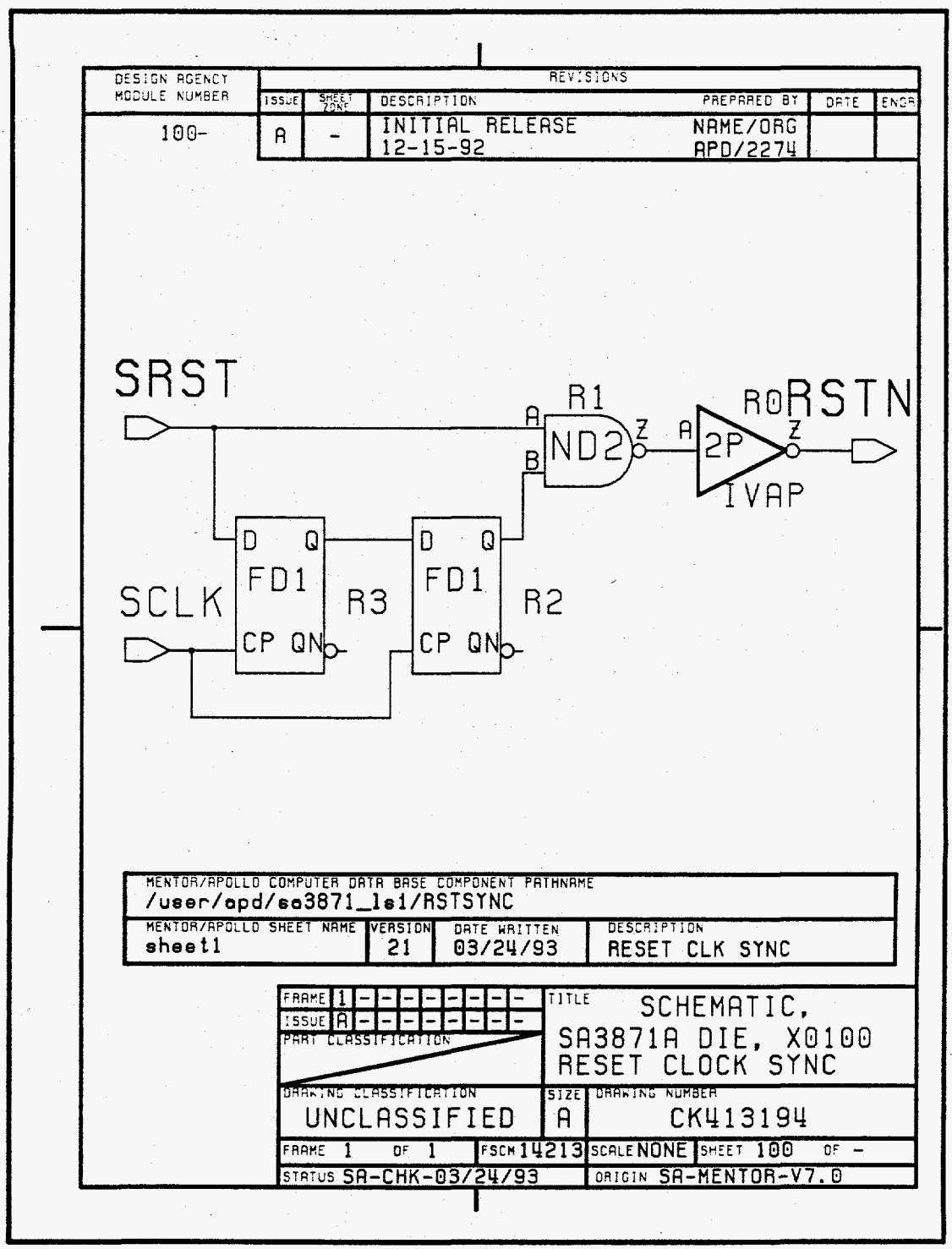
(c)


ADDRLAT
X0300
IC17
CTR14B
X0200
IC22
RSTSYNC
X0100
IC24
CMRA220A
IC5
CF105100
IC21
IC6
IC1
IC2
IC3
IC4
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC18
IC19
IC20
IC23
IC25
IC26
IC27
IC28
LD3
FD2
FD2P
AN2
OR2
MUX21H
P215
P214
P213
P212
P211
P210
P2I(5:0)
A(6:0)
DINP
TEST_BOSIN
CPU_RST
P0I0
P1I(7:0)
PAROM11
PAROM10
PAROM9
PAROM8
PAROM17:0
TEST_ROM
WEN
P310
P311
P312
P313
P314
P315
P316
P317
TEST_RAM
CNT_II
TEST_CNT
SRSTNC
SCLKC
DOUT
P200
P201
P202
P203
P204
P205
P206
P207
P1O(7:0)
AO(6:0)
P300
P301
P302
P303
P304
P305
P306
P307
PR(7:0)
CAST
DISOUT
PDAOUT
ICLKOUT
TUOS1OUT
TUOS2OUT
DLS1OUT
DLS2OUT
VT1OUT
VT2OUT
IX0OUT
Z14
K250OUT
PSENN
PDO(7:0)
ALECLK
P30(7:0)
P20(7:0)
P0(7:0)
2MS
1MS
P50KA7
B11

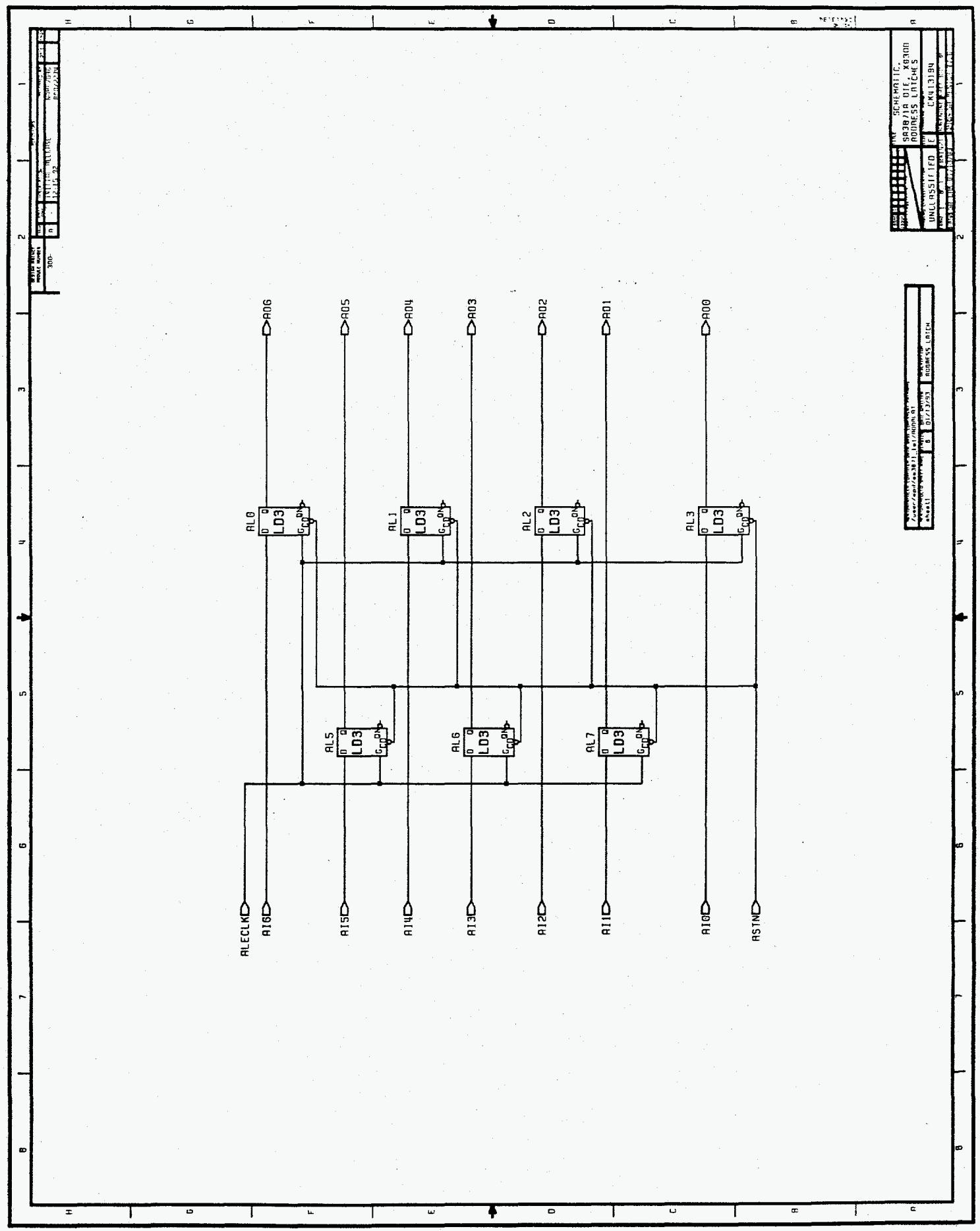
(d)


SCL
RSTN
TEST_CNT
FD2S
EO1
EO
EN
ND2
AN3
NA2
IVA
IV
z(13)
z(14)
z(11)
z(12)
z(10)
z(9)
z(8)
z(7)
z(6)
z(5)
z(4)
z(3)
z(0)
z(1)
z(2)
n56
(5)
CNT_TI
SCLK
SCHEMATIC,
SA3871A DIE, X0200
15BIT COUNTER
UNCLASSIFIED
CK413194
15BIT COUNTER

(e)

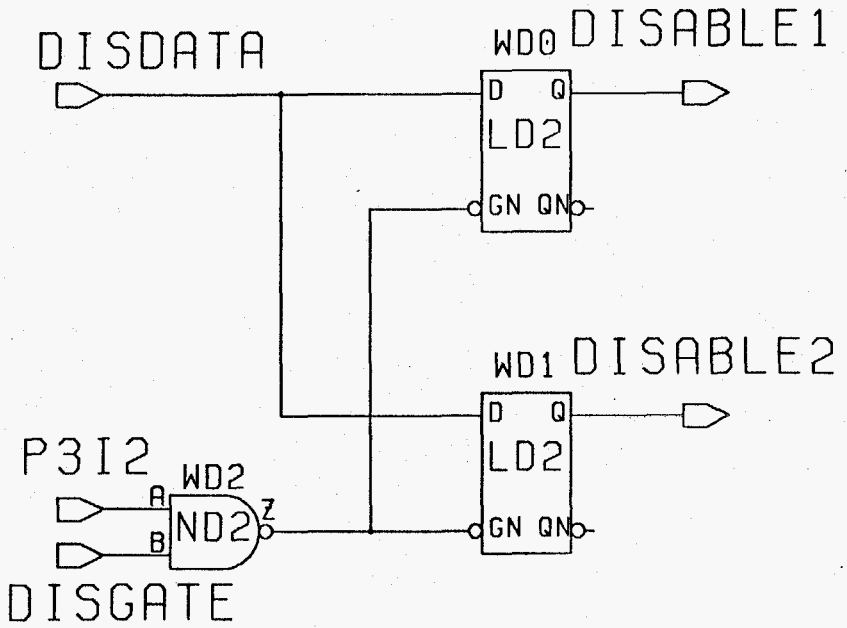

DESIGN AGENCY MODULE NUMBER
100-
REVISIONS
ISSUE
SHEET ZONE
DESCRIPTION
PREPARED BY
DATE
ENGR
A
-
INITIAL RELEASE 12-15-92
NAME/ORG APD/2274
SRST
SCLK
R1
ND2
A
B
Z
R0
2P
IVAP
RSTN
D Q
FD1
CP QN
R3
R2
MENTOR/APOLLO COMPUTER DATA BASE COMPONENT PATHNAME
/user/apd/sa3871_1e1/RSTSYNC
MENTOR/APOLLO SHEET NAME
sheet1
VERSION
21
DATE WRITTEN
03/24/93
DESCRIPTION
RESET CLK SYNC
FRAME 1
ISSUE A
PART CLASSIFICATION
TITLE
SCHEMATIC,
SA3871A DIE, X0100
RESET CLOCK SYNC
DRAWING CLASSIFICATION
UNCLASSIFIED
SIZE
A
DRAWING NUMBER
CK413194
FRAME 1 OF 1
FSCM 14213
SCALE NONE
SHEET 100 OF -
STATUS SA-CHK-03/24/93
ORIGIN SA-MENTOR-V7.0

(f)


SCHEMATIC,
S938/1A DIF, X8100
ADDRESS LATCHES
UNCLASSIFIED
CKU13194
A06
A05
A04
A03
A02
A01
A00
AL0
AL1
AL2
AL3
AL5
AL6
AL7
LD3
ALECLK
AI06
AI05
AI04
AI03
AI02
AI01
AI00
ASTN

(g)

DESIGN AGENCY MODULE NUMBER	REVISIONS					
	ISSUE	SHEET ZONE	DESCRIPTION	PREPARED BY	DATE	ENGR
8-	A	-	INITIAL RELEASE 12-15-92	NAME/ORG APDISCH/2274		



MENTOR/APOLLO COMPUTER DATA BASE COMPONENT PATHNAME			
/user/apd/sa3871_le1/WD			
MENTOR/APOLLO SHEET NAME	VERSION	DATE WRITTEN	DESCRIPTION
sheet1	2	03/31/93	WATCHDOG

FRAME 1 ISSUE A	PART CLASSIFICATION	TITLE SCHEMATIC, SA3871A DIE, X0008 WATCHDOG
DRAWING CLASSIFICATION: UNCLASSIFIED	SIZE B	DRAWING NUMBER CK413194
FRAME 1 OF 1	SCM 14213	SCALE NONE SHEET 8 OF -
STATUS SA-CHK-03/31/93		ORIGIN SA-MENTOR-V7.0

Appendix 2. Nuclear Safety Critical SRAM Characterization and Aging Study Reliability Support Report #95-4

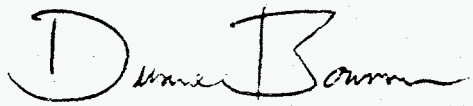
Sandia National Laboratories

Albuquerque, New Mexico 87185-1081

date: September 11, 1995

to: Brent Meyer, MS-1072 (2274)

from: Duane Bowman, MS-1081 (Reliability Physics Dept. 2276)



subject: Nuclear Safety Critical SRAM Characterization and Aging Study
Reliability Support Report #95-4

Introduction

106 Commercial versions of the SA3871 have been procured from LSI Logic, in order to characterize the sensitivity of its SRAM volatility to its board-level test conditions, and to perform a stockpile aging study of the SRAM volatility. We have burned-in all 106 parts so they would resemble WR parts during this study.

It became evident early on that in order to provide data that would be useful to the next-assembly customer, and to understand exactly what is going on inside the SRAM, we would have to devise IC-level testing that represented a "look-alike" to its next-assembly use. Leroy Tafoya, John Dye and I took several sets of measurements from the MC4396 intent board, in order to understand exactly what electrical and environmental conditions the SA3871 sees, and how it responds. This data was used by Gerald Hash in the Radiation Assurance and Technology Department 1332 to devise the SA3871 testing. Gerald also performed all of the characterization. I enlisted the aid of Mike Deveney in the Component Information & Management Department 2252 to model the SRAM and its use conditions, in order to help us devise the testing and to predict sensitivities to use conditions.

Findings

Preliminary results have been obtained. The major finding is that reset-time is highly sensitive to V_{dd} rise-time, previously unknown. The expected high sensitivity to temperature has also been characterized. We have made significant progress in understanding the device physics of the SRAM volatility: it turns out that the primary data leakage path is a mildly forward-biased p-n junction, previously unknown; and a mechanism whereby charge can be made to preferentially accumulate back onto the data node has been discovered. These account for the two major dependencies, ambient temperature and V_{dd} rise-time, that the next-assembly customer needs to be concerned with. We have also discovered that the reset-time is very dependent on the particular IUQS code used. Finally, sensitivities to V_{dd} level and V_{dd} fall-time have also been investigated and found to be of less concern.

Detail

Figure 1 shows the manner in which bits reset in the external SRAM, under "realistic" board-level testing conditions at -55°C. This is actually a facsimile of what is likely occurring in its next assembly use, since we cannot get this data off of the board, and instead had to obtain it from our system-level "look-alike" testing. All parts tend to have this general shape of reset-time distribution, but the time-scale can vary considerably from part to part. Also, reset-time depends on more than this reset-time distribution, as explained in the next paragraph.

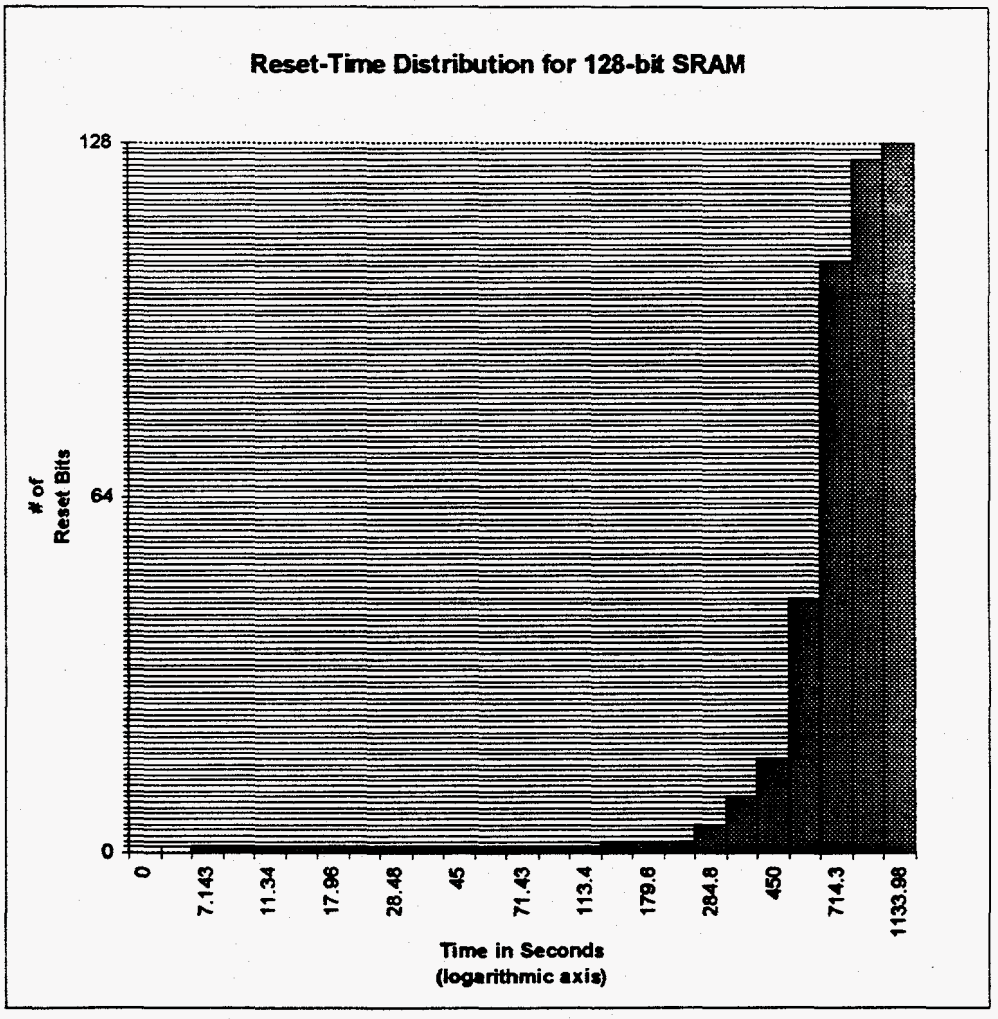


Figure 1

In our ASIC-level test, we write 1's into all 128 bits of the SRAM, and monitor each bit as it resets. However, we must remember that at the board-level there are 96 bits stored in the SRAM, half of which are 1's. Hence, there is a 48:128 or 0.375 chance that any given bit in the SRAM would have contained a "1", had the ASIC been tested with the real IUQS pattern on its board. So, it may take anywhere from 1 to 10 of the 128 SRAM bits to be reset before the IUQS code would have been invalidated, using a

criteria of 99% confidence. By the time 20 bits have reset, we are 99.99% confident that the IUQS code would have disappeared. So, safing at the board-level represents a combination of SRAM volatility and a random process. This is an important feature because the spread in bit reset-times on a single part is as large as two orders of magnitude, with one or more bits being significantly leakier than the rest. We have observed parts that reset very quickly on the next-assembly board, but turned out to be less volatile than parts that reset very slowly on the board, due to this random process. Hence, the code itself can have a substantial effect on the results.

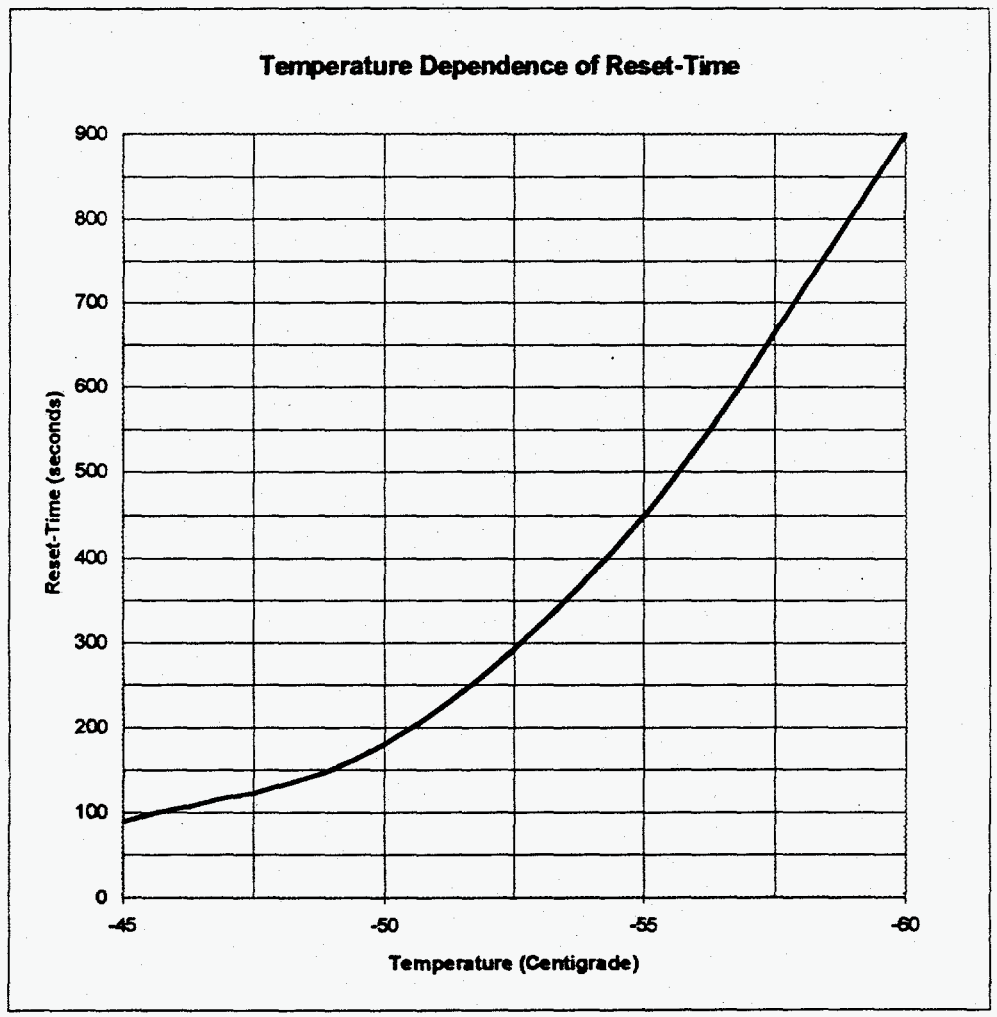


Figure 2

A typical dependence of reset-time on temperature is shown in Figure 2, for a part that takes a long time to reset. *Note that this is one of the parts that reset quite quickly on the next-assembly board, due to the randomness of the code; the figure reflects the reset-time of the 8th bit to reset of the 128 bits.* It is seen in all parts that we have tested that somewhere on the temperature axis the SRAM reset-times start to climb dramatically. This is almost entirely due to the temperature dependence of the current through a mildly forward-biased p-n junction in the unbalanced SRAM cell. At this

time, it appears that for a typical slow resetting part, a 5°C decrease around -55°C can result in about a doubling in reset-time. Temperature is controlled to within 5°C in production testing. We control it to within 1°C in our characterization study, and it is the intent of the ensuing aging study to determine if this temperature characteristic shifts to the left, toward higher temperatures.

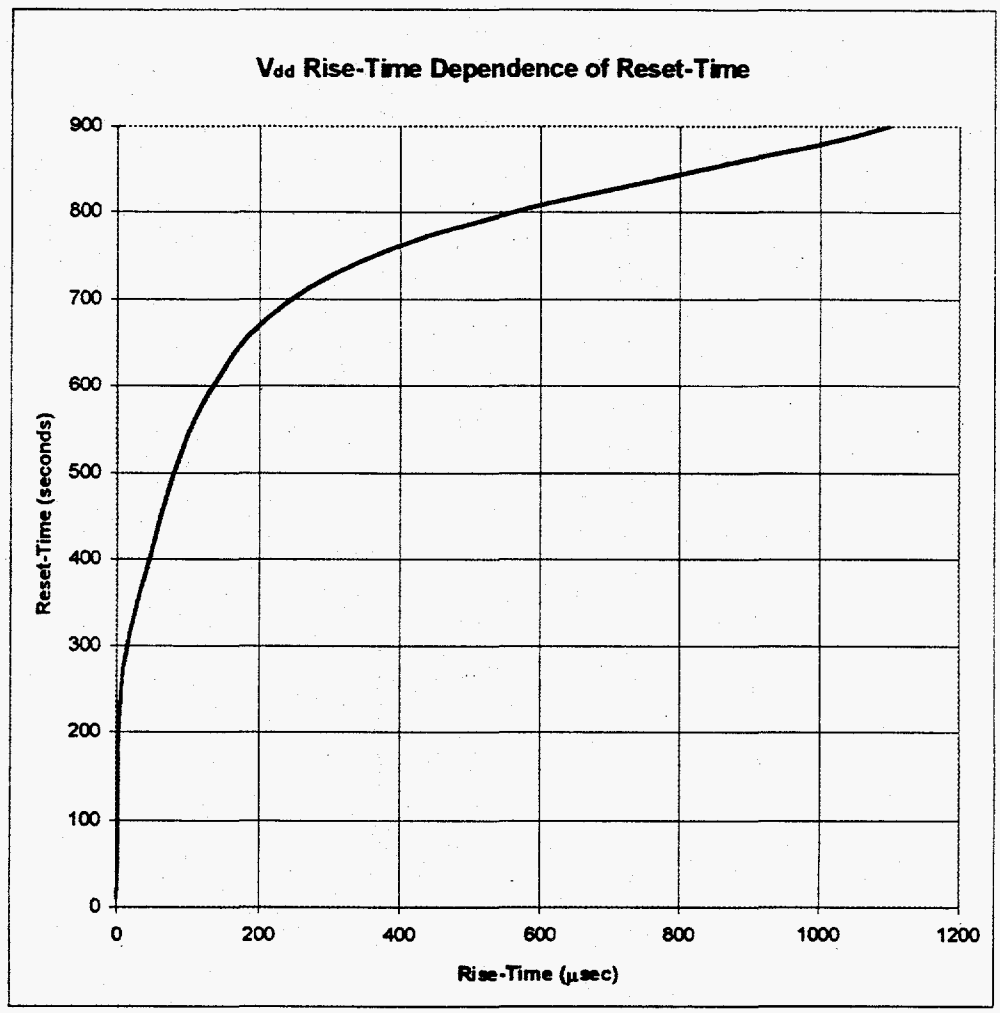


Figure 3

The dependence of reset-time on V_{dd} rise-time is shown in Figure 3. Again, this is from one of the slow resetting parts, and represents the reset-time of the 8th bit to reset of the 128 bits. *The part reset more quickly on the next-assembly board, due to the randomness of the code.* The rise-time dependence is very severe in the very short rise-time regions, as shown by the nearly vertical slope of Figure 3 near zero rise-time. This effect was predicted by analog circuit simulations done by Mike Deveney and was crucial to our progress. It turns out that with comparatively slow rise-times, the internal data node in the SRAM cell has an opportunity to charge back up before all the pull-up and pull-down transistor combinations turn on. This is important to know for our characterization activities because fast and uncontrolled rise-times are often used in

part-level testing. We will control the rise-time in our ongoing measurements and make it comparable to that seen by the ASIC on the board. The board-level rise-time is on the order of 100 µsec, being determined by several other components on the board in the powering paths to the ASIC. This is the reason that ASICs that take seconds to reset in component-level testing take minutes to reset in board-level testing. Fortunately, in the range of 100 µsec on Figure 3, the dependence of reset-time on further decreases in rise-time is not as severe as it is for very fast rise-times - it takes more than a doubling in rise-time to affect another doubling in reset-time.

The dependence of reset-time on the upper level of V_{dd} is unimportant at the board-level because charge is not trapped in the data node until V_{dd} decreases below the CMOS threshold voltage of less than one volt. For extremely fast fall-times, as might be seen in an IC tester, a higher initial voltage might result in more trapped charge; but at the board-level, the fall-time is controlled and extremely slow, such that all internal charge is easily leaked out until the transistors cut-off at a value of Vdd of less than a volt. Therefore, the initial value of V_{dd} is entirely unimportant. At the other end, when V_{dd} is reapplied, the "decision" made by the SRAM cells to retain a "1" or reset to "0" is determined by the time V_{dd} has reached 3 volts, so the upper level of V_{dd} is again unimportant. We will not vary V_{dd} in our characterization and aging studies, because it needlessly complicates more important issues, such as rise-time and self-heating of the ASIC.

The dependence of reset-time on the lower level of V_{dd} is very significant in IC-level testing. For instance, dropping V_{dd} to 50 mV results in a reset-time that is five to seven times greater than if V_{dd} were dropped to 0 volts. However, at the board-level, V_{dd} predictably drops toward zero, and in 3 minutes is always below 1 mV and no longer important. In our characterization and aging studies, because we are more concerned about SRAMs that have reset-times greater than three minutes, we will drop V_{dd} to 0 volts.

The dependence on V_{dd} fall-time is important but completely predictable, and does not need to be included in the study. The V_{dd} fall-time on the board is such that it takes about 60 seconds for V_{dd} to fall below the CMOS threshold voltage, and this merely adds about 60 seconds to the reset-time of the ASIC. Also, at around 60 seconds the V_{dd} fall-time suddenly shortens due to load changes on the board, so the rate of decay after this is relatively fast and has a relatively small and predictable effect on reset-time. By 120 seconds, it is down to 1 millivolt. It is not warranted to use the real fall-time in our test, because our test time would increase dramatically and the effect of fall-time is fully predictable. During our characterization studies, we will simply add a constant value to our reset-times to account for the predictable V_{dd} fall-time that exists on the board.

Future Activity

It is our intent to characterize more parts and to ultimately characterize the dependence of reset-time on long-term stockpile aging. This will involve placing parts in

accelerated aging environments, and will take up to a year to complete. Parts should be in ovens and undergoing radiation doses, to simulate stockpile aging in an accelerated fashion, by the end of FY95. Aging and monitoring of reset-times will continue for at least one year, depending on the acceleration of any observed aging trends. Preliminary conclusions on trends to be expected in the stockpile should be available by the end of FY96. Please see myself or the SA3871 product engineer for updates and any reports.

DJB:2276

Copy to:

Gerald Hash, 1332
Mike Deveney, 2252
Tim Mirabal, 2272
Bill Miller, 2276
John Dye, 2314
Rich Kreutzfeld, 5111

Distribution:

1 DOE/AL
PO Box 5400
Attn: WPD, T. Pellegrino
Albuquerque, NM 87185

2 Allied-Signal Inc.
Kansas City Division
2000 East 95th Street
P.O. Box 419159
Attn: D/848, R. J. Kilzer
D/848, Greg Enserro
Kansas City, MO 64141-6159

1	MS0447	R. E. Kreutzfeld, 5111
1	MS0490	R. D. Pedersen, 12324
1	MS0537	D. R. Weiss, 2314
1	MS0537	D. J. Brandt, 23148
1	MS0537	J. A. Dye, 2314
1	MS0537	M. J. Mundt, 2314
1	MS0637	R. A. Sanchez, 12336
1	MS0637	E. L. Saverino, 12336
3	MS1072	R. L. Simpson, 2274
1	MS1072	K. K. Ma, 2274
1	MS1072	B. T. Meyer, 2274
1	MS1072	R. Baldonado, 2274
1	MS1073	T. J. Mirabal, 2272
1	MS9018	Central Tech Files, 8523-2
5	MS0899	Tech Library, 13414
1	MS0619	Print Media, 12615
2	MS0100	Doc Proc, 7613-2 (For DOE/OSTI)