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A PROGRAMMABLE, LOW NOISE, MULTICHANNEL ASIC FOR READOUT OF PIXELATED AMORPHOUS SILICON ARRAYS

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Pixelated amorphous silicon arrays used for detecting X-rays have a number of special requirements for the readout electronics. Because the pixel detector is a high density array, custom integrated circuits are very desirable for reading out the column signals and addressing the rows of pixels to be read out. In practice, separate chips are used for readout and addressing. This paper discusses a custom integrated circuit for processing the analog column signals. The chip has 32 channels of low noise integrators followed by sample and hold circuits which perform a correlated double sample. The chip has several programmable features including gain, bandwidth, and readout configuration. This work is partially supported by DOE contract No. DE-AC02-76CHO3000 and NIH grant RO1-CA51397.

Introduction

Amorphous silicon pixel arrays are becoming an important tool for radiotherapy and diagnostic imaging (1,2). They are radiation hard, relatively inexpensive to manufacture, and can be as large as 0.4 m on a side. Signals from the pixels are passed via integrated thin film transistors (TFT's) to the detector periphery for amplification and digitization.

The detectors in this paper are referred to as MASDA (Multi-element Amorphous Silicon Detector Array) detectors. They have several unusual characteristics. The TFT's have a large charge injection when switched on, causing large offsets in the readout electronics. The TFT's also have a large on resistance which makes signal transfer from a pixel cell relatively slow. The pixels and buses on the detector can have large capacitance which makes low noise operation difficult. In addition, these detectors are under continuous development, resulting in a wide variation in dynamic range, capacitance, and other parameters which must be accommodated by the readout electronics.

Readout of MASDA detectors with discrete components is impractical due to the small size of the pixels and the large number of channels needed to read out an array. Custom integrated circuits are essential. In the past some attempts were made to read out MASDA detectors with ASIC's designed for other applications (3). This paper describes a 32 channel full custom integrated circuit designed specifically for processing signals from amorphous silicon pixel arrays.

General Operation

Figure 1 shows a MASDA detector with readout electronics. An image on the pixel detector is read out through a set of custom readout chips (MASDA-R chips) and commercial A/D converters. A shift register enables one row of pixel TFT gates at a time. This transfers pixel signals from a given row to columnar buses which pass the signals to the bottom edge of the detector for processing by the custom integrated circuits.

The MASDA-R readout chip has 32 identical channels intended to process the signals from 32 columns of a pixel detector. A functional block diagram is shown in Figure 2. Pixel signals are integrated, then sampled and held for serial readout through a common analog output port. One important feature of MASDA-R is pipelined operation, which allows continuous signal acquisition from row to row on the detector and avoids deadtime due to readout. Each channel has an integrator followed by two identical signal paths labeled "A" and "B". While signals from a given row are being integrated and stored in one path, the signals stored in the other path (from the previous row) are being presented to the output for readout.

Another important feature of MASDA-R is correlated double sampling with differential readout. Each

signal path has a "before" and an "after" sample and hold circuit, followed by output bus precharge circuits and analog multiplexers. The "before" and "after" circuits are identical and are used to form the differential analog output for readout. This configuration greatly reduces the effect of low frequency noise at the input, and tends to cancel common mode or systematic noise after the integrator.

The differential outputs from all the Mux/Precharge circuits feed a common pair of bus lines. The signals from each channel are placed sequentially on the common bus pair during readout. All 32 channels may thus be read out serially through Port #1. Alternatively, the control logic allows the output bus pair to be split between channels 16 and 17 in order to reduce the total readout time. In that case, Channels 1-16 are read out through Port #1 and channels 17-32 are read out concurrently through Port #2. The control logic allows the channels to be read out from top to bottom or from bottom to top.

Since MASDA-R operation is pipelined with simultaneous acquisition and readout, the time required to read out all the channels must be arranged to be equal to the time given to transfer pixel charges to the integrator.

Single Channel Operation

A pixel cell can be modeled by a diode and capacitance in parallel along with a TFT as shown in Figure 3. The TFT can be considered to be a switch with an infinite "off" resistance, a relatively large "on" resistance and parasitic capacitances Cgd and Cgs. The pixel accumulates signal charge while the TFT is off, and this charge is periodically transferred to the readout electronics by turning the TFT on. For a detector with n rows, the TFT's of any row are on for 1/n of the readout time and off for the remainder, due to sequential enabling of the rows. During the TFT off time, Cpix is initially charged to Vb-Vin and is discharged by X-rays hitting the pixel. (Vin is the integrator input reference voltage.) Enabling a row turns on the TFT's of that row which causes Cpix to be "recharged" to Vb-Vin. The necessary charge is supplied by the integrator, with a dominant time constant introduced by the R(on) of the TFT and Cpix. The integrator output signal is thus a measure of the total X-ray exposure on the pixel cell during the TFT off time.

Figure 4 shows a single MASDA-R channel. The integrator has 6 different feedback capacitors, a reset switch and a capacitively coupled charge injection circuit. Each Sample and Hold circuit has a programmable series resistor which may be used to limit signal risetime and reduce noise. Switches RSTA and RSTB provide a fast discharge path for the sampling capacitors during integrator reset. The "before" and "after" sample and hold circuits provide a differential output signal which is placed on the output bus via a precharge circuit and multiplexer. Without the precharge circuit, the parasitic capacitance of the output bus, Cbus, would reduce the magnitude and linearity of the signal seen at the chip output. When a signal path is to be read out, the appropriate precharge switches (PCA or PCB) are shorted in order to charge the output buses to the levels that are held on the sample capacitors, without disturbing the held levels. Once the buses are precharged, the precharge switches are opened and the sample capacitors are placed directly on the bus via the appropriate multiplexer switches (MuxA or MuxB). Precharge amplifier noise and offsets are thus reduced by a factor equal to the ratio of the sample capacitance to the parasitic bus capacitance.

Timing signals for the two pipelined signal paths are shown in Figure 5. Consider the signal acquisition for signal path "A" followed by the readout of signal path "A". Initially, switches RST, RSTA, and BEFA are shorted, which resets the integrator and capacitors C(BEFA) and C(AFTA). When RST and RSTA are opened, there is some charge injection from those switches and some time is allowed for the integrator to settle. After the integrator settles, switch BEFA is opened which cause a "before" sample to be stored on C(BEFA). Immediately after BEFA opens, switch AFTA is shorted along with the TFT which connects the desired pixel to the integrator input. The TFT has a relatively large charge injection which is canceled to first order by injecting a programmable charge Qin through Cinj at the same time AFTA is shorted. While AFTA and the TFT are shorted, the pixel cell is being recharged and a signal is transferred to the sample and hold capacitor C(AFTA). To end the acquisition cycle, AFTA is opened followed a short time later by the opening of the TFT. This results in an "after" sample being stored on C(AFTA).

Chip readout is controlled by a readout clock that places the signals stored on the sample and hold capacitors onto the readout bus pair at the appropriate time. Readout of signal path "A" is shown on the right half of Figure 5. All 32 channels may be read

out through Port #1 or Channels 1-16 may be read out through Port #1 while channels 17-32 are read out through Port #2. Figure 5 shows a readout using both ports. On the first clock tick of the readout cycle, one output bus is precharged with the signal from channel 1 and the other output bus is precharged with the signal from channel 17. After precharge, the signals for channels 1 and 17 are directly multiplexed to the appropriate buses. After channels 1 and 17 are read out, 2 and 18 are read out and so forth until all 32 channels have been read out.

Test Results

The MASDA-R chip, which has dimensions of 5.4 mm x 5.7 mm , was designed in the Hewlett Packard 0.8 micron CMOS process. Approximately 250,000 channels have been fabricated and packaged in 64 pin TQFP packages. The devices have been tested separately and with detectors. Results presented here are for chip tests only.

The MASDA-R has a maximum output range of 3.5 V when operating from a 5.5 V power supply. Linearity error over the full range is less than 0.1 %. The chip is designed to handle a maximum input charge of 80 pC but can also provide a full scale output for much smaller input charges. Integrator gain and range are adjusted by 6 binary weighted feedback capacitors (0.36 to 11.6 pF) which can be inserted in any combination. The integrator is designed to have a much faster risetime than the signal arriving from the detector. Integrator input capacitance affects the integrator response time. A lower input capacitance means a faster integrator risetime and therefore more noise. To obtain a more uniform response with different input capacitance, bandwidth adjustment is provided in the form of a programmable resistor in series with the sample and hold capacitor. Input noise measurements with different BW settings are shown here for an integrator feedback capacitance of 2.9 pF.

Cin	t(10-90)	Noise
10 pF	1.73 us	460 erms
30	2.05	690
50	1.50	1120
50	1.93	1000
50	2.40	920
70	1.80	1330
90	2.15	1540

As can be seen from the 50 pF measurements, the user can make a tradeoff between integrator risetime, which should not be unnecessarily fast, and equivalent input noise.

Crosstalk from one channel to a neighbor channel is less than 0.1%. Crosstalk from signal path "A" to signal path "B" in the same channel is less than 0.02%. Power dissipation is about 8.5 mw/channel.

In a typical application the output of the MASDA-R chips are intended to be digitized to 16 bits. Off line gain and offset corrections are made for each pixel cell.

Conclusion

A 32 channel full custom integrated circuit for amorphous silicon pixel arrays has been built and successfully tested. The MASDA-R represents a significant advancement in the development of integrated circuit readout electronics for amorphous silicon pixelated arrays.

References

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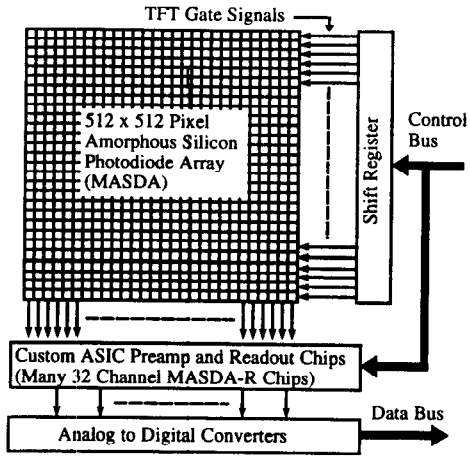

Figure 1 - Pixel Array with Custom Readout Chips

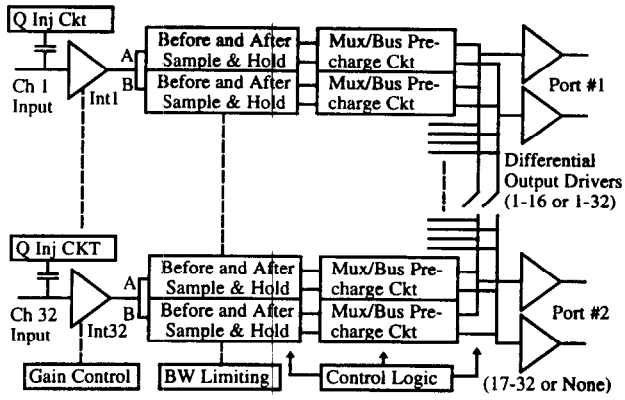

Figure 2 - Block Diagram of 32 channel MASDA-R Readout Chip

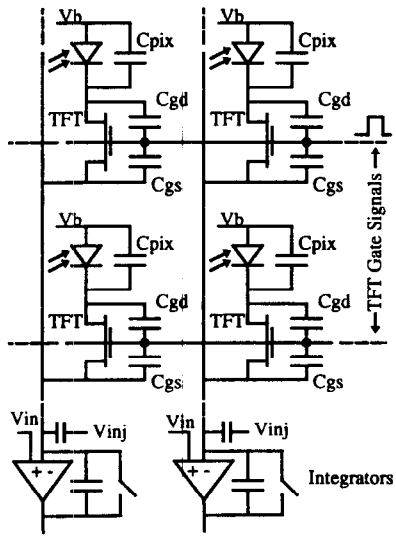

Figure 3 - Amorphous Pixel Cells and Integrators

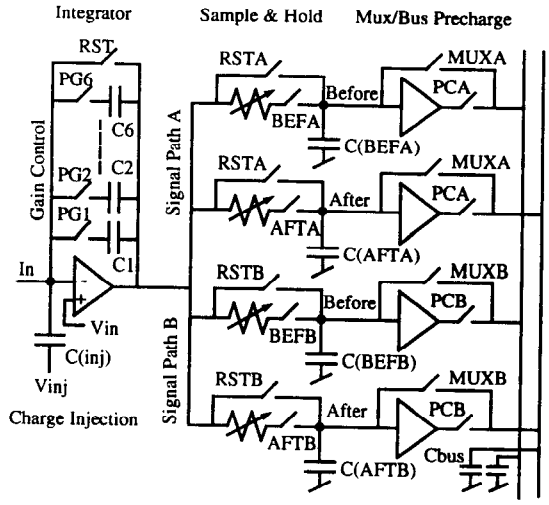

Figure 4 - MASDA-R Single Channel Diagram

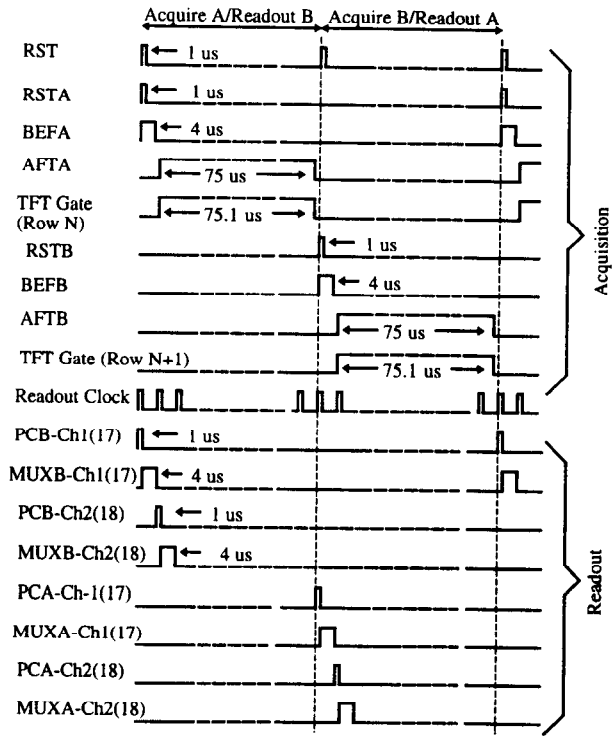

Figure 5 - MASDA-R Typical Timing Diagram