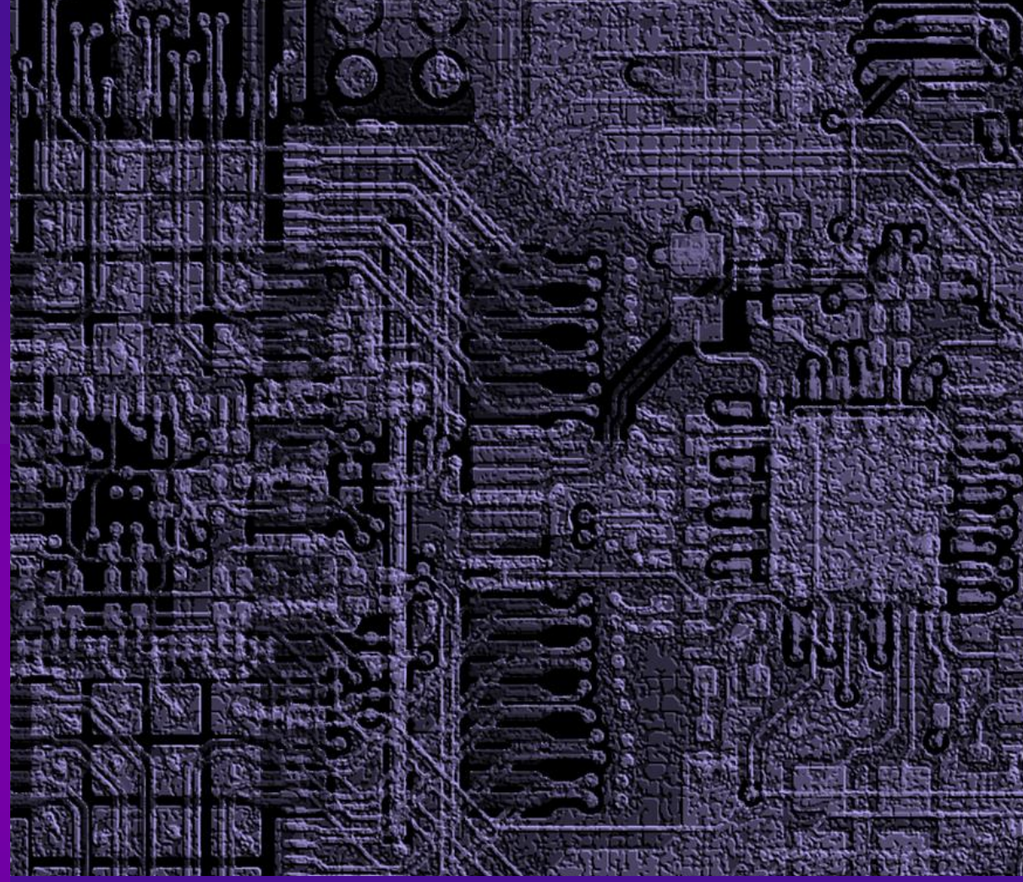
Design, verification and integration of a fast digitizer for nuclear structure experiments. Application to the detectors EXOGAM and NEDA

PhD Thesis



Design, verification and integration of a fast digitizer for nuclear structure experiments. Application to EXOGAM and NEDA detectors

Francisco Javier Egea Canet

Supervisors

Dr. Vicente González Millán
Dr. Andrés Gadea Raga

2015

PhD Thesis
Francisco Javier Egea Canet

VNIVERSITAT DE VALÈNCIA

VNIVERSITAT DE VALÈNCIA

Departament d'Enginyeria Electrònica

PhD Thesis

Design, verification and integration of a fast digitizer for nuclear structure experiments. Application to EXOGAM and NEDA detectors

Presented by:

Francisco Javier Egea Canet

Supervised by:

Dr. Vicente González Millán
Dr. Andrés Gadea Raga

Index

Abstract

Nuclear structure experiments are carried out in order to understand the many properties of a very complex body: the nucleus. Different nuclear isotopes involve very different properties as for example stability, deformation, production cross-section, decay modes, etc. It is well known that a comprehensive understanding of these properties is compulsory in order to deal with the most recent challenges of nuclear fundamental physics, as well as in more applications such as: radiotherapy, medical imaging, astrophysics, biology, material sciences, nuclear energy, etc. Up to now, around 6000 different nuclear isotopes are predicted to exist, but until now the properties of only 3000 have been partially studied.

Measuring nuclear properties mentioned above is not an obvious task. It requires a large knowledge about interaction of radiation with matter, complex detectors arrays with hundreds of channels, and therefore, complicated electronics to achieve such measurements. The most well-known and useful method used to observe the nuclear properties is the gamma-ray spectroscopy, which obtains the energy spectra based on the energy of the gamma rays impinging in the detector. In order to perform efficiently the gamma-ray spectra, and to be capable of observing the properties of exotic nuclei, it is required complex and expensive instrumentation, which, for the case of nuclear structure is being implemented by means of high-resolution gamma-ray spectrometers coupled with ancillary detectors, such as neutron detector or charged particle detectors.

Regarding the electronics, it is obvious that most applications are heading towards the digital electronics, making possible and easier the implementation of more generic and flexible electronics, given the capability to implement more complex data analysis algorithms, faster communication protocols and reconfigurable firmware, among others. However, part of the measurements used to characterize the nucleus when performing high-resolution spectroscopy, such as the time of flight or the energy resolution, still, the performance obtained with analog electronics overcomes the capabilities of digital systems, entailing a big challenge when these measurements move to the digital world without a big performance drop.

This text aims to introduce and show the capabilities which can be obtained with digital systems when performing measurements with high-resolution gamma spectrometers, keeping a good energy resolution while enhancing capabilities related to integration, economic, flexibility and communications. Concretely text deals with the design, verification and integration of a high-speed digitizer, capable to deal with the requirements of the HP-Ge high-resolution gamma-ray spectrometer EXOGAM (EXOtic GAMma array) and the future NEDA (Neutron Detector Array) fast neutron detector, used as an ancillary neutron detector for EXOGAM and AGATA. Finally, the conclusion shows the successful attempt to integrate a digital system in a task which has been implemented up to the date with analog electronics. Therefore, showing the evidence that high-resolution gamma-ray spectroscopy with digital systems is definitely possible, this text establishes an outline for future applications in the field of instrumentation applied for the nuclear structure research.

Resum

Els experiments en estructura nuclear es porten a terme per poder entendre les propietats d'un sistema molt complex, el nucli atòmic. Els isòtops nuclears posseeixen propietats molt diferents, com ara puguen ser la estabilitat, deformació, secció eficaç de producció, modes de desintegració, etc. És evident que un enteniment complet d'aquestes propietats és necessari per poder satisfer les finalitats a les quals es pretén arribar, tant en el marc de la física teòrica nuclear, com en aquelles aplicacions que se'n deriven d'ella, com ara: radioteràpia, imatge mèdica, astrofísica, biologia, ciència dels materials, etc. Fins al moment, s'han predit un nombre de 6000 isòtops existents, encara que les propietats de tan sols uns 3000 s'han estudiat parcialment.

La mesura de les propietats del nucli no és per res una tasca fàcil. Requereix d'un ampli coneixement sobre la interacció de la radiació amb la matèria, la instal·lació de complexos detectors amb centenars de canals, així com la electrònica associada i les granges d'ordinadors que s'utilitzen per al processat. L'eina més utilitzada pels físics avui en dia per a obtenir les propietats del nucli és la coneguda com espectroscòpia de rajos gamma, que utilitza l'espectre d'energies d'aquests rajos mitjançant la energia dels rajos que col·lisionen al detector. Per a dur aquesta tasca eficientment, sobretot a aquells nuclis anomenats "nuclis exòtics", es necessita una complexa infraestructura, que per al cas de la anàlisi de la estructura nuclear, s'implementa amb espectròmetres de rajos gamma d'altra resolució, junt amb detectors complementaris com ara els detectors de neutrons i els detectors de partícules carregades.

Pel que fa a la electrònica, es evident que moltes aplicacions s'encaren cada cop més a la electrònica digital, la qual fa més fàcil la implementació d'una electrònica més flexible, donada la versatilitat dels dispositius programables per a poder implementar algoritmes complexos, així com també de la seua integració. Tanmateix, algunes de les mesures que s'utilitzen per a la caracterització del nucli, com per exemple el temps de vol o la resolució en energia encara es fan actualment amb mètodes analògics, donada la gran dificultat per dur-los a terme mitjançant electrònica digital sense degradar la qualitat de la mesura.

Aquesta tesi mostra el rendiment que se'n pot obtenir d'un sistema digital qual es fan mesures amb espectròmetres de rajos gamma d'altra resolució, on el desafiament és mantenir la qualitat dels sistemes analògics pel que fa a la resolució en energia, i amb la millora que aporten els sistemes digitals per a poder donar més flexibilitat, integració, millorar les comunicacions, així com també reduir els costs. Concretament, el text tracta sobre el disseny, proves i la integració d'un digitalitzador d'alta velocitat, que siga capaç de complir amb les especificacions que es requereixen per al espectròmetre d'alta resolució EXOGAM (EXOtic GAMma array), així com també del futur detector de neutrons NEDA (NEutron Detector Arrary), que serà utilitzat complementàriament amb EXOGAM i AGATA. Les Conclusions d'aquest text mostren l'èxit al integrar un sistema digital que fins al moment s'ha utilitzat mitjançant mètodes analògics. D'aquesta manera, amb la prova de que fer espectroscòpia de rajos gamma mitjançant sistemes digitals, aquest text estableix un marc de treball per a futures aplicacions al camp de la instrumentació i electrònica aplicada per al futur de la recerca en la estructura del nucli atòmic.

1. Introduction

This first introductory chapter is aimed to present the work which has been carried out during the preparation work of this PhD thesis. Special attention is paid on the research motivation, the objectives proposed and the methodology employed to carry on the current research. The last point, called "Thesis draft", briefly presents each of the following chapters with a short description, so the reader can follow easier the document.

1.1. Introduction

The understanding of the atomic nucleus is the task of the nuclear physics field. It is a challenging goal since the atomic nucleus is a quantic mesoscopic system built by two types of fermions. Finding out the nuclear properties of the thousands of bounded isotopes is a task hardly to be reached soon. Yet, the enrichment in knowledge concerning the nuclear structure has encouraged new tendencies and techniques in other scientific disciplines such as medicine, astrophysics, material sciences, etc. Therefore, the synergies among the different scientific branches not only provides tangible solutions and new developments yet to be used by the human being so far in a near future, but also, elaborates a connected tissue of fundamental knowledge among the different scientific disciplines, going towards a future better understanding of the physics. Since the 60s, one of the methods arisen for research in nuclear structure which became the most popular, and still widely used nowadays is the so-called gamma-ray spectroscopy, which uses the detection of the gamma-rays to obtain properties from nuclei. Yet, not only some nuclei involve very complex structures, but additionally, most of them, around 99.5 % of the predicted nuclei, are unstable, causing the nuclei under research to fall into a different nuclei, obtaining a complete different structure. A study of these nuclei requires among others high-resolution gamma spectroscopy techniques so that the energies can be measured accurately in order to develop more reliable nuclear models. Therefore, high-resolution gamma spectroscopy has provided remarkable merits on the field of the nuclear physics such as research on neutron-rich nuclei, decay from superdeformated states, triaxial nuclei, etc. For more details of the merits obtained with high-resolution gamma spectroscopy, refer to [1].

A parameter of paramount importance in the field of gamma-spectroscopy is the energy resolution, which is defined as the capability of a system to distinguish between energies when they are close to each other. Hence, high-resolution spectra show narrower peaks, corresponding to the more accurate measures of the energies of the captured gamma-rays, which, unlike with lower resolution acquisition methods, as the peaks become widened, can make undistinguishable two energies as they are detected as a single peak. Energy resolution may be degraded by the type of detector used but also the electronics noise as well.

Nowadays the research on nuclear structure has motivated physicists and engineers to build up high-resolution detector arrays to obtain higher efficiency information regarding still unknown decay levels and properties of exotic nuclei. Among the most modern instruments, we should mention the HP-Ge (High-Purity Germanium) array detectors, such as EUROBALL [2], GAMMASPHERE [3], MINIBALL [4], EXOGAM [5], AGATA [6], GRETA [7], which are

coupled together with ancillary neutron detectors such as Neutron Wall [8, 9], the future NEDA [10, 11], and charged-particle detectors such as TRACE [12] and DIAMANT [13] among others in order to obtain information regarding the reaction channel.

Obtaining high-resolution spectra depends mostly on the detector carrying out the task. Even though the detector geometry, construction and material impact mostly on the resolution, the electronics and processing techniques influence largely the instrument performance, not only on the resolution, but also on the read-out and processing capabilities. Traditionally, electronics dealing with the signal processing of pulses from the detectors had always been based on analog systems, using a slow A/D converter to acquire either the peak amplitude after shaping or the time between two signals after applying Time-to-Amplitude (TAC) conversion techniques. Although analog electronics present the best performance for some features, such as resolution for time and energy measurements, the problems that analog electronics entail, such as lack of flexibility, electromagnetic susceptibility, and often, the unfeasibility to implement certain algorithms makes difficult the use of analogue electronics to achieve the demands of the most modern instruments, making digital electronics, based on fast-sampling A/D devices, to get every time more into stage. For instance, the new-generation gamma spectrometer AGATA [6], being developed by a broad European collaboration expects more than 6000 channels for gamma array tracking. Therefore, the trend in electronics for the nuclear physics is more and more into the use of digital systems [6, 14, 15, 16], where more complex PSA (Pulse-Shape Analysis) algorithms, data throughput, high-speed communications and firmware reconfiguration can be achieved in a more feasible way.

The increasing use of digital electronics in this field, and motivated by the possibility to optimize both efforts and economic resources, several groups are making efforts to find common points between projects, seeking synergies between them. For our case, a synergy at the level of front-end electronics has been studied, leading to the design of a common digitizer and pre-processing electronics, the so-called NUMEXO2, which is expected to be used as the future upgraded electronics of EXOGAM (EXOtic GAMma array), and NEDA (NEutron Detector Array) [17]. The EXOGAM, [5], a HP-Ge (High-purity Germanium) gamma-ray spectrometer, currently used at GANIL (Grand Accélérateur d'Ions Lourds) facility, is undergoing an upgrade towards fully digital electronics, named as EXOGAM2 [18], proposed in 2009. This new electronics is devoted to enhance the system efficiency by performing the front-end electronics with fast sampling digitizers while preserving the energy resolution performance. NEDA [10], on the other hand is a new-generation neutron detector array currently being by a broad international collaboration of 8 countries with 21 research institutes, including Spain, expected to be used as an ancillary neutron detector together with high-resolution gamma-ray spectrometers such as AGATA, EXOGAM, etc. NEDA, as well as its predecessor, the Neutron-Wall [8], is used coupled with gamma-ray spectrometers to provide information about the reaction channels, acting as a neutron multiplicity filter. The detection mechanism of NEDA modules is based on the scintillation. For the case of NEDA, due the lack of materials only sensitive to neutrons, an organic scintillator sensitive also to gamma-rays is used together with techniques which allow to distinguish gamma-rays from neutrons. As we have seen, EXOGAM and NEDA differ much both in terms of detection mechanism and proposal coming from very different nature: high-resolution gamma-ray spectroscopy with HP-Ge versus neutron-gamma discrimination to achieve a neutron multiplicity filter using fast signals from scintillator. However, this difference is not always translated into an incompatibility when dealing with electronics.

The present PhD thesis has been done in the framework of the new digitizer plus pre-processing platform NUMEXO2. The migration from analog to digital electronics has replaced

the usage of TACs and analog shapers sampled with slow A/D devices to a new philosophy in which the main components are fast-sampling A/D, which digitize the whole waveform instead of acquiring only the time/energy parameters, and programmable logic devices, such as FPGA (Field Programmable Gate Arrays), in charge to perform, not only the time and energy measurements, but also to the management of communication protocols. NUMEXO2 is composed of a motherboard, developed mainly at the GANIL laboratory, and a set of 4 FADC Mezzanines, in charge to cope with the fast A/D conversion task, main object of this thesis. Therefore, the main goal of the present research work is the design, verification and integration of the FADC Mezzanine cards with NUMEXO2 digitizer, confirming the suitability of the new front-end electronics based on fast sampling ADC applied to the fields of nuclear physics. An added value of complexity in this research activity is the fact that the design must be suitable both for EXOGAM2 and NEDA, requiring to study both physics cases and adopting common solution.

1.2. Objectives

Considering the framework and motivations described in the previous paragraphs, the goals sought to develop in this work are summarized in the following points:

- Background study: Becoming familiar with any development involved in a scientific application requires a minimal background knowledge so that, not only the design and verification can be carried out properly, but also, one can obtain the required basic foundations to understand the aim of the overall project in a scientific framework.
- Design and verification of the FADC Mezzanines. The goals cannot be separated by their importance since all of them are necessary. However, this task can assumed as the most time-consuming. The first step is the design and verification of the FADC Mezzanine, compliant both for EXOGAM and NEDA demands. As the design and verification tasks can be considered as a whole, it must be foreseen a procedure to verify the FADC Mezzanine performance before being in any experimental environment. In order to test that the FADC Mezzanine is suitable for the experiments, we need to study, as well, how the parameters referred in electronics are linked to the parameters specified in experimental nuclear physics.
- Integration of the FADC Mezzanine in real nuclear physics experiments with EXOGAM and NEDA detectors. In this part, the FADC Mezzanine will be part of the whole electronic chain developed at the moment involving real detector units, in which the suitability for an experiment is verified.

1.3. Methodology

The methodology employed in this thesis has been structured as it follows.

Background

A first task, envisaged not only to become familiar with design specifications in the field of the nuclear physics, but also to obtain a basic background knowledge regarding the goal of the experiments carried out foresees a brief but comprehensive study of the experimental environment and the underlying physics. Therefore, a descriptive, outline of nuclear physics and radiation interaction of matter is presented, as well as the detection mechanisms

commonly used in radiation detection, focusing mainly on semiconductors and organic scintillators, as it is for our concrete case. A second field of study, more application-oriented concerns the understanding of the relationship between the parameters of common use in gamma-ray spectroscopy to the parameters commonly used in electronics. Some of these parameters of common use in physics are the energy resolution and neutron-gamma discrimination performance, not trivial to be linked with electronics-wise specifications such as ENOB, bandwidth and sampling frequency. Finally a third specific point emphasizes on the study of the instruments, involving the study of EXOGAM and NEDA detectors structure and front-end electronics. A special emphasis is also put on the study of the digitizer NUMEXO2.

FADC Mezzanine design

The core task of the research work focuses on how to apply the background concepts to a real design in a scientific application. After the background study, it is revealed that the most stringent design constraints are high performance on noise characteristics, since it is linked to the energy resolution in HP-Ge detectors, and also high sampling ratios due to the timing resolution required to perform measurements which improve the neutron-gamma discrimination performance. Both constraints will be object of a major research to seek for devices capable to carry this task out, choosing a specific fast sampling device, the core component of the FADC Mezzanine. Moreover, the choice of such a device entails later on to add extra circuitry to not degrade the acquisition, such as jitter-cleaner devices, low-noise analog matching drivers, power supply regulators, layout constraints, etc. Also, the fact that the FADC Mezzanine is part of a bigger chain will require the study of the to NUMEXO2 and the rest of closer-in electronics to the detector.

Testbench platform development

Since it is compulsory to debug the electronics before its use in real experiments, including the prototypes, this point can be considered as a feedback process with the previous point until a fully-compliant version is obtained. This task obeys the development of a customized characterization system to evaluate the FADC Mezzanine performance before releasing it for experiments with a real detector. Therefore, some extra tools, such as connectivity to standard laboratory equipment and data analysis tools must be developed. Additionally, as the amount of boards expected to be used in the final experiment can be counted in hundreds, the tool has to be developed in a production-oriented manner, meaning that during the testing stages, the process must be fast and with minimal human interaction. Some of the sub-tasks included during the testbench platform development are the design of hardware communication boards, data readout from the Mezzanines and capability to inject signals to perform different types of measurements.

FADC Mezzanine tests

Provided that the testbench platform, the verification of the FADC Mezzanine passes by performing noise measurements all along the FADC dynamic range. Since the noise measurements are of extremely big importance for the experiments, these tests are carried out with different conditions of bandwidth, sampling frequency, etc. Next, frequency-domain measurements usually performed in commercial ADCs, such as the SINAD (Signal to Noise and Distortion Ratio) and SFDR (Spurious-Free Dynamic Range) will also be carried out, as well as measurements related to the ADC nonlinearities.

FADC Mezzanine production

One of the directions after the FADC Mezzanine prototype verification is the mass production. Using the test platform, the same process must be carried out for the whole production of NEDA boards, close to one hundred cards.

FADC Mezzanine integration

This task refers to the other direction after the FADC Mezzanine has been correctly verified. Among other sub-tasks required to proceed on, it comprises the understanding, not only of NUMEXO2 motherboard, but especially of specific firmware parts and the DAQ (Data Acquisition system), placed at the back-end.

The first experiment takes place with EXOGAM detectors, where energy resolution measurements are required to verify the suitability for gamma-spectroscopy applications. For this case, most of the firmware IPs used in NUMEXO2 are already developed by other parties and ready to be used.

Nevertheless, in case of NEDA, the integration focuses not only in the neutron-gamma discrimination performance of the FADC Mezzanine, but also, in the integration with the upgraded version of the GTS (Global Trigger and Synchronization) system, envisaged to serve a larger amount of triggering channels for the future experiments with AGATA and EXOGAM. Since part of the NEDA electronics are still not ready, some modules and IPs require to be developed in order to integrate the FADC Mezzanine with the rest of the chain. Concretely, in this part it is described the techniques of Pulse Shape Analysis (PSA) in order to perform a first-level triggering algorithm, connected to the GTS.

Results and conclusions

The final point provides results both in terms of intrinsic FADC Mezzanine performance, and also, provided after the integration with the rest of electronics, within a more experimental-oriented framework. The latter make reference to the energy resolution measurements performed with EXOGAM2 HP-Ge detectors and the neutron-gamma discrimination performance for NEDA. Due to the project timeline of NEDA, the neutron-gamma discrimination performance results are taken using a real detector, but performing the measurements off-line, unlike the case of EXOGAM, where the energy resolution is already obtained after applying a moving window deconvolution (MWD) in an FPGA. After all measurements, a set of conclusions and future overview is extracted at the end of the text.

1.4. Summary

In section 1.3 it is commented the thesis methodology, whose points could be linked to one of the chapters this PhD is divided into. These are:

- Chapter 2 aims to provide a basic knowledge and concepts about the underlying physics which take part on our application. Concepts such as the gamma spectroscopy, Segré's isotopes chart, as well as the mechanisms of interaction of photons with matter, semiconductor devices, scintillators and photomultipliers.

- Once the physical concepts had been clarified, chapter 3 contextualizes the experimental environment of the FADC Mezzanine, core of this project. Therefore, EXOGAM2 and NEDA detectors are presented in this part, focusing on their structure and their front-end

electronic chain. After the detectors and electronics are introduced, the common points between them are analyzed, including the description of the NUMEXO2 digitizer, and also the set of specifications which lead to the design of the FADC Mezzanine.

- Chapter 4 deals with the electronic design of the FADC Mezzanine in detail, based on the specifications obtained from the chapter 3. A full in-view is approached starting from the first prototype block diagram to the last final FADC Mezzanine version.

- Chapter 5 makes reference to the FADC Mezzanine testbench platform design, describing the hardware, firmware and software elements needed to carry out a comprehensive characterization.

- The firmware integration tasks carried out are presented in chapter 6. It comprises two big parts: firstly, the integration of the FADC Mezzanine in NUMEXO2 together with the DAQ system. secondly, it is discussed the design and implementation of a prototype of PSA algorithm for NEDA future firmware in NUMEXO2, and how these blocks are linked to the FADC Mezzanine.

- Chapter 7 shows the results obtained for the final FADC Mezzanine version, leading to a conclusion concerning the integration of the FADC Mezzanine as part of the EXOGAM2 / NEDA electronics.

- Finally, in chapter 8, the conclusions of the thesis work are presented and discussed comprehensively, mentioning as well the future work of the whole project.

- Additionally, an Annex presents the measurements performed to a set of cables between NUMEXO2 and the analog front-end. Since the part did not belong concretely to any of the topics above, we preferred to separate it in an annex section.

2. Gamma spectroscopy physics and detection mechanisms

In this chapter the concept of gamma spectroscopy, as one of the most important methods for nuclear structure research, is presented. A brief and descriptive, but comprehensive introduction to the underlying physics of our application is necessary to establish specifications before proceeding afterwards to design the associated electronics. Therefore, in case that the reader is familiar with these concepts, this chapter could be perfectly skipped. Hence, we focus on the role of exotic nuclei in physics, photon-matter and neutron-matter interaction, as well as the detection mechanisms of semiconductors, scintillators and photomultiplier tubes (PMTs).

2.1. Exotic nuclei

Every element on the earth is constituted basically from protons, neutrons and electrons, gathered into a structure called atom. The atom structure consists in two parts: a dense region called nucleus, surrounded by a cloud of electrons. Even if the atomic nucleus size ($\sim 10^{-15}$ m) represents five orders of magnitude less than the whole atom ($\sim 10^{-10}$ m), most of the mass is concentrated in the nucleus.

Nuclei are bound thanks to a subtle equilibrium between strong and electromagnetic forces. Nucelons are bound due to the nuclear strong force, which causes protons and neutrons to be held together in the nucleus. However, when the number of nucleons increases, the action of the electromagnetic repulsive force can overcome the strong force, leading the nucleus to be unbound. Additionally, nuclei away from stability might transform into another one – whenever this process is energetically favored – by transforming protons (neutrons) into neutrons (protons) through the weak beta-decay processes or by emitting heavier particles like alpha particles. These kinds of processes are called radioactive decay and the nucleus is deemed unstable A more specific approach can be given considering the nuclear shell model [19], analogous to the atomic shell model, which describes the nucleus structure by means of different energy levels according to Pauli's exclusion principle. This model has verified, among others, the existence of magic numbers, referring to certain nucleonic arrangements with a number of nucleons such that they are completed in a shell, showing more tightly-bounds and stability than their neighboring nuclei[1].

Hence, for a given atomic number (*Z*), every combination with different number of neutrons provide what is called a nuclear isotope. Nuclei with different number of protons and neutrons

[1] *A neighbor is meant to those nuclei adjacent in the Segré chart. They are called neighboring isotopes if they are nuclei with one more or less neutrons – for example ^{40}Ca has as neighboring isotopes the ^{39}Ca, ^{41}Ca, neighboring isotones if they have one more or less proton, or neighboring isobars if they have the same mass.*

are represented in a chart called "Segré Chart", which contains the basic information of each nucleus such as the half-life, spin-parity, abundance, decay modes, etc. [20]

Segré chart arranges graphically all the different isotopes discovered till now, arranging the atomic number, also known as *Z*, on the vertical axis to the number of neutrons *N*, on the horizontal axis. There are more or less around 250 stable nuclei, and about 3000 different unstable nuclei discovered up to now although it is believed that it could exist a number of isotopes up to 6000. This sort of representation was firstly published by Giorgio Fea in 1935, and later on expanded by Emilio Segré in 1945. Since then, it has become a basic tool for the nuclear physicists. Stable nuclei are placed at a line called the *β*-stability line. For light nuclei, up to *Z*=28, the *β*-stability line increases linearly in a proportion such that *N*=*Z*. However, this linear tendency starts to bend down for nuclei heavier than *Z*=28, requiring more and more neutrons to make more stable heavier elements, due to the larger coulombian repulsion of protons.

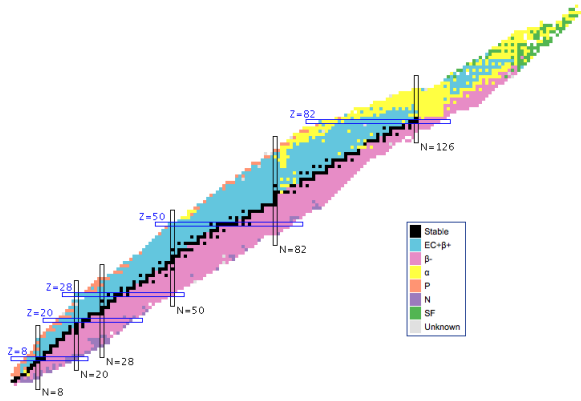


Figure 2.1: Segré Chart [20]

In Fig. 2.1 is depicted the Segré chart, showing in black the stable nuclei passing across the *β*-stability line. On its left, a group of isotopes plotted in blue make reference to the proton-rich nuclei (unstable nuclei with less neutrons than the stable ones), and on its right their counterparts in pink, the neutron-rich nuclei, referred to the nuclei with excess of neutrons. Exotic nuclei, called to those nuclei whose ratio of neutron number (*N*) to proton number (*Z*) is much larger or smaller than the nuclei usually found in nature, are delimited by the neutron and proton drip-lines, across which no isotope can exist any longer. Research concerning the proton drip-line [21] has got well-established values covering a good part of the elements, nevertheless, the heaviest element for which the neutron drip-line has been reached to its theoretical maximum is the oxygen with *N*=16, showing the neutron drip-line is still poorly understood.

Research on exploring the exotic nuclei is not retained only to dig upon the neutron drip-line. Even if the proton drip-line is by far more clarified than the neutron-drip line, there are still matters of interest to be understood within this region for certain heavy proton-rich nuclei, for instance the ^{100}Sn, the heaviest self-conjugate doubly-magic[2] nucleus expected to be bounded [22].

[2] *A magic number in nuclear physics is referred to a certain arrangement of nucleons which are particularly stable and generates an energy gap in the single-particle energies. The set of*

Furthermore, interest is also put on the properties of super-heavy elements, matter of special interest in order to find a new "valley of stability". The existence of super-heavy long-lived nuclei is evidenced based on the theoretical prediction of magic numbers existing for N=184 and Z=114 or Z=126.

2.2. High-resolution gamma spectroscopy

According to the quantum mechanics, an excited nucleus is a nucleus whose state is in a higher energy than its ground state, where the ground state is the one whose energy is the lowest for a certain nucleus [21, 23]. In fact, any excited nucleus can emit radiation in different ways before reaching to its ground state. Just to make an idea about the complexity of the nuclear decay modes, as an example, Fig. 2.2 illustrates a picture of the ^{196}Pb isotope partial decay scheme, which shows the de-excitation level paths of the nucleus.

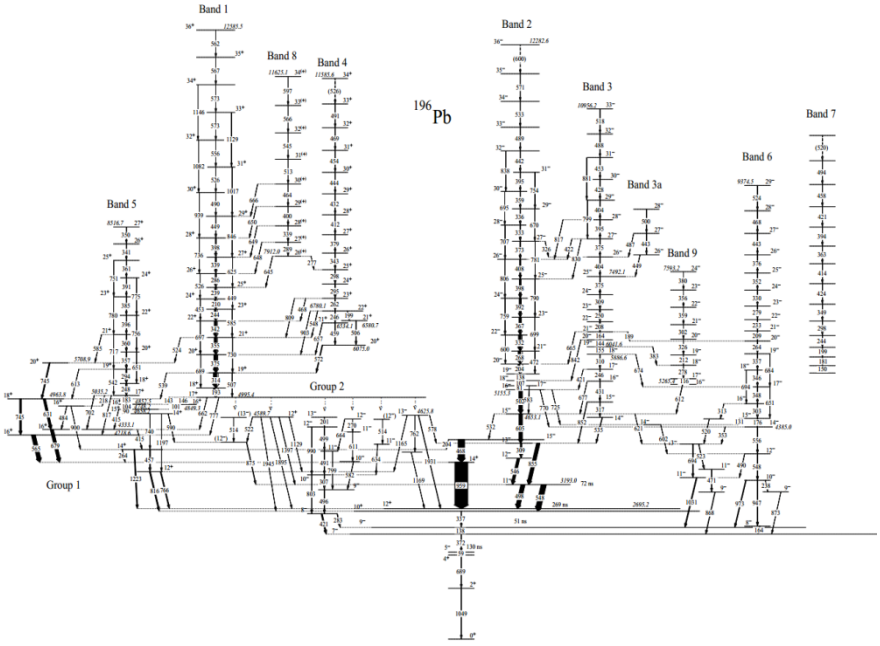


Figure 2.2: ^{196}Pb partial de-excitation level scheme [24]

One might observe different decay modes in nuclei, including among others, the gamma-ray emission, internal conversion, alpha emission, neutron emission, β+ emission, β- emission, electron capture, fission, etc. The ones related to the de-excitation of the nucleus itself, correspond to decay between different excitation energies in the same nucleus. The decay modes involving weak interaction and / or particle emission modifies as well the nucleus that emits the radiation. The most common technique to obtain the energy level scheme of a nucleus is the so-called gamma-ray spectroscopy. Gamma-ray spectroscopy is a

well-known magic numbers are 2, 8, 20, 28, 50, 82 and 126. Doubly-magic numbers are referred if both the number of protons and neutrons belong to a magic number. Examples of "doubly-magic" nuclei are ^{4}He, ^{16}O, ^{40}Ca, ^{48}Ca, ^{56}Ni, ^{100}Sn, ^{208}Pb.

method used in nuclear physics to investigate nuclei through the energy spectra of the gamma-rays emitted during the de-excitation process.

2.2.1. The role of HP-Ge in high-resolution gamma spectroscopy

The example shown in Fig. 2.2 is only one among the hundreds of complex decay schemes for a certain nuclei. The capability to distinguish these levels in the decay scheme is directly connected to the spectrometer capability to distinguish between two gamma rays of slightly different energy. This property is known as energy resolution, and it is a must for a specific branch of the gamma spectroscopy, known as high-resolution gamma spectroscopy.

High-resolution gamma-spectroscopy is where HP-Ge-based (High-purity Germanium) detectors become important. Characterized for their remarkable energy resolution, they have been successfully used in high-resolution spectroscopy projects, such as EXOGAM, EUROBALL, GaSP [25], etc. leading to important achievements such as the discovery of new decay modes of superdeformed nuclei, high-spin spectroscopy, search of symmetries in *N~Z* nuclei, etc. [1] Other materials used in gamma-spectroscopy are, among the most widely used, $LaBr_3$(Ce) [26], NaI(Tl) and CsI(Tl) [27] inorganic scintillators, even though their energy resolution cannot be compared to the HP-Ge, making the semiconductor one order of magnitude (~0.2 – 0.8 %) higher than scintillators (> 3 – 5 %). Fig. 2.3 shows the energy resolution comparison of ^{60}Co gamma spectrum using HP-Ge and NaI(Tl), where the performance from both materials can be compared. However, not all the HP-Ge features are positive. Despite of the costly material, its small energy gap (around 0.7 eV), makes them inoperative at room temperature, requiring voluminous dewars and an expensive continuous use of liquid nitrogen to keep them cooled down. Besides, large-volume HP-Ge detectors normally involve limited time resolutions, in the order of 8-10 ns, due to the dependence of the impact position of the gamma-ray in the detector [28], where scintillators become more suitable when dealing with experiments requiring faster responses ~1ns, and also rather low efficiency compared to scintillators.

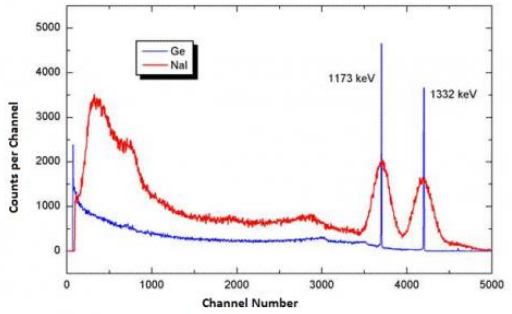


Figure 2.3: Comparison of the ^{60}Co gamma spectrum between HP-Ge and NaI(Tl) [29]

2.2.2. From the Geiger-Müller counter to the gamma-tracking arrays

Yet after the radioactivity discovery in 1896 by Henri Becquerel, the first approach to measure it was performed by using the Geiger counter (also called Geiger-Müller counter),

whose principle was discovered by Hans Geiger in 1908, producing the first practical tube in 1928 [30]. Its mechanism was based on the interaction of the radiation ionizing the gas under a high electric field, sensitive to alpha and beta particles, and to gamma-rays as well. The usage of the Geiger counters allowed the measurement of the background radiation, even though the device could not differentiate between the type of particles impinging and their energies.

It was already in the early sixties when the first gamma-spectroscopy experiments with the capability to distinguish between energies were implemented using NaI(Tl) scintillators. Taking benefit of its remarkable efficiency, the first arrays ever developed were the Spin Spectrometer and the Crystal Ball, making use of 72 detectors for the last case [31, 32]. However, in late sixties, new materials with higher resolution such as the Si(Li) and Ge(Li) detectors [33], consisting in semiconductors doped with lithium started to arise. Yet in seventies, these Ge(Li) detectors were the pioneers in high-resolution gamma spectroscopy based on germanium, achieving efficiencies around 10-15% and 2.5 keV at 1.33 MeV energy. Unfortunately, Ge(Li) detectors had to be kept at low temperatures not only during operation, yet during its growth and storage, creating a problem to deal with them. In 1978, Ge(Li) detectors were abandoned, replacing them by the actual HP-Ge (High-Purity) with BGO [34] (named as well bismuth germanium oxide or bismuth germanate) escape suppression shields to maximize the peak-to-background ratio. This new approach led to success the OSIRIS project in 1986, followed by TESSA [34], NORDBALL [35] and HERA, making use in the last case of 21 HP-Ge detectors, increasing its efficiency up to 25%. Later on, new arrays with increasingly higher efficiencies were developed alongside the world giving path to the birth of the projects GAMMASPHERE in 1993, EUROGAM [36] in 1994 and EUROBALL in 1997.

Afterwards, a big step was achieved in the field of gamma-ray spectroscopy after the introduction of segmented HP-Ge detectors, adding to the system performance, a higher position resolution. MINIBALL was the first setup of this kind used at REX-ISOLDE facility at CERN (moreover, the first one which made use of digital electronics), design with encapsulated hexagonal detectors and reaching two-dimensional position resolutions close to 5 mm. EXOGAM, SEGA and TRIGESS were developed in parallel with MINIBALL, but using segmented HP-Ge clovers.

Nowadays, a series of new important technical developments, namely the Ge detector segmentation, the pulse shape analysis techniques and gamma-ray tracking, lead to the last-generation spectrometers: AGATA in Europe and GRETA in U.S.A. In such spectrometers gamma-ray tracking allows to estimate not only the energy, position and time, but also, provides capability to reconstruct the trajectory of the scattered gamma-ray. This new approach leads to increase significantly the global efficiency, where Compton-suppression shields become already unnecessary.

2.2.3. The role of ancillary detectors in gamma spectroscopy

As we mentioned before, the study of the gamma energy spectra leads to determine most of the properties of a certain nucleus. However, the information provided from the gamma energy spectra is not sufficient, or the sensitivity of the instruments is not high enough, making necessary the usage of ancillary detectors.

An ancillary detector is an instrument coupled to a gamma spectrometer used to provide further information about the reaction channel or the de-excitation mode, making possible to

determine the nature of the isotope being analyzed or provide additional information. The most common types of ancillary detectors are neutron detectors and charged particle detectors. Some examples of ancillary detectors in nuclear physics are NEDA, object of this thesis are and Neutron Wall [8, 22] for neutron detector arrays and TRACE [12], DIAMANT [13], as examples of charge-particle detector arrays, among others. Some experiments involving coupled detectors took place at GANIL (Grand Accélérateur National d'Ions Lourds) in 2005 and at LNL (Laboratori Nazionali di Legnaro) in 2006, using EXOGAM, also object of this thesis, coupled with the Neutron Wall and DIAMANT. For future experiments in RIB[3], such as SPIRAL2 [37] at GANIL, and SPES [38] at LNL, it is expected to couple NEDA detector with AGATA, EXOGAM and TRACE.

2.3. Gamma spectroscopy physical processes and detection mechanisms

In the following paragraphs, the main physical processes involved in EXOGAM and NEDA detectors are descriptively explained. This includes firstly a brief introduction to the photon-matter and neutron-matter mechanisms, focusing on the most common phenomena for high-resolution gamma spectroscopy. Afterwards, an overview to the semiconductor-based and scintillation-based detection mechanisms will be presented before starting with the detector structure, detailed in the chapter 3.

2.3.1. Photon-matter interaction mechanisms

The study of the interaction between radiation and matter is a complex field of study. For this reason, in this section we introduce only the main processes which belong to the interest of the gamma spectroscopy.

According to what has been previously mentioned, gamma-ray spectroscopy is based on the detection of the gamma-rays impinging on the detector. Nonetheless, due to the uncharged nature of the gamma-rays, photons do not create ionization or excitation of the medium, making impossible to detect them directly. Instead, the procedure used in the detectors consists of detecting the fast electrons excited by the impinging gamma-rays, which allows subsequently to obtain information about the gamma-ray itself. Three photon-matter mechanisms are among the most important in the field of gamma-ray spectroscopy, which are: photoelectric effect, Compton scattering and pair production. [39].

The photoelectric effect

A photoelectric effect is carried out when a photon interacts with an electron bound to the atomic shell. Hence, the photon is absorbed in the atom and the electron is released with a kinetic energy equal to: $E_{e^-} = h\nu - E_b$, which is the impinging photon energy minus the electron binding energy E_b. After the electron has been released, a slot is left in the atomic shell, which is quickly rearranged. This rearrangement produces the emission of X-rays which can ionize further atoms as well. Since the photon is fully absorbed in a single interaction, the photoelectric effect can be regarded as the ideal process in gamma spectroscopy where the emitted photoelectron contains most of the energy, which can be visualized in the spectra as

[3] *RIB stands for Radioctive Ion Beam*

monoenergetic peak, and then, the remaining energy is carried by the X-rays. Fig. 2.4 shows the physical mechanism and the spectrum obtained.

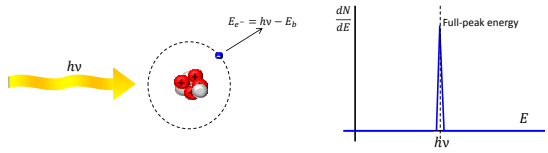


Figure 2.4: Photoelectric effect and histogram

The Compton scattering

The Compton effect, unlike the photoelectric effect, is based on a scattering mechanism instead of absorption. Compton scattering takes place when the photon interacts with a free electron, producing the mentioned scattering. When a photon interacts with the free electron by Compton scattering, the photon and electron are deflected with a certain angle, where part of the photon energy has been delivered to the recoil electron, and the photon retains the rest of the energy. According to the expression 1), the energy of the recoil electron as a function of the scattered angle θ is:

$$E_{e^-} = h\nu - h\nu' = h\nu\left(\frac{(h\nu/m_o c^2)(1-\cos(\theta))}{1+(h\nu/m_o c^2)(1-\cos(\theta))}\right) \qquad 1)$$

Two important cases can be extracted from equation 1). On the one hand, for $\theta \cong 0$, the photon takes away most of the energy, leaving no energy for the recoil electron, and on the other hand, the contrary case when $\theta \cong \pi$, producing the maximum energy transfer between the incoming gamma-ray and the electron. In this case, the recoil electron carries all the energy, making the gamma-ray to be backscattered. In a real detector, all scattered angles from 0 to π may occur, producing a continuous range of emitted energies from the recoil electron. This effect is reflected in the gamma spectrum as a continuum, called Compton Continuum, which spans from low-energies in the spectrum to the maximum called Compton edge, produced for $\theta \cong \pi$. Fig. 2.5 depicts the effect and the Compton continuum in the energy spectrum.

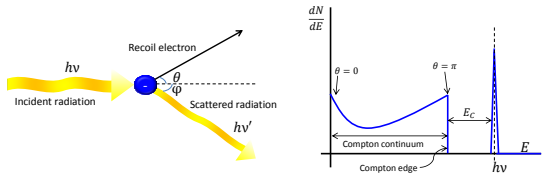


Figure 2.5: Compton effect and histogram

E_c refers to the gap between the gamma ray and the Compton edge. The Compton effect is dominant for gamma-ray energies above 200 keV.

Pair production

The last important process is called pair production and it takes place when a gamma-ray with energy high enough (>1.022 MeV) creates an electron and a positron if there is a nucleus nearby in order to conserve the linear momentum. The positron and electron released will be scattered in 180º and the energy of each will be the half of the photon energy. Since the electron and positron rest energy is 511 keV, the possibility of a pair production can only be feasible if the gamma-ray has an energy higher than 1.022 MeV. The energies of the positron and electron, therefore are:

$$E_{e^-} + E_{e^+} = h\nu - 2m_o c^2 = h\nu - 1.022\ MeV \qquad 2)$$

Once the gamma becomes into an electron-positron pair, the destiny of this process leads to a set of different possibilities. Usually, the positron interacts instantaneously with another electron producing an annihilation into two new gammas. If the resulting gammas after annihilation do not produce further interactions, this will be reflected into a double scape peak on the gamma spectrum, set at 1.022 MeV lower than the total energy peak. On the other hand if only one of this gamma scape, the result produces a single escape peak, 511 keV away from the total energy peak, as it is indicated in Fig. 2.6.

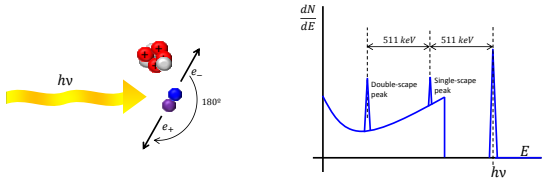


Figure 2.6: Pair production and histogram

Each of the processes mentioned above occur with different probabilities according to the energy of the impinging photon and the material atomic number *Z*. Hence, the photoelectric is predominant at lower energies, mainly X-rays and gamma rays below 200 keV and for materials with high *Z*. Pair production is predominant at higher energies above 7 MeV, also with increasing occurring probability for materials with higher *Z*. Finally, the Compton effect is mostly predominant at medium energies, from few hundred keV to several MeV [5], as shown in Fig. 2.7. A deeper study of these effects can be consulted in [20, 22, 31].

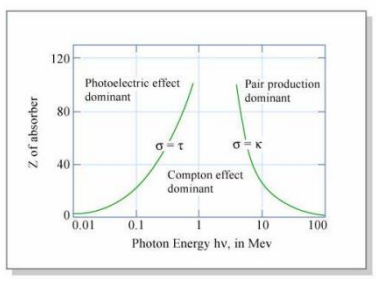


Figure 2.7: Photon-matter interaction effect dominancy plot, in function of Z and photon energy. Ge has Z=32, value which has been used to determine which effect was dominant depending on the gamma-ray energy [21]

2.3.2. Neutron-matter interaction mechanisms

Due to their uncharged nature, neutrons are difficult to detect, being untied to Coulumb processes. Moreover, unlike gamma-rays, neutrons do not interact directly with electrons, instead, the interaction is produced mostly between the neutron and the nuclei, releasing more charged particles, and leading to a wide sort of further nuclear reactions [40].

Depending on the neutron energy, many cases can be contemplated, although mainly two types of interaction can be distinguished, these are: scattering and absorption processes. Firstly we might point out scattering mechanisms, produced mainly in the MeV range [41], where the neutron can carry on energy enough to transfer an appreciable amount of kinetic energy in one collision with a nucleus, and then to undergo a neutron moderation, slowing down and loosing energy in each collision. Among the scattering processes, we might distinguish between elastic scattering *A(n,n)A*, and inelastic scattering *A(n,n')A**[4]. Inelastic scattering implies that the involved nucleus might jump to an excited state after the collision with the neutron. This process takes place when the neutron energy is specially high (> 1 MeV). Afterwards, the nucleus undergoes in an internal rearrangement emitting radiation. On the other hand, in elastic scattering the nucleus does not experience a change to an excited level. In case of neutron detectors, it is preferred the scattering mechanisms with light nuclei, such as hydrogen or helium.

A second type of neutron interaction can take place if the neutron is captured or absorbed by the nucleus instead of scattered, providing a wide assortment of possibilities. The most common ones are the emission of a proton (n,p), deuteron (n,d), alpha particle (n,α), fission products (n,f) after the neutron capture / absorption and the radiative capture reaction (n,γ) of neutrons. Neutrons can be detected indirectly by means of the secondary processes produced by either the emission of gammas or charged particles after a neutron capture / absorption. The cross section for the absorption process is higher for thermal and slow neutrons (~0.025 eV) whereas the scattering processes are more important for fast neutrons (> 1 MeV) [21, 41].

Neutron detection can be achieved by different means depending on the energy range of the neutrons. Some examples to detect slow neutrons are detection in ionized ^{3}He or BF_3 chambers, ^{10}B-aligned gas detectors, and radiative capture in gadolinium foils. In case of detecting fast neutrons, the most widely-known methods are ^{4}He and CH_4 [40], scintillation produced in lithium glass fibers [21], and, as it is the case for NEDA and Neutron Wall, neutron interaction with aromatic organic scintillators [10, 11].

2.3.3. Detectors based on semiconductors

This sub-chapter emphasizes on the description of semiconductor materials, as an introduction to EXOGAM physics detector, based on HPGe. Germanium is an element which belongs to semiconductors, as well as the silicon (Si), two of the most important materials used for semiconductor-based detectors in the field of the nuclear and particle physics.

[4] *This type of notation is commonly used in the field of nuclear physics, representing a straightforward way to describe nuclear reactions. Supposing a generic case, the reaction A(B,C)D, this would mean the interaction of the element B with the nucleus A, producing after the interaction the nucleus D and the particle C. The example used in the reference, A(n,n)A represents the elastic scattering when a neutron interacts with a certain nucleus "A". The notation of A* shown afterwards makes reference to a nucleus in an excited state.*

The P-N Junction

Radiation detection mechanism based on semiconductors is based on the physical phenomenon which occurs when a p-n junction is formed. When a p-n junction is created, either by diffusion or ionic implantation, the semiconductor undergoes an impurity concentration gradient, making the excess of electrons in the n-type to migrate towards the p-type and the other way around in case of holes transported towards the n-type semiconductor. The diffusion charge carriers recombine themselves with their counterparts, producing static charged ions in the crystal lattice. Hence, a charged region called "depletion region" is formed. The depletion region increases until there is an electric charge large enough to repel new charge carriers. In Fig. 2.8, it is depicted the process which summarizes the p-n junction formation.

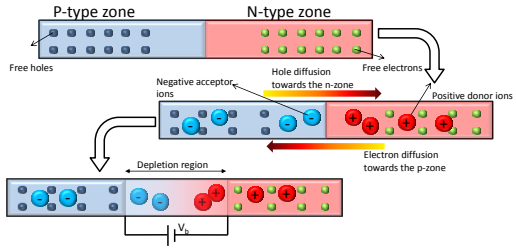


Figure 2.8: Creation of the depletion region in a p-n junction

As a consequence of the accumulated charge in the depletion region, a non-zero local electric field contact potential V_b, which usually lies around 0.7 V for Si and 0.3 V for Ge, is present at the junction. This feature is of special interest for radiation detection, since the particles impinging in the depletion region will be swept by the effect of the local electric field.

Polarizing the P-N junction for radiation detection

In real applications for radiation detection using semiconductors, the contact voltage originated at the depletion region is fairly poor to provide a good efficiency in radiation measurements since the area sensitive to radiation is too small. When a reverse bias is applied to the p-n junction, all the voltage appears at the depletion region, increasing the difference of potential. According to Poisson's equation, the space charge must increase too, extending the volume of the sensitive region. Normally, the reverse voltage applied is big compared to the contact voltage, circumstance which makes the applied voltage to dominate over the intrinsic generated voltage. Fig. 2.9 shows the effect of widening the depleted region by applying a reverse bias to the p-n junction.

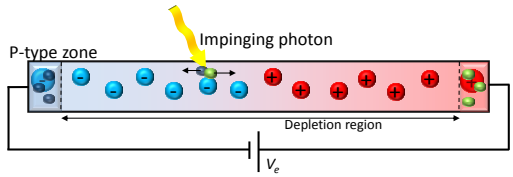


Figure 2.9: Radiation detection mechanism in a reverse-biased semiconductor. The collision of the gamma-ray in the depletion region causes electron-holes pairs which are immediately drifted towards each electrode.

2.3.4. Fast neutron detection with organic scintillators.

NEDA detector is used to provide information about the reaction producing the nucleus being studied. This procedure can be carried out by detecting the fast neutrons using organic scintillators, although these materials are also sensitive to gamma-rays, needing a method to discriminate gammas from neutrons.

Each of the NEDA detectors is based on the scintillation mechanism, a technique used when good timing performance is sought. In the following sections, a brief introduction the light production mechanism in organic scintillators and its conditioning using fast photomultiplier tubes is presented.

Organic scintillator physics

Radiation detection with scintillators is considered one of the most traditional and efficient methods used up to now, not only for gamma spectroscopy, but also to detect fast neutrons. Scintillator materials work on the principle to transform the kinetic energy of the impinging particle into light by means of the material luminescence properties. Usually, scintillators require to be coupled to photomultipliers in order to provide an amplified current pulse from the light produced in the detector. Fig. 2.10 shows the coupling between the scintillator and the photomultiplier.

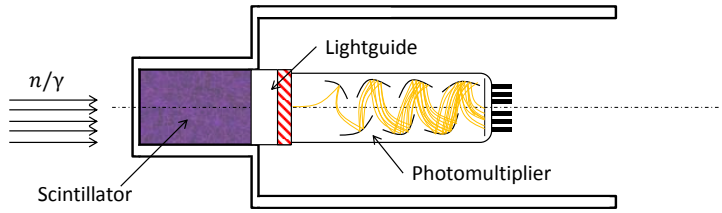


Figure 2.10: Scintillator coupled to a photomultiplier

Among the big assortment of scintillating materials, we might classify them into inorganic crystals, organic liquids and plastics. Although focusing on the materials it is not the scope of this thesis, it should be mentioned the different uses of each type. Inorganic crystals, due to their higher Z elements which the crystal is grown of (CsI(Tl)), NaI(Tl), $LaBr_3$, etc.), are specially suited for gamma spectroscopy. Nevertheless these materials are not the best option for fast neutron detection. For this case, organic liquids are preferred for its higher hydrogen contents and fast response, and, in some cases, such as BC501-A or BC537 [11], also different type of response for different impinging particles, fact which allows to discriminate between them.

Organic liquid scintillators are based on aromatic carbohydrates. The luminescence mechanism is due to the covalent chemical π bonds, formed when the two or more p orbitals from the carbon atom overlap. The result of this overlapping implies the formation of a delocalized π-system, which consists in two symmetric lobes separated by a nodal plane. The case of the benzene is shown in Fig. 2.11 [42].

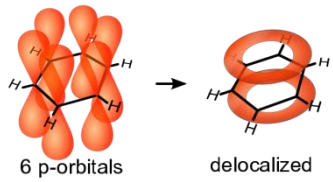


Figure 2.11: Formation of delocalized π-states in aromathic substances [42]

Based on the energy levels of the π-electron, referred to the p-electrons which form the delocalized system, we can study the luminescence from their energy transitions. Therefore, we will refer to the ground state as S_0, the ionization energy as I_π, and $S_1, S_2, S_3 \ldots$ to their respective excited states, called singlet states. Furthermore, the molecules can have lower-state energy levels, called triplets, named as T_1, T_2, T_3, and other vibrational states designed as $S_{01}, S_{02} \ldots, S_{11}$ and $T_{01}, T_{02} \ldots, T_{11}$ associated either to each singlet or triplet state. Given this complex structure, three different types of light emission can be extracted. Fluorescence is the fastest decay mode, given by the transition $S_{10} \rightarrow S_{0x}$, whose decay time is from 1 to 10 ns. Phosphorescence consists in the light emission after an energetic transition to a metastable triplet state, usually T_{10}, providing decays on the order of 100 μs and higher. Finally the last emission mode is called delayed fluorescence, which happens when an energetic transition comes back to a singlet state after passing by a metastable state. Normally this transition is produced by thermal effects and its decay is close to 1 μs. In Fig. 2.12, it is schematized the energy level of a π-electron.

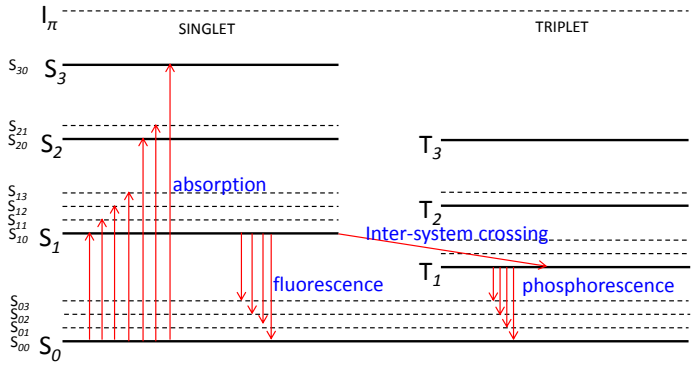


Figure 2.12: Molecular energy levels of the π-electrons, which give path to luminescence effects

The combination of light decay modes produce in some organic scintillators, instead of a simple exponential light output response, a pulse whose shape is a sum of exponential functions with different time constants. Therefore, the time output signal contains two well differentiated components, each attributed to a different type of luminescence emission. The fast component is given by the prompt fluorescence decay time, around a few ns, where the slow decay component comes mainly from the delayed fluorescence, whose decay time lies around the hundreds of nanoseconds.

Neutron-gamma discrimination

Even if the light yield is mostly comes from the fast decay component, the slow component is crucial for pulse shape analysis [22]. The physical foundation which allows to understand how the discrimination is carried out is based on how the energy from the recoiling particles is deposited in the material. In order to study the particle discrimination, we introduce the parameter dE/dx, which denotes the energy deposition rate. In case of gamma rays, as they interact mainly with the surrounding electrons, the interaction produces light recoiled electrons, leading to low dE/dx. The elastic interaction mechanism between neutrons and nucleons within the nucleus produce proton ejectiles that have larger dE/dx compared to electrons. From the point of view of electronics, this distinction between particles can be observed in the pulse tail. While preserving the pulse amplitude, gamma-rays, due to the lower dE/dx, will produce the tail component to fall much faster than the pulse coming from a neutron whose tail component will fall slower due to its larger dE/dx. Afterwards, by means of electronics systems [21, 43], this discrimination is enhanced in order to produce a more thorough discrimination. In Fig. 2.13 [44] it is shown the different time-domain pulses obtained from different exciting particles using a commercial stilbene scintillator.

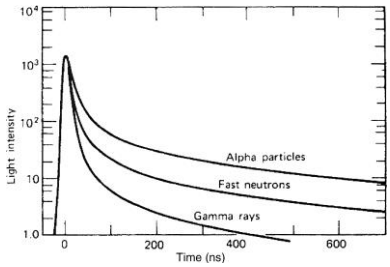


Figure 2.13: Pulse shapes for different particles impinging in the scintillator [45]

2.3.5. Photomultipliers

Photomultipliers (PM) are devices which convert the light into a measurable electric current. Usually radiation detectors based on scintillators are coupled to photomultipliers since they are capable to convert a weak light, around hundreds of photons into a noticeable current adding a minimal amount of noise. Some newer applications make use of the newest progresses in PM, such as the silicon photomultipliers (SiPM) in the field of medical physics for PET (Positron-Emission Tomography), [46] although for our application, that requires large areas, PM tubes remain still mostly used.

The basic elements of any photomultiplier tube are a photocathode, several dynodes, and an anode, set and fixed into a vacuum tube called photomultiplier tube. When the light strikes onto the photocathode, due to the photoelectric effect, the electrons are emitted from the photocathode surface. Those electrons are being drifted alongside of the set of dynodes towards the anode. Hence, in order to achieve such effect, the photocathode is connected to the most negative potential inside the photomultiplier tube, whereas the anode is connected to the most positive potential V_A. Each dynode is connected to increasingly-positive voltages (V_1, V_2, ...V_7), achieving the acceleration effect from photocathode to anode.

When an electron is released from the photocathode, it is attracted by the more-positive electric field of the first dynode, causing the electron to impact on it. The impact of these electrons tears off more electrons from this first dynode, which will be accelerated towards the

second dynode. Likewise, the electrons released from the second dynode will get through all the dynode stages, releasing more and more electrons as the electrons move forward till the last dynode and the anode, where a substantial amount of electrons has already been collected. The ratio between the electrons collected at the anode and the electrons released from the photocathode is known as the photomultiplier gain, which is normally from 10^5-10^6 when using photomultiplier tubes. Fig. 2.14 shows the photomultiplier electron collection mechanism and the different potentials where the dynodes and anode has been connected at. More details about PMTs can be found at [47].

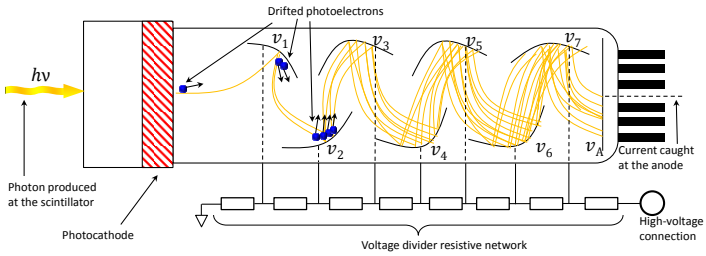


Figure 2.14: Photomultiplier schema and their electron drifting mechanism

Chapter Summary

A brief introduction to the underlying physics of the gamma spectroscopy has been given, focusing on the photon-matter and neutron-matter interaction mechanisms, semiconductors, organic scintillators and photomultiplier tubes, covering the topics for our interest and for further linking between the physical and the specifications which will justify the production of a new electronic acquisition. With all the aforementioned concepts already clarified, the following chapter aims to introduce the EXOGAM2 and NEDA detectors, and the specifications for the FADC Mezzanine.

3. EXOGAM2 and NEDA detectors

This chapter introduces EXOGAM and NEDA detectors and instrumentation, as experimental environment upon the FADC Mezzanines will be part of. In this chapter, the study of the detectors structure, and their electronics will convey us to establish the specifications for the FADC Mezzanine design, presented in the following chapters.

3.1. The EXOGAM2 high-resolution spectrometer

EXOGAM (EXOtic GAMma array spectrometer) is a HP-Ge (High-Purity Germanium) high-resolution gamma-ray spectrometer, which has been using the exotic radioactive beams as well as high intensity stable beams from the SPIRAL (Système de Production d'Ions Radioactifs et d'Accelération en Ligne) accelerator. Currently it is placed at GANIL (Grand Accélérateur National d'Ions Lourds), in Caen, France.

The main characteristic of the high-resolution spectrometers is the high sensitivity which allows the extraction of rare events, corresponding in the gamma spectra to very weak transitions. Both photopeak efficiency, energy resolution and high peak-to-total ratio help he identification of the weak transitions. Therefore, during the design of EXOGAM, the main goal was the optimization of the photo-peak efficiency while preserving the spectral quality, including in experimental conditions that require Doppler correction and using anti-Compton shields. Besides, this high efficiency was sought due to facility startup using ion beams with intensities from 100 to 1000 times lower than in stable beams, where a 20% at 1.3 MeV was at least demanded [48].

The EXOGAM array belongs to the generation of compact high efficiency arrays, built for the early exotic ion beam facilities, in this case SPIRAL, with limited segmentation used only for Doppler correction and with high efficiency at low gamma-ray multiplicity. EXOGAM contributions in the field of nuclear physics using exotic and high-intensity stable ion beams led to a better understanding of the atomic nucleus.

3.1.1. EXOGAM detector structure

EXOGAM is composed of 16 high-purity n-type germanium clover detectors [Clover]. Additionally, each one of the four Ge crystals forming the clover composite detector has segmented outer contacts, as it is shown in Fig. 3.1. This segmentation strategy has been designed in order to reduce the Doppler broadening[5] and the multiple-hits events. An

5 Doppler broadening in gamma-ray spectroscopy causes the peaks in the spectra to broaden, due to an effect caused by distribution of velocities caused by the Doppler effect. The

additional reason which justifies the detector modularity was the future capability of EXOGAM to be coupled with other complementary detectors, such as VAMOS [49], AGATA, NEDA or Neutron Wall.

Each crystal has an inner contact, and four outer lower-resolution contacts, placed at the corners of each crystal to obtain information regarding position. All contacts are provided to a cooled preamplifier based on FETs, although the energy resolution is specified mainly for the inner contacts (< 2.1 keV at 1.33 MeV). Therefore, a clover makes a total amount of 20 acquisition channels (4 inner and 16 outer contacts). Besides, each clover is surrounded on the rear part and sideways by escape BGO (Bismuth-Germanate) / CsI (Cesium Iodine) suppression shields, used to reduce the partially-absorbed gamma-rays recorded in the active detectors, reducing this way the Compton continuum observed on the energy spectra. Fig. 3.1 shows an schematic view of the EXOGAM detector at different levels, i.e. detector, clover and crystal.

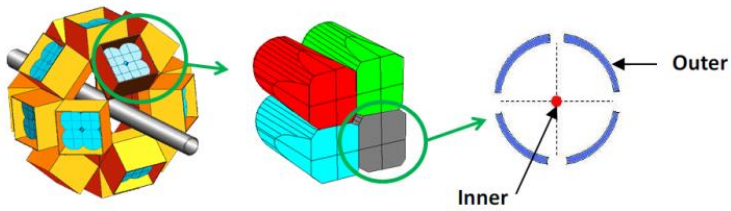


Figure 3.1: EXOGAM High-purity Ge clover structure. Left: EXOGAM detector array. Center: HP-Ge clover. Right: Zoomed segmented crystal. Courtesy of GANIL.

Fig. 3.2 (left) shows a clover cross-section, including the suppression shields and the cold finger, where the germanium clover is depicted in blue. Compton-suppression BGO crystals are plotted in green and yellow, where 4 BGO channels per clover (1 per crystal) are attached. On the rear part, a CsI-based back catcher is added to minimize the events escaping from the large area behind the clover, adding 4 more channels. From the rear side, the nitrogen dewar establishes the crystal operating temperature to 70 K, taking maximum profit of the energy resolution and lowering the noise. Gathering all channels, each clover includes a set of 28 contacts (20 for the HP-Ge channels, 4 BGO and 4 CsI). Additionally, in order to increase the photo-peak efficiency, the EXOGAM clover geometry is arranged placing 8 detectors at 90º to the target and the other 8 at 135º, as it is shown in Fig. 3.2. (right).

main contribution of Doppler broadening is the solid angle of the detectors, especially at 90º where the deterioration is maximum.

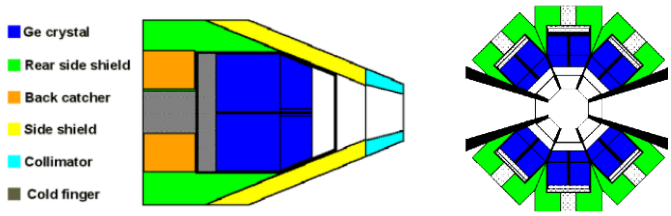


Figure 3.2: Left. Left. HP-Ge clover cross-section of one single EXOGAM detector. Right. Cross-section schematic view of EXOGAM, showing the relative position of the detectors in the array. Courtesy of GANIL

In order to increase the dynamic range without affecting the resolution, the inner channel, which is the one from which the energy information is extracted, is instrumented with a dual acquisition channel. The specifications allow to acquire with a resolution of 2.3 keV at 1.3 MeV, but this resolution is referred to a dynamic range of 6 MeV. Additionally a second channel is added with a total dynamic range of 20 MeV.

3.1.2. EXOGAM2 electronics

EXOGAM2 electronics upgrade comes from the need of a system capable to deal with higher counting rates up to 50 kHz while preserving the energy resolution and avoiding single pileup by moving the former electronic to a fully digital system in order to cope with the new physics program. This new approach will dote the electronics with faster communications and capability to implement more complex and efficient data algorithms to estimate better the energy and the position of the gamma-ray interaction. Fig 3.3 shows the global EXOGAM2 electronics layout, designed by GANIL.

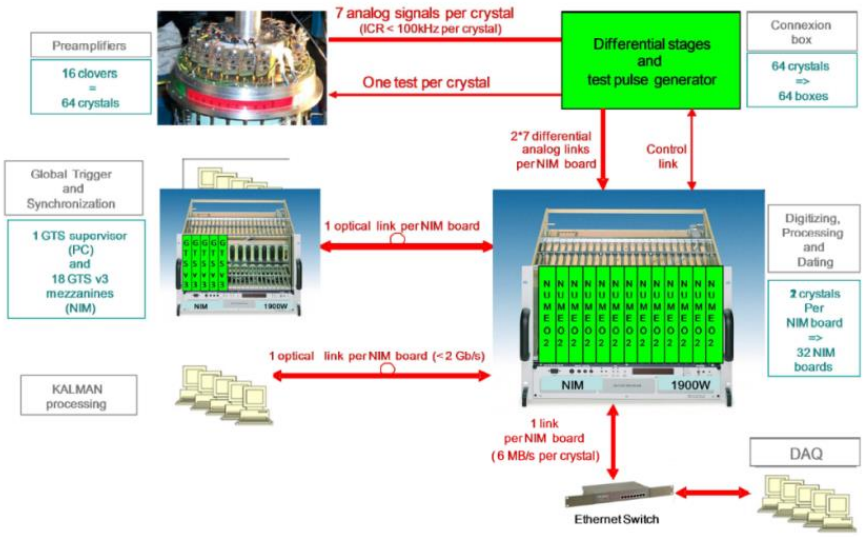


Figure 3.3: EXOGAM2 electronics layout. Courtesy of GANIL

EXOGAM former electronics were mostly based on the EUROGAM and EUROBALL electronics, the readout and the trigger systems built in VXI (VME eXtension for Instrumentation) were the same. The EXOGAM front-end electronics VXI hosted the shaping, timing and ADC electronics for the central and outer contacts as well as for the anti-Compton shield. Nevertheless, due to the big amount of background to be removed by EXOGAM, and given that it uses segmented arrays, more emphasis is put on the add-backs[6] and the energy resolution. More details about EXOGAM previous electronics can be found in [50].

In order to achieve the new required performances, the EXOGAM2 upgrade is envisaged to substitute the old VXI system by a fully-digital sampling electronics with a new digitizer / processing card, called NUMEXO2, that makes use as well of the AGATA GTS (Global Trigger System). In Fig. 3.3, it shown the electronics layout, comprising the charge preamplifiers, digitizers / processing, the GTS, as well as the computer farms (KALMAN and DAQ). KALMAN filtering expected to be hosted in a computer farm to implement gamma-ray spectroscopy algorithms using Kalman filtering [51], although this approach is still under research.

Each quarter of a clover delivers 8 electronic channels (4 outer channels, 1 BGO, 1 CsI and 2 channels for inner contact at 6 MeV and 20 MeV). High-resolution energy measurements are mostly taken from the inner contact, where two ranges are used simultaneously, increasing the dynamic range without compromising the resolution of the low-energy range. However the specification for the outer channels and scintillators are more relaxed in terms of resolution. Summing up, a total amount of channels rises up to 512 channels (320 from HP-Ge and 128 from BGO / CsI).

Charge preamplifiers

When an event occurs in the detector, the ionizing radiation produces an electron-hole pair that move towards the electrodes, producing a certain amount of charge proportional to the photon energy. Normally, detectors based on semiconductors do have a big output capacitance, often fluctuating, which make voltage-sensitive amplifiers to be unsuitable since the collected charge depends on a varying parameter. In this sort of designs, charge-sensitive preamplifiers (CSP) are mostly preferred, since under certain conditions, the collected charge does not depend on the output capacitance [22, 49].

Assuming that $A \gg (C_d + C_f)/C_f$, where A is the preamplifier open-loop gain, and C_f, C_d are the feedback and detector capacitances respectively, the output voltage is thereby dependent mostly on the feedback capacitor, obtaining $V_o \approx -(Q/C_f)$. EXOGAM preamplifiers, as many others do, make use of a resistive feedback mechanism in order to discharge the feedback capacitor, avoiding thus voltage saturation. Given a trade-off between the counting rate of 50 kHz, and the SNR, the decay time is set to 50 μs. Fig. 3.4 shows the basic schema of a charge-sensitive preamplifier.

[6] *An add-back is a technique which consists of summing appropriately the signals from different crystals of the clover. This technique is mainly sought to achieve a substantial efficiency gain and an increase of the peak-to-total ratio, collecting the charge in case that the gamma-ray interacted with different crystals.*

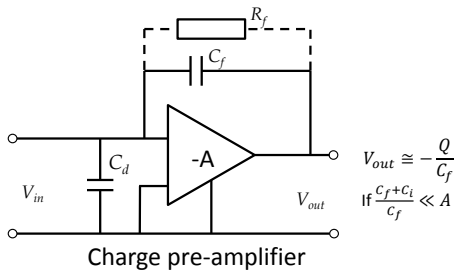


Figure 3.4: Charge preamplifier with resistive feedback generic structure and output equation.

The connection box B3

Placed next to the detectors, on the sideways of the cooling dewars, the connection box B3 takes a double functionality . Firstly, it converts the signals from one crystal to differential, before being sent to the digitizer, placed 10m away. Additionally, pulse generator function based on programmable devices is attached internally to test the preamplifier. Fig. 3.5 shows the B3 connection box block diagram, describing graphically its functionality.

Regarding the input interface, 8 single-ended to differential channels are used, where the signals from the germanium detectors (both inner and outer) are calibrated at 200 mV/MeV. Additionally, signals from BGO and CsI scintillators include an additional charge integrator before the amplifier whose time constant is set to 10 μs. All outputs are driven through 2 HDMI connectors, for later digitalization at the FADC Mezzanines. The test generator works with an ensemble of 16-bit LTC1668 DACs and a MAX II EPM240T100C5N CPLD under SPI commands from NUMEXO2 and a NIM[7] trigger signal to start the waveform. Among other features which might be adjusted, we should mention the rise-time, the output voltage amplitude, polarity, and the possibility to control the trigger rate.

[7] *Normally, fast-logic negative NIM logic levels are defined as current levels, referred to 50 Ω, depending on the NIM sub-standard as well. A common use of the NIM levels establish the high level at 16 mA, obtaining @ 50 Ω, -800 mV. For more information concerning NIM logic, consult [105].*

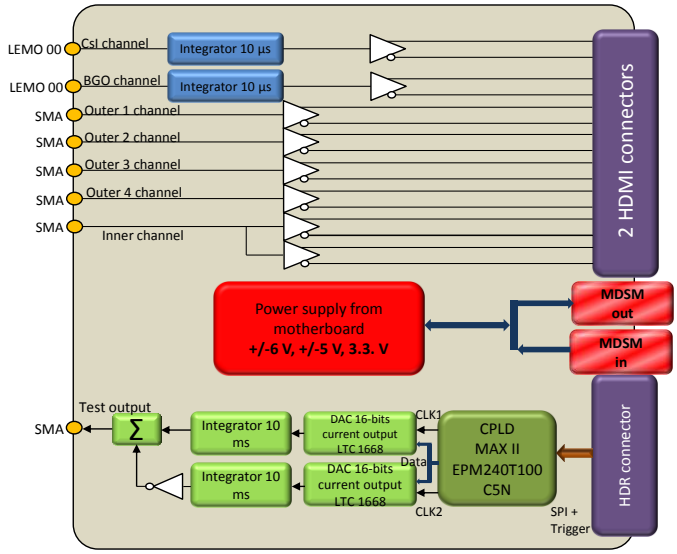


Figure 3.5: B3 Connection box block diagram

The power supply is obtained from the NUMEXO2 digitizer through a MDSM cable, obtaining ±6 V and ±12 V. where several voltages are generated directly at the connection box using DC/DC converters and LDOs. A total amount of 64 connection boxes are required to fulfill the EXOGAM acquisition needs for the 16 clovers.

3.2. The NEDA neutron ancillary detector

NEDA (NEutron Detector Array) is an array of new-generation neutron detectors currently being developed by an international collaboration with 21 institutes of 8 countries. It is foreseen to be the successor of the Neutron Wall [Neutron Wall] detector, which had been used up to now as ancillary neutron detector for gamma-ray spectroscopy experiments, first with EUROBALL in LNL (1998) and IReS (2000-2003), and afterwards coupled to EXOGAM in GANIL after 2005. Most of the experiments required as well the additional use of charge-particle detectors such as DIAMANT or EUCLIDES. NEDA, when completed, is expected to work coupled with present and future generation of detector arrays such as EXOGAM, GALILEO, AGATA or PARIS [52].

3.2.1. Introduction

In nuclear structure experiments, mainly those ones exploring unknown regions of the isotopes chart, information concerning the identification of the reaction channel is required in order to know the reaction products. This can be achieved out by detecting efficiently the emitted charged particles (α,p) and neutrons [53]. A specially interesting case to study in exotic nuclei are the very deficient neutron nuclei, located nearby the N=Z zone in the nuclide Chart. Some of the reactions involved to obtain those exotic nuclei emit multiple neutrons, although with very small cross-sections, reasons for which multiple neutrons become

extremely difficult to detect. Hence, the design of NEDA is envisaged to obtain large neutron efficiencies, coping with the case of neutron multiplicity, where a 6 % has been predicted by the simulations in case of emission 2n [54].

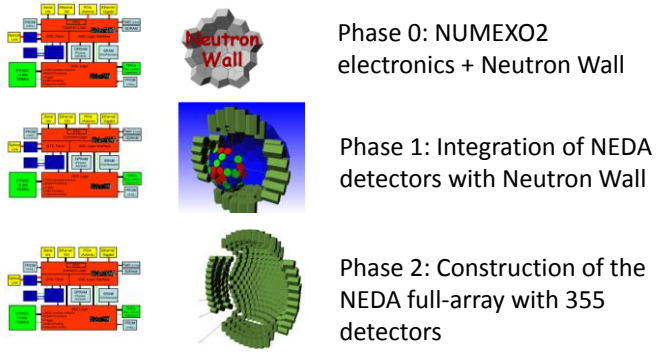


Figure 3.6: Phases of the NEDA project. Courtesy of the NEDA collaboration

The efficiency of neutron collection for multiple neutrons emission in case of Neutron Wall was below 2 % for the case of two neutrons and even much smaller for three neutrons. One of the reasons for such a low efficiency is the ambiguity in the discrimination of such events from the ones produced by neutrons scattering among detectors. This effect is known as crosstalk.

NEDA design has been divided in three stages, detailed as it follows: NEDA stage 0 is meant to be the upgrade of the Neutron Wall electronics, replacing the analog NIM modules by the new digital electronics using NUMEXO2. In this phase the participation of the FADC Mezzanine starts as the most important part on the experiment since all prototypes will be verified during this period. NEDA Phase 1 is dedicated to incorporate 90 detectors combined with the Neutron Wall (45 detectors from Neutron Wall + 45 from NEDA), while the NEDA Phase 2 is expected to use the full 2π array with a total amount of 355 detectors. Finally, a posterior Phase 3 will focus on the research of new materials, light readout systems and the possibility to use highly-segmented neutron arrays progressing towards more efficiency and improved performance. A small schema of the phases has been depicted in Fig. 3.6.

3.2.2. NEDA construction and Phase 0-1 envisaged for 2015

Recent developments focused on the NEDA detector geometry and materials have been carried out obtaining improved performances over the Neutron Wall detector in terms of neutron collection efficiency. Nowadays, the current NEDA status is still focused on the characterization of scintillators and PMTs with the aim to increase the neutron efficiency, timing and neutron-gamma discrimination performances. Two organic liquid scintillating materials have been characterized, the BC501-A and BC537, in parallel with new PMTs such as the XP4512, R4144 and SuperBialkali PMTs [55]. The preliminary results based on simulations [11] have pointed out the BC501-A as the candidate for NEDA as well as it did for the Neutron Wall.

Furthermore, simulations concerning the array geometry analyzed the two scintillating materials over a set of different geometric arrangements, among them, the previously used for Neutron Wall [54]. Fig. 3.7 shows the geometries and neutron efficiency (1n and 2n) obtained for each case. Hence, the best performance was obtained for the fourth case using BC501-A. Even though the seventh configuration obtained a higher efficiency for all cases, the amount of electronics required declined the configuration as less optimal and much more resource-consuming. By using the fourth configuration the total solid angle coverage rises up to 1.88π, with an efficiency of 30.1% to detect 1n and 5% for 2n [10].

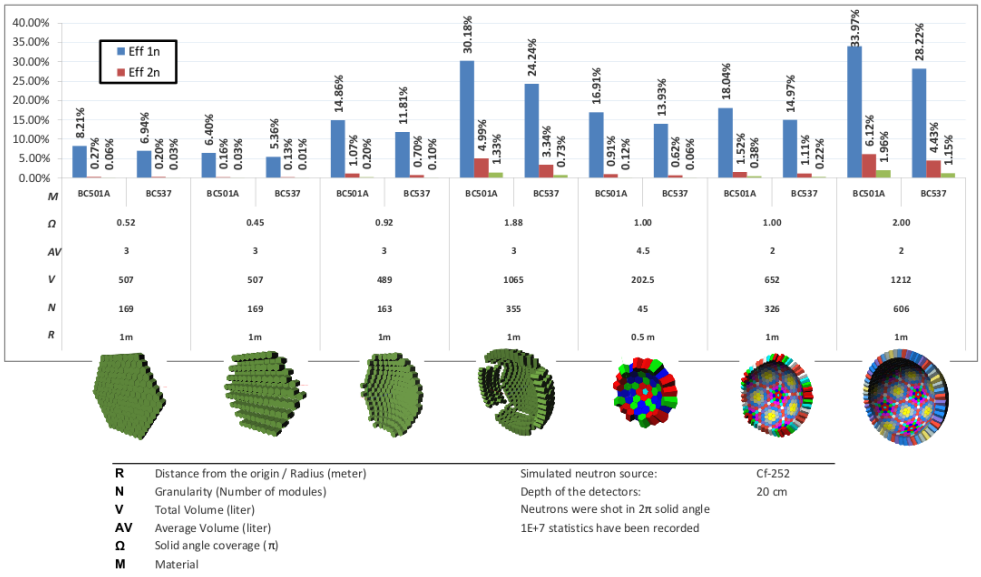


Figure 3.7: Simulations performed to evaluate the neutron collection efficiency (1n, 2n and 3n) for different geometrical arrangements. A ^{252}Cf emulated source was used to perform the simulations. When referred in the text, the first is called to the leftmost part while the seventh is the rightmost configuration. Courtesy of the NEDA collaboration

Focusing on the detector development, each NEDA single cell contains a total amount of 3 liters of BC501-A fitting into a hexagonal shape whose outer dimensions are 146 mm long x 200 mm tall. As the BC501-A is highly reactive to air, each cell is filled with Ar gas before inserting the scintillator, a procedure which is carried analogously to empty the unit. Besides, the cell is provided with an expansion chamber foreseeing the liquid expansion with temperature, a security mechanism to prevent the cell from exploding. The inner part of the chamber containing the BC501-A is covered by a reflecting paint to optimize the light path towards the PMT. Fig. 3.8 shows a model of the whole unit and its cross-section view.

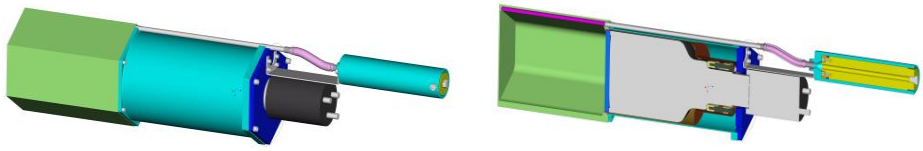


Figure 3.8: Whole and cross-section view of a NEDA single unit cell. Courtesy of the NEDA collaboration

An initial phase involving 45 NEDA detectors is envisaged to be merged in 2015 together with another 45 channels from Neutron Wall, being the NEDA phase 1 experiment. The experiment will serve to be coupled with other gamma-ray spectrometers such as EXOGAM and AGATA as it is illustrated in Fig. 3.9.

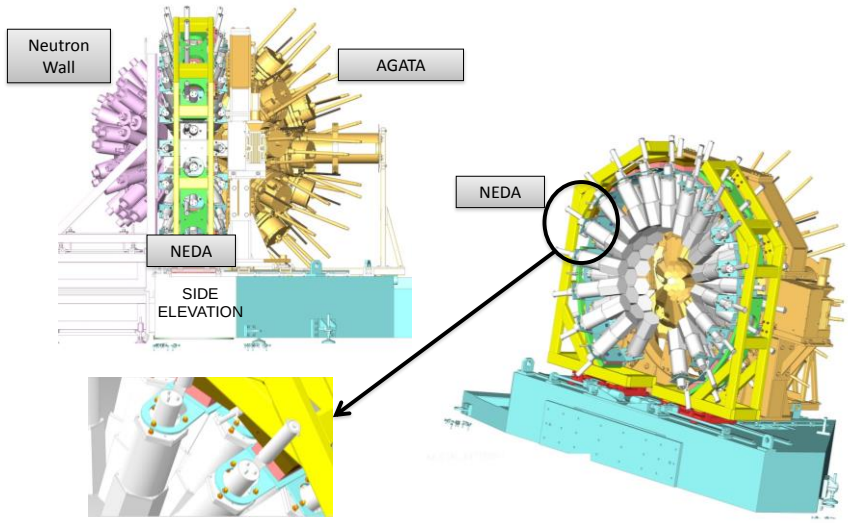


Figure 3.9: Schema of NEDA merged with AGATA and neutron wall. Courtesy of the NEDA collaboration

3.2.3. NEDA electronics

As part of the elements used in NEDA, specially the digitizer NUMEXO2 and the GTS, are used also for other instruments, it was preferred to detail them in section 3.3. Fig. 3.10 depicts the electronics required to process a total amount of 45 channels for the Phase 1.

Each PMT output is connected to a patch panel closely attached to the detector via a short BNC cable. Inside each front-end patch, the signals from 4 PMTs are converted to differential before being sent to the NUMEXO2 digitizers, similarly as it was performed using the B3 board in EXOGAM2. In addition, the PMTs high voltage is supplied from the CAEN modules SY527, placed 20m away from the detectors.

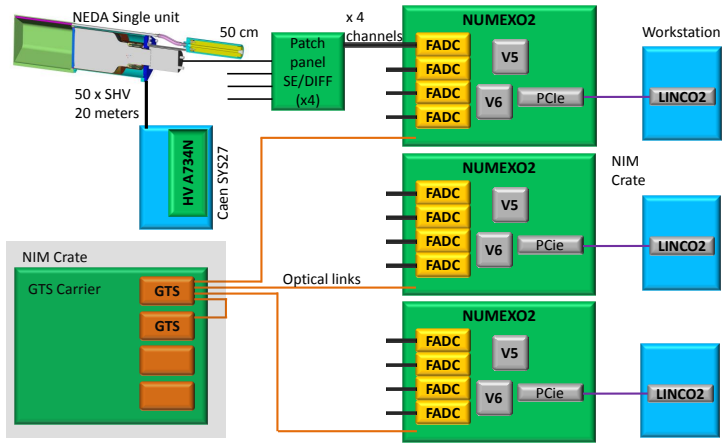


Figure 3.10: General layout of NEDA electronics for the phase 1, involving a total amount of 45 detectors

The arrangement shown for the Phase 1 requires at least 3 NUMEXO2 digitizers capable to cope with the acquisition and pre-processing up to 48 channels. Each Virtex-5 includes a GTS leaf in charge to deliver the trigger requests from the 16 channels placed inside one digitizer to another crate including the trigger processor and the GTS Mezzanines. The system requires only one carrier and 2 GTS Mezzanines for NEDA Phase 1 electronics, one serving as a 3-to-1 Fan-in Fan-out unit and the other as a root module, although the number increases to 5 GTS V3 Mezzanines when using 90 detectors.

Inside the Virtex-6, the sampled pulses are processed in order to reduce the total amount of triggers, using for that purpose a PSA algorithm, providing only a trigger only if a neutron is detected. Then, a package is prepared sending the event info between both FPGAs before sending the data together with the timestamp via the PCIe to a workstation. In the computer farms an enhanced NGD is carried out, performing analysis using bidimensional plots with two variables (TOF, ZCO, charge comparison, energy) and a classification method, normally based on neural networks [56].

3.3. The NUMEXO2 digitizer and the GTS (Global Trigger System)

The following section has been separated from the description of the rest of front-end electronics for EXOGAM2 and NEDA since both the NUMEXO2 [18] digitizer and pre-processing board, and the GTS (Global Trigger System) [57] are common to both detectors. Following the review of the general electronics layout from EXOGAM2 and NEDA, a comprehensive outline is required to understand all blocks from NUMEXO2. Then, in the next section 3.4 after all NUMEXO2 blocks are commented, the main specifications to design the FADC Mezzanine board, based on the physical experimental constraints, will be individuated and detailed. Furthermore, a section is left to comment the functionality and importance of

the GTS in the context of the experimental environment, since it will be used, not only for EXOGAM2 and NEDA, but also in other detectors such as AGATA[8], TRACE, etc.

3.3.1. Description and block diagram of the NUMEXO2 digitizer

NUMEXO2 is one of the most important elements in the EXOGAM2 and NEDA electronics; it plays the role of digitizing and pre-processing for the two detectors, even if their aim regarding the detected radiation and the methodology are very different. Nevertheless, the NUMEXO2 functionalities can be summarized in: A/D conversion, data pre-processing connection with the GTS system and communication link management for 16 channels. NUMEXO2 is composed of a motherboard - which has been developed by the GAP (Group d'Acquisition pour la Physique) from GANIL (Grand Accélérateur National d'Ions Lourds), in Caen, France - and the set of 4 FADC Mezzanines in charge to perform the A/D conversion for 4 channels. Since the FADC Mezzanine is the main object of this PhD thesis, chapters 4, 5 and 7 analyze in detail the design, test and results of the daughterboard, while the description of the motherboard is carried on the following paragraphs.

NUMEXO2 owes its flexibility to the use of digital electronics with programmable logic devices. The consequences of this are crucial since even though the hardware basis is common, the inclusion of last-generation high-performance programmable devices provide NUMEXO2 the flexibility to implement different digital signal processing algorithms. In particular, NUMEXO2 comprises 2 high-performance FPGAs (Field-Programmable Gate Arrays), a Virtex-6 and a Virtex-5 from Xilinx. Fig. 3.11 illustrates the main NUMEXO2 block diagram, including the FPGAs, FADC Mezzanine and communication links.

NUMEXO2 is designed to be held into the NIM standard crate, from which the power supply is delivered to the rest of electronics within the digitizer, including the FADC Mezzanines. The average power consumption per digitizer running at 200 MHz sampling frequency and with both FPGAs with the firmware downloaded is expected not to be higher than 100 W.

[8] *The GTS was initially proposed to be used for AGATA, and then it was inherited for the use with EXOGAM2, NEDA and other detectors.*

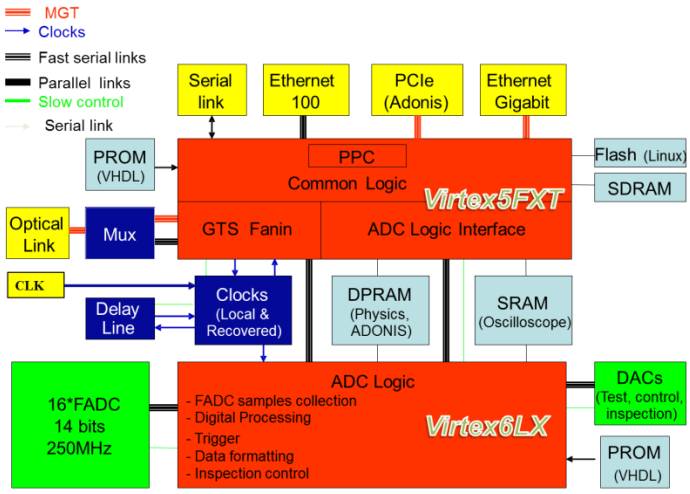


Figure 3.11: NUMEXO2 general block diagram. Courtesy of GANIL.

3.3.2. NUMEXO2: Virtex-6 block. Data collection, digital signal processing and data readout

The Virtex-6, concretely the model V6-LX130T, is the largest logical device in NUMEXO2 and carries out most of the pre-processing tasks such as deserialization, digital signal processing, configuration and oscilloscope. Fig. 3.12 schematizes all these functionalities into a block diagram.

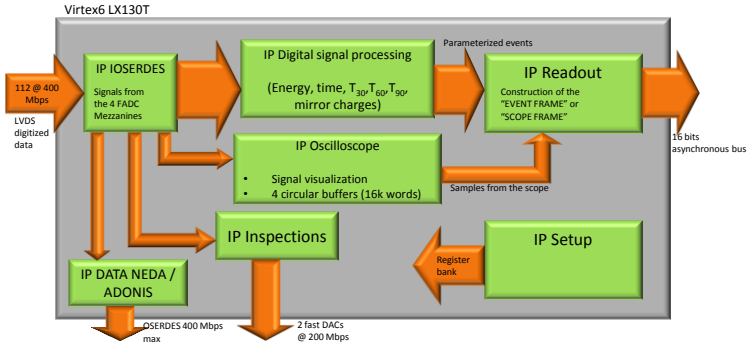


Figure 3.12: NUMEXO2 Virtex-6 block diagram. Courtesy of GANIL

FADC data collection (ISERDES) IP

This block collects raw data from the 4 FADC Mezzanines at 200 MHz sampling frequency, distributed throughout 7 differential pairs per channel and redistributes it to the rest of the FPGA as samples to be processed by standard algorithms after the deserialization process. The deserialization consists of converting the odd / even input multiplexed bits into raw samples, using the input logic ISERDES to achieve the goal. Since the total number of channels per

digitizer is 16 channels at 400 Mbps, the total amount of pins rises up to making use of a total amount of 240 pins – each FADC chip contains an output differential clock and 7 differential pairs/channel readout, making use of 30 pins per chip - being the block which employs most of the I/O and ISERDES (Input Serialization-deserialization) FPGA resources. As a curiosity, the data rate for each channel is 2.8 Gbps, and 44.8 Gbps if we treat the numbers at the digitizer level.

Digital signal processing IP

This is the block which mainly differs between EXOGAM2 and NEDA, where separated signal processing techniques are required. In case of EXOGAM2, the digital signal processing (DSP) extracts the energy and timing information hardware-wise, providing hence, a substantial data reduction, since only the aforementioned information are sent instead of the full sampled raw data. This block includes:

- Energy calculations make use of several blocks. Firstly, a MWD (Moving Window De-convolution) performs a trapezoidal filtering over the original digitized pulse. Afterwards, the energy is computed as the height between an average of the top and pre-trigger baseline samples. Finally, a histogram builder arranges the energy calculations in a spectra form, useful for test purposes, although not complete due to the lack of time relation between the signals.
- A digital CFD (Constant Fraction Discriminator) that provides a trigger to the Virtex 5. CFDs are implemented on the inner channels only.
- Hardware structures for timing measurements based on interpolations and micro-delays in order to achieve timing resolutions below the clock period. In case of EXOGAM, at least 1 ns is needed. Other timing measurements conform those computed over the rise-time, where the time after the signal crosses the 30%, 60% and 90% threshold are also needed.
- Algorithm to distinguish mirror charges based on thresholds applied to the Outer HP-Ge channels.

On the other hand, NEDA pre-processing is mainly devoted to provide a trigger request to the GTS, after performing a NGD algorithm so that GTS only receives a trigger request after a neutron was detected. However, the goal of the NGD algorithm at this level, is to provide a first-level discrimination, in order to reduce the triggers produced by gamma-rays. Afterwards, a more exhaustive processing, carried out at the workstations, performs the discrimination more accurately. As well as in EXOGAM electronics a digital CFD is used to start the execution of algorithms before the real trigger request is sent to the GTS. Unlike the case for EXOGAM, for NEDA requires cubic interpolation to obtain resolutions close to 1 ns. However, most of digital signal processing to obtain the bidimensional[9] plots is carried out via software due to the big complexity it would entail to perform the tasks online.

Oscilloscope IP

This block is used to observe and display the signals at different points inside the FPGA, such as the raw-data from the FADC, data after trapezoidal filtering, among others. It comprises a set of four 32-kBytes circular buffers, allowing the monitoring of data at a

[9] *Bidimensional NGD plots are used in NEDA to estimate more precisely the type of particle impinging the detector. They make use of two variables such as the TOF and PSA parameters arranged as a histogram. In section 3.4, more details are provided.*

maximum sampling rate of 200 MHz and a maximum rate of 40 Hz. Among other functionalities, it allows to adjust the time base from 5 ns to 81.92 μs as well as the type of input trigger input applied.

Data readout IPs

This block carries out the data transmission from the Virtex-6 to the Virtex-5. It includes two types of communication protocols depending on the detector used, wrapping all data and adjusting the frame within a certain format. The blocks are called readout IP and the NEDA/ADONIS IP.

The readout IP establishes a different frame format for data coming from EXOGAM detector. Two different modes can be selected: parameterized data based on the EXOGAM DSP block calculations, which include the energy value and timing measurements, and the oscilloscope mode, which sends the information from the oscilloscope block. While the parametric mode of communications is mainly used on the experimental environment providing a drastic data reduction, the oscilloscope mode plays a major role during the development and test phase.

On the one hand, ADONIS / NEDA IP are blocks physically separated from the readout IP, using other lanes and working as a synchronous fast link with the deserialized samples from the IOSERDES block. On the other hand, if it is working on ADONIS[10] (EXOGAM) mode, 1 over 4 samples from both inner channels are sent to the Virtex-5. On the other hand, for NEDA mode, only a set of 250 raw-data samples is wrapped and sent to the Virtex-5 using the fast link.

Inspection lines IP

The IP consist of a set of multiplexers which allow to select internal signals at different points of the Virtex-6 and to drive them out of the FPGA so that they can be measured using an oscilloscope, enhancing the test capabilities of NUMEXO2. The signal selection depends on the value set in certain registers of the Setup IP, which can be accessed using the software interface GECO (Ganil Electronic COntrol). At the front panel, 2 analog and 2 digital signals can be accessed using LEMO connectors. Two external fast digital-to-analog (DACs), allow the visualization of analog signals. Among the analog signals which can be selected, we find the raw-data input, the output of the trapezoidal filter and the analog-wise conversion of the formatted frame which is sent to the V5. Regarding the digital lines, the options lay among the several clock sources and trigger signals from the digital CFD. Other internal control lines can be selected as well.

Setup IP

This block contains a set of registers used to configure the rest of the blocks within the Virtex-6, aiming to provide a flexible, dynamic and easy-to-configure device. Registers can be read and written using the software tool GECO, working under the TCP/IP protocol via the Virtex-5. Some of the parameters the setup block takes in charge with are the IODELAY step value, the trapezoidal filter parameters, the timescale for the oscilloscope mode and the

[10] *ADONIS is a type of protocol used in EXOGAM to analyze raw data.*

possibility to either choose parametric or oscilloscope mode in case of using EXOGAM2 electronics via the slow link.

3.3.3. NUMEXO2: Virtex-5 block. GTS leaf and communications management

A second programmable device on NUMEXO2 is the device Virtex5FX70T, which manages the data reception with from the Virtex-6 after the processing. It manages the communication ports and includes the GTS leaf, linking NUMEXO2 with the GTS. Fig. 3.13 illustrates the internal blocks inside Virtex-5 which can be described as:

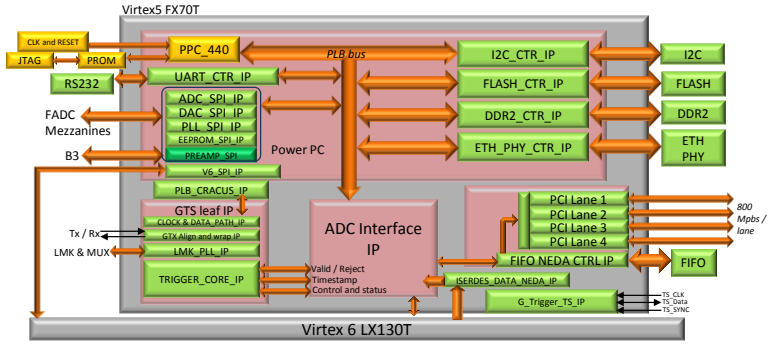


Figure 3.13: NUMEXO2 Virtex-5 internal block diagram. Courtesy of GANIL

ADC Interface

The ADC interface block carries out multiple functionalities as the data receiver from Virtex-6. Firstly, it collects and unpacks the data frame from Virtex-6 putting it into a buffer and waits for the event data to be validated / rejected by the GTS leaf. Also, at this level, if the event was validated from the GTS, the leaf attaches the timestamp received, where the ADC interface takes the data bundled with the timestamp either to the PPC in case of EXOGAM2 and the preliminary phases of NEDA, or the PCIe if using NEDA experiments.

PowerPC (PPC) and its peripherals

Virtex-5 includes a hardware PowerPC (PPC) 440 processor with and embedded Linux OS, facilitating to cope with the complexity of the TCP/IP protocol. The processor carries in itself a good part of tasks among which we can find the configuration of the rest of blocks inside the Virtex-5, such as the Ethernet Gigabit management, configuration of the PCIe setup registers, the GTS leaf setup (performed through the PLB Cracus IP), interaction with the Virtex-6 setup, FADC Mezzanine SPI registers, B3 registers, as well as the management of external Flash (256 Mb) and DDR (1 Gb) memories and a serial port which allows to monitor the status of the Linux OS booting. Although Virtex-5 can be clock from many sources as we detail in the GTS leaf, the PPC is the only device in the whole NUMEXO2 which must be clocked always from a local clock.

GTS leaf

Inherited from AGATA, the GTS system aims to provide synchronization in digital multichannel systems and event validation/rejection. Next section provides a more global overview regarding the GTS functionality. The GTS system is structured as a tree, where the GTS leaf is hierarchically emplaced at its bottommost part, and it is in charge to receive and pack the trigger requests provided from the Virtex-6 to the rest of the GTS (tree and trigger processor), placed outside NUMEXO2. Each NUMEXO2 contains one GTS leaf, connected optically to GTS crate and it is capable to manage up to 16 channels.

The configuration of the leaf is performed using the PLB Cracus IP, a register bank. Other functionality of the leaf is the optical transceiver control, a clock multiplexer which allows the selection between several input clock sources (local oscillator, recovered clock from the optical links and external source clock), providing it to a PLL. Besides, it includes a data path block, aiming to equalize the phase and control the data direction (TX or RX), and, finally, a trigger core, used to receive the trigger requests from Virtex-6 and start the GTS cycle. Finally, at the leaf level, the timestamp is generated and attached to the validated / rejected event. It consists of a 48-bit counter, with a resolution of 10ns.

PCI express IP

NUMEXO2 includes as well an optical link containing 4 PCIe Endpoint lanes, capable to run up to 3.2 Gbps (800 Mbps each), fulfilling NEDA specifications in terms of data throughput. In the middle of the PCIe driver there is a FIFO used to buffer the data between the ADC interface and the driver itself.

3.3.4. The Global Trigger System (GTS)

An upgrade towards a full-digital system requires the implementation of a system capable to synchronize all channels by delivering a common clock through the optical links, sort and accept/reject events. This revolutionary idea, inherited from AGATA, is being implemented for the EXOGAM and NEDA electronics. One of the most interesting features it provides is the possibility to use it between different detectors, making possible different combinations of detector coupling.

GTS is based on a tree topology, and it contains three different types of firmware depending on the hierarchical position in the tree: on one side, the aforementioned GTS leaves, at the bottom of the tree, which are in charge of generating the local trigger to the trigger processor, are placed inside the Virtex-5 in NUMEXO2. Out of the digitizer, we find the Fan-in Fan-out and the Root units which are hosted in an additional NIM crate reserved for the GTS. The latter two firmwares (ROOT and FIFO) can be downloaded into V3 Mezzanines. Their functionality is to gather the trigger requests from several leaves / FIFO units until the root module, which provides a single optical link to the trigger processor. Additionally, the root module is capable to distribute the clock to all digitizers, synchronizing all modules. Each V3 Mezzanine has 1 upstream and 3 downstream optical links, where each upstream link from either the GTS leaf or a Fan-in Fan-out is connected to a downstream link from the GTS upper level. Finally, all nodes converge at the root node whose upstream link is connected to the trigger processor. The trigger processor is the element in the top of the GTS and it is in charge to cope with the event validation and rejection. For EXOGAM2, using 32 NUMEXO2 boards to sample the channels corresponding to 16 clover detectors. Therefore, the GTS tree requires a total amount of 18 V3 Mezzanine units, 17 of them used as 3-to-1 Fan-in Fan-out units one

as a root module. On the other hand, NEDA Phase 1 with 45 channels only requires making use of 2 V3 Mezzanines (1 Fan-in Fan-out and 1 root node) since only 3 NUMEXO2 boards would be used. The tree schema is shown in Fig. 3.14.

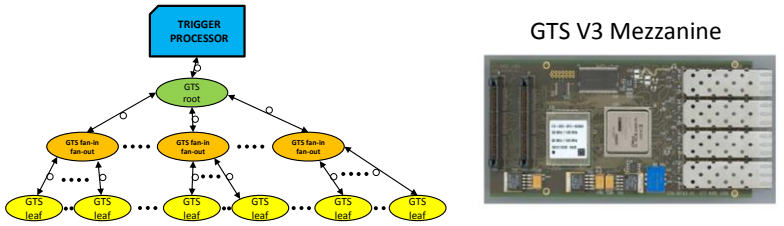


Figure 3.14: Left. GTS tree hierarchical topology. Right: Picture of the GTS V3 Mezzanine, placed in the NIM GTS crate. Courtesy of the AGATA collaboration

3.4. EXOGAM2 / NEDA synergy and specifications for a common FADC Mezzanine design

This section aims to analyze the features and common points between the EXOGAM2 and NEDA, which would lead to a common digitizer design. Concretely, we have focused mostly on the specifications which give place to proceed for the design of the FADC Mezzanine, omitting details concerning the rest of elements from NUMEXO2 such as the communications link capability, type of FPGA selected, etc. Summarizing the information from section 3.1 and 3.2 regarding the detector structure and electronics, the design leads to a set of trade-offs given the different detector the mezzanine is expected to work with. On one hand, EXOGAM2 electronics is devoted to increase the system counting rate capabilities without degrading the energy resolution and peak-to-total ratio. On the other hand, NEDA is meant to maximize the NGD performance by means of pulse-shape analysis in a broad energy range.

Among the specifications which need to be analyzed in order to establish common points for the digitizer design, specially we focus on the parameters of major concern for the analog-to-digital conversion and how this process degrades the measurements in the nuclear physics environment. Among these parameters, special attention has been put on the energy resolution, NGD (Neutron-Gamma Discrimination) performance, dynamic range and their relationship to ENOB, sampling frequency and rise-time.

3.4.1. Analysis of the physical specifications and relation to the electronics

Often, the relationship between physical parameters and the associated electronics is not an obvious task. Some examples are the required sampling frequency or number of bits given the energy resolution specified for an energy and dynamic range or the merit figure in terms of NGD to achieve a certain performance. Most of these parameters are derived after a simulation and are not straightforward to be obtained analytically.

Energy resolution and effective number of bits

HP-Ge are nowadays the radiation detector with one of the best energy resolution in gamma-ray spectroscopy applied to the nuclear structure research[11]. On the energy spectrum, as we noticed in Fig. 2.3, high resolution can be considered as a very narrow peak. Quantitatively, the resolution is commonly expressed in terms of its FWHM (Full-Width Half Maximum) [21], measuring the width of the peak at half its maximum. Any additive noise source will degrade this performance. Considering the noise sources both from the detector and from the electronics, in case of HP-Ge, the major contribution should come from the crystal. Hence, the electronics should not to degrade the crystal resolution, and this can be achieved by adding minimal amount of noise compared to the detector. Fig. 3.15 shows the concept of FWHM in a gamma spectrum.

Normally in electronics, and specially in A/D converters design, the energy resolution can be translated in terms of effective number of bits (ENOB). This term is directly linked to the SNR and takes into account not only the quantization noise, but also all thermal, jitter and other noise sources. An important fact is the procedure to calculate the ENOB depending on the input signal used. For instance, the intrinsic noise is calculated after fitting to a Gaussian curve the noise measured, but, the ENOB is calculated with a sine input and using methods based on FFT [58]. In gamma spectroscopy, the resolution is set over the energy spectrum after applying to a pulse a MWD [59] shaper (Moving Window Deconvolution) to obtain the energy after shaping. Hence, from the spectrum, the SNR and ENOB are derived.

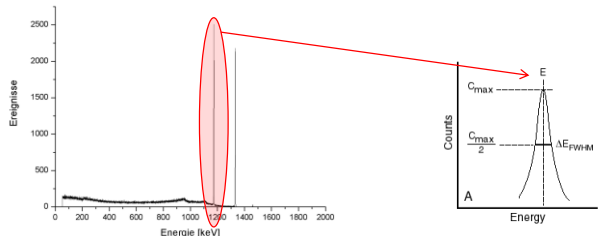


Figure 3.15: Energy resolution for a HP-Ge detector [21]

The specification of the energy resolution for EXOGAM2 electronics is inherited from the specifications of the old electronics. The goal is to preserve the energy resolution using digital electronics, while increasing the system capability in terms of flexibility, integration and data rates. The specification established a FWHM of 2.3 keV @ 1.33 MeV for the whole electronics chain including the detector, B3 card, FADC Mezzanines and the trapezoidal filter performed digitally afterwards. The SNR (Signal to noise ratio), for the given specification can be calculated as:

$$SNR = 20\log_{10}\left(\frac{E_0}{\sigma}\right) = 20\log_{10}\left(2.35\frac{E_0}{FWHM}\right) \qquad 3)$$

where E_0 is the energy at which the energy resolution has been specified. A common procedure is the energy using ^{60}Co, a common isotope which has peaks at 1.17 and 1.33 MeV,

[11] *The crystal diffractometers for gamma-rays have higher energy resolution, but they can only be used in particular conditions. They have extremely low efficiency and require a very clean production.*

although energies are referenced to the second peak. For E_0=1.33 MeV and $FWHM$ = 2.3 keV, a SNR of 62.66 dB is obtained. The relationship between FWHM and σ can be calculated as 4) if the peak is Gaussian.

$$FWHM = 2.35\,\sigma \qquad 4)$$

Based on the SNR, the effective number of bits can be calculated as follows based on the generic formula:

$$ENOB = \frac{SNR\ (dB) - 1.76}{6.02} \qquad 5)$$

From 5), a value of 10.11 ENOB [60] is obtained for the whole electronic chain together with the detector. It was foreseen that each electronic device placed straightaway before the trapezoidal filter (B3 + FADC Mezzanine) should not add more than 1 keV each to degrade the signal, letting 1.81 keV for the detector itself. Assuming for the FADC range a maximal noise contribution of 1 keV established for the same energy, an ENOB = 11.32 is obtained using 3), 4) and 5).

Dynamic range

The dynamic range of measurement is tightly connected to the energy resolution. Large dynamic ranges introduce problems to detect small energies, since they are at the level of the noise, and on the other hand, smaller ranges provide better resolution for the same A/D converters but reduce the information obtained from the energy spectra by cutting the higher energies. In EXOGAM2, the inner contact is used to calculate optimally the energy and providing a trigger while the outer channels are left to estimate the position of the interaction. Therefore, the strategy used to enhance the resolution consists of using for the inner channel two different energy ranges, 6 and 20 MeV. The energy range can be changed at the level of the sampling board by adding properly a voltage divider so that the gain is reduced.

In case of NEDA the physics cases foresee the study of neutrons with deposited up to 8 MeVee. Maximally, it is desired to have 2000 energy channels, which in terms of energy refer to 4 keVee, and thus can be expressed in ENOB as 11 bits.

Neutron-gamma discrimination performance

Calculating what is the required ENOB and sampling frequency in order to obtain certain NGD is not a straightforward task and requires simulations in order to estimate the parameters. NGD performance is linked to the timing resolution used to measure the TOF and PSA-based techniques such as the Charge comparison and the ZCO method. A good NGD can be achieved by applying a classification rule among a 2-dimensional plot containing in one axis the TOF while the other independent axis is left for another discrimination technique such as the ZCO or charge-comparison methods An example of NGD using bidimensional charts is depicted in Fig. 3.16, where the Y axis represents the TOF and the X axis is used for the ZCO.

The timing resolution required to measure the TOF is directly connected to the detector size and the distance from the source. For NEDA detectors around 1-1.5 ns is expected to be obtained by the detector itself without any other jitter-degrading source. Unlike in analog electronics, where remarkable timing resolutions could be achieved using BaF_2 scintillators as a reference, in digital systems it turns out that the number of samples on the rising time is determining to achieve good timing resolutions. Nevertheless, even though the timing

performance is strongly dependent on the sampling frequency, the type of interpolating algorithm used directly on the samples might be decisive to achieve the goal.

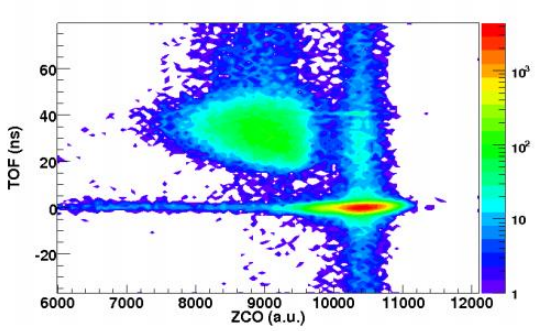


Figure 3.16: Example of bi-dimensional NGD graph, arranging together TOF and zero-crossover (ZCO) measurements [22].

The experiments carried out at LNL, show which is the timing resolution when using different fitting algorithms at different sampling frequencies and ADC resolutions, comparing the results to a Strück digitizing module working at 500 MHz and 12-bit resolution [61]. If a down-sampling to 200 MHz algorithm is applied and the implementation of fitting and interpolation algorithms is carried out, it turns out that 200 MHz is suitable for NEDA in terms of timing resolution. However, going below 200 Msps degrades dramatically the timing resolution, being hence 200 Msps the minimal sampling frequency to perform timing measurements. Regarding the ADC resolution, it influences in a minor way provided the number of bits does not decrease dramatically [62].

NGD performance is quantified by means of figures of merit (FOM) applied to the ZCO, charge-comparison or TOF spectra. Using this type of detectors, gamma rays and neutrons arise in two peaks, over which the FOM can be calculated. Hence, the figure of merit M described as 6).

$$M = \frac{|X_\gamma - X_n|}{W_\gamma + W_n} \qquad 6)$$

where X_γ and X_n are positions of the gamma and neutron peaks and W_γ, W_n are their respective FWHMs. A second gamma-neutron discrimination parameter defined as R aims to provide the number of the collected neutrons compared to the background events. R is defined in 7) as:

$$R = \frac{N_b}{N_n - N_b} \qquad 7)$$

where N_b are the background events and N_n are the real neutron events. A small value of R indicates a good discrimination of real neutron events from any other events.

In [63], the performance of different digital neutron-gamma discrimination algorithms is presented, expressed in terms of the figures of merit M and R versus energy aforementioned figures of merit 6) and 7). In this paper it is compared both the algorithm performances in terms of figure of merit M, which are depicted in Fig 3.17, and also the performance that it can be achieved if using a digital system given a sampling rate and a certain resolution (Fig. 3.18). Regarding the resolution required, most of the algorithms do not undergo an improvement

when using resolutions larger than 10 bits in most of the cases as it can be seen in Fig. 3.18. Analogously, the same reasoning can be applied to the sampling frequency, observing that the FOM does not experience an improvement in most of the cases after 100 Msps. The results obtained from several algorithms, depicted in Fig. 3.17, and the detail analysis can be found as well in [63].

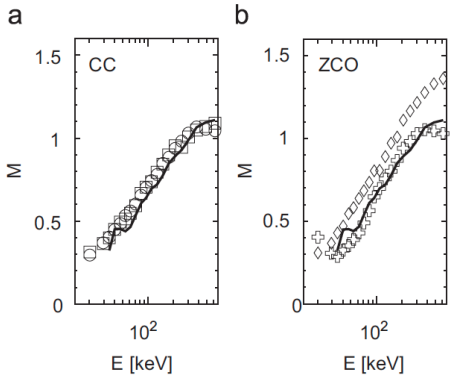


Figure 3.17: Performance comparison between different neutron-gamma discrimination algorithms. The performance is shown for the figure of merit M and R comparing types of charge-comparison (CC) and zero cross-over (ZCO) algorithms. Convolution (crosses), integrated rise time (diamonds), slow component (circles) and GDM integral (squares), together with the analogue pulse-shape discrimination (solid line). Courtesy of [63].

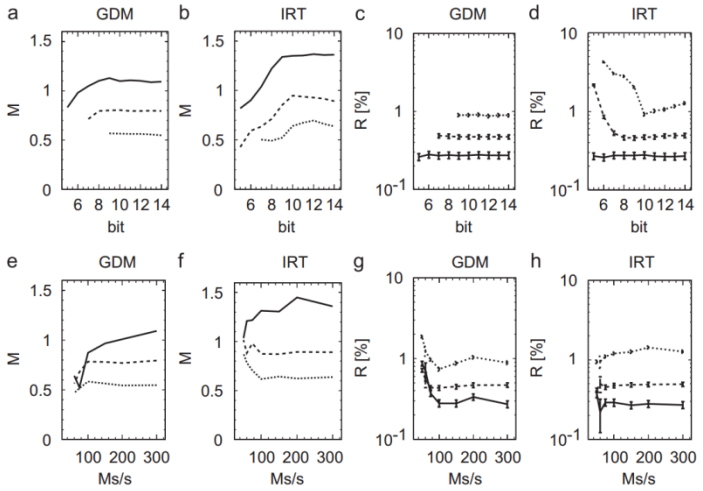


Figure 3.18: Performance comparison of several neutron-gamma discrimination algorithms, for several sampling frequencies and number of bits of the ADC. The performance is shown for both figures of merit M and R comparing the charge-comparison based GDM and the ZCO-based algorithm IRT. Courtesy of [63].

Bandwidth and signal rise-time

In nuclear physics, the fastest part of the signal is normally the rise-time. The study of the signal rise-time is directly related to the bandwidth required to transmit the pulse with minimum shape degradation. Even though the famous relationship between bandwidth and rise is given by the expression 8), described as:

$$BW \approx \frac{0.35}{t_r} \qquad 8)$$

In HP-Ge detectors, as well as in any semiconductor detector, also in gas chambers, the collection time of the electron-hole pair depends on the position where the gamma-ray impinged creating the pair. Also, the signal rise time is caused merely by the induction caused by the charge movements when reaching the electrode [23]. In the case of EXOGAM, given the material and the detectors size, the collected signals involve rise-times between 100-200 ns On the other hand NEDA signals depend on the scintillating material and the PMT tube, usually leading to much faster rise-times from 1.5 ns to 15 ns [47]. For the case of BC501-A-based scintillators using the PMT XP4512PA, is close to 6.5-7 ns. However, for the case of NEDA, part of the front-end electronics and the 10-m cable between NUMEXO2 and the detector widen slightly the rising-time reaching values close to 10 ns.

Substituting the rise-time values obtained both for EXOGAM2 and NEDA signals, a bandwidth result of 3.5 MHz and 35 MHz are obtained respectively according to the expression 8). However, in practice, if some of the pulse attributes such as the shape or the peak amplitude are needed to be preserved, higher bandwidths can be selected at the expense of a slightly noisier contribution. In case of EXOGAM pulses, after being processed by the charge preamplifier, a total bandwidth of 30 MHz is selected, incurring close to a factor 10 over the results obtained from 8). The total bandwidth majorly affects the rise-time and the resolution to measure the TOF, reason for which a total BW of 100 MHz was chosen.

3.4.2. Conclusions from the specifications

Based on the specifications which provide a link between the physical specification world and the real parameters which take part in a digitizer design, this paragraph gathers the content of the previous section. This allows proceeding straightforward to the choice of the main electronic devices, part which is fully described in the chapter 4.

Summarizing the constraints obtained in terms of resolution, for EXOGAM a minimum amount of 11.3 ENOB is needed not to lose energy resolution, while for NEDA, according the dynamic range requirements, 11 bits was fair enough to deal with the physics cases. This makes HP-Ge to be more restrictive in terms of resolution, being hence the minimal resolution under which we should not go. Regarding the minimum sampling frequency, the most restrictive term in this case is provided from the timing resolution loss it can entail to sample below 200 Msps, being the specifications for the NEDA PSA algorithms much more relaxed (100 Msps at 10 bits), as well as the minimal sampling frequency for EXOGAM (100 Msps).

Chapter summary

After having reviewed and understood the underlying concept of physics involving HP-Ge detectors, in this chapter the instruments EXOGAM and NEDA, have been presented. One of the emphasis points has been the digitizer NUMEXO2, the common point between EXOGAM2

and NEDA, subject for which the FADC Mezzanine specifications were introduced thereby in. The last section presented the specifications required to design the FADC Mezzanine, taking into consideration the type of signals being involved, resolution and sampling frequency. Hence, the next chapter deals with the electronic design based on NUMEXO2 conception and the aforementioned specifications to fulfill the requirements from both detectors.

4. FADC Mezzanine design

This chapter can be considered as the core chapter of this PhD thesis. Taking as starting point the section 3.4, where the specifications are summarized, the design of the FADC Mezzanine will be discussed.

It is foreseen to provide to the reader the most straightforward manner to follow the design. Hence, given the specifications, the first step is to propose a block diagram for the design. For each block of the diagram, taking into account the specifications and the full diagram design, the next step is a detail study of the main components necessary to implement the block, comparing alternative components and solutions, and then choosing the best ones fitted. As the design proceeds forward, more focus is put into more specific issues, such as the resistor values of the analog stage and the noise models. Finally, the design continues by describing issues regarding power consumption, interfacing to the front-end electronics and the motherboard, control and programmability, PCB design and manufacturing, covering comprehensively the whole FADC Mezzanine design.

4.1. From the specifications to the block diagram

Based on the specifications established in 3.4, the FADC Mezzanine must fulfill the following requirements:

- Continuous acquisition of four channels, according to NUMEXO2 specifications.
- Signals from NEDA impose a condition on the minimum sampling rate due to its faster pulse signals involving rise-times around 10 ns with decay time in the range of few hundreds ns. The minimum sampling frequency in order to achieve a reasonable timing performance, essential to perform NGD, is 200 MHz sampling frequency, as we mentioned before.
- Each FADC Mezzanine contains 4 acquisition channels working in parallel.
- Based on the energy resolution parameter for the inner HP-Ge EXOGAM spectrometer, a resolution of at least 11.3 ENOB is needed, in order not to degrade the resolution.
- Gain flexibility. It is specified to acquire samples both working at 6 MeV and 20 MeV for the case of EXOGAM2.
- Dynamic offsets, allowing the acquisition of both bipolar and unipolar signals, taking moreover advantage of the full FADC dynamic range.
- Flexibility and testability. Taking into account the total number of FADC Mezzanines for EXOGAM and NEDA, they rise up to 200 units where a quick and automated test must be carried out during the production test.
- 4 FADC Mezzanine are plugged onto NUMEXO2 motherboard, which fits into a NIM crate. Hence, the FADC Mezzanine size must be designed taking the NUMEXO2 size constraints. Details concerning the size position of the components regarding the motherboard placement restrictions are discussed in physical design, sub-section 4.9.

On the basis of the points mentioned above, the block diagram, shown in Fig. 4.1, has been drafted.

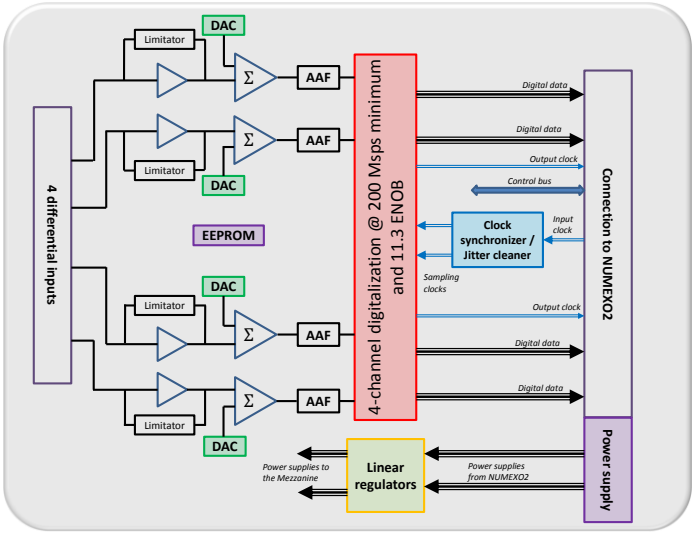


Figure 4.1: FADC Mezzanine general block diagram

Taking each block separately, it is possible to emphasize particular characteristics.

- The A/D devices, corresponding to the block depicted in red, in charge to acquire samples with a minimum sampling rate of 200 MHz at 11.3 ENOB.
- A clock synchronizer and jitter-cleaning device. High-sampling frequencies are highly affected by the clock jitter, degrading the SNR, and consequently, decreasing the resolution. Moreover, most of the on-the-market devices offer several clock outputs, thus, when needed, the device can be used also as a clock fan-in fan-out unit.
- Devices capable to drive dynamic offset values allowing to fully exploit the A/D dynamic range. Common devices to achieve this goal are digital-to-analog converters (DACs) or digital potentiometers.
- Analog coupling stages, whose function is to fit the input voltage range to the FADC full-scale range adding a minimal amount of noise to preserve the resolution. In addition, the diagram shows voltage limiters, used to protect the analog coupling stages from high-voltage peaks, an important fact due to the cosmic rays which might impinge into the scintillator, and an AAF (Antialiasing Filter) used to reduce the noise bandwidth and the aliased frequencies.
- Memory. Used to store miscellaneous information for FADC Mezzanine identification.
- Control bus. Usually, some commercial devices such as A/D converters, PLLs, EEPROM, DACs etc. include a set of registers in order to select the most appropriate parameters. Hence, the bus is fundamental to program the devices and make them work. Besides, programmable devices enhance the device testability.
- Power regulators and connectors. The Mezzanines are read out and power-supplied from the motherboard, although linear regulators are used on the Mezzanine to

provide and clean all the required power supplies to the devices. On the other hand, the analog inputs are provided directly to the Mezzanine without passing by any connector on the motherboard.

4.2. Study of the A/D devices

The FADC is the core of the Mezzanine, therefore, the election of device implies one of the most important steps during the design stage. It is important not only choosing a device capable to fit into the specifications, but also to seek the optimal device (simplest, less power consuming and easiest to communicate with). Table 4.1 compares the performance of several A/D devices, based on the information taken from their datasheets.

Table 4.1: Comparison of high-speed A/D devices

Device reference	f_{sMAX} *(MHz)*	Company	nº bits	nº channels	ENOB	Outputs	BW (MHz)	Package	Power /ch. (W)
ADS6244	105	Texas	14	2	11.3	2 LVDS	500	48-VQFN	0.9
ADS62P49	250	Texas	14	2	11.7	7 LVDS	700	64-QFN	1.25
AD9250	250	AD	14	2	11.5	Serial 8b/10b	1000	48-LFCSP	0.71
ADS61B49 [64]	250	Texas	14	1	11.3	7 LVDS	500	48-QFN	0.79
AD9643-250	250	AD	14	2	11.6	7 LVDS	350	64-LFCSP	0.614
LTC2156-14	210	Linear	14	2	11.3	7 LVDS	1250	64-QFN	0.65
ADS4149	250	Texas	14	1	11.2	7 LVDS	400	48-QFN	0.265

ADS6244 [65] was initially discarded due to the lack of sampling frequency and (105M maximum when 200M are at least required. Comparing the performance of the rest of devices in terms of sampling frequency and resolution it can be noticed that most of them behave quite similarly. Therefore, single-channel devices were firstly discarded in order to take benefit of the Mezzanine size, as well as these devices whose output protocol are based on serial encoded links such as the AD9250 [66]. The reason of not choosing A/D with serial output comes from the compliancy with the firmware development in the Virtex-6, whose resources were optimized to read the ADCs using DDR LVDS lines. Regarding the rest of dual A/D, ADS62P49 [67], LTC2156 [68] and AD9643 [69], finally the decision was keen on the device whose ENOB was the highest, electing the ADS62P49 – in fact, the LTC2156 with 11.3 fits too tightly the resolution requirements - as the most appropriate election at the expense of higher power consumption.

The election of the ADS62P49 as the optimal device for our application was then confirmed by verifying its functionality with the ADS62P49 evaluation module from Texas Instruments. The setup consisted of the aforementioned evaluation module interfaced to a ML605 board with a Virtex-6 which contained an ISERDES IP in order to deserialize and provided the capability to monitor data using the Chip Scope Pro. The evaluation module provides two types of analog input stages, one based on transformers, and a second one using the fully-differential amplifier THS4509 Texas Instruments. Configuring the analog stages with the fully-differential amplifier, and then, providing a sampling clock of 200 Msps, the noise performance obtained was a noise standard deviation of 1.3 ADC counts, providing an ENOB of 11.83 ENOB. This result confirmed the suitability of this device as the FADC for our

application. Firstly, the evaluation module was tested by GANIL, and then verified using a second evaluation board in Valencia.

4.2.1. ADS62P49 device overview

The most important consequence of the A/D device choice is the dependence of the rest of the Mezzanine components on the A/D architecture and performance figures, therefore, it is relevant to discuss the A/D characteristics in order to understand the design of the full Mezzanine. In Fig. 4.2, it is shown the A/D block diagram, detailing the internal blocks and interface.

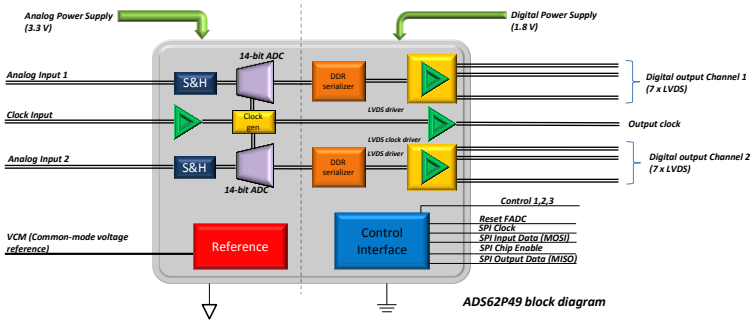


Figure 4.2: ADS62P49 device block diagram

The double lines refer to the differential inputs/outputs while the SPI control lines are plotted as single continuous lines. Among other details, it is worth to mention the ensemble of differential outputs, gathered in groups of seven pairs, the common-mode voltage reference V_{CM}, SPI control interface, and separated analog and digital power supplies and grounds. Internally, the FADC architecture is based on a pipelined architecture, obtaining the desired 14-bit sample after sampling on several sub-ranging lower-resolution stages [70].

Power supply and power consumption

As seen in Fig. 4.2, ADS62P49 requires two different power supplies. On one side, an analog power supplies the analog comparators at 3.3 V, consuming a maximum amount of current of 305 mA when sampling at 250 MHz. On the other hand, the FADC digital output drivers require 1.8 V and a supply current of 133 mA. Summing up both contributions, the total power consumption for each FADC at 250 MHz is:

$$P_T = P_{analog} + P_{digital} = V_{cc_{analog}} I_{cc_{analog}} + V_{LVDS} I_{LVDS} \\ = 3.3\,V * 330\,mA + 1.8 * 133\,mA \approx 1.25\,W \qquad 9)$$

Expression 9) shows the whole power consumption for 1 chip. When using two chips at maximum sampling frequency, the power rises up to 2.5 W.

Analog and clock inputs

Analog inputs are provided differentially plus a common voltage set by V_{CM} to 1.5 V, allowing the use of unipolar power supplies. The ADC full range scale is set to ±1 V differential. Therefore, that means that for a certain voltage difference V_{ip}-V_{in} = +1 V, the output corresponding to this code will be the highest code for a 14-bit ADC, which is 0x3FFF. Analogously, given an input differential voltage V_{ip}-V_{in} equal to -1 V, it will be assigned the lowest output code, which is 0x0000. Likewise, if the differential input is set to 0 V, the code corresponds to the value only with V_{cm}, assigned to 0x1FFF.

Understanding the internal structure of the analog input stage is crucial for the design of the analog drivers. One fundamental feature to be taken into account from the datasheet regarding the analog driver design is the input impedance of 1 MΩ in parallel with 3.5 pF where the capacitive term influences drastically on the frequency response at high frequencies of the antialiasing filter. The clock input is preferable to be driven differentially and AC-coupled for best performance, either in LVDS or LVPECL, although it works, besides, with a CMOS standard input clock if properly terminated.

Digital outputs

Fig. 4.3 shows a chronogram with the timing and signals involved in the conversion. The study of the chronogram is necessary for the design of the connectors, the test platform which is presented in the following chapter, and the firmware inside the Virtex-6 for NUMEXO2.

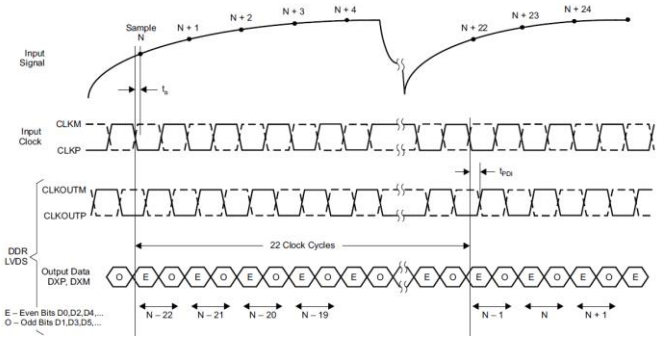


Figure 4.3: ADS62P49 digital output chronogram protocol [67]

Is important to mention that bits are serialized in pairs before being delivered to a differential pair, reducing the total number of output lines by a half. For instance, bits 0 and 1 are driven to the output pair nº0, while bits 2 and 3, thus, to the pair nº1. The same procedure is done for the rest of bits. Serializing the output bits implies to duplicate in the output data rate, obtaining for 250 MHz sampling frequency, an output throughput of 500 Mbps per differential pair, and thus up to 7 Gbps/device, for the 14 the pairs within one chip. The output clock is provided as a DDR (Double Data Rate), to reduce the clock frequency by a half, although the deserialization process requires of specific resources in the firmware in order to obtain the raw-data samples.

ADS62P49 slow control and register setup

ADS62P49 includes two different control modes which make possible to configure the device parameters, increasing its versatility and testability. Some of these parameters, are, for instance, the type of output protocol (CMOS, LVDS), output data format (2's complement / binary offset), capability to use test modes, gain and offset adjustments, readout enable, and data versus clock output phase among others.

Two types of configuration can be applied, being the "serial mode" the most interesting due to its higher versatility and possibility to be implemented in a master device controller such as an FPGA, DSP or microcontroller. The "parallel mode", which makes use of jumpers to test the different test modes, offers a much lower range of possibilities for testing. Since the serial protocol is based on SPI, an additional point to take into account once the FADC has been selected is the type of low-speed control protocol used by the rest of devices, since uniformity will lead to a simpler design.

Each register contains 8 bits, accessible using an address of 8 bits as well. However, only a limited number of bits from certain registers can be modified by the user whilst the rest remain reserved. The configuration procedure can be easily performed by implementing the SPI protocol, taking into account the following constraints:

- 16 bit data (8 for the address and 8 for the register data).
- Data latched during the falling clock edge.
- Maximum SPI clock at 10 MHz.
- Chip enable signal is enabled low.

4.3. Study of the jitter cleaner devices

In high-speed A/D design, a "must" is the adequate choice of a low-jitter sampling clock. The jitter is directly translated into noise and the amount of noise depends on the fastest signal component, thus the jitter impacts SNR, degrading the ENOB. Specially, in the case of pulses from the detector involving fast rising times the consequences may be dramatic if the jitter effects are not taken into account. The magnitude of the SNR degradation caused by jitter effects is connected to the maximum slope of the input signal, i.e. with the signal bandwidth by the following equation [71, 72].

$$SNR_{jitter} = -20\log_{10}(2\pi f_{in}\tau_a) \qquad 10)$$

where τ_a is the aperture RMS jitter. Assuming a NEDA signal with a 10 ns rise-time, the maximum equivalent frequency which does not slow down the slope according to expression 10) is 100 MHz. The maximum allowable jitter, assuming no other noise sources, can be calculated from equation 11).

$$\tau_a = \frac{10^{-\frac{SNR_{jitter}}{20}}}{2\pi f_{in}} = \frac{10^{-\frac{69.78}{20}}}{2\pi 100 * 10^6} = 516.2\ fs \qquad 11)$$

Nevertheless, in practice, the jitter is not the only source which might be translated to noise, fact for which a clocking device with lower jitter must be chosen. Another common way to calculate the jitter comes from Fig. 4.4, which depicts the results from the expression 11) in a graphical form.

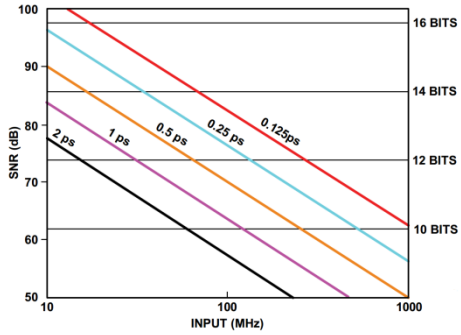


Figure 4.4: SNR contribution from jitter sources

Having described already the jitter impact on the analog-to-digital conversion, the next step consists of choosing a jitter cleaner to fulfill jitter requirements. As it was the case in the selection of the A/D chips, not only the jitter matters in the process of choosing a device. For instance, the inclusion of integrated elements and control compatibility have been taken into account to simplify the overall design. The records of analyzed devices are shown in Table 4.2, detailing the parameters in which more emphasis we put in.

Table 4.2: Comparison of jitter cleaner devices

Device reference	*RMS jitter*	Integrated VCO?	Integrated Filter?	Programming protocol	Outputs	Package
CDCE72010 [73]	--	Yes	No	SPI	10 LVDS / LVPECL	64-QFN
LMK03001C	400 fs	Yes	Yes	µWire	3 LVDS / 5 LVPECL	48-LLP
AD9510 [74]	500 fs	No	No	SPI	4 LVDS / 4 LVPECL	64-LFCSP

Among all the devices which have been examined, the final choice was devoted to the LMK03001C [75], due to its overall simplicity, easy programming by using the µWire[12] and the inclusion of integrated VCO and partially-integrated filter, an interesting approach in designs requiring high-density in terms of devices and components. Extra features we should mention are its 48-LLP package and the single power supply at 3.3 V.

4.3.1. LMK03001C device overview

As we did with the ADS62P49 FADC, the LMK03001C is another of the main devices, for which a few paragraphs are necessary to introduce its behavior and performance of this device. Fig. 4.5 shows the functional block diagram.

[12] *µWire stands for a serial control protocol created by National Semiconductors, highly compatible with the SPI.*

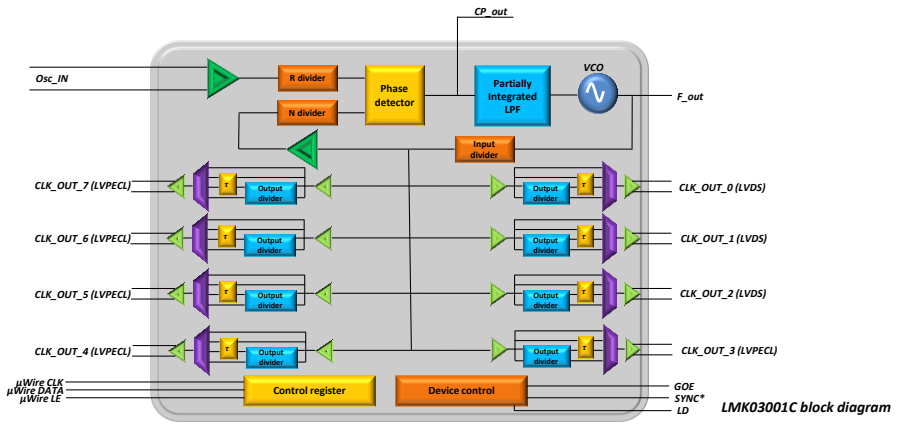


Figure 4.5: LMK03001C functional block diagram

µWire control protocol

As the SPI, also the µWire is based on a synchronous serial protocol, for which a single standard is not widely used, requiring the compliancy between the master and the slave using more generic SPI master drivers in the firmware. Some differences over the SPI from ADS62P49 is the lack of readout signal, the data length of 32 bits and the rising-edge latching.

LMK03001C configuration responds to the setup of the 16 32-bit registers during the device startup. Some parameters are required to be programmed before any clock is delivered like the frequency divider values, the output phase delay adjustment and cut-off frequency of the partially-integrated filter. In the register bank, R0-R7 are devoted to configure the local output parameters and some of them can be skipped, whilst the registers R13-R15 are mostly related with the global mode configuration and must be obligatorily set up.

Selection of an output clock frequency

According to Fig. 4.5, two different parts of the device can be distinguished: the PLL and the output driver tree. Thanks to this tree structure, LMK03001C offers the possibility to drive different clock frequencies using an input fixed frequency only by setting up the values of the internal local dividers. Fig. 4.6 shows schematic overview in which the PLL functionality can be laid out and the associated equations described.

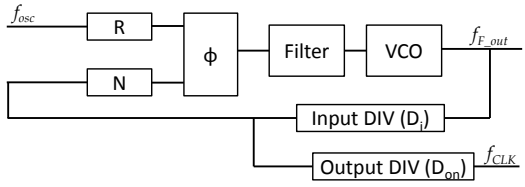


Figure 4.6: Schematic overview of the LMK03001C dividers

From the datasheet specifications, the VCO can be tuned between frequencies from 1.5 GHz to 1.6 GHz, while the input oscillator frequency f_{osc} is provided from NUMEXO2 motherboard as a 100 MHz clock differential signal. One design criteria is to establish that the frequencies on both sides of the phase comparator are equal, so that their difference tends to a zero error, working as a classic closed-loop system and recommended to be close to 10 MHz. Therefore, the equation at the phase comparator is:

$$\frac{f_{osc}}{R} = \frac{f_{vco}}{N * D_i} \qquad 12)$$

The second equation comes from the desired local clock frequency as

$$f_{CLK_n} = \frac{f_{vco}}{D_i * D_{o_n}} \qquad 13)$$

In which the D_{o_n}term stands for the *n*-th clock output divider value. Values written in the output divider are automatically divided by 2, this means that only even divisions are allowed at the output.

To obtain f_{CLK_0} = 100 MHz from the expressions 12) and 13), we must choose an appropriate f_{vco} to achieve the desired frequency. Since frequency divisions are preferred to be performed in even terms, it was preferred to choose an even multiple of the desired output frequency, f_{vco} = 1.6 GHz. The phase comparator frequency of 10 MHz imposes an R divider value of 10 and the f_{vco} sets the product $D_i \cdot D_{o_n}$=16, selecting D_i= 2 and D_{o_n}= 8. Finally the loop can be closed by selecting N = 80, according to 13). Deriving the same expressions in order to obtain 200 MHz can be easily achieved keeping the values for f_{vco} and D_i , changing only D_o to 4. The same procedure leads to the divider values for 50 MHz, 150 MHz and 250 MHz sampling frequencies, shown in Table 4.3.

Table 4.3: Divider values to obtain different sampling frequencies using the LMK03001C and a 100 MHz input clock source

f_{CLK}	R	N	Di	Do	f_{VCO}
50 MHz	10	80	2	16	1.6 GHz
100 MHz	10	80	2	8	1.6 GHz
150 MHz	10	30	5	2	1.5 GHz
200 MHz	10	80	2	4	1.6 GHz
250 MHz	10	50	3	2	1.5 GHz

4.4. Study of the analog drivers

As it was mentioned several times throughout the text, low-noise is directly connected to the energy resolution for gamma-ray spectroscopy with HP-Ge detectors. The election of an appropriate analog stage requires not only by the election of the most suitable analog drivers, commonly based on operational amplifiers, transformers or fully-differential amplifiers (FDA), but also being concerned about the type of topology and discrete elements, requiring the use of specific noise models to study thoroughly the origins and impact of the noise.

4.4.1. Study of the analog drivers

The analog driver stage matches the input voltage range to the FADC voltage range adding a minimal amount of noise so that no resolution is lost in the process. Additionally an offset is

added at this level in order to take profit of the full FADC range. Using the specifications from the section 3.4, we have summarized the requirements on the design of the analog stages in the following points:

- Bandwidth: NEDA signals contain pulses with rise-times of 10 ns, where a bandwidth degradation influences and smoothens the signal rising time. Even if smoother rise-times might lead to better timing measurements in digital systems, the design must foresee signals whose bandwidth is close to 100 MHz.
- Low-noise injection. Noise from the analog stage is square-added to the FADC noise. In order to reduce the influence of this stage to the A/D noise, the RMS noise voltage should be below 1 LSB.
- Concerning range, the input is a differential signal while it will be driven to an ADC device with differential inputs plus a common-mode voltage.
- Flexibility in the channel gain. EXOGAM2 channels must have the capability to be set at different energy ranges. The design must foresee he capability to work under gains that give 6 MeV and 20 MeV as full energy ranges.
- Offset. Taking advantage of the full FADC range and the possibility to move the baseline to acquire either positive, bipolar or negative pulses, an offset is needed to fulfill the specification concerning the FADC range.

Study of an analog high-speed amplifier

The pulsing nature of the detector signals make unfeasible the use of transformers since its band-pass frequency response damages the signal shape, necessary for the PSA. Instead, the employment of fast high-bandwidth amplifiers based on high-speed amplifiers is preferred although the noise performance is not comparable to those obtained with transfomers. The list of devices under considerations for the design is summarized in Table 4.4, where basically, low-noise fully-differential amplifiers (FDA) and high-speed OpAmps are considered.

Table 4.4: Comparison of high-speed analog amplifiers

Device reference	Device type	Voltage noise density (nV/sq(Hz))	Current noise density (pA/sq(Hz))	Bandwidth (at G=1)	Package	Input impedance
AD8002 [76]	CFA[13] (dual)	2.25	2.2	400 MHz	8-SOIC	10 MΩ (50 Ω)[14]
AD8139	FDA	2.25	2.2	410 MHz	8-SOIC	600 kΩ
AD8132 [77]	FDA	8	1.8	350 MHz	8-SOIC	10 MΩ
THS4509 [78]	FDA	1.9	2.2	1.9 GHz	16-QFN	1.3 MΩ

Since the signal treatment is performed over differential signals, although the CFA provide also a solution for differential signal processing, the election for a FDA is preferred in case they provide similar performances in terms of noise since they are specially envisaged to deal with differential signaling. Therefore, the device elected is the AD8139 [79].

[13] *CFA stands for Current Feedback Amplifier.*

[14] *CFAs have different input impedances on the positive (high-impedance) and negative input (low-impedance). The number in brackets refers to the impedance seen from the negative input.*

Study of a baseline offset mechanism

To take full advantage of the dynamic range of the ADS62P49, i.e. differential range of ±1V, requires the addition of a voltage such that the baseline can be moved to the extreme values in case the signal to be acquired has only positive or negative component (unipolar), setting the baseline value either to +1 V or -1 V. This constraint becomes a must for the EXOGAM2 / NEDA synergy since EXOGAM2 provides positive pulses while NEDA fast pulses from the PMTs are originally negative. Fig. 4.7 depicts examples of bipolar and unipolar acquisitions with their baseline levels set at their optimal positions.

Even if the election of devices of this kind is of paramount importance from the point of view of noise injection, the sort of variables influencing on its choice are not as critic as the FADC or jitter-cleaner. Some examples of devices which can be used to provide a variable offset DC signal are DACs (Digital-to-Analog Converters) and digital potentiometers, although DACs are preferred due to the fact that the resolution is normally higher than in digital potentiometers. Therefore, the main need is to find a device with low-noise injection and in case of DACs with higher resolution than the FADCs. Speed does not play an important role for this case since the offset values applied are DC voltages. Other parameters to optimize the choice are low-power consumption, device integrability, simplicity and compatibility with the rest of devices. In table 4.5, an overview of DACs with resolutions higher than 16 bits based on SPI taken into consideration for the design.

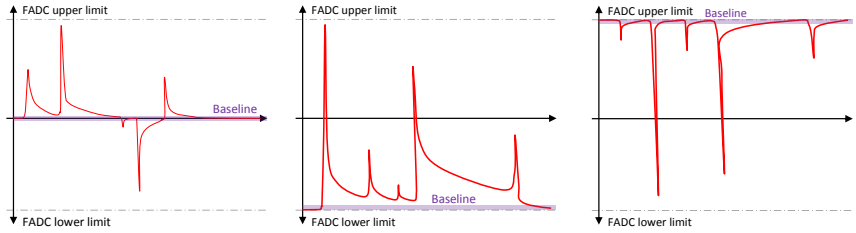


Figure 4.7 Examples of how the baseline can be moved to increase the dynamic range. Left. Acquisition of bipolar signals. Center. Acquisition of only-positive signals. Right. Acquisition of only-negative signals

Table 4.5: Comparison of Digital-to-Analog converters

Device reference	Output channels	Control Interface	Power	Package
DAC3283	2 diff.	Parallel / SPI	750 mW	48-QFN
DAC8532	2	SPI	2 mW	8-MSOP
AD5662	1	SPI	1.25 mW	8-MSOP / 9-SOT-23
AD5062	1	SPI	2 mW	8-SOT-23

After analyzing all the characteristics of the DACs mentioned in the table above, DAC8532 [80] fits the best the requirements due to its small size, double channel and low power consumption. Even though the DAC provides the capability to drive dynamic voltages, the DAC range does not have to be necessarily matched with the ADC range, requiring a linear transformation of the offset levels in order to fit entirely into the desired range. This adaptation can be done by using operational amplifiers. Moreover, it is fundamental that this intermediate offset driver is as well a very-low noise stage since it will be directly injected to the high-speed analog driver. Table 4.6 shows a set of operational amplifiers evaluated for the design.

Table 4.6: Comparison of precision OpAmps for an offset driver

Device reference	Output channels	Voltage noise (nV/sq(Hz))	Current noise (pA/sq(Hz))	Package
ADA4004-1/2/4 [81]	1/2/4	1.8	1.2	SOIC8/SOIC14/CSP
ADA4817-1 [82]	1	4	0.0025	SOIC8
OPA209 [83]	1	2.2	0.5	SOIC8
AD8597 [84]	1	1.07	2.3	SOIC8

A decision among these devices is fairly difficult, because all of them perform excellently in terms of noise. Finally the decision was keen on the ADA4004-2 due to the inclusion of 2 OpAmps in only one package, and a remarkable performance both in voltage and current noise.

Design of the high-speed analog driver using the AD8139

In case of EXOGAM2, the single-ended to differential connection box B3 (introduced in section 3.1.2) sets the relation between voltage and energy at 200 mV/MeV, being the starting point to determine the input ranges in volts. For an energy range of 5 MeV, this means that the input voltage is ±1V, provided differentially. Repeating the same process for 20 MeV, the analog stage must be capable to deal with signals of ±4 V. Fig. 4.8 shows an event covering the whole input dynamics and how should it be mapped into the ADC range.

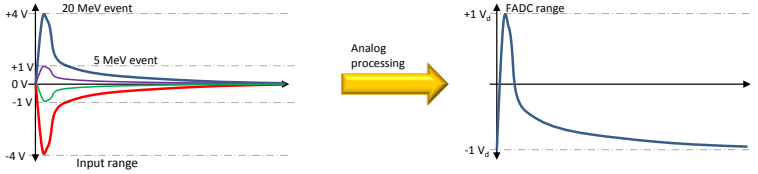


Figure 4.8: Example of how an 5 MeV and 20 MeV should be mapped in order to cover the whole dynamic range. Input signals are displayed breaking down both positive and negative components while the FADC input signal is depicted already differential

Taking the example from Fig. 4.8, for 5 MeV, the differential voltage between both waveforms is 2 V, which corresponds to the same differential voltage at the FADC input, hence, a unitary gain stage plus an offset adjustment is needed. In contrast, a range of 20 MeV needs to be divided by 4 before being driven to the ADC. Summing up, the analog stage must have either unitary or 0.25 gain depending on the channel which is applied to, plus the offset correction.

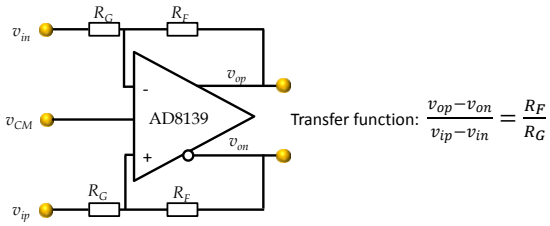


Figure 4.9: Standard schema of a fully-differential amplifier and its transfer function

Fig. 4.9 shows the basic transfer function of a generic FDA. Unfortunately, FDAs are devices which in most of the cases cannot operate below certain gains due to stability reasons. In our case, unitary gain is the minimal, requiring alternative topologies in case of lower gains are desired. Another constraint is the noise performance, optimal for unitary gain and decreasing as the gain increases. Moreover, the optimal noise performance is not achieved only by selecting a unitary gain, but also with the optimal choice of the surrounding discrete components.

The strategy used to achieve both gain flexibility and optimal noise performance is by using the basic AD8139 configuration with the addition of a T-divider at the input. Thus, an added degree of freedom is required to match the impedances and achieve gain flexibility using the intermediate node v_{xn}. Applying the equations at this node does not only allow to reduce the gain by a factor, but also allows to keep the input impedance equal to the feedback resistor so that they are equal and the FDA works as in unitary gain. The topology of the resulting network is depicted in Fig 4.10.

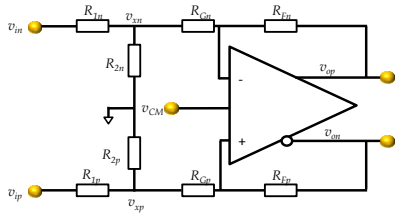


Figure 4.10: Proposed AD8139-based topology, aimed to provide flexibility in order to set the both impedance and gain requirements.

Applying the second Kirchoff's law to v_{xp} and v_{xn} nodes, as:

$$\left.\begin{aligned}\frac{v_{ip}-v_{xp}}{R_{1p}} &= \frac{v_{xp}-v_{p}}{R_{Gp}} + \frac{v_{xp}}{R_{2p}} \\ \frac{v_{in}-v_{xn}}{R_{1n}} &= \frac{v_{xn}-v_{n}}{R_{Gn}} + \frac{v_{xn}}{R_{2n}}\end{aligned}\right\} \quad 14)$$

Another equation is required to eliminate the terms, v_{xn} and v_{xp} relating the terms v_{xn} and v_{xp} to the output nodes v_{on} and v_{op} as:

$$\left.\begin{aligned}\frac{v_{xp}-v_p}{R_{Gp}}&=\frac{v_p-v_{on}}{R_{Fp}}\\ \frac{v_{xn}-v_n}{R_{Gn}}&=\frac{v_n-v_{op}}{R_{Fn}}\end{aligned}\right\} \quad 15)$$

Assuming a negligible resistance value tolerance for this analysis and pairing each component to its mirrored counterpart so that $R_{1n} = R_{1p}$, $R_{2n} = R_{2p}$, $R_{Gn} = R_{Gp}$ and $R_{Fn} = R_{Fp}$, we obtain a handier transfer function. In order to obtain the final transfer function expression with the divider, the terms at the amplifier input terminals v_n and v_p, must be isolated in each part of the equation 14) and 15). After algebraic manipulation the differential output term $(v_{op} - v_{on})$ is described in function of $(v_{ip} - v_{in})$, assuming that the branches are balanced.

$$\frac{v_{op}-v_{on}}{v_{ip}-v_{in}}=\frac{R_F}{R_G}\frac{1}{R_1}\left(\frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_G}}\right) \quad 16)$$

The impedance equality for optimal noise performance, establishes the equality between the feedback resistor and the equivalent resistor seen at the input. The impedance the amplifier sees at the input is equal to the input resistor R_G in series with the parallel of the T-divider resistors R_1 and R_2, building the term $R_G + R_1||R_2$ and thus, leading to the following equality.

$$R_F = R_G + R_1||R_2 \quad 17)$$

A third design constraint is the impedance matching seen from the input for a termination equal 100 Ω, making the design more difficult with the topology presented in Fig. 4.10, where gain, termination and optimal noise performance are constraints which must be fulfilled simultaneously.

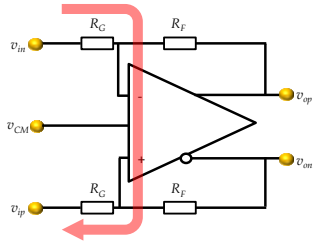


Figure 4.11: Schema to visualize the input differential impedance in a fully-differential amplifier

Fig. 4.11 depicts the differential input impedance seen from the amplifier. For a balanced FDA, the input differential impedance simplifies to:

$$Z_{in\_diff} = 2R_G \quad 18)$$

As the design with a single amplifier may lead to a problematic behavior, it was preferred to separate the termination contribution from the gain and offset adjustment by using a double stage based on the AD8139. Considering a standard stage based on the AD8139, but adding a single termination R_T on each part of the differential pair, the circuit would look like in Fig. 4.12:

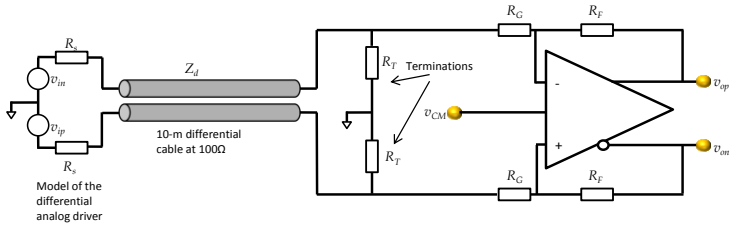


Figure 4.12: Analog stage including input terminators

The idea is to isolate the stage containing terminators from the next stage including the gain and offset adjustments. Additionally, in order to optimize the noise performance also on the first stage, it must be designed at unitary gain as well. Gathering both parts stages, the whole schema for one analog channel is illustrated in Fig. 4.13.

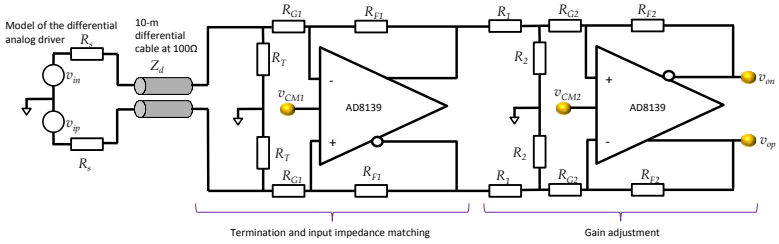


Figure 4.13: Analog stage based on a double AD8139 stage.

Starting from the topology that has been described, the set of equations required to design the second (or each new) stage are the gain equation 19), the equality of impedances – to optimize the noise performance and ensure the stability – corresponding to expression 20) and the terminator equation 21).

$$Gain = \frac{R_{F2}}{R_{G2}}\frac{1}{R_1}\left(\frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_{G2}}}\right) \quad 19)$$

$$R_{F2} = R_{G2} + R_1||R_2 \quad 20)$$

$$R_T||R_{G1} = 50 \quad 21)$$

Following the recommendations from the datasheet, for unitary gain conditions, $R_{F1} = R_{F2} = 200\Omega$. Under this condition, equation 21) can be easily solved, obtaining $R_T = 66\Omega$. The choice of R_1 and R_2 is a little bit more complex due to the non-linear equation system formed by the expressions 19) and 20).

Since the second amplifier must be ready to operate for unitary gain too, the equivalent schema would be rather simplified if making $R_2 \to \infty$ only for the case of G=1, where the resistor does not require to be mounted. Still R_1 and R_{G2} are present at the input of the second amplifier, where the condition $R_1 + R_{G2} = R_{F2} = 200\ \Omega$ must be satisfied. Choosing $R_{G2} = 100\ \Omega$ establishes R_1 to be set to 100 Ω. For G = 0.25, the equations become more cumbersome, requiring the whole expression both in 20) and 21). Taking the value for unitary gain of R_{G2}=100 Ω, the solution leads to R_1 = 400 Ω and R_2= 133 Ω, being R_1 and R_2 the only different values for different gains. The resistor values are detailed in Table 4.7.

Table 4.7: Resistor values for the analog stage in ohms.

Gain	R_T	R_{G1}	R_{F1}	R_1	R_2	R_{G2}	R_{F2}
1	66	200	200	100	open	100	200
0.25	66	200	200	400	133	100	200

Regarding the AC behavior of the fully-differential section, it is important to mention two points: the behavior at very high frequencies of the AD8139 and the inclusion of an antialiasing filter in order to reduce the unnecessary frequencies and noise.

Observing the large-signal frequency response of AD8139 in Fig. 4.14, it can be noticed the small overshoot of 1 dB occurring at frequencies between 100 MHz and 200 MHz. This effect can be solved by flattening the frequency response using a 1 pF feedback capacitor in parallel with R_F.

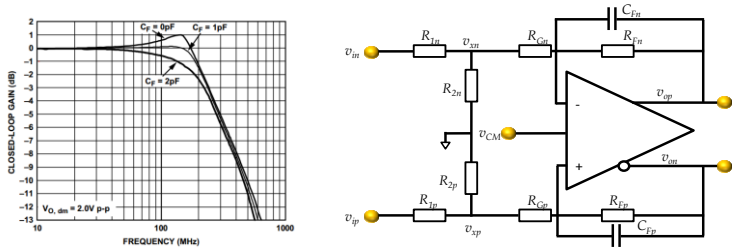


Figure 4.14: Left) Overshoot effects on the large-signal frequency response [79] b) Feedback capacitor placement for overshoot flattening

The feedback amplifier network becomes $Z_F(p) = 1/(1 + pC_F R_F)$ adding a pole at $f_c = 1/2\pi R_F C_F =$ 795 MHz, obtaining a larger pole frequency than the amplifier pole itself. Nevertheless, it is not foreseen this pole acting as the bandwidth adjustment, whereas the antialiasing filter carries on this functionality, using C_F only for overshoot removal. Choosing the filter cut-off frequency can be implemented by adding at the ADC input a single-pole low-pass fully-differential filter. The procedure of how to design this kind of filters is shown in Fig. 4.15 [85, 86].

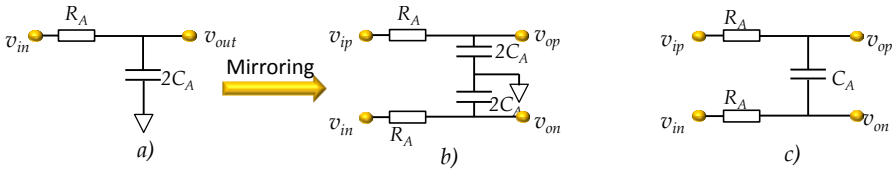


Figure 4.15: a) Single-pole low-pass filter. b) Overlapping the structure with a mirrored version, obtaining a differential-like structure. c) Equivalent structure for fully-differential filtering

Expression 22) describes the transfer function for a fully-differential single-pole filter, including the ADC parasitic input capacitance of 3.5 pF, which must be taken into account specially for high bandwidths, where its contribution is mostly noticeable. However, ADC input resistance has been considered high enough (1 MΩ) to be omitted in the calculations.

$$G_d(p) = \frac{1}{1 + 2pR_A(C_A + C_{in\_FADC})} \qquad 22)$$

Taking a R_A= 50 Ω low enough compared to the input impedance, input impedance of 1 MΩ, capacitors can be chosen taking 35 MHz for EXOGAM2 electronics and 100 MHz for NEDA, obtaining respectively C_A = 41.5 pF and 12 pF respectively. Including the term of the antialiasing filter into the general transfer function, the expression can be approximated to:

$$\frac{(v_{op} - v_{on})(p)}{(v_{ip} - v_{in})(p)} \cong \frac{R_F^2}{R_{G2}} \frac{1}{R_1} \left(\frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{G2}}} \right) \left(\frac{1}{1 + pR_A C_A/2} \right) \qquad 23)$$

Noise model of the high-speed driver based on AD8139

In low-noise applications design, it is convenient to study the noise sources using circuital noise models so that the major contributions to the noise total response can be characterized. The model shown in Fig. 4.16, shows a breakdown of the contribution from the fully-differential amplifier and the thermal noise from the resistors, modeling the main sources of noise in this sort of circuits [87].

The noise analysis can be more easily performed by separating the analog circuit into two sub-stages (squared in a red dashed line) and then applying the Friis' formula. For each of them, we apply hence the superposition theorem to each source taking squared magnitudes of voltages and currents, so that they can be summated in terms of power. Analyzing the noise contributions from the first stage, we obtain the expression 24)

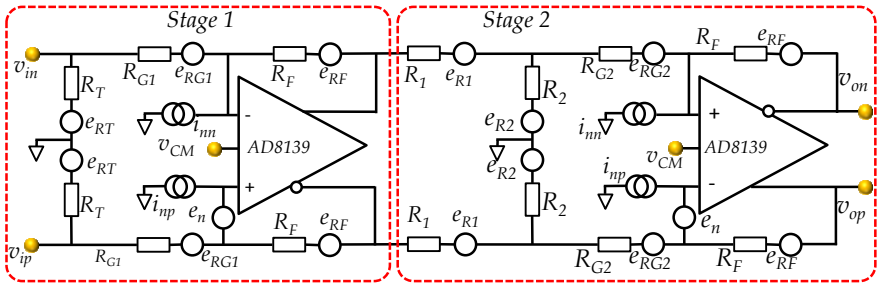


Figure 4.16: Noise model for the high-speed driver

$$e_{o\_s1}^2 = e_n^2 \left(1 + \frac{R_F}{R_{G1}}\right)^2 + i_{nn}^2 R_F^2 + i_{np}^2 R_F^2 + 8kTR_F + 8kTR_{G1}\left(\frac{R_F}{R_{G1}}\right)^2 + 8kTR_T\left(\frac{R_F}{R_{G1}}\right)^2 \qquad 24)$$

The term $8kT$ arises from gathering the contributions from 2 resistors in the term for the thermal noise $4kT$, where k is Boltzmann's constant $k = 1.38 \cdot 10^{-23} J/K$, assuming a temperature of 300 K. Substituting the resistor values and the fully-differential white noise contribution $e_n = 2.25\ nV/\sqrt{Hz}$ and $i_{nn} = i_{np} = 2.2\ pA/\sqrt{Hz}$ [79], the total output spectral noise density is $e_{o\_s1} = 6\ nV/\sqrt{Hz}$. Applying the same procedure to the second sub-stage, is slightly more cumbersome, due to the contribution from the T-divider which attenuates the noise contribution of R_1 and R_2. Also, the noise gain is now provided by the equivalent impedance seen backwards from the input terminal, which is $R_{eq} = R_{G2} + R_1 || R_2$. Therefore, the expression is:

$$e_{o\_s2}^2 = e_n^2\left(1+\frac{R_F}{R_{eq}}\right)^2 + i_{nn}^2R_F^2 + i_{np}^2R_F^2 + 8kTR_F + 8kTR_{G2}\left(\frac{R_F}{R_{eq}}\right)^2 + 8kTR_1\left(\frac{R_F}{R_{eq}}\right)^2\left(\frac{R_2||R_{G2}}{R_2||R_{G2}+R_1}\right)^2 + 8kTR_2\left(\frac{R_F}{R_{eq}}\right)^2\left(\frac{R_1||R_{G2}}{R_1||R_{G2}+R_2}\right)^2 \quad 25)$$

The total contribution from the second sub-stage is $e_{o\_s2} = 5.83\ nV/\sqrt{Hz}$. The total output spectral noise density can be obtained by applying Friis' formula. As the structure is simplified since amplifiers are set to unity gain for optimal noise performance, the total noise contribution of both stages leads to:

$$e_o = \sqrt{e_{o\_s1}^2 + e_{o\_s2}^2} = 8.36\ nV/\sqrt{Hz} \quad 26)$$

Recalling the definition of noise bandwidth, the transfer function $|T(f)|$ from 27) can be modeled as a first-order single-pole transfer function. Applying the noise bandwidth definition from [88]:

$$v_{noise\_RMS}^2 = \int_{BW} e_o^2\,(f)|T(f)|^2 df = e_o^2 B_{eq} \quad 27)$$

for a first-order filter, $B_{eq} \cong 1.57 f_c$, where f_c is the filter cut-off frequency. The results of v_{noise} for f_c =30 MHz and f_c =100 MHz are 45.81 μV_{RMS} and 83.65 μV_{RMS} respectively. A common way to convert from RMS noise to peak-to-peak voltage[15] is to use $v_{noise_{pk-pk}} \cong 6.6 v_{noise\_RMS}$, assuming that the probability that a sample will overcome the peak-to-peak threshold is close to 0.1%. Hence, we obtain 552.09 $\mu V_{pk\text{-}pk}$. By comparing the results to the effective LSB voltage from ADS62P49, we obtain:

$$v_{LSB\_eff} = \frac{R}{2^{ENOB}-1} = \frac{2\ V}{2^{11.7}-1} = 601\ \mu V \rightarrow v_{noise_{pk-pk}} = 552\ \mu V < v_{LSB\_eff} \quad 28)$$

where it is evidenced that the contribution from the analog stage is smaller than the contribution from the LSB bit, verifying the analog stage suitability.

Simulations

Noise performance from Analog Devices can be verified using tool Diff-Amp calculator, which uses information regarding the range, noise and distortion taking into account the device used, resistor values and tolerances, power supply, and the possibility to use a low-pass filter at the output and load type. The results the tool offers are depicted both numerically and in a sector graph detailing the noise contribution from each component, especially interesting matter when driving high-resolution analog-to-digital converters. On the other hand, a drawback is the lack of circuit topologic versatility, offering only the possibility to use the standard balanced configuration. A tool screenshot is illustrated in Fig. 4.17.

[15] *As the noise is Gaussian, always there is a probability that at a certain time, the noise will exceed the value obtained as $V_{pk-pk} \cong kV_{RMS}$. For k=6.6 the probability of a sample to exceed the threshold is 0.1 %*

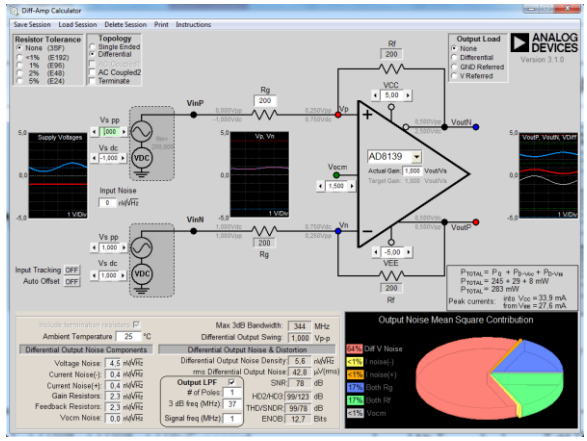


Figure 4.17: Screenshot of the Analog Devices tool for simulation on fully-differential amplifiers

The design simulation setup proceeds obtaining the noise density from the first stage and using this value as the noise spectral input density for the second stage. The first stage was modeled using a termination equal to $R_T = R_G||R_s$ whose source impedance is set to 50Ω, obtaining an output spectral noise density of $5.7\ nV/\sqrt{Hz}$. Using this spectral noise density as the input for noise calculations on the second stage, we simulated the effect of choosing different antialiasing filter orders at different frequencies, analyzing the effect of the noise, which is shown in Fig. 4.18. Using a unitary gain configuration for the second stage, where $R_{G2} = R_{F2} = 200\Omega$, the spectral voltage density at the ADC input rises to $e_o = 8\ nV/\sqrt{Hz}$. Comparing this result with the $8.36\ nV/\sqrt{Hz}$ obtained by applying the theoretical model, we conclude that a first-order filter suits our application the noise contribution is below the LSB voltage.

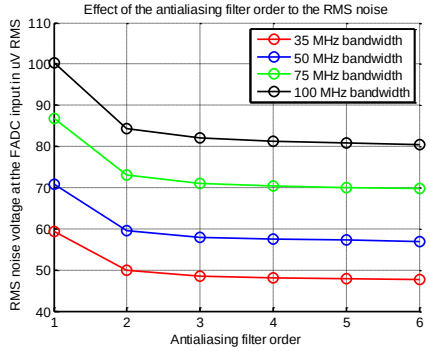


Figure 4.18: Effect of the antialiasing filter order over the total amount of noise

Design of the offset driver

Getting back to the FADC dynamic range specifications, the specified differential input range is ±1V differential, meaning that the offset driver must be capable to drive both extreme voltages. A strategy to add the dynamic offset in fully-differential amplifiers so that the offset

infers on the differential voltage is to add them using a second input branch in parallel to the input branches, and in both positive and negative terminals. For our case, this modification is applied on the second stage immediately after the T-divider, as it is shown in Fig. 4.19.

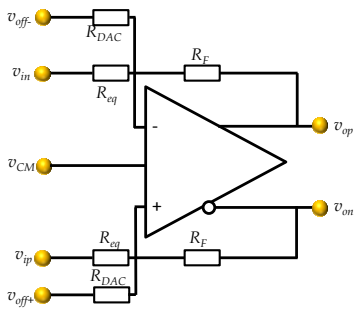


Figure 4.19: Inclusion of offset terminals to the high-speed analog driver based on AD8139

The DC transfer function is then modified as shown in 29) where R_{DAC} and $v_{off+} - v_{off-}$ should be designed.

$$v_{op} - v_{on} = \frac{R_F}{R_{eq}}(v_{ip} - v_{in}) + \frac{R_F}{R_{DAC}}(v_{off+} - v_{off-}) \qquad 29)$$

Of course, including a second branch influences the first branch as it is placed in parallel. However, as the parallel of both input resistors is always smaller than any of the resistors itself, the gain will be always greater than one. Nevertheless, the choice of R_{DAC} must be done carefully, to minimize the influence over the main branch. Higher R_{DAC} implies higher v_{off} until the ADA4004-2 limitations whereas lower R_{DAC} impacts mostly on the overall gain. To choose the value of R_{DAC}, it is simpler to neglect the input term, being connected to the ground terminal, and assuming only the input voltages from the offset branch. A second simplification can be assumed since the voltages are always symmetric and $v_{off+} = -v_{off-}$. Establishing the ADC boundary conditions, the equations lead to:

$$v_{op} - v_{on} = \begin{cases} \frac{R_F}{R_{DAC}}(-2v_{off}) = -1 \\ \frac{R_F}{R_{DAC}}(+2v_{off}) = +1 \end{cases} \qquad 30)$$

R_{DAC} maximum value is conditioned by v_{off} maximum voltage, limited by the ADA4004-2 clipping voltage, set to ±3.6 V. The selected maximum v_{off} was established to 3.3V, saving a security margin from the amplifier saturation and taking advantage over the DAC8532 voltage reference. Hence, for v_{off} = 3.3 V, substituting in 30) it leads to R_{DAC} = 1.32 kΩ. Afterwards, the design of the linear transformation intermediate stage using the ADA4004-2 can be carried out by establishing input/output conditions at the DAC output and the maximum voltages set at the offset branch of the AD8139 as:

$$\begin{cases} Code = 0x0000 \rightarrow v_{DAC} = 0 \rightarrow [v_{off+} = -3.3V, v_{off-} = +3.3V] \\ Code = 0xFFFF \rightarrow v_{DAC} = 3.3 \rightarrow [v_{off+} = +3.3V, v_{off-} = -3.3V] \end{cases} \qquad 31)$$

which can be rearranged in terms of a linear function model $f(x) = ax + b$, v_{DAC} as a variable:

$$\begin{cases} v_{off+} = 2v_{DAC} - 3.3 \\ v_{off-} = -2v_{DAC} + 3.3 \end{cases} \quad 32)$$

and a constant supplied from a low-noise voltage reference. The schematic approach and the transfer function are depicted in Fig. 4.20.

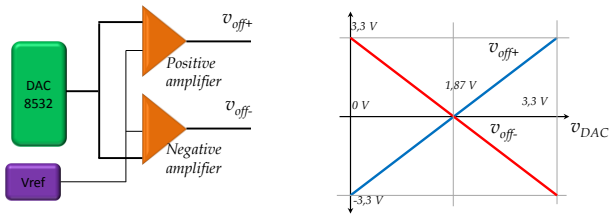


Figure 4.20: left) Schema of the negative and positive amplifier. Right) Transfer function in DC

Implementing the function from 32) electronically can be carried out by means of a generic adder-subtractor topology (Fig. 4.21) using the ADA4004-2, whose transfer function is given in 33). Supplying two offset inputs require two operational amplifiers, making very interesting the choice of dual chips, such as the ADA4004-2

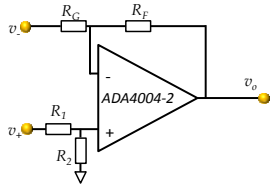


Figure 4.21: Generic topology using the ADA4004-2 for voltage linear mapping

$$v_o = v_+\left(\frac{R_2}{R_2 + R_1}\right)\left(1 + \frac{R_F}{R_G}\right) - v_-\frac{R_F}{R_G} \quad 33)$$

According to equation 33), both negative and positive linear transformations can be applied by connecting the terminals v_{DAC} and v_{ref} to the respective inverting or non-inverting op-amp inputs, depending on the desired polarity for each case, obtaining the transfer function for our specific case in expression 34)

$$\begin{cases} v_{off+} = v_{DAC}\left(\frac{R_{2p}}{R_{2p} + R_{1p}}\right)\left(1 + \frac{R_{Fp}}{R_{Gp}}\right) - v_{ref}\frac{R_{Fp}}{R_{Gp}} \\ v_{off-} = v_{ref}\left(\frac{R_{2n}}{R_{2n} + R_{1n}}\right)\left(1 + \frac{R_{Fn}}{R_{Gn}}\right) - v_{DAC}\frac{R_{Fn}}{R_{Gn}} \end{cases} \quad 34)$$

where the resistors with sub-index p correspond to the amplifier with the positive slope and sub-index n would to the negative amplifier part.

A first step in the design has been to take a 3.3V reference voltage, allowing the removal of part of the resistors on the positive amplifier. This leads to $R_{Fp} = R_{Gp}$ and the other term $(1 + R_{Fp}/R_{Gp})$ =2 in the v_{DAC} term, being automatically set without making necessary the use of the voltage divider of R_{2p} and R_{1p}. Analogously, for the negative amplifier, a similar procedure can be followed to implement the desired transfer function. As v_{DAC} slope following equation

34) requires a gain of -2 in the inverting input section, this establishes that $R_{Fn} = 2R_{Gn}$, and $(1 + R_{Fn}/R_{Gn})$ = 3. In contrast to the positive amplifier, the gain at the non-inverting input obliges the driver to be set to $R_{1n} = 2R_{2n}$. Taking resistors in the order of tens of kΩ, the set of resistors chosen is summarized in Table 4.18:

Table 4.8: Resistor values for the offset driver in ohms

Element	R_{Fp}	R_{Gp}	R_{1n}	R_{2n}	R_{Fn}	R_{Gn}
Resistance	10 kΩ	10 kΩ	20 kΩ	10 kΩ	20 kΩ	10 kΩ

In contrast with the bandwidth and noise trade-off for the high-speed driver stage, the offset driver bandwidth should be reduced as much as possible, letting only DC frequencies to pass through. Fig. 4.22 shows the modification on the schema which allows to filter both inputs.

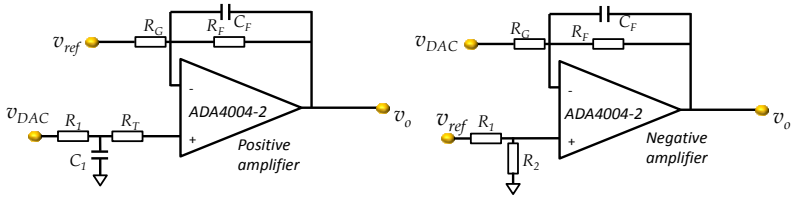


Figure 4.22: Schema of the offset driver with the capacitors

The differences between both schemas reside on the fact that v_{ref} does not require to be filtered twice since it comes from a filtered source. Calculating the transfer functions in AC aims to prove that not any capacitor value added on the feedback branch provides an efficient manner to filter the noise. The AC response of the offset amplifier is shown in 35)

$$\begin{cases} v_{of+}(p) = v_{DAC}\left(1 + \dfrac{R_{Fp}}{R_{Gp}(1 + R_{Fp}C_{Fp}p)}\right)\left(\dfrac{1}{1 + R_1C_1p}\right) - v_{ref}\dfrac{R_{Fp}}{R_{Gp}}\left(\dfrac{1}{1 + R_{Fp}C_{Fp}p}\right) \\ v_{of-}(p) = v_{ref}\left(\dfrac{R_{2n}}{R_{2n} + R_{1n}}\right)\left(1 + \dfrac{R_{Fn}}{R_{Gn}(1 + R_{Fn}C_{Fn}p)}\right) - v_{DAC}\dfrac{R_{Fn}}{R_{Gn}}\left(\dfrac{1}{1 + R_{Fn}C_{Fn}p}\right) \end{cases} \quad 35)$$

It can be noticed when developing the expressions in 35) that both inputs become filtered by the effect of C_F, but unavoidably a zero appears at the non-inverting input, which is mostly critic for DAC unfiltered output of the positive amplifier, where an extra pole is needed to filter it, due to the influence of the undesired zero. The frequencies of the poles for the negative amplifier are

$$f_{pole\_n} = \frac{1}{2\pi R_{Fn}C_{Fn}}\ ,\ f_{zero\_n} = \frac{1}{2\pi(R_{Fn}||R_{Gn})C_{Fn}} \quad 36)$$

and for the positive amplifier are:

$$f_{pole\_p} = \frac{1}{2\pi R_{Fp}C_{Fp}}\ ,\ \frac{1}{2\pi R_1C_1},f_{zero\_p} = \frac{1}{2\pi(R_{Fp}||R_{Gp})C_{Fp}} \quad 37)$$

As the frequency corresponding to the zero is dependent on the pole, the only requirement in case of the positive amplifier is to set the second pole f_{pole_p} at least one decade below f_{zero_p} producing an effective filtering effect for the DAC. Selecting a C_F= 100 nF, creates a pole at f_{pole_n} = 79.5 Hz and f_{zero_n} = 238 Hz, while this last affects only the v_{ref}. For the positive

amplifier, a similar approach leads to f_{pole_p} = 159 Hz and f_{zero_p} = 318 Hz, making the pole f_{p1} < 31.8 Hz. Again, selecting C_1=10 µF, locates the pole at 1.59 Hz reducing notably the noise at this part. The values of R_T=1 kΩ and R_1= 10 kΩ have been selected in order to avoid the connection of a capacitance at the input nodes, which produces an unstable behavior.

Common-mode voltage and reference voltage distribution

The internal 1.5 V voltage reference of the FADC has been used as a clean reference. However, as the number of devices to supply the reference is large and the internal reference can only deliver 4 mA, buffering and amplification becomes necessary to prevent voltage drops. A voltage reference amplifier, built using the ADA4004-2 is proposed in Fig. 4.23 to provide the 3.3 V, applying the filtering methods used for the offset drivers. The voltage gain now becomes $G_{COM} = 1 + R_F/R_G$, so we obtain a gain of 2.2. Choosing R_G=10 kΩ makes R_F=12.2 kΩ whilst the values for the rest of components are C_F=100 nF, C_1=10 µF, R_T=1 kΩ and R_1= 10 kΩ.

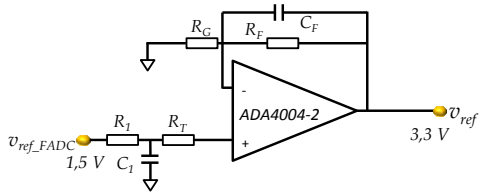


Figure 4.23: Reference voltage amplifier topology

Another important point is the voltage reference distribution, grouping all circuits which are power-supplied by the same regulator and reference-supplied by the same FADC, avoiding the noise on one of the groups to create an influence on other groups. Fig. 4.24 shows the distribution process for both groups, taking the ADC reference source and its amplified version used for the DACs and the offset amplifiers. Therefore, the power regulator which supplies the FADC 1 generates a common voltage of 1.5 V, used to rise the common level up to this voltage for channels 1 and 2. Afterwards, the amplified 3.3 V taken from this source also delivers the references to the channels 1 and 2, closing the loop. Similarly, the same strategy is performed to supply the FADC 2 chip, whose reference delivers their corresponding references to channel 3 and 4.

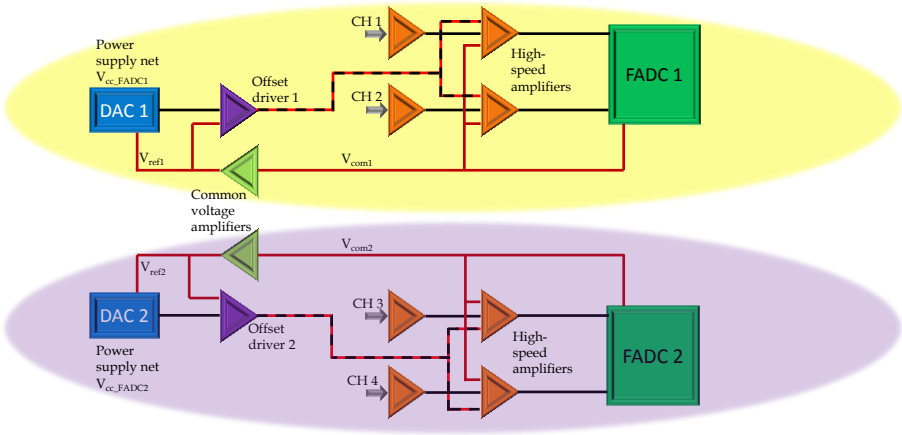


Figure 4.24: Distribution of the reference voltages across the FADC Mezzanine, showing the voltage groups

4.5. Analog interface design

According to the general layout in Fig. 3.3, NUMEXO2 digitizer and the FADC Mezzanines are placed 10m away from the detector and front-end electronics, requiring a physical connection between both parts. Due to the fast nature of the signals, a connection with a good transmission at high frequencies is required. With such purpose, a testbench has been developed to characterize a set of different cables and determining the best solution applying bandwidth, crosstalk and EMI tests. Two items need to be selected, namely the connector and the cable itself. The cable connector selection determines also the mezzanine connector and, therefore, mechanical constraints have to be considered. Since this chapter covers the design of the FADC Mezzanine, this section is introduced due to the fact that the input connector is placed on the Mezzanine, but the election of a cable is considered as a part of the global design, and, therefore, the details concerning the tests and results are covered more extensively in Annex A.

In conclusion, the results obtained in the test, shows the necessity to use the HDMI cable. For EXOGAM2 is sufficient to use the HDMI v1, since it provides a good response for 30 MHz, a good crosstalk and EMI results for a reasonable economic and light cable, being the case completely different for NEDA, which requires the use of the v1.4 Infinite. Nevertheless, the choice of any of the two HDMI versions does not make a difference on the FADC Mezzanine design since the PCB connector is the same.

4.5.1. Interface FADC Mezzanine to the front-end electronics using the HDMI connector

The HDMI connector used contains 19 pins, consisting of 4 groups for high-speed signal transmission lines, containing a differential pair and its grounding, and a set of 7 single-ended signals, which remain unused for our application.

The pin assignment for the HDMI connector is strongly dependent on the placement of the analog stages, which at the same tine depend on the board-to-board connectors and ADC placement. Details concerning the component placement are given in section 4.9.3. Table 4.9 summarizes the pin placement of the HDMI connector, where the 4 differential pairs (pins 1-12) have been assigned to each channel respectively, while the rest (13-19) since remain unused, have been connected to GND.

Table 4.9: HDMI connector pin assignment

Pin number	Pin net	Pin number	Pin net
1	Channel 1 (-)	11	GND
2	GND	12	Channel 4 (+)
3	Channel 1 (+)	13	GND
4	Channel 2 (-)	14	GND
5	GND	15	GND
6	Channel 2 (+)	16	GND
7	Channel 3 (-)	17	GND
8	GND	18	GND
9	Channel 3 (+)	19	GND
10	Channel 4 (-)		

4.6. Slow control design

Several active devices require a specific setup based on SPI or μWire control protocol. Additionally, while some devices require writing certain parameters in the registers to work, others such as the DAC operate mainly as a response to the commands of delivering a voltage. As the result of the slight differences between the protocols and working modes, it has veen necessary to perform a compliancy study.

4.6.1. Interfacing the FADC with a master device

A total amount of 9 SPI lines are used for the Mezzanine SPI control, using a common SPI CLK and data in/out pins, and 6 dedicated pins for the chip enable signals. Additionally, 2 extra control lines (RESET_FADC and SYNC*) are used as extra signals out of the SPI standards. In this sub-section only issues concerning the hardware design are described in detail, keeping the differences at the firmware level to be discussed in chapter 5, in the firmware section.

While the logic voltage levels are compliant among all the devices, this cannot be applied to the maximum current require for the SPI CLOCK and Data-in signals, therefore, it is mandatory to increase the fan-out current, requiring the use of current drivers. A second fact which justifies the use of drivers is the Data-out signals, not necessarily references to high-impedance, hence, encouraging the use of tri-state devices for the readout management. The chips SN74LVC2G126 (high-enabled) and SN74LVC2G125 (low-enabled) [89] offer both the current buffering and the tri-estate functionality. Fig. 4.25 shows the logic driver connections, splitting the SPI CLK and SPI DATA IN in two groups to relieve the fan-out effects and the readout connections.

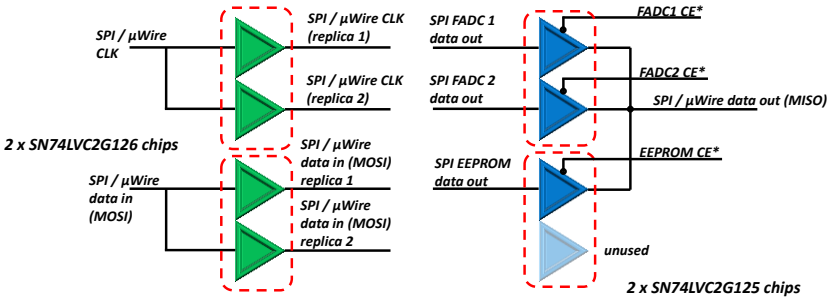


Figure 4.25: Connection of the logic tri-state drivers for readout and current supply.

The grouping of all the control lines and logic drivers forms the full slow-control block diagram, shown in Fig. 4.26.

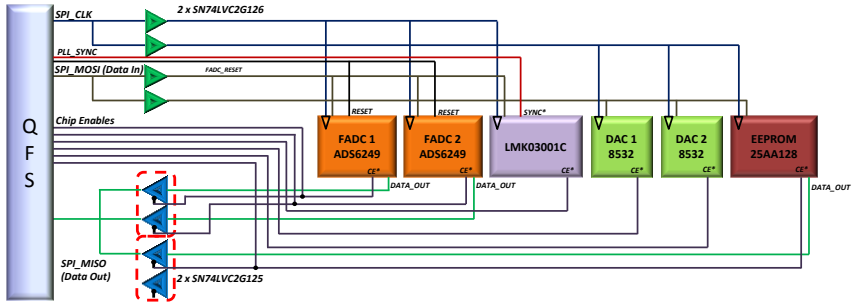


Figure 4.26: FADC Mezzanine control block diagram, including the programmable chips, logic drivers

4.7. FADC Mezzanine – NUMEXO2 interface design

The interface between the FADC Mezzanine and NUMEXO2 motherboard is done by using high-speed board-to-board connectors, where bit rates up to 500 Mbps are transmitted. The signals can be grouped as it follows:

- 28 LVDS ADC data pairs (56 high-speed lines).
- 2 LVDS output clocks (4 pins).
- 1 LVPECL clock input (2 pins).
- 9 signals for the SPI control (SPI_CLK, MISO, MOSI 6 chip enable).
- RESET FADC + PLL SYNC (Extra control signals, 2 pins).
- 4 different power supplies.
- 4 extra differential pairs reserved for a future use, called “NEDA extra pairs”.
- Ground signals for the rest of unused pins.

Summing up, a total amount of 81 signals are needed. Two different connectors from SAMTEC have been proposed to provide a solution:

- FMC LPC connector ASP-134603-01 from SAMTEC, used on the ML605 evaluation board. It is provided with 160 pins along 4 rows.
- QFS-026-04.25-L-D-PC4 [90], from SAMTEC. Each mezzanine will require at least two of them. This connector is provided with 52 signals pins and 8 thicker power pins.

Due to the mechanical unsuitability of the FMC connector, the choice has been the QFS connector from SAMTEC. The second task consists of distributing the signals optimally, but this task has been rearranged several times during the PCB design until the optimal solution was found. Nevertheless, some guidelines to achieve an optimal solution are:

- Grouping of the differential outputs within a channel in the same region.
- Addition of ground pins between a high-speed differential signal and a single-ended low-speed signal, isolating low-speed signals from the high-speed data fast edges.
- Power supply delivery through the dedicated thicker pins.

Taking into account the conditions mentioned above the signal pin-out has been established as follows.

- The LVDS data signals groups are placed on the connector extremes, each of them in a different side. The final pin-out shown in Fig. 4.27 was selected after the ADC placement during the PCB design.
- SPI signals left in the connector center, leaving a set of GND pins in between.

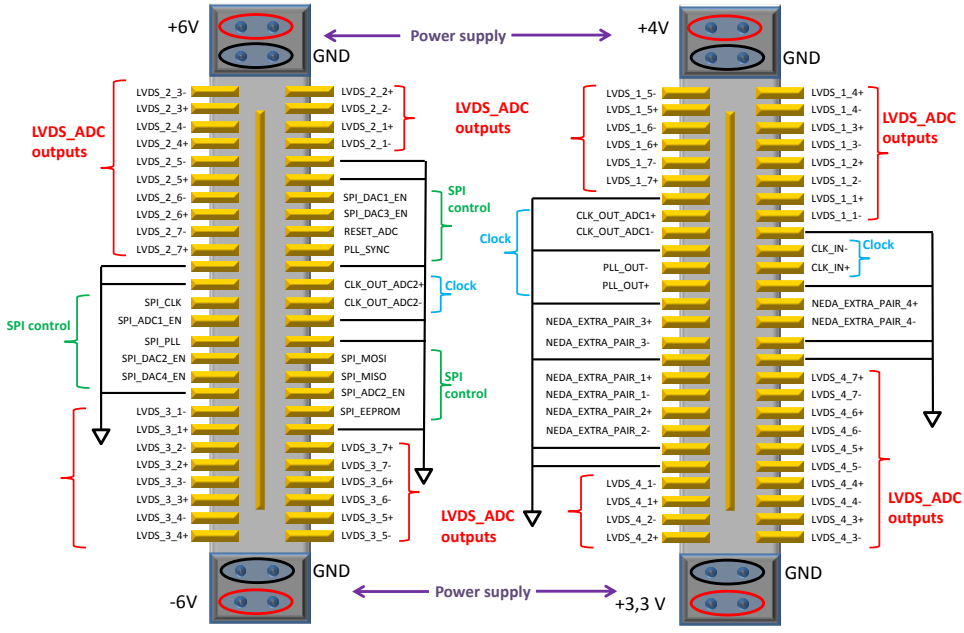


Figure 4.27: QFS-026-04.25-L-D-PC4 connector pin-out

4.8. Power supply design

The choice of an appropriate power supply design stage makes an important role on the design of mixed electronic systems, involving the study of power demands, as well as the influence of noise on the A/D conversion. Hence, the use of LDOs (Low-Dropout voltage) voltage regulators combined with optimal power distribution techniques are necessary when designing high-speed acquisition systems.

4.8.1. Study of the device power requirements

Input power supply is provided through NUMEXO2 by the QFS connectors, where 4 different power supplies are obtained through specific thicker pins envisaged for power transmission. The power sources are the following:

- +6 V, provided directly from the NIM power supply.
- -6 V, provided directly from the NIM power supply.
- +3.3 V, provided from the PTH08000WAH DC/DC converter, placed in NUMEXO2 board.
- +4 V, provided from the PTH08T230W DC/DC converter, placed in NUMEXO2 board.

Within a bank, 2 pins drive the power supply while the other 2 are used as a ground connection. Once the input voltages are known, the next step consists of analyzing how much power does each device require.

ADAS62P49 FADC power supplies

Power supply distribution on the ADCs is a critical matter, where each ADC uses its own LDO for the analog power supply, while the digital power supply may be shared using only a common LDO. In expression 9) it is shown the contributions for the maximum power consumption for 250 MHz, rising up to 2.5 W when 2 devices are operating.

LMK03001C power supply requirements

Power consumption of this device is strongly dependent on how many outputs are enabled and how they are configured. For our case, assuming that we are using 2 LVDS outputs, and based on the most restrictive configuration pattern (delayed and divided output), the power estimation proceeds as follows:

$$P_{PLL} = V_{CC}\left(I_{core} + I_{buff_{LOW}} + 2I_{LVDS} + 2I_{delay\_divided}\right) = \\ 3.3V\left(86\,mA + 9mA + 2 \cdot 17.8ma + 2 \cdot (8.5mA + 9.9mA)\right) = 533.74\,mW \quad 38)$$

LMK03001C needs its own, isolated from the ADC analog power supplies due to the big amount of noise introduced by the high-speed clocks. However, the power distributed is shared to the logic current drivers SN74LVC2G125/6.

DAC 8532 power supply

DAC devices, even though their consumption is much lower than the PLL and the ADCs, require a clean power supply to preserve the resolution. As it was seen in section 4.4.6 (Fig. 4.29), each DAC shares its power net with the corresponding ADC in which the same

channel/s is involved. Hence, the LDO supplying the analog ADC voltage can be used to supply the DAC only if they contain the same acquisition channels. The total power consumption for the DACs is:

$$P_{DAC} = I_{CC}V_{CC} = 0.5\ mA \cdot 3.3\ V = \ 1.6\ mW \quad 39)$$

which, for 2 devices rises up to 3.2 mW.

AD8139 full differential amplifier

Both analog drivers, AD8139 and ADA4004-2 are supplied with a bipolar power supply with ±5 V. According to the datasheets, the total power consumption taking into account all devices is, for the AD8139:

$$P_{AD8139} = 8 * P_{device} = 8I_{CC}(V_{CC} - V_{SS}) = 8 \cdot 24.5mA \cdot \big(5V - (-5V)\big) = 1.96\ W \quad 40)$$

$$P_{AD4004-2} = 7 * P_{device} = 7I_{CC}(V_{CC} - V_{SS}) = 7 \cdot 2.2mA \cdot \big(5V - (-5V)\big) = 154\ mW \quad 41)$$

4.8.2. Design of the power supply stage

Based on the device power requirements, a supply schema using a set of LDOs and the input voltages has been proposed. The selected devices for our application are the fixed-voltage LDOs from the family TPS796XX [91] from Texas Instruments, where the last two digits, marked as "*XX*", indicate the output voltage (in hundreds of millivolts). The choice of fixed-voltage regulators was preferred due to its higher accuracy and the lack of need for external network resistor tolerance, which is specially critical for the ADS62P49 device and DACs. In case of the negative voltage regulators, the choice was the LT1175-5 [92], a fixed-LDO set to -5 V. A general law to design power supply systems based on LDOs is to take the desired output voltage the closest possible to the value $V_i - V_d$, where V_d is the minimum drop-out voltage, which for the TPS796XX family is 330 mV, minimizing the power dissipated in the regulator. The power supply schema is depicted in Fig. 4.28 drafting a topological view.

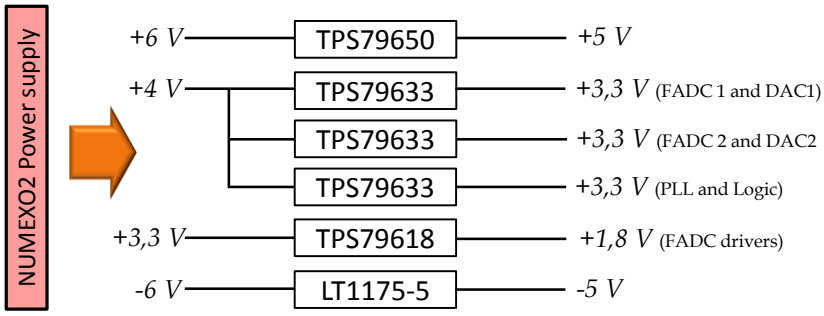


Figure 4.28: Power supply topologic schema

The contributions from all the device power consumption are gathered in table 4.10.

Table 4.10: Power dissipation in the LDO devices

Device	*Vi*	*Vo*	*Io*	*Pd=Io(Vo-Vi)*
TPS79650	+6	+5	196 mA (AD8139) + 15.4 mA (ADA4004-2)	211.4 mW
TPS79633 (FADC1)	+4	+3.3	330 mA	231 mW
TPS79633 (FADC2)	+4	+3.3	330 mA	231 mW
TPS79633 (PLL, Dig.)	+4	+3.3	161 mA	116.9 mW
TPS79618	+3.3	+1.8	266 mA	400 mW
LT1175-5	-6	-5	196 mA (AD8139) 15.4 mA (ADA4004-2)	211.4 mW

The total power dissipated only inside the LDOs rises up to 1.4 W.

Total power estimation

Summing all the power contributions from all the main devices and the dissipation inside the LDOs, the total power rises up to:

$$P_{TOTAL} = P_{ADC} + P_{PLL} + P_{DAC} + P_{AD4004-2} + P_{AD8139} + P_{d\_LDO} = \\ = 2.5W + 533.74\,mW + 6.4mW + 154mW + 1.96W + 1.4W = 6.55W \quad (42)$$

Thermal considerations

Given the noticeable power dissipated at the LDOs, it is important take care of the package and PCB heat dissipation guidelines, minimizing the chip overheat. Based on the generic thermal resistance expression (43):

$$T_J - T_A = \theta_{JA} P_d \quad (43)$$

where T_J and T_A are the junction (chip) and ambient temperatures respectively, P_d is the dissipated power and θ_{JA} is the junction-ambient package thermal resistance in ºC/W. From the values obtained in the table 4.11, and establishing that is, the different cases for different packages are:

Table 4.11: Comparison of different thermal resistance packages.

θ_{JA} [C/W]	DRB / S8	DCQ	KTT / Q	DIP	T	ST
TPS796XX	47.8 - 80	70	25	-	-	-
LT1175-5	60-100	-	27 - 60	80-120	50	50

Considering the most demanding requirement, which is for the TPS79618, consuming a total power of 400 mW only at the LDO, and choosing the DCQ package with a θ_{JA} = 70 ºC/W, to burn the chip at T_J = 125ºC, it would be necessary to have a power consumption of 1.42 W, more than 3.5 times the maximum estimated power. Taking 400 mW for a DCQ package, in the worst case, leads to a maximum temperature increase of 28ºC. For the LT1175-5, dissipating 211 mW, it was preferred a solution using the S8 package combined with proper layout techniques aimed to distribute the heat across the board, which for the S8 package (60-70 ºC/W) leads to a maximal temperature increase of 15º.

Improved ripple rejection performance considerations and power supply filtering

Another common parameter in LDO design is the "Ripple Rejection Ratio", which measures the regulator robustness at the output against input voltage variations. Fig. 4.29 shows an example for the TPS796XX LDO series, providing good performances at low frequencies (60 dB) which degrade as the frequency increases. The point at which the ripple rejection starts to degrade is 10 kHz, and beyond this value, the high-frequency components may be transferred across the LDO increasing the noise in the power supply of critical components.

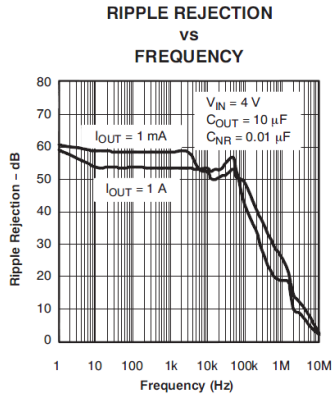


Figure 4.29: Example of TPS796XX Ripple Rejection frequency-domain curve [91]

Minimizing the degradation of the ripple rejection ratio at higher frequencies can be achieved by means of a low-pass LC filter or π filter, used to reduce the high-frequency components that the LDO cannot remove. A common design criterion is to set the filter cut-off frequency lower than the frequency at which the LDO rejection ratio starts to degrade, which for our case is approximately 100 kHz. In order to avoid a deregulation of the delivered voltage caused by the series resistance of the inductor, the low-pass filter is placed before the LDO.

The inductor

For designs on power supply filters, as it is the case, not only the nominal inductance but also the series resistance and the maximum current make an important role on the choice of the inductor. Setting the filter cut-off frequency one decade before the LDO Ripple-rejection elbow, close to 10 kHz, and the C = 100 µF, leads to an inductance value of 1 µH using expression 44):

$$f_{cut\_off} = \frac{1}{2\pi\sqrt{LC}} \qquad 44)$$

These requirements motivated the choice of the inductor MLZ2012A1R0WT [93] from TDK, a 1 µH SMD-based inductance capable to admit a maximum current of 900 mA with a series resistor of 0.1 Ω enough to avoid a high drop voltage but still considerable to produce a damping effect on the resonance produced by the LC network. Other interesting features of this component are its small 0805 SMD package and its self-resonance, set at 160 MHz, which still warrantees an inductive behavior at the frequencies of interest. Figs. 4.30 and 4.31 show the simulation model in LTSpice IV and the frequency response results for the designed filter.

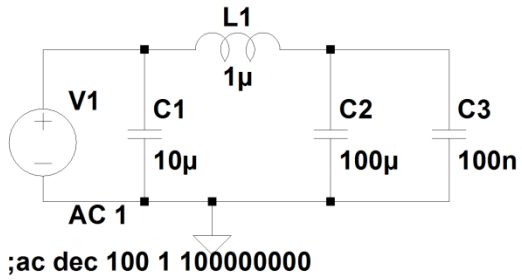


Figure 4.30: Simulation model of the power supply filter

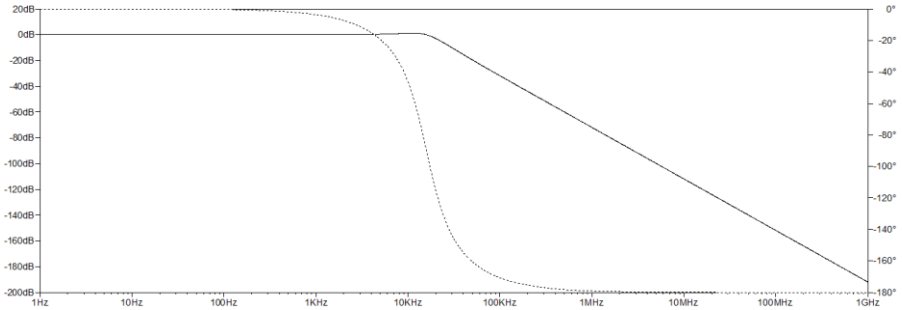


Figure 4.31: Simulated filter frequency response

The magnitude Bode plot shows the cut-off frequency close between 10 kHz and 20 kHz, with a -40 dB/dec slope and the damped resonance caused by the inductance series resistor of 0.1 Ω.

4.9. Physical design and PCB layout

This sub-chapter focuses on the FADC mezzanine PCB design and board layout, providing as well a brief outline about criteria to be adopted for the optimal design of high-speed systems, as well as the component placement and optimal stack-up.

4.9.1. Board size specifications

FADC Mezzanine dimensions are constrained among others by the NUMEXO2 card dimensions based on a NIM crate and the placement of certain critic devices onto the motherboard such Virtex-6, Virtex-5, the board-to-board connectors and the front-panel connectors.

- NIM crate width dimensions restrict the FADC Mezzanine y-axis dimension. Additionally, this size should be reduced since a short gap must be left between Mezzanines.
- NUMEXO2 front panel is provided with a set of LEMO connectors to be used as test outputs for the EXOGAM2 new front-end electronics. This obliges to slot the Mezzanine corners at the front-panel side, as depicted in Fig. 4.32.

- QFS connectors must be placed as close to the front panel as possible, aiming to ease the carrier motherboard routing.

Taking the NIM width (183 mm) and setting the gap between Mezzanines to 1-2 mm, the width was limited to 42 mm. Then, even though there is more freedom to choose the length, an optimal mechanical symmetry along the QFS connectors sets the Mezzanine length to 98.5 mm. In Fig. 4.32 it is shown the NUMEXO2 dimensions including the FADC Mezzanine size while being plugged in. Additionally, the already mentioned shape irregularity due to the inclusion of LEMO connectors, removes a total area of 9 x 16 mm on each front-panel corner,

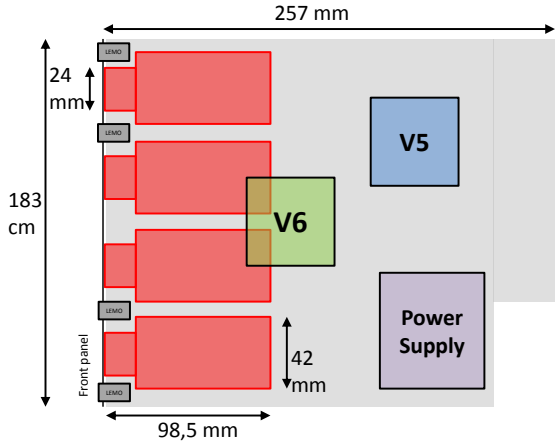


Figure 4.32: NUMEXO2 physical dimensions, containing its main elements

4.9.2. Stack-up

The decision on the stack-up is based on how many layers would be used as routing layers and the number of power supplies, as well as considerations of influence between the analog and digital circuitry, and high-speed transmission line modeling.

Therefore, beginning from the fact that high-speed traces are placed on the external layers minimizing hence the number of vias, five routing layers and three power planes are necessary given the board size and the high number of differential traces. The distribution of ground and power planes was done considering the number of layers used for high-speed signal transmission, requiring an adjacent plane to achieve microstrip and stripline structures. Finally, a total amount of 12 layers was required, obtaining the structure shown in Fig. 4.33. Referring the layer 1 as 'TOP' and 12 as 'BOTTOM', high-speed traces fall within these extremes, adding the layer 8 and 10 for high-speed clocks and high-speed analog traces minimizing the influence from the digital traces to the analog lines. Ground planes are then placed in layers 2, 7, 9 and 11. In contrast, whereas critical signals such as high-speed traces have been carefully placed in priority, power planes and low-speed signals were left for the remaining space in the stack-up center.

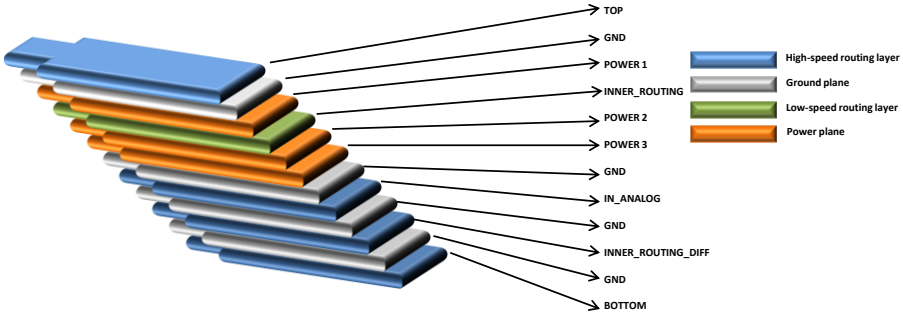


Figure 4.33: FADC Mezzanine stack-up

4.9.3. Component placement

The FADC Mezzanine component placement obeys a straightforward design, only retained by the critical position of the connectors. Hence, the HDMI connector is placed next to the front panel, followed by the analog stage, the ADC immediately afterwards and the QFS connectors on the bottom side the closest possible to the front panel, minimizing hence the signal path. The HDMI connector must be placed on the bottom side in order to make the screwing accessory compliant with the NIM dimensions, avoiding obstacles in the crate. Fig. 4.34 shows the cross-section details, which shows the obvious unsuitability of the HDMI connector being placed on the other side.

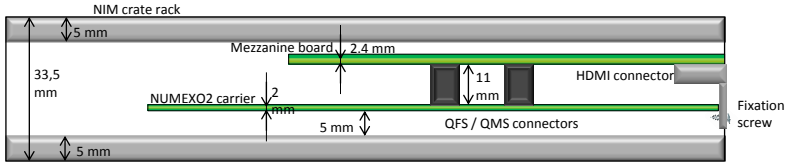


Figure 4.34: Detail of the NIM rack cross-section, including NUMEXO2 carrier and the FADC Mezzanines

Regarding the placement of the QFS connectors, the optimal way is their vertical arrangement after the analog amplifiers, concretely at 42.29 and 57.29 mm away from the front panel side. However, connector optimal placement is linked to the FADC chips placement, where exploiting the symmetry placement strategies, the length-matching of the data output lines becomes more straightforward without any need of extra area for serpentines. In Fig. 4.35 the symmetry features is displayed.

The rest of components, such as the PLL, DACs, EEPROM, logic drivers and LDOs, it has been preferred to place them on the right side of the FADC, optimizing the datapath placement and routing. Some guidelines for placing these components are the short traces required for the sampling clocks, where the PLL is placed next to the ADCs, and the DAC device placement, placed in the same region as the corresponding channel they drive. Finally, once the ADC placement has been decided, the analog amplifiers are placed close to the ADC as it is shown in Fig. 4.36, providing also the definitive connector pin-out shown in Fig. 4.27.

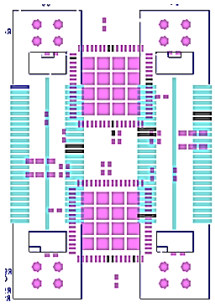


Figure 4.35: Symmetry between the FADC chips (pink, placed on the TOP layer) and the connectors (blue, place on the BOTTOM layer) improves and simplifies the routing and adjustment of the high-speed traces.

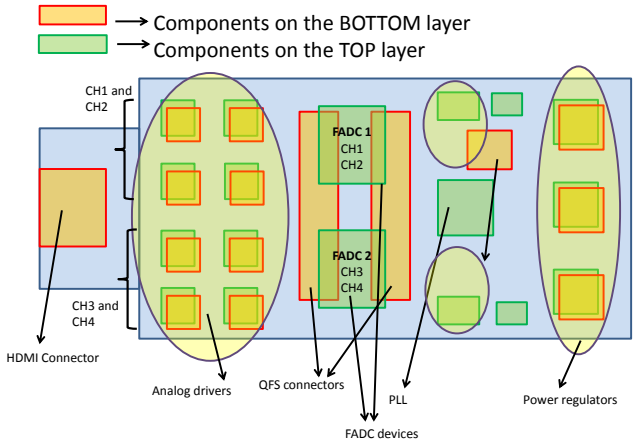


Figure 4.36: Descriptive schema regarding the placement of the main components on the FADC Mezzanine

4.9.4. Routing considerations

Groups of differential lines carrying high-speed data in parallel require of length-matching in order to properly synchronize the signals at the receiver. In addition, the differential impedance must be matched to 100 Ω. Taking the FR-4 electric relative permittivity ε_r= 4.5, copper thickness '*t*' = 35 μm, and the use of tightly-coupled differential pairs, the following expressions have been used to design the differential traces [94].

$$Z_{d\_microstrip} = \frac{174}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98d}{0.8W + t}\right)\left(1 - 0.48e^{-0.96\frac{S}{d}}\right) \quad 45)$$

$$Z_{d\_stripline} = \frac{120}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2d + t)}{0.8W + t}\right)\left(1 - 0.347e^{-2.9\frac{S}{2d+t}}\right) \quad 46)$$

to achieve a differential impedance of 100 Ω. Table 4.12 shows the microstrip and stripline values used for the inner and external layers.

Table 4.12: Differential trace parameters selected for external and internal layers

	Microstrip (TOP / BOT)	Stripline (Inner layers)
W(mm)	0.17	0.12
S(mm)	0.12	0.22

At 500 Mbps (the maximum data rate provided from the FADC), the duration of the data signals is 2 ns. The distance a wave can run across the microstrip in 2 ns is $"l = \frac{v_p}{\sqrt{e_r}} = 28.98\ cm"$. Taking the longest trace as a reference, which is 13mm, and selecting a tolerance of 1% (0.13 mm) between traces, means that the wave requires 0.89 ps in order to travel 0.13 mm. This difference in time is less than 1/2000 fraction of the period, which is negligible for our case. Nevertheless, the adjustment of FADC clock output phase can offer an extra degree of freedom, allowing the adjustment of the phase depending on the sampling frequency.

Moreover, further layout guidelines are the stray capacitance at the input of the FDAs which appears from both input nodes to the common terminal. Stray capacitance might produce ringing and affect the closed-loop performance. Minimizing the parasitic effect can be achieved by removing the copper area under the input pads in all layers. Another recommendation is to use sufficient amount of ground vias in order to guide properly the current return path in multi-layer boards. Specially, in the surroundings of the FADC chips, the digital outputs are traced unavoidably close to the analog input trace. When such a circumstance happens, it is of extreme importance that the return current paths are correctly guided using the return ground vias, avoiding to drive the current through an undesired path. Fig. 4.37 shows a screenshot with the implementation mentioned above, taken directly from the PCB design.

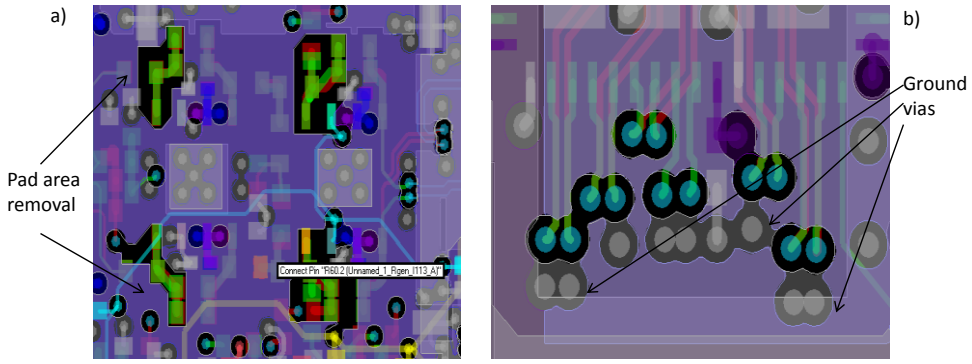


Figure 4.37: a) Stray capacitance reduction by pad area removal. b) Addition of return ground vias to minimize the current spreading effect alongside the board.

4.9.5. Manufacturing

The FADC Mezzanine prototypes have been produced in Spain. The company in charge of the PCB production is Lab-Circuits, from Barcelona, while the assembly was performed by Teydisa, in Madrid. During the manufacturing, differential impedance, quality of the dielectric material, metallization, as well as the board class was taken into account.

PCB manufacturing is performed using FR-4-based cores surrounded by a selectable thickness copper layer on both sides and a gluing material called '*prepeg*' to ensemble them. For our design, a set of 5 cores equally distributed in terms of weight across the symmetry center are used, taking into account a balanced weight distribution, equaling the copper thicknesses across the PCB vertical symmetry center, as it is depicted in Fig. 4.38.

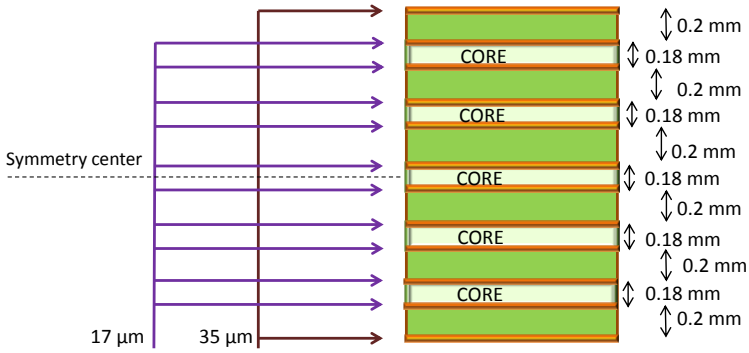


Figure 4.38: Detailed cross-section view of the FADC Mezzanine PCB

Given the amount of components and an estimation of the number of traces and vias, the FADC mezzanine manufacturing class belongs to the class 7 according to the Lab-Circuits standards [95] with the following restrictions. Fig. 4.39 shows a picture of the final prototype.

- Via drill and via size of 0.2 mm, with a surrounding metal 0.1 mm crown for external and 0.125 mm for internal layers.
- Minimum trace width and gap separation. For external traces with a 35 µm copper thickness, the minimum trace is 0.1mm while for 17 µm it reduces to 0.075 mm.

Figure 4.39: Picture of the FADC Mezzanines. Up) Top view. Down) Bottom view

4.10. Review of early prototypes and corrections

FADC Mezzanine final performance has not been obtained at the first attempt. Most of the problems related to noise are specially difficult to observe their sources of origin, where four prototype versions were required to achieve to the final design. Obviously, the version history

attached in this section stands for a brief overview regarding how the prototypes were improved step by step, observing the problems and solutions adopted. Table 4.13, summarizes the prototypes we were testing and the production and the issues encountered which encouraged us to move to a new version.

Table 4.13: Mezzanine versions. Production dates and issues encountered

	Production date	Issues encountered
Mezzanine V1	November 2011	Bad resolution in the whole FADC range
Mezzanine V2	July 2012	Bad resolution for certain offset values
Mezzanine V3	February 2013	Bad resolution for certain offset values
Mezzanine V4	July 2013	Bad resolution for certain offset values. Found a pattern to improve the noise for these values
Mezzanine V5	November 2013	Final version

4.10.1. Reviews on the first prototype

The reasons which encouraged the redesign of an improved version of the mezzanine are mostly related to the bad noise resolution. The measurements have pointed out that the source of the noise comes from a badly-designed analog driver stage. Hence, the changes from the first to the second prototype involve the most notorious changes to the mezzanine due to the implementation of different analog stage based on a combined topology of CFAs and FDAs, differing device used as well. The amplifier chosen is the CFA AD8002 from analog devices, in which the analog circuit structure was divided into three different parts: a voltage follower, a control amplifier to control the gain and offset, and a last full-differential amplifier thought to balance the differential signal and provide the V_{com} voltage. The schema is depicted in Fig. 4.40.

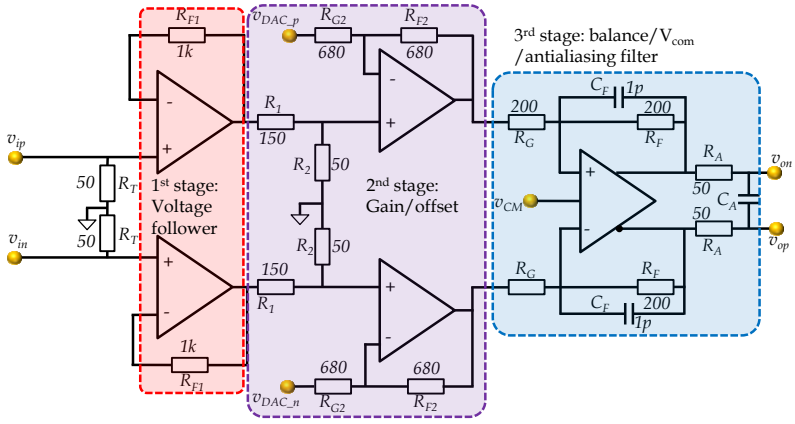


Figure 4.40: High-speed stage for the first Mezzanine prototype

Among the most important details about this circuit, we can focus on is the gain resistors, set by R_1 and R_2, and the offset input provided via the second stage with 680 Ω resistor in order not to destabilize the CFA [76]. In case of the AD8002, optimal noise performance is obtained for a unitary gain on the DAC input, obliging a gain reduction of 0.3 in the intermediate stage, in order to convert from ±3.3V to ±1V. Another fact is the use of a different OpAmp model, the AD8662 from Analog Devices, less optimal in terms of noise than the ADA4004-2.

Noise measurements showed a noise contribution worse than the expected, with σ_{noise} > 2.6 ADC counts, larger than specified regardless the channel and sampling frequency. Experiments a), b) and c), shown in Fig. 4.41 revealed that the FADC nor the AD8139 were the noise main sources, obtaining a dramatic noise increment when measuring the AD8002 CFA. The evidence was confirmed by bypassing the follower stage (1st stage based on AD8002) to the AD8139 (Experiment g). The subsequent experiments are depicted in Fig. 4.41 while the results obtained for such experiments, expressed in ADC counts, are summarized in table 4.14.

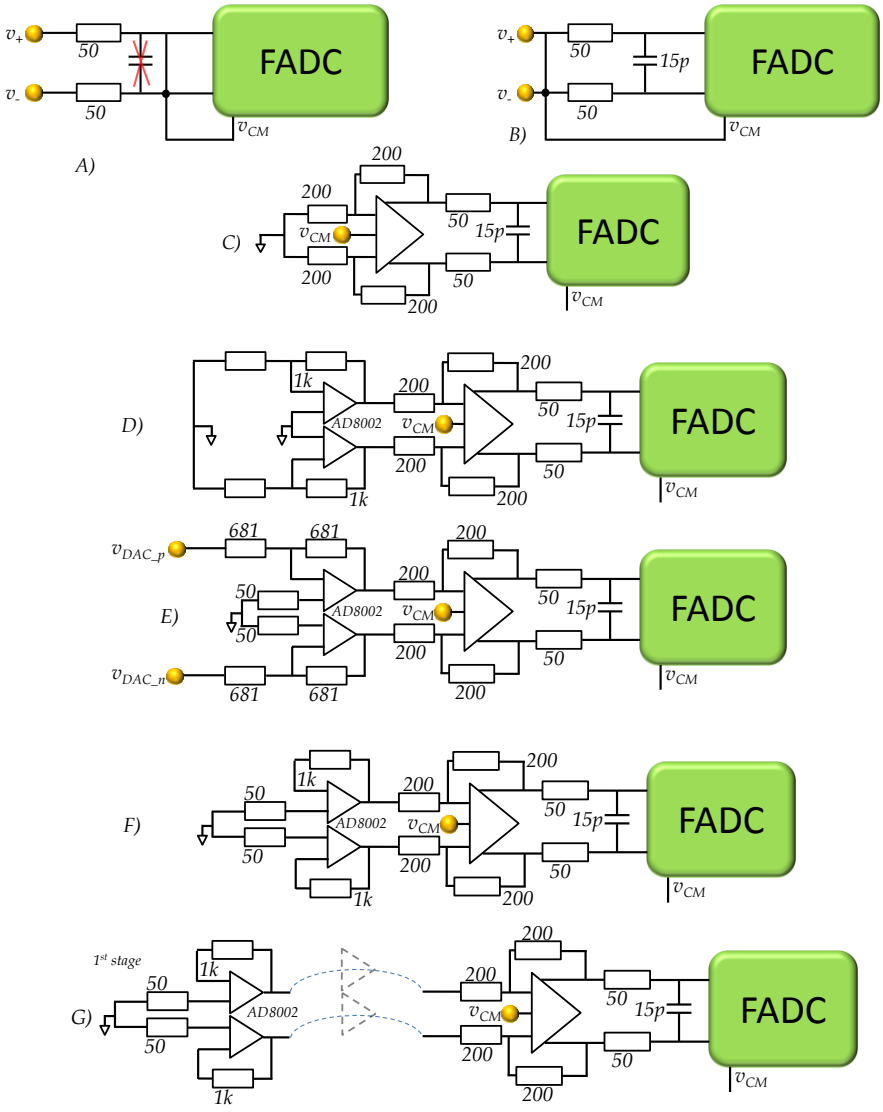


Figure 4.41: Experiments performed to determine noise sources

Table 4.14: Noise tests applied to the FADC Mezzanine version 1 and the noise sigma values

Experiment	$\sigma_{noise}(100\ MHz)$	$\sigma_{noise}(200\ MHz)$
A (FADC)	1.06	1.18
B (A + filter)	1.12	1.13
C (B+ AD8139)	1.38	1.36
D (C+AD8002 second device)	2.32	2.23
E (Include offset input)	2.44	2.62
F (Use 2nd stage as a follower)	2.10	2.00
G (Bypass stage 1 to AD8139)	2.35	2.21

Also, results considering the whole analog stage, including both CFAs per channel have been measured, obtaining even noisier results, as it is shown in Table 4.15.

Table 4.15: Noise tests applied to the FADC Mezzanine version 1 considering the whole analog stage

Channel	$\sigma_{noise}(100\ MHz)$	$\sigma_{noise}(200\ MHz)$
1	2.68	2.91
2	2.76	3.05

Provided the results from Table 4.14 and 4.15, it points out the AD8002 as the source of noise regardless the type of configuration used (follower, gain or gain + offset). Therefore, the research for an alternative analog stage avoiding the use of CFA for its implementation was compulsory.

4.10.2. Reviews on the second prototype

Reaching a new design without any CFA, this stage is based only on fully-differential amplifiers. Concerning the analog stage, the only remarkable difference between this version and the final one is the gain set for the offset stage associated to the resistor attached to the DAC branch. Looking at Fig. 4.42, R_{DAC} was chosen initially to 200Ω, fact which brought the amplifier to instability. Furthermore, new devices were sought for the offset amplifier where a better performance was found out with the ADA4004-2 device, which was substituted on this device by the AD8662 [96]. Tests carried out evaluated the correct behavior of the high-speed amplifier AD8139 without R_{DAC}, confirming the evidence of the impact of R_{DAC} in the high-speed analog stage. This issue was solved when increasing R_{DAC} to 1k32, reducing the influence of R_{DAC} on the overall amplifier gain, although implying as well in higher gains in the intermediate offset driver stage. The resistor of 1k32 was selected due to the ADA4004-2 maximum output voltage (±3.6 V) when supplied at ±5 V. Fig. 4.42 shows the change performed to the analog stage.

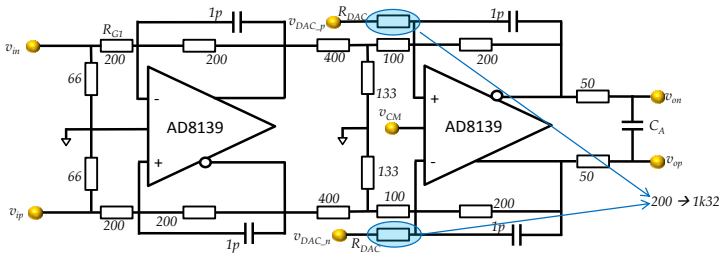


Figure 4.42: Analog stage of the FADC Mezzanine second version, showing the value change on R_{dac}

Unlike the first prototype, this one accomplished the specifications in terms of noise without offset input, reaching resolutions of σ_{noise} = 1.4 ADC counts at 70 MHz bandwidth for 200 MHz sampling frequency. Still, the unification of the offset driver with the high-speed stage did not performed according to the design requirements, fact for which the offset driver was object for a separated research. One of the phenomena which disclosed the problematic behavior of the offset stage is the noise fluctuation depending on the DAC value applied, where results varying from σ_{noise} = 1.4 to σ_{noise} = 2.25 have been obtained. In Fig. 4.43 it is depicted the σ_{noise} dependency on the offset values applied to the high-speed stage, where a particular shape arises showing worse behavior as far as the baseline level moves away from the central position of the FADC range.

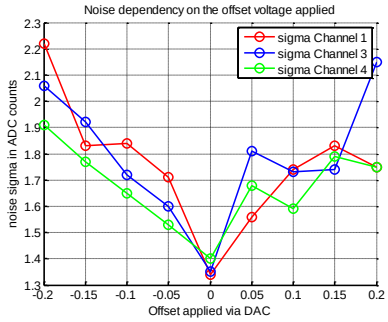


Figure 4.43: Noise dependency on the offset applied to the differential amplifier via the DAC

Among the points which were under study, special emphasis was put on how the voltage references and DAC sources were driven through the circuit, observing that the references were obtained directly from the power planes, foreseeing for the next prototype to obtain the reference sources from the FADC internal voltage reference instead.

4.10.3. Reviews on the third prototype

FADC Mezzanine third version disposed already of a well-design high-speed filter with references taken carefully from clean reference instead of noisier power planes. Despite of the carefulness of this new approach, the behavior in terms of noise of the offset driver did not change much from the previous version. After the tests at GANIL in April 2013, the noise performance was slightly improved for the offset extreme values using filters with low bandwidths, 1 Hz – 100 Hz to all the stages involving the path of offsets and voltage references (Vcom amplifier and offset amplifier). Fig. 4.44 shows the changes made at the level of the offset stage.

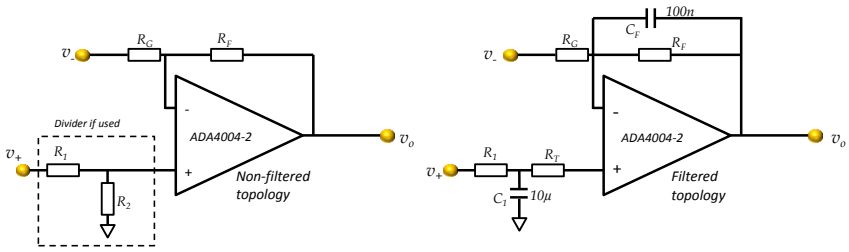


Figure 4.44: Noise performance improvement by filtering the offset stage

4.10.4. Reviews on the fourth prototype

The fourth FADC Mezzanine version was tested in July, 2013, in Valencia, achieving the improved performance not only at the middle level, but also at the ADC extremes (applying the modifications after the tests at GANIL), for which the resolution failed on the third prototype. The reasons for a fifth prototype were envisaged after the experiments using a DC sweep across all the ADC range, where several anomalies were observed, understood and corrected. Unlike the changes among versions performed up to now, the changes from the fourth to fifth prototype only undergo layout modifications.

A more comprehensive test regarding an analysis of the whole dynamic range was due, verifying the same noise performance in the whole ADC range. The experiment consists of splitting the ADC range in several zones - 200 zones for the tests, although it can be adjusted from the testbench platform - and taking a set of 8 windows, where each one contains 32k samples at each zone. Fig. 4.45 shows the results obtained for all four channels at 100 MHz and 200 MHz sampling frequency.

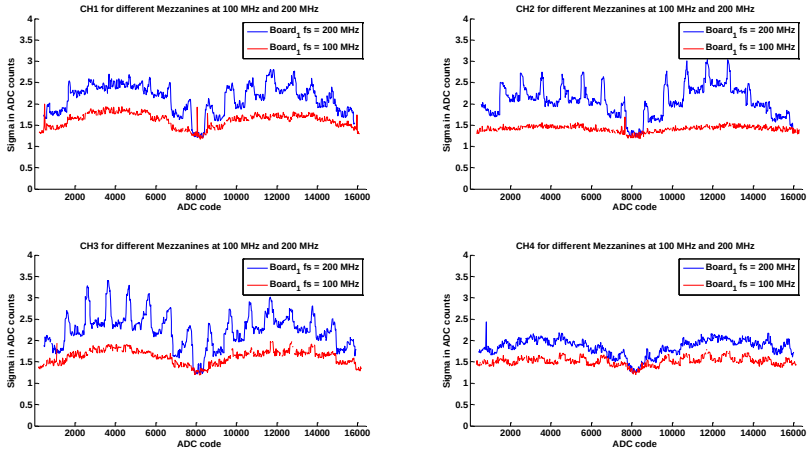


Figure 4.45: Noise performance (expressed in ADC counts) versus the ADC code (expressed in decimal). Each graph makes reference to a measurement obtained for a single FADC Mezzanine both at 200 MHz sampling frequency (blue) and 100 MHz (red)

It can be noticed, especially at 200 MHz sampling frequency, the presence of several peaks at certain codes, being those much smaller at 100 MHz. Besides, it can be also noticed that the baseline average test points used on the previous prototypes, which are 0x2000 (8192), 0x0000 and 0x3FFF (16384) are the ones at which the noise performance is the best, being the most conflictive ones around the points 0x1000 (close to 4000) and 0x3000 (around 12000). However, even if the peaks would not appear, the ADC response obeys a two-lobed shape whose maxima are placed at these conflictive points. Another point to look at is the improved performance of the channel 4 over the rest, on the basis of this evidence, a problem with the FADC component was discarded. Taking these results, several experiments were carried out to observe where the peaks were coming from.

The first experiment compared the noise performance, taking the DC sweep either from the DAC or from a waveform generator. Concretely, for our setup, the arbitrary waveform

generator AFG33522A from Agilent, driving DC voltages with the same step size used for the DAC (200 steps). By performing this experiment, we intended to understand the influence of the offset stage in the design.

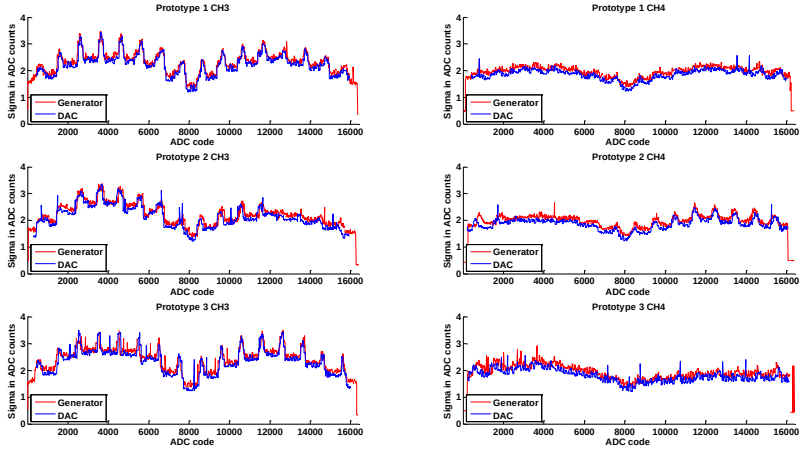


Figure 4.46: Noise performance plots for 3 FADC Mezzanine prototypes, comparing the noise standard deviation using an external signal generator and the internal DAC at 200 MHz.

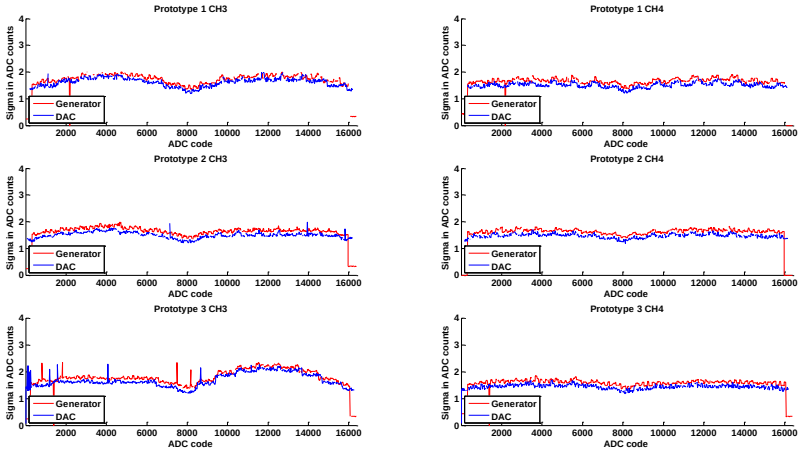


Figure 4.47: Noise performance plots for 3 FADC Mezzanine prototypes, comparing the noise standard deviation using an external signal generator and the internal DAC at 100 MHz.

Figs. 4.46 and 4.47 show the results of the experiment, revealing that peak-patterns are still present no matter what the source is. In case of using the signal generator, the overall noise performance is slightly higher due extra front-end electronics and the HDMI cable contribution. However, the pattern shape follows the same structure regardless of the source origin, discarding hence, the DAC as the source of uneven noise behavior throughout the ADC range.

A second experiment measures the noise performance at different bandwidths. The following experiment performs the same measurement for bandwidths equal to 30, 50 and 100 MHz.

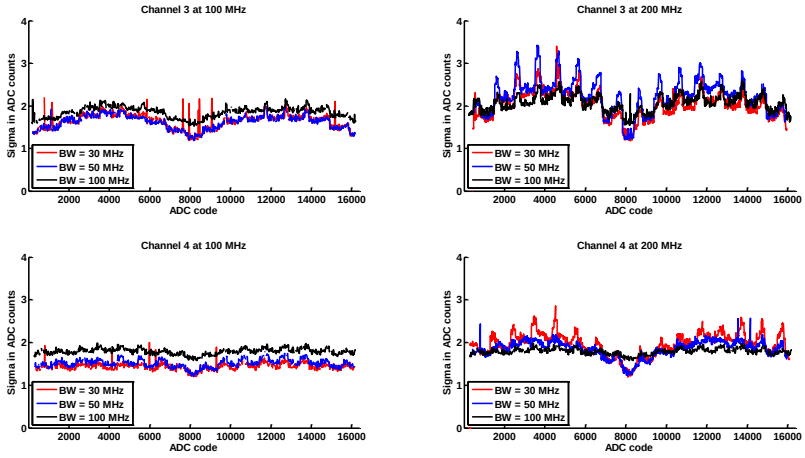


Figure 4.48: Noise performance comparison at different bandwidths obtained with the FADC Mezzanine version 5

Fig. 4.48 reveals an impacting result. While at 100 MHz the noise increases as the bandwidth does, according to the theoretical behavior, the effect at 200 MHz is unexpected. At 100 MHz the overall noise performance flattens reducing the peaks even though the noise at the middle and extremes increases. However at lower bandwidths, the effect of the peaks become even more dramatic, meaning that the experimental noise does not come only from the elements which were considered as noise source, meaning that the effect is not only due to the noise. Another experiment which was intended to understand the problem source, being discarded the analog amplifiers and the DACs as a possibility, is a finer ADC sweep, now with 2000 steps instead of 200. With this measurement it is foreseen to search the peak width and separation, as well as the evolution of the noise alongside the range.

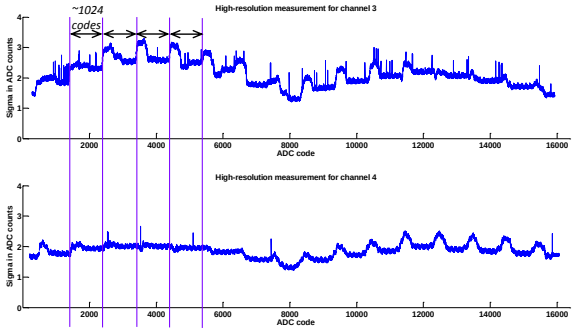


Figure 4.49: Noise measurements taking a granularity of 2000 codes

By carrying out the adequate measurements on CH3 and CH4, it was observed that the separation between peaks on was roughly equidistant, with an approximated separation of 1000 codes. This effect can be appreciated in Fig. 4.49. The same measurements were taken with other FADC Mezzanines, leading to the same results although on CH3, in all cases, the peaks appeared with much more prominence than in CH4. Analogously to the peak separation, but with less accuracy, the peak width can be extracted, being in most cases around 250 samples. Given that the separation between peaks, peak width and number of total peaks are related to 2^n numbers (each acquisition contains 16 peaks, being the minima always centered at the point 0x2000), variables such as the influence from the digital lines on the analog traces was taken into account as a source of the problem. The influence from the digital lines over the analog traces has been studied, firstly by analyzing the Mezzanine layout, and then, studying the digital lines behavior depending on the output codes.

Firstly, considering how the digital and analog traces are routed in the surroundings of the FADC device and connectors, the marked area overlaps the analog trace and the connector pads, becoming especially notorious on the channel 3. A second fact involving the layout is the ground plane placed in the stack-up position 9, between the inner analog trace and the digital traces underneath, causing a sharing of the return currents coming from both layers. Although it is somehow difficult to know where exactly the return current paths goes back into the driver, the return current follows the least-impedance path, which for this case is led by the ground plane in layer 9. However, the lack of ground return vias makes this return current path not to follow a controlled straightforward path before reaching the device of origin. Taking into account that the analog signals carry part of this current by the same ground plane as the digital signals do, the return currents both from the digital lines and analog lines might produce crosstalk effects.

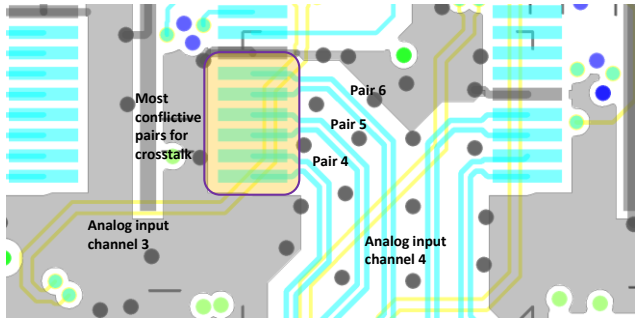


Figure 4.50: Zoomed layout section around the FADC surroundings and connector. Analog traces are shown in yellow and indicated while the digital traces routed on the bottom are depicted in blue, pointing out to the most likely conflictive lines.

Fig. 4.50 shows the routing close to the FADC and connectors in case of the CH3 and CH4, where the most disparity between results is obtained. In the picture, it can be observed that for the CH3, the analog trace overlaps with the connector pad area whilst on the CH4 it doesn't happen, being an issue which can relate the results to the design.

To understand the way how crosstalk can affect the analog trace, it is necessary to go back to sub-section 4.2.1, where the output ADS62P49 protocol is described. Each pair of odd/even bits is grouped in a differential pair, requiring seven differential traces to transmit the whole sample using a DDR sampling clock (latching the odd bits on the rising edge while the evens

on the falling edge). This fact causes inherently to obtain different line behaviors depending on the input code. For instance, an input such that the output delivers only zeros (0x0000) or only ones (0x3FFF), will produce each differential line to behave as a DC signal since every even/odd pair is equal. On the other hand, if we drive a voltage such that the even bit is the opposite of the odd bit (such as 0x1555) or (0x2AAA), these combinations make the differential line behave as an oscillating clock line. This hypothesis relates the amount of crosstalk in the analog line with the output code received, making some combinations more conflictive than others.

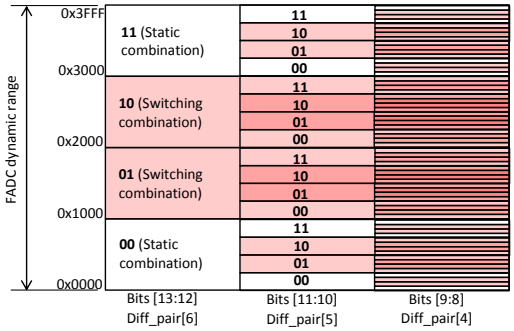


Figure 4.51: Table of crosstalk-conflictive and non-conflictive crosstalk codes

Fig. 4.51 describes the conflictive and non-conflictive combinations for a code where only the six most significant bits have been taken all over the fourteen using DC input voltage. Switching combinations are plotted in transparent red while constant combinations remain in white. As the number of simultaneous conflictive combinations from differential channels overlap, the pink color used to plot a single switching combination has been depicted in a more reddish one, meaning that two or three lines are switching simultaneously instead of one. Fig. 4.51 intends only to provide an idea about the codes which can be conflictive, used only as a tool to correlate the position switching combinations throughout the FADC range with the patterns observed in the previous figures. Nevertheless, although the pattern does not have to be strictly linked to the table since the layout complex geometry does not have to relate linearly the amount of crosstalk with the type of output code.

A second point which may relate the crosstalk with the noise is due to the ADC sampling frequency and the frequency of the digitized crosstalk-induced signals, considering that the crosstalk comes from the data lanes which are switching. Due to this fact, the coupled signal cannot be seen unless a higher frequency is used to observe the peaks of the crosstalk. However, as the induced signal is added to the input branch, this effect is translated during the sampling process as apparent noise, due to the fact that during the FADC sampling, the coupled peak might have been caught or not, hence, adding the amplitude peak as an undistinguishable noise contribution from the white noise from the previous analog stages. The consequences of these effects mentioned above can be linked to the results obtained in Figs. 4.45, 4.46 4.47 and 4.48 given the peak periodicity, where 16 peaks can be clearly seen in CH3, linking the number of peaks to an influence of crosstalk from the diff_pair[4] over the analog signal. Nevertheless, not all the influence can be directly attributed to diff_pair[4] from CH3 since also diff_pair[5] and diff_pair[6] overlap that area, but, according to the number of peaks which should produce on the results, the effect is not strongly manifested. Nevertheless, this effect is not trivial to determine, since the common-mode return currents paths - which is a ground or power plane - of each differential pair, follow a different return path, commonly

not straightforward due to the layout complexity, large amount of vias, large number of return currents from different pairs which can combine themselves during the return path, and layer change, making difficult to know that the influence is only due to a crosstalk from a single differential pair and not to a combination of effects.

Another experiment which is implemented by changing the antialiasing filter topology typical 1st-order RC low-pass filter to a lead-lag (RCR filter). On the PCB, the 0 Ω resistors in series with the capacitor, allow to carry out this experiment easily. Fig. 4.52 shows the change on the schema.

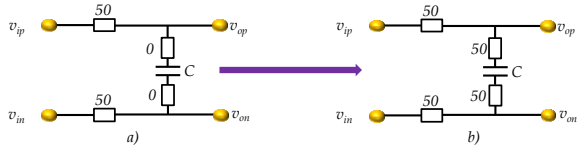


Figure 4.52: Filter topology change experiment from a) RC filter to a RCR (lead-lag) filter

The experiment consisted in a sweep at 200 MHz sampling frequencies over 2 channels, setting the bandwidth to 50 MHz in both experiments.

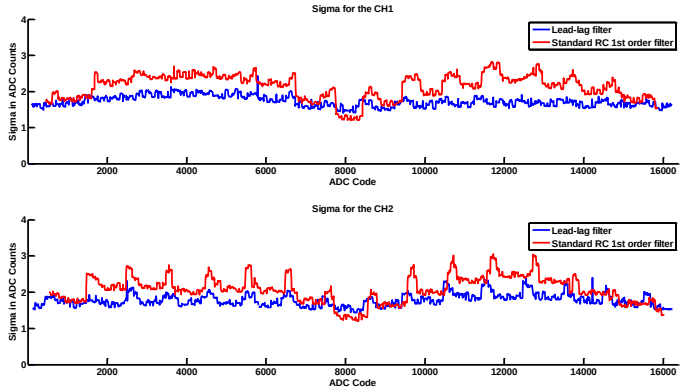


Figure 4.53: Noise performance comparison between different filter structures applied to CH1 and CH2 at 200 MHz

It can be noticed in Fig. 4.53 the peak reduction when changing to a lead-lag structure. However, the benefit obtained with a more flattened noise-versus-code response, occurs at the expense of a worse resolution in the zones at which the best performance was obtained with a single-pole RC filter. The causes which can produce this type of behavior are complex and difficult to predict, although it was hypothesized that the contributions to such peaks were not produced by an active noise source, but to the conversion into noise of a coupled signal due to the sampling process.

If a circuit model containing the elements form the antialiasing filter to the FADC device is considered, modeling the line in between as a sensitive differential noise, we obtain the circuit depicted in Fig. 4.54. Therefore, the more flattened response when implementing the lead-lag filtering could be explained due to the position where the digital signals couple with the analog traces and the antialiasing filter position.

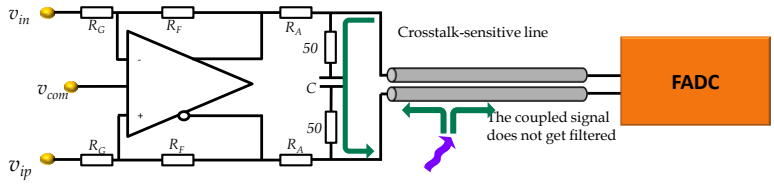


Figure 4.54: Circuit model aimed to understand the source and influence of crosstalk.

At high-frequencies the capacitor behaves as a low-impedance element, therefore, the effective impedance formed by branch of the antialiasing filter at high-frequencies is 100 Ω, producing the near-end crosstalk to be filtered, fact which does not happen when the resistors on the RCR branch are set to 0 Ω. On the other hand, the far-end crosstalk, instead, becomes unfiltered due to the position of the filter, incurring in an inefficient strategy. In contrast, Fig. 4.55 shows the model proposed for the antialiasing filter placement thought for the final prototype, where both crosstalk components become filtered in case this phenomenon happens. In any case, the lines have been carefully rerouted aimed to minimize the impact from the digital lines on the analog traces.

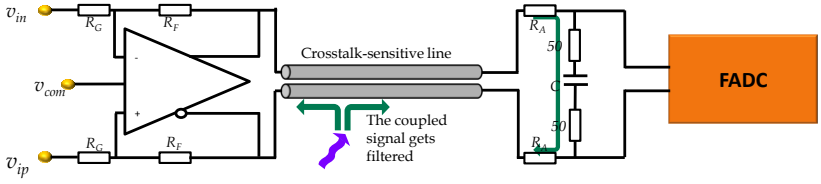


Figure 4.55: Proposed circuit aimed to minimize the effects of crosstalk on the digitalization by optimizing the filter placement.

Concluding the measurements performed to understand and minimize the influence of the uneven noise behavior, it was concluded to keep the design but changing the layout by following some rules which were not taken into account on version 4. Table 4.16 summarizes the points, at the level of the analog stage which changed from one version to another.

Table 4.16: Configuration of the analog stage throughout the FADC Mezzanine versions

	Type of amplifier	Offset output voltage / R_{DAC}	Common voltage connection	Offset filtering
V1	CFA / FDA	±1, 681 Ω	Power supply	No
V2	FDA	±1 , 200 Ω	Power supply	No
V3	FDA	±3.3 , 1.32 kΩ	Vcom amplifier	No
V4/5	FDA	±3.3 , 1.32 kΩ	Vcom amplifier	Yes

Chapter summary

This chapter was devoted to provide a detailed scheme concerning the design of a FADC Mezzanine for the new electronics of EXOGAM2 and NEDA. Among the main topics, special focus was pointed on the device selection and the low-noise specification, related to the nature experiments in high-resolution gamma spectroscopy. Other associated matters are the study

of the interfaces of the FADC Mezzanine with the rest of adjoining circuitry, presenting from the main device choice until reaching the tiniest details.

The next chapter introduces the test environment required to perform the evaluation and measurements of the FADC Mezzanine, including both the platform development as well as the measurements required to evaluate an acquisition system both for general propose and specially in the context of the nuclear physics.

5. FADC Mezzanine Testbench design

The design of a customized testbench platform is due to qualify the FADC Mezzanine and evaluate its performance figures. This chapter introduces the parameters and methods used to evaluate the acquisition both in a standard domain, envisaged towards common A/D qualification tests such as nonlinearities and in measurements in the frequency domain. Concretely, the chapter has been divided into two sections. Firstly, the type of measurements to be applied are discussed, followed by the design of the platform itself, included in the second part.

5.1. Test requirements

The goal of the work described in this chapter is the design of a test platform to fully test the Mezzanine in a minor amount of time. The requirements to achieve such goal can be summarized in the following points:

- FADC Mezzanine control capability devices via SPI protocol. The platform must be able to act on the device registers in order to enable different configuration modes, accelerating the location of mistakes in case of unexpected behavior.
- Capability to communicate with laboratory equipment. Dedicated interconnection boards might be needed to link the interface the Mezzanine with laboratory equipment such as signal generators.
- Data analysis. A/D qualification is implemented with digital signal processing algorithms, either in firmware or software.
- Quick and user-friendly. As a test platform is expected to be used for a serial production, a fast and easy interface must be provided for the user of the test bench.

5.2. Analog to digital conversion quality characterization parameters

The parameters presented in the following paragraphs, describe a way to quantify the quality of an A/D conversion system. Any system is limited in resolution theoretically by its thermal noise contribution whereas for an A/D conversion, quantization noise is inherently added to the conversion process. Assuming that there are no other noise contributions, signal-to-noise from quantization ratio (SQNR) is defined by:

$$SQNR = 10\log_{10}\frac{P_{signal}}{P_{quant.}} = 20\log_{10}\frac{V_{signal}}{V_{quant.}} = 6.02N_{bits} + 1.76 \qquad 47)$$

Where P expresses the signal and noise terms in power, V in RMS voltage and N_{bits} is the number of nominal bits of the analog-to-digital converter. Additionally, for notation convention, SQNR is referred only to the signal-to-noise ratio due to quantization effects, where SNR is meant for a generic expression involving any type of noise [60, 97].

In the practice the noise contributions into a conversion system are not only due to quantization. Thermal effects, clock jitter and shot noise in active devices, for instance, degrade the SNR. Additionally, PCB layout, power supply decoupling and the technology of the discrete surrounding components, might lead to different noise performances. A widely-used parameter, called effective number of bits (ENOB), is defined to describe the number of bits useful over the physical bits of an ADC, calculated from the SNR expression. Converters with 12 bits can lose over 1.5 bits, whereas converters with higher number of bits lose even more bits due to the increasingly difficulty to reduce the noise at higher resolutions.

Standard qualification parameters used to evaluate can be separated in three different groups according to the measurement method: parameters evaluated in stationary conditions, parameters evaluated in the frequency domain, and differential (DNL) and integral nonlinearities (INL). Moreover, acquisition qualification in the nuclear physics domain needs to introduce the concept of energy resolution, and the quality of neutron-gamma discrimination.

5.2.1. Noise performance in stationary analysis

Stationary parameters are quantified without using any input signal so that the system intrinsic noise can be measured. A second procedure consists of a adding DC input signal to evaluate the performance in different zones of the A/D range, where the resolution might change.

Even though noise can be characterized in the frequency domain, as stationary measurements do not require the noise frequency response, a time-domain analysis provides utter information for the FADC Mezzanine qualification. One of the most widely used methods to describe theoretically the noise is by defining its mean value μ_x and its variance σ_x^2, assuming that the statistical properties of the signal do not change within a time window T as:

$$\mu_x = \lim_{T\to\infty} \frac{1}{T} \int_0^T x(t)\, dt \tag{48}$$

$$\sigma_x^2 = \lim_{T\to\infty} \frac{1}{T} \int_0^T [x(t) - \mu_x]^2\, dt \tag{49}$$

When a set of digital samples is used instead, the integrals are replaced by sums for a time window of N samples [88]:

$$\widehat{\mu_x} = \frac{1}{N} \sum_i x_i \tag{50}$$

$$\widehat{\sigma_x^2} = \frac{1}{N-1} \sum_i (x_i - \widehat{\mu_x})^2 \tag{51}$$

Time-domain standard deviation can be measured in ADC counts, and then converted to ENOB using the expression 52).

$$\sigma_t^2 = \sigma_q^2 + \sigma_n^2 = \frac{R^2}{12}\left(\frac{1}{4^B} + \sigma_n^2\right) = \frac{R^2}{12}\frac{1}{4^{ENOB}} \qquad 52)$$

The expression comes from the quantization variance σ_q^2, and adding the rest of contributions given by σ_n^2 such as thermal, jitter, etc. In practice, the total measured noise variance is given by σ_t^2 making an analogy between the SQNR expression to the physical number of bits and 52) with ENOB [15]. *R* refers to the dynamic range (either in ADC counts or volts), and *B* is the physical number of bits.

5.2.2. Frequency-dependent qualifications

Less used in the field of the nuclear physics, but still mandatory to qualify an A/D system are the frequency-domain tests, where input sinusoidal signals are used to observe the frequency effects in the system. The most common tool to perform analysis in frequency domain is the Fast-Fourier transform (FFT) [58].

However, before introducing any parameter, it is of paramount importance to distinguish between noise and distortion when performing tests in the frequency domain. Noise is characterized by a random signal produced by thermal effects and shot noise while the sources of distortion arise from the device nonlinearities. When performing tests in frequency domain using sinusoidal inputs, device nonlinearities can create a sort of new frequencies located at integer multiples of the input frequency, called harmonics. In addition, in A/D conversion, these new frequencies can appear reflected at the signal bandwidth if the antialiasing filter does not eliminate the frequencies before the conversion.

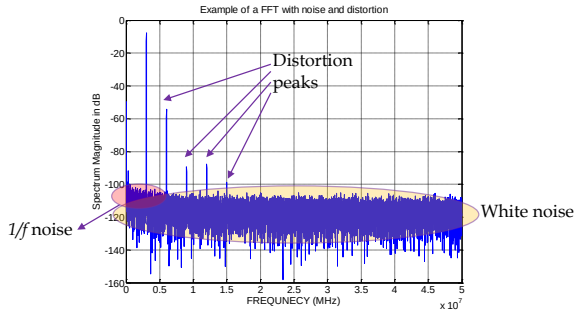


Figure 5.1: Example of FFT containing noise and distortion

Analysis methods based on FFT provide a powerful tool to analyze and distinguish noise from distortion effects. White noise is manifested along the whole signal bandwidth, while distortion is present only at certain frequencies forming narrow peaks. In Fig. 5.1 it is depicted an example of FFT with noise and distortion effects.

Several parameters are used to measure and distinguish the noise from distortion in the frequency domain. To avoid confusion, for notation convention, the *SNR* in frequency domain will be defined as SNR_f, in contrast with the definition for stationary measurements, called just *SNR*. Hence, recalling the definition, SNR_f is defined as:

$$SNR_f = 10\log_{10}\frac{P_{signal}}{P_{noise}} \qquad 53)$$

Moreover, a more generic term in frequency domain analysis for A/D qualification is the SINAD (Signal-to-Noise and Distortion), which includes the distortion peaks in the formula as:

$$SINAD = 10\log_{10}\frac{P_{signal}}{P_{noise} + P_{distortion}} \quad 54)$$

Based on the SINAD, we can calculate the ENOB in frequency-domain as:

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad 55)$$

The expression 55) assumes that the signal covers the whole dynamic range. However, it is often introduced a normalization factor if the amplitude does not get across the whole range. Therefore, the corrected formula is written as:

$$ENOB_c = \frac{SINAD - 1.76 + 20\log_{10}\left(\frac{A_{FS}}{A_i}\right)}{6.02} \quad 56)$$

where A_{FS} stands for the full-scale amplitude and A_i refers to input amplitude. By means of these parameters, a graph of *SINAD / ENOB* in function of the frequency is obtained, analyzing how the distortion and noise affect the system. Other applications require of the so-called parameter SFDR (Spurious-Free Dynamic Range), defined as the difference produced in the FFT by the highest distortion peak and the signal peak.

5.2.3. Differential (DNL) and Integral (INL) nonlinearities

The ideal transfer function of any A/D converter can be represented as a staircase function whose step width is the LSB voltage. Dividing the full-scale range in 2^N levels lead us to obtain a set of voltages v_{ti} which represent the transition voltage between a code C_i and C_{i+1}. Ideally the transition voltages are equally distributed where the step width is constant, called LSB voltage v_{LSB}. However, in the reality, several errors occur during conversion. Among the most common ones we can mention the gain error, offset error and nonlinearities [98]. Gain and offset error are defined as the errors either in slope or over the zero point respect to a line passing over the ideal transfer function. Hence, the errors can be defined as a variation over the slope or in the zero-crossing point of the transfer function. A more generic approach consists of measuring the Differential (DNL) and integral (INL) nonlinearities.

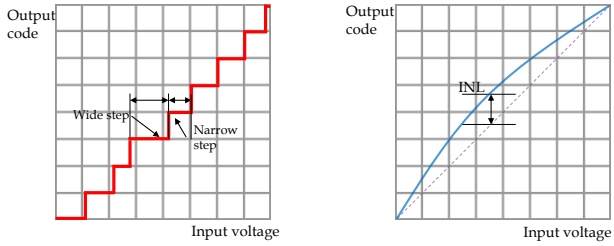


Figure 5.2: Graphical representation of DNL (left) and INL (right)

When using them, we measure how the transfer function shape and code widths change along the whole dynamic range. DNL is defined as the difference in the step width of a certain code over the ideal step width v_{LSB}. Wider steps give positive DNL while narrower steps give negative DNL ones. In contrast, INL information is related to the deviation of the experimental

transfer function code-to-code respect to an ideal line, called "best-straight line" method. In Fig. 5.2 is shown graphically the concept of DNL and INL. Expression 57) and 58) introduce the expressions to obtain the DNL and INL, respectively.

$$DNL_i = \frac{v_{t(i+1)} - v_{ti}}{v_{LSB}} - 1 \quad 57)$$

$$INL_i = \sum_{j=1}^{i} DNL_j = \frac{v_o - v_{zero}}{v_{LSB}} - i \quad 58)$$

where $v_{t(i+1)}$ and v_{ti} are the transition voltages for the i-th code, v_{LSB} is the ideal LSB voltage and v_{zero} is the minimum analog input that provides an output code different to zeros.

In practice, obtaining the DNL and INL can be carried out using statistical methods, called code-density methods. Unlike the methods based on analog integrating servo-loops [99], used in high-resolution nonlinearities measurements in A/D systems, for our FADC Mezzanine it was preferred to use the sinusoidal histogram method [100, 101]. This method is used to obtain the DNL and INL based on code density tests obtained from a sinusoidal input signal instead of sawtooth waveforms. This method is specially recommended when evaluating ADCs above 12-bit resolution, provided that sinusoidal waveforms can be generated with more accuracy.

Sinusoidal histogram method for nonlinearity measurements

When using the sinusoidal histogram method for nonlinearity measurements, three parameters must be carefully taken into account: input frequency, signal amplitude and number of records. On one hand, signal amplitude must cover the entire dynamic range in order to cover all the possible codes without clipping. The second point is to select an input coherent frequency equal to a high prime number of cycles, avoiding repetitive sampling at the point within a cycle (sampled at all possible different phases). To obtain the desired input frequency f_{in}, expression 59) is used:

$$\frac{f_{in}}{f_s} = \frac{N_c}{N_R} \quad 59)$$

where N_c refers to the number of cycles and N_R is the record length. The desired ratio may be found out by setting a ratio such that $N_C/(N_R + 1)$ is a prime integer number. For instance, taking a record length of N_R = 32768 makes $N_R + 1$ = 32769, which can be factorized in terms of prime numbers as 3*3*11*331, therefore, N_C can be set to 331, which for a f_s of 100 MHz, f_{in} would be 1.01013183975 MHz. Once an input frequency is chosen, the next step consists of choosing the total number of records based on the experimental desired accuracy. In order to choose a proper number of samples, expressions 60) and 61) give a number assuming a DNL error and certain degree of confidence with the measurement [101]. Hence:

$$N_{R_{min}} = \left[\pi 2^{B-1}\left(Z_{\frac{\alpha}{2}}\right)^2\right]/\beta^2 \quad 60)$$

$$Z_{B,\frac{\alpha}{2}} = \sqrt{2}\, erfc^{-1}\left(1 - (1-\alpha)^{2^{-B}}\right) \quad 61)$$

where β makes reference to the DNL error in LSB expected, B is the number of bits and α is the degree of confidence for the measurement, which leads to the term $Z_{B,\alpha/2}$. For B=14 bits, the values obtained for several values of β and α are summarized in Table 5.1. A consequence which can be automatically derived from the numbers is the increasingly number of records required, if an analysis with low DNL error is desired.

Table 5.1: Number of samples required for different values of confidence and DNL error when using the sinusoidal histogram method

Confidence	*β=0.1*	*β=0.1*	*β=0.5*	*β=1*
90 %	6264206	1741052	178568	69642
95 %	9886714	2471678	395469	98867
99 %	17077785	4269446	683111	170778

After choosing these three parameters, the histogram must be obtained and accumulated at each acquisition, obtaining the characteristic sine bathtub histogram function. The plot shows that the most probable values are concentrated on the sinusoidal extremes, while the transitions containing the highest derivatives correspond to the least likely value. We define the histogram $H[j]$ as the number of counts for a code j and the cumulative histogram $CH[j]$, as the mapping of the cumulative bins up to the specified point j. The expression 62) describes mathematically how to obtain $CH[j]$ from the histogram values $H[j]$.

$$CH[j] = \sum_{i=1}^{j} H[i] \tag{62}$$

Afterwards, the ADC transfer function and nonlinearities can be extracted converting the cumulative histogram from the sine input to a linear function using the expression 63) (a nonlinear transformation). In 63) the experimental transition levels of the transfer function can be found out by applying the transformation:

$$T[j] = -\cos\left(\frac{\pi \cdot CH[j-1]}{\sum_j H[j]}\right) \tag{63}$$

obtaining subsequently the bit width as:

$$W[j] = T[j] - T[j-1] \tag{64}$$

Directly, based on the bit widths and the transition levels, the generic expressions 57) and 58) may be applied to obtain the DNL and INL patterns based on a code.

5.3. The testbench platform

This section presents the design of the set-up used to fully characterize the FADC Mezzanine. On the following paragraphs we describe the specifications and elements to carry out this task, detailing the hardware, firmware and software elements.

5.3.1. Testbench platform specifications and capabilities

A major issue is to envisage the design of the platform towards a medium-size mass production, involving the verification of 90 Mezzanines for NEDA and 128 for EXOGAM2, fact which increases the total number of channels up to 872, being the test time an important factor to take into account. Not only the quickness when testing, but also the test completeness is a demand, involving a whole FADC Mezzanine qualification both in terms of frequency-domain and static tests. Some of the points where to focus on are:

- On-line data analysis. Quickness during testing does not necessarily mean to analyze data in real time. However, the system must be designed to run

autonomously without human interaction except for the startup and stop, and in case of changing the parameters. Tasks such as the FADC Mezzanine control, data collection, analysis and storage should be able to be automatized.

- Development of front-end electronics. The goal is to design a low-noise front-end board which allows communication with a signal generator to provide stimuli. Moreover, a second board is a must to link the FADC Mezzanine with a firmware.
- Automatic equipment control. Using laboratory equipment for an automated test makes specially attractive the use of GPIB ports to control remotely the equipment. For our case, an arbitrary waveform generator was used.
- Integrated and expandable firmware design.
- A Graphical User Interface (GUI) for a friendly interaction of the user (testing or developing) with the set-up.

In views of the aforementioned specifications, a solution to design test platform would contain the following points.

- UART communication. Since an on-line data analysis is not required, signal records can be stored internally in a temporary memory before their processing. This fact significantly reduces the complexity of the communication protocol between the FPGA and the computer.
- Firmware implementation by means of IP cores instead of embedded processors, including a UART – SPI communication and a set of temporal memories.
- A GUI and communication between the FPGA and the PC based on LabView software, where acquisition, analysis and control tasks can be easily integrated.
- A front-end electronics board, using 4 single-to-differential converters with capability to attenuate the gain and provide filtering.

The test platform block diagram is illustrated in Fig. 5.3.

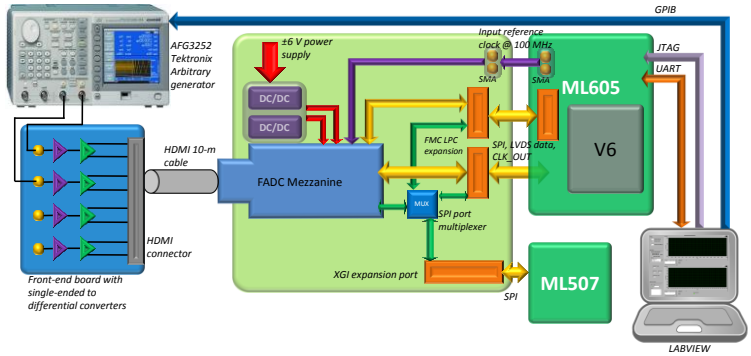


Figure 5.3: Automated testbench block diagram

The block diagram comprises the following elements:

- The FADC Mezzanine, device under test (DUT).
- An FPGA-based evaluation module, concretely the Xilinx evaluation board ML605 [102], used to collect and send the digitized data to a computer.
- An interconnection board between the ML605 and the FADC Mezzanine, used to deliver clocks, power supply and provide compatibility between connectors.
- An HDMI Infinite 1.4 10 meter cable.

- A front-end board used to drive the signals from the waveform generator to the FADC Mezzanine, providing also an interface with the HDMI cable.
- A waveform generator. Two of them have been used: Agilent 33522A and Tektronix AFG3252.
- Optionally, an ML507 with a Virtex-5 used to provide the slow control. For these tests, the slow control has been commanded directly from Virtex-6.
- A PC with the LabView software installed to collect and analyze the acquired data.
- 2 USB-MiniUSB cables to link the JTAG and UART to a PC.
- A GPIB-USB cable to command the waveform generator.
- SMA cables.

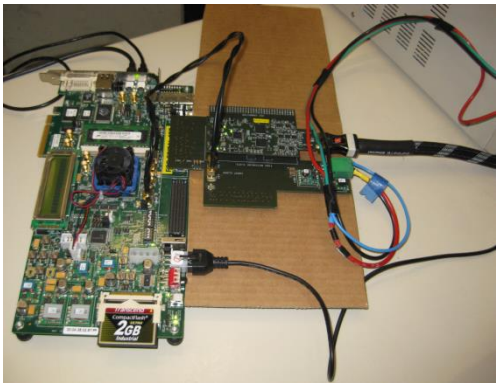


Figure 5.4: Picture of the complete testbench: On the left, the ML605 EVM from Xilinx. Plugged to the ML605, the connection board and the FADC Mezzanine. At the far right, the HDMI Infinite v 1.4 is shown. The picture was taken in February, 2013, at LNL (Laboratori Nazionali de Legnaro) the NGD tests with the FADC Mezzanine

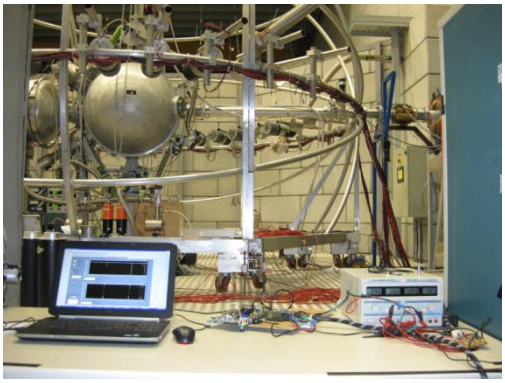


Figure 5.5: Picture of the testbench at LNL. On the left, the computer used to collect and process data. In the middle, the FADC Mezzanine and the evaluation modules. On the right, the single-ended to differential module and the power supply

Figs. 5.4 and 5.5 show two pictures of the testbench platform during the tests at LNL, Legnaro.

5.3.2. Hardware elements

The ML605 evaluation board

The evaluation board ML605 from Xilinx, shown in Fig. 5.6, is the processing core of the FADC Mezzanine testbench platform. It contains a Virtex-6 XC6VLX240-T, which performs the firmware tasks such as the FADC Mezzanine control, data collection and temporary storage. Some of the peripherals to be used are:

- The FMC LPC connector. Provides the main interface between the FPGA and the Mezzanine, designed to drive high-speed signals.
- SMA cables. Coaxial connectors are used to supply the input clock and trigger signals.
- JTAG. Only used during the startup to program the Virtex-6 device.
- UART. Embedded in a USB connector, it is the main communication link for both control and data acquisition.

Figure 5.6: ML605 evaluation board from Xilinx. Courtesy of Xilinx

Front-end electronics intermediate board

A fully-automated FADC Mezzanine testbench would require a signal generator with 4 channels. Provided that waveform generators drive signals in single-ended format, a single-ended-to-differential system is due to drive the signals towards the HDMI cable. In addition, the board presented provides a provisional interface between the NEDA PMTs and the FADC Mezzanine. In Fig. 5.7 is presented the block diagram.

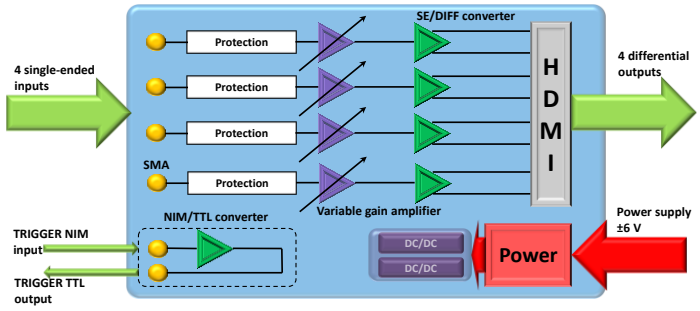


Figure 5.7: Front-end electronics board block diagram

The design contemplates the following functionalities:

- 4-channel single-ended to differential low-noise stages.
- Protection system against high-voltage peaks, avoiding damage on the front-end and back-end electronics.
- NIM-to-TTL logic converter, aimed to make compliant the ML605 logic levels with the NIM electronics. This extra functionality was envisaged during the test stages using the NIM electronics from Neutron Wall.

Regarding the single-ended to differential channel, the topology combines both fully-differential amplifiers for the single-ended conversion, and low-noise operational amplifiers to provide an easier gain control. The AD8139 was used for fully-differential amplifier while the AD4817-1 High-speed FET-based is used at the single-ended part. A unitary-gain operation mode is selected for the AD8139, operating under the optimal noise conditions, while a follower using the ADA4817-1 preceded of a potentiometer is used to adjust the gain. Since the output impedance from AD4817 Z_{out} << 200 Ω, it is possible to implement the single-ended to differential converter branches symmetrically using 200 Ω resistors on both positive and negative inputs. Fig. 5.8 shows the electronic circuit for the front-end electronics circuit.

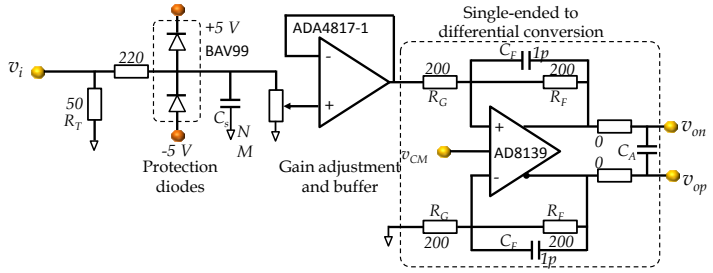


Figure 5.8: Front-end electronic channel schematics

The part preceding the buffer is composed by an overvoltage protection circuit, a smoothing capacitor C_s and a terminator in split configuration. The protection circuit is based on low-capacitance (<1.5 pF) fast-switching Shottky diodes from the BAV99 series, driving overvoltage peaks towards the power supply, with a current being limited by the 220 Ω resistor. The input terminators R_{T1} and R_{T2} may be configured either for current or voltage inputs. In case of a current input (from a PMT) the current input is transformed into voltage with the input voltage divider point. On the other hand, for standard voltage inputs from a signal generator, R_{T1} is set to 0 Ω and R_{T2} to its corresponding termination impedance, typically 50 Ω.

A second sub-circuit circuit converts the NIM current levels to TTL voltages inputs from the ML605. In fast-negative logic using NIM modules, logic is provided by current pulses in which the logic one lies in between -14 to -18 mA (-700 mV to -900 mV @ 50 Ω). As the logic levels may vary between modules, a converter based on operational amplifier was selected, converting the logic levels from -700 mV to +2.5 V using an inverting configuration. The converter circuit is shown in Fig. 5.9:

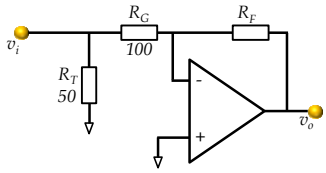


Figure 5.9: NIM-to-TTL logic converter

R_F is selected to provide an appropriate gain depending on the NIM module. Typically for levels from -700 mV to -900 mV a gain of -2.8 to -3.6 is selected. The LeCroy Fan-out NIM module makes use of a logic set to -700 mV, requiring a R_F of 357 Ω. Fig. 5.10 shows a picture of the single-ended to differential module.

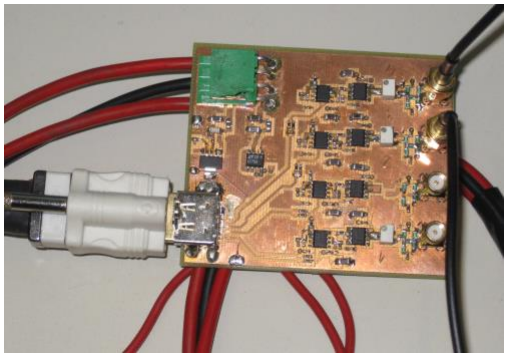


Figure 5.10: Picture of the single-ended to differential module

Design of an interconnection board between ML605 and the FADC Mezzanine

An intermediate board is required to communicate the FADC Mezzanine with the rest of external devices such as the ML605, and signal generators. Due to the FMC LPC connector pinout, only 2 channels can be digitized at the time. Hence, the specifications for the intermediate board can be summarized in the following points:

- Communication for digitized 2 channels between the ML605 and the FADC Mezzanine.
- Capability to select the channels under test (either CH1,CH2 or CH3,CH4)
- Power supply and input clock connectors.
- FADC Mezzanine SPI control port selection either from ML605 or ML507.

According to the specifications, the block diagram illustrated in Fig. 5.11, summarizes the main aspects discussed above. The board includes mainly connectors to adapt between the ML605 and the mezzanine, power supply and a multiplexer to select the control either from the ML605 or from the ML507. The connectors included in the test board are the respective male / female counterparts of the FADC Mezzanine and ML605 connectors. Therefore, the device references are:

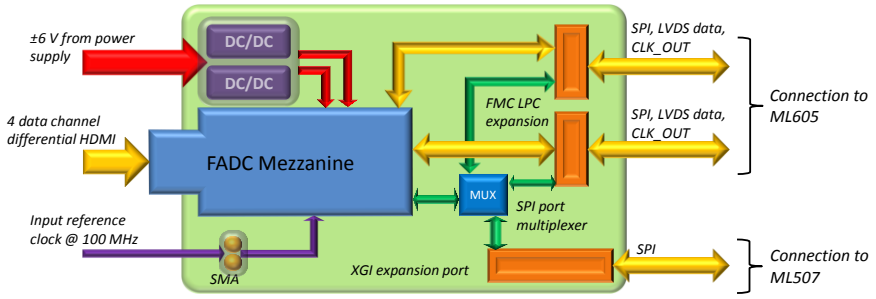


Figure 5.11: Test interconnection board block diagram

- 2 x QMS-026-05.75-L-D-PC4, corresponding to the counterpart for the FADC Mezzanine connector QFS-026-04.25-L-D-PC4.
- 2 x FMC VITA 57 ASP-134605-01 male connectors, counterpart of the female connector ASP-134603-01 from the ML605, allowing acquisition for the 4 channels.
- High-speed SMA connectors for the differential clock input.

The design of the power supply regulators has been emulated according to NUMEXO2 power supply demands, using the same DC/DC converters for the test board. Taking the power supply at ±6V, the switched regulators are aimed to generate the rest of input voltages 4V and 3.3V. Therefore we have:

- PTH08T230W DC/DC converter is used to obtain 4V from 6V.
- PTH08000WAH DC/DC converter is used to obtain 3.3V from the 6V.

Both devices are built-in power supplies containing already the regulator, power elements and inductor, still requiring the use of external resistors in order to set the desired output voltage and a set of external bypass capacitors to improve the filtering performance.

SPI control multiplexing is implemented using integrated analog switches, capable to work either as a multiplexer or de-multiplexer. In our design, the multiplexed pin is attached to a FADC Mezzanine signal, whereas the two selectable inputs are connected to the FMC VITA connector and the XGI expansion port respectively. The chip used is the quad 2:1 ADG774 device.

Regarding the layout, two main issues must be taken carefully into account: group length-matching and board geometry. The board geometry constraints are obliged due to the possibility to connect simultaneously the ML507 [103] for slow-control and the ML605. Finally, the board shape adopted is shown in Fig. 5.12, where the PCB area for the connector stands out in order to link the board without obstructing the rest of elements.

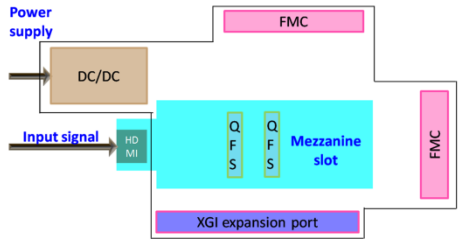


Figure 5.12: Test interconnection board geometric shape

In contrast to the symmetry layout guidelines of the FADC Mezzanine, due to the intermediate board irregular geometry shape, the use of serpentines to match the lengths within a channel was necessary. Therefore, 28 pairs are matched in groups of 7 within a tolerance of ±0.5 mm (± 3.53 ps), as well as in the FADC Mezzanine. Fig. 5.13 depicts a zoomed-in picture of the differential pairs routed to the connector.

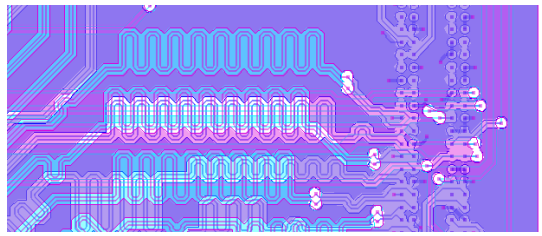


Figure 5.13: Serpentine routing detail on the test interconnection board FMC connector

The board required six layers to drive the properly high-speed traces with their corresponding ground planes, and, additionally, two extra inner layers for the power supplies and the SPI lines.

HDMI cable

An HDMI 1.4 Infinite 10m-long cable with 4 differential channels is devoted to link the front-end board to the Mezzanine. The cable used during the testing is the same one discussed in section 4.5.

5.3.3. Firmware structure implemented in Virtex-6

The firmware features a communication link between the GUI and the FADC Mezzanine. The bloc diagram in Fig. 5.14 illustrates the IPs inside the Virtex-6. Two main functionalities can be distinguished, to mention: the FADC Mezzanine setup, carried through the SPI IP after unwrapping the content of the UART commands, and the data readout, which makes use of the ISERDES and set of FIFOs to store temporary the samples. A finite state machine controls the process from the top level of the hierarchy.

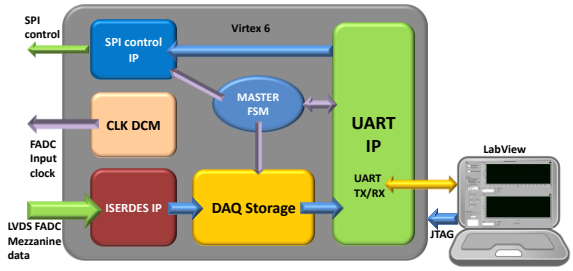


Figure 5.14: Firmware for the automated testbench block diagram

Two modes can be mainly selected depending on the type of measurement / experiment carried out: FREE-RUNNING mode and the TRIGGER mode. Measurements involving standard ADC characterization make use of the FREE-RUNNING mode in which the system is continuously acquiring samples. On the other hand, TRIGGER makes use of an external signal to start the acquisition, envisaged towards a more realistic experimental.

ISERDES IP

The first stage of data readout is performed by using a customized arrangement of serialization/deserialization data sub-blocks (called ISERDES), prepared to work at rates higher than 400 Mbps. Internally, the concatenation of the ISERDES [104] blocks include always their own IODELAY[16], coping properly with the delay adjustment.

ISERDES IP has been implemented to deliver at its output four 14-bit outputs, each containing the corresponding even/odd samples of 2 FADC channels as it is shown in Fig. 5.15, while at the inputs there are 14 LVDS channels, containing even/odd multiplexed bit duplets. The deserialization is performed with a DDR clock latching the odd bits on the rising edge and the even bits in the falling edge, requiring two clock cycles of the FADC output clock to create an output sample at the ISERDES IP output. Additionally, a half-divided clock is delivered too, which is used as the Chip Scope Pro logic analyzer sampling clock.

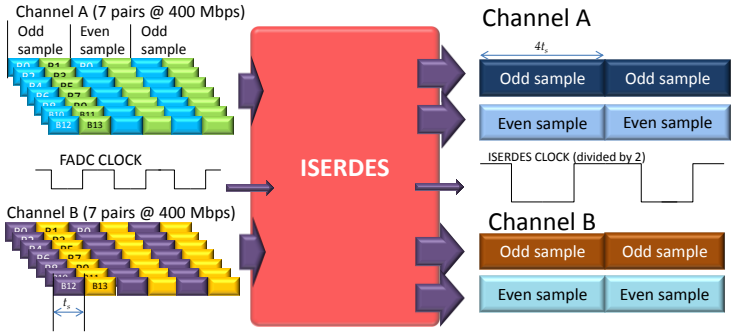


Figure 5.15: ISERDES functional block diagram

[16] *ISERDES and IODELAY sub-blocks belong to Xilinx corporation, as well as the arrangement of those to be prepared to work on for data collection of the ADS62P49.*

Master FSM

Master FSM is the main firmware controller, placed on top of the hierarchy, controlling the activation and sequence of other FSM placed in lower hierarchical positions placed inside the UART IP, the SPI IP or the DAQ storage IP. Therefore, if using the FREE RUNNING mode, two main functionalities are necessary to build up the state diagram: SPI Programming stage and data acquisition. The state machine can be modeled as in Fig. 5.16.

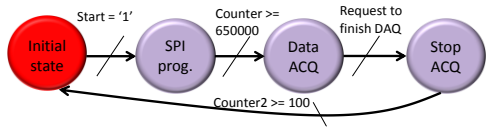


Figure 5.16: Master FSM on FREE-RUNNING mode

The FSM starts with the 'SPI programming state' after having received a specific RESET command received by the UART port. Then, during the SPI programming stage, the FSM enables the SPI driver and disables the DAQ storage for 650000 clock cycles (3.25 ms), time which takes the SPI to send the SPI commands to the FADC Mezzanine. After that time, the SPI IP is disabled and the DAQ is enabled, initiating the data collection and delivery through the UART until the cycle finishes. After all samples are delivered, the DAQ IP control sends a request signal informing that the acquisition has finished, making the FSM to return to the initial state. If the TRIGGER mode is used, a new 'Waiting Trigger' state is added after the SPI programming where the FSM remains until a trigger allows to proceed to the next state. The corresponding state-machine is shown in Fig. 5.17.

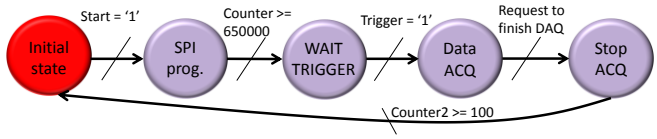


Figure 5.17: Master FSM on TRIGGER mode

Perhaps one of the most critical issues on the mater FSM is the reset mechanisms management, obliging the use of a hard despite of the soft reset via LabView from the UART. The need is due since the soft reset does not reset the RX UART IP and mainly restarts the master FSM cycle. Instead, the hard reset is performed using the ML605 buttons, forcing the firmware to re-initialize in case of an unexpected behavior.

UART block and command format

UART IP communicates the FPGA with the LabView using a half-duplex link. Its functionality is clearly separated into two different blocks: Mezzanine control and data readout. In the control bock, the UART receives a set of commands from LabView, which are then used either to deliver SPI/µWire commands or to communicate with the rest of the firmware. On the other hand, data readout is performed always after the control task, sending byte by byte all samples stored into the FIFOs.Internally, the IP contains 5 sub-blocks:

- RX register. A SIPO (Serial-in Parallel-out) 40-bit shift used to hold temporally the whole command provided by LabView, before being unwrapped.

- TX register: Based on a PISO (Parallel-in Serial-out) shift register of 10 bits, takes the byte to be transmitted from the FIFOs plus the start/stop bits.
- Clock controllers: Two of them are used to provide a clock burst to each shift register. Their timing has been adjusted to work at 1.5 Mbps in both cases.
- UART FSM controller. Controls the sequence for the RX register. TX register operations control is carried out by the storage element unit.

The command size of 40-bit was determined based on the longest SPI frame of 32 bits for the LMK03001C plus a header of 8 bits. The header contains extra information regarding the chip to which the command is addressed, as well as other future functionalities foreseen. Fig. 5.18 shows how the bits are distributed along the header.

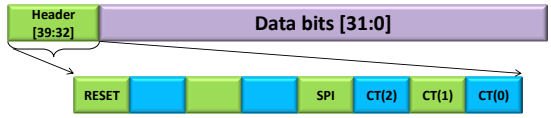


Figure 5.18: Header schema for the testbench control

Table 5.2 summarizes the type header format according to the command type.

Table 5.2: Header patterns used to control the testbench firmware

Command	Header (39:32)								Description
Reset	1	X	X	X	X	X	X	X	Soft reset command
SPI Frame	0	X	X	X	1	CT2	CT1	CT0	CT bits contain codified information for the chip
FADC Reset	0	X	X	X	0	0	0	1	Resets the FADC registers
PLL Sync	0	X	X	X	0	0	1	0	Synchronizes PLL outputs
PSA Command	0	X	X	X	0	0	1	1	Writes a certain command in the PSA block

Furthermore, given the different required bits depending on the programmed device via SPI, the excess last data bits (16 bits for the FADC and 8 for the DACs) are filled with zeros to be compliant with the frame size. Details regarding the transmission frame are detailed in Table 5.3.

Table 5.3: Types of SPI frames according to their length. Matching with the chip scope and the bits CT

Device	CT[2:0]	Data[31:24]	Data[23:16]	Data[15:8]	Data[7:0]
FADC	000 / 001	DATA	DATA	0x00	0x00
DAC	010 / 011 100 / 101	DATA	DATA	DATA	0x00
PLL	110	DATA	DATA	DATA	DATA
EEPROM	111	DATA	DATA	0x00	0x00

The header bits CT[2:0] are used to activate the chip enable signals. Therefore, as 6 programmable devices are on the Mezzanine, at least 3 bits are needed. On former Mezzanine versions, 4 DACs devices were used, taking the combinations of 100 and 101 for their management, although this is not used on the current version.

Regarding the clock generation for the registers, a external component is used to generate a clock burst of 10 cycles (8 data + start + stop bit) to trigger and shift the content of the RX / TX registers at 1.5 Mbps. However, since the frequency generated by counters is not exactly 1.5 MHz, due to the fact that a counter using a 200 MHz (5 ns) clock does not adjust exactly to the time required to match the UART clock period (666.66 ns). Hence, it is preferred to restart the counters after each burst, waiting for a new UART frame, avoiding thus phase shifts. The mechanism is depicted in Fig. 5.19.

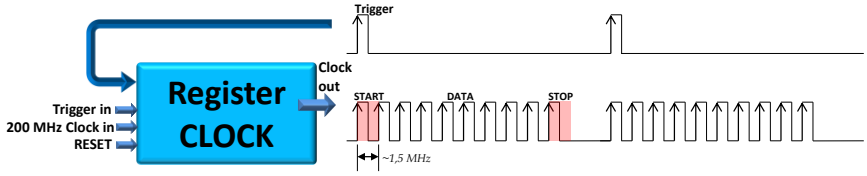


Figure 5.19: Generation of clock bursts for UART registers triggering

A particularity of the RX register is its 40-bit size. This means that it is required to receive 5 bytes before it delivers its content. It has been introduced an extension consisting on the addition of a cycle in order to dump the register content only after the 5th byte is fully received, as depicted in Fig. 5.20.

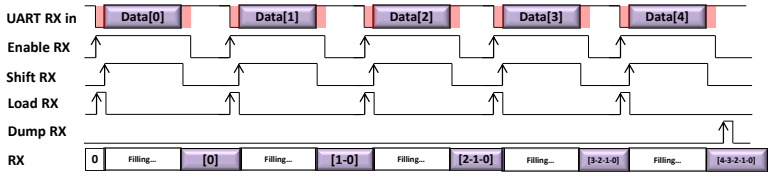


Figure 5.20: Control patterns and register evolution for a data frame of 5 bytes on the UART RX register. The control signals are generated in the local UART FSM.

Taking the value of a counter used to know which bit of the UART frame is being transmitted, defined as '*C*' counter, and the number of bytes received, the cycle across the FSM can be divided in two paths: normal path and special path, reserved only for each 5th byte. Changing state has been adjusted using the '*C*' counter for a reception at 1.5 Mbps. Hence, by using the schema from Fig. 5.21, data is only incorporated to the RX register during the 'Shift data' state, neglecting the start/stop bits. Additionally, during each 5th byte the alternative path is followed, dumping the register content during the '*Stop Dump*' state.

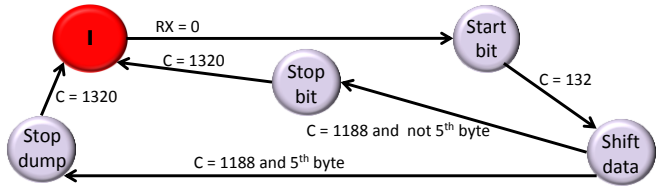


Figure 5.21: UART RX register FSM

SPI block

The SPI driver is one of the common blocks between the FREE-RUNNING and TRIGGER version, requiring only the setup of the FADC Mezzanine. The driver itself is constituted by a PISO (Parallel-in Serial-out) register and a FSM used to control the register actions. The basic operation mode consists of distributing the UART 40-bit frame along with the data and *chip enable* bits (bits 34:32). Then the local SPI FSM establishes the timing according to the SPI/μWire chronogram.

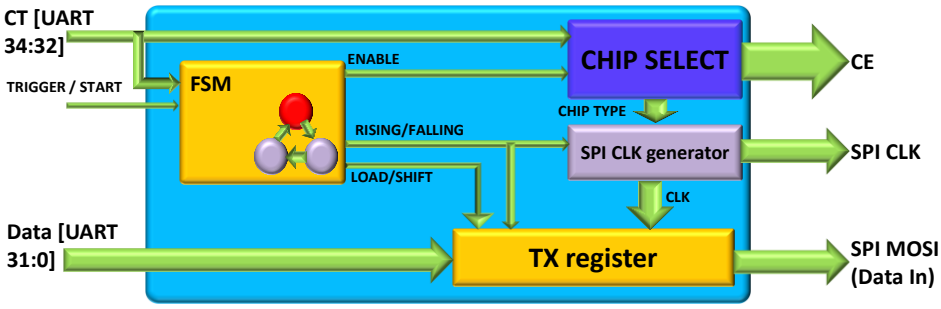


Figure 5.22: SPI block embedded on the version 2 firmware block diagram

Fig. 5.22 shows the internal SPI block diagram from a hierarchical view. It contains not only the FSM and the register, but also a set of logic blocks, called CHIP_SELECT and SPI_CLK generator, aimed to simplify the FSM structure. The CHIP_SELECT block control the chip enable signals using the CT bits from the header, and the SPI_CLK generator block generates the SPI_CLK signal with the edge compliancy based on a logic signal from the FSM.

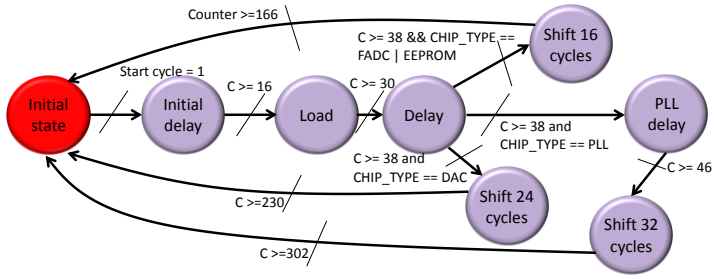


Figure 5.23: SPI FSM diagram

The SPI FSM starts when the UART dumps the context of the RX register after having received the 5th byte, following the FSM shown in Fig. 5.23. The first state of the FSM is an '*Initial delay*' toggling down the chip enable signal until arriving to the '*Load*' state, where the UART data is really dumped into the TX SPI register, ready to be shifted and delivered to the FADC Mezzanine. After the '*Load*' state and a common '*Delay*' state, the FSM splits into three branches according to the requirements of the chip currently under configuration. Fig. 5.24 illustrates an example of an arbitrary SPI cycle, showing both SPI outputs and internal control signals, in the case of a device clocked by rising edge.

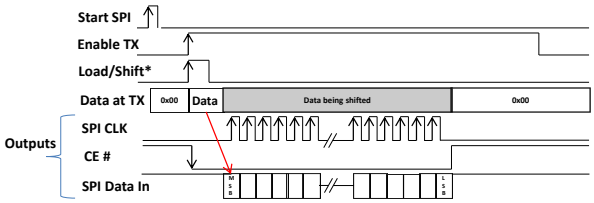


Figure 5.24: Standard SPI writing cycle for a device clocked during the rising edge. The picture shows an arbitrary number of cycles

Basically the '*Shift*' states differ in terms of the time for which the block called 'SPI CLK generator' is enabled, allowing to control the number of clock cycles. A last remark must be taken into account for the PLL SPI CLK signal generation, where an extra '*PLL delay*' state is necessary to avoid an extra clock cycle which occurs in the TX register, generating a fake shifting.

DAQ Storage

This block refers to the temporary memories used to store signal segments, making compliant the delivery of high-speed data from the ISERDES with the UART at 1.5 Mbps. This approach is especially useful and can be directly used in case of stationary and frequency-domain measurements, delivering the portion of acquired signal to the computer. Hence, the employment of FIFOs with independent writing/reading clocks fits perfectly into our requirements, needing a total amount of 8 FIFOs, 16k-depth and 8-bit-width. Each group of 2 FIFOs stores the lower and higher part of the sample respectively, as it is shown in Fig. 5.25.

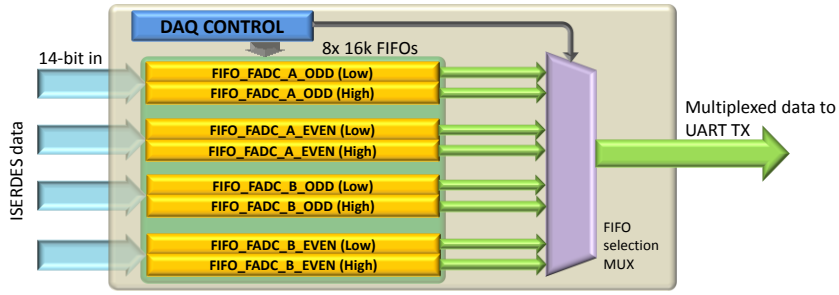


Figure 5.25 DAQ storage block diagram

The DAQ control mechanism is fairly simple. Basically consists of a first simultaneous FIFO filling-up followed by a sequential reading of the acquired data until all FIFOs are emptied. The DAQ control block controls both the full/empty and write/read FIFO enables. Besides, it controls the FIFO selection from the 8:1 output multiplexer, which copes with the FIFO channel selection towards the UART TX register. DAQ cycle starts with a command from the Master FSM as soon as the SPI Programming state finishes, and the cycle finishes after the last FIFO is emptied, toggling a signal which warns the Master FSM that the readout cycle has finished.

Fig. 5.26 shows an example of FIFO reading cycle, getting the last bytes from a FIFO and starting with the first words from of the following one. An external signal inside the DAQ

activates the 10-cycle clock burst for the UART TX register, synchronizing the FIFO with the UART.

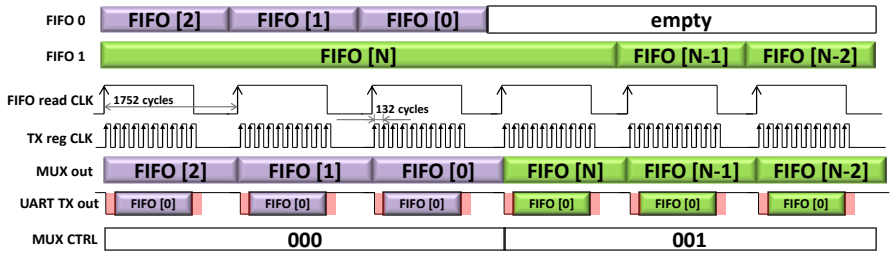


Figure 5.26: FIFO reading chronogram. It includes FIFO 0 and FIFO 1, as the outputs from both FIFOs, FIFO read CLK as the reading clock, TX reg CLK as the UART register control, the MUX output, the UART output and the MUX control bits

In case of using TRIGGER mode, is often interesting to visualize part of the sample before the trigger occurs, allowing the calculation of the baseline level for amplitude measurements. In practice, this type of sampling can be easily achieved by introducing a delay shift register which is running continuously, as depicted in Fig. 5.27. Since the time required to readout all FIFOs is in the order of seconds, the dead time is very high, fact which can be improved by reducing the FIFO size from 16k to the corresponding event size. In NEDA, normally 1k samples per event are enough, meaning that 512-byte FIFOs are needed. Even though there is a high dead time, in terms of event storage, it would mean to capture an average of 4 or 5 Hz, meaning that a timing histogram, which requires at least a minimal amount of 20.000 events would need at least 1 hour and a half, while a measurement used for NGD, involving at least 200.000 events would need between 11 and 12 hours to be completed.

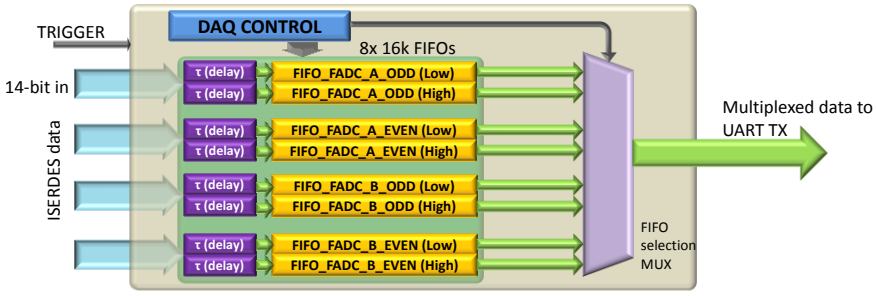


Figure 5.27: DAQ storage block diagram incorporating the TRIGGER functionality and the shift register used to store the pre-trigger samples

5.3.4. LabView graphical interface

The LabView-based software establishes the interaction between the user/designer and the FADC Mezzanine, becoming the control tool on the top of the hierarchy. The specifications for the software platform can be divided in the following points:

- Serial communication.
- FADC Mezzanine setup via graphical interface.

- Capability to perform data analysis such as noise measurements, parameters on the frequency domain, and DNL / INL.
- Data storage capability.
- Versatility to operate under continuous modes and triggered modes.
- GPIB communication with an arbitrary function generator.
- User-friendly graphical user interface.

The block diagram shown in Fig. 5.28 illustrates how the aforementioned points have all been gathered. Some of the most important blocks are:

- UART block initialization
- FADC Mezzanine setup and software reset: This blocks provides the commands which are converted to SPI to configure the Mezzanine.
- Data collection and reordering: Inside these blocks, the data captured by the UART is reorganized into raw data.
- FIFO: A buffer used to communicate the data between the producer and consumer loops, reducing the influence on the processing and the data acquisition.
- Data analysis block: Used to perform the calculations over the raw data and provide results useful to verify the data acquisition quality.
- Data storage block: Used to store optionally the raw data or the parameters evaluated after the analysis.
- Graphical user interface: Communicates with the user to enter parameters and visualize the data both in raw samples and after processing.

The following paragraphs are devoted to introduce more deeply each of the blocks. A first sub-section describes the code architecture, as well as each block separately, and the second subsection focuses on the graphical user interface.

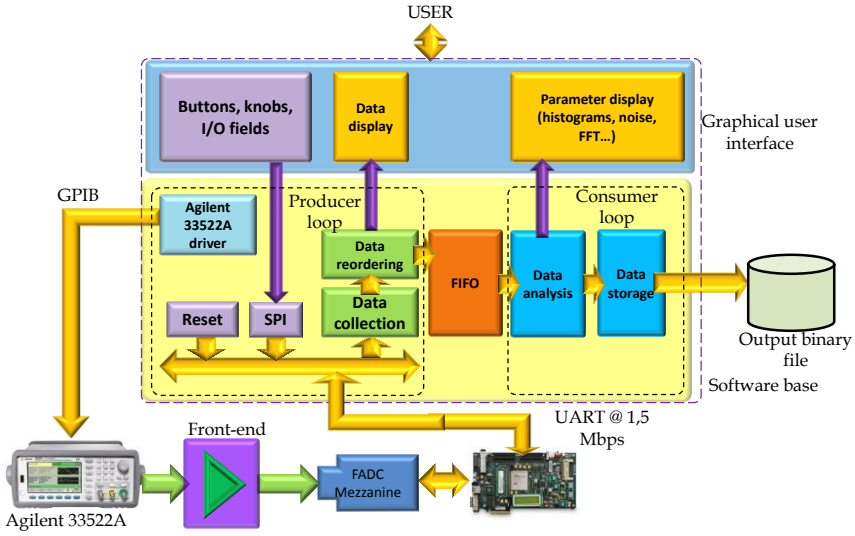


Figure 5.28: Software architecture based on the LabView platform

Code architecture

Since the application is envisaged towards data acquisition while performing as well data analysis and storage functions, a producer/consumer architecture [105] performs the best for our requirements. Hence, the code is divided mainly into two main loops, the producer loop and the consumer loop. Both loops are connected via a FIFO which delivers data from the producer to the consumer, avoiding to slow down the collection data process.

The producer loop assumes the FADC Mezzanine control tasks such as the reset and the register setup via SPI/μWire control. The GUI allows, by means of an easy-user interface to enter and read values from buttons, slides, etc, a value which is then packaged into a command sent to the FPGA and converted to SPI protocol. Data collection and reordering tasks are performed inside the loop as well, where the bytes from UART are reordered to build up the signal. Then, after all samples are taken, they are sent to the queue for further data analysis. A second functionality of the producer loop is the setup of the arbitrary waveform generator depending on the data analysis type being involved. For example, FFT-based measurements make use of sine waveforms while the baseline resolution tests do not need any input signal. All tasks are executed sequentially according to the flow diagram in Fig. 5.29.

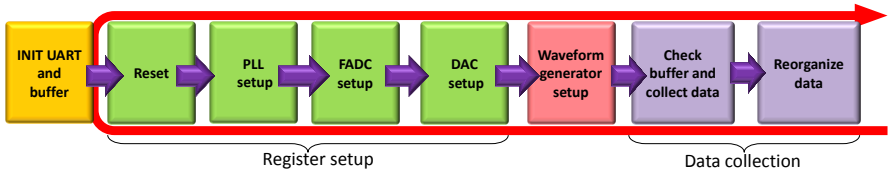


Figure 5.29: Producer loop sequence

Analogously, a similar structure is applied to the consumer loop, where the queued data is retrieved for data analysis, visualization and storage. Since not all type of data analysis is necessary simultaneously, it has been decided that only the one required will be applied. The decision on the type of analysis to be applied determines the generator setup; for example, a nonlinearity measurement needs a sinusoidal signal while a noise measurement would a sweeping DC signal. In total, a set of 4 analysis modes are programmed: Static measurements, DAC sweep, FFT measurements and nonlinearities. The program allows to store either the data from the analysis or the raw data. Additionally, a second smaller consumer loop verifies the reminiscent elements in the queue stopping the program in case of data overload. Some of the most important blocks are:

Serial port initialization. This first step configures the serial port to run at the fastest baud rate capable to work with LabView, at 1.5 Mbps. Other configuration settings are used to establish the utilization of parity bits (set by default to none), number of stop bits (set by default to 1) and timeout (set by default to 10 s). A second task initializes the size of the data collection buffer, set by default to 500.000 samples and checking out that it is empty before the FADC Mezzanine setup tasks.

FADC Mezzanine setup block and software reset. The software layer in LabView builds up the SPI/μWire commands based on the controls interacting with the user on the front panel. Recalling the data format exposed in table 5.2 and 5.3, each command gathers the data content plus the header delivering a 5-byte frame to the RX UART register.

The controls from the main control panel set boolean and numeric variables which correspond to the device configuration parameters. The register build-up consists of a set of arithmetic, shifting and string concatenation operations applied to these variables, resulting in a hexadecimal number which contains the final register value and the corresponding header, forming the 40-bit frame. Fig. 5.30 shows an example for the PLL register R0, showing the LabView controls involved in the register setup and the respective position within the register.

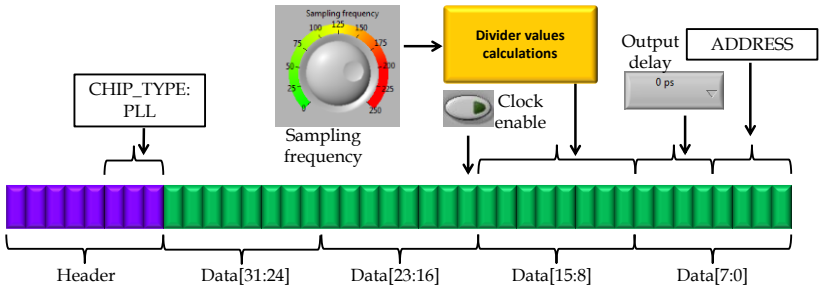


Figure 5.30: LabView frame build-up example for the PLL register R0-R7

Since the UART block works on bytes with string format, each numerical 40-bit frame must be separated in 5 bytes, swapped from LSB to MSB and reconverted to string format before sending the frame via serial port.

Generator control block. Placed in between the register setup and the data collection, this sub-block provides via GPIB the corresponding data to the arbitrary waveform generator Agilent 33522A. For static measurements and DAC sweep, the waveform generator remains off since no waveform is required to perform these analysis. In case the FFT mode is selected, the generator delivers a sine output based on the amplitude, offset and frequency parameters from the box 9 (Fig. 5.32). When nonlinearities measurements are involved, the generator is programmed with a coherent frequency and selectable amplitude after the user chooses a prime number of cycles to fit into the record.

Data collection block. Beforehand, the data collection block may be divided in two big tasks: data collection and data reorganization. While data collection captures the data received at the PC serial port, the reorganization block rearranges the bytes from the serial port into the original samples.

Data collection checks out firstly that the amount of data received at the UART corresponds with the size of expected data. Afterwards, using the UART VISA read block, these bytes are captured inside the buffer and stored in string format. The number of received bytes may change depending on the test carried out whereas each acquisition cycle captures a total set of 8 FIFOs each with a total depth *L*. Therefore, for FREE-RUNNING tests, the total amount of bytes must be set to 131072 bytes while tests with the TRIGGER mode reduce the total amount of data to 16384 bytes (each FIFO containing 2k bytes).

The second step consists of rearranging the data, providing the original 14-bit signal-wise format. The UART acquired string is converted to 8-bit integer and ordered. Then, the next process interlaces the odd- even bits into a single channel unit. The final set of data is a 16-bit integer array whose length is *2L*, being *8L* the total amount of data received at the UART. Fig. 5.31 represents graphically the reorganization method.

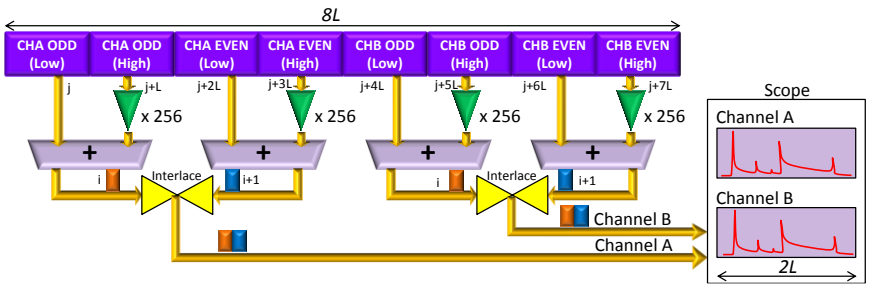


Figure 5.31: Data restructuring algorithm

Data analysis block. Being the main task inside the consumer loop, proceeds depending on the type of analysis detected. The simplest analysis mode is used for static measurements mainly devoted to calculate the baseline noise. With this mode enabled, the generator is disabled, the FADC seeing only the intrinsic noise from the rest of electronics. Simultaneously, in the visualization tab, the standard deviation is shown, both calculated in time domain, and after a Gaussian fitting function. Similarly, the DAC sweep mode provides the same statistical measurements but displaying in a screen the evolution of the mean value and standard deviation while the DAC input code code sweeps from 0x0000 to 0xFFFF, passing by as many steps as the user demands.

Frequency-based measurements make use of the power spectrum to obtain all its parameters, like the SINAD, SFDR, etc. Aiming to compare the real performance of the FADC Mezzanine, the tool provides the capability to select between the real acquired data and an internal generator capable to simulate a sinusoidal waveform, with capability to add noise and distortion. When performing the nonlinearities measurement, the software calculates the necessary amount of iterations to fit into the confidence (α) and β factor requirements. Afterwards, a sub-VI accumulates the histograms of the waveforms in order to perform the algorithm presented in section 5.2.3. As a result of how the INL / DNL measurements are implemented, the screen is refreshed in each iteration although the valid result is only shown after the program stops.

Data storage block. Simply this part of the program is dedicated to provide an easy procedure to store the acquired data and parameters in a binary format for a future retrieval, provided the LabView advantage to work with path variables. Among the functionalities it provides we can point out the option to select the channel to store, as well as the capability to store files automatically with increasingly-indexed self-created file names, useful in long-term acquisitions involving the storage of hundreds of thousands of files. Most of the code for this part is devoted to create automatically the file names provided an initial path.

Graphical user interface architecture

Because there is a big amount of parameters to be managed by the GUI, the interface is separated into several tabs, allowing to switch them during the acquisition. The tabs defined are:

FADC Mezzanine setup tab (Fig. 5.32). Contains most of the common parameters to set up the PLL, FADC and DAC, a ring controller which allows to select the type of analysis and the arbitrary waveform controls. Each type of analysis includes its own parameters, where the ones which affect the generator control are included in this tab.

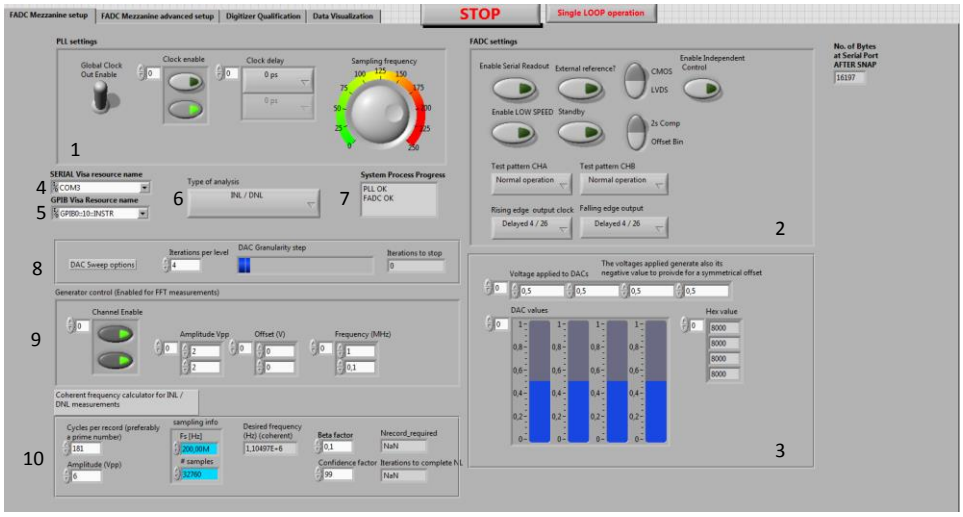


Figure 5.32: GUI screenshot. Main control panel

The controls and indicators can be described as: **1.** PLL settings (clock delays, sampling frequency and clock enable). **2.** FADC chip settings such as the output clock phase, data mode (CMOS / LVDS), power down modes and the output data format (2s/binary offset). **3.** DAC voltages normalized to a scale from 0 to 1. **4.** Serial port COM. **5.** GPIB port. **6.** Type of analysis undergoing (static / DAC sweep / FFT / Nonlinearities). **7.** Process indicator box. **8.** DAC sweep mode controls, including number of steps and number of measurements per step. **9.** Signal generator commands for the FFT mode. Among others, it allows to enable / disable the channel and select the offset, amplitude and frequency. **10.** Commands for the INL / DNL measurements such as the degree of confidence and the amplitude. The frequency is delivered automatically using a coherent frequency calculator, based on the number of points and sampling frequency.

FADC Advanced Mezzanine setup tab (Fig. 5.33). It allows to write directly the value of the register, including some specific registers which are set in the main tab as default values. This tab it is useful mostly during the FADC Mezzanine prototype testing.The controls and indicators can be described as: **11.** FADC registers. **12.** PLL registers. **13.** DAC registers.

Data analysis tab (Fig. 5.34). Provides a more extensive assortment of measurements involving noise characterization, frequency-domain and nonlinearity measurements. The set of measurements being displayed may be enabled / disabled concerning the type of measurement carried out.

The controls and indicators can be described as: **14.** DAC sweep evolution measurements of mean values in a) and standard deviation measurements in b). **15.** Power spectrum. **16.** Frequency-based measurements, such as the ENOB (taken from the spectrum), SINAD and SFDR. **17.** Test generator (performed inside LabView) controllers. It is used to compare the performance of the acquired signals to a theoretical waveform. **18.** Optional low-pass and high-pass filters options. Channel selection (either A or B) and acquired / theoretical

waveform selection button. **19.** Signal histogram. **20.** DNL screen. **21.** INL screen. **22.** Nonlinearities numerical results (Maximum DNL and INL values, range coverage).

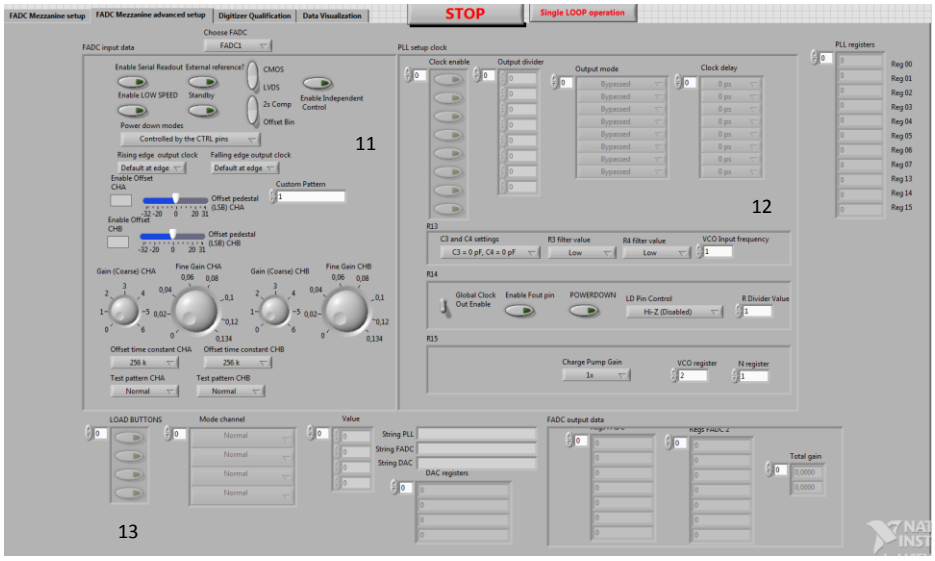


Figure 5.33: GUI screenshot. Advanced register setup panel

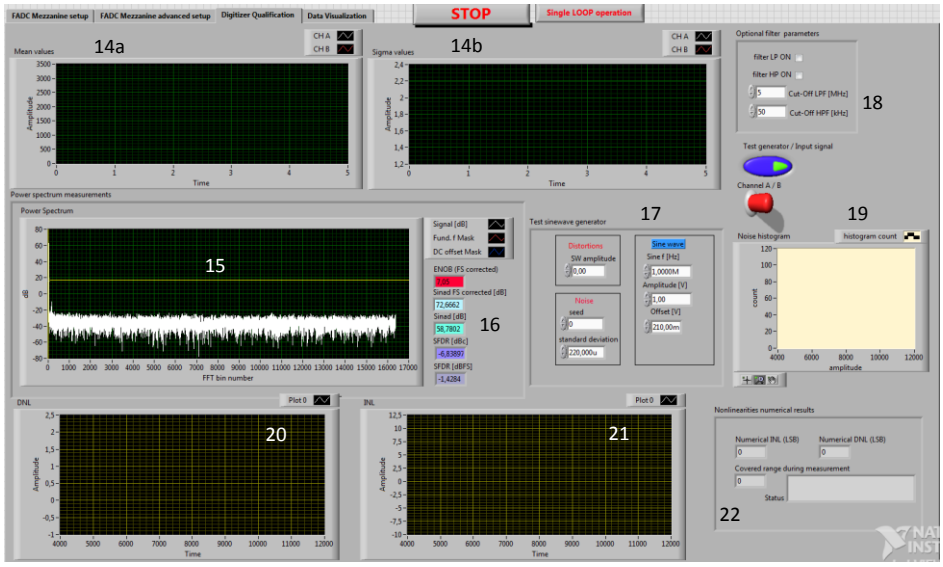


Figure 5.34: GUI screenshot. Data analysis panel

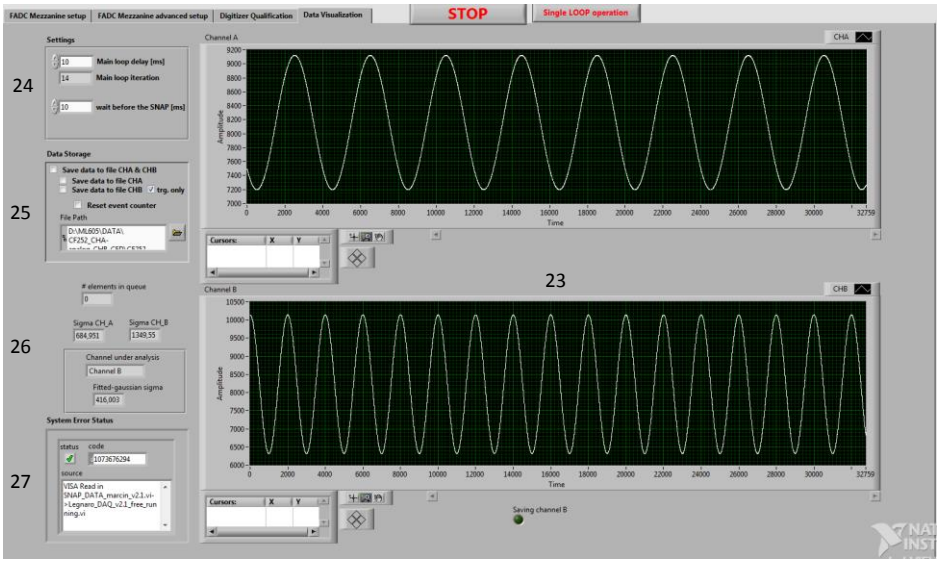


Figure 5.35: GUI screenshot. Data visualization panel

Data visualization tab (Fig. 5.35). Displays the acquired signal after reorganization, as well as a small assortment of parameters which provide an approximation regarding data quality. Besides, within this tab, the options regarding data storage are included as well.

The controls and indicators can be described as: **23.** Signal display in time domain. **24.** Timeout settings. **25.** Data storage settings and trigger mode settings. **26.** Standard deviation measurements used to evaluate the signal resolution. **27.** Error status box.

Chapter summary

In this chapter, the design of a test platform aimed to verify the FADC Mezzanine functionality has been described. Firstly, the parameters used to evaluate and characterize commercial ADCs have been presented, followed by the definition of energy resolution in the context of nuclear physics. Then, the hardware and software elements have been studied, building up step by step the whole system.

The results obtained using this testbench platform are shown and commented in chapter 7, leaving the chapter 6 for the firmware integration topics.

6. Integration and firmware development

The present chapter is divided into several sections corresponding to the different tasks performed concerning NEDA NUMEXO2 firmware development and adaptation. Firstly, we introduce the integration of the FADC Mezzanines in the NUMEXO2, preparing the device for its use in an application different from the EXOGAM2 one. This task has been initially carried out for the EXOGAM2 electronics since most of the firmware blocks have been developed for this instrument by GANIL. The setting up all with the corresponding firmware allows to verify the whole electronic chain, starting from the HP-Ge crystals until the DAQ acquisition system.

After verifying that the electronics chain was working for the EXOGAM2 case, the NUMEXO2 board firmware was studied to adapt it for NEDA requirements. In this chapter, a gamma-neutron discrimination algorithm is discussed, with the goal to provide a first-stage neutron trigger to the GTS, aiming as well at minimizing the amount of data transfer that could be produced by gamma-rays. Concerning that gamma-neutron discrimination (NGD) algorithm, we will discuss first the set of algorithms studied in reference [61]. Then, the discussion will be followed by the description of the implementation of one considered optimal for the first-level trigger. Given the necessity to speed up this development, some of the IPs required for NEDA have been firstly evaluated using part of the testbench presented in the previous chapter. The goal of using the test platform to integrate the gamma-neutron discrimination algorithm IPs is the verification of the block itself and its connection to the GTS provided a smaller version of the electronic chain. After verifying the NGD IP inside the testbench, the next step consisted of implementing the IP in the real NUMEXO2 board.

6.1. Integration of the FADC Mezzanine in EXOGAM2 and NEDA electronics

The integration of the FADC Mezzanine started as soon as the verification of the latest prototype confirmed that the specifications for all detectors were met. Concretely the process started in February 2014 at GANIL, and then continued afterwards in the respective laboratories where the development of electronics related to NUMEXO2 were taking place. This is the case of the NUMEXO2 card for NEDA, whose development will take part in Valencia. Therefore, the integration of the whole electronics chain involves the usage of all hardware, firmware and software tools.

6.1.1. Initialization process

It was preferred to leave a section to explain the whole initialization process of NUMEXO-2 and the DAQ. Furthermore, the software tools, developed by GANIL, required to configure NUMEXO2 and perform the data acquisition are also presented. A sub-section is dedicated mainly to the hardware initialization, confirming that the firmware has been properly

downloaded either in the FPGAs or in the Flash memories. Then, the second sub-section describes the software tools and the procedure to launch the acquisition.

NUMEXO2 initialization and firmware downloading

The initialization process can be separated into the following sub-stages: Power-up, firmware downloading into the flash memory and setting up the basic parameters in NUMEXO2. An issue to remark is the NUMEXO2 card labeling, which indicates which of the pre-series modules are used for its corresponding application. Table 6.1 summarizes the application of each application. From all of them, only NUMEXO2-3 and NUMEXO2-5 have been used for these tests.

Table 6.1: NUMEXO2 labeling with its corresponding detector

Board label	Application
NUMEXO2-1	EXOGAM2 prototype
NUMEXO2-2	EXOGAM2 prototype
NUMEXO2-3	EXOGAM2 pre-series
NUMEXO2-4	EXOGAM2 pre-series
NUMEXO2-5	NEDA pre-series
NUMEXO2-6	S3 pre-series
NUMEXO2-7	PARIS pre-series

The process starts by powering up and downloading the corresponding firmware into the dedicated flash memories. Firstly the power-up sequence was performed without Mezzanines, which were added after the firmware downloading. This allowed to verify the power consumptions in both conditions. The NUMEXO2 card was powered verifying its power-up sequence, obtaining a total amount of 25 W without including the Mezzanines. When placing the FADC Mezzanines, the power consumption raised to 50 W approximately.

Regarding the initialization process, each FPGA is linked to its own JTAG chain. The Virtex-6 includes two 32 MB EEPROMs capable to be configured either separately (2 different *.bit files can be stored), or in a master-slave mode (a bigger file can be stored). A second JTAG port allows the use of Chip-Scope Pro during the development phase. This configuration can be set by using several jumpers in NUMEXO2. The procedure to download the firmware in the Virtex-5 –since it contains an embedded processor with an operating system- requires a particular sequence: firstly the *.mcs file (containing the V5 firmware) must be downloaded into the flash memory, afterwards, the bootloader file which includes the Linux embedded IS is stored into a second flash memory. Finally an I2C small PROM memory containing data about NUMEXO2 identification parameters such as the IP is programmed. During the first V5 firmware download, it is need to set up the processor parameters, e.g. regarding the NUMEXO2 identification and communication, such as the MAC address IP address and the serial port baud rate. The booting procedure can be seen using a Linux terminal dedicated to check the sequence from the serial port.

Software tools and DAQ launching

Whenever NUMEXO2 is powered-up and correctly booted, the start-up and data acquisition process can be launched whenever a TCP/IP connection is available. At this point, the different software tools can already be used. The first tool to verify that the FADC responds correctly to the SPI commands delivered from NUMEXO2 is the GECO tool. GECO is in charge to send slow control commands through the TCP/IP. As some of the devices in the FADC Mezzanine can be written but not read back, a set of mirror registers implemented in Virtex-5 allow GECO to read the value of those values. However, correct behavior of the FADC

Mezzanines and NUMEXO2 under the GECO commands has been verified checking the overall functionality of GECO commands. Fig. 6.1 shows a screenshot of the control interface GECO.

Figure 6.1: GECO screenshot while running. Courtesy of GANIL

After verifying the NUMEXO2 slow control functionality, the next step is to check the DAQ – named NARVAL -. Presently, until the integration of the NUMEXO2 initialization in the RC (Run Control), in order to perform the start/stop DAQ operations, they must be performed both at the NUMEXO2 board and inside the RC GUI. Furthermore, the command sequence must start with the NARVAL part, preserving the NUMEXO2 start in the second stage. The RC control shows a grid where several actions such as add/modify/delete can be applied over each actor[17]. By default, a catcher actor, a watcher actor and a storage actor (which shows itself as disabled) is shown. For this particular setup, the catcher actor makes reference to the NUMEXO2 board read-out process, then, the watcher actor role is to sort and analyze data, as well as the performing the histograms using the GRU libraries for further visualization. Finally, the storage actor refers to the code in charge of writing the data in the disk unit, although in the configuration shown, the latter is disabled. Before acting on NUMEXO2, the RC must be put into monitoring mode, then, the initialization and start processes can be started from the GUI by pressing their corresponding buttons. A screenshot depicted in Fig. 6.2 shows the system running. Between actors the data transfer rate is also depicted.

[17] *An actor, in this context, stands for a processing unit, i.e. a program that performs a certain action in the data flow. Examples of actors are: producer/catcher, watcher, consumers and storage units.*

Figure 6.2: RC GUI shows the running processes in NARVAL. Courtesy of GANIL

Once NARVAL is started, the NUMEXO2 start command can be sent through the SC_client terminal. Before starting the data taking in NUMEXO2, the SC_HOST and SC_PORT environmental variables must be set to "*numexo2-x*" and "*8061*", where x refers to the NUMEXO2 identifier (in case of NEDA is numexo2-5). According to the FSM (Finite-State Machine) depicted in Fig. 6.3, every command through the SC_client refers to a transition into the diagram, until starting the data taking process after applying 'start'. Once all commands are applied, it is possible to see in the RC window that the data is processed by the different actors, thus it is possible to verify the correct behavior of the acquisition system.

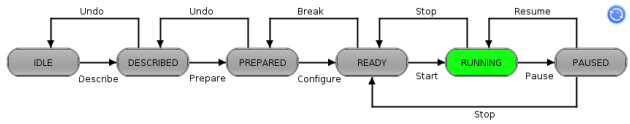


Figure 6.3: FSM describing the transitions to start the acquisition in NUMEXO2. Courtesy of GANIL

Following the start of the data taking, the next step consists of launching the histogramming process GRU and the display process ViGRU. GRU can be launched by running a GruScript.c. Inside ViGRU, it can be selected the channel to plot the energy spectra histogram inside a preselected window. The 6 MeV central contact was selected to illustrate the display of the spectra. Displaying and limited analysis of the spectra, provided by ViGRU has helped the commissioning of the FADC Mezzanines inside NUMEXO2 and the DAQ system.

6.1.2. Setup to test the energy resolution

During the week from 11th to 14th February, 2014, tests with radioactive sources were carried at GANIL to measure the energy resolution in closer conditions to the experimental environment. Firstly, a ^{60}Co source with counting rate < 100 Hz, placed 20 cm away from the detector, was used to check the energy range and the obtained energy resolution was used to verify the specifications in terms of ENOB. A second calibration using ^{152}Eu was then used to expand the calibration for a wider range of energies. The experiment included the clover EURISYS S07 from the EXOGAM detector attached to a B3 connection box, whose power supply was provided externally. The digitizer NUMEXO2 was linked via the HDMI 10-m long cable using the latest FADC Mezzanine version 5 with G=1, sampling at 200 MHz and 50 MHz bandwidth. The experimental setup is shown in Fig. 6.4.

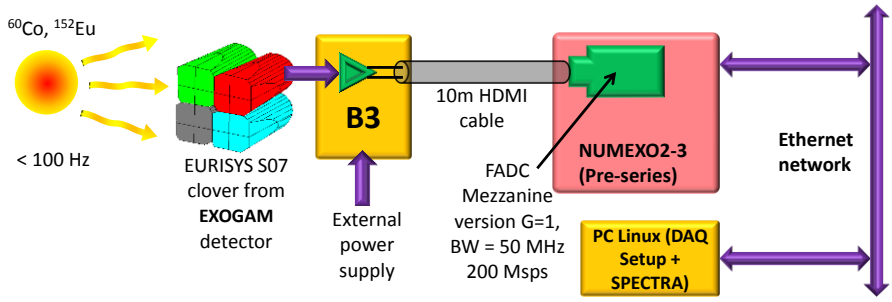


Figure 6.4: Experimental setup used to perform energy resolution measurements with the EXOGAM detector using NUMEXO2 digitizer and the FADC Mezzanines.

Regarding the hardware material used to assemble the electronic chain setup at GANIL, it is required:

- A NUMEXO2 motherboard. Concretely for the tests, the NUMEXO2-3 was used.
- Minimally 1 FADC Mezzanine.
- 1 HDMI 1.4 Infinite cable
- A B3 connection box
- A clover HP-Ge detector. Alternatively, a pulse generator capable to emulate the pulses from the detector can be used to verify the electronics.
- A NIM crate to provide power supply to the NUMEXO2 motherboard and thus, to the FADC Mezzanines mounted on it.
- An external power supply to provide energy to the connection box.
- An Ethernet cable to link the EXOGAM2 data output to a PC. Optionally a second RJ-45 cable might be used to visualize the status of Virtex-5 booting although depending on the computer it requires a converter to DB9 or USB.
- A Linux PC, preferably containing the CentOS 6.5 and the following tools used by GANIL.
    - GECO (Ganil Electronics Control). This software it is used mainly to read and write the NUMEXO2 registers. GECO is provided with a friendly GUI, which allows, among other things to select inspection lines, read and configure the ISERDES delays, observe the oscilloscope mode and set parameters of the MWD.
    - Narval and the Running Control GUI. Narval is the data acquisition core system and it involves not only EXOGAM2. Narval is envisaged to be used for AGATA and other experiments. In order to add the actors in charge of carrying out a certain task, Narval can be controlled from the RC (Running Control) GUI.
    - GRU and ViGRU. Applications based on the Root data analysis tool developed at CERN, GRU (GANIL Root Utilities) is a set of libraries to cope with the analysis tools required for the experiments performed at GANIL. ViGRU (Visual GRU) is an additional tool used to illustrate the spectra and the results whose analysis was carried by GRU.
- Optionally, LEMO cables can be connected to an oscilloscope to visualize the signal seen by the inspection lines.

In order to have realistic energy resolution measurements, the FADC Mezzanine settings were stablished to unity gain and antialiasing cut-off frequency of 35 MHz. The parameters which optimize the response of the trapezoidal filter both in terms and counting rate were K = 18 μs (slope time of the trapezoid, both for the rising and falling part) and M = 2 μs (flat-top part of the trapezoid). Finally, in order to perform spectra, a notorious amount of events was required to perform statistics, taking at least 100.000 events to perform the energy spectra.

GANIL software tools such as GECO, ViGRU and NARVAL were used to interact between the user and NUMEXO-2. The results of the energy resolution measurements are shown in the next chapter, followed by a conclusion of using the FADC Mezzanine for experiments in the EXOGAM2 detector environment.

6.1.3. The test setup for the NEDA NUMEXO2 card, the GTS and the PCIe readout integration

After the setting of the test setup in GANIL, a test setup for the NEDA full electronics chain was installed in Valencia with the aim to reproduce the same setup as the tests carried out in GANIL, and also using the prototypes for future NEDA developments. The goal of doing this is to establish a starting point in order to develop firmware for NEDA by reusing part of the firmware used for EXOGAM2. It is necessary to point out that most of the tools, firmware and software from GANIL setup, have been reused with a few adaptations. Fig. 6.5 shows the elements used for the tests.

- To avoid the complication of using the detectors during the test, the waveforms were generated using the waveform function generator Agilent 33522A, programming via LabView the corresponding EXOGAM2-like pulses with 100 ns rise time, 50 μs exponential decay time and selectable gain.
- The B3 was replaced by the prototyping version of the single-ended to differential board. As well as the B3, it was supplied externally.
- The FADC Mezzanine versions used for the test setup correspond to the Mezzanine V5, with gain settings set to 1 and bandwidth to 35 MHz, according to the same setup performed in GANIL.
- Two different NUMEXO2 boards were used for the prototype. Firstly, the prototype NUMEXO2-3, envisaged to be used for the EXOGAM2 experiments was firstly tested, performing the same setup as in GANIL. Afterwards, the board was replaced by the NUMEXO2-5, which is the prototype expected to be used in NEDA.
- The firmware downloaded in both FPGA devices Virtex-5 and Virtex-6 belong to the firmware used for EXOGAM2, developed by GANIL. After the functionality of the whole system was verified using the NUMEXO2-3 for EXOGAM, the next step consisted into testing the same firmware using a different board, concretely the NUMEXO2-5 for NEDA. Regarding the firmware versions used for the test, the Virtex-6 contained the latest fully operative version while the Virtex-5 used a version capable to deal with 2 trigger requests (coming from the inner channels CH0 and CH8).
- The control interface and DAQ was performed using GANIL software tools of GECO, GRU, ViGRU and NARVAL. All tools were installed in a PC of our laboratory using the same OS (CentOS 6.5), in order to reproduce exactly the same environment as in GANIL.

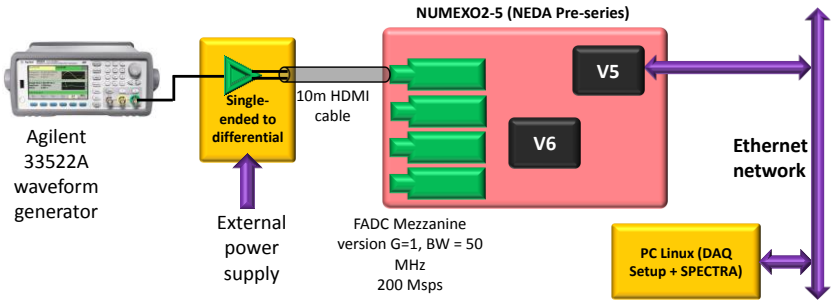


Figure 6.5: Experimental setup used to verify the functionality of NUMEXO2-5 using EXOGAM2 firmware and GANIL DAQ installed in Valencia

Therefore, using the aforementioned elements, the tests consisted on:

- Verifying the correct behavior of the FADC Mezzanines on both NUMEXO-2 boards (the one used for EXOGAM-2 and the one used for NEDA).
- Verifying the correct behavior of the firmware envisaged for EXOGAM2, using both NUMEXO-2 boards.
- Verifying a correct interaction between the software tools and both NUMEXO-2 boards using the tools installed in the PC emplaced in Valencia.

After the hardware and software tools were properly installed, the three points mentioned above were carried out, commissioning the system integration in Valencia, and establishing a starting point for NEDA firmware developments. Figs. 6.6 and 6.7 show pictures of the setup block diagram from Fig. 6.5. Specially, Fig. 6.7 shows a detail of the NUMEXO2-5, currently working.

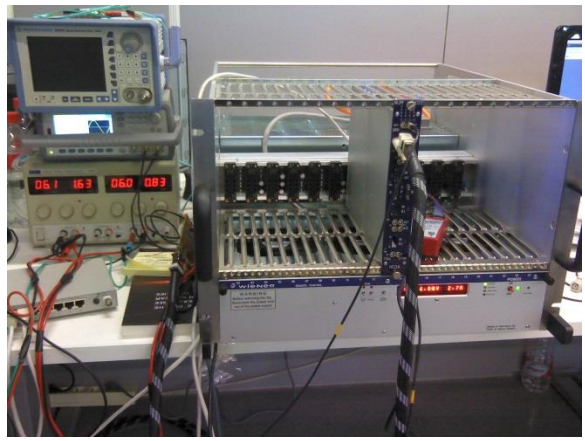


Figure 6.6: Picture of the testbench performed in Valencia

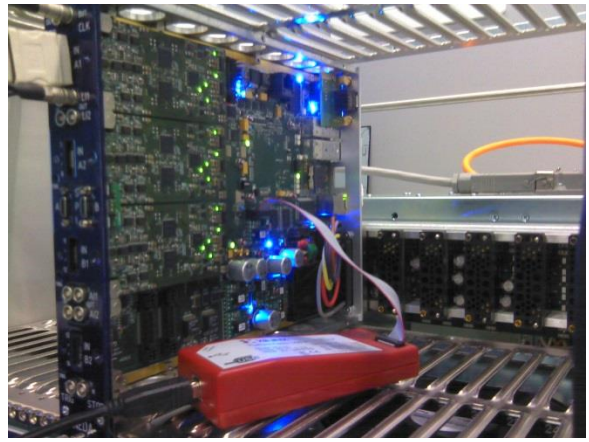


Figure 6.7: Picture of NUMEXO2-5 with 3 FADC Mezzanines working in a high-power NIM crate. Tests performed in Valencia

GTS integration tests

After the verification of the NUMEXO2-5, the next step consisted into adding a small GTS tree to the system, formed by a root module, a fan-in fan-out and a leaf. The tests were carried out both using NUMEXO2-3 and NUMEXO2-5. Furthermore, additional software tools to manage the GTS severs were also used. The goals to achieve with this tests are:

- To build a small GTS tree in Valencia, using the GTS carriers both from EXOGAM2 and NEDA.
- Observe a proper interaction between NUMEXO2 and the GTS, verifying that the GTS delivers validations when working in all-validated mode.

To perform this test, the following elements were used:

- A NUMEXO2 digitizer, which contain the corresponding firmware for 2 trigger requests.
- 4 FADC Mezzanines (even though for the tests carried out, 2 out of them are enough since the TR are received from channel 0 and 8)
- 4 GTS V3 Mezzanines (can correspond either to leaves, fan in-fan out or root modules)
- A GTS Carrier board.
- A NIM crate.
- A Linux PC with CentOS 6.5 to launch the acquisition and configure both the NUMEXO2 board and the GTS Mezzanines.
- Optical SFP transceivers (depending on the tree size, but maximally, 10)
- 4 LC/LC fibers
- LEMO cables used to (for the inspection lines)
- A generator to produce trigger requests. Agilent 33522A was used.
- An oscilloscope
- A Xilinx USB II programmer
- An Ethernet switch and 3 Ethernet cables to build up the network.

- No trigger processor was used for the tests, meaning that all the collected trigger requests were validated.
- Firmware: Regarding the firmware, the same versions as the ones used to perform the test described in the previous section were used, both for the Virtex-6 and for the Virex-5. Therefore, the GTS can only accept 2 trigger requests from NUMEXO-2.

Fig. 6.8 shows a block diagram of the electronic setup, showing also the connections to the GTS tree. In addition to the standard initialization process described in section 6.1.1, when the GTS tree is added, a set of extra steps must be followed. Firstly, each GTS Mezzanine must contain its own dedicated firmware to work as a root, fan-in fan-out module or leaf. After the firmware downloading and powering up, the boards can be located using ping commands through the Ethernet network, ensuring that all GTS modules and NUMEXO2 are connected. For this step is not required to have the optical connections.

The next step consists of launching the GTS server and building the GTS tree. For the tree building, optical connections must be properly connected. Both steps can be performed by executing the gts_server and the ManualGTSControl.sh scripts, developed by GANIL. Later on, the clocks from NUMEXO2 and the FADC Mezzanines must be synchronized with the GTS clock. This operation is performed by using GECO to act on the synchronization signals of the NUMEXO2 PLLs. After synchronizing the clocks, the steps from section 6.1.1 can be now used to launch the acquisition system and put NUMEXO2 in a run state so that it can deliver trigger requests.

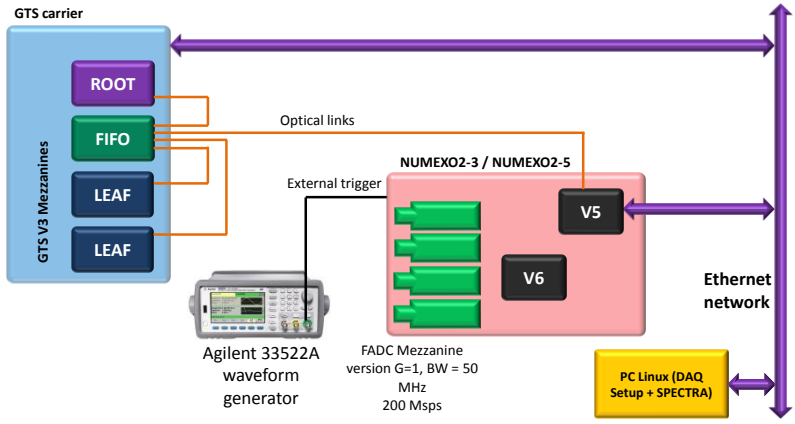


Figure 6.8: Experimental setup used to verify the functionality of the GTS together with NUMEXO2

Trigger signals for this experiment were driven using the Agilent signal 33522A waveform generator, where a simultaneous request was delivered to channels CH0 and CH8 – EXOGAM inner channels – In order to verify the correct behavior of the GTS connections, a Chip Scope instance was launched in Virtex-5 to visualize the number of accepted trigger requests for each channel, confirming the performance of the GTS system with NUMEXO2.

Tests with the PCIe

Another integration test carried out is the readout verification using the PCIe protocol. The main goal of this experiment is to verify the continuity and performance of the datapath between the FADC Mezzanines and the PC, passing through the Virtex-6, Virtex-5 and the external FIFO in NUMEXO2.

The elements used to carry out the integration of the PCIe readout data are:

- The NUMEXO2-3 board used for EXOGAM2.
- A NIM crate.
- FADC Mezzanines. At least one of them is necessary to visualize data.
- A Linux PC computer with the GANIL tools installed. Mainly, the only tool important for this test is GECO, which is used to configure the FADC Mezzanines and Virtex-6.
- A LINCO2 card with 4 lanes.
- A PCIe-compatible PC. For our case, the Intel Power Edge 1800 was used.
- Ethernet cables and a switch to provide connection to the PC Linux and NUMEXO2.
- A 4LC/LC optical fiber to link NUMEXO2 and the LINCO2 board.
- Firmware elements: the firmware used in the Virtex-5 belongs to a newer version containing the drivers for the PCIe (GTSupgrade_PCIe_iserdes.bit) while the firmware for Virtex-6 remained the same as in the aforementioned experiments.
- Software tools: The data acquisition tools used for the data readout of the PCIe are the Dalton Test Acquisition, developed by IPNO.

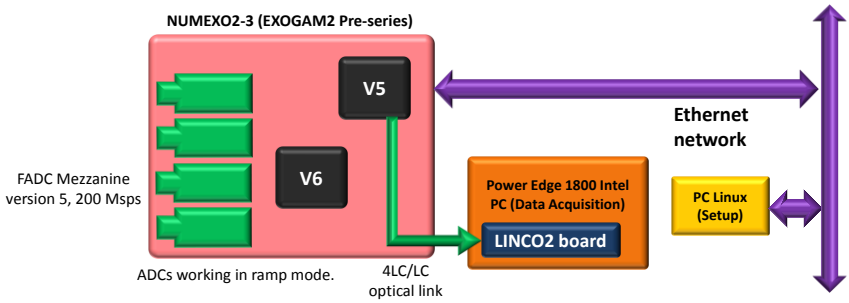


Figure 6.9: Experimental setup used to verify the functionality of the PCIexpress together with NUMEXO2

After having installed successfully the Dalton Test Acquisition in the Intel Power Edge PC, the experiment made use of the FADC Mezzanine test models in order to deliver a ramp function. Configuring this mode can be achieved using GECO, installed in the Linux PC. The tests confirmed the experiment suitability by displaying in the PC the ramp waveforms. However, the waveform was showing some peaks, fact for which the firmware in the Virtex-5 must still be modified. Fig. 6.10 shows an screenshot of the DAQ used to read out data from the PCIe.

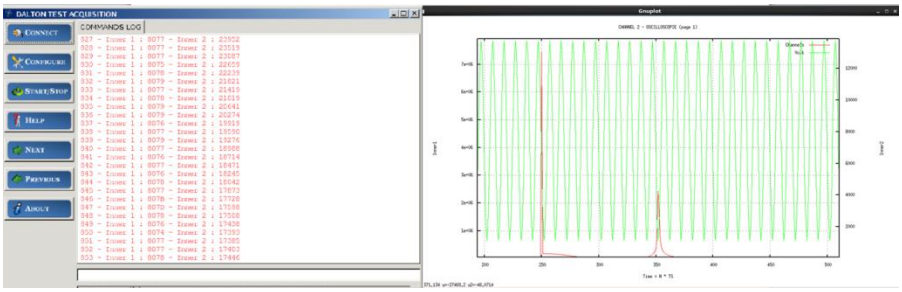


Figure 6.10: Screenshot of the Dalton Test Acquisition running. Courtesy of GANIL

6.2. Design of a PSA algorithm for NEDA. Integration in an evaluation board

In this section, two main topics are discussed: First, the study of the PSA neutron-gamma discrimination and their feasibility to implement them into FPGAs. Taking profit of the testbench platform developed for the Mezzanine tests (described in chapter 5), the first stage consisted on the implementation of the algorithm into the testbench before bundling all blocks together inside NUMEXO2. Finally, the whole GTS system was implemented as a second stage to verify the functionality of the trigger request cycle, following the results of the NGD algorithm.

6.2.1. Pulse-shape discrimination methodologies used in neutron-gamma discrimination

Neutron detectors based on organic scintillators are sensitive to gamma rays as well, requiring an on-line method to distinguish between neutrons and gammas. Using a real-time processing technique to deal with the discrimination would increase the overall system efficiency by rejecting the events produced by gamma-rays, avoiding to waste processing time since only neutron events are of interest. As mentioned in previous chapters, the liquid scintillator BC501-A provides the capability to discriminate between gamma-rays and neutrons, on the basis of the shape of the signal, through the Pulse Shape Analysis.

Based on the knowledge of the interaction of particles with matter, a sizeable number of pulse-shaped based methods to deal with the discrimination between particles and gammas were developed. In our implementation, the goal of a “hardware” NGD algorithm is not to discriminate unequivocally all neutrons from gammas, but to eliminate most of the events produced by gamma-rays using simple algorithms. The accurate NGD techniques, require usually complex algorithms, for example the ones based on neural networks [56], an issue which is not sought to provide only a first-level trigger request, focusing rather more in simple and robust algorithms which can be implemented in FPGA for larger amount of channels. Two simple methods are compared for implementation, namely the charge-comparison method (CC) and the IRT (Integrated rise-time) method [55, 63].

The charge-comparison method

The charge comparison method provides discrimination information based on the differences on the integrated charge evaluated in different waveform time windows. In Fig. 6.11, averaged gamma-ray and neutron waveforms, normalized to the amplitude are shown. It is easy to note that these waveforms have two different parts, namely the fast component – that follows the rising of the pulse – and the slow component – the tail of the signal. It is evident in the figure that once the amplitude is normalized, the tail differs so much between gamma-rays and neutrons, that allows the discrimination between them. This method establishes that the ratio δ defined between the integrals applied to the slow component and the fast component, provide a parameter to discriminate between neutrons and gammas.

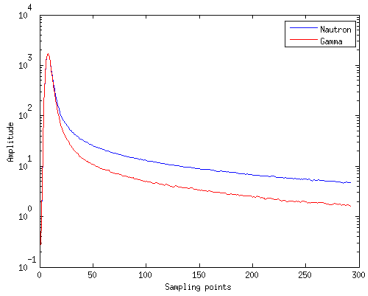


Figure 6.11: Examples of average neutron (blue) and gamma-ray (red) acquired waveforms. It can be noticed the difference in the decay time, due to the different scintillation components excited when the neutron and the gamma-ray deposit the energy in the detector media.

Equation 65) describes mathematically the method in terms of the fast and slow integration times α and β, respectively. In the digital approach δ becomes into $\hat{\delta}$, and therefore, the integrals are calculated as sums given the number of samples from α and β:

$$\delta = \frac{\int_{\beta} v(t)dt}{\int_{\alpha} v(t)dt} \rightarrow \hat{\delta} = \frac{\sum_{n=\alpha+1}^{\beta+\alpha} v(n)}{\sum_{n=1}^{\alpha} v(n)} \qquad 65)$$

Even though the digital implementation of the charge-comparison method is straightforward, its calibration by analog means entails difficulties due to the usage of two different time gates. Hence, for this reason, the method has not been widely used in analog electronics, becoming more popular the zero-crossover method with constant fraction discriminator.

The Integrated rise-time (IRT) method

The IRT method bases the clue on of the NGD based on the time difference after the integrated input pulse overcomes a predefined set of thresholds. These two thresholds (set respectively to the 10% and 72% of the pulse height) determine the start and stop point at which the time measurement should be taken, being, for the case of neutrons a usually longer time as it can be seen in Fig 6.12 [63].

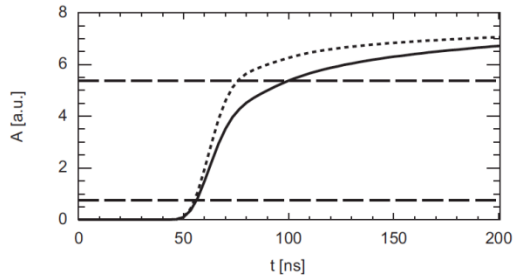


Figure 6.12: Processed averaged pulses. Difference between the integrated rise times for a gamma-ray (short-dashed line), and a neutron (solid line). The points at 10% and 72% of the pulse height are indicated by long-dashed lines [63]

The performance one can expect by implementing this algorithm is highly dependent on the precision provided by the time measurement. Hence, by looking at Fig. 6.12, the IRT measured for neutrons lies around 40 ns, while for gamma-rays the average is between 15-20 ns. As the clock period (5 ns) is on the order of the measurements, a performance enhancement can be obtained by means of interpolation, although this largely affects the FPGA resources, which should be taken into account for the implementation.

Comparison and choice

The comparison has been done considering both neutron/gamma discrimination performance through the figure of merit and the algorithm complexity. Based on [63] both algorithms of ZCO based on IRT and the charge comparison method present a similar figure of merit *M*, although the performance for the IRT is slightly larger according both to Fig. 3.17 and Fig. 3.18. This would make somehow IRT a more suitable option in principle.

On the other hand, analyzing the computational complexity for both algorithms, the charge comparison method requires at least 3 integrators (fast part, slow part and baseline removal unit), plus a multiplication hardware unit so that the baseline can be removed depending on α and β. IRT algorithm operational principle is simple, it only requires two integrators (one for the signal and another for the baseline removal). Although dealing with the thresholds is simple, the algorithm becomes dramatically more complex when dealing with time measurements resolutions below the clock cycle. Since the period measurement is on the order of magnitude of the clock cycle, IRT performance can be largely decreased, hence, being interpolations inside the FPGA a must. Based on the fact that at this stage of the processing, the algorithm simplicity becomes a major factor, both algorithms have been compared without using interpolation units inside the FPGA.

In views of the complexity demanded by the IRT when performing interpolation, the fact that the figure of merit provided by IRT is not much better than the one provided by the charge-comparison method, and the robustness of the charge-comparison method even working at the clock cycle, these facts have led the charge-comparison method to be chosen as the first option for the neutron-gamma discrimination based on pulse shape analysis implemented in an FPGA.

6.2.2. Implementation of the charge-comparison method in a Virtex6 using the ML605

The prototyping of the NGD implementation has been performed using the FADC testbench platform, acquiring only 2 channels. Integrating the pulse shape analysis block with the rest of the firmware requires communication with the ISERDES allowing the data to come into the PSA processing, a Chip Scope Pro logic analyzer to visualize the results from the integration, and the blocks in charge to perform the FADC Mezzanine configuration, which are the UART and the SPI. Fig. 6.13 shows the interaction of the PSA block with the rest of the firmware.

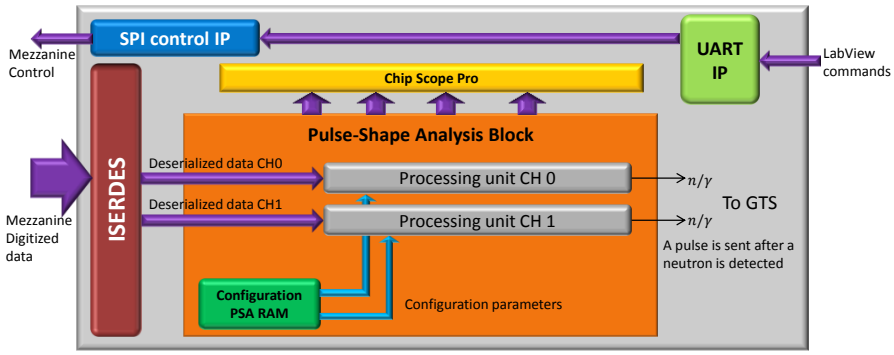


Figure 6.13: Interaction of the PSA block with the rest of the firmware in the testbench platform

Internally, the PSA block can be divided into two different parts: the configuration part and the processing unit. Inside the configuration block, a small RAM stores the parameters related to the PSA which shall be used on the processing unit, whereas the second block performs all the operations. Unlike the configuration block, which is a common block, the processing unit requires to be replicated individually for each channel. Later on the real implementation of the PSA process in NUMEXO2, the RAM will be replaced by the IP set-up registers.

The PSA configuration block. Memory map

Any variable which shall be used during the PSA analysis as a parameter such as α and β, as well as specific controls interacting into the PSA block are stored into a small RAM during the prototype phase. The memory map is structured as depicted in Fig. 6.14. Most of the parameters stored into the RAM are then used either in the processing unit or on the rest of the PSA block as control bits for test purpose.

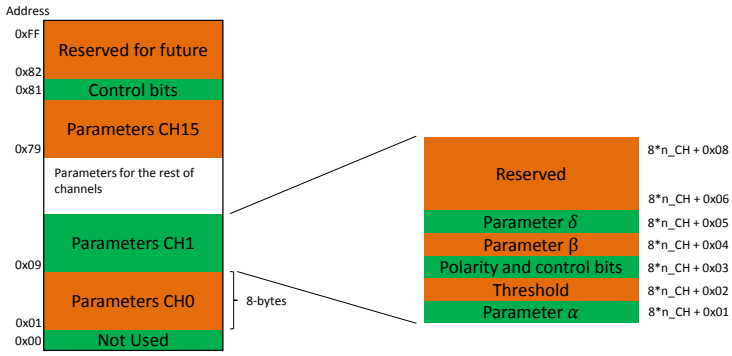


Figure 6.14: PSA RAM memory map

The RAM organization scheme shows a region from 0x01 to 0x80, which is dedicated to store the parameters for each individual channel. The space reserved for each channel contains 8 bytes and is structured as follows:

- 1 byte for the α parameter (fast integration number of samples)
- 1 byte for the β parameter (slow integration number of samples)
- 1 byte reserved for control bits regarding an individual channels: These controls concern the signal polarity and the possibility to activate a serial readout.
- 1 byte used to adjust the signal threshold which starts up the integration.
- 1 byte used for the $\hat{\delta}$ parameter, also called discrimination parameter, which is used at the end of the calculations to compare both integrations.

The processing unit

The processing unit lays out the main core of the PSA block, implementing the charge comparison method to carry on the first-level trigger for NGD. Given the raw data as an input, the processing unit delivers a signal to the GTS leaf if the event analyzed was likely a neutron. The block diagram is shown in Fig 6.13.

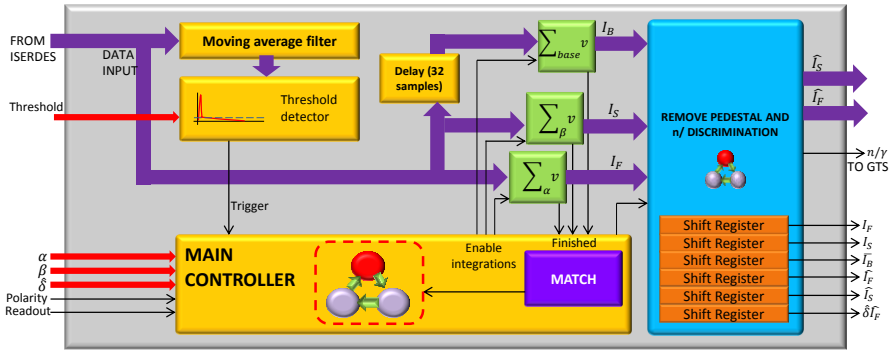


Figure 6.15: Processing unit block diagram

Taking a closer look to the block diagram, the system architecture consists of a main controller and a set of calculating slave blocks which may have as well a local controller inside

to be used in case of more complex operations were required. According to the Fig. 6.15, each block carries out the subsequent task:

- Main controller: Enables / disables the rest of the blocks according to a set of parameters and to an execution sequence.
- Moving average filter: Precedes the threshold detector. By using this filter, the threshold detection avoids spurious noise sources and provides robustness. For this case, an 8-th order moving average is used.
- Threshold detector: Delivers a pulse to the main controller if the signal crosses a certain level set by the user as a parameter.
- Integrators: Using a recursive addition method, the integrators provide the slow, fast and baseline integrals I_S, I_F and I_B, the latter calculated over the 32 samples preceding the trigger. After an integral is finished, it sends a flag to the main controller.
- Match unit: A sub-block inside the main controller, takes the flags after integrations are calculated and waits until the last integration is done. Afterwards, it sends a flag to the pedestal correction unit to start the following calculation process.
- Pedestal correction unit and neutron/gamma discrimination: Gathered in the same block to take advantage of the reusability of the hardware resources, this multifunctional block calculates both the part of area which shall be subtracted from the pulse and provides the trigger to the GTS after comparing both integrals with the parameter $\hat{\delta}$. Besides, it incorporates a set of 6 PISO (Parallel-In Serial-Out) registers in case the results of the integration are required to be read with a minimal amount of resources from a logic analyzer. The integral terms I_S, I_F and I_B refer to the original integrated variables, while $\widehat{I_S}$ and $\widehat{I_F}$ are calculated after subtracting the average value from the input. Expressions 67) and 68) show the procedure to subtract the baseline, while 69) provides the expression to deliver a trigger request in case the PSA algorithm recognizes an event as a neutron.

$$\widehat{I_S} = I_s - \beta\overline{I_B} \quad 66)$$

$$\widehat{I_F} = I_f - \alpha\overline{I_B} \quad 67)$$

$$\begin{cases} n/\gamma = 1 \; if \; \widehat{I_s} > \hat{\delta}\widehat{I_F} \\ n/\gamma = 0 \; if \; \widehat{I_s} < \hat{\delta}\widehat{I_F} \end{cases} \quad 68)$$

Taking a closer look to the operations performed inside the pedestal correction unit, an inner FSM controls the order of the operations and the data-path according to the diagram shown in Fig. 6.16.

The main feature it can be observed in the block diagram is the usage of only one multiplier (22-bit for the input A while 8-bit for the input B), and a set of multiplexers used to control the data-path. This approach was taken because the data flow dependency, in which the term $\widehat{I_F}$ is needed back into the input to compute again $\hat{\delta}\widehat{I_F}$, given that the multiplier was not longer used when performing $\hat{\delta}\widehat{I_F}$. If a 3-staged pipelined multiplier is used, taking into account that the data throughput is of one clock-cycle, the total amount of time spent is 12 clock cycles to obtain the discrimination.

The processing unit is carried out in a distributed manner by implementing a FSM (Finite-State machine) in the main controller, and also inside some of sub-blocks. The interaction mechanism between the master FSM and the slave blocks placed one step below make use of start/finish pulses. Not only this strategy is aimed to enhance the system modularity design, but also to provide flexibility in case the system requires a more complex approach.

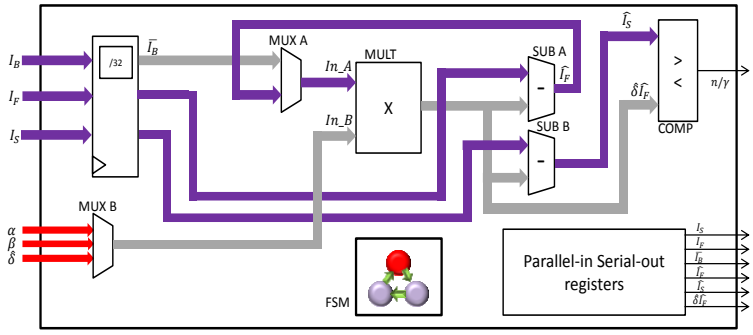


Figure 6.16: Pedestal correction unit internal architecture

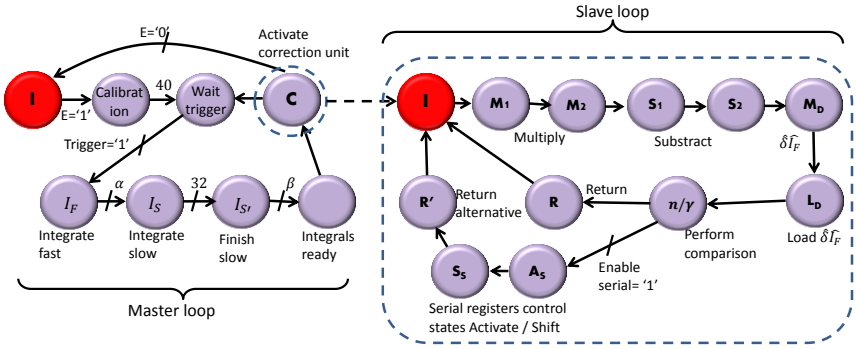


Figure 6.17: Processing unit control sequence

The structure depicted in Fig. 6.17 provides an example of the aforementioned FSM design strategy. The master loop makes reference to the main controller while the particular slave depicted does it for the pedestal correction unit, placed in the state 'C' of the main controller.

Initially, the system remains disabled until the enable signal toggles high. Before receiving any trigger, a pre-calibration is made in order to set the threshold which will shoot the trigger. Once this process has finished after 40 cycles, the system turns into its waiting state until an event comes and sets the trigger signal to 1. Triggering the system enables the integrators within their corresponding time according to α and β parameters, as well as the baseline counter, which counts the 32 samples previous to the trigger, stored into the delay line. Even though each integral provides its finish flag back to the main controller, normally it is the slow integral the last which finishes after β cycles, for which the pedestal correction is ready to start. Inside the 'C' state, the slave FSM gets enabled, with a set of states coping with the operations order and data-path guidance. The states are coordinated in order to provide maximum efficiency, taking profit especially of the multiplier pipelined architecture. Most of the cycles are activated for only one clock cycle, whose synchronism from the FSM is planned to move the data through the units until reaching the state for the n/γ discrimination. Optionally, if the enable serial registers is set to '1', two additional sates, A_s and S_s are added to control the register operations. Either with the serial register option enabled or not, the system always goes back to the initial state through a return state (R,R'), which delivers a pulse after the operation. In case of disabled registers, the finished flag is toggled

synchronously with the n/γ trigger signal, otherwise, the finished flag is done after the completion of the serial transmission.

6.2.3. PSA debugging and parameter calibration

The PSA firmware calibration has been carried out using the testbench platform whose block diagram is shown in Fig. 5.3. It features the PSA block link to the rest of firmware (ISERDES, SPI, etc.). The waveforms used for the discrimination have been acquired using a setup with BC501A-filled detector coupled to a XP4512 PMT, and digitized with of the '*Strück*' SIS3350 12-bit digitizer at 500 MHz. After performing data processing and acquiring a significant number of signals, a set of averaged and normalized version of gamma/neutron signals have been obtained. The waveforms are depicted in Fig. 6.18.

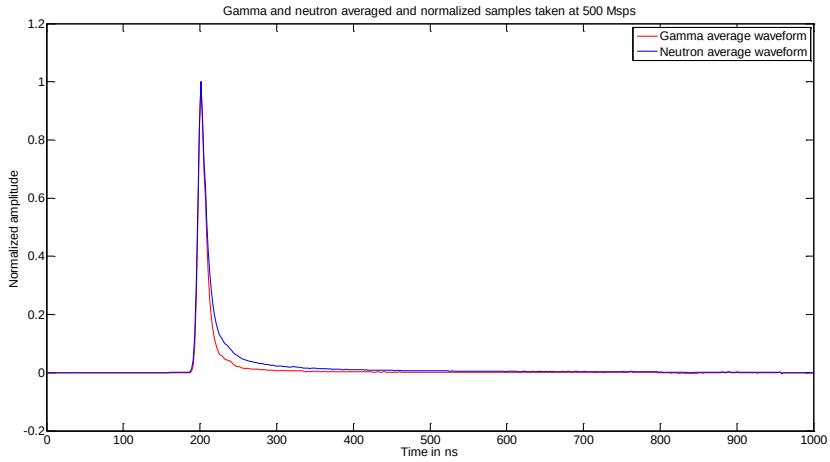


Figure 6.18: Average neutron and gamma-ray waveforms

A software tool has been developed to drive the samples from the gamma/neutron waveforms through the arbitrary signal generator Agilent 33522A, being those the test signals to debug the PSA algorithm. Among other functionalities of this software we can point out the file readout, downsampling to 250 MHz, and to provide an amplitude modulation in order to evaluate the discrimination at different amplitudes. The functionality of this program is integrated with the rest of the software, in which an extra resource is included to control the GPIB port. After the gamma/neutron waveform synthesis at the generator, the waveforms are passed by the front-end board, FADC Mezzanine and delivered back to the Virtex 6.

The readout of the integral values were performed using Chip Scope Pro, attached to the outputs of the PISO (Parallel-Input Serial-Output) registers from which the values of $I_s, I_f, \overline{I_b}, \widehat{I_s}, \widehat{I_f}$, and $\hat{\delta}\widehat{I_F}$ were retrieved and calculated. Although initially the value of $\hat{\delta}$ is set arbitrarily, observing the values of $\widehat{I_s}, \widehat{I_f}$ allows to adjust the value of $\hat{\delta}$. The tests used to calibrate $\hat{\delta}$ consisted of driving several events of both gamma/neutron-associated waveforms at different amplitudes. Fig. 6.19 offers an example of acquisition performed with emulated waveforms. If a zoom-in is performed for each event, the integral values can be extracted using data processing techniques, taking into account the start pattern "10" and end pattern "01", used to recognize where data start and finishes.

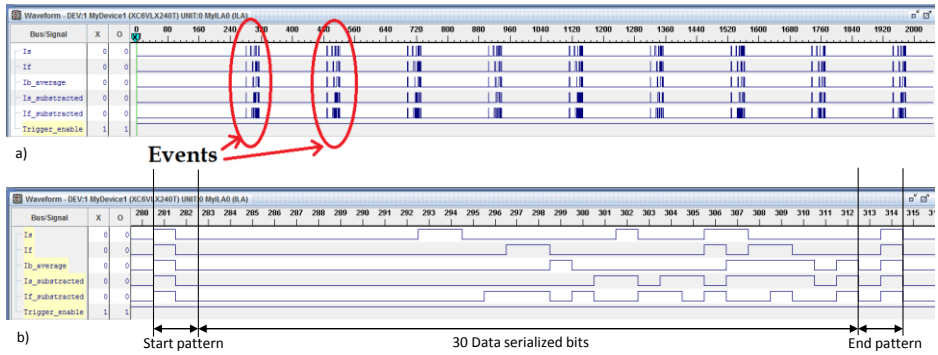


Figure 6.19: Chip Scope Pro screenshot where the integral values can be obtained. a) Example for one acquisition. b) Event zoomed, showing all the values. Results obtained with α and β set to 5 and 100 respectively

In total, a set of 20-25 waveforms were used at different amplitudes, knowing beforehand the waveform type. Fig. 6.20 shows an example of how the discrimination parameters may be extracted. Hence, The x-axis represents the signal amplitude while the y-axis shows the ratio $\widehat{I}_s/\widehat{I}_f$.

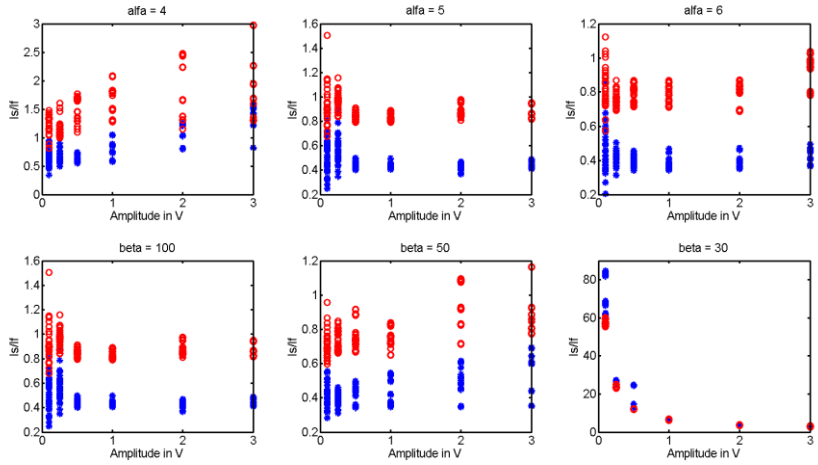


Figure 6.20: $\widehat{I}_s/\widehat{I}_f$ versus signal amplitude. Up) sweep across several α values setting β = 100. Down) sweep across several β values setting α = 5. Events produced by gamma-rays are plotted as stars while neutrons do with circles

Based on Fig. 6.20, the $\hat{\delta}$ value can be estimated for different settings of α and β. Concretely for α=5 and β=100, leading to the design of the parameter $\hat{\delta}$. For different values of α, the figure shows that the fast integral should not be below α=5, where the algorithm loses its discrimination properties. On the other hand, values of α higher than 7 were not reported since the fast integral is used merely to normalize the fast integral value. Looking at the β sweep values in Fig 6.20, it can be seen that the discrimination parameter becomes dependent on the signal amplitude, fact which is harmful in a real experiment. Considering real signals

with different amplitudes, the combination of parameters α=5 and β=100, provided the best performance.

The limitations of our FPGA hardware, together with the necessity to implement 16 channels of discriminator forces us to use only multiplication of the $\hat{\delta}$ term times $\hat{I}_f$. Nevertheless the discrimination itself can be understood more straightforward using the inverse relation $\hat{I}_f/\hat{I}_s$ instead, so that $\hat{\delta}$ is directly proportional to inverse ratio $\hat{I}_f/\hat{I}_s$. Although the discrimination is fuzzier at lower amplitudes it can be seen that at higher amplitudes, $\hat{I}_f/\hat{I}_s \approx$ [1 - 1.2] for neutrons while it turns up to [2 – 2.3] when dealing with events associated to gamma-rays. Thus, depending on the permissiveness of the discrimination to neutrons, an optimistic $\hat{\delta}_o$ (allows all neutrons even some gamma-rays), pessimistic $\hat{\delta}_p$ (allows only neutrons even though some neutrons could be rejected) or standard discrimination threshold $\hat{\delta}_s$ (an hybrid solution in between the pessimistic and optimistic) can be set. Since the ratio values are decimal and $\hat{\delta}$ deals with integer numbers, the term $\hat{I}_s$ can be easily scaled by a power of two so that $\hat{\delta}$ turns into an integer after a rounding process. If $\hat{I}_s$ is scaled by 256, the $\hat{\delta}$ can be calculated as shown in Table 6.2.

Table 6.2: Values of $\hat{\delta}$ obtained for α = 5 and β = 100

Condition	Observed threshold	Discrimination condition	Scaled discrimination condition	$\hat{\delta}$
Pessimistic	1.3	$0.769\hat{I}_f < \hat{I}_s$	$197\hat{I}_f < 256\hat{I}_s$	197
Standard	1.5	$0.666\hat{I}_f < \hat{I}_s$	$170\hat{I}_f < 256\hat{I}_s$	170
Optimistic	1.8	$0.555\hat{I}_f < \hat{I}_s$	$142\hat{I}_f < 256\hat{I}_s$	142

Fig. 6.21 shows an example of neutron / gamma discrimination using synthetic waveforms with 2V peak amplitude and a periodic frequency of 769.23 kHz. The gamma/neutron discrimination signal, which delivers a trigger request to the GTS has been marked in the picture, confirming the algorithm performance.

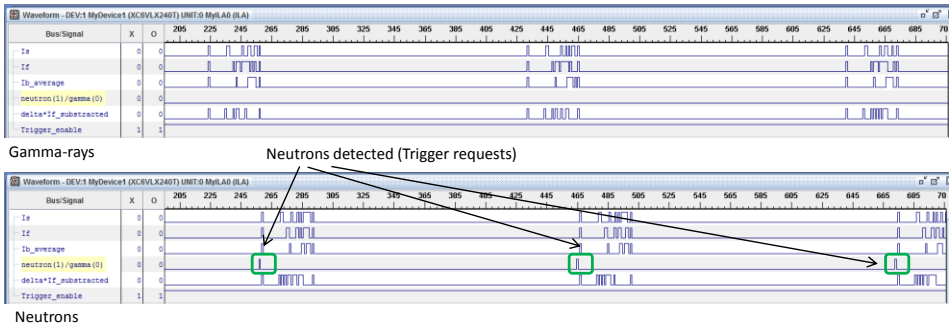


Figure 6.21: Chip Scope Pro screenshots for gamma rays (up) and neutrons (down)

6.2.4. GTS integration into the ML605

As it was previously mentioned in sub-section 3.3.4, the GTS is a system in charge to cope with the overall system synchronization, clock delivery and the event validation / rejection. Even though in the global electronics layout, the GTS leaf is implemented in the Virtex-5 of

NUMEXO2 using dedicated links between the Virtex-6 and Virtex-5 to drive the trigger request signals, a first implementation into a single Virtex-6 device was carried out in order to understand the behavior of this complex system and to test the interaction of the NGD block with the newly-developed GTS for NEDA. Among some of the tasks, it is needed to understand the concepts related to the GTS cycle such as the timestamp, local trigger, validation-rejection and the different latencies involved in the process.

Concretely, the first step for the integration of the GTS was carried out using the FADC testbench platform, integrating the GTS in two major phases. The first phase consisted only the reused firmware used for the Mezzanine test and the GTS, including the latter all the elements. For testing the implementation at this stage, a specific configuration for the trigger processor was due, providing a trigger validation for any incoming trigger request. Besides, for the first stage, a pulse generator was used to deliver the trigger requests to the GTS, observing mainly the behavior of the GTS signals with Chip Scope Pro. The block diagram for the first phase of the GTS integration into the Virtex-6 is depicted in Fig. 6.22. The purpose of this first stage is to understand the behavior of the GTS in terms of signals and timing.

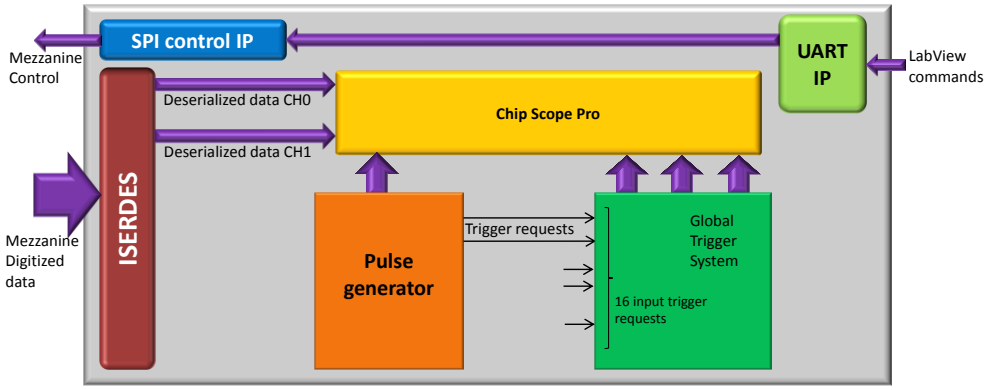


Figure 6.22: GTS Integration phase 1

In order to show how GTS works, the trigger validation/rejection cycle is sketched in Fig. 6.23. After a trigger request occurs, the corresponding signal is immediately sent to the GTS leaf. Besides, the GTS contains a global counter which produces a field called the timestamp, used to tag the moment at which the trigger request was received within a resolution of 10 ns. Then, the GTS leaf sends the timestamp field and the notification of a trigger request (now depicted as Local Trigger [0]) to the trigger processor, which takes this information together with the triggers from other detectors in order to provide either a validation or a rejection. The time lapsed between the trigger request and the notification to the trigger processor is called local latency whose main responsible is the GTS leaf, which is usually 1 clock cycle. After the trigger processor has analyzed the triggers, either a validation or a rejection signal is received together with a field (named as val_rej_tag[7:0]), which contains the timestamp of the event which was previously sent to the trigger processor, so that both match. Notice the serialization of the 48-bit timestamp value into sets of 8 bits. In addition, val_rej_tag [7:0] field includes, after the 6th received byte, a set of 3 bytes which refer to the event counter, which is increasing progressively.

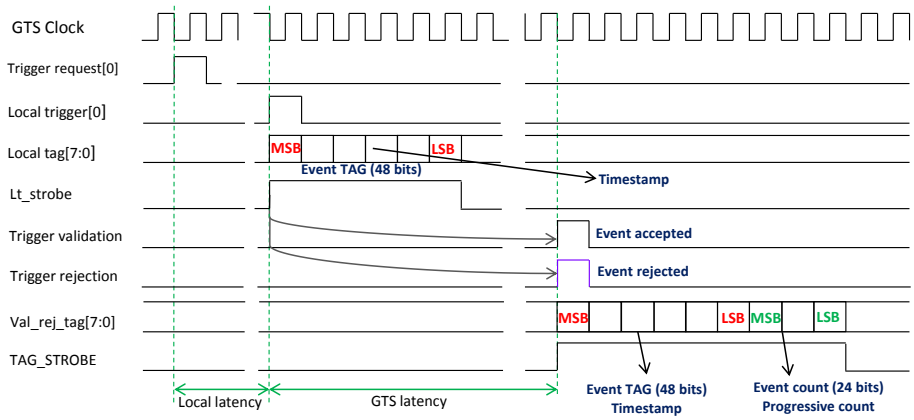


Figure 6.23: GTS chronogram

The experiments carried out helped to understand the behavior of the GTS itself, using different request conditions at the level of the pulse generator. These tests involved the delivery of a single trigger request, several simultaneous requests, and requests separated by a certain amount of time. Figs. 6.24 and 6.25 show a couple of examples for two simultaneous requests. The trigger request field is in reality the corresponding bit pattern encoded in hexadecimal, meaning that the 0x0007 refers to three requests provided from CH0, CH1 and CH2. Nevertheless, in the reality the trigger request from the CH1 was not connected to the GTS, being the real value of the trigger request 0x0005, as the local_trigger bit pattern shows.

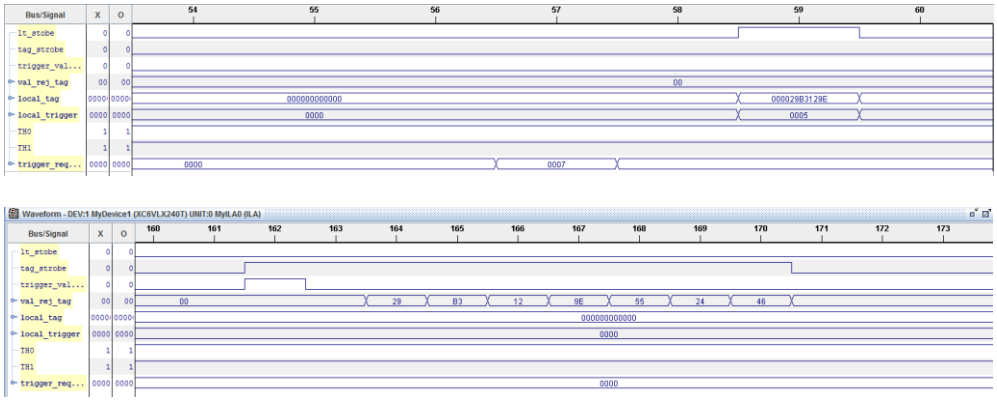


Figure 6.24: Example of trigger request and validation for two simultaneous requests. Up) Request chronogram. Down) validation chronogram.

The concordance between the timestamp values set at the request and at the validation which is 0x0029B3129E can be clearly noticed. The event counter set at the 3 last bytes is 0x552446. Taking the following consecutive trigger request example, shown in Fig. 6.24, also with two simultaneous requests, we observe the following:

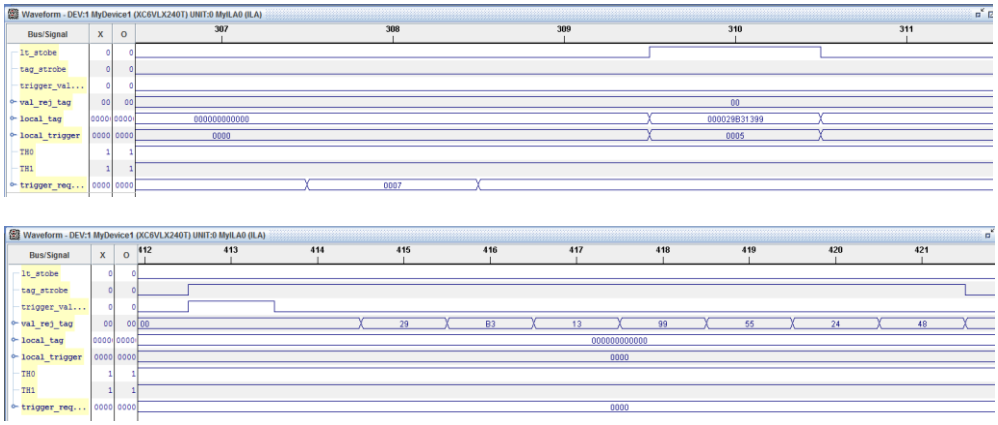
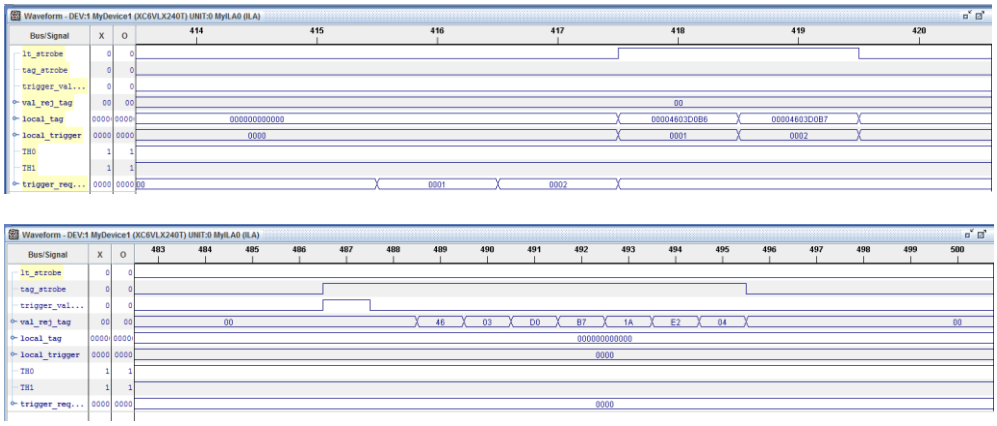


Figure 6.25: Second example of trigger request and validation for two simultaneous requests. Up) Request chronogram. Down) validation chronogram.

the event count has increased by two to 0x552448, meaning that the behavior of the GTS in terms of the event counting under the condition that all requests are accepted is correct[18]. Notice that the latency between the requests and validations is 103 cycles for both of them. The experiment was repeated for more trigger requests verifying the same latency in all of the examples taken.

The second experiment delivers three trigger requests consecutively, taking a clock cycle separation between the second and third request, as shown in Fig. 6.26.



[18] *This assumption is correct as long as we validate all trigger requests, fact for which a trigger processor is not required. In reality, in a real experiment, several local trigger requests with the same timestamp might be regarded as the same physical event due to the trigger processor algorithm. In consequence, in a real environment only one validation would be given even if several trigger requests are delivered.*

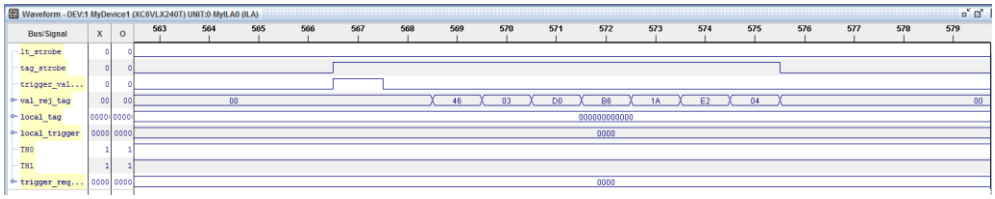


Figure 6.26: Example of trigger request and both validations for two consecutive requests. up) request chronogram. middle) first validation chronogram. down) second validation chronogram

Unlike the first experiment, where only one trigger validation for both trigger requests is used (taking into account that both of them were accepted), when the requests do not occur in the same clock cycle, both validations are delivered separately with its corresponding timestamp (in case we are working, of course with an all-validation mode). If we look at the event counting field, both of them contain the same value. However if we take more examples of consecutive events, the count is increased by two on the following request, meaning that the event count proceeded correctly. Another issue is the validations order. On the example shown above the timestamp from the second event is sent first, but actually this fact mostly depends on how the internal GTS buffers organize the data, given that some events may take longer processing than others due to processing complexity in the trigger processor. This fact might lead to receive before validations with timestamps of events which were triggered later.

After the GTS behavior was well understood, the next step consisted of integrating the pulse-shape analysis block into the firmware together with the GTS, so that two separated blocks which worked properly were combined. The trigger requests are now provided as a result of the processing performed by the PSA block. Fig. 6.27 shows the block diagram of the current setup.

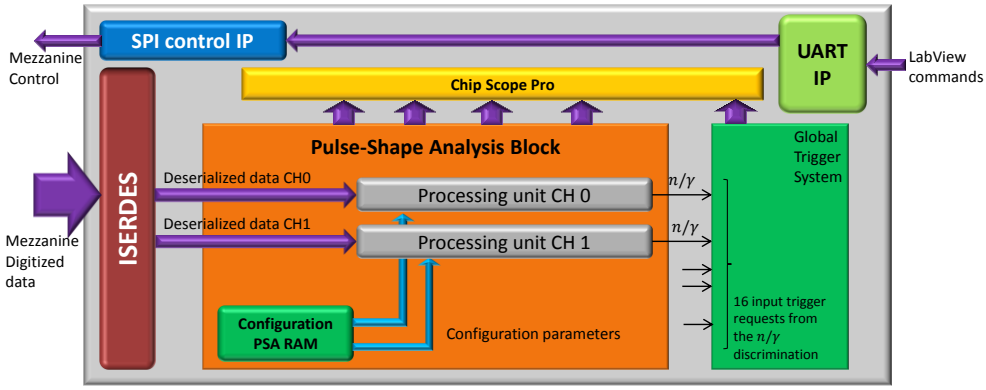


Figure 6.27: GTS integration with the PSA block

The test when including both the PSA algorithm and the GTS in the same device was carried out, commissioning the functionality of the neutron trigger implementation. In this way, the tests confirmed that the behavior is the same when merging both blocks together as the performance obtained when evaluating each block separately.

Chapter summary

After a set of chapters involving the design of the FADC Mezzanine and the measurements carried out in order to verify its functionality, this chapter has focused on firmware integration into the NUMEXO2 digitizer. Concretely, the integration required the development of PSA algorithms used for the neutron/gamma discrimination used in the neutron detector NEDA.

The pulse-shape analysis integration involved the study of an optimal solution, in terms of NGD and hardware resources, which can cope with the NEDA performance demands. As a result of this analysis, the charge comparison method has been implemented, as well as carrying out the algorithm calibration as well as the description of the tests necessary to prove that the algorithm provides the required functionality.

7. Results

In this chapter, the results obtained with the final prototype of the FADC Mezzanine are presented, leading to the conclusions that the design is valid for both EXOGAM2 and NEDA. The results obtained with former Mezzanine versions are thoroughly shown in section 4.10, focusing on how older versions were improved and reviewed leading to the current design.

7.1. FADC Mezzanine final results

Most of the tests carried out are focused on the noise performance, which plays a major role on the energy resolution when performing tests with HP-Ge detectors. The noise performance has been analyzed throughout the whole FADC range, verifying that the specifications are accomplished and not only for the encoding corresponding to the setting of the baseline, but in all the FADC range where the peak maxima may fall in. The reason to perform measurements across the whole range was that the tests performed in former versions revealed a non-uniform noise response along the dynamic range. A non-uniform ADC noise response has a consequence that pulses whose amplitude fall in the most conflictive zones areas, to produce wider peaks in the energy spectrum at certain regions.

The measurements presented hereby show a comparison between the former and the final prototype at the sampling frequencies and bandwidths used for the experiments.

7.1.1. Noise performance versus sampling frequency

Firstly, the noise performance of the latest FADC Mezzanine version (v5) was compared to the former v4, checking out that layout changes were effective. Fig. 7.1 and 7.2 show the experiments taken at 100 MHz and 200 MHz sampling frequency respectively. Measurements were taken under the same conditions as the ones taken for the former prototype Mezzanine V4. Hence, each measurement contains the division of the FADC rage in 200 zones. In each zone, 8 sets of 32 ksamples were acquired by changing the level of the baseline in each zone.

The results in Fig. 7.1 and Fig. 7.2 show a clear global improvement in the response for the four channels of the Mezzanine between the two presented versions. Although the results in version 4 at 100 MHz were fair enough to put the FADC Mezzanine into a real experiment, the resolution worsened at 200 MHz, showing a set of peaks spaced equidistantly. The layout changes performed in version 5 shows an efficient improvement, especially at 200 MHz, where the peaks appearing on the version 4 have been drastically reduced. Additionally, a slight improvement can be seen when sampling at 100 MHz.

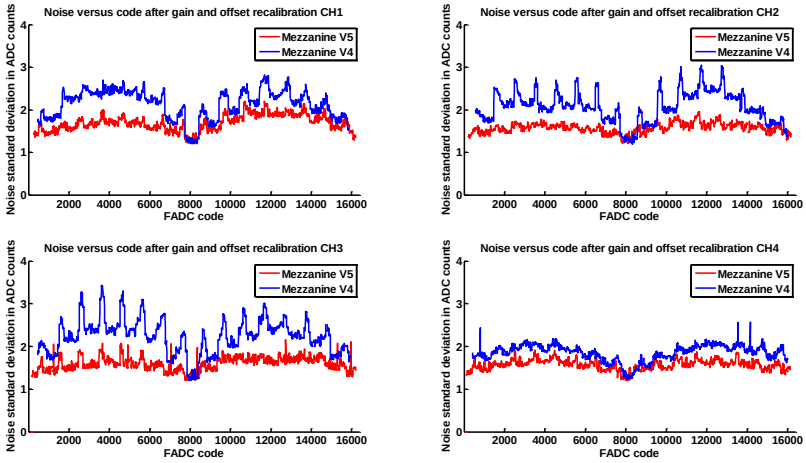


Figure 7.1: Noise performance comparison between Mezzanine V4 (former) and Mezzanine V5 (current and final) or the four channels at 200 MHz sampling frequency.

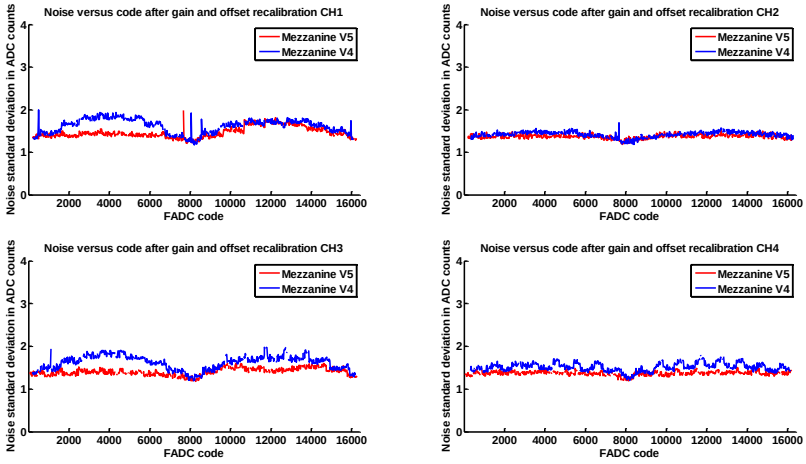


Figure 7.2: Noise performance comparison between Mezzanine V4 (former) and Mezzanine V5 (current and final) or the four channels at 100 MHz sampling frequency.

The worst case at 100 MHz happens for the channel nº1, around the code 12000, observing a local maximum approximately of σ=1.9, which translates into an ENOB = 11.28. as it was for the version 4, the best resolution values are obtained at the levels where the baseline would be set when performing real experiments, which are the extreme (both top and bottom) and middle values, obtaining resolutions between σ=1.2 and σ=1.4 (ENOB between 11.7 and 11.9).

7.1.2. Noise performance for different bandwidths

A second set of measurements compares how the bandwidth affects the noise performance at different sampling frequencies. Recalling the specifications from chapter 3, EXOGAM2 required a minimum bandwidth of 30 MHz although the measurements have been taken with 50 MHz. On the other hand NEDA fast signals required a minimum of 100 MHz in bandwidth in order to perform accurately timing measurements even though the sampling frequency of 200 is of MHz.

Fig. 4.45 from chapter 4 revealed a noise performance dependency on the ADC code which could not be related to any normal phenomena related to the noise itself, appearing higher peaks at lower bandwidths. This behavior can be explained by other phenomena which becomes into noise, but are uncorrelated with standard noise sources. For this reason, the same measurement was carried out for different bandwidths and different sampling frequencies. The results are shown in Figs. 7.3, 7.4 and 7.5.

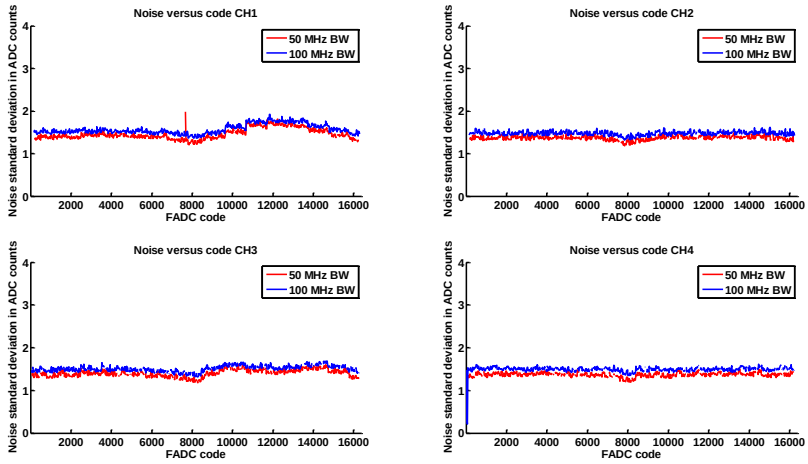


Figure 7.3: Noise performance comparison for the Mezzanine four channels at 50 MHz and 100 MHz bandwidth, sampling at 100 MHz

As it can be seen, with version 5, noise increases with the bandwidth. The results for 100 MHz (Fig. 7.3) show a slight uniform noise increase when the bandwidth is 100 MHz. At 200 MHz sampling frequency (Fig. 7.4), the difference seems slightly bigger between the sigma taken at different bandwidths. Also, the presence of non-uniform noise response reveals that crosstalk influence from the digital lines and the antialiasing filter that, although reduced over the version 4, is still present at 200 MHz (Fig. 7.4).

Besides, a measurement at 250 MHz was performed foreseeing the possibility to upgrade NEDA electronics to 250 MHz for further improvement of timing measurements. Nevertheless, at 250 MHz, Fig. 7.5 illustrates that the zones more exposed to the crosstalk effects worsen dramatically, showing the Mezzanine vulnerability to the crosstalk at higher sampling

frequencies.

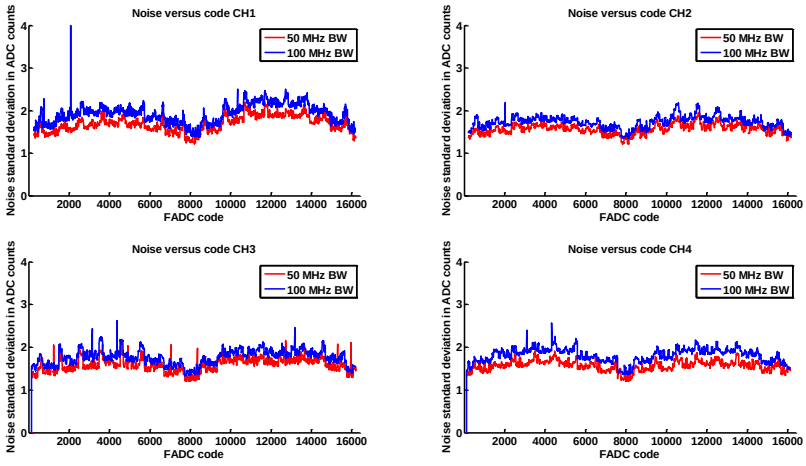


Figure 7.4: Noise performance comparison for the Mezzanine four channels at 50 MHz and 100 MHz bandwidth, sampling at 200 MHz

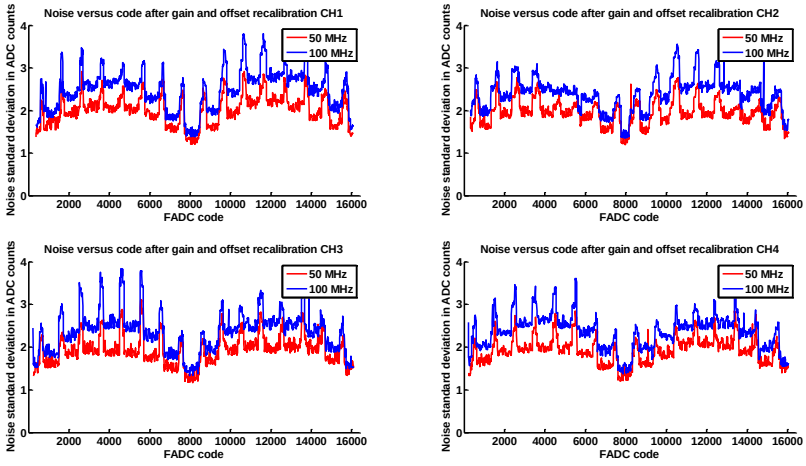


Figure 7.5: Noise performance comparison for the Mezzanine four channels at 50 MHz and 100 MHz bandwidth, sampling at 250 MHz

The large differences between sigma at 50 MHz and 100 MHz bandwidth at 250 MHz sampling frequency shows the influence of other factors external to the noise sources in case of sampling at 250 MHz. This effect can be observed due to the unequal $\Delta\sigma$ distribution across the ADC code where differences between $\Delta\sigma$ at different bandwidths oscillate between 0.1 and 1. On the other hand, the effect at lower sampling frequencies is more flattened, meaning that the increase of noise when increasing from 50 MHz to 100 MHz can be attributed to noise sources.

7.1.3. Frequency-domain noise measurements

The final aim of our FADC Mezzanine involves dealing with fast pulses with defined frequency ranges for the rise time and fall time. Therefore, it is important to check the noise components at the frequencies of interest. Hence, the measurements have been taken using the final Mezzanine v5 with an analog BW = 50 MHz, 200 MHz and absence of input analog signal, with the HDMI cable disconnected from the rest of electronics. The FFTs are applied over a set of 32k samples. Fig. 7.6 illustrates that in all channels the noise behaves in a similar way, without any impact of particular frequencies in the spectrum. Some interesting facts are the noise floor, present in all channels close to -110 dB, and the slightly higher noise power contribution at lower frequencies due to the *1/f* noise contribution, which can be noticed at the first bins of the frequency spectrum.

The performance over the frequency domain with an input signal has been evaluated by measuring the SINAD and SFDR, which gather the effects of harmonic distortion into the noise. The measurements are applied to CH3 and CH4 using the Mezzanine V5 and the Agilent 33522A waveform generator, extending from 100 kHz to 30 MHz. In addition, aiming to compare the behavior at different amplitudes and gains, both SINAD and SFDR are evaluated at G=1 and G=0.25 by applying an input sinusoidal whose amplitude produces at the FADC the same range of output codes. From Fig. 7.7, it can be concluded that all parameters get worse as the frequency increases. It can be noticed that the SINAD is more affected for waveforms with higher amplitude since the generator produces higher distortion for sinusoidal waveforms generated with higher amplitudes. The same fact can be appreciated when looking at the SFDR. Then for amplitudes covering the same FADC dynamic range such as $4V_{pp}$ input for G=0.25, and $1V_{pp}$ input with unitary gain, the distortion is always higher for waveforms generated at higher amplitudes.

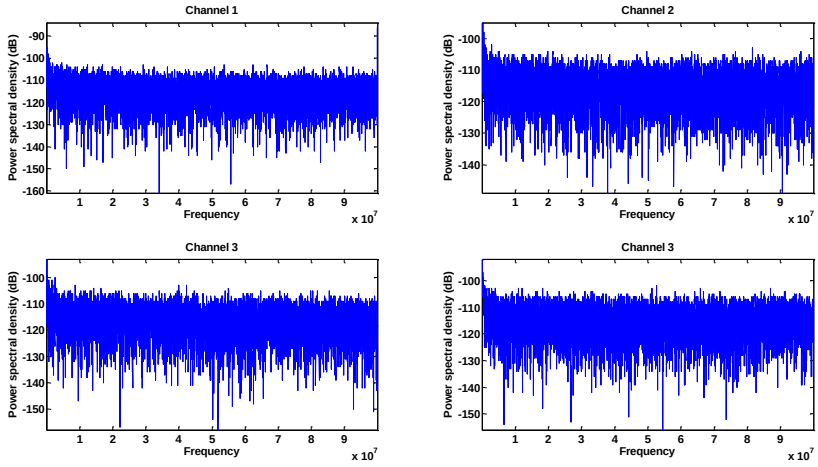


Figure 7.6: FFT measurements applied to the FADC Mezzanine in absence of input analog signal at 200 MHz sampling frequency and 50 MHz bandwidth.

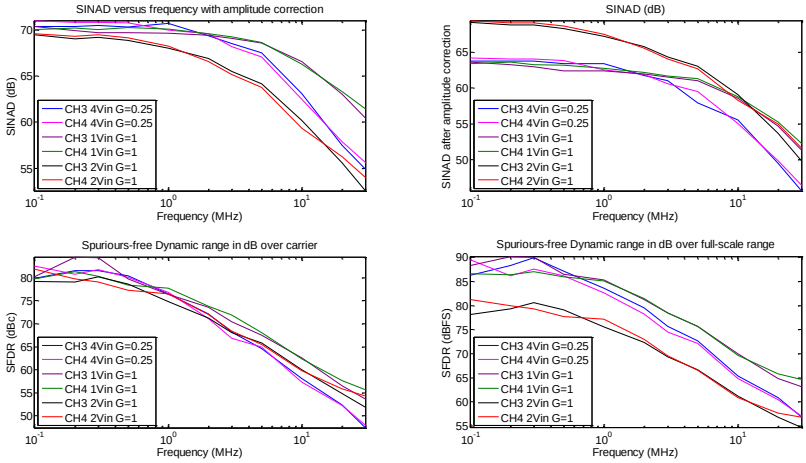


Figure 7.7: SINAD and SFDR measurements obtained for several Mezzanine configurations in terms of gain and input amplitude. SFDR measurements have been referred both to the full-scale ADC range and to the input signal amplitude (carrier)

7.1.4. DNL and INL results

DNL and INL measurements have been obtained by applying the sinusoidal histogram. In order to carry out the measurement properly, the sinusoidal input signal amplitude has been calibrated to fit the whole FADC dynamic range. Secondly, a coherent input frequency, selected to 1.01013183975 MHz was chosen to perform the measurements. A trade-off between measurement confidence and time has set the record window to 2.5 million of samples, with a 95% degree of confidence and a DNL expected error of β =0.2 LSB. Results for DNL and INL are depicted in Fig. 7.8 as an example.

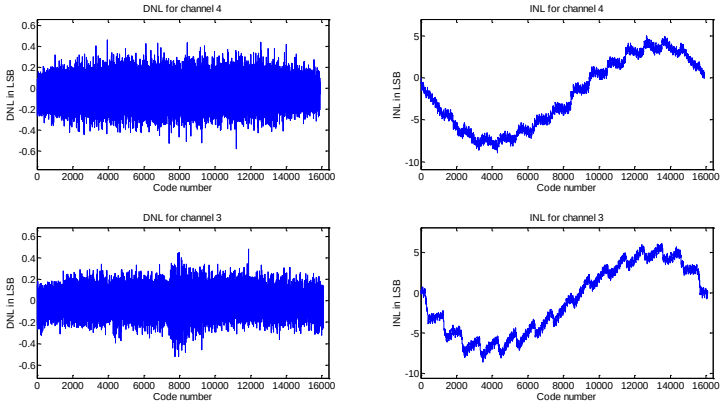


Figure 7.8: DNL and INL results obtained for CH3 and CH4 by applying the sinusoidal histogram method

According to Fig. 7.8, the DNL and INL fit within the specifications given by the ADS62P49 datasheet. Similar results have been obtained also for channels 1 and 2. Since the noise studies have led to satisfactory results, the contributions both from the INL and DNL have been considered negligible for the experiments.

7.1.5. Energy resolution measurements at GANIL

Fig. 7.9 shows the energy spectra and a zoom in the main energy peaks at 1.17 MeV and 1.33 MeV of the ^{60}Co, the latter used to obtain the resolution after applying a Gaussian fitting function. The measurements were carried out using one of the inner contacts of the HP-Ge detector @ 6 MeV range, concretely the INNER_B channel. Unlike the tests envisaged for NEDA, which make use of our testbench platform, energy resolution measurements were acquired using the current NUMEXO2 setup and DAQ at GANIL.

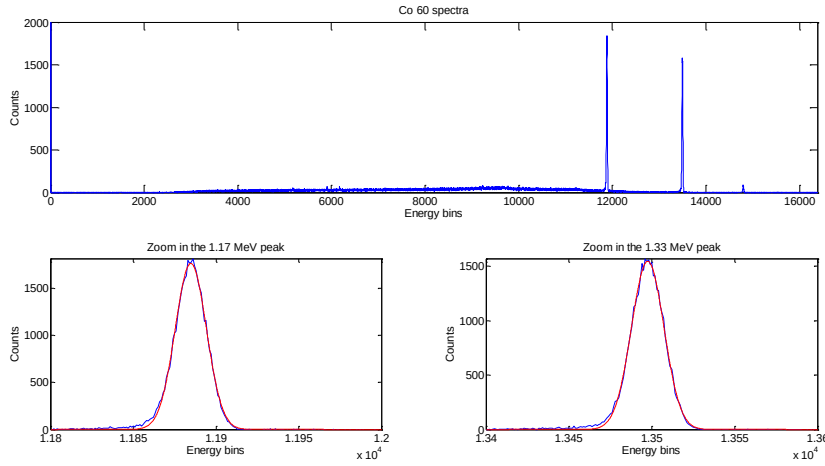


Figure 7.9: Up) Energy spectra using a ^{60}Co source. Down-left) Zoom in performed at 1.17 MeV and. Down-right) Zoom-in performed at 1.33 MeV.

Obtaining fine energy resolution measurements not only depend on the noise performance, but also on the overall gain. The whole electronic chain contains two main points at which the gain can be changed, the FADC Mezzanine and the trapezoidal filter. Optimal results have been obtained with a unitary gain for the FADC Mezzanine combined with the MWD parameters K = 18.6 µs and M = 2 µs. After a large amount of statistics are acquired (> 10.000 events), using the energy peaks from ^{60}Co, the energy resolution can be extracted by obtaining the amount of energy per LSB.

$$Energy/_{LSB} = \frac{1.33\ MeV - 1.17 MeV}{Bin(1.33\ MeV) - Bin(1.17\ MeV)} = 0.099\ keV/LSB \qquad 69)$$

By fitting each peak with a Gaussian function, the energy resolution can be extracted from its σ and multiplying by 2.35 to obtain the FWHM. With the measured σ = 9.87 LSB, the energy resolution @ 1.33 MeV is:

$$FWHM@1.33MeV = 2.35\sigma * Energy/_{LSB} = 2.35 * 9.87 * 0.099 \frac{keV}{LSB} = 2.3\ keV \qquad 70)$$

This number corroborates the demanded specifications in terms of energy resolution for the EXOGAM detector.

Analogously, the energy resolution can be verified for lower-energy gamma-rays using a ^{152}Eu source. The experiment has been carried out using the same setup as in ^{60}Co, but changing only the radioactive source. Similarly as in the ^{60}Co, the approximated counting rate is 100 Hz for the experiment. The spectra obtained with ^{152}Eu and the energy resolutions of the corresponding peaks are illustrated in Fig. 7.10 and Table 7.1.

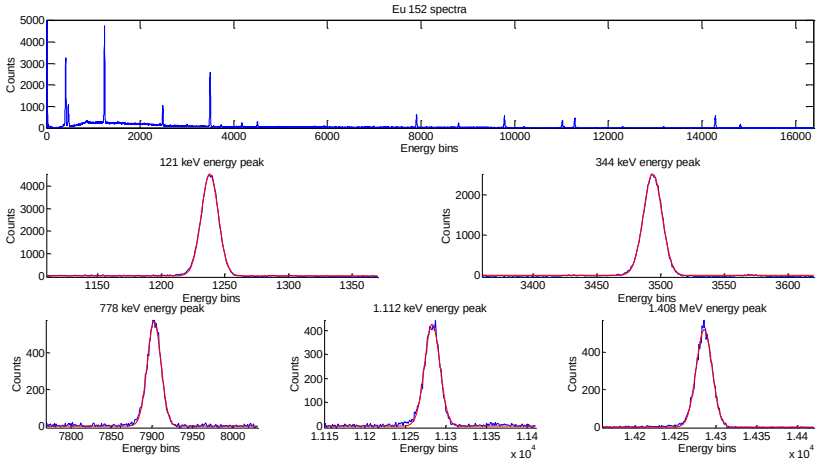


Figure 7.10: ^{152}Eu spectra and its corresponding peaks at 121 keV, 344 keV, 778 keV, 1.112 MeV and 1.408 MeV

Table 7.1: Energy resolution for the ^{152}Eu peaks

Energy	121 keV	344 keV	778 keV	1.112 MeV	1.408 MeV
Energy resolution	1.562 keV	1.702 keV	1.968 keV	2.203 keV	2.302 keV

7.1.6. Timing and NGD measurements at LNL

A commissioning has been carried out at LNL (Laboratori Nazionali di Legnaro), in order to evaluate the timing and NGD capabilities with the FADC Mezzanines and, therefore checking the feasibility of using them for the NEDA detectors. The experiment consisted in using radioactive sources of ^{60}Co and ^{252}Cf to acquire data applying on them the timing and PSA algorithms. As the NEDA firmware integration in NUMEXO2 was still under development at the time of the measurements, the testbench platform presented in chapter 5 was used to acquire data while the algorithms were run off-line in LabView.

Timing measurements were done using two BC501A-based scintillators coupled to the XP4152 PMTs placed 40 cm away from a 3 MBq ^{60}Co source. Both PMT XP4512 outputs were connected to a Fan-in Fan-out NIM analog module to obtain signal replica. One of the outputs was driven to the digital setup consisting of the FADC Mezzanine, ML605 and the single-ended to differential module, while the other was driven throughout NIM coincidence modules and

CFDs, delivering only a trigger signal when a coincidence between any of the neutron detectors was detected. After a trigger condition occurs, the acquisition process in the ML605 starts, buffering data and sending it to the PC. The buffer size is limited by the FPGA memory resources and the timing and PSA algorithmic requirements to 2k-samples per channel, 200 of them pre-triggered and used to calculate the baseline afterwards in the PC. Fig. 7.11 shows the physical setup used for timing measurements while the electronics are depicted in Fig. 7.12.

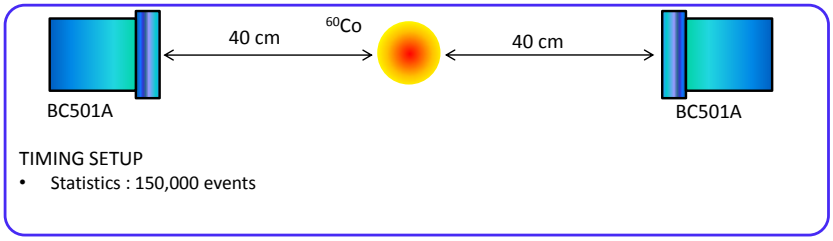


Figure 7.11: Timing setup used at LNL for timing measurements

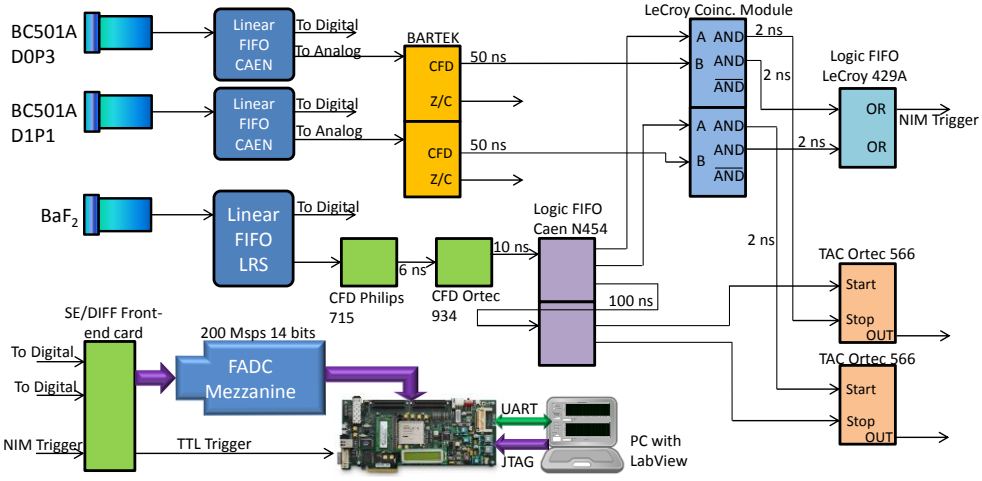


Figure 7.12: Electronics setup (both analog and digital) at LNL

To test the performance of the PSA algorithms, a similar setup was used but replacing the ^{60}Co source with a ^{252}Cf one with 4 MBq activity that emits both neutrons and gamma-rays. A BC501-A-based neutron detector was now placed 1 m away from the source and a BaF_2 detector 50 cm away were used, although the signal from the BaF_2 detector, was not used afterwards for data analysis, but only to produce triggers. The setup is depicted in Fig. 7.13.

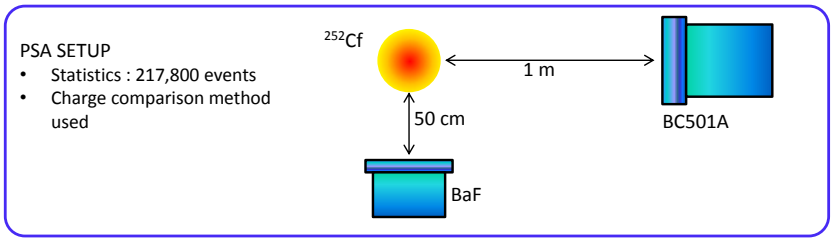


Figure 7.13: Pulse-shape analysis setup used at LNL

Timing results

To evaluate the performance of the Mezzanine in terms of timing resolution, the 2k sample set acquired after a trigger condition occurs is processed in two ways using a cubic interpolation with spline functions: the first one uses the full set of samples and the other uses the result of a digital constant fraction discriminator (CFD) implemented in LabView. The reason for applying this kind of processing can be found in reference [62] where several interpolation algorithms were compared using a Strück SIS3350 digitizer at 500 MHz downsampled to 200 MHz to prove the suitability of timing measurements at this lower sampling frequency.

A threshold proportional to the signal amplitude is applied to the full set of samples while the zero crossover point is estimated in the DCFD output. The time difference between the two acquired channels processed in both is histogrammed. As a result, a FWHM of 1121 ps was obtained with the DCFD, while 1136 ps was the estimation using the full set of samples. Both results are compliant with the performance expected in the detector.

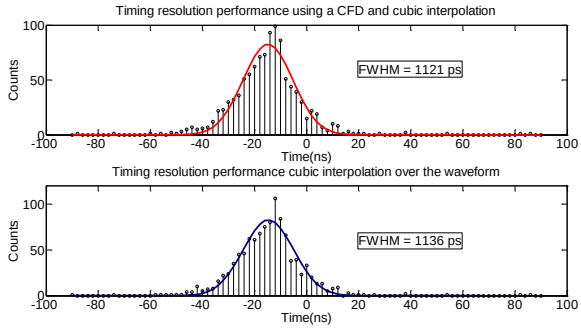


Figure 7.14: Timing resolution histograms obtained for: a) cubic spline applied over the digital constant fraction discrimination, and b) cubic spline applied over the original signal

Fig. 7.14 shows the histograms for both methods with a Gaussian fit. Comparing these results with those of reference [106], using the Strück SIS3350 for 200 Msps, the timing resolution obtained is 1.04 ns FWHM using a threshold of 100 keVee. This result is in good agreement with our results using the FADC Mezzanine.

Pulse-Shape Analysis using the Charge-Comparison method

A histogram based on the charge-comparison method has been applied to demonstrate the capability to perform PSA with the FADC Mezzanine at 200 MHz. An acquisition of 217.600 events from a 4 MBq ^{252}Cf source was performed to draw the histograms. Using the NIM modules an energy-equivalent threshold was set to capture data for pulses higher than 50 keVee. The values of α and β have been found out after an optimization process, leading finally to integration time gates of α = 25 ns and β = 500 ns. By recalling the expression 6) from chapter 3, the figure of merit M is used to quantify the discrimination performance. Fig. 7.15 shows the histogram for discrimination, where the x-axis represents the ratio, described as the ratio between the slow and fast integral after subtracting the baseline values over 32 samples.

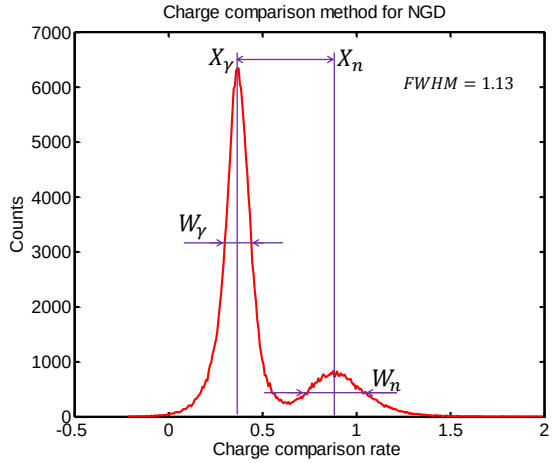


Figure 7.15: Neutron-gamma discrimination performance using the charge comparison algorithm for α = 5 and β = 100. The horizontal axis represents the ratio

A M=1.13 was obtained taking into account that low-energy neutrons are involved in the process. If a threshold condition is applied at 62.5 keVee, a reasonable threshold for neutron discrimination in NEDA, the figure of merit M improves up to M =1.3. Comparing the results obtained with the aforementioned conditions with the ones provided in Fig. 3.17, in which several algorithms based on charge-comparison (called GDM) and on zero-crossover (IRT), it is easy to conclude that the present algorithm is suitable for our application of a first-level NGD. The results obtained are in good agreement with those obtained with the Strück SIS3350 digitizer, although the final results have not been published yet [Private Communication].

Chapter Summary

In this chapter it has been shown the suitability of the FADC Mezzanine for experiments performed with both NEDA and EXOGAM2 detectors. Hence, the suitability test has been carried out firstly, by ensuring the intrinsic behavior of the FADC Mezzanine fit within the ENOB and sampling frequency specifications before putting them into the experimental environment. Both intrinsic and experimental-focused measurements, have shown satisfactory results, whose conclusion leads to the possibility to use the FADC Mezzanine in a

real experiment. In the next chapter discusses the conclusions extracted and how they can be laid out for a future overview.

8. Conclusions

In this thesis, the work corresponding to the design, verification and integration of a high-speed sampling board, part of the NUMEXO2 digitizer for the detectors EXOGAM and NEDA has been presented. Summarizing the tasks performed within this thesis, they can be classified in three main points: first, the study of both the underlying physics and the detector instrumentation, establishing a conceptual framework to become familiar with the FADC Mezzanine design specifications. Second, the development of both the FADC Mezzanine and other testing tools aiming at verifying the correct FADC functionality. And finally, the third point to emphasize is the study of the experimental environment which allows the integration of the FADC Mezzanine with the upgraded electronics for EXOGAM detector, EXOGAM2, and also for the new-generation neutron detector, NEDA. Before introducing the final conclusions of this work, a few paragraphs will be dedicated to review the process carried out throughout the thesis.

Starting by basic foundations of physics, photon-matter and neutron-matter interaction mechanisms were reviewed, in order to understand the basics of gamma-spectroscopy and its role in nuclear physics. Also, in the same chapter, in a more specific context related to the EXOGAM and NEDA detectors, their detection mechanisms were also introduced, in particular those related to detectors based on semiconductors, organic scintillation and photomultipliers. The last point we focused in the introductory chapter is the importance of the PSA in applications requiring particle-type discrimination, applicable in charged-particle detectors, and, particularly for our case, the use neutron-gamma discrimination in neutron detectors. A brief outline of the detector physics is clearly important from the point of view of what type of signal features each detector and what kind of processing should be applied. A second introductory chapter was focused more in the detector itself and the linkage between the physical foundations and the parameters used for the electronics design, introducing the concepts of energy resolution and neutron-gamma discrimination performance, which are in turn, the parameters which set the most of the constraints to design the FADC Mezzanine, such as ENOB, bandwidth, input range and sampling frequency.

The FADC Mezzanine design has been analyzed in detail throughout the document. Special emphasis has been put on the main devices selection such as the FADC, establishing a reference point to proceed with the selection of the rest of devices such as the PLL and the topology of the analog drivers. Moreover, during the design of the analog stages, we studied the noise models applied to operational and fully-differential amplifiers, stepping forward thoroughly during the design of the analog part. Not less important, it should be noticed the design of the power supply stages and filters, crucial to succeed on achieving the desired resolution. In parallel with the inwards-wise design, a study of the interface between the FADC Mezzanine and the closer-in electronics to the detector was carried out. During the cable selection, crosstalk, bandwidth and EMI tests were performed to select the best solution to interconnect both parts, finally choosing the HDMI cable. During the output interface design between the FADC Mezzanines and NUMEXO2 motherboard, issues such as the power supply voltages, number of signals, data throughput and clock delivery were studied. To conclude with the Mezzanine design, the final stage was devoted mainly to study the effects in the PCB design of high-speed sampling systems. Achieving the finest noise performance is a goal which was not obtained at the first hit requiring five prototypes to achieve the desired ENOB. The

first prototypes made use of topologies based on current-feedback amplifiers, being replaced by fully-differential amplifiers in posterior versions. Finer tuning was required from the second prototype on, focusing on the analog trace layout and ground place structure. At the end, after fine-tuning all details, the specifications demanded by the physics were fulfilled, coping with the energy resolution and NGD performance.

In parallel with the FADC Mezzanine first prototype production, a testbench platform was developed with the proposal to verify the FADC Mezzanine performance. As the FADC Mezzanine is a custom device for a specific application, some elements such as interconnecting boards were designed specifically to interface the device under test with the commercial evaluation board ML605 and the laboratory equipment. A graphical user interface was designed to ease the development and testing process by providing on the one hand control tasks, and on the other hand data-analysis tools used to verify the performance of the device under test.

Once verified the suitability of the FADC Mezzanine design for our experimental application, the work related to the FADC Mezzanine has been split in two branches. The first was the production of a sufficient number of mezzanines to cope with the necessities of the early phases of NEDA. The second task concerns the integration of the FADC Mezzanine board with the rest of electronics and in the experimental environment. Regarding the first task, it should be remarked that the use of the testbench platform allowed a quick verification and commissioning for all FADC Mezzanines needed for the introductory phases of NEDA. All produced units have been tested successfully. It is important to notice that the test procedure for EXOGAM2 and NEDA have been different. For instance, as the firmware for the Virtex-6 developed by other collaboration parties was developed in parallel with the FADC Mezzanine, most of the IPs were available during the energy resolution tests. Besides, the rest of hardware electronics which were partially retrieved from the former front-end electronics such as the preamplifiers and the B3 board allowed the FADC Mezzanine performance tests in an environment closer to the real conditions, using a fully-implemented NUMEXO2 digitizer. Nevertheless, in case of NEDA, the design process has been carried in a different way. Nowadays, there are still electronic modules under development, such as the front-end electronics and part of the firmware IPs. Therefore, the first attempt to obtain measurements for the NGD performance before using NUMEXO2 was based on the implementation of off-line PSA and timing algorithms.

A specific chapter is dedicated to describe the integration the FADC Mezzanine with the NUMEXO2, performing a complete setup which included both the front-end electronics and the DAQ tools (GECO, Vigru, NARVAL, etc.) firstly at GANIL, and later on, in Valencia, gathering the parts from all collaboration parties in a single laboratory, an approach which is still under development for NEDA. During the NUMEXO2 development, several firmware IPs for NEDA were implemented using the ML605, such as the charge-comparison algorithm, and a fully-included version of the GTS envisaged to test all the functionalities into a single device. Since the implementation of the PSA and GTS IPs led to a successful behavior, the next step in an early future will consist of the migration of the PSA algorithm in NUMEXO2.

The main point which can be concluded from this work is that a fully-digital front-end electronics system has been introduced in a project in which the former front-end electronics were mostly based on analog systems. During the chapter 3, it was mentioned the former electronics from EXOGAM and Neutron Wall, based both on analog systems. Therefore, the usage of a new fully-digital front-end electronics system has provided the system of a state-of-the-art electronics with a high degree of flexibility and configurability, a feature difficult to achieve by analog means. Another fact is linked to the capability to perform experiments

involving higher counting rates, majorly due to the capability of off-line processing with pile-up reduction, and also, to the improvement of the bandwidth capabilities using fast optical links.

However, life is not all that beautiful with digital systems. In case of EXOGAM2, even though the specifications in terms of energy resolution were tied to obtain 2.3 keV@1.33 MeV, the resolution obtained with former EXOGAM analog electronics was still higher, 2.16 keV@1.33 MeV. Same as for NEDA, regarding the timing resolution obtained, still, the performance obtained with our digital electronics does not reach yet the performance obtained with analog electronics, where resolutions below 1 ns could be obtained with the appropriate setup. In any case, this is the drawback that entails the utilization of digital electronics in experiments related to radiation detection.

Taking into account the inherent problematic that the introduction of digital electronics carry on, mainly because the digitalization always entails an information loss, the slight loss of resolution has fitted into the specifications not far from the performance obtained with analog systems. Nevertheless, the direction of improvement followed by the introduction of digital electronics in the front-end was mostly focused on the added degree of flexibility, communications improvement and capability to perform on-line algorithms implemented in programmable devices, fact for which it can be concluded that the migration from analog to digital electronics has been mostly successful. Further improvements, at least for NEDA, will require firmware developments in views of performing high-resolution TOF measurements high resolution inside the FPGA, improving hence the NGD, and reducing drastically the total data throughput.

Another important point is the fact that this work has been carried out as a synergy between several projects, leading to a common solution and, subsequently to a reduction of resources. This has been the case for NUMEXO2 and also the FADC Mezzanines, where a successful attempt to implement a synergy at the level of front-end electronics has made possible the development of a common system both for EXOGAM2 and NEDA.

The usage of digital electronics with the FADC Mezzanine and NUMEXO2 digitizer opens new experimental opportunities in the field of nuclear physics given the overall improvement of the instrument, contributing on the research of exotic nuclei far from stability. Additionally, we must point out also the role of the FADC Mezzanine itself as a research work for high-speed and low-noise analog-to-digital conversion.

Contributions and outlook

Summarizing all the points into a single paragraph, a new digitizing FADC Mezzanine has been successfully implemented and integrated in the framework of EXOGAM2 and NEDA, improving the performance in terms of bandwidth capabilities and flexibility, fitting as well within a reasonable energy resolution, suitable to proceed on the experiments without a notorious information loss. Also, a second contribution to the new firmware for NEDA has been commissioned, being the starting point for the integration of the rest of electronics. This is the case of the PSA algorithm inside the Virtex-6, which, even though it is a prototype, it has proved its suitability to implement a first-level trigger algorithm for NEDA in its role of neutron-gamma discrimination. By using the presented algorithm most of the events produced by gamma-rays can be discarded, reducing the total data throughput.

From the last point on, the verification of NUMEXO2 whole setup for EXOGAM2, including as well the DAQ system, together with the verification of the PSA algorithms for NEDA in an evaluation platform, foresees firstly to migrate and integrate the PSA IPs for NEDA. This task is comprised in the framework to adapt the EXOGAM2 firmware for NEDA, not being only the PSA IP the only change to perform. In the first quarter of 2015 it is expected to make the NUMEXO2 system running including the PSA for 16 channels. As it is logical to envisage, the second goal is basically the use of NUMEXO2 in a real NEDA experiment. Hence, after all IPs for NUMEXO2 are integrated properly, together with the rest of electronic modules such as the front-end electronic boards, NEDA will take up experiments using the new digital electronics.

Annexes

A. Analog interface design and test

According to the general layout schema from Fig 3.3, NUMEXO2 digitizer and the FADC Mezzanines are placed 10m away from the detector and front-end electronics, requiring a physical connection between both parts. Due to the fast nature features from the signals, a testbench has been developed to characterize a set of different cables and determining the best solution applying bandwidth, crosstalk and EMI tests. Hence, a set of 4 cables have been characterized, allowing the selection of a FADC Mezzanine input connector.

A.1. Testbench equipment for cable measurements

The candidates for connection to the front-end are:

- MDSM coaxial cable, containing 19 coaxial connections
- HDMI cable
- HDMI v 1.4. Infinite
- PoCL-Lite camera cable.

Additionally, the extra equipment for the cable performance test includes:

- The arbitrary waveform generator AFG3252 from Tektronix, capable to synthetize signals with frequencies to 240 MHz and pulses involving rise and fall times until 2.5 ns, far enough for the Mezzanine requirements and for the cable test.
- High-voltage pulse generator NSG1025 from Schaffer, used to provide high-voltage peaks for the EMI test.
- The Oscilloscope TDS5104B from Tektronix, with a bandwidth of 1 GHz and sampling frequency of 5 Gsps.
- Connectors for the cables under test.
    - MDSM-15PE-Z*-VR22 for the MDSM multi-coaxial cable.
    - HDMR-19-01-X-SM-PF used for both HDMI cables v1 and 1.4 Infinite.
    - HDR-EC14LFDTG2 is used for the tests of the PoCL-Lite flex camera link.
- Adaptor boards. Provides an interface between the laboratory equipment and the cables under test using SMA. The board is depicted in Fig A.1.
- SMA/BNC connectors and terminators.

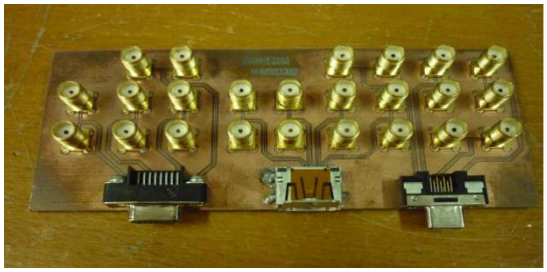


Figure A.1: Adaptor board for the cable test

Fig. A.2. shows the complete testbench with the adaptor boards, the cables and the generators.

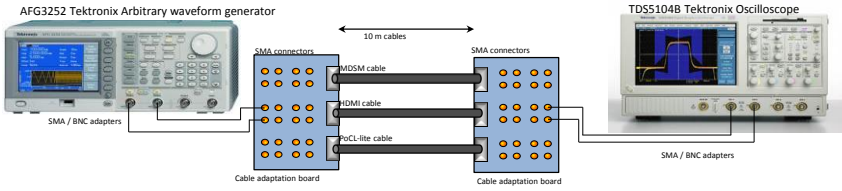


Figure A.2: Cable testbench schema

A.2. Bandwidth measurements

The procedure to measure the bandwidth consists of driving sinusoidal input signals with constant amplitude across a frequency sweep, measuring the amplitude degradation at the output versus the frequency. Then, the bandwidth is then calculated as the frequency at which the input amplitude decreases by 3 dB below the input voltage. The bandwidth setup test is described in Fig. A.3.

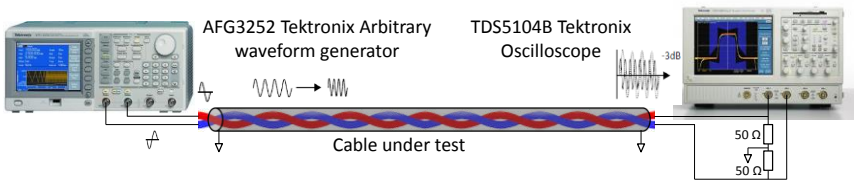


Figure A.3: Cable test setup for bandwidth measurements

Provided the generator dual output, the tests can be carried out using the second channel in inverted polarity synchronized with the other channels. Analogously, the output is measured with the oscilloscope using the MATH function to calculate the differential voltage. For the tests 2 V_{pp} differential sinusoidal inputs from 100 kHz to 240 MHz were used, taking a set of 10 data points per decade from 1 MHz to 240 MHz and 1 point per decade from 10 kHz to 1 MHz, establishing the low-frequency data as reference.

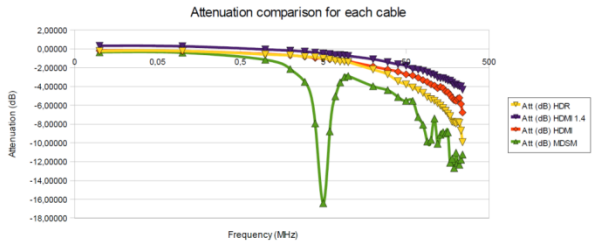


Figure A.4: Frequency plot of the cable bandwidth

Results for bandwidth are summarized in Table A.1 and Fig. A.4, where the frequency response is depicted. All cables show an ideal behavior until they reach 1 MHz. At 5 MHz the multi-coaxial cable exhibits a strange behavior, which starts to lose performance after a few MHz, and making it unsuitable for the application. The rest of the cables show a characteristic single-pole-like frequency response.

Table A.1: Bandwidth results for different cable tests.

Cable under test	- 3 dB point (BW)	- 6 dB point
MDSM	--	--
HDMI	70 MHz	230 MHz
HDMI v1.4 Infinite	120 MHz	> 240 MHz
PoCL-Lite	35 MHz	130 MHz

Results from Table A.1 prove that the most appropriate cables which accomplish the requirements are the both of the HDMI versions, even though the HDMI v1 has a very tight bandwidth if we compare the requirements for NEDA.

A.3. Crosstalk measurements

Crosstalk tests are performed by driving on one of the pairs a differential pulse and measuring the induced voltage on a second victim pair at the far-end. Specially, it is interesting to study the effect for different edge times, where the measurements have been using with10ns and 2.5 ns, even though the latter is out of the specifications, aimed mostly to measure the cable robustness against coupling. The waveforms used for this tests consists of square waveforms of 1 V (and -1V for the inverted input), and according to Fig. A.5, the unused pairs must be terminated in order to avoid reflections from the victim pairs.

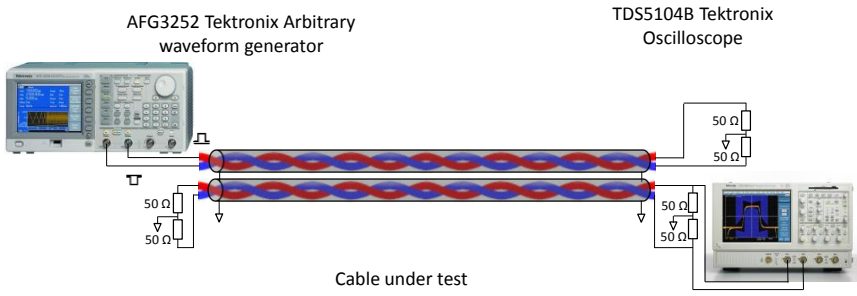


Figure A.5: Cable test setup for crosstalk measurements

The crosstalk measurements are summarized in Table A.2 for 10ns and 2.5 ns edge times, obtaining the crosstalk of the differential signal (and not the induced crosstalk on each pair conductor)

Table A.2: Crosstalk test comparison table for different cables at different rise / falling times

Cable	t_r = 10 ns	t_r = 2.5 ns
MDSM	14 mV	43.8 mV
HDMI	2.73 mV	3.82 mV
HDMI v1.4 Infinite	3.94 mV	8.02 mV
PoCL-Lite	3.16 mV	4.18 mV

Results evidence the higher suitability of the HDMI cables versus their counterparts PoCL-Lite and MDSM.

A.4. EMI measurements

Since the experimental area undergoes processes involving radiation, it is of major interest to test the shielding and grounding robustness against high-voltage peaks susceptible to be induced into the cable. EMI measurements can be implemented by applying high-voltage pulses induced to the cable by means of a conductive surface such as a piece of foil paper embracing part of the cable outer surface. The setup to measure the cable EMI is depicted in Fig. A.6. As well as it was made for crosstalk measurements, for the experimental procedure, it is required to terminate correctly each unused pair, preventing the cable from undesired reflections which could falsify the measurements.

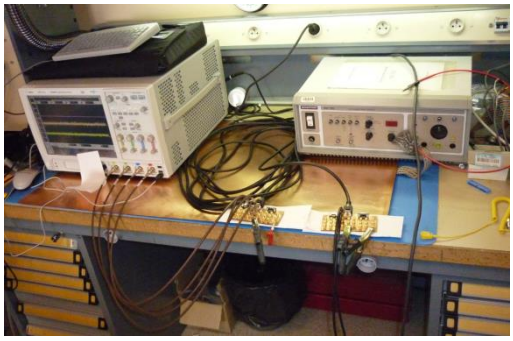


Figure A.6: Picture of the EMI tests at GANIL in June 2011

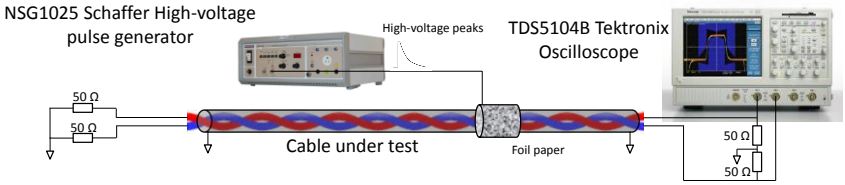


Figure A.7: Cable test setup for electromagnetic interference measurements

A high-voltage pulse generator NSG1025 from Schaffer was used to inject 1 kV high-voltage pulses of 1 μs width with a 50 Hz periodicity. Besides, a copper plate was used to ground the whole testbench by grounding the equipment chassis, as depicted in Fig A.7. The EMI results for the tested cables are synthetized in Table A.3.

Table A.3: EMI results for different cables.

Cable under test	Peak-to-peak of the induced voltage for 1 kV voltage peak
HDMI v1.4 Infinite	356 mV
HDMI	1.077 V
PoCL-Lite	6.252 V

Given the HDMI v 1.4 Infinite double-shielding features, it performs much better against high-voltage peaks than the other two candidates.

A.5. Conclusions

Based on the measurements performed, it is clearly obvious the unsuitability of the MDSM cable due to its high crosstalk level and dreadful frequency response. However, both HDMI and HDR show a satisfactory bandwidth, compliant for the new EXOGAM2 electronics. Nevertheless HDR PoCL-Lite cable fails for NEDA specifications with its 35 MHz bandwidth, feature which is accomplished by their HDMI counterparts. HDMI v1.4. offers a bandwidth feature more than enough for NEDA, although HDMI v1 bandwidth of 70 MHz is still too tight for low for NEDA specifications.

Crosstalk results reveal that PoCL-Lite does not cancel properly the crosstalk, since the induced peaks are coupled in different signs to the pair, obtaining a difference twice the original value. This unexpected and undesirable effect makes it less preferable towards other candidates such as the HDMI versions, in which the crosstalk is induced in both lines with the same sign, being then cancelled when receiving the differential signal.

Finally, for the EMI measurement it has been evidenced that HDMI v 1.4 performs the best with its 356 mV (for 1 kV peak) due to its double-shielding construction. However, this excellent performance in terms of EMI and crosstalk brings a drawback on the mechanical side, producing a big strain on the front panel. Due to mechanical stiffness issues an accessory which includes a screw for easy plug-in plug-out is located at each connector extreme, allowing an improved fixation of the HDMI.

In conclusion, according to all the results obtained, the choice for a cable was inclined to use the HDMI cable. Even though EXOGAM2 is able to use the HDMI v1, providing good crosstalk and EMI results for a reasonable economic and light cable, the case differs strongly for NEDA, demanding the use of the v1.4 Infinite. Nevertheless, the choice of any of the two HDMI versions does not make a difference on the FADC Mezzanine design since the PCB connector is the same.

List of Figures

List of Tables

Acknowledgments

The fact that this work could have been carried out is not a merit that someone can keep for oneself, but it is, absolutely the opposite. Teamwork, collaboration and learning from the experienced people are the words which could summarize the fulfillment of this text.

- Firstly, I would like to thank my directors Dr. Vicente González Millán and Dr. Andrés Gadea Raga to tutoring and assist me during this four-year work, helping me in some tasks and introduce me into the world of research.
- I also want to thank the GAP team from GANIL, which was in fact the starting point for me into all of this story, specially to Michel, Abder, Charles and the rest of the people who is working there. Also I would like to thank Gilles de France in order to facilitate me the opportunity of a staying there and Chiheb, an ex-member of the GAP for the great time spent in there.
- Also, I want to thank to Dr. Enrique Sanchis, in order to allow me the opportunity to work with them.
- May the list continue on, the next ones are my university colleagues whom I spent with them every coffee. Gess, Javier, Chema, Ramón, Pablo, Fernando and David.
- A special thank to help with development of the testbench platform must be addressed to Dr. Marcin Jastrząb, for the best moments both in the laboratory and also, in the bar.
- Also to the people from the rest of the NEDA collaboration, specially to José Javier Valiente, which allowed me to perform the measurements in Legnaro and to spend a good time there.

Finalment, les últimes dedicatòries van per als meus amics i la meua família, donat el seu suport incondicional. Podria no acabar la llista, però entre ells van als meus pares, a Ainara, Jean, Gonzalo, Carlos, Merxe, Raquel i els meus avis.

This work has been supported by the Generalitat Valenciana, Spain, under grant PROMETEO/2010/101 and by the Spanish MINECO under grants AIC-D-2011-0746, FPA2011-29854 and FPA2012-33650.

References

[1] W. Korten, S.Lunardi, «Achievements with EUROBALL spectrometer» October 2003. [Online]. Available: http://irfu.cea.fr/Sphn/Deformes/EB/eb-report-final.pdf.

[2] G. de Angelis, A. Bracco, D. Curien «The EUROBALL gamma ray detector spectrometer» Eurphysics News, 2003. [Online]. Available: http://idefix.mi.infn.it/~wieland/paper_wieland/articleeuroball.html.

[3] F. S. Goulding, D. A. Landis, N. Madden, M. Maier, H. Yaver Goulding, «GAMMASPHERE - Overview of Detector and Signal Processing System,» *Nuclear Science Symposium and Medical Imaging Conference Record, 1995,* vol. 1, pp. 432-436, 1995.

[4] J. Erberth et al, «Miniball: A Gamma-Ray Spectrometer With Position-Sensitive Ge Detectors For Nuclear Structure Studies At REX-ISOLDE» *Frontiers of Nuclear Structure,* nº CP656, pp. 349-356, 2003.

[5] G. de France, «EXOGAM detectors» GANIL, [Online]. Available: http://pro.ganil-spiral2.eu/laboratory/detectors/exogam/exogam-detectors.

[6] S. Akkoyun et al., «AGATA - Advanced Gamma Tracking Array,» *Nuclear Instruments and Methods in Physics Research,* nº 668, pp. 26-58, 2012.

[7] C.W.Beausang et al, «GRETA. The gamma-ray energy-tracking array. Status of the development and physics opportunities» *Nuclear Instruments and Methods,* vol. B 204, pp. 66-74, 2003S.

[8] J. Nyberg, «Neutron Wall,» 27-30 May 2008. [Online]. Available: http://egp-workshop.in2p3.fr/docs/Talks-Mardi/nwall-jn.pdf.

[9] Ö. Skepstdedt et al, «The EUROBALL neutron wall – design and performance tests of neutron detectors,» *Nuclear Instruments and Methods,* vol. A421, pp. 531-541, 1999.

[10] J.J. Valiente-Dobón, «NEDA - Neutron Detector Array,» 22-25 February 2012. [Online]. Available: http://www.mi.infn.it/WSBormio-Milano2012/Doc/TALK/Dobon-Bormio12-web.pdf.

[11] G. Jaworski et al., «Montecarlo Simulation of a single detector unit for the neutron array NEDA» *Nuclear Instruments and Methods A,* vol. 673, pp. 64-72, 2012.

[12] D. Mengoni, «Status of the TRACE Array,» November 2010. [Online]. Available: http://agenda.infn.it/getFile.py/access?contribId=55&sessionId=30&resId=0&mater

ialId=slides&confId=2660.

[13] B. Nyakó, «Performance of the DIAMANT detecotr at GANIL and plans for improvements,» 26 April 2007. [Online]. Available: http://ew2007.ganil.fr/presentation/Nyako-EXOGAM-WS07-final.pdf.

[14] B. Lofstedt. e. al., «A Digital Front-End and Readout Microsystem for Calorimetry at LHC - The FERMI Project,» *IEEE,* Vols. %1 de %20-7083-0883-2/93/$3.00/, 1993.

[15] L.Bardelli, G.Poggi «Digital Sampling Systems in High-resolution and Wide Dynamic Range Energy Measurements» *Nuclear Instruments and Methods in Physics Research A,* vol. 560, pp. 571-523, 2006.

[16] A. Pullia, «Design-Charted Aided Optimization of Digital Spectrometers» *Transactions of Nuclear Science,* vol. 49, nº 4, pp. 1791-1797, 2002.

[17] G. de France, «EXOGAM2 + NEDA» June 2009. [Online]. Available: http://www.slcj.uw.edu.pl/neda/istanbul/presentations/9-france.NEDA_meeting_June09.ppt.. [Último acceso: 6 February 2013].

[18] M. Tripon, «EXOGAM2 Technical Specifications,» GANIL, 2012. [Online]. Available: http://pro.ganil-spiral2.eu/laboratory/detectors/exogam/the-exogam2-project

[19] K. Krane, Introductory Nuclear Physics, John Wiley and sons, 1987.

[20] A. Sonzogni, «Chart of Nuclides,» NNDC, [Online]. Available: http://www.nndc.bnl.gov/chart/. [Último acceso: 20 March 2013].

[21] G.F.Knoll, Radiation Detection and Measurement, Michigan: John Wiley & Sons Inc., 1999.

[22] P.-A. Söderström, «Development of Nuetron Detectors for the Next Generaton of Radioactive Ion-Beam Facilities,» Uppsala Universitet, Uppsala, 2009.

[23] W.R.Leo, Techniques for Nuclear and Particle Physics Experiements, Switzerland: Springer-Verlag, 1993.

[24] A.K.Singh et al. «Detailed study of magnetic rotation in 196Pb,» *Nuclear Physics A,* vol. 707, pp. 3-31, 2002.

[25] S. Lunardi, «The gamma-ray spectrometer GASP,» [Online]. Available: http://www.infn.it/csn3/esperimenti2001/sommario/gasp.pdf. [Último acceso: January 2013].

[26] O. Roberts et al., «Neutron Response of 1.5" LaBr3(Ce) Crystal Scintillators for PARIS,» November 2008. [Online]. Available:

http://paris.ifj.edu.pl/documents/detectors/Ce.pdf.

[27] L.J. Meng et al., «The design and performance of a large-volume spherical CsI(Tl) scintillation counter for gamma-ray spectroscopy,» *Nuclear Instruments and Methods A,* vol. 485, pp. 468-476, 2002.

[28] F.C.L. Crespi et al. «HPGe detectors timing using pulse shape analysis technique» *Nuclear Instruments and Methods,* 2010.

[29] «Universitet I Oslo» [Online]. Available: https://wiki.uio.no/mn/safe/nukwik/index.php/Gamma_Spectroscopy_and_Detectors.

[30] Radiochemical Methods Group, W1V 0BN. Royal Society of Chemistry, «Discovery of radioactivity,» Royal Society of Chemistry, [Online]. Available: http://www.rsc.org/images/essay1_tcm18-17763.pdf. [Último acceso: 20 March 2013].

[31] W. Gellety, J. Erberth «Gamma rays. Past present and future» 2006. [Online]. Available: http://www.euroschoolonexoticbeams.be/site/files/nlp/LNP700_contrib3.pdf.

[32] J. Eberth, «From Ge(Li) detectors to gamma-ray tracking arrays – 50 years of gamma spectroscopy with germanium detectors,» *Progress in Particle and Nuclear Physics,* vol. 60, p. 283–337, 2008.

[33] N. Tsoulfanidis, Measurement and Detection of Radiation, University of Missouri-Rolla: Taylor and Francis, Second edition, 1995.

[34] J. Erberth, «From Ge(Li) detectors to AGATA to gamma-ray tracking arrays (AGATA),» 24 March 2011. [Online]. Available: http://wwwgerda.mppmu.mpg.de/symp/02_Eberth.pdf. [Último acceso: 7 February 2013].

[35] S. Arnell et al. «A 2-pi neutron and -y-ray multiplicity filter for the NORDBALL detection system» *Nuclear Instruments and Methods,* vol. A 300, pp. 303-311, 1991.

[36] Y. Ötkem, «Multi-detector arrays,» [Online]. Available: http://thm.ankara.edu.tr/tac/YAZOKULU/yazokulu2/dersnotlari/oktem_school.pdf

[37] J-L. Biarrote et al. «Beam Dynamics Studies For The Spiral-2 Project. Proceedings of EPAC 2006» 2006. [Online]. Available: https://accelconf.web.cern.ch/accelconf/e06/PAPERS/WEPCH007.PDF.

[38] G. de Angelis, «SPES: the INFN exotic beam ISOL facility @ LNL» 2013. [Online]. Available: https://indico.cern.ch/event/248321/session/4/contribution/10/material/slides/0.pdf.

[39] I. Rittersdorf, «Gamma-ray spectroscopy,» 20 March 2007. [Online]. Available: http://www-personal.umich.edu/~ianrit/gammaspec.pdf.

[40] T.W.Crane, M.P.Baker «13 - Neutron detectors» [Online]. Available: http://www.fas.org/sgp/othergov/doe/lanl/lib-www/la-pubs/00326408.pdf.

[41] P. Rinard «12 - Neutron Interactions with Matter» [Online]. Available: http://www.fas.org/sgp/othergov/doe/lanl/lib-www/la-pubs/00326407.pdf.

[42] KMetz «Aromaticity description for non-science nerds» 24 February 2011. [Online]. Available: http://organickmetz.blogspot.com.es/2011/02/aromaticity-description-for-non-science.html.

[43] H. Spieler, «Radiation Detectors and Signal Processing,» 8-12 October 2001. [Online]. Available: http://www-physics.lbl.gov/~spieler/Heidelberg_Notes_2001/index.html.

[44] L.M. Bollinger, G. Thomas, «Measurement of the Time Dependence of Scintillation Intensity by a Delayed-Coincidence Method» *Review of Science Instruments,* vol. 32, nº 1044, 1961.

[45] Oxford Journals «Radiation Protection Dosimetry» [Online]. Available: http://rpd.oxfordjournals.org/content/126/1-4/253/F1.expansion.

[46] R. Pestotnik, S. Korpar, H. Chagani, R. Dolenec, P. Krizan, A. Stanovnik, «Silicon Photo-multipliers as Photon Detectors for PET» *IEEE NuclearScience Symposium Conference Record,* vol. N50, pp. 3123-3127, 2008.

[47] Photonis Imaging. Sensors «Photomultiplier tubes basics» [Online]. Available: http://particle.korea.ac.kr/lab/cata_basic.pdf.

[48] J. Gerl «High-resolution detectors in nuclear spectroscopy» *Nuclear Instruments and Methods in Physics Research A,* vol. 442, pp. 238 - 243, 2000.

[49] M. Rejmund et al. «Performance of the improved larger acceptance spectrometer: VAMOS++» *Nuclear Instruments and Methods in Physics Research A. doi:10.1016/j.nima.2011.05.007,* 2011.

[50] I.Lazarus, «The EXOGAM Electronics System Architecture» [Online]. Available: http://npg.dl.ac.uk/documents/edoc405/System-Arch-v05.htm.

[51] R. Faragher, «Understanding the Basis of the Kalman Filter Via a Simple and Intuitive Derivation» IEEE SIGNAL PROCESSING MAGAZINE, 20 August 2012. [Online]. Available: https://www.cl.cam.ac.uk/~rmf25/papers/Understanding%20the%20Basis%20of%20the%20Kalman%20Filter.pdf.

[52] A. Maj, «PARIS detector» November 2011. [Online]. Available:

http://agata03.ific.uv.es/WSPrometeo_2011/presentations/Maj_PARIS.pptx.

[53] A. Pipidis et al. «The Genesis of NEDA (NEutron Detector Array): Characterizing its Prototypes» LNL anual report.

[54] T. Hüyük. et al. «Conceptual Design of the NEutron Detector Array (NEDA) and an early implementation of NEDA with AGATA» *Submitted to NIM A,* 2014.

[55] X.L. Luo et al. «Test of digital neutron–gamma discrimination with four different photomultiplier tubes for the NEutron Detector Array (NEDA) » *Nuclear Instruments and Methods in Physics Research A,* vol. 767, pp. 83-91, 2014.

[56] E. Ronchi et al. «An artificial neural network based neutron–gamma discrimination and pile-up rejection framework for the BC-501 liquid scintillation detector» *Nuclear Instruments and Methods,* vol. A 610, pp. 534-539, 2009.

[57] M. Bellato et al. «Sub-nanosecond clock synchronization and trigger management in the nuclear physics experiment AGATA,» *Journal of Instrumentation,* vol. 8, nº P07003, 2013.

[58] Analog Devices. Walt Kestler, «Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor» 2009. [Online]. Available: http://www.analog.com/static/imported-files/tutorials/MT-003.pdf.

[59] A. Georgiev, W. Gast and R.M.Lieder «An Analog-to-Digital Conversion Based on a Moving Window Deconvolution» *Transactions on Nuclear Science, IEEE,* vol. 41, nº 4, pp. 1116-1124, 1994.

[60] Analog Devices. Walt Kester, «MT-001 Tutorial. Taking the Mystery out of the Infamous Formula, "SNR = 6.02N + 1.76dB" and Why You Should Care» 2009. [Online].

[61] SIS GmBH, «SIS3350 500 MHz 12-bit VME Digitizer» 28 January 2009. [Online]. Available: http://orca.physics.unc.edu/~markhowe/VME/SIS3350_files/sis3350.pdf.

[62] V. Modamio et al. «Timing for liquid scintillators» Presented in Acireale, at the NuPNET NEDENSAA meeting, 20-22 February 2013. [Online].

[63] P-A. Söderström et al. «Digital pulse-shape discrimination of fast neutrons and g rays» *Nuclear instruments and methods,* vol. 594, pp. 79-89, 2008.

[64] Texas Instruments, «14-/12-Bit, 250-MSPS ADCs With Integrated Analog Buffer,» October 2008. [Online]. Available: http://www.ti.com/lit/ds/symlink/ads61b49.pdf.

[65] Texas Instruments, «Dual channel, 14-bit, 125/105/80/65 MSPS ADC with serial LVDS outputs» May 2007. [Online]. Available: http://www.ti.com/lit/ds/slas542a/slas542a.pdf.

[66] Analog Devices, «14-Bit, 170 MSPS/250 MSPS, JESD204B, Dual Analog-to-Digital Converter. Datasheet AD9250. Revision B» 2012. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD9250.pdf.

[67] Texas Instruments Inc., «Dual Channel 14-/12 bits 250-/210 MSPS ADC with DDR LVDS and Parallel CMOS outputs - SLAS635B» April 2009, Revised January 2011.

[68] Linear Technologies, «LTC2157-14 /LTC2156-14/ LTC2155-14. Dual 14-Bit 250Msps/210Msps/170Msps ADCs» 2011. [Online]. Available: http://cds.linear.com/docs/en/datasheet/21576514fb.pdf.

[69] Analog Devices, «14-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC). Datahseet AD9643. Revision E,» 2011. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD9643.pdf.

[70] Analog Devices. W. Kestler, «ADC Architectures V: Pipelined Subranging ADCs. MT-024 Tutorial,» 2009. [Online]. Available: http://www.analog.com/static/imported-files/tutorials/MT-024.pdf.

[71] Brad Bannon and Allen Barlow. Analog Devices, «Aperture Uncertainty and ADC System Performance. Application note AN-501,» 2006.

[72] Analog Devices. Paul Smith, «Little Known Characteristics of Phase Noise,» 2004.

[73] Texas Instruments, «Ten Output High Performance Clock Synchronizer, Jitter Cleaner, and Clock Distributor,» June 2008. [Online]. Available: http://www.ti.com/lit/ds/symlink/cdce72010.pdf.

[74] Analog Devices, «1.2 GHz Clock Distribution IC, PLL Core, Dividers, Delay Adjust, Eight Outputs» 2005. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD9510.pdf.

[75] National Semiconductors, «Precision clock conditioner with Integrated VCO. Datasheet 202114» September 2010.

[76] Analog Devices, «Dual 600 MHz, 50 mW Current-feedback amplifier. Revision D,» 2001. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD8002.pdf.

[77] Analog Devices, «Low Cost, High Speed Differential Amplifier. Revision I,» 2009. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD8132.pdf.

[78] Texas Instruments, «Wideband, Low-noise, Low-distortion, fully-differential amplifier» January 2005, Revised November 2009. [Online]. Available: http://www.ti.com/lit/ds/symlink/ths4509.pdf.

[79] Analog Devices, «Low Noise, Rail-to-Rail, Differential ADC Driver. Datasheet AD8139. Revision B» 2007. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD8139.pdf.

[80] Texas Instruments, «DAC8532 Dual-Channel, Low Power, 16-Bit, Serial Input Digital-to-Analog Converter. SBAS246A» December 2001 - Revised May 2003.

[81] Analog Devices, «1.8 nV/√Hz, 36 V Precision Amplifiers,» 2011 Revision G. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADA4004-1_4004-2_4004-4.pdf.

[82] Analog Devices, «Low Noise, 1 GHz Fast FET Op Amps,» 2008 Revision O. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADA4817-1_ADA4817-2.pdf.

[83] Texas Instruments, «2.2nV/√Hz, Low-Power, 36V Operational Amplifier,» November 2008. [Online]. Available: http://www.ti.com/lit/ds/symlink/opa209.pdf.

[84] Analog Devices, «Single and Dual, Ultralow Distortion, Ultralow Noise Op Amps,» 2007, Revision D, 2013. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD8597_8599.pdf.

[85] Ken Chan, Texas Instruments, «Design of Differential Filters for High-Speed Signal Chains. Application Report SLWA053B,» November 2007, Revised April 2010. [Online]. Available: http://www.ti.com/lit/an/slwa053b/slwa053b.pdf.

[86] R. Pallàs-Areny, Óscar Casas, «Basics of Analog Differential Filters» *IEEE Transactions on Instrumentation and Measurement,* vol. 45, nº 1, pp. 275-279, 1996.

[87] Texas Instruments, «AN-1719. Noise Figure Analysis Fully Differential Amplifiers. Application report,» 2007. [Online]. Available: http://www.ti.com/lit/an/snoa506a/snoa506a.pdf.

[88] R. Pallàs-Areny, Analog Signal Processing, Wiley-Interscience, 1999.

[89] Texas Instruments, «SN74LVC2G126. Dual Bus Buffer Gate With 3-State Outputs (Rev. J),» April 1999, Revised January 2007. [Online]. Available: http://www.ti.com/lit/ds/symlink/sn74lvc2g126.pdf.

[90] Samtec, «High Speed Combo RF & Power. F-213,» [Online]. Available: http://www.samtec.com/documents/webfiles/pdf/qfs_pc.pdf.

[91] Texas Instruments, «Ultralow-Noise, High PSRR, fast, RF, 1A Low-Dropoutlinear regulators. SLVS351N,» September 2002, Revised January 2011. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps79650.pdf.

[92] Linear Technologies, «LT1175. 500mA Negative Low Dropout Micropower Regulator,» November 2009, Revised July 2011. [Online]. Available:

http://cds.linear.com/docs/en/datasheet/1175ff.pdf. [Último acceso: June 2013].

[93] TDK, «Inductors for Decoupling Circuits, Multilayer/STD, Magnetic Shielded MLZ series,» May, 2012.

[94] H. Johnson, M. Graham. High-speed digital design. A handbook of black magic, Prentice Hall. ISBN 0-13-395724-1, 1993.

[95] Lab-Circuits, «Parámetros de fabricación multicap,» February 2012. [Online]. Available: http://www.lab-circuits.com/es/para_fabricacio_multicapa.php.

[96] Analog Devices, «Low Noise, Precision 16 V CMOS Rail-to-Rail Operational Amplifiers. AD8661/AD8662/AD8664» 2006 Revision D. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/AD8661_8662.pdf.

[97] Analog Devices, «AN-282. Fundamentals of Sampled Data systems»

[98] Maxim application notes, «INL / DNL Measurements of High-Speed Analog-To-Digital Converters (ADCs) » September 2000. [Online].

[99] EDICIONES TECNICAS REDE SA, «Medidas de las INL/DNL en los convertidores A/D de alta velocidad,» *REVISTA ESPAÑOLA DE ELECTRONICA,* vol. 544, nº ISSN: 0482-6396, pp. 70-74, Marzo 2000.

[100] Maxim, «Histogram Testing Determines DNL and INL errors» *Application note 2085,* 2003.

[101] J. Blair, «Histogram Measurement of ADC Nonlinearities Using Sine Waves» *Transactions on Instrumentation and Measurement,* vol. 43, nº 3, pp. 373-383, 1994.

[102] Xilinx, «ML605 Hardware User Guide. UG534» October 2012. [Online]. Available: http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf.

[103] Xilinx, «ML505/ML506/ML507 Evaluation Module User Guide. UG347,» May 2011. [Online]. Available: http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf.

[104] Xilinx, «Virtex-6 FPGA SelectIO Resources. UG361,» November, updated 2014. [Online]. Available: http://www.xilinx.com/support/documentation/user_guides/ug361.pdf.

[105] National Instruments, «Introduction to LabView Design Patterns» [Online]. Available: http://www.ieee.li/pdf/viewgraphs/labview_design_patterns.pdf.

[106] V. Modamio et al. *Nuclear Instruments and Methods A,* vol. 775, pp. 71-76, 2015.