A NANO-CMOS BASED UNIVERSAL VOLTAGE LEVEL CONVERTER FOR MULTI-V_{DD} SoCs

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Power dissipation of integrated circuits is the most demanding issue for very large scale integration (VLSI) design engineers, especially for portable and mobile applications. Use of multiple supply voltages systems, which employs level converter between two voltage islands is one of the most effective ways to reduce power consumption.

In this thesis work, a unique level converter known as universal level converter (ULC), capable of four distinct level converting operations, is proposed. The schematic and layout of ULC are built and simulated using CADENCE. The ULC is characterized by performing three analysis such as parametric, power, and load analysis which prove that the design has an average power consumption reduction of about 85-97% and capable of producing stable output at low voltages like 0.45V even under varying load conditions.

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CHAPTER 1

INTRODUCTION AND MOTIVATION

1.1 Introduction

Portable devices like cell phones, personal digital assistants (PDA), laptops, digital cameras and a variety of such other devices are highly popular among various users in the market. This requirement for portability has put forth number of restrictions on the size, weight, and battery life of such devices [Chandrakasan 1992, Mohanty 2001]. Low power design is the key to meet the demands for such lightweight and longer battery life devices. Hence, power dissipation is one of the fundamental design concerns that current day very large scale intregration (VLSI) design engineers have to cope with while dealing with integrated circuit designs. Power minimization is not only essential for portable devices but also necessary for improving reliability of high-end microprocessors and data processing which include real time data processing and decoding of audio/video data [Igarashi 2000, Mohanty 2001]. Significant research progress has been made during recent years to reduce the power dissipation of an integrated circuit.

1.1.1 Sources of Power Dissipation

The total power consumed by a circuit can be basically categorized into four types: (i) capacitive switching power, (ii) power consumption due to short circuit current, (iii) sub-threshold leakage power, and (iv) power consumption due to leakage

current [Sadeghi 2006, Chandrakasan 1992, Mohanty 2001]. This can be shown using the equation (1):

$$P_{total} = \alpha C V_{dd}^2 f + I_{sc}.V_{dd} + I_{sub}.V_{dd} + I_{gateleakage}.V_{dd} \quad [1]$$

In the above equation the first term represents the power consumption due to switching activity in the system. This type of power consumption is called as *dynamic power*. In equation (1), α is the switching activity, C is the capacitance of the load, f is the clock frequency and V_{dd} is the supply voltage. The second term of the equation represents the power consumption due to static current or dc current. This type of power consumption is called as static power. The static current arises due to the presence of path for direct connection between voltage source V_{DD} and ground. The power consumption due to static current is highly undesirable in low power designs. Finally, the third and the last terms in the equation (1) represent the power consumption due to leakage currents. Leakage current results from substrate injection and sub threshold effects [Chandrakasan 1992].The other form of leakage current is gate leakage current, arising from gate oxide which is mostly dependant on gate oxide thickness. Among these four, types the power consumption of an integrated circuit is mostly dominated by the dynamic power consumption [Sadeghi 2006, Mohanty 2001]. This is because the dominant feature in any well designed circuit is its switching activity [Chandrakasan 1992].

1.1.2 Techniques for Power Reduction

It is evident from equation (1) that the power consumption varies quadratically with the supply voltage. Thus, lowering the supply voltage will reduce the power

consumption quadratically. This is one way of achieving power dissipation reduction of an integrated circuit. But, this method is not considered as an efficient way for achieving power minimization because lowering supply voltage will increase the propagation delay of the circuit [Mohanty 2005].

Researchers have developed a variety of techniques to reduce the power consumption which include transistor sizing, multiple threshold voltage *(V_{TH}),* using multiple channel lengths and oxide thicknesses for reduction of various forms of power consumptions as presented in equation (1). Transistor sizing is an efficient method to achieve a good tradeoff between power minimization and performance of the design [Ishihara 2004]. It has been proved that by transistor sizing for equal rise and fall time, the short-circuit component of the total power dissipation can be maintained at less than 20% [Veendrick 1984]. However these techniques suffer from certain drawbacks as described. First of all, the power reduction achieved from transistor sizing reduces as soon as the slack in the circuit begins to disappear [Ishihara 2004]. As stated above, the power dissipation reduction by lowering supply voltage affects the performance of the circuit as it increases the propagation delay. For some applications, this low performance can be improved by pipelining and parallelism, but it increases the latency of the design [Chandrakasan 1992, Ishihara 2004]. Also, the power reduction by these techniques suffers from the effects of increase in leakage current. Thus, compared to these methods one of the most effective ways to lower power dissipation is by using multi-voltage systems wherein the chip is supplied with multiple voltages. Through a multi-voltage system power reduction can be achieved without the degrading the

performance of the system. This technique does not affect the latency of the system. The biggest advantage of this scheme is that same fabrication techniques can be used for processing the chip. And also there is no need for creating parallel / pipelined data paths which in turn result into heavy area penalty increasing the latency of the design [Sundararajan 1999].

1.2 Need for Level Converter

Multiple voltage supply systems are most efficient and commonly employed techniques for low power designs. The idea behind this technique is to use multiple supply voltages for a single chip by dividing the integrated circuit into regions, called *voltage islands*, operating at different voltages. The circuits which are on the critical path are supplied higher voltage level (V_{DDH}) and the circuits which are off the critical path are made to run at a lower voltage level (V_{DDL}) [Usami 1997]. A level converter is needed at the interface of a gate operating at V_{DDL} and a gate operating at V_{DDH}. The insertion of level converter between two voltage islands is essential to avoid the static current which might lead to undesirable power consumption [Yu 2001]. Thus a level converter can be defined as a simple circuit which converts the voltage at its input from one voltage level to another. A level converter can be inserted according to the requirement of level conversion in a circuit. Level converters which are inserted only at the interface of the cells operating at different voltage levels are synchronous level converter. The level converters which are inserted anywhere in the circuit wherever level conversion is required are known as asynchronous level converters [Usami 1997].

A detailed description of multi-voltage supply systems is given in [Usami 1997]. This concept of level converters can be more clearly explained through Fig. 1.2 which shows a multi- V_{DD} system where the system is divided into voltage islands operating at dual voltages V_{DDH} and V_{DDL}. Transistor level circuit diagram of and AND gate andan inverter which are working at different voltages. The inverter I1 is operating at lower voltage (V_{DDL}) and the AND gate I2 is operating at higher voltage (V_{DDH}). The two gates are connected directly without any level converter such that output of I1 is driving the gates of I2. In such scenario, when the input node N1 swings from high to low, then output at node N1 is not sufficient to turn off the pull up network of I3 completely. At the same time the pull down network is also switched on, as a result of this there exists a direct path for static current flow from V_{DD} to ground. This flow of static current is highly undesirable as it consumes more power. Thus, a level converter is inserted at the interface of the voltage islands operating at different voltage levels.

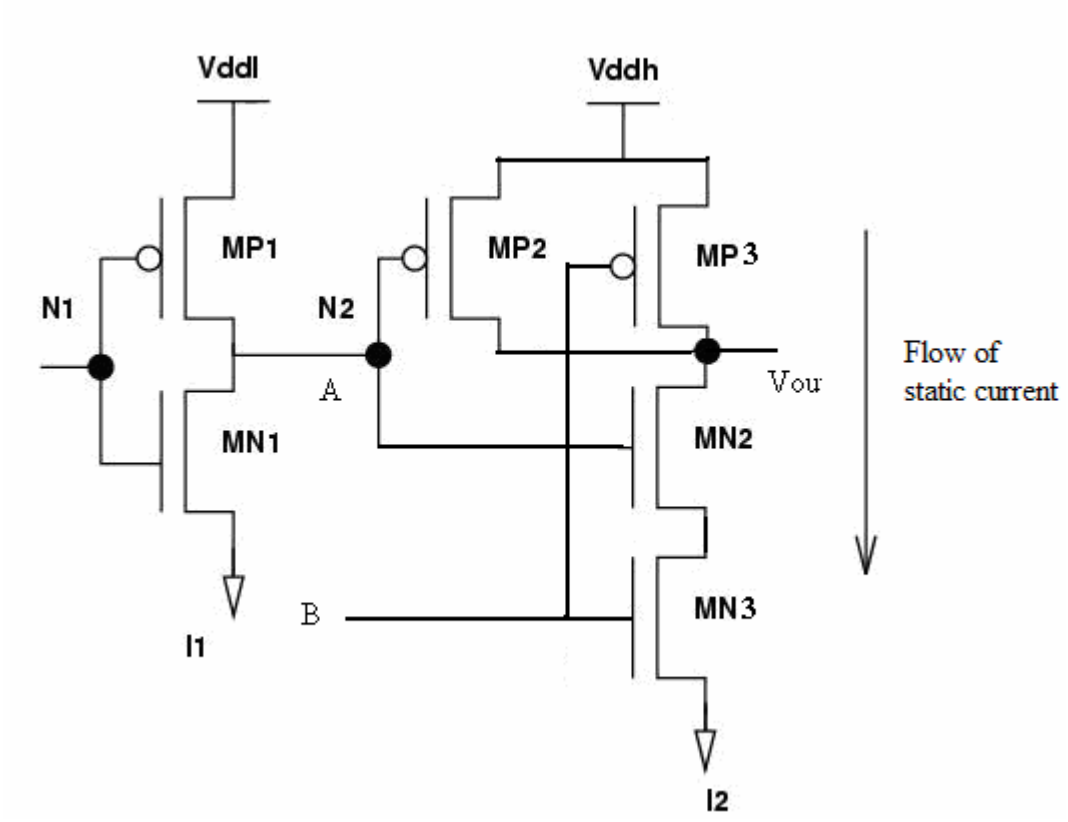

FIGURE 1.1 Direct connection between V_{DDL} and V_{DDH} circuits demonstrating the need for voltage level converter.

The level converters in literature can be basically categorized into two types: (i) level-up converters and (ii) level-down converters. In level up conversion the input voltage (V_{DDL}) is converted to a higher voltage level (V_{DDH}). On the other hand level down conversion the input voltage (V_{DDH}) is converted to a lower voltage level (V_{DDL}). From the system performance point of view, it is very important to decide where and what type of level converter should be inserted to achieve the required target specification. Algorithms like clustered voltage scaling (CVS) and extended clustered voltage scaling (ECVS) help such kind of decision making [Usami 1997]. In CVS, all the gate which are running at same voltage level are grouped together and the level

converter is only required at the interface between the two regions at different voltages [Kulkarni 1999]. On the other hand, ECVS technique is more flexible which allows insertion of level converter wherever it is required in the circuit [Usami 1997].

Designing a multi voltage system is a very complex procedure and also has a significant number of design constraints are involved. It is important to consider all the design constraints to build a highly efficient low power circuit. A level converter itself consumes power for its operation and hence needs to be accounted for. Thus, a proper tradeoff must be maintained between the number of level converters used and the target power savings [Ishihara 2004]. The other challenge involved in designing an efficient multi-voltage SoC is to minimize the cost of level conversion and maintain an efficient power distribution network [Ishihara 2004].

In this thesis, a unique level converter called universal level converter (ULC) for a dual voltage system is proposed. This level converter is capable of four types of operations such as: (i) level up conversion, (ii) level down conversion, (iii) blocking of signal and (iv) passing the signal. The details of the design implementation and simulation results of ULC are discussed in chapter 3, chapter 4 and chapter 6 respectively. The layout details are described in chapter 5. The future works for the design are discussed along with the conclusion at the end, in chapter 7.

CHAPTER 2

RELATED RESEARCH WORKS

Level converters are very important for multi-voltage supply systems. In the recent years, a lot of research has been going on which concentrate on the aspect of power reduction through multi-voltage system on chips (SoCs) and level converters. In this chapter, a review of the research work done in multi-voltage systems and level converters is presented. Section 2.1 shows various research work done for multi-voltage supply systems. Sections 2.2 and 2.3 discuss in brief various researches done in level up converters and level down converters.

2.1 Research in Multi Voltage Systems

The ever growing need for low power design for various day to day, especially for mobile applications has motivated the very large scale integration (VLSI) design engineers to study and work on various techniques for power reduction. As discussed in chapter 1, the most commonly used and, importantly, efficient method for power dissipation reduction, is by using a multi-voltage supply system which make use of level converters. The key to design a multiple voltage system is to divide the integrated circuit into regions working at different voltage levels. For designing such systems algorithms like clustered voltage scaling (CVS) are widely used. CVS methods allows synchronous level conversion which means that after dividing the integrated circuit into different regions or cells working at different voltages, level converters are inserted

only at the interface of two cells. Authors in [Usami 1997, Horowitz 2004] discuss in details about multi voltage supply systems and various algorithms followed for assignment of V_{DD} to cells. These algorithms mainly decide where and what type of level converters should be used in the circuit. In [Usami 1997], the authors have studied the CVS structure in detail and proposed a novel architecture called the extended CVS (ECVS) and they have also proposed a synthesis technique of the structure. This architecture allows inserting a level converter where ever there is a large slack between the gates. Slack is defined as the difference between the required time and the arrival time of the signal at the gate [Usami 1997]. The authors have proposed an in-house tool called power slimmer which controls the level converter insertion by synthesizing the ECVS structure from a gate-level mapped netlist. ECVS scheme allows asynchronous level conversion which allows inserting a level converter anywhere in the circuit. In [Horowitz 2004], the authors propose a technique where in it reduces the number of interface level converters leading to a clustered voltage scaling. In [Igarashi 2000], authors describe gate level power minimization using dual supply voltages. The concept that the authors have proposed is that all the gates and flip flops which are off the critical path are made to run at a reduced supply voltage to save power. This is done by performing static timing analysis for a given circuits with a single V_{DD} and extracting the gates which are not on the critical path and assigning V_{DDL} to them. In [Mohanty 2005] the authors have proposed various minimization methodologies for power reduction of an integrated circuit taking into consideration the design process

variations. The authors have created a unique power reduction model which can be easily integrated into behavioral tasks.

2.2 Research in Level Up Converter

While designing a multiple supply voltage system, it is essential to consider the overhead caused by the level converters [Roy 2002]. To reduce this overhead, generally multiple voltage systems implement pipeline flip flops along with level converters at the end of low V_{DD} clusters [Roy 2002]. The flip flops combined with level converters perform the operation of latching and level conversion at the same time. Such flip flops are called as a level converting flip flops. In [Ishihara 2004], key properties and design metrics of a level converter for dual- V_{DD} systems are examined. The authors have studied the traditional level converter circuits like cross coupled level converter (CCLC), single supply diode voltage limited buffer level converter (SSLC), pass transistor half latch (PHL) and pre-charged circuit. Several new level converting flip flop circuits called LCFFs are also proposed and these new designs are compared to the above mentioned traditional level converting circuits in terms of level converter performance and robustness as well as system level performance and robustness. The proposed level converting flip flops exhibit improved energy-delay product values, reduced system-level power and better immunity to supply noise without incurring significant layout are penalties.

In [Yu 2001], [Chin 2005], [Kulkarni 1999], and [Sadeghi 2006] the authors have studied a conventional level converter circuit known as dual cascode voltage

switch (DCVS). The DCVS circuit is a small circuit which consists of a PMOS pair connected back to back which act as a differential pair. Each of the above referenced papers proposes new level converter designs considering DCVS as a baseline design. In [Sadeghi 2006], authors propose a new level converter circuit based on the keeper transistor concept in pass transistor logic. The keeper transistor is used as a level restorer in the pass transistor logic [Bellaouar 1995]. Then the authors have compared the performance of the proposed circuit and the traditional DCVS by calculating the delay, power and energy-delay product. Five new asynchronous level converting circuit designs are proposed in [Kulkarni 1999]. The simulation results show that the proposed designs consume 8-50% less energy at equivalent or better speeds as compared to the other designs at 0.13um CMOS technology. A new level converter design has been presented in [Chien 2005]. The design is based on DCVS. In this paper the authors have compared the speed and power consumption of their level converter design and DCVS. In [Yu 2001], a new level converting circuit called symmetrical dual cascode switch (SDCVS) is proposed. The authors have addressed to the contention problem of DCVS and provided a solution for the same in this paper. The authors state that the contention problem will give rise to increased delay time and power consumption. Two additional NMOS are added to the DCVS design to eliminate the contention problem.

Two new logic level converter designs are presented in [Nam-Seog 2003]. The two designs are dynamic logic level converter (DLC) and dynamic logic level converter for duty ratio conversing (DDLC). These two designs are applied to a 72 Mb DDR SRAM which allow the chip to operate at a low voltage of 1.2V when the supply

voltages are around 1.5V or 1.8V. The DLC design consists of a self-resetting dynamic CMOS logic which makes it much faster in operation.

2.3 Research in Level Down Converters

In [Kanno 2000], a distinct level down converting circuit is proposed. This circuit consists of a differential input pair circuit acting as the level converting circuit. This level converter provides stable operation for low voltage and high speed use [Kanno 2000]. The circuits make use of thin gate oxide MOSFETS which enable a faster level conversion. The differential input pair of this level converter offers a high immunity against power supply bouncing.

Table 2.1 shows the different research works in level converters categorized on the basis of type of the level converter proposed, technology used for simulation, calculated power consumption values and the design approach followed.

TABLE 2.1 Table showing the research work in level converters.

Author name	Year	Techno-logy	Delay	Power Consumption μW	Type of Circuit	Design Converter approach
[Nam-Seog 2003]	2003	.001μm	< 120ps	-----	Level up	Dynamic Level
[Ishihara 2004]	2004	0.13μm	287 ps	10%	Level up	LCFF
[Kulkarni 1999]	1999	0.13μm	25%	7.3%	Level up	DCVS and Keeper transistor
[Yu 2001]	2001	0.35μm	60%	220.57	Level up	SDCVS
[Sadeghi 2006]	2006	0.1μm	----	----	Level up	Keeper transistor in pass transistor
[Kanno 2000]	2000	0.14μm	----	----	Level down	Differential input pair operation
[Chin 2005]	2005	0.18μm	----	----	Level up	(DCVS)

2.4 Research Contribution of this Thesis

The research work presented in this thesis contributes to the design implementation and characterization of a exclusive design of level converter called universal level converter (ULC). The design implementations done for this thesis include the schematic as well as the layout of the design.

This level converter is one of its kind because there have been either level up converter or level down converter proposed so far. The uniqueness of this design, which separates this design from the other designs, is that it is capable of four types of level converting operations on the input signal. These operations include (i) level up conversion, (ii) level down conversion, (iii) passing the signal and (iv) blocking the signal. Thus, ULC can be used for multi- V_{DD} based dynamic power reduction as well as power gating for power reduction. In this thesis work, various power and design constraints which are essential for low power designs are considered. The ULC design is optimized by performing various analyses. The analyses include power analysis, parametric analysis, and load analysis. With these analyses the power consumption of ULC under varying load conditions can be determined. Also it is proved that the design of universal level converter produces a stable output under low voltage conditions and varying loads. The schematic implementations and characterization of the design are made both at 90nm and 45nm technologies. The layout design is done for 90nm technology. The characterization, simulation results and layout design are also performed.

CHAPTER 3

TRANSISTOR LEVEL SCHEMATIC DESIGN OF UNIVERSAL LEVEL CONVERTER FOR 90nm TECHNOLOGY

3.1 Overall View of Universal Level Converter

Universal level converter (ULC) can be simply defined as a system which performs four distinct level converting operations on the input signal. These four operations include (i) level up conversion, (ii) level down conversion, (iii) passing of signal and (iv) blocking of signal. Level up conversion can be stated as conversion of a low voltage signal (V_{DDL}) to a higher voltage level (V_{DDH}). While in contrast, level down conversion can be defined as conversion of a higher voltage signal (V_{DDH}) into a low voltage (V_{DDL}). Passing of the signal indicate bypassing the signal to the other side of the network without doing any operation on the signal and blocking indicates completely stopping the input signal from appearing at the other side. The universal level converter can be programmed for all the above four mentioned functionalities depending on the type of requirement. The type of operation to be performed can be selected using the two control signals. Figure 3.1 shows a high level block diagram of the proposed ULC.

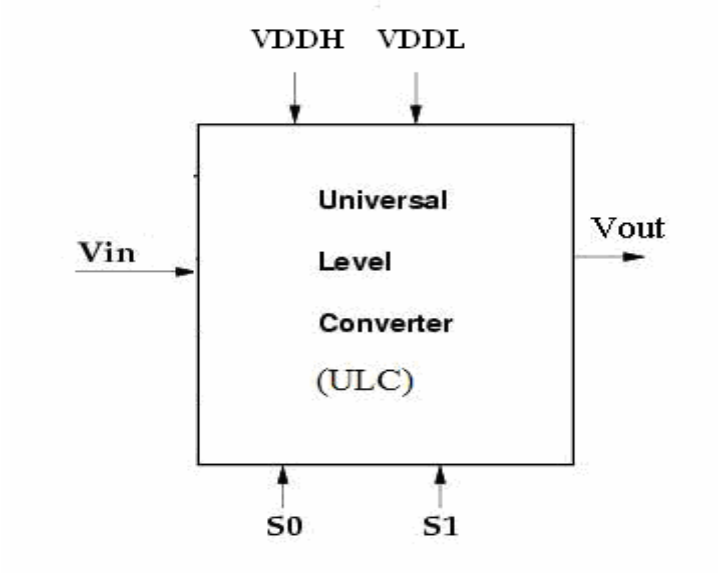

FIGURE 3.1 High level view of proposed universal level converter (ULC).

As shown in the diagram, ULC has in all five input pins and one output pin. The input signal is applied at pin *Vin* and output is taken across *Vout. s0* and *s1* are the pins for the control signals. The dual supply for ULC consists of V_{DDH} and V_{DDL}. The level converter employs four separate circuits that correspond to the above mentioned four distinct operations. Figure 3.2 shows the detailed view of the different blocks which constitute to the design of ULC. The *CCLC* block is used for level up conversion, while *DL* block is used for level down conversion. The passing and blocking functionality is achieved through the *pass circuit* and *block circuit*. The schematic details of these blocks are discussed shortly. The outputs from these four blocks are coupled to the output of ULC through a multiplexer. The two control signals s0 and s1 are used to select the preferred operation of ULC.

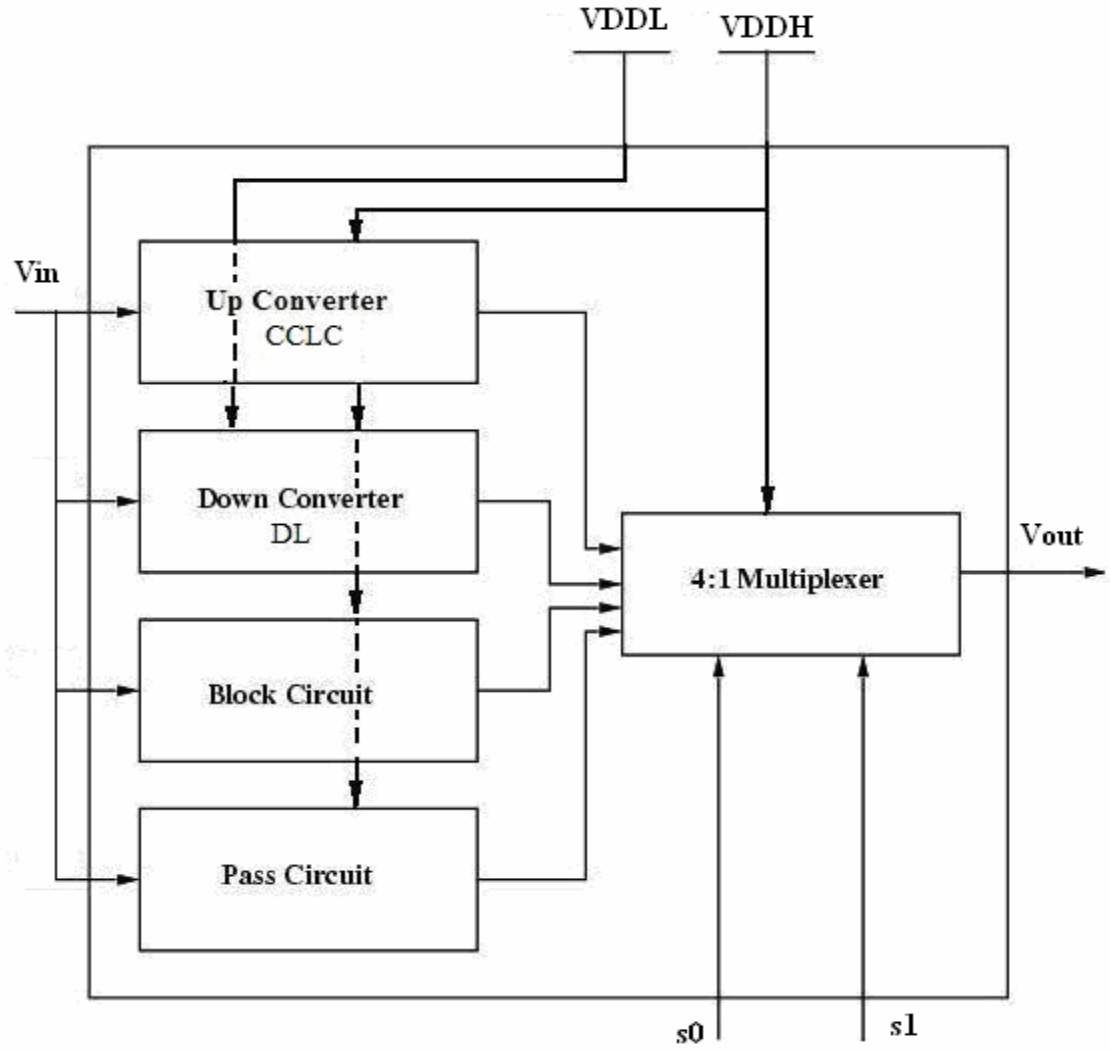

FIGURE 3.2 Detailed block diagram of universal level converter demonstrating its operational capabilities.

3.2 Schematic Details of Universal Level Converter

ULC employs four different blocks for the four distinct operations performed on the input signal. A wide variety of circuit topologies can be used for building level converting circuits. In this section the detailed description on type of circuits used for

level conversion and the working of ULC though various blocks of ULC with the help of detailed transistor level circuit diagrams of each block is given.

3.2.1 Level Up Converter

The level up converter is responsible for conversion of a signal at lower voltage (V_{DDL}) level to a higher voltage (V_{DDH}). This block makes use of cross coupled level converting (CCLC) circuit to achieve the up conversion functionality. The CCLC circuit is an asynchronous level converter, which means it can be inserted anywhere in the circuit wherever level conversion is necessary. Because of this flexibility, CCLC is one of the most commonly used designs to suppress the dc current [Ishihara 2004]. Figure 3.3 shows the transistor level circuit diagram of cross-coupled level converter.

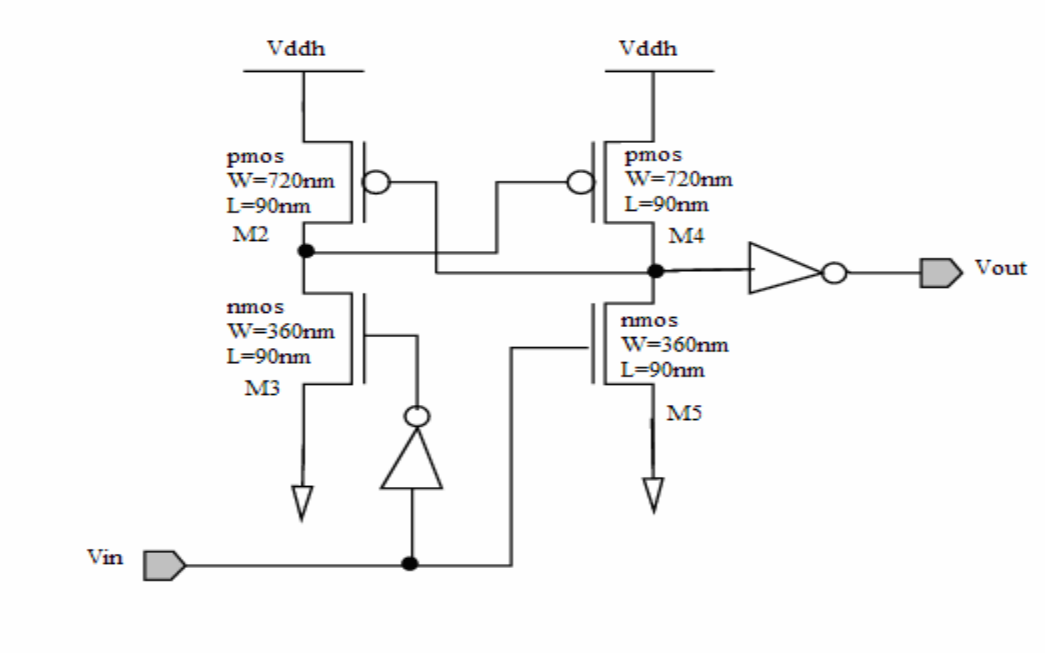

FIGURE 3.3 Transistor level circuit diagram of cross coupled level converter (CCLC).

As shown in the diagram, CCLC consists of two PMOS transistors connected in a back to back fashion. This cross-coupled PMOS pair acts as a differential pair. So, when the output at one side of the circuit goes low, the transistor on the opposite side is turned on and the voltage at the other side gets pulled up. To understand the working of the circuit let us assume that input voltage of the signal at Vin is low. Due to this transistor M5 is in cut off and M3 is switched on because of the inverter. This provides a direct connection to ground pulling N1 to ground. This will bias M4 and it will switch into conduction and a higher voltage is given at output.

The reverse process takes place when the input swings from low to high. When the input voltage at Vin is high, transistor M5 is in switched on and M3 is in cut-off. M5 provides a direct connection to ground pulling N2 to ground. And this will give a lower voltage at the output.

3.2.2 Level Down Converter

The level down converter is responsible for converting the high voltage (V_{DDH}) input signal to a lower voltage level (V_{DDL}). A differential pair level converter which acts as a level down converter circuit is used for achieving the functionality of level down conversion. Such type of level converter finds applications in high speed DSP chips [Kanno 2000]. The differential input pair down converter circuit is very efficient for high speed and low voltage devices. [Kanno 2000] It has high noise immunity against supply voltage bouncing [Sanchez 1999]. The high noise immunity for a level converter circuit is very helpful for low voltage designs because when V_{DD} is scaled

down according to the low power design requirement but while doing so, noise in the circuit is not considered [Kanno 2000]. This has impact on the output quality of overall system.

The circuit diagram for the differential input level down converter is shown in Fig. 3.4. The circuit runs at a dual voltage which consists of V_{DDH} and V_{DDL}. The circuit consists of a cross-coupled PMOS pair made up of M2 and M3, similar to the level up converter circuit. The lower voltage signal V_{DDL} is applied at inverter operating at V_{DDH}. The higher level of the signal is converter to a lower level at the output side.

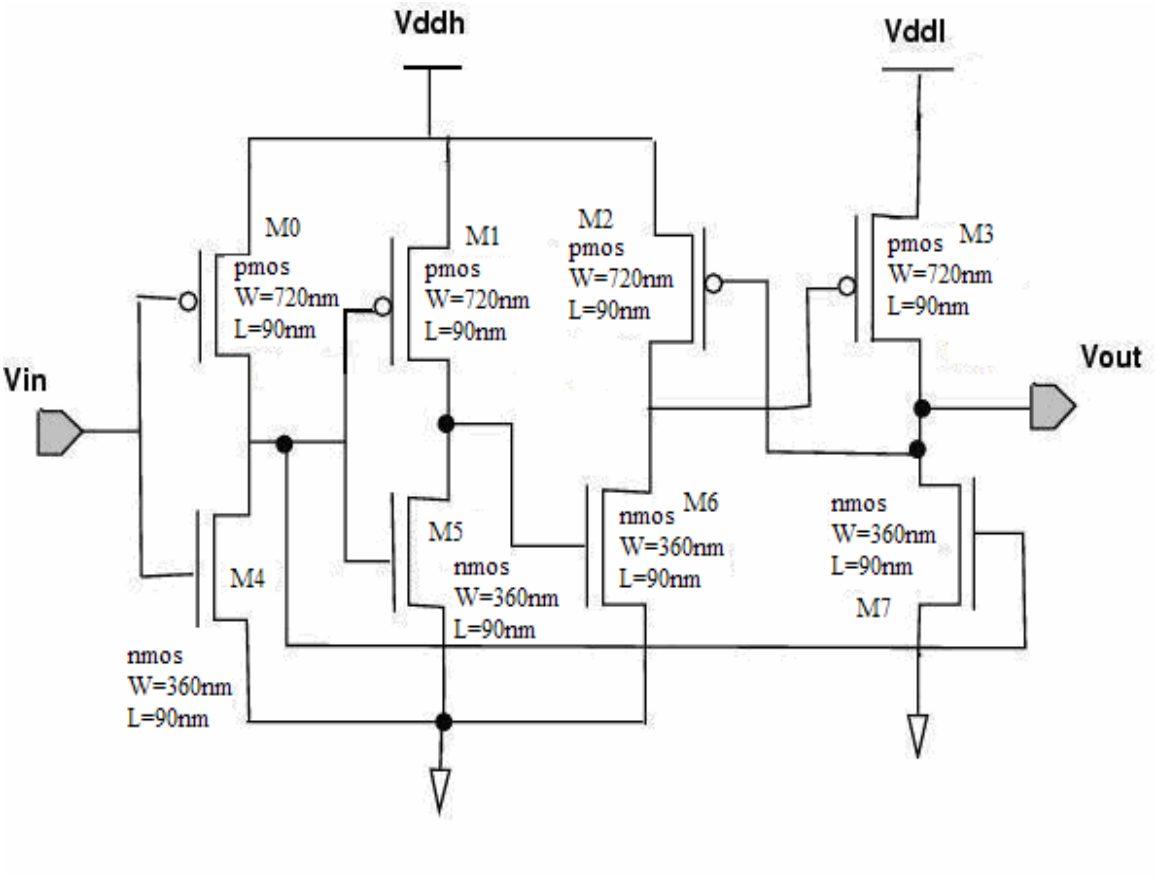

FIGURE 3.4 Transistor level circuit diagram of level down converter.

3.2.3 Blocking Circuit

The blocking circuit completely stops any kind of signal at the input side from appearing at the other side. This feature is very important in cases when total isolation from the input signal is required for reduction of standby leakage power. The blocking circuit is built by using a tri-state circuit which makes use of a transmission gate. The tri-state buffer circuits acts as a high impedance circuit when it is in "*not enabled*" mode. The state of high impedance can be defined as state of the output circuit which is not is driven by the circuit. The circuit diagram for the blocking circuit is shown in Fig. 3.5. As shown in the circuit diagram the blocking circuit employs a transmission gate and an inverter to achieve the functionality of blocking the signal. Table 3.1 shows the truth table for tri-state buffer circuit which shows that the circuit acts as a high impedance circuit when gb = 0 i.e. it is not enabled. Here *Z* indicates the high impedance state. This type of circuit is very handy when designing a data path or multiplexers.

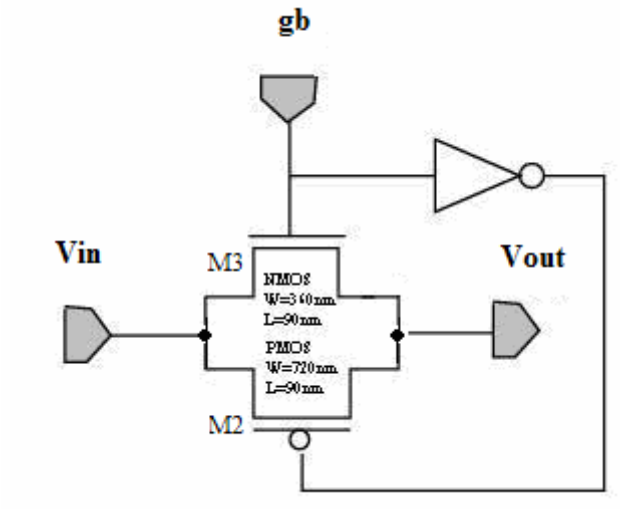

FIGURE 3.5 Transistor level circuit diagram of blocking circuit using a tri-state buffer.

TABLE 3.1 Truth table for the tri-state buffer circuit.

gb	Input	Output
0	0	Z
0	1	Z
1	0	0
1	1	0

3.2.4 Passing Circuit

The function of passing circuit is to bypass the input signal as it is to the other side of the circuit. In other words it acts as a buffer between the input and output. The passing circuit is designed with the use of a transmission gate. The circuit diagram of passing circuit is shown in Fig. 3.6. Transmission gates are specifically used to build the pass circuit because of its ability to pass strong 0 or strong 1. The circuit shown below acts as a pass circuit when the signal at g is high (1) and that at gb is low (0) passing a strong 1 to the output.

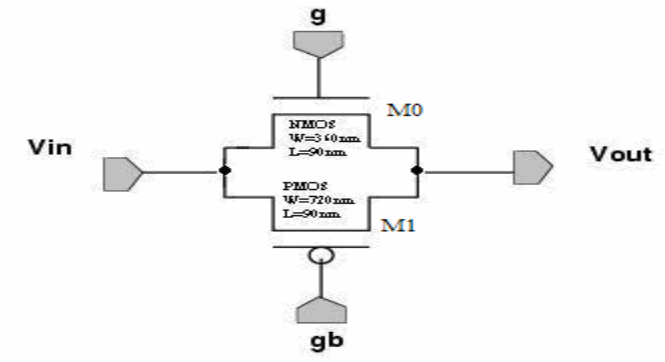

FIGURE 3.6 Transistor level circuit diagram of passing circuit.

3.2.4 4:1 Multiplexer

Multiplexer is a circuit which can couple several inputs to a single output. In other words, multiplexer acts as a multiple input, single output switch. As it is already discussed, the ULC design employs four individual circuits to obtain the level conversion functionalities. The circuits produce four independent outputs which constitute the ULC output. There has to be a means by which these four signals can be connected to the output terminal and any output signal can be observed at the output terminal according to the requirement. Thus, a 4:1 multiplexer circuit is used to couple the outputs of the four blocks to the output terminal of ULC. Taking into consideration the power consumption constraints for low power design, the multiplexer circuit is built by using transmission gates. Because the multiplexer circuit with transmission gates use lesser number of transistor as compared to the multiplexer circuit using gates. Consequently, lesser transistor will lead to lower power consumption.

Two 2:1 multiplexers, composed of transmission gates, are used to build a 4:1 multiplexer circuit. The circuit has two control signals s0 and s1 which decide the type of signal at the output terminal of ULC. Fig. 3.7 shows the high level block diagram of 4:1 multiplexer. The transistor level circuit diagram of 2:1 multiplexer using two transmission gates and two transistors is shown in Fig. 3.8.

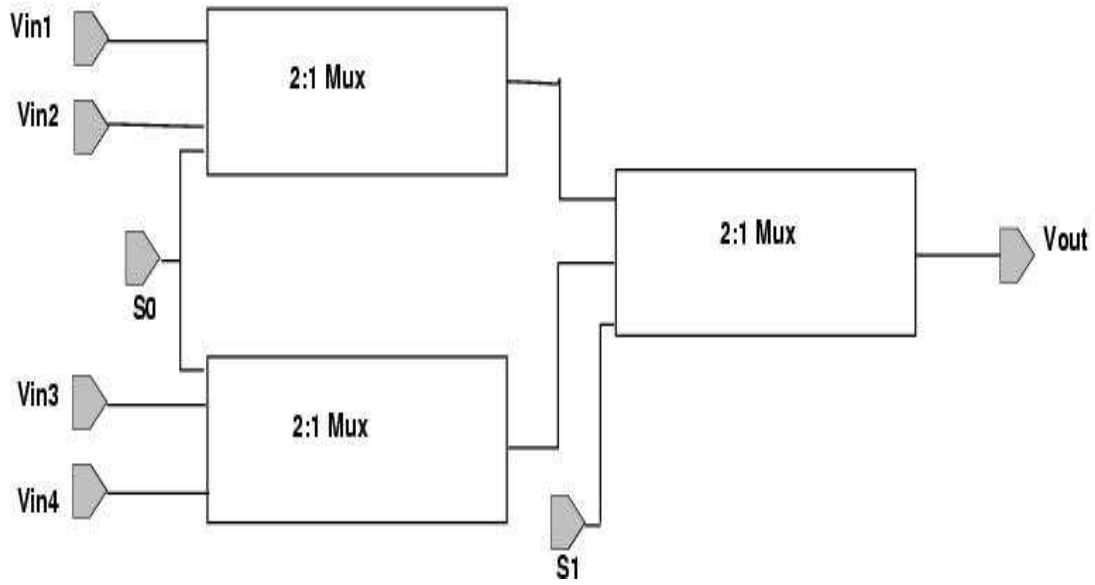

FIGURE 3.7 High level block diagram of 4:1 multiplexer.

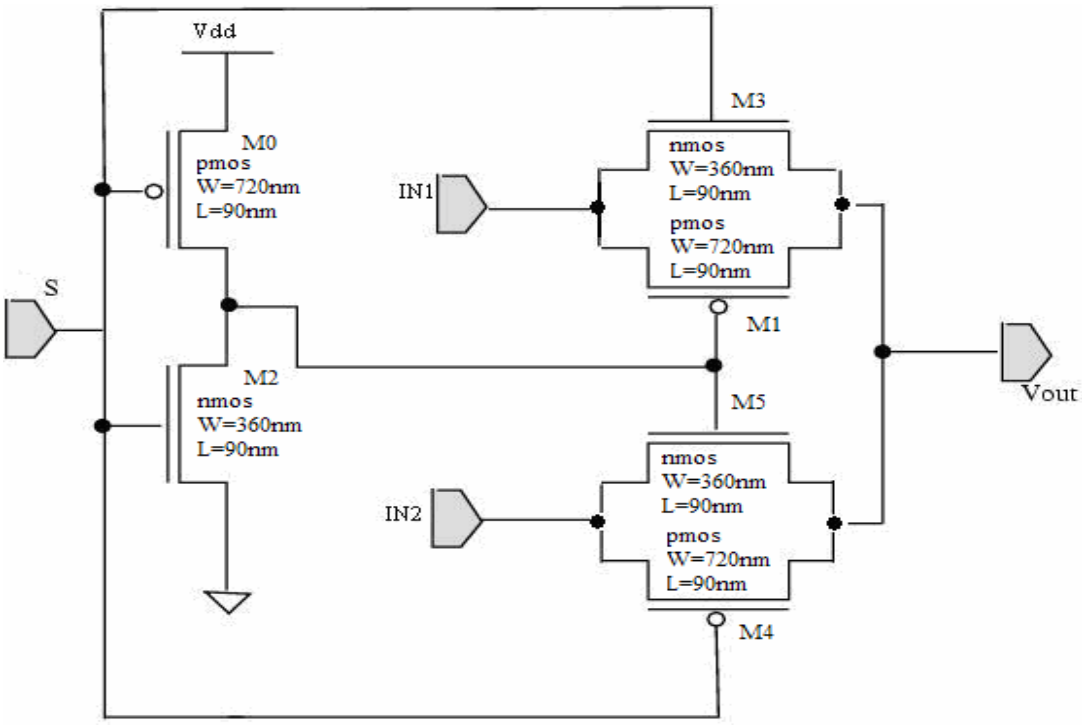

FIGURE 3.8 Transistor level circuit diagram of 2:1 multiplexer.

The input signal to the controls s0 and s1 play a very vital role in deciding the output of the universal level converter. Depending on the values of these control signals the multiplexer circuit couples one of its four inputs to the output. The Table 3.2 describes the type of output of ULC depending on the values of s0 and s1.

TABLE 3.2 Type of operation of ULC based on control signals s0 and s1.

Select Signal		Type of Operation
S0	S1	
0	0	Blocking operation
0	1	Passing operation
1	0	Level down conversion
1	1	Level up conversion

The transistor level diagram of universal level converter is as shown in the circuit diagram given in Fig. 3.9.

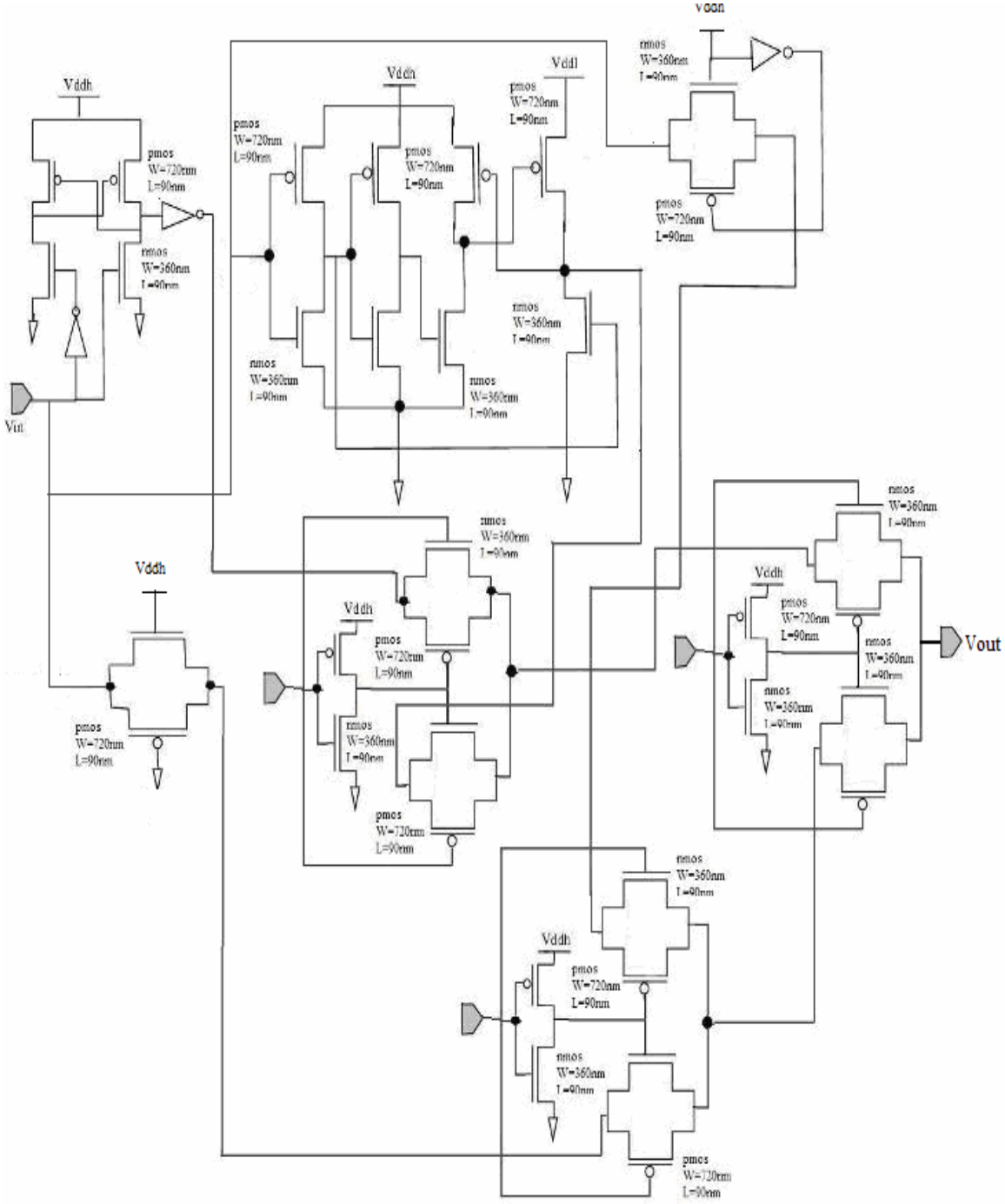

FIGURE 3.9 Transistor level circuit diagram of universal level converter at 90nm technology.

CHAPTER 4

CHARACTERIZATION AND SIMULATION RESULST OF ULC AT 90nm TECHNOLOGY

The detailed simulation procedure followed for verifying the results of universal level converter (ULC) in its various modes of operation are discussed in this chapter. In the later part of the chapter the three characterizations carried out on ULC are discussed.

4.1 Simulation of Universal Level Converter

Simulation of any design facilitates verification of overall system level operation. The schematic of universal level converter is built using the virtuoso schematic editor in Cadence and the circuit is simulated using Spectre simulator. All simulations are performed using the 90nm model files from predictive technology models (PTM). For schematic design, a W/L ratio of 4:1 is used, and the device parameters for PMOS are taken as W= 720nm and L = 90nm and for NMOS are W= 360nm and L = 90nm. The values of threshold voltages (V_{TH}) for PMOS and NMOS are -0.339V and 0.339V respectively. The values for the dual voltage supplies are used as V_{DDH} = 1.2V and V_{DDL} = 1.02 (85% V_{DDH}). The test bench for the simulation setup is shown in Fig 4.1.

As shown in the diagram, the dual voltage sources V_{DDH} and V_{DDL} are connected to pins V_{DDH} and V_{DDL}. The value of load capacitance used is 45fF. The pin *Vin*

represents the input pin where a piecewise voltage signal is applied as input. *s0* and *s1* are the control signal pins which decide the type of output of ULC.

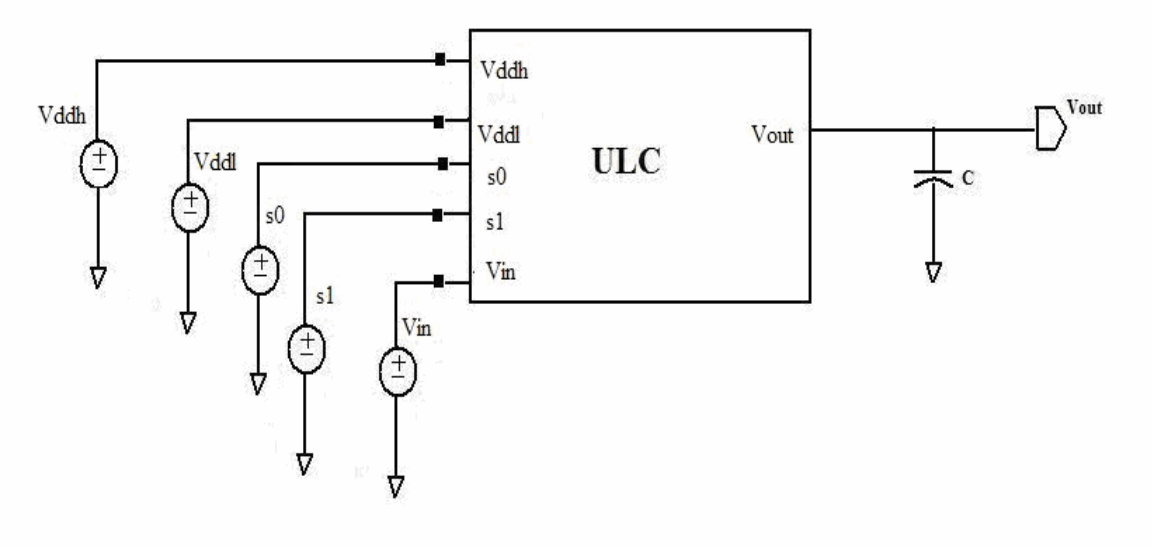

FIGURE 4.1 Simulation test bench for universal level converter.

The circuit is simulated in the *analog design environment (ADE)* using the *BPTM_90nm* technology model file. A transient analysis for 100nsec is performed during simulation and the output of ULC is observed in its different modes of operation as discussed Table 3.2. The Fig. 4.2 shows the output of the universal level converter in all of its four modes of operation. The universal level converter can also be used in a programmable logic mode where in the values of control signals s0 and s1 change according to a specific time duration or clock signal. Then depending on the current states of s0 and s1, the universal level converter will operate accordingly producing the output results for that specific s0 and s1 values and that period of time. The design is tested for its functionality for such programmable environment by running a simulation in which the states of s0 and s1 changes every 30nseonds and the universal level

converter is produces the desired output depending on the values of s0 and s1. This simulation results are shown in Fig. 4.3.

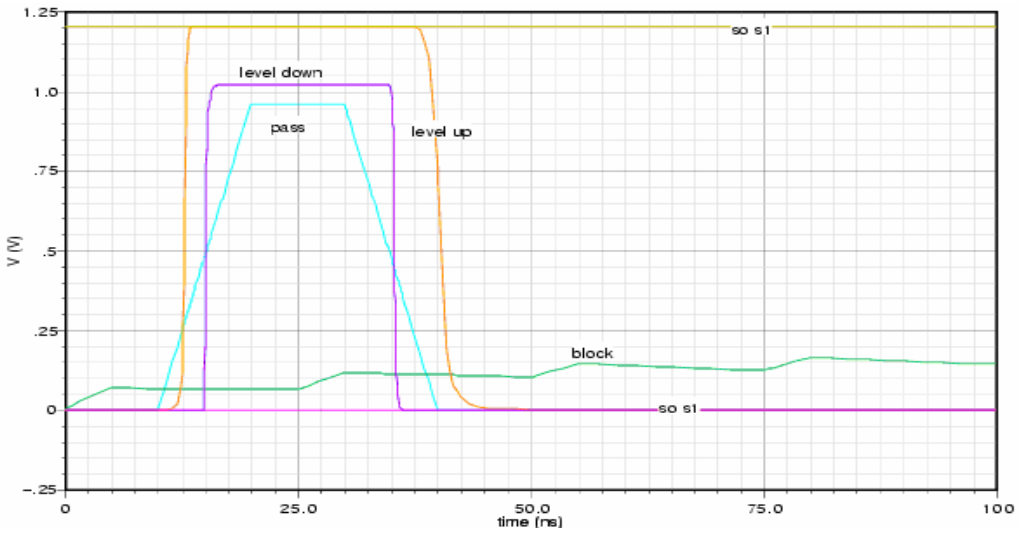

FIGURE 4.2 Simulation result of universal level converter showing the outputs for all the four modes of operation.

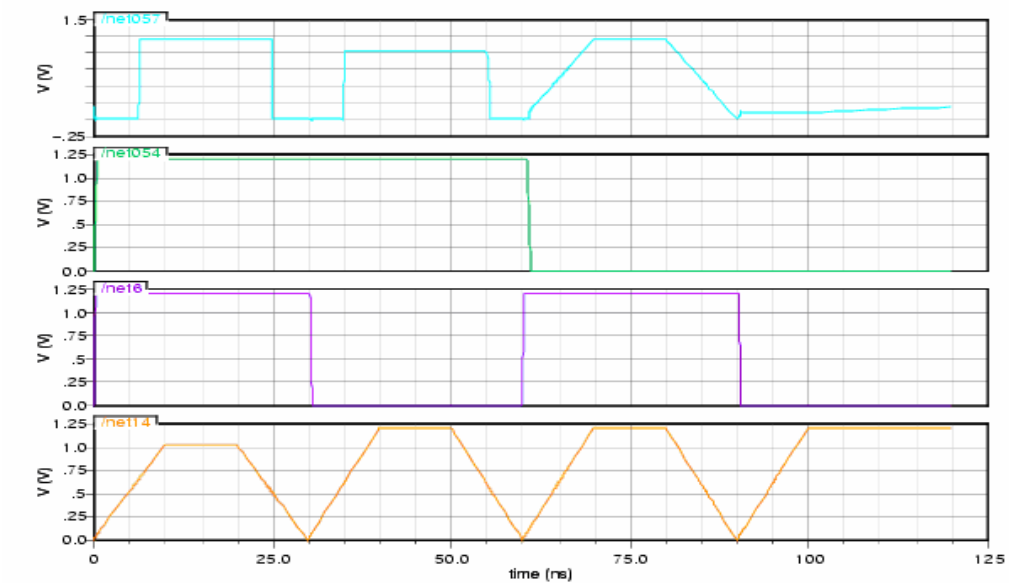

FIGURE 4.3 Simulation result of universal level converter showing the outputs for all the four modes of operation in a programmable design environment.

The output plots of Vout against Vin for level up converter, level down converter, blocking circuit and pass circuit individually are shown and discussed in sections 4.1.1 through section 4.1.4.

4.1.1 Level Up Converter

The level up converter is built using a cross coupled level converter and it is responsible for converting a lower voltage (V_{DDL}) signal at its input to a higher level (V_{DDH}) at the output. During simulation of ULC, a transient analysis for 100nsec is performed where both the control signals so and s1 are high. With these input states of the control signals, the output of the ULC is the output of the level up converter circuit. As shown in the output plot in Fig. 4.4 the input signal at pin *Vin* is a piece wise linear voltage signal at 1.02V. This signal at a lower voltage level is converted to a higher level of 1.2V by the level up converter circuit.

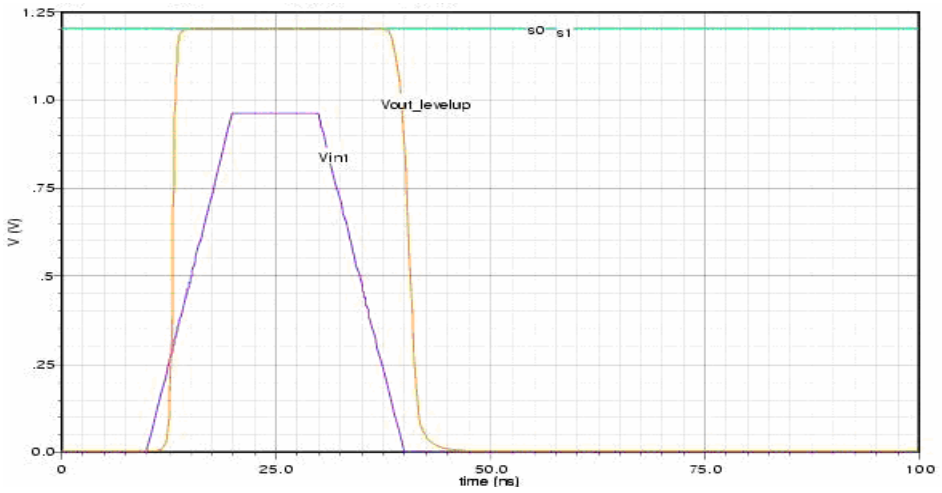

FIGURE 4.4 Output waveform for level-up conversion with V_{DDL} = 1.02V, V_{DDH} = 1.2V and load = 45fF.

4.1.2 Level Down Converter

The level down converter is made up of a circuit which employs a differential input pair for the level conversion. This circuit is responsible for converting a higher voltage (V_{DDH}) signal at its input to a lower level (V_{DDL}). During simulation of ULC, if s0 is maintained low and s1 is high then the output of ULC is the output of level down converting circuit. The input signal in this case is also a piecewise linear signal at a voltage of 1.2V (V_{DDH}). This signal is applied at *Vin* terminal of ULC. As shown in the output plot a transient analysis is carried out for 100nm where a piecewise linear input signal at 1.2V (V_{DDH}) is given and at output signal at 1.02v is observed.

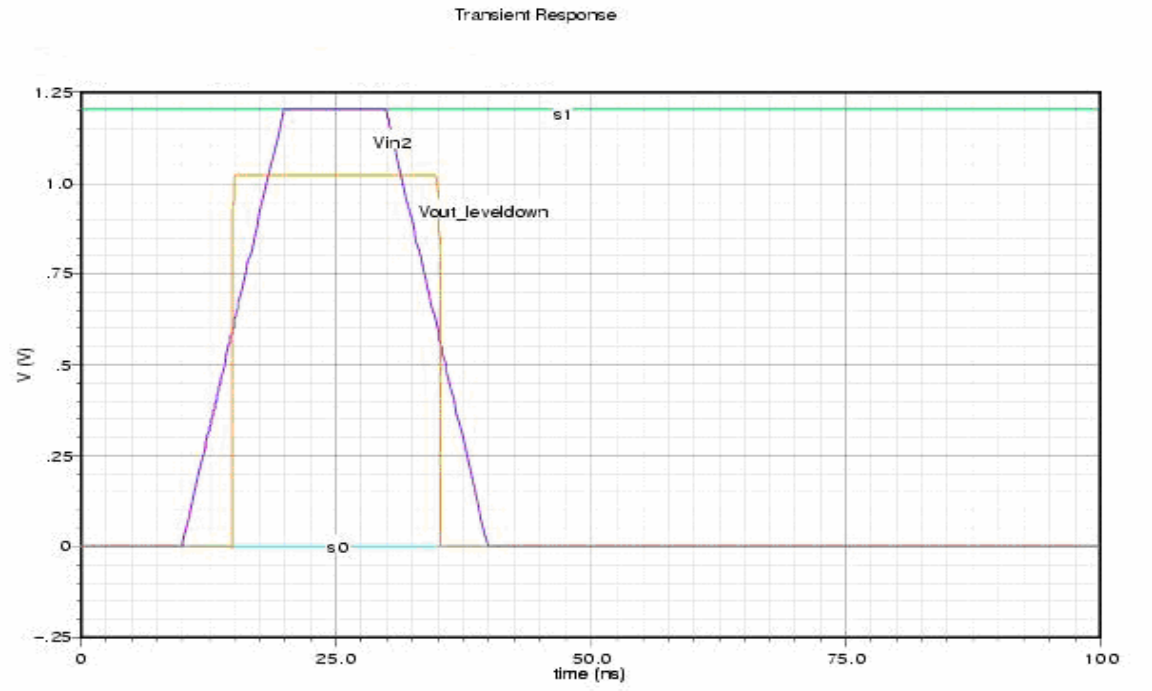

FIGURE 4.5 Output waveform for level-down conversion with V_{DDH} = 1.02V, V_{DDL} = 1.2V and load = 45fF.

4.1.3 Blocking of Signal Operation

When s0 is low and s1 is also low then ULC acts as a blocking circuit. The blocking circuit is a circuit which blocks the input signal completely from appearing at the other side of the circuit. In other word, the blocking circuit completely isolates its input side and the output side. Irrespective of the input signal a substantial output signal is not obtained. For verifying the working of this circuit a transient analysis for 1µsec is carried out with an input of pulse voltages given at pin *Vin*. The output is shown in Fig. 4. From the output it is evident that even when the input is as high as 1.2V the output voltage is very low below 0.36V which is less than the threshold voltage of PMOS and NMOS which is used in the design. For this output a transient analysis for 1µsec is performed to ensure that the circuit blocks the signal over an entire length of a longer input voltage signal.

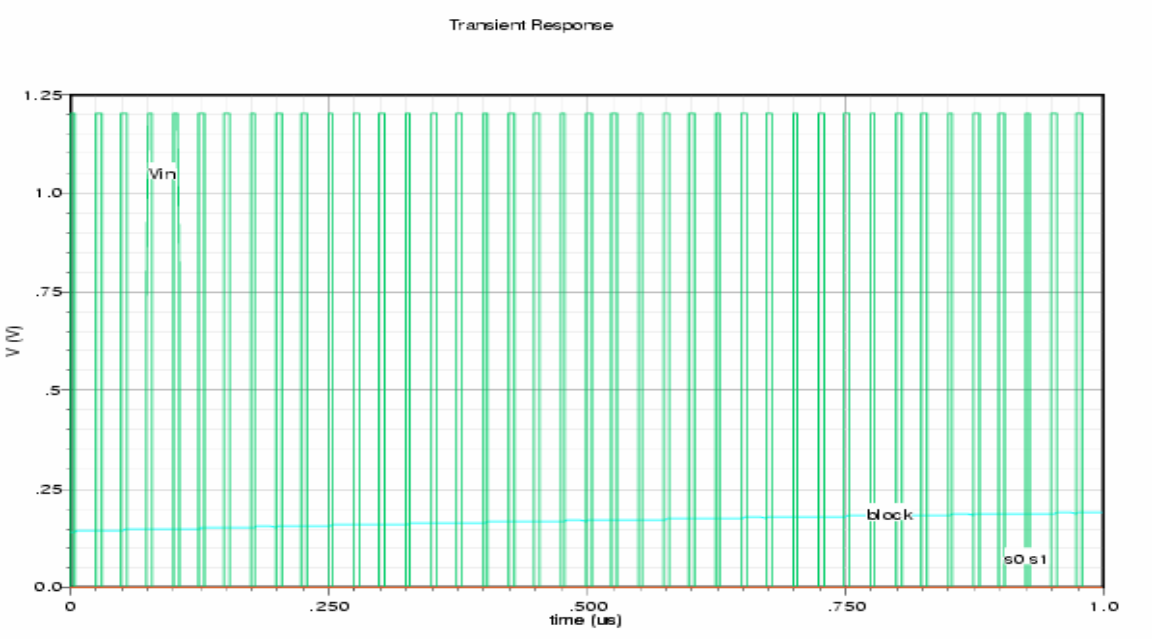

FIGURE 4.6 Output waveform of blocking of signal operation.

4.1.4 Passing of Signal Operation

Passing of signal indicate bypassing the input signal to output as it is. ULC can be made to work as a passing circuit when control signal s1 is low and s0 is high. In this mode of operation of ULC, whatever input signal is applied at pin *Vin*, it is passed to as it is to the output side without doing any operation on the signal. In other words, this circuit acts as a simple buffer circuit. This is shown in the plot given in Fig. 4.7. As shown an input signal at 1.2V is applied which is bypassed to output as it is.

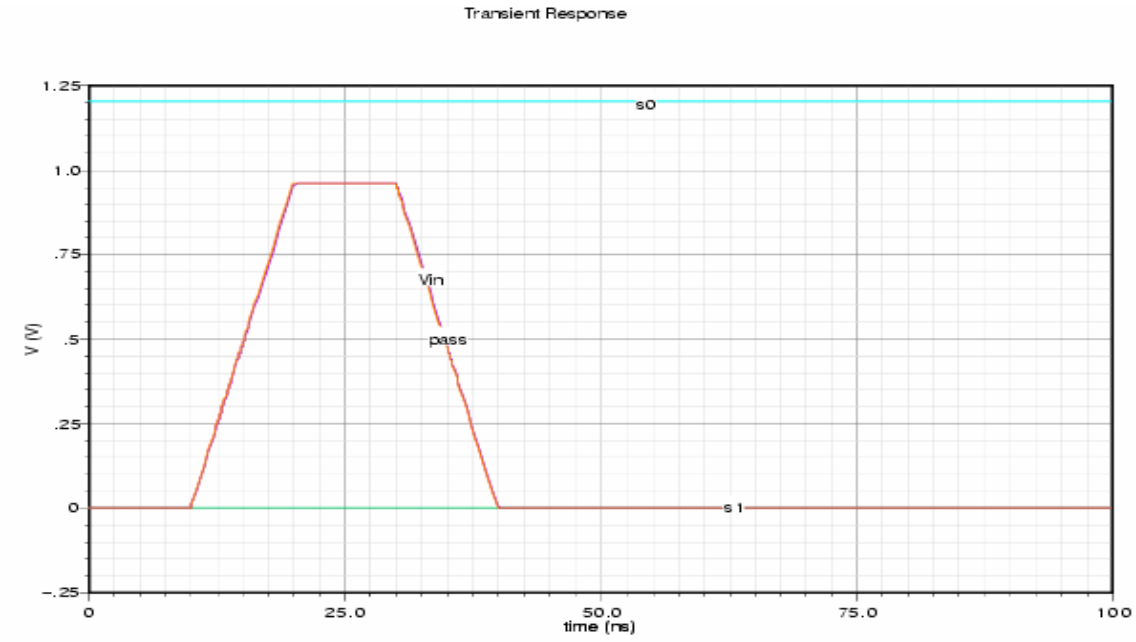

FIGURE 4.7 Output waveform of passing of signal operation.

4.2 Characterization of Universal Level Converter

In low-power circuit designs, it is of paramount importance to consider various design constraints concerning power consumption, lower voltage level and load it can drive and many more. Our design of universal level converter mainly focuses on low

power multi-voltage circuits applications. Thus, it is very essential to consider these design limitations. Keeping in mind these design constraints and to make sure that the universal level converter design is essentially a low power consuming circuit in itself, the ULC circuit is studied and analyzed under various input conditions. And the circuit is characterized by performing following three analyses:

(i) Parametric analysis,

(ii) power analysis , and

(iii) load analysis.

These characterizations are discussed in the following subsections.

4.2.1 Parametric Analysis

Parametric analysis is a process in which the circuit behavior is observed while continuously changing one of its input parameters. The *parametric analysis tool* from the *analog design environment* is used for performing this analysis. In this type of analysis, a transient analysis is carried where in the output voltage is observed for a varying input voltage. For this analysis the value of V_{DDH} voltage is kept at a constant level which is 1.2V and the voltage at V_{DDL} is varied from 0.1V to 1.02V with an increasing step of 0.102V. The value of control signals s0 and s1 are both kept high to achieve the level up conversion functionality. The output signal is observed at the output terminal *Vout* of ULC. The plot for the parametric analysis for up conversion is shown in Fig. 4.8 which confirms that the circuit produces a stable output even for voltage V_{DDL} l as low as 0.6V.

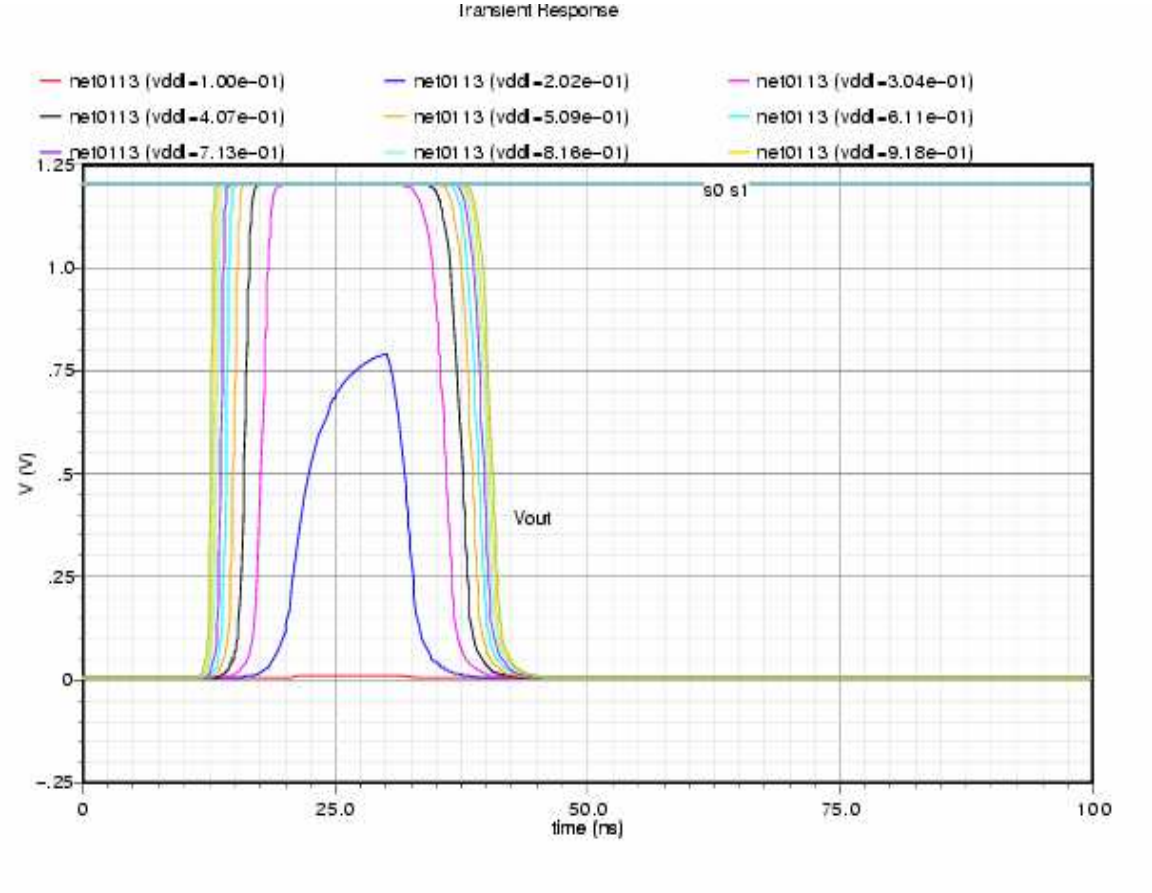

FIGURE 4.8 Parametric analysis for up-converter circuit showing the output (Vout) waveforms when the V_{DDL} is varied from 0.1V to 1.02V with an increasing step of 0.1V and constant V_{DDH} = 1.2V.

The same steps are followed for level down converter parametric analysis. The values for the control signal are kept at s0 as low (0V) and s1 as high (1.2V). In this case also V_{DDH} is kept at a constant higher voltage and V_{DDL} is varied from 0.1V to 1.02V with an increasing step size of 0.102V. The output plot for the down converter parametric analysis is shown in Fig. 4.9. From the plot it can be determined that the down converter circuit can produce a stable output even for Vddl as low as 0.73V.

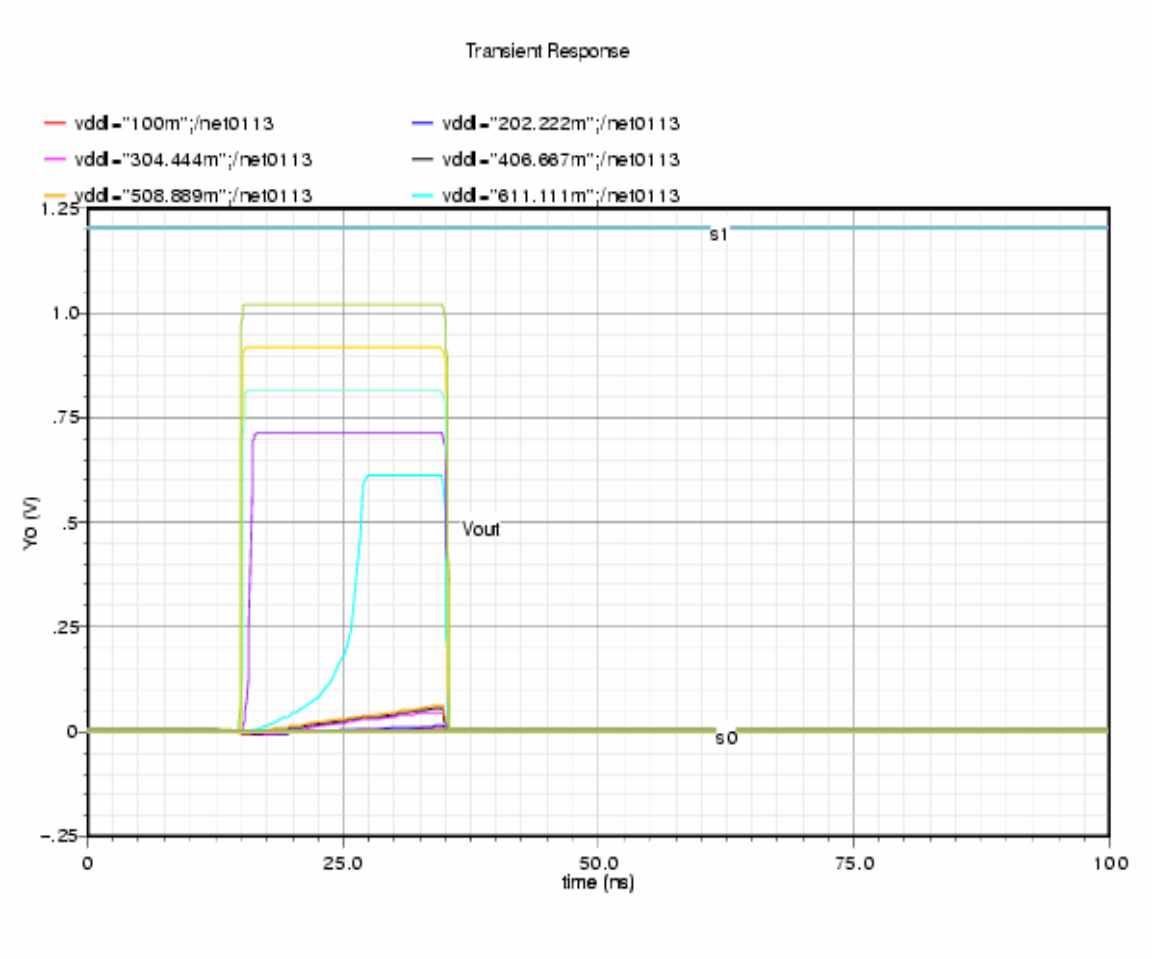

FIGURE 4.9 Parametric analysis for down-converter circuit showing the output (Vout) waveforms when the V_{DDL} is varied from 0.1V to 1.02V with an increasing step of 0.1V and constant V_{DDH} = 1.2V.

The parametric simulation results for the pass circuit are shown in Fig. 4.10. For simulation the same steps described above are followed. But in this case to achieve the functionality of blocking signal s0 is high and s1 is kept low. The value of V_{DDL} is varied from 0.1V to 1.02V with an increasing step of 0.2V. The results show that the pass circuit

is able exactly represent the input voltage at its output even for a lower voltages 0.25V.

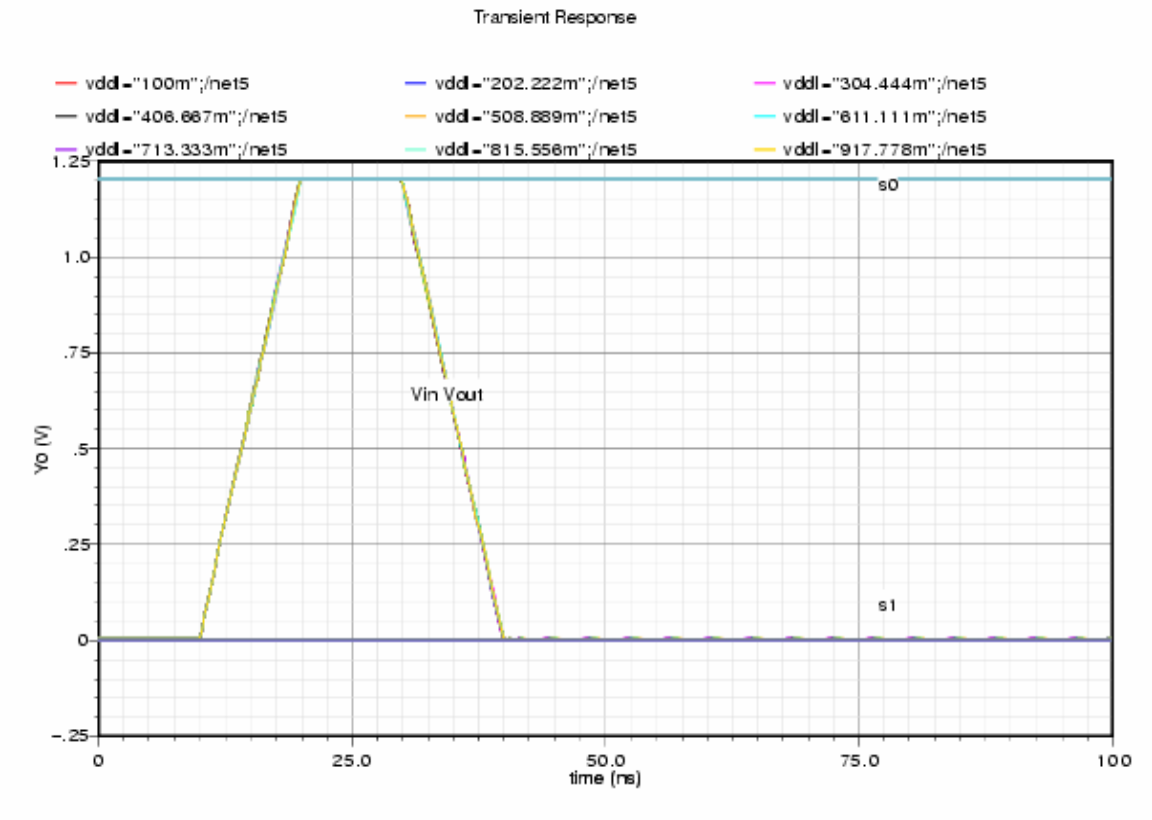

FIGURE 4.10 Parametric analysis for pass circuit showing the output (Vout) waveforms when the V_{DDL} is varied from 0.1V to 1.02V with an increasing step of 0.2V and constant V_{DDH} = 1.2V.

Looking at these plots it can be proved that ULC gives a stable output for the supply voltage as low as 0.6V which is a desirable property for a low power design.

4.2.2 Power Analysis

Power analysis includes determining the total power consumed by the overall universal level converter circuit. The total power consumed by individual blocks which make up the universal level converter is also calculated during power analysis. Power

analysis is be done by using the *browser* and *calculator* tools of analog design environment during simulation of the circuit. The total power of the universal level converter is the sum of the power consumed by each of the five blocks of ULC and it can be calculated using the following formula:

$$P_{ulc} = P_{cclc} + P_{dl} + P_{block} + P_{pass}. \qquad [2]$$

During the power analysis, the total power consumed by ULC at three different loads is calculated. This is shown in Table 4.1. These calculations show that the average power consumed by ULC is 27.534μW. From the power analysis it can be concluded that the proposed design of universal level converter consumes very less power as compared to the other level converters at other technologies. This comparison shows a total of 87.2% of power consumption reduction at a 90nm technology from those of other level converters at a greater technology.

The tables from Table 4.2 through Table 4.7 shows the detailed power consumption of the individual level converting blocks of ULC, including the power consumed by each transistor.

TABLE 4.1 Table showing the average power consumed by the universal level converter under three different capacitive load conditions.

Load	Circuit	Power Consumption (μW)	Total Average Power Consumption (μW)
10fF	Level-UP Converter	16.10	26.928
	Level-Down Converter	10.575	
	4:1 Mux	0.22426	
	Block Circuit	0.026244	
	Pass Circuit	0.002242	
45fF	Level-UP Converter	16.2702	27.4801
	Level-Down Converter	10.50702	
	4:1 Mux	0.613143	
	Block Circuit	0.024201	
	Pass Circuit	0.00256	
90fF	Level-UP Converter	16.477	28.1982
	Level-Down Converter	10.5725	
	4:1 Mux	1.12139	
	Block Circuit	0.0262963	
	Pass Circuit	0.002489	

TABLE 4.2 Power consumption of level up converter.

Sub circuit	Transistor	Type	Average Power
Inverter	M0	PMOS	4.933 μW
	M1	NMOS	3.525 μW
--	M2	PMOS	0.4029 μW
--	M3	NMOS	0.574 μW
--	M4	PMOS	4.087 μW
--	M5	NMOS	1.084 μW
Total average power		16.477 μW	

TABLE 4.3 Power consumption of 4:1 multiplexer circuit.

Transistor	Type	Average Power
M0	PMOS	0.0302 μW
M1	PMOS	0.220 μW
M2	NMOS	0.00022 μW
M3	NMOS	0.299 μW
M4	PMOS	0.00017μW
M5	NMOS	0.00003 μW
Total average power		1.121 μW

TABLE 4.4 Power consumption of level down converter circuit.

Transistor	Type	Average Power
M0	PMOS	4.058 μW
M1	PMOS	0.6784 μW
M2	PMOS	0.711 μW
M3	PMOS	0.0695 μW
M4	NMOS	2.990 μW
M5	NMOS	0.447 μW
M6	NMOS	0.3229 μW
M7	NMOS	0.285 μW
Total average power		10.572 μW

TABLE 4.5 Power consumption of pass circuit.

Transistor	Type	Average Power
M0	PMOS	0.124 nW
M1	NMOS	0.117 nW
Total average power		0.242 nW

TABLE 4.6 Power consumption of blocking circuit.

Sub circuit	Transistor	Type	Average Power
Inverter	M0	PMOS	0.000097 μW
	M1	NMOS	0.019 μW
--	M2	PMOS	0.006 μW
--	M3	NMOS	0.0005 μW
Total average power		0.02 μW	

4.2.3 Load Analysis

Load analysis is a very important category of analysis for any electrical system design. Load analysis helps the designer in understanding the transient behavior of a system at different loads which mainly helps in verifying the overall system functionality.

The universal level converter is used as an interface between two circuits (or gates) operating at different voltage levels. There might be many chances when the output load of the level converting circuit is changing quiet often. Thus it is of great importance that it should be made sure that the design of ULC produces the desired results even under such varying load conditions. Therefore a load analysis on ULC is performed where the output load capacitance of the circuit is varied and the effect of that on the output signal is observed. During the load analysis of the universal level converter the output of the circuit by varying the capacitive load at the output from 1fF to 200fF is studied. From this analysis it can be concluded that ULC produces a stable output under varying load conditions. This is again an important design feature for voltage level

converters. The Fig 4.10, Fig. 4.11 and Fig. 4.12 show the output plot for load analysis on level up converter, level down converter and pass circuits.

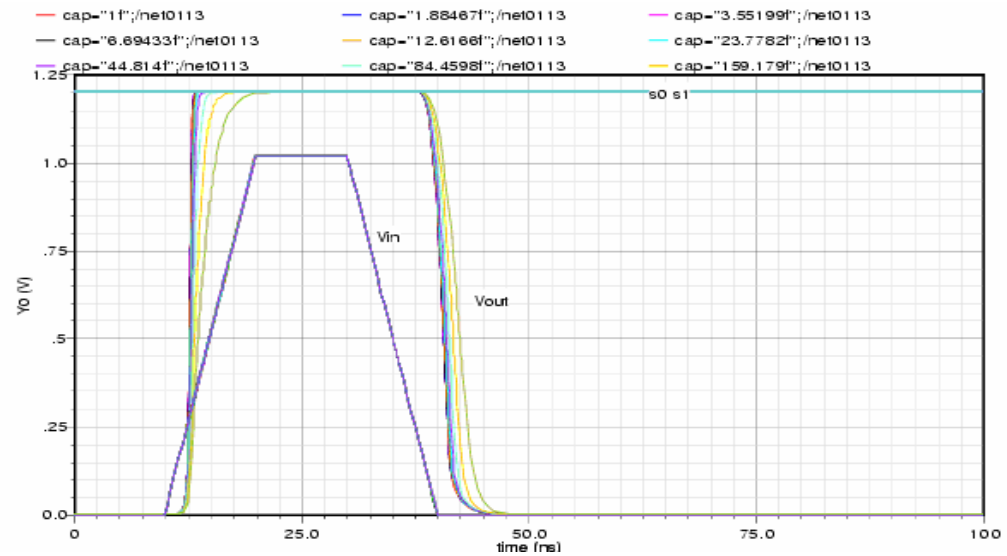

FIGURE 4.10 Output for level up conversion under different load conditions with load varying from 10fF to 200fF.

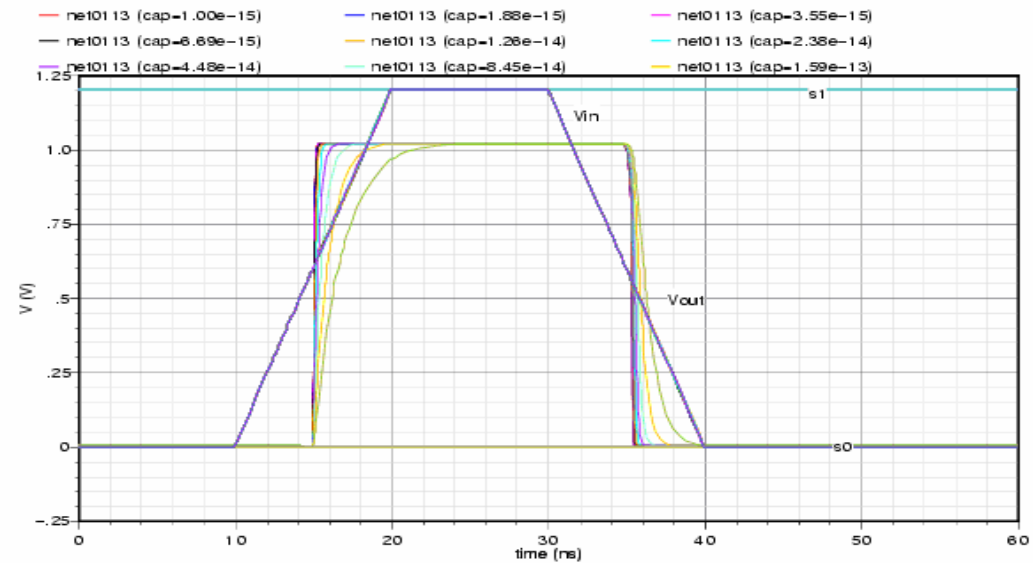

FIGURE 4.11 Output for level down conversion under different load conditions with load varying from 10fF to 200fF.

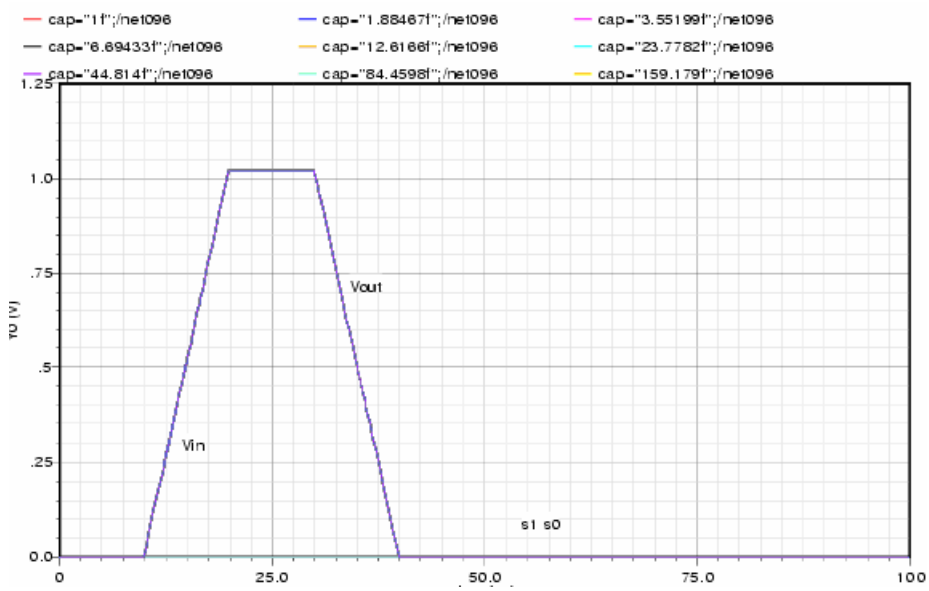

FIGURE 4.12 Output for level down conversion under different load conditions with load varying from 10fF to 200fF.

CHAPTER 5

CUSTOM LAYOUT DESIGN OF UNIVERSAL LEVEL CONVERTER AT 90nm TECHNOLOGY

Next step in the standard design flow of any integrated circuit, after schematic implementation, is creating the layout of the schematic. Layout creation is followed my parasitic extraction, several design optimization and finally fabrication of the integrated circuit. In this thesis, a layout has been created for the design after testing and analyzing the universal level converter circuit. A layout describes the various layers using which the integrated circuit can be fabricated while manufacturing. The layers in a layout describe the physical characteristics of the device. In full custom design all the layers of the design are drawn by the designer manually taking care about all the design rules. On the other hand, in automated design by instantiating the standard cells [Tutorial 1]. The layout of universal level converter has been designed using Cadence virtuoso layout design tool.

All the layout designs use the standard process design kit *(PDK)* for 90nm technology from cadence called *gpdk_90nm (generic process design kit)* downloaded from the Cadence foundry solutions. A PDK is a complete set of technology files that enable custom IC circuit design within cadence custom IC design environment [Tutorial 1]. All the layouts of ULC and the different blocks of ULC are created at a 90nm technology. A W:L ratio of 2:1 is used for PMOS and NMOS where the device parameters for PMOS are W= 1um, L = 100nm and that of NMOS are W = 500nm and L = 100nm. The designs are verified by using the Assura design rule file *assuraDRC.rul*

and *divaDRC.rul* in DRC check. The layout designs of ULC and the blocks are discussed in the following sections.

5.1 Layout Design of Level Up Converter

The layout for the cross coupled level up converter is shown in Fig 5.1. It has a total of 6 transistors and it has one output and one input. The inputs and the outputs are shown by the *Vin* and *Vout* rails. V_{DD} represents the voltage supply rail for the level converter.

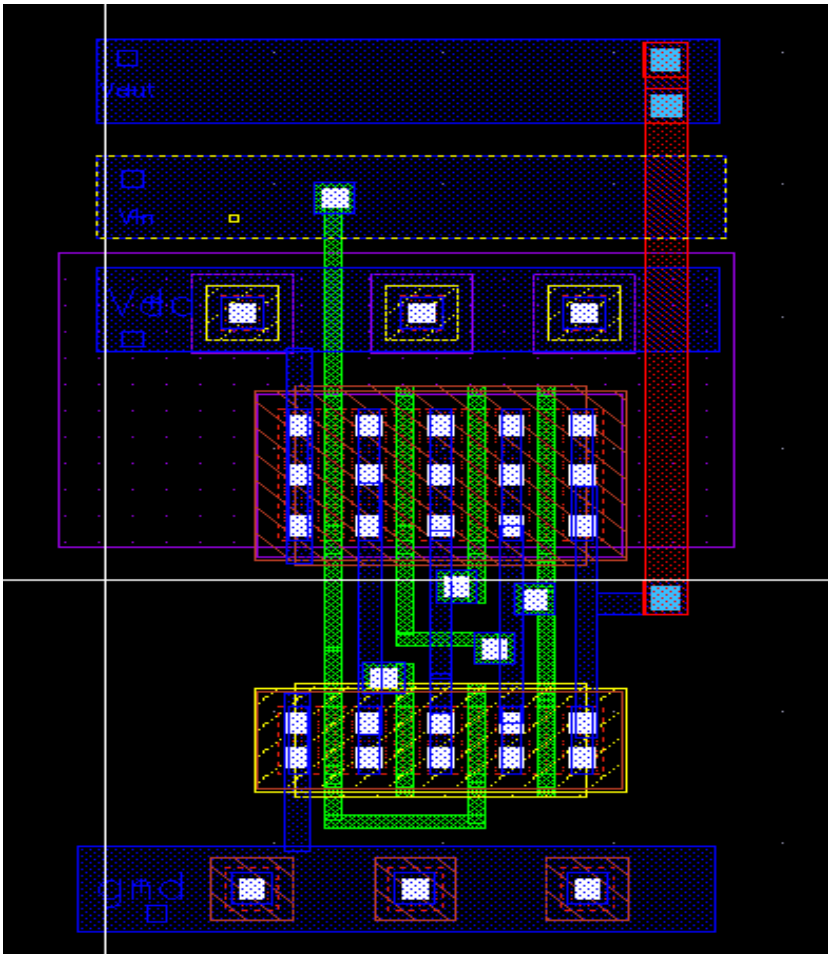

FIGURE 5.1 Layout design of cross coupled level up converter circuit.

5.2 Layout Design for Level Down Converter

The layout for the level down converter circuit is shown in Fig. 5.1. The level - down converter circuit has two voltage supply rails V_{DDH} and V_{DDL}. The input is connected to the *Vin* rail and output to the *Vout* rail.

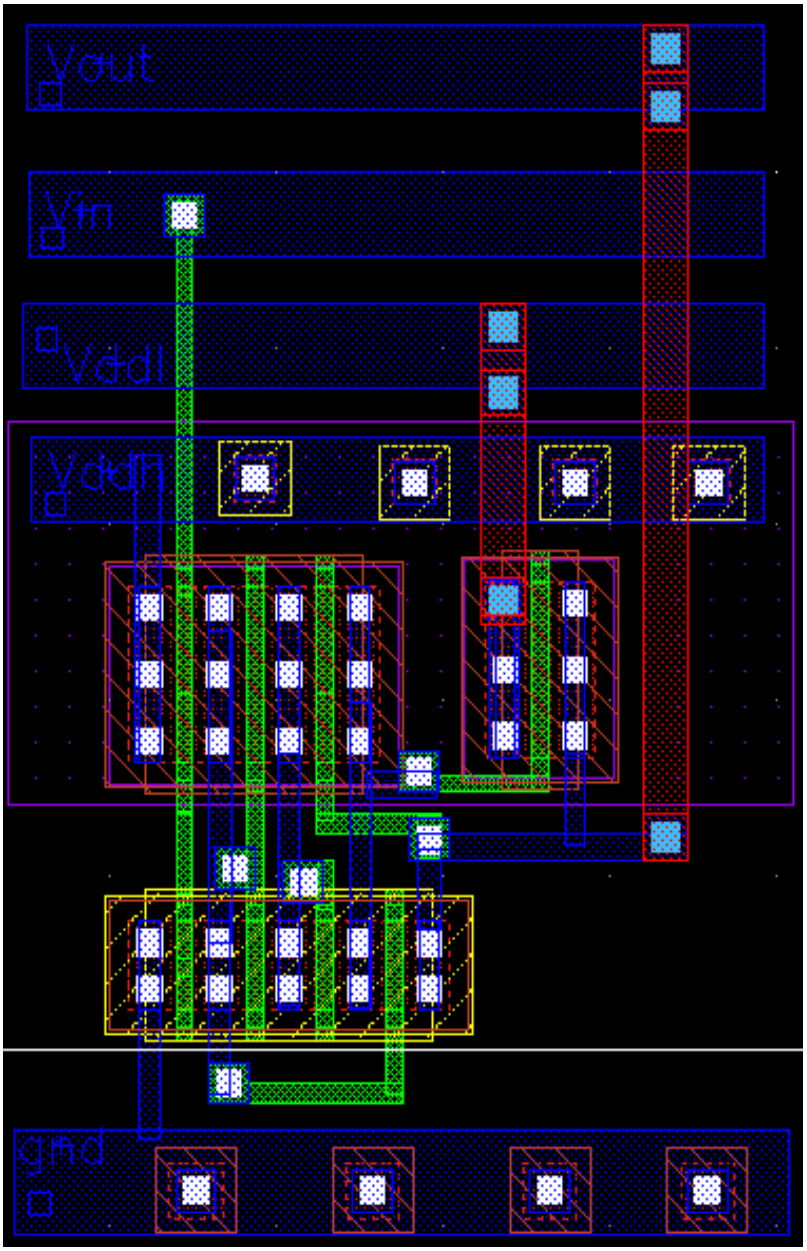

FIGURE 5.2 Layout for level down converter circuit.

5.3 Layout Design of Blocking Circuit

The layout for the level down converter circuit is shown in Fig. 5.3. The blocking circuit consists of an inverter and a transmission gates. The inverter is shown of the right side part of the design and on the left is the transmission gate. The inputs, output and voltage supply are connected Vin, Vout, and the Vdd rails.

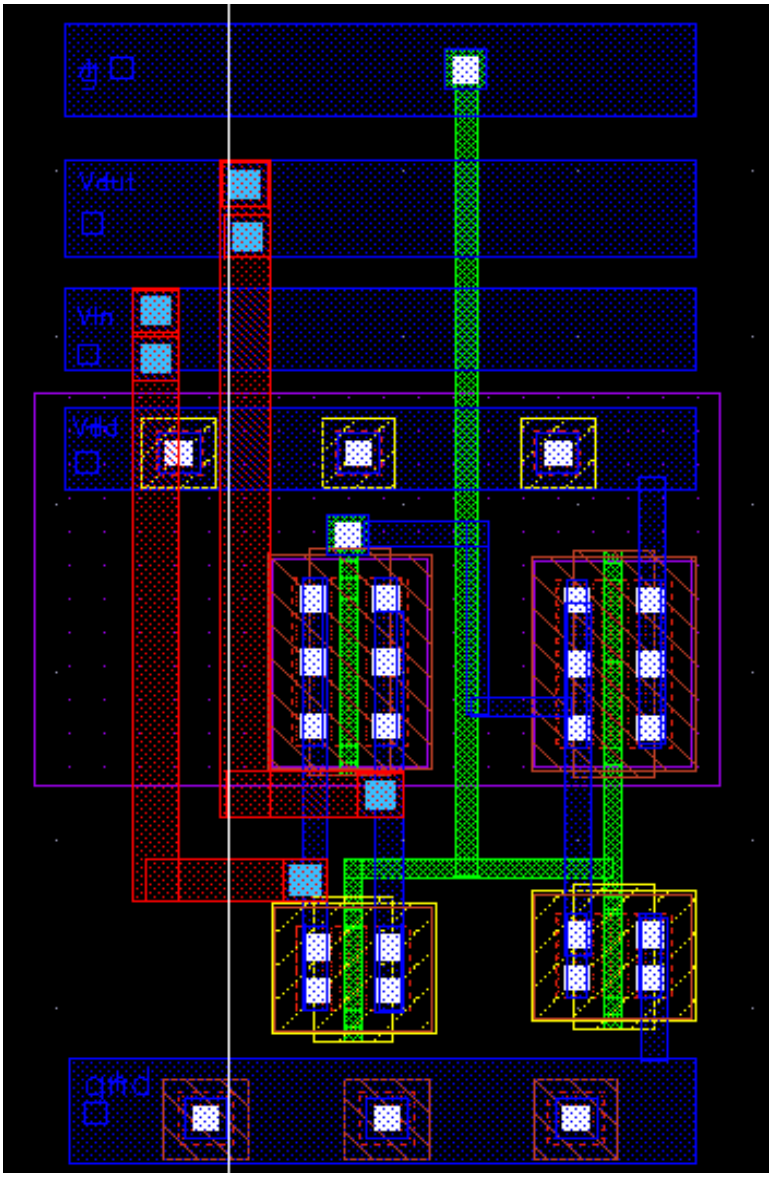

FIGURE 5.3 Layout of the blocking circuit.

5.4 Layout Design of Passing Circuit

The layout for the level down converter circuit is shown in Fig. 5.4. The layout of the pass circuit is very simple only consisting of two transistors forming a transmission gate.

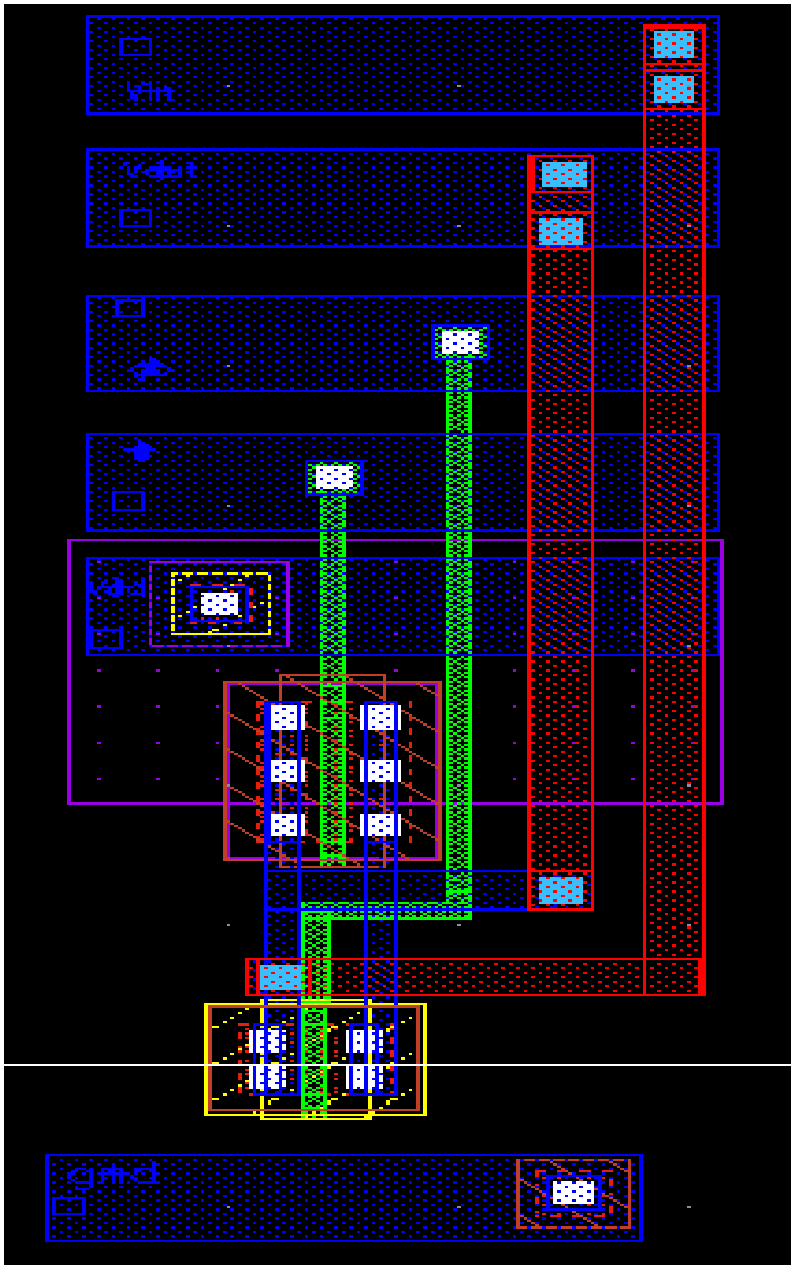

FIGURE 5.4 Layout of pass circuit.

5.5 Layout Design of 4:1 Multiplexer

The layout is as shown in Fig. 5.5. It has for input rails *Vin1*, *Vin2*, *Vin3* and *Vin4* and one output rail *Vout*. The voltage supply rail is shown by V_{DD} .

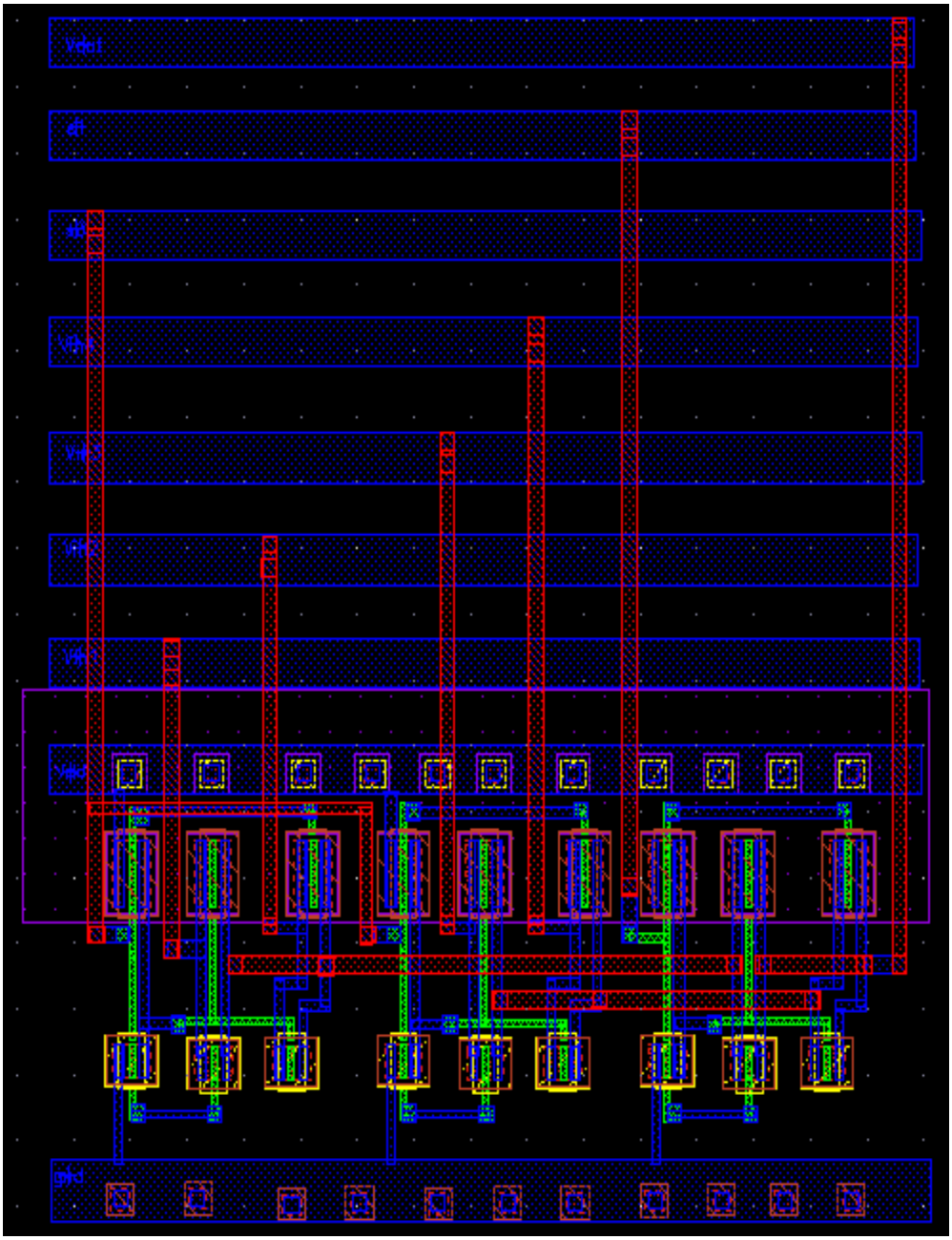

FIGURE 5.5 Layout of 4:1 multiplexer.

5.6 Layout Design of Universal Level Converter

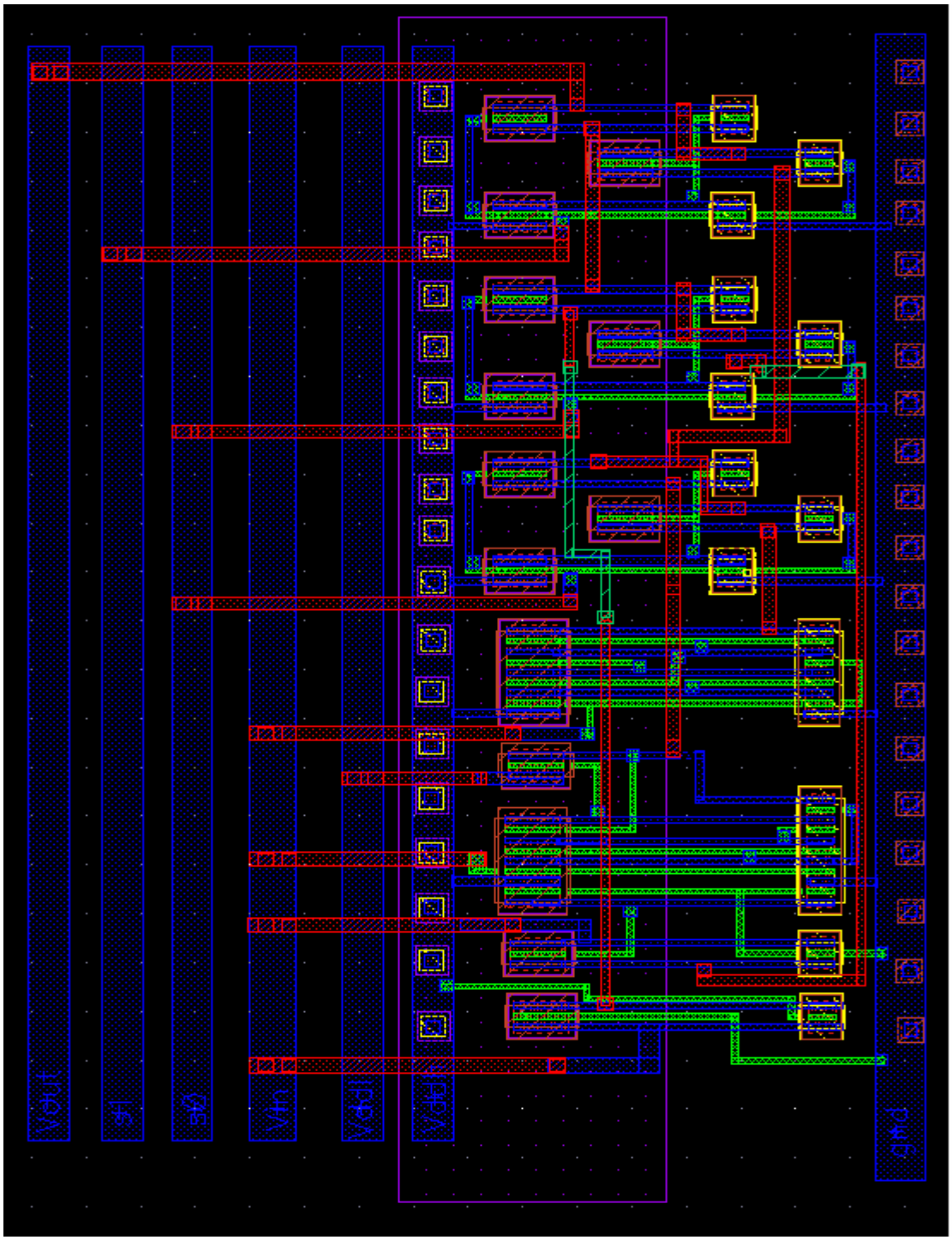

FIGURE 5.6 Layout of the universal level converter circuit.

The layout of the universal level converter is as shown in Fig. 5.6. The universal level converter has one input signal Vin which is represented by the *Vin* rail. The dual voltage supplies are connected through V_{DDH} and V_{DDL} rails. The output is connected to the output rails *Vout* . This layout consist five circuits, level up converter, down converter, pass circuit, block circuit, and 4:1 multiplexer circuit, built as a single circuit. The control signals are applied through s0 and s1.

CHAPTER 6

SIMULATION AND CHARATCTERIZATION OF UNIVERSAL LEVEL CONVERTER AT 45nm TECHNOLOGY

The circuit of the universal level converter is also built and characterized at 45nm technology. The circuit diagram of the universal level converter remains the same as described earlier in chapter 3. But the model files, device parameters and the supply voltages will change according to the technology used. The simulation and characterization details of ULC at 45nm technology are discussed in this chapter.

6.1 Transistor Level Schematic Design of Universal Level Converter

The circuit diagram of universal level converter at 45nm technology is similar to that built at 90nm technology. The ULC consist of four circuits dedicated to the four distinct level converting operations. A 4:1 multiplexer, made of transmission gates, is used to couple the four different outputs to the single output of the universal level converter circuit. The input signal is applied across the Vin pin of ULC. s0 and s1 are the control signals which are used to select the type of output at Vout. The transistor level schematic of universal level converter at 45nm technology is as shown in Fig. 6.1.

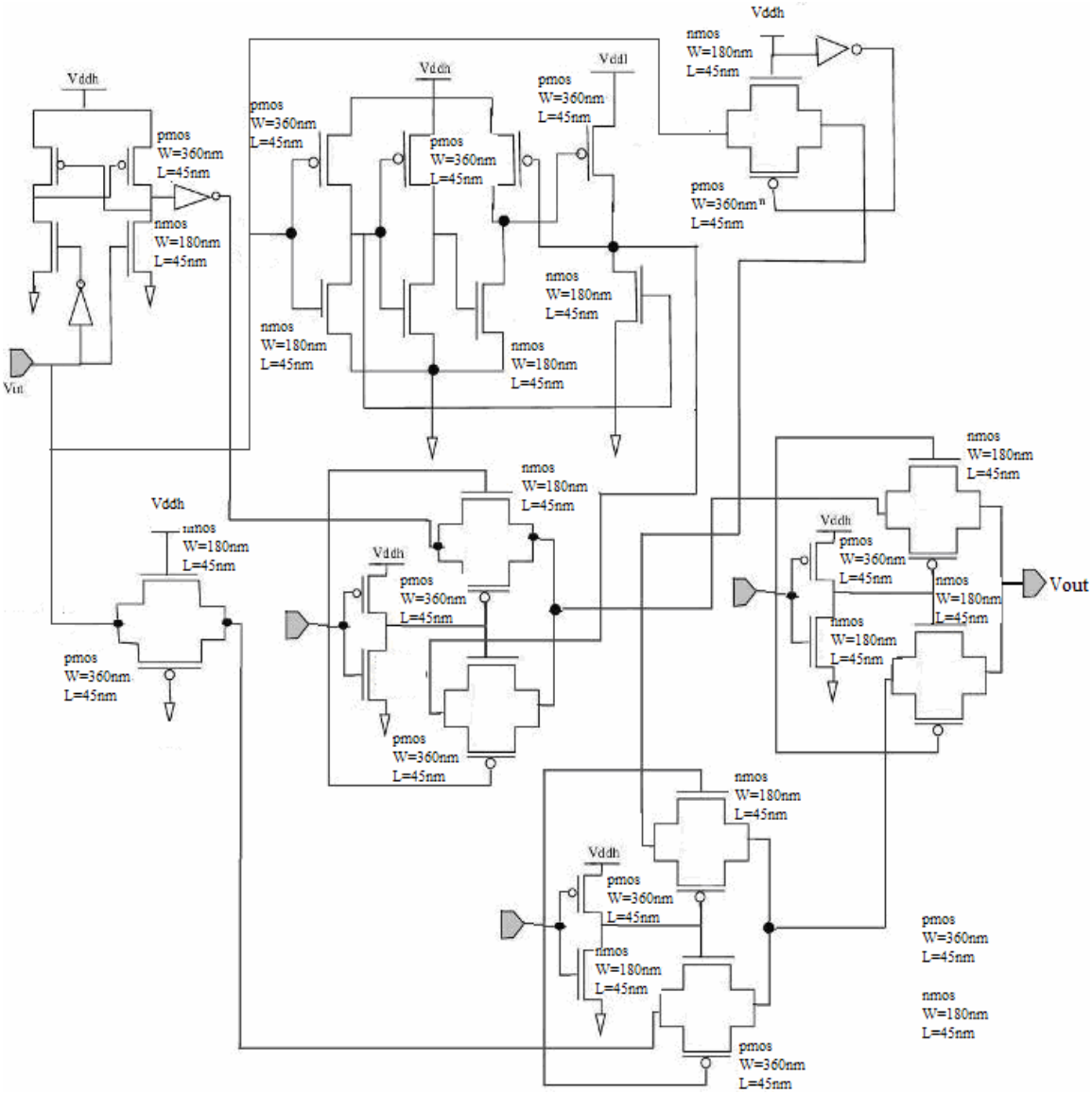

FIGURE 6.1 Transistor level circuit diagram of universal level converter at 45nm technology.

6.2 Simulation Results of Universal Level Converter

The simulation set up for 45nm technology is same as shown in Fig. 4.1. But to simulate ULC at this technology a BSIM4_45nm technology model file from PTM

(predictive technology model) is used. For this schematic design, a W/L ratio of 4:1 is used, and the device parameters for PMOS are W= 360nm and L = 45nm and for NMOS are W= 180nm and L = 45nm. The values of threshold voltages (V_{TH}) for PMOS and NMOS are -0.22V and 0.22V, respectively. The typical values for the dual voltage supplies are used as V_{DDH} = 0.7V and V_{DDL} = 0.595 (85% V_{DDH}). The dual voltage supplies at pins V_{DDH} and V_{DDL} are connected to voltage sources. The value of load capacitance used is 15fF. The pin *Vin* represents the input pin where a piecewise voltage signal is applied as input. *s0* and *s1* are the control signal pins which decide the type of output of ULC. The circuit is simulated in the *analog design environment (ADE)* and a transient analysis for 100nsec is performed during simulation. The output of ULC is observed in its different modes of operation as discussed Table 3.2. The Fig. 6.1 shows the output of the universal level converter in all of its four modes of operation.

The ULC can be used in a programmable logic environment where the control signals s0 and s1 change with time and the output of the ULC is also expected to change accordingly. The ULC design at 45nm technology is tested for such requirements and Fig 6.2 shows the output results for such scenario. The sub sections from 6.1.1 through 6.1.4 discuss the simulation results of each block of ULC independently.

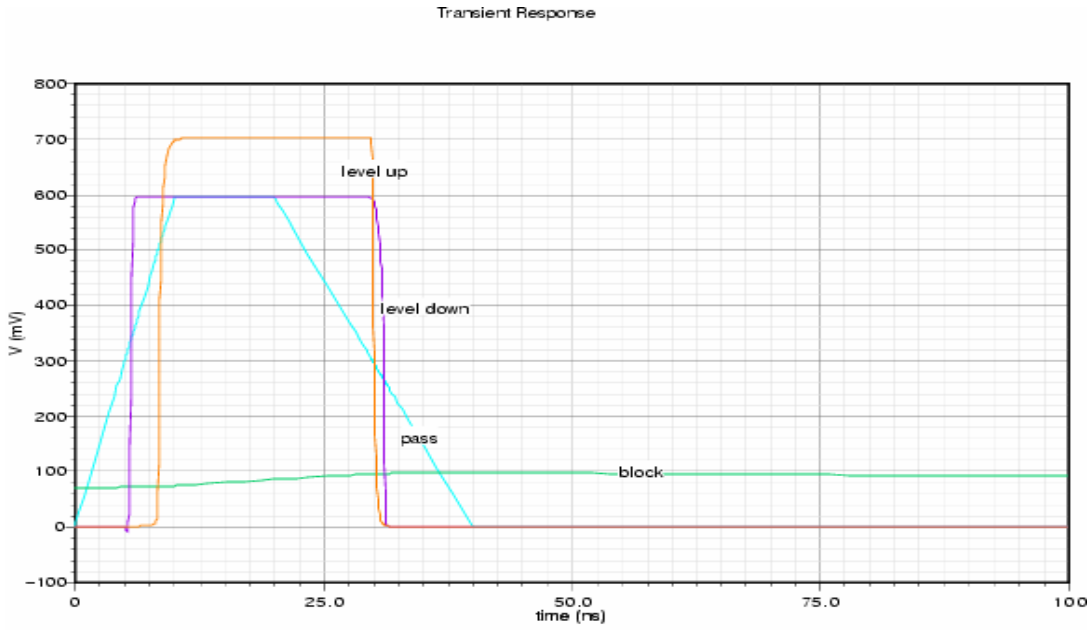

FIGURE 6.1 Simulation result of universal level converter showing the outputs for all the four modes of operation.

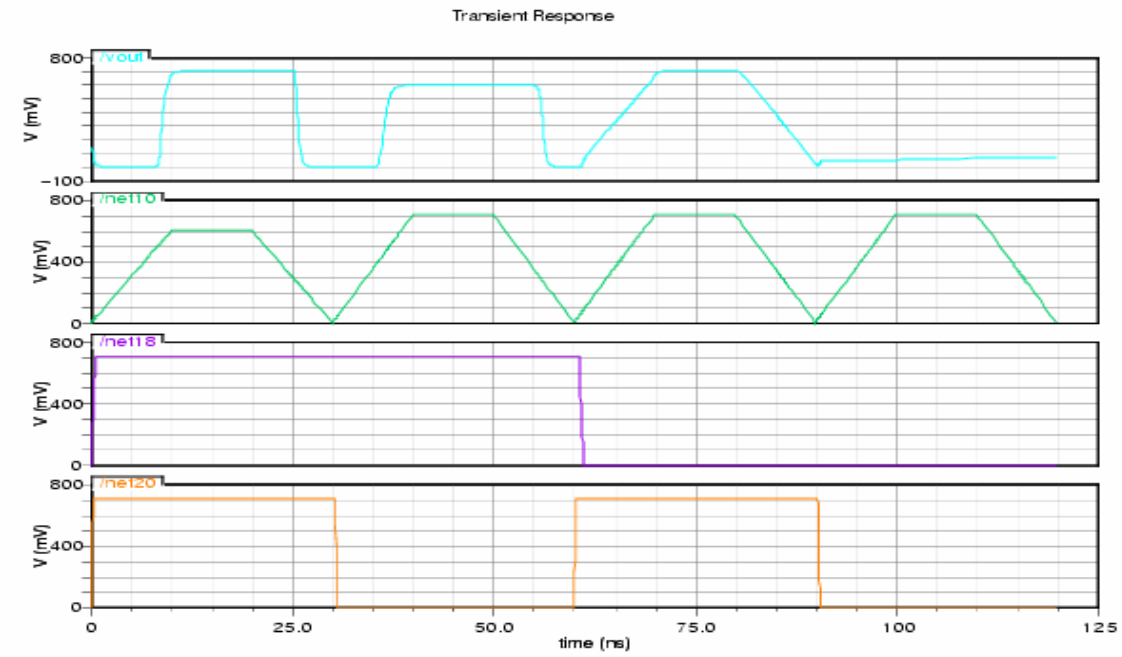

FIGURE 6.2 Simulation result of universal level converter showing the outputs for all the four modes of operation in a programmable design environment.

6.1.1 Level Up Converter

For level up converter simulation, a transient analysis for 100nsec is performed with both the control signals so and s1 as high. With these input states of the control signals the output of the ULC is the output of the level up converter circuit. As shown in the output plot in Fig. 6.3 the input signal at pin *Vin* is a piece wise linear voltage signal at 0.595V. This signal at a lower voltage level is converter to a higher level of 0.7V by the level up converter circuit.

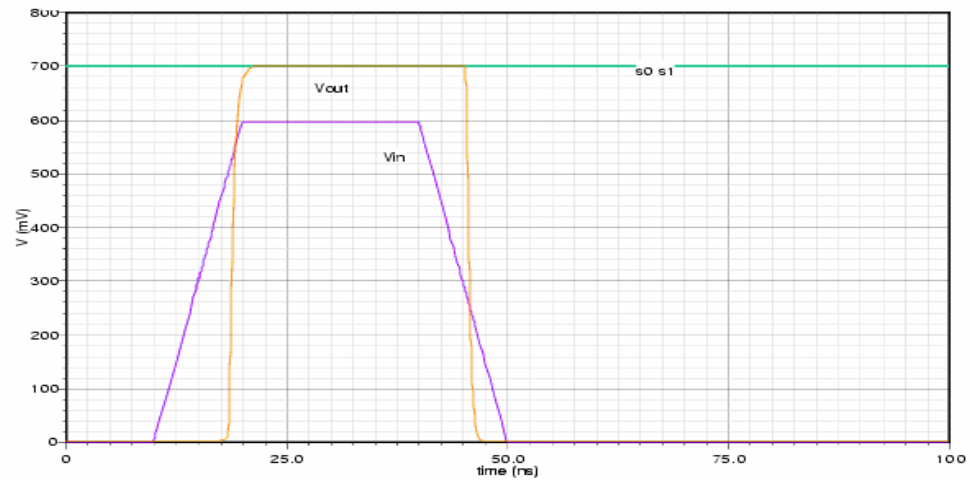

FIGURE 6.3 Output waveform for level-up conversion with V_{DDL} = 0.595V, V_{DDH} = 0.7V and at a of load = 15fF.

6.1.2 Level Down Converter

During simulation of ULC if s0 is maintained high and s1 is low then the output of ULC is the output of level down converting circuit. The input signal in this case is also a piecewise linear signal at a voltage of 0.7V (V_{DDH}) applied at *Vin* terminal of ULC. A transient analysis is carried out for 100nsec and the output result is observed.

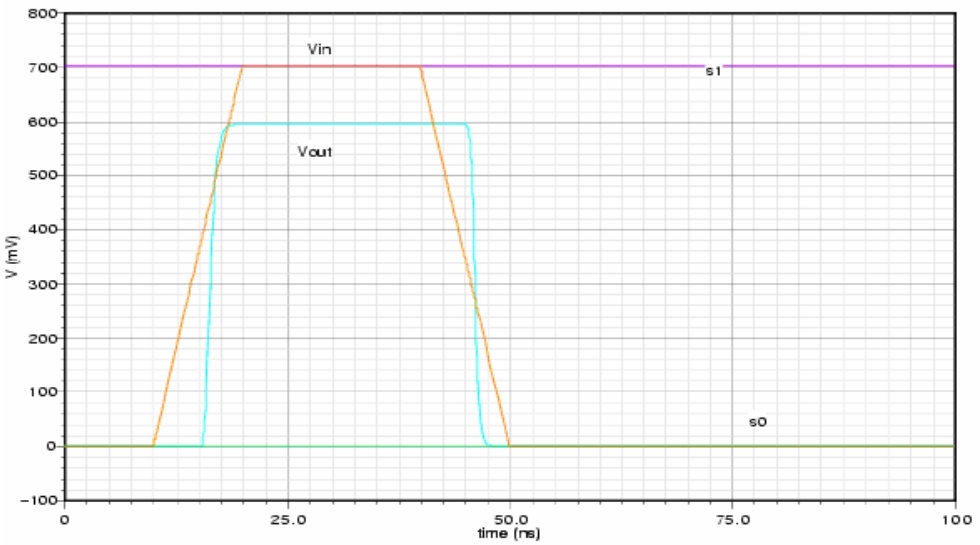

FIGURE 6.4 Output waveform for level-down conversion with V_{DDL} = 1.02V, V_{DDH} = 1.2V and at load = 15fF.

6.1.3 Blocking of Signal Operation

When s0 is low and s1 is also low then ULC acts as a blocking circuit. The output is shown in Fig. 4.3 as below. From the output it is clear that even when the input is as high as 1.2V the output voltage is very low below .36V which is less than the threshold voltage of PMOS and NMOS which are used in the design.

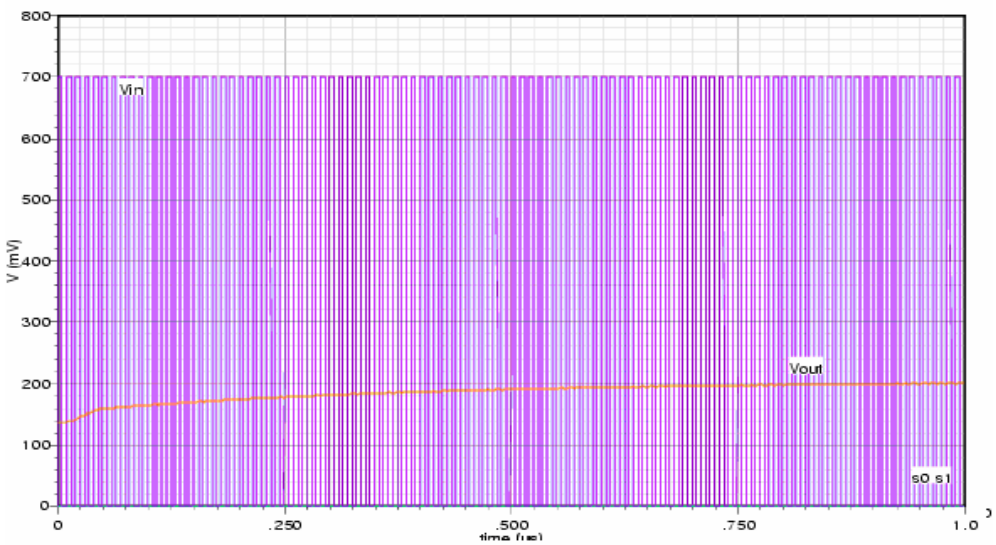

FIGURE 6.5 Output waveform of blocking of signal operation.

6.1.4 Passing of Signal Operation

ULC can be made to work as a passing circuit when control signals1 is low and s0 is high. As shown an input signal at 0.7V is applied which is bypassed to output as it is.

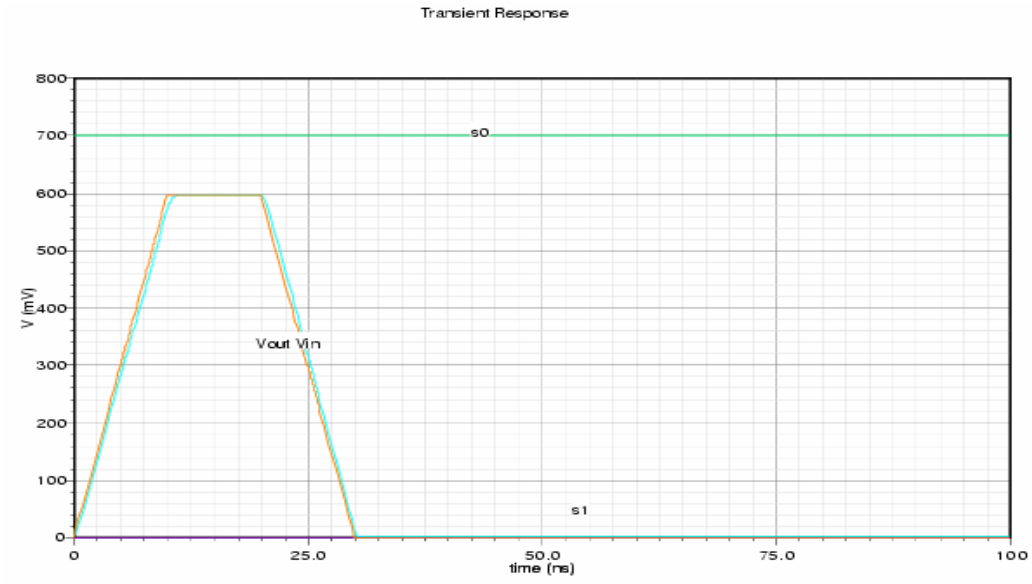

FIGURE 6.6 Output waveform of passing of signal operation.

6.2 Characterization of Universal Level Converter

It is very essential to characterize any design if it is to be used for low power applications. By doing the power consumption and the load the design can handle can be determined. The ULC design is characterized by performing three analyses:

(i) parametric

(ii) power

(iii) load analysis

The output results of ULC for these three analyses are shown in the following subsections.

6.2.1 Parametric Analysis

Parametric analysis is nothing but varying one of the parameters and observing the effects it has on the output. The *parametric analysis tool* from the *analog design environment* is used. A parametric analysis on the universal level converter is performed for it level up conversion, level down conversion and pass signal mode of operation. A transient analysis for 100ns is carried where in the output voltage is observed for a varying lower voltage (V_{DDL}). The value of V_{DDH} voltage is kept at a constant level at 0.7V and the V_{DDL} voltage is varied from 0.1V to 0.595V with an increasing step of 0.1V. The output signal is observed at the output terminal *Vout* of ULC for the level up conversion, level down conversion and pass circuits. These results are shown in Fig. 6.7, Fig. 6.8, and Fig. 6.9 respectively.

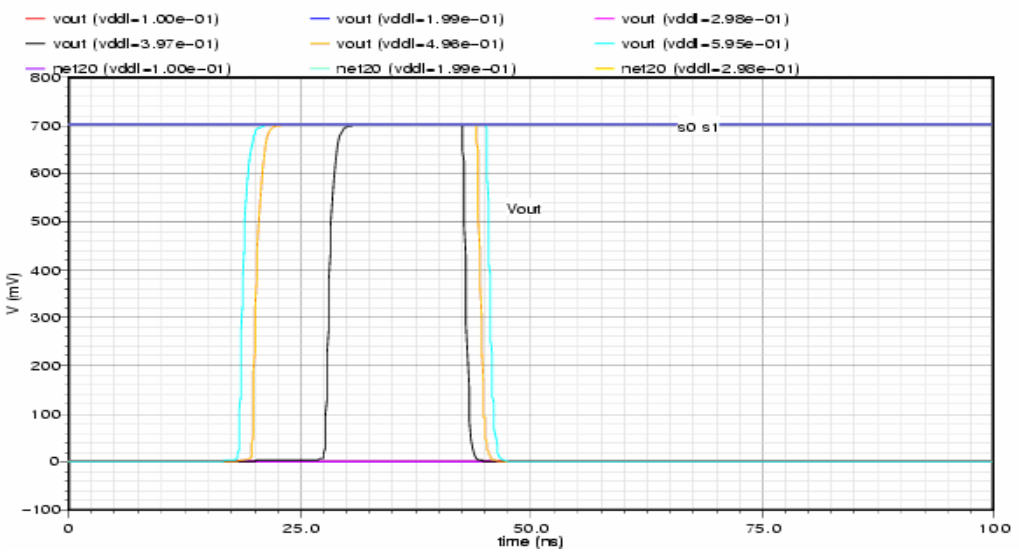

FIGURE 6.7 Parametric analysis for up-converter circuit showing the output (Vout) waveforms when the V_{DDL} is varied from 0.1V to 0.595V with an increasing step of 0.1V and constant V_{DDH} = 0.7V.

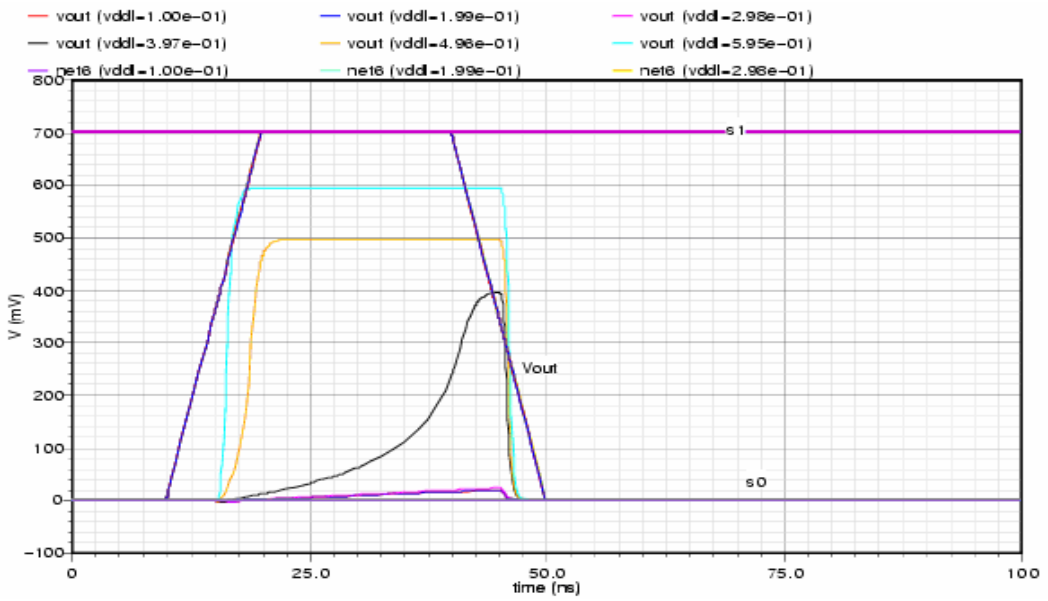

FIGURE 6.8 Parametric analysis for down-converter circuit showing the output (Vout) waveforms when the V_{DDL} is varied from 0.1V to 0.595V with an increasing step of 0.1V and constant V_{DDH} = 0.7V.

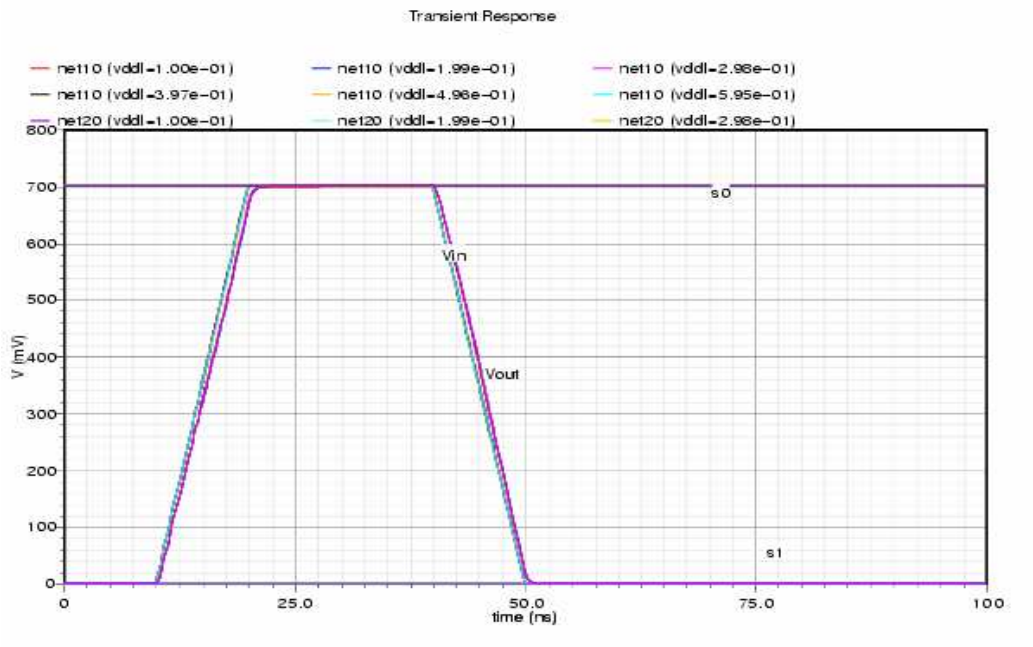

FIGURE 6.9 Parametric analysis for pass circuit showing the output (Vout) waveforms where the V_{DDL} is varied from 0.1V to 0.595V with an increasing step of 0.1V and constant V_{DDH} = 0.7V.

The parametric analysis results prove that the universal level converter circuit can work very efficiently at 45nm technology even at lower voltages like 0.45V. This is a very important lower power design property.

6.2.2 Power Analysis

The power analysis for ULC at 45nm technology is done in the same way as for ULC at 90nm technology. The analysis includes calculating the power consumed by ULC on the whole and also the power consumed by each block of ULC and the power consumed by the transistors. For doing this analysis the browser and the calculator tools of *analog design environment* are used after simulating the circuit diagram. The total

power consumed by the universal level converter can be given as the sum of power consumed by each block that constitutes the ULC. The total power consumed can be found out by using the formula:

$$P_{ulc} = P_{cclc} + P_{dl} + P_{block} + P_{pass}.$$

The power consumption calculated for the universal level converter and the different blocks of ULC at three different load is shown in Table 6.1. From these power calculations it can be concluded that universal level converter has a very low average power dissipation of about 3.533 μW.

TABLE 6.1 Power consumption of universal level converter for three different loads.

Load	Circuit	Power Consumption (μW)	Total Average Power Consumption
10fF	Level-UP Converter	1.899 μW	3.3082 μW
	Level-Down Converter	1.170 μW	
	4:1 Mux	0.842 μW	
	Block Circuit	0.0184 μW	
	Pass Circuit	0.0033 μW	
45fF	Level-UP Converter	1.958 μW	3.5118 μW
	Level-Down Converter	1.170 μW	
	4:1 Mux	0.2555 μW	
	Block Circuit	0.0184 μW	
	Pass Circuit	0.0033 μW	
90fF	Level-UP Converter	2.029 μW	3.7790 μW
	Level-Down Converter	1.170 μW	
	4:1 Mux	0.4048 μW	
	Block Circuit	0.01840 μW	
	Pass Circuit	0.0033 μW	

The following tables from Table 4.2 through Table 4.7 shows the detailed power consumption of the individual level converting blocks of ULC, including the power consumed by each transistor for a load of 10fF.

TABLE 6.2 Power consumption of level up converter.

Sub circuit	Transistor	Type	Average Power
Inverter	M0	PMOS	0.255 μW
	M1	NMOS	0.337 μW
--	M2	PMOS	0.101 μW
--	M3	NMOS	0.640 μW
--	M4	PMOS	0.158 μW
--	M5	NMOS	0.170 μW
Total average power		1.89 μW	

TABLE 6.3 Power consumption of level down converter.

Transistor	Type	Average Power
M0	PMOS	0.338 μW
M1	PMOS	0.0595 μW
M2	PMOS	0.201 μW
M3	PMOS	0.0470 μW

M4	NMOS	0.256 μW
M5	NMOS	0.0450 μW
M6	NMOS	0.134 μW
M7	NMOS	0.0880 μW
Total average power		1.157 μW

TABLE 6.4 Power consumption of 4:1 multiplexer.

Transistor	Type	Average Power
M0	PMOS	0.0170 μW
M1	PMOS	0.0317 μW
M2	NMOS	0.0344 μW
M3	NMOS	0.0004 μW
M4	PMOS	0.00002 μW
M5	NMOS	0.0004 μW
Total average power		0.0842 μW

TABLE 6.5 Power consumption of blocking circuit.

Sub circuit	Transistor	Type	Average Power
Inverter	M0	PMOS	0.0164 μW
	M1	NMOS	2.509 pW

--	M2	PMOS	0.0002 μW
--	M3	NMOS	0.00164 μW
Total average power		0.0184 μW	

TABLE 6.6 Power consumption of pass circuit.

Transistor	Type	Average Power
M0	PMOS	1.439 nW
M1	NMOS	1.884 nW
Total average power	3.323 nW	

6.2.3 Load Analysis

In load analysis of ULC, the circuit output is observed for a varying load conditions. The effect on the output for a varying load from 1fF to 200fF is studied in load analysis. From this analysis it can be concluded that the ULC produces a stable output under varying load conditions. This is again an important design feature for voltage level converters. The Fig. 6.10, Fig. 6.11 and Fig. 6.12 show the output plot for load analysis on level up converter, level down converter and on pass circuits.

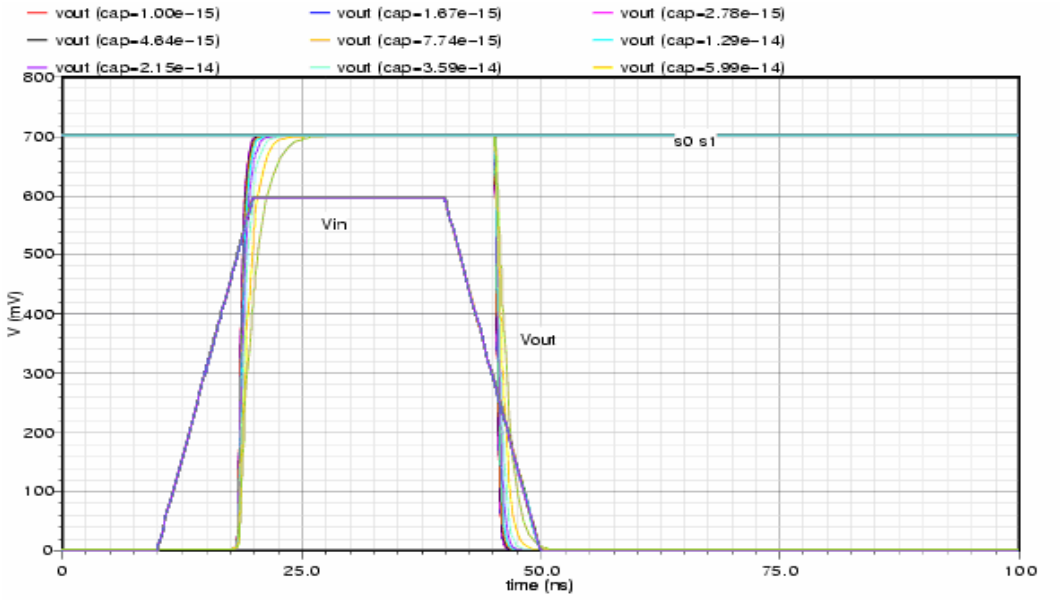

FIGURE 6.10 Output for level up conversion under different load conditions with load varying from 10fF to 200fF.

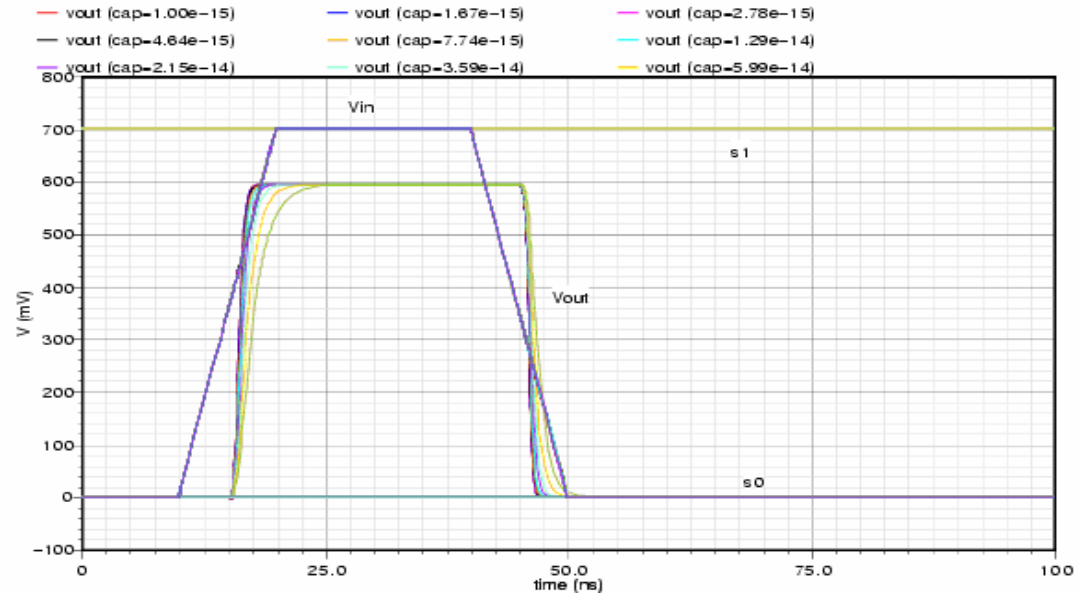

FIGURE 6.11 Output for level down conversion under different load conditions with load varying from 10fF to 200fF.

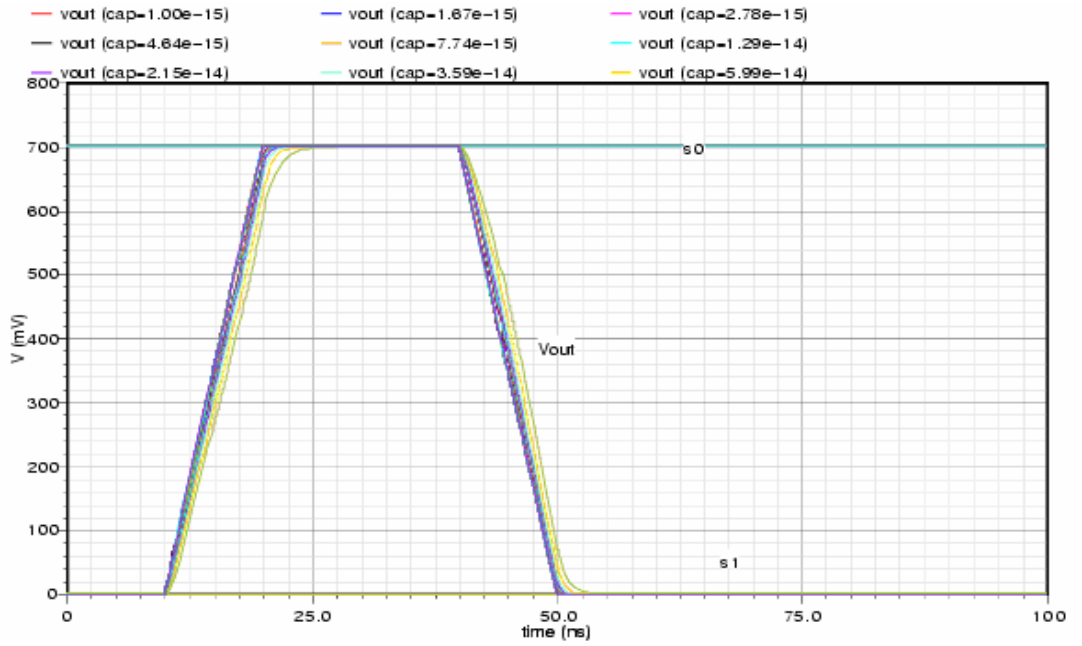

FIGURE 6.12 Output for level up conversion under different load conditions with load varying from 10fF to 200fF.

CHAPTER 7

CONCLUSION AND FUTURE WORKS

A novel level converter circuit called universal level converter (ULC) is presented. This design is capable of performing four distinct types of level converting operations. The circuit of ULC is built and tested at 90nm and 45nm CMOS technologies. The simulation results prove that the circuit can also be used in a programmable logic mode where the functionality of the circuit can be changed according to a clock signal. The design is characterized by performing parametric, power and load analysis. These three analyses prove that the proposed level converter design is not only a low power design but it also provides a stable output under varying load conditions. The parametric and load analysis results prove that the design of universal level converter produces a very stable output at low voltage such as 0.7V at 90nm design and 0.45V at 45nm design with a varying load fro 1fF-200fF. The power analysis results prove that the universal level converter has a power dissipation reduction of about 85% - 97% as compared to other level converter designs at a different technology. The ULC consumes an overall average power of about 3.557μW at 45nm technology and about 27.535μW at 90nm technology. The layout of ULC and the individual blocks of ULC is created successfully at 90nm technology and verified for its correctness by performing a DRC check using the divaDRC.rul and assuraDRC.rul files.

Future extension can be made to this thesis both at schematic and layout level. The schematic can be further scaled down to lower technology keeping in mind the

various design constraints for low power design. The delay aspect of the universal level converter can be studied at more detailed level.

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