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LOW-VOLTAGE CONTINUOUS-TIME LINEAR EQUALIZER FOR DIGITAL VIDEO APPLICATIONS

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San José State University

In Partial Fulfillment

of the requirements for the Degree

Master of Science

by

Poonam V. Agale

August 2014

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The Designated Thesis Committee Approves the Thesis Titled

LOW-VOLTAGE CONTINUOUS-TIME LINEAR EQUALIZER FOR DIGITAL VIDEO APPLICATIONS

by

Poonam V. Agale

APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

SAN JOSE STATE UNIVERSITY

August 2014

Dr. Shahab Ardalan	Department of Electrical Engineering
Dr. Sotoudeh Hamedi-Hagh	Department of Electrical Engineering
Prof. Morris Jones	Department of Electrical Engineering

ABSTRACT

LOW-VOLTAGE CONTINUOUS-TIME LINEAR EQUALIZER FOR DIGITAL VIDEO APPLICATIONS

by Poonam V. Agale

This thesis presents a low-voltage continuous-time linear equalizer for the digital video application of 1080p HD video with a data rate of 3 Gbps. The equalizer was designed in the CMOS 45 nm technology with a supply voltage of 1V and bias current of 1.5 mA. The equalizer has a variable gain, which can be adjusted to suit the cable length and physical parameters. The circuit design of the equalizer filter includes a 3-stage filter, where each stage has been implemented as a variable gain amplifier along with a linear transconductance amplifier as a gain control stage. The equalizer is capable of compensating for the loss of a coaxial cable within the range 0-240 m in length, with each stage compensating for a cable of 80 m. The circuit design of the equalizer was implemented in the CMOS 45 nm technology in Cadence Virtuoso. The equalizer was also tested in Matlab, using the model of the coaxial cable to demonstrate the equalization of the data. The transient results of the equalized data, as well as the eye diagrams, are presented in this work.

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1. Introduction

1.1. Background

The on-chip communication frequency increased tremendously from 1994 to 2004, crossing into the GHz range [1]. This spurt in the on-chip communication frequency has been due to rapidly shrinking silicon processes, which have improved on-chip bandwidth capabilities. Microprocessor speeds have not increased much after 2004 so as to limit the power consumption on IC's [1]. This spurt in on-chip capabilities has caused a demand for higher bandwidth capabilities for the off-chip interfaces.

The demand for HDTV has brought about the need for high data rates in the transmission of digital data. Data rates in the range of 3 Gbps are needed for 1080p HD video, and there is a higher need for data rates. Digital video applications use serial digital interfaces to handle the requirements of uncompressed digital video. The coaxial cable is a serial digital interface used for digital video applications like 1080p HD video. The 1080p HD technology is a mature technology and is being standardized in the market today. In the consumer domain, almost all flat panel displays with HDMI 1.3 interfaces can display 1080p HD video.

1.2. Motivation

This need for high data rates has led to the development of techniques that create more room in the bandwidth domain and thus reduce effects like ISI. Adaptive equalizers [2],

[3] have been implemented for digital video applications in a 0.8 μm/14 GHz BiCMOS process and a 14 GHz bipolar process respectively. Other equalizers [4], [5] have achieved up to 3.5 Gbps with a 1.8 V supply in a CMOS process and 10 Gbps with a 3.3 V supply in a SiGe BiCMOS process. These implementations show that high-data rates using an unknown cable length (up to a certain range) can be achieved with adaptive equalization. However, there is still a need for low-voltage and low-power equalizers, implemented in a CMOS process for better integration with the receiver circuits of the transmission system.

The need for equalization is to eliminate the effects of ISI, which occur due to the non-linear effects of the channel and cause successive symbols to blur together. Figure 1.1 shows perfect PRBS data generated in Matlab, which is used for input to the coaxial cable. The low-pass nature of the cable affects the data, and this can be clearly seen in the Figure 1.2. The data output from the cable is shown in Figure 1.3, and the data are attenuated due to the low pass characteristics of the cable. The cable model that has been created and used is the model of a Belden 1694A cable, which is designed for high-speed transmission of digital data.

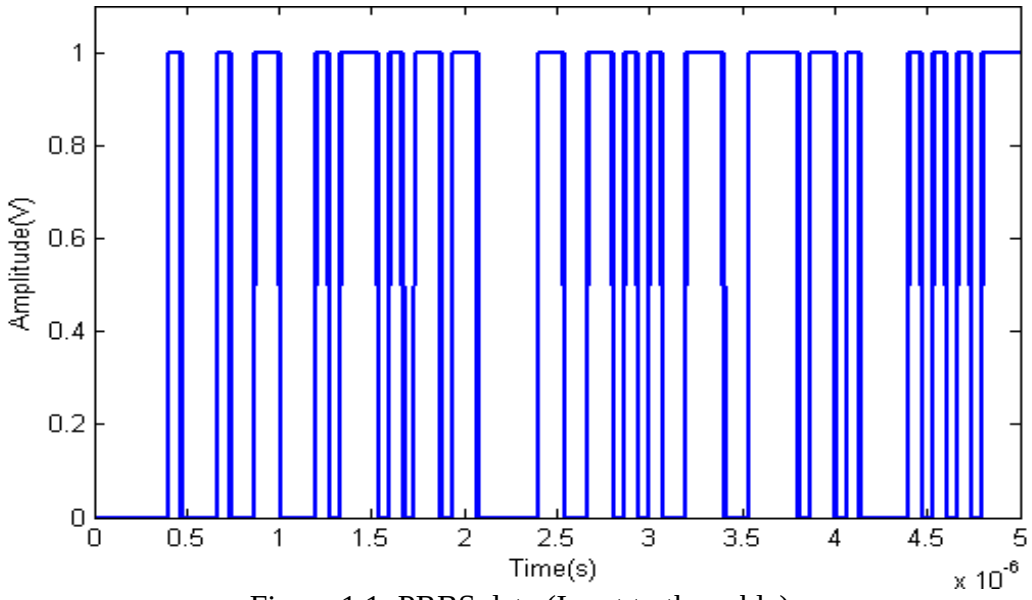

Figure 1.1: PRBS data (Input to the cable)

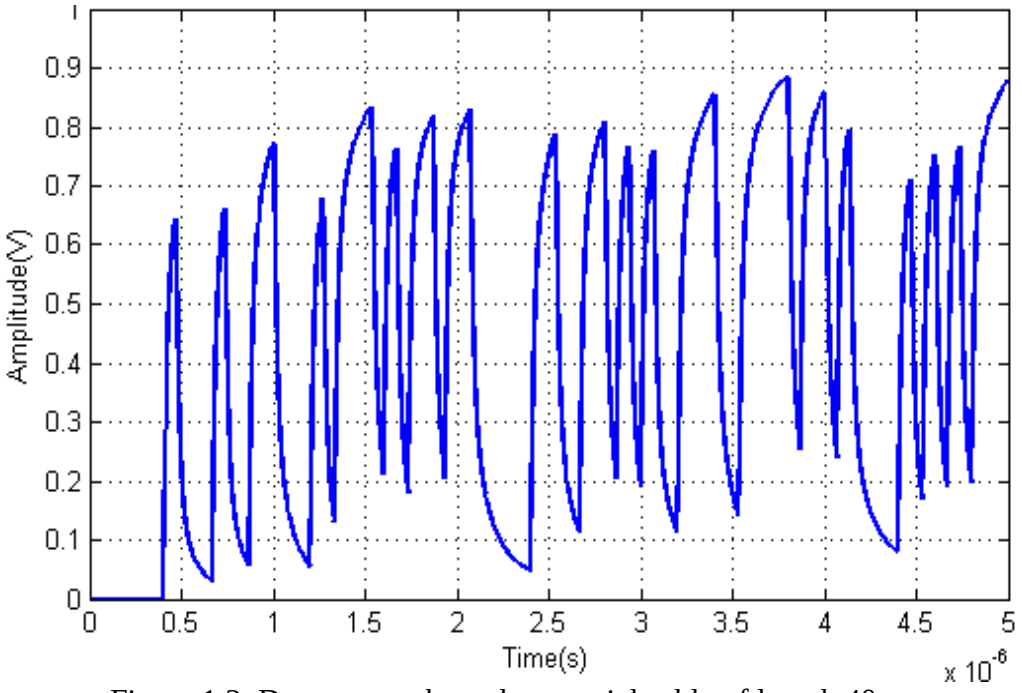

Figure 1.2: Data output through a coaxial cable of length 40 m

The coaxial cable has an inner conductor, which is surrounded by insulating material (dielectric). The dielectric material is then covered with a copper shield, and finally a

plastic sheath surrounds and completes the cable. The inner conductor and the outer conductor are configured in such a way that they form concentric cylinders while having a common axis, as shown in Figure 1.3. The copper shield is kept at ground potential, while the electrical signal propagating through the cable is applied to the center core conductor. The coaxial cable insulates the signal from the outside electric and magnetic fields and has less leakage than other cables.

A digital coaxial cable is better shielded for interference and has higher impedance, allowing it to handle more energy and a larger range of electrical frequencies.

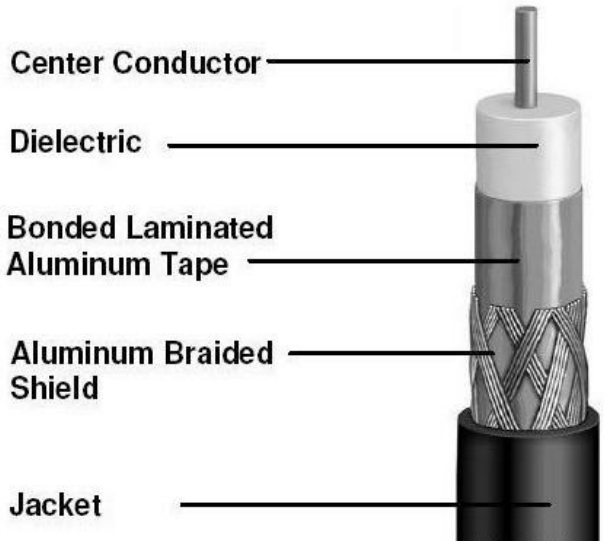

Figure 1.3: Coaxial cable

One such digital coaxial cable that is used for video applications is the Belden 1694A cable, with an impedance of 75 Ω. This HD designed coaxial cable can carry the 3 Gbps signal needed for 1080p/50 HD video with an attenuation of 21 dB for a cable of 100 m.

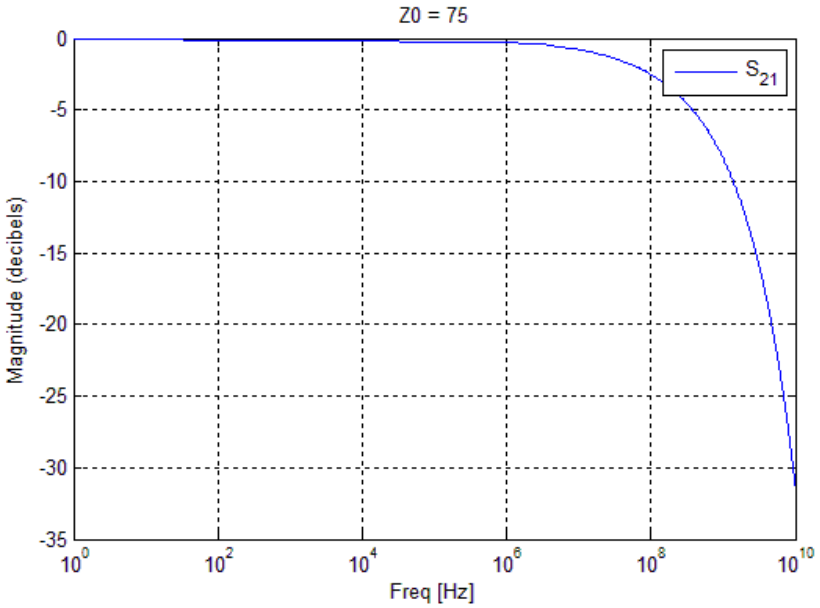

Figure 1.4: Coaxial cable frequency response (length = 80 m)

In recent years, coaxial cables have been applied in a wide variety of residential, commercial, and industry installations. One of the applications of coaxial cables is for digital video applications. The losses in the coaxial cable are due to the resistance of the conductors and the dielectric that is used for insulating the conductors consumes power. Losses in the transmission line arise from sources like radiation, dielectric loss, and skin effect loss [6].

Attenuation is the inherent signal power loss in the coaxial cable, and it is dependent on both the frequency and the length of the cable. Attenuation is caused by the DC resistance of the center conductor and the dissipation factor of the dielectric material. Attenuation is typically expressed in dB/100 ft.

Reflection losses are based upon signals reflecting back to the source rather than propagating through the cable. These reflections are caused by impedance mismatches or

variations due to any physical changes in the cable. The reflection losses can be minimized by quality cable manufacturing techniques and proper installation techniques [7].

Insertion loss is the combination of attenuation losses and reflection losses, resulting from impedance changes at the cable input and output interface plus any reflection losses along the cable length, along with any other losses such as radiation. Conductor losses vary with the square root of frequency, which is due to the skin effect. Losses from the dielectric increase with frequency and are due to friction from the resistance of the conductor [8].

The cable loss characteristics can be modeled as a function of frequency [3]:

$$C(f) = e^{-k_s l(1+j)\sqrt{f} - k_d f} \tag{1.1}$$

where, k_S is the skin effect constant, k_d is the dielectric constant and l is the cable length.

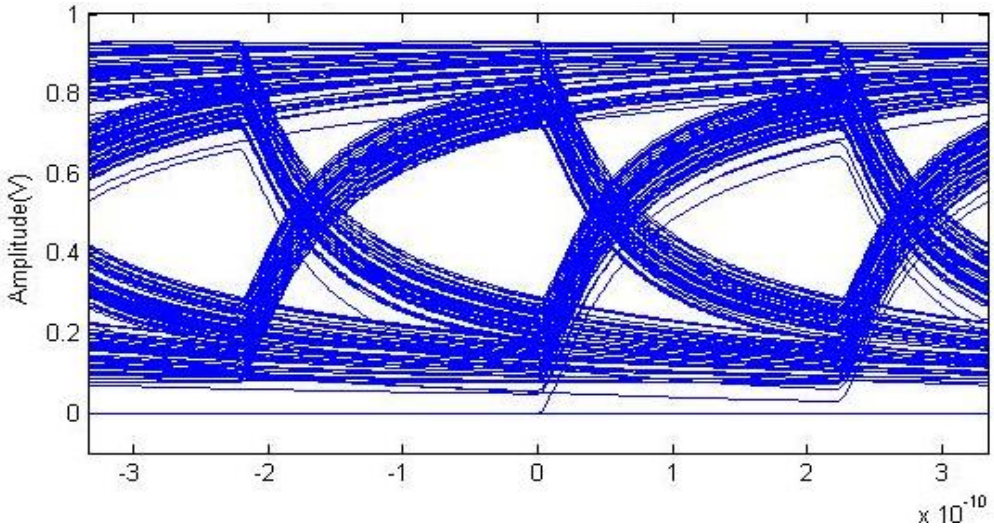

Figure 1.5: Eyediagram of data output from a 40 m cable

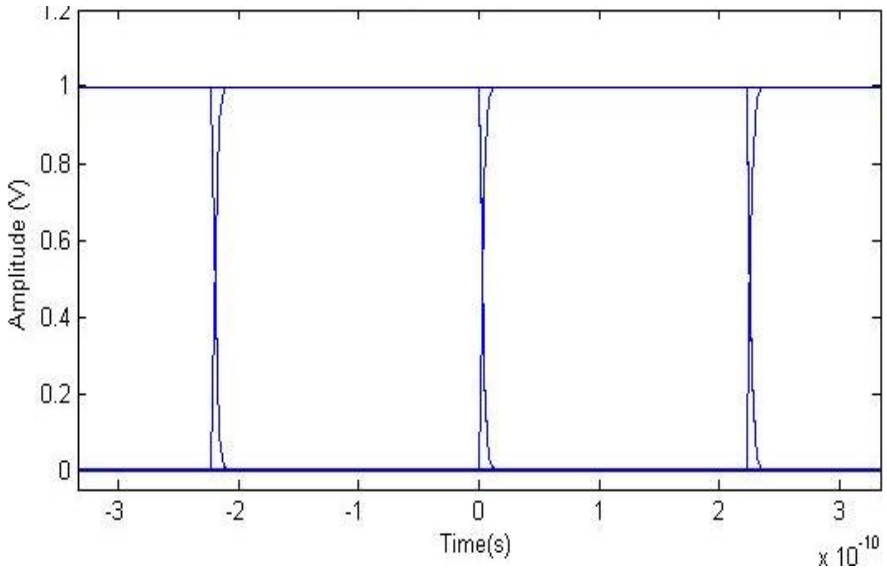

Figure 1.6: Eyediagram of equalized data simulated in Matlab

The eye diagram shown in Figure 1.5 is that of the data output through a 40 m cable. Clearly, the eye opening is small due to the distortion and attenuation of data and a considerable amount of jitter can be seen to occur in the eyediagram. The data output from the cable is then put through a filter whose transfer function is the inverse of the cable function. This filter acts as an equalizer and amplifies the attenuated data, resulting in a wider eye opening as shown in Figure 1.6. The equalizer transfer function used to obtain this eye diagram is an ideal transfer function obtained as the inverse of the cable transfer function. Due to the ideal nature of the equalizer in this case, the eye diagram of Figure 1.6 is an ideal eye diagram with a wide eye opening and no jitter.

2. Continuous-time linear equalizer

2.1. Equalization

According to the Shannon-Hartley theorem, the maximum data rate at which the error-free signal can be transmitted through a band-limited channel in the presence of noise can be improved by widening the bandwidth of the transmission channel or improving the signal-to-noise ratio of the signal. The general formula for Shannon-Hartley's theorem is expressed as [9]:

$$C = \mathrm{B}\log_2(1+SNR) \tag{1.2}$$

where,

C = data rate measured in number of bits per second

B = Bandwidth of the signal measured in Hertz

SNR = Signal to noise ratio

Equalization is a method where a waveform is manipulated at either the transmitter or the receiver in order to compensate for the imperfections of the channel, and thus restore signal integrity. Equalization can be achieved by providing a flat band frequency response which extends slightly beyond the operating frequency of the system. Conventional methods such as replacing the channel with low-loss material, incorporating a repeater in

the channel, and reducing the channel length are no longer effective in solving high-speed communication issues [9]. Besides correcting for the channel frequency-response anomalies, the equalizer can cancel the effects of multipath signal components, which can manifest themselves in the form of voice echoes, video ghosts, or Rayleigh fading conditions in mobile communications channel [10].

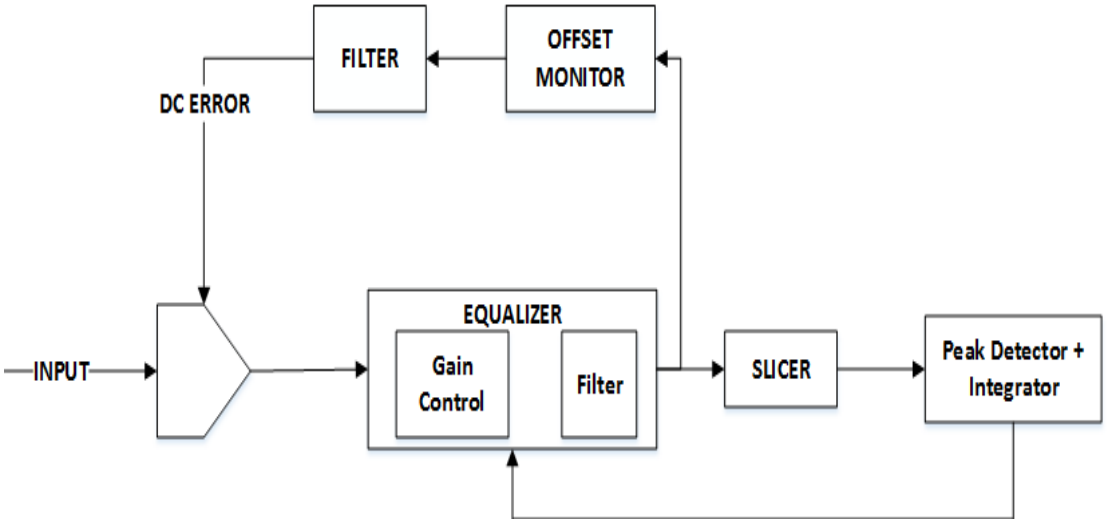

Figure 2.1: Block diagram of the proposed equalizer

The block diagram in Figure 2.1 shows the system diagram of the proposed equalizer. The equalizer consists of two main parts: one is the equalizer filter, and the second part of the equalizer is the DC restorer combined with the gain decision circuit. The gain selection depends on the attenuation affecting the input signal, while the attenuation is a function of the cable length and the cable physical parameters.

The adaptive gain control block is used to compare the received signal with a reference level, and then determine the gain of the filter that needs to be implemented. The received signal is used to determine the average or the peak amplitude of the signal. The signal is

subjected to a slicer circuit and then an integrator, from which a dc voltage value is obtained which is proportional to the peak of the received signal. This dc voltage is then compared to a reference value and an error signal is obtained. The error signal determines the number of filter stages and the level of gain in each stage that will be used to amplify the received signal. This process is iterated till the generated error signal is within an acceptable range.

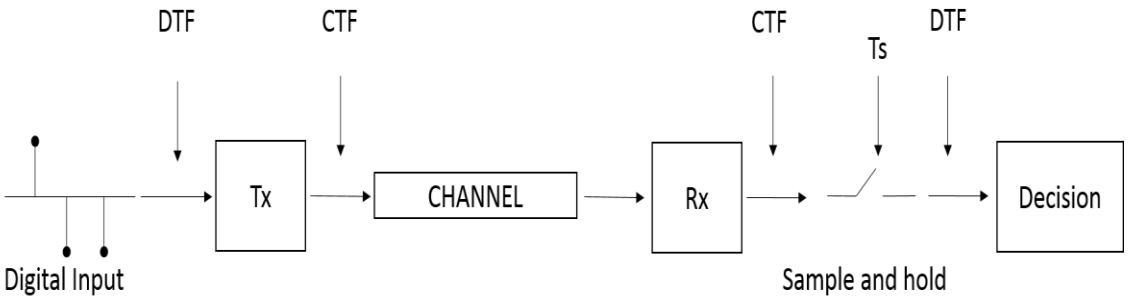

Figure 2.2: Block diagram of a Transmission System

The block diagram in Figure 2.2 is that of a digital transmission system which can be improved with the use of discrete-time or continuous-time filters. The placement of the discrete-time or continuous-time filters has been shown above, exploring both the receiver and transmitter placement options. As can be seen from the Figure 2.2, the discrete-time filter is placed after the sample and hold circuit at the receiver. The sample and hold circuit takes samples of the continuous-time data such that a sample is created with every clock edge. If the clock has any jitter or skew, the wrong data might be sampled and would eliminate any chance of recovery of the data. In the case of the continuous-time filter, the data is first equalized and then it is sampled. The data can therefore still be recovered, even if it has been sampled incorrectly. Another factor is to decide the

placement of the filter at the transmitter or at the receiver. Placing the filter at the transmitter is not very ideal for adaptation, as the filter response has to be adjusted based on the time varying channel. Therefore, if the filter is at the transmitter, a feedback will be needed from the receiver to the transmitter to adjust the response of the filter. In the other case, if the filter is at the receiver, the response of the filter can be easily adjusted depending on the channel response.

Transmit equalization pre-distorts a transmitted signal by amplifying the high-frequency content of the signal to compensate for the expected amount of loss through the channel. The emphasized portion of the signal is attenuated by the channel resulting in an open eye that can be easily interpreted by the receiver. However, the lower supply voltage due to process scaling trend and high channel losses imply that majority of the equalization is performed at the receiver side [11].

There are two main techniques that are employed to formulate the filter coefficients, which will ultimately aim to compensate for the low-pass characteristics of the channel.

1. Automatic Synthesis

In this method, the equalizer receives a time-domain reference signal and compares it to a stored copy of the undistorted training signal. This comparison results in an error signal which can be determined to calculate the transfer function of the inverse of the channel transfer function. The formulation of this inverse filter may be accomplished strictly in the time domain, as is done in the ZFE and LMS systems. Another method is to convert the training signal to a spectral representation to enable the formulation of the

inverse channel response. The inverse spectrum is then converted to a time-domain representation for calculating the filter tap weights. The main disadvantage of using this method is that the training signal which is as long as the filter tap length must be transmitted [10].

2. Adaptation

In adaptation, the equalizer attempts to minimize the error signal based on the difference between the output of the equalizer and the estimate of the transmitted signal, which is generated by the decision device. The adaptation tries to keep the difference between what was most likely transmitted and what was received to a minimum. Adaptation techniques can prove useful to compensate for minor variations in the channel response and to a certain length of the channel.

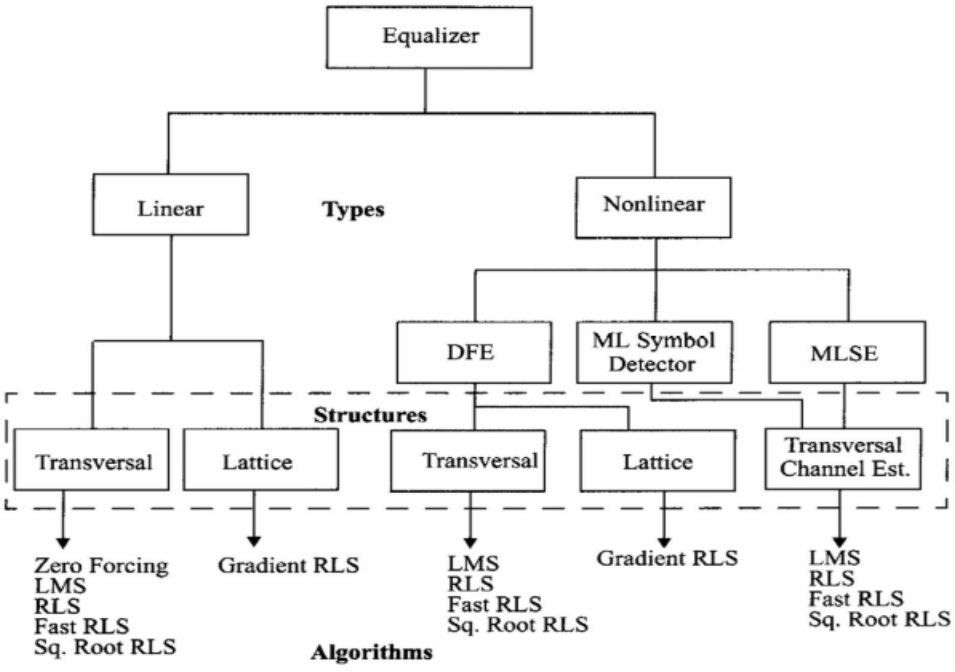

Figure 2.3: Classification of Equalizers [12]

2.2. Literature survey

The purpose of performing a literature survey was to find the processes and methods in which the equalizers have been designed so as to determine the approach needed to take to design a low-voltage and low-power equalizer, as well as to judge the need of such a project. As seen from the table above, a low-voltage equalizer design is needed to bridge the gap between highly evolving digital circuits and the analog circuits, which are mostly designed in higher technologies with higher supply voltages.

This work competes with the previous works in terms of better integration with the existing digital circuits due to its low-voltage design. Most digital circuits in the industry are fabricated in the lowest technology possible for optimizing area, as well as performance. The low-voltage design of this work enables a low-power performance of the circuit, even with high-biasing currents.

Table 1: Literature Survey

Conference/ Year	Author/Corporate Author	V_{DD} (V)	Technology	Data rate	Max length of cable	Peak to peak jitter	Power Dissipation
ISSCC 1999	Shakiba, M. H.	5	0.8um/14 GHz Bipolar	1.5 Gbps	100m of Belden 8281	< 0.1UI	12.7mW
ISSCC 1996	Baker, Alan J.	5	0.8um/14 GHz BiCMOS	400 Mbps	300m of Belden 8281	< 0.1UI	
CICC 1998	Babanezhad, J. N.	3.3	0.4um CMOS	100 Mbps	125m CAT5 UTP cable	0.14 UI	65mW
ISCAS 1999	Hartman, G. P.	3.3	0.5um CMOS	143 Mbps	215m coaxial cable for SMPTE Std 259M		30mW
VLSI-DAT 2006	Lu, Jian-Hao	1.8	0.18um CMOS	3.125 Gbps	20m Belden 8219 cable	0.25 UI	14.8mW
Asian-SSCC 2008	Park, P	1.3	90nm CMOS	20Gbps	equalizes 7.5dB attenuation at 10GHz	0.32 UI	138mW
ISSCC 2005	Jaussi, J. E.	1.7 V	0.13um CMOS	8Gbps	17cm FR4 traces		280mW
ISSCC 2005	Gondi, S	1.2	0.13um CMOS	10Gbps	30 inches of FR4 traces	15ps	25mW
ISCAS 2011	Ganzerli, M, D.	1.1	45nm	13.5 Gbps	equalizes up to 18dB loss	0.4UI	8mW
CICC 2009	Shin, D. H.	1	90nm CMOS	12Gbps	72 inch RG-58 cable		1mW
This thesis	Agale, P.	1	45nm CMOS	3Gbps	240m RG-6 cable		15mW

2.3. Linear equalization technique

The linear equalization technique is implemented at the receiver, where the equalizer has a transfer function which is equal to the inverse of the transfer function of the cable. The equalizer implements peaking at higher frequencies and degenerated gain at lower frequencies to compensate for the cable losses as shown in Figure 2.4.

The frequency response represented by the blue line in Figure 2.4 is the response of a 40 m coaxial cable (Belden 1694A), and the frequency response depicted in red is the frequency response of the equalizer. As seen in the graph below, the equalizer response compensates for the low-pass characteristics of the coaxial cable. The equalizer curve was implemented in cadence using a differential amplifier as well as a Gilbert cell as a variable gain amplifier. Both these designs will be explained in detail in the following sections. The equalizer response curve was then exported from cadence to Matlab and plotted with the curve of the coaxial cable.

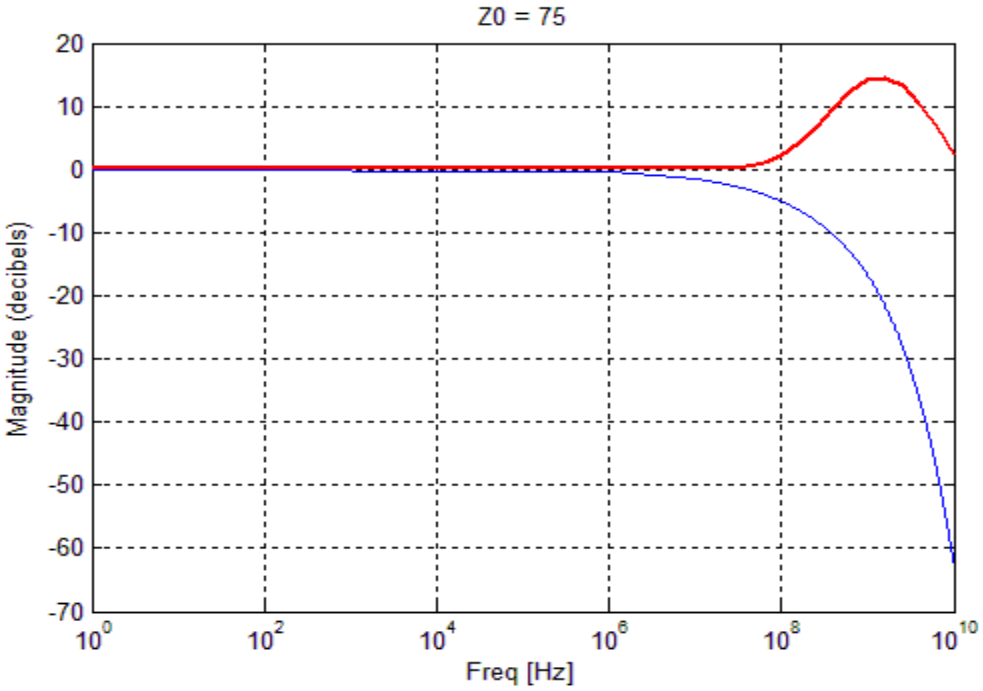

Figure 2.4: Frequency response of the cable and the equalizer

The design of gain-peaking circuits must satisfy many difficult requirements [13]:

1. Sufficient gain boost at high frequencies

2. Matching the inverse loss profile of the channel with reasonable tolerance

3. Minimal low-frequency loss to minimize the noise accumulation in cascaded stages and provide sufficient swings for the CDR

4. Well-behaved phase response to achieve a low jitter

5. Reasonable linearity so that the equalizer transfer function acts as the inverse of the channel loss profile

6. Small input capacitance

7. Tunability of the boost to allow adaptation

2.4. Design and implementation

CTLE is essentially a high-pass filter targeted to compensate the undesired low-pass effects of the channel. Multi-stage CTLE are the most inexpensive, low power option to implement, and can be adapted very well to the channel loss [11]. On the one hand, passive CTLE is constructed using only passive electronic components such as resistors, capacitors, and inductors. Therefore, high-pass response of passive CTLE is not coupled with signal amplification. On the other hand, active CTLE provides high-frequency gain boosting by means of real zeroes using RC degeneration. CTLE is normally designed and analyzed in the frequency domain; the most important step in CTLE design is to accurately place the poles and zeroes according to the inverse loss profile of the target channel [9].

This design of a continuous time linear equalizer aims at the design of a high-pass filter which provides high-frequency boost at 1.5 GHz. The longer the length of the channel, the higher is the attenuation at the operating frequency. Therefore, as the cable length gets longer, the amplifier needs to modify its gain to be higher to now equalize the data. From observing previous works, it was determined that multiple stages of the filter would prove efficient in providing the appropriate gain for a particular length of the cable with certain physical parameters. The proposed filter is divided into three stages, with each stage providing a gain of 20 dB at 1.5 GHz to compensate for the losses of the cable length of 80 m each. Therefore, the filter as a whole will be able to compensate the losses of the cable length from 0 to 240 m. Each filter stage will be able to adapt to a change of the

length of the cable or any other parameter which may cause a change in the frequency response of the cable. The gain of the variable gain amplifier can be controlled by a control voltage. This control voltage is converted to a current modulation by a linear transconductance amplifier. The linear transconductance amplifier thus modulates the control stage in the amplifier, which in turn varies the gain of the amplifier.

2.4.1. Design specifications

The desired peaking frequency for the continuous time linear equalizer is 1.5 GHz. The design has been implemented in the 45 nm CMOS technology, which is conducive for high-frequency designs.

$$Period = \frac{1}{Frequency} = 0.6667ns \tag{1.3}$$

The rise/fall time should be 1/10th of the period to allow for enough time for data read/data to be stable.

Rise time/Fall time = 1/10th of the period = 66.667 ps

Slew rate = 15 V/ns

CL = 40 fF (for next stage)

Parasitic capacitances for routing = 100 fF (assumption)

SR = Iss/CL

Iss = 1.5 mA

Therefore, the amplifier is designed with a bias current of 1.5 mA.

The bias current specification of the amplifier should be designed to be 1.5 mA. The biasing parameters are discussed in the section below, along with the design constraints of the amplifier. The continuous time linear equalizer has been designed in the CMOS 45 nm technology which has a supply voltage of 1 V. Since the equalizer circuit is placed in the front-end of the receiver in the transmission system, an equalizer fabricated in a technology with a supply voltage of 1 V can now be integrated with the receiver circuit and fabricated in the same technology. Designing the analog and digital components of the circuit with the same supply voltage helps in reducing an alternate power supply, which is used for the analog equalizer in most receiver circuits. This not only saves the total area of the design, but also enables integration of the design and thus improves cost and performance.

The first step in designing the amplifier is to find the biasing of the differential pair, such that the gain is optimum and the bandwidth extends beyond 1.5 GHz. Designing the amplifier in the CMOS 45 nm technology helped in extending the bandwidth to the GHz range. The circuit used to determine the bias point of the amplifier is shown in Figure 2.5. The gm of the amplifier was designed to be at a value of 15.43 mA/V. The V_{DS} voltage of the transistor was limited by the available headroom of the circuit, while the V_{GS} - V_{TH} (V_{OV}) voltage was designed to be within the saturation limits of the transistor.

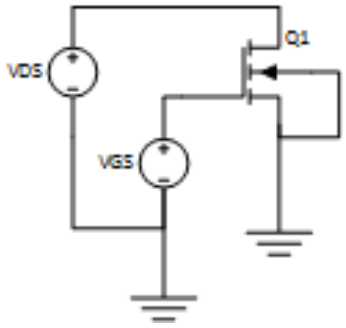

Figure 2.5: Differential amplifier (NMOS transistor) testbench schematic

The following graph in Figure 2.6 shows the current biasing of the differential pair NMOS transistor by varying the width of the transistor to match the current of 1.5mA. Due to this large biasing current, a parameter of the transistor that suffered was the output resistance (R_{ON}) or drain to source resistance of the amplifier as shown in Figure 2.7. The parameter called 'region' in Figure 2.7, which is of the value 2 indicates that the transistor is in saturation region.

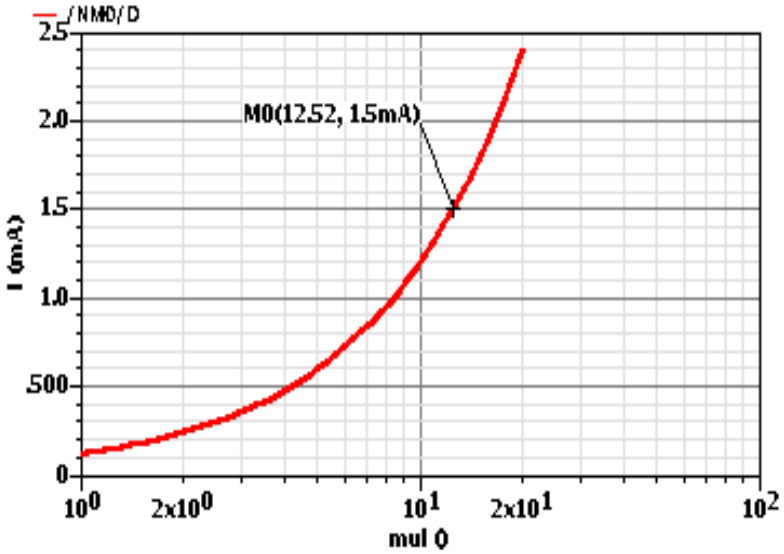

Figure 2.6: Differential amplifier (NMOS transistor) bias

Test	Output	Value	Spec
thesis_feb:char_gm_id_nmos:1	/NM0/D		
thesis_feb:char_gm_id_nmos:1	gm	15.37m	
thesis_feb:char_gm_id_nmos:1	region	2	
thesis_feb:char_gm_id_nmos:1	ron	199.9	
thesis_feb:char_gm_id_nmos:1	gds	2.175m	
thesis_feb:char_gm_id_nmos:1	Ids	1.5m	

Figure 2.7: Differential pair (NMOS transistor) parameters

A technique to improve the R_{OUT} (drain to source resistance) of the transistors is to increase the length of the transistor. It is shown below in Figure 2.8 that the gm*R_{OUT} product increases quite significantly with the length of the NMOS transistor. However, increasing the length of the differential pair transistors in the amplifier circuit in turn reduces the bandwidth of the amplifier. Hence, the length of the differential pair was maintained at 45 nm. The tradeoff during the design of the amplifier was between the gain and the bandwidth of the amplifier. The length of the tail transistor of the differential pair was increased to 1 um to increase the resistance of the transistor. A reduced resistance of the tail transistor would degrade the performance of the differential pair amplifier.

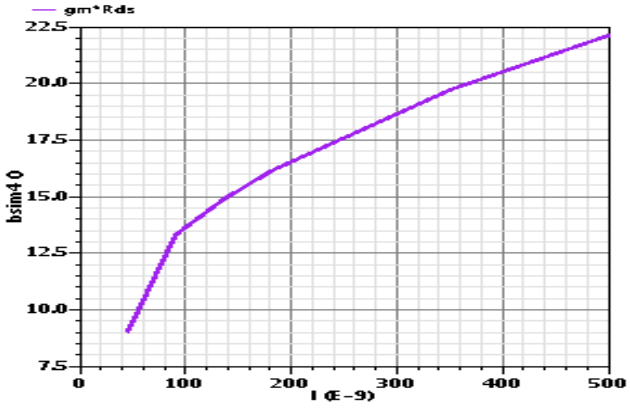

Figure 2.8: gm*Rout v/s length of the transistor

The high biasing current demands (3 mA and 6 mA) of this design resulted in an extremely large width of the tail transistors. Due to this, the R_{OUT} of the transistor could not be designed to a large enough value as to suit a constant current source. The length of the tail transistor was increased to be 1 um so as to increase the R_{OUT} of the transistor and avoid discrepancies in the circuit due to PVT variations.

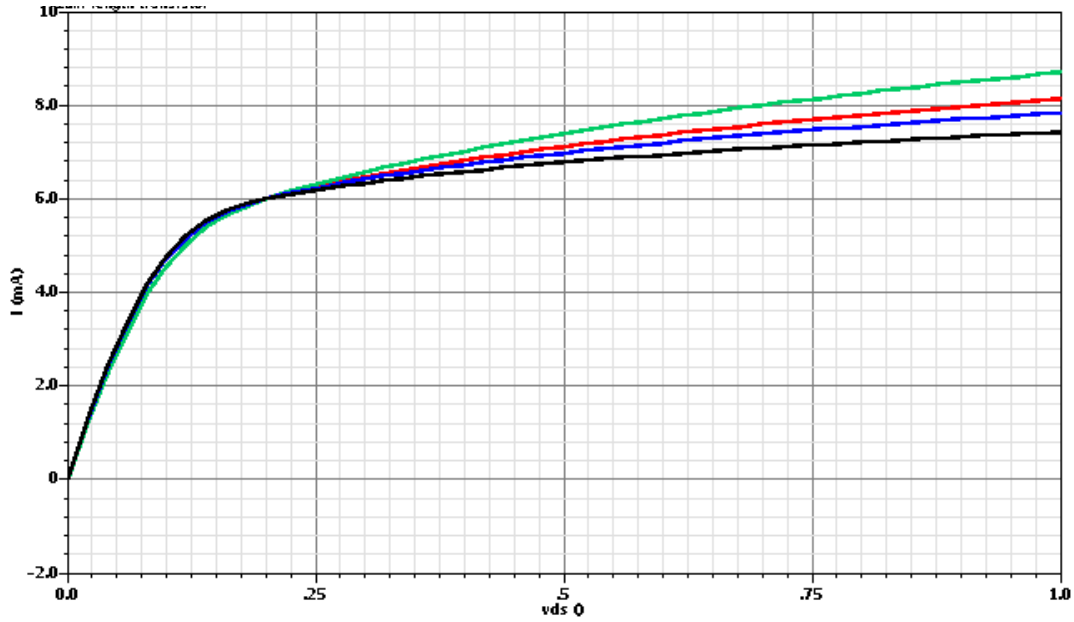

Figure 2.9: Transfer characteristics of different length (1 um, 0.5 um, 0.35 um, 0.18 um) transistors

As can be seen from the plot above, increasing the length of the transistor reduces the channel length modulation in the output curve. This makes the transistor more suited to be a tail transistor. The graph in black in Figure 2.9 is the output characteristic graph of a transistor of length 1 um. The graphs in blue, red, and green are the output characteristics of transistors of length 0.5 um, 0.35 um, and 0.18 um, respectively. Ideally, the tail transistor has very high impedance and almost no channel length modulation.

2.4.2. Variable gain amplifier

The first implementation of the variable gain amplifier is a differential pair amplifier, which is a first order system with a single pole and a zero and is shown in the Figure 2.10. The differential pair amplifier is designed to provide a variable gain by varying the tail current of the differential amplifier.

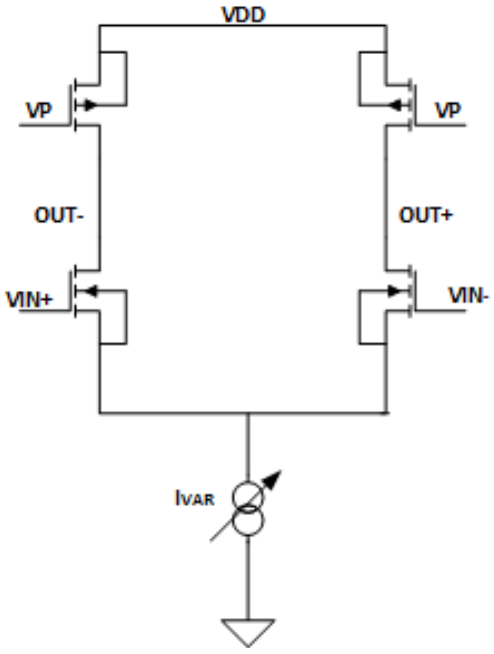

Figure 2.10: Differential pair amplifier

The graph in Figure 2.11 shows the linear relationship between the control voltage and the variable tail current. The maximum tail current is 1.5 mA which corresponds to the maximum gain of the amplifier. The Figure 2.12 shows the frequency response of the amplifier with variable gain, which corresponds to the different tail bias currents. The range of the amplifier varies from 14.17 dB to 0 dB, which can be controlled by varying the bias current of the amplifier.

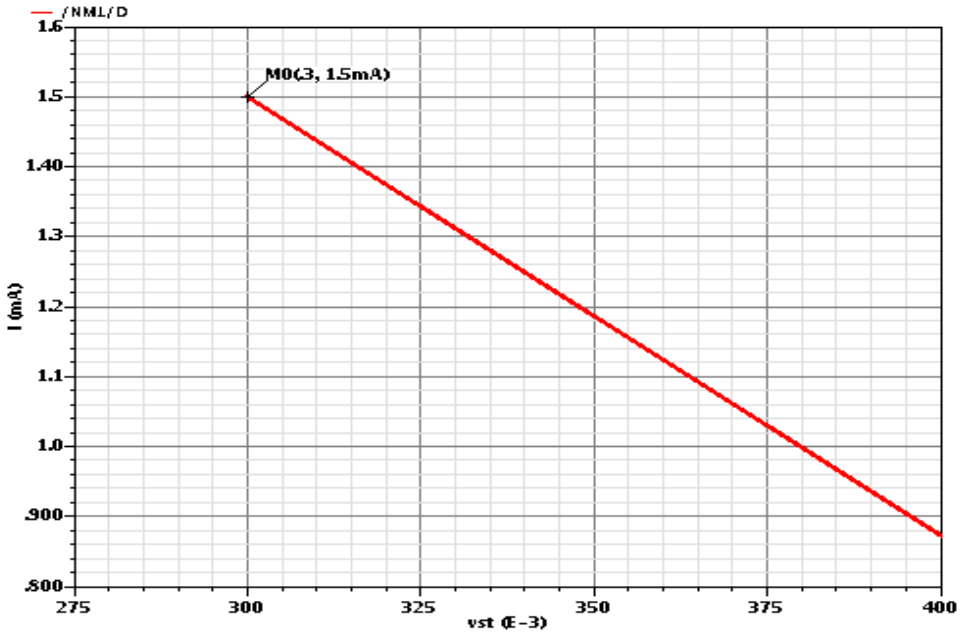

Figure 2.11: Linear relationship between the control voltage and the bias current

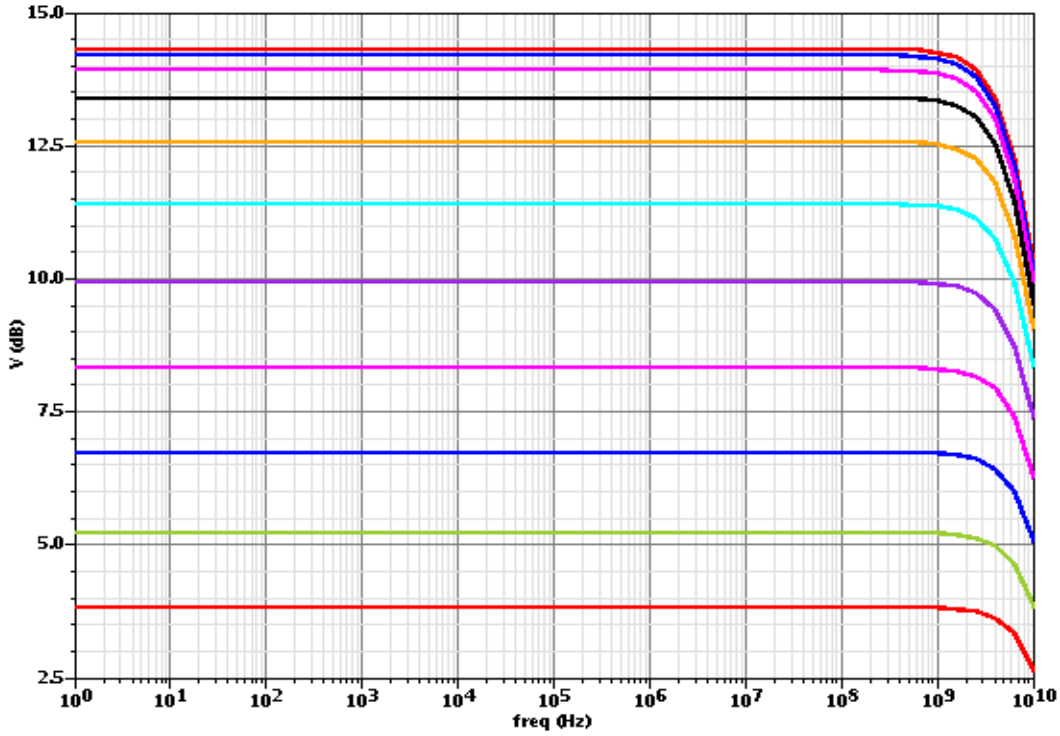

Figure 2.12: Frequency response of the amplifier showing variable gain

2.4.3. Source degeneration

The objective of source degenerating the amplifier is to provide a high-frequency boost, while at the same time attenuating the low-frequency gain. This technique is instrumental in achieving a transfer function of the amplifier which is the inverse of the transfer function of the cable. The analysis of the amplifier with source degeneration and the resulting response curves are shown in detail in this section.

Low frequency analysis: At low frequencies, the impedance of the capacitor (Xc) is high enough that the capacitor can be assumed to be an open circuit. In this case, the resistor does the job of degenerating the gain of the amplifier at low frequencies as stated in Equation 1.4.

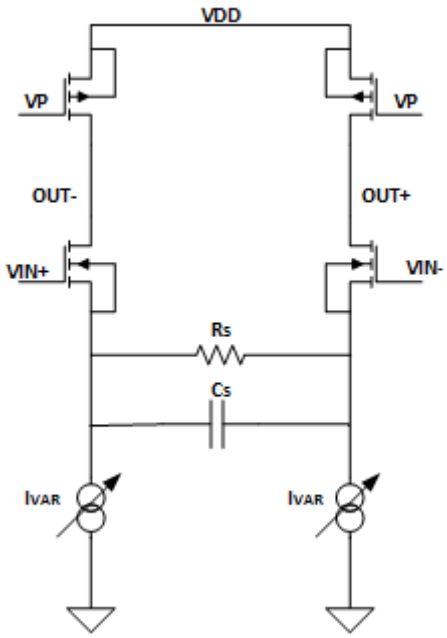

Figure 2.13: Differential pair with source degeneration

$$Gain = \frac{g_m R_L}{1 + g_m R_S} \tag{1.4}$$

If $R_S >> 1/gm$;

$$Gain = \frac{R_L}{R_S \parallel R_{TAIL}} \tag{1.5}$$

The gain at the lower frequencies is independent of the gm of the amplifier and becomes a function of R_L and R_S. In this case, gm = 15.08 mA/V, and R_S = 2.5 KΩ, and since 1/gm = 66.313 V/A; $R_S > 1/gm$. However, the source resistance is in parallel with the tail transistor resistance, which limits the value of the degenerating resistance ($R_S \parallel R_{TAIL}$). Another issue that arises is that the PMOS load resistance does not stay constant with variable gain values, which results in variable DC gain values. The DC or low frequency gain has been expressed in the Equation 1.5.

High frequency analysis: At high frequencies, the impedance of the capacitor becomes low enough to act as a short circuit and short the source resistance (R_S) in the amplifier circuit. At this point, the differential pair can exhibit the qualities of an amplifier, and thus we can achieve high-frequency gain. The max gain of the differential circuit is gm*R_L as shown in Figure 2.14, and the location of the pole as stated in the Equation 1.6 can be approximated to:

$$w_{p1} = \frac{g_m}{C_S} \tag{1.6}$$

The zero and the pole location can be manipulated by appropriately changing the value of the degenerating resistor (R_S) and the capacitor (C_S). The frequency response represented by the black line in Figure 2.14 is the ideal frequency response needed by the equalizer. The peak should occur at the operating frequency of the receiver. The location of the zero can be changed by changing the value of the source capacitance and thus the bandwidth of the amplifier can be altered as shown in Figure 2.18.

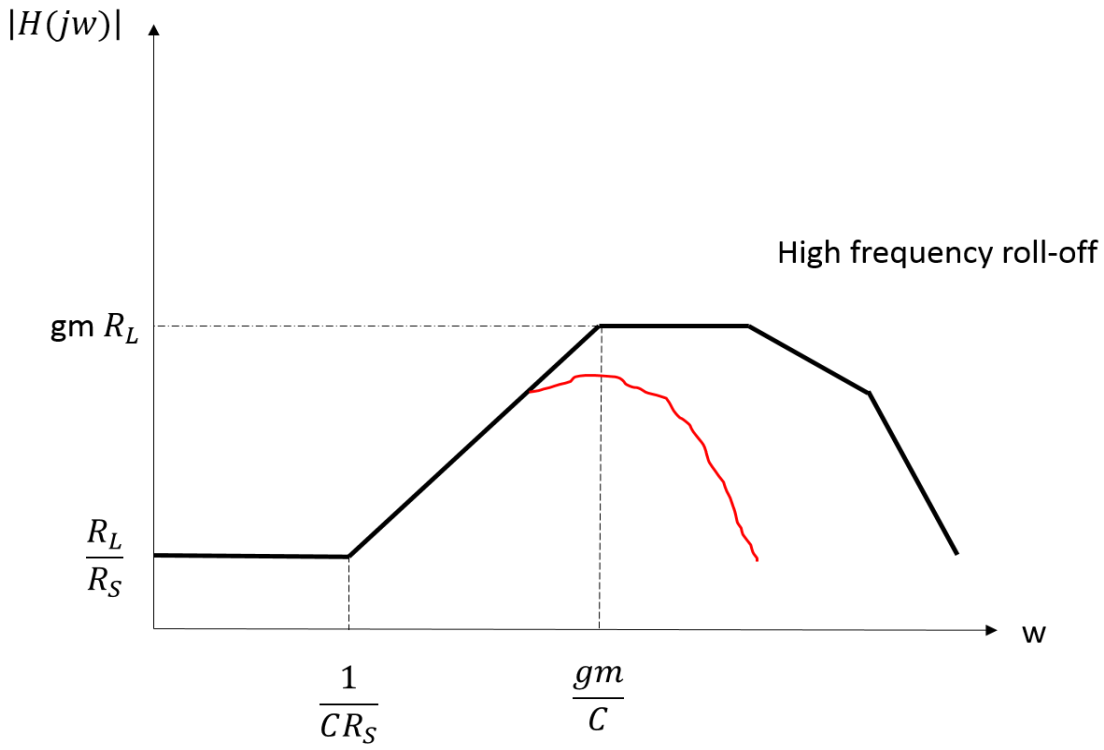

Figure 2.14: Frequency response of a first order system

Determining the transfer function of the circuit will give an insight into the placement of the pole and the zero of the circuit and thus determine the peaking frequency of this first order CTLE. The peaking frequency can be manipulated by varying the value of the

degenerating capacitor and the low frequency gain can be varied by varying the value of the degenerating resistor.

$$H(s) = \frac{g_m R_L}{1 + g_m Z_S} \tag{1.7}$$

$$Z_S = \frac{R_S}{1 + s C_S R_S} \tag{1.8}$$

$$H(s) = \frac{g_m R_L [1 + s C_S R_S]}{1 + g_m R_S + s C_S R_S} \tag{1.9}$$

If $R_S \gg 1/gm$;

$$Gain = g_m R_L \left[s C_S + \frac{1}{R_S} \right] \tag{1.10}$$

The gain will roll-off at high frequencies; it may not even reach a high gain of $gm*R_L$ due to parasitics of the amplifier, but may roll-off at a smaller gain as depicted by the red curve in Figure 2.14. The above calculations are of an ideal perspective, to determine the location of the zero and the pole of the first-order CTLE in a simplistic way. However, as shown in the Figure 2.14, the frequency response does roll-off and this shows that the transfer function does include another pole.

$$w_{P2} = \frac{1}{R_L C_L} \tag{1.11}$$

This pole capacitance should practically also include the parasitic capacitances of the transistor, for example, the gate to drain capacitance (C_{GD}) and the bulk to drain

capacitance (C_{BD}), but for now those parasitics have been excluded. The complete transfer function of the circuit can therefore be summarized as:

$$H(s) = \frac{g_m}{C_L} \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + \frac{g_m R_S}{2}}{R_S C_S} \right) \left(s + \frac{1}{R_L C_L} \right)} \tag{1.12}$$

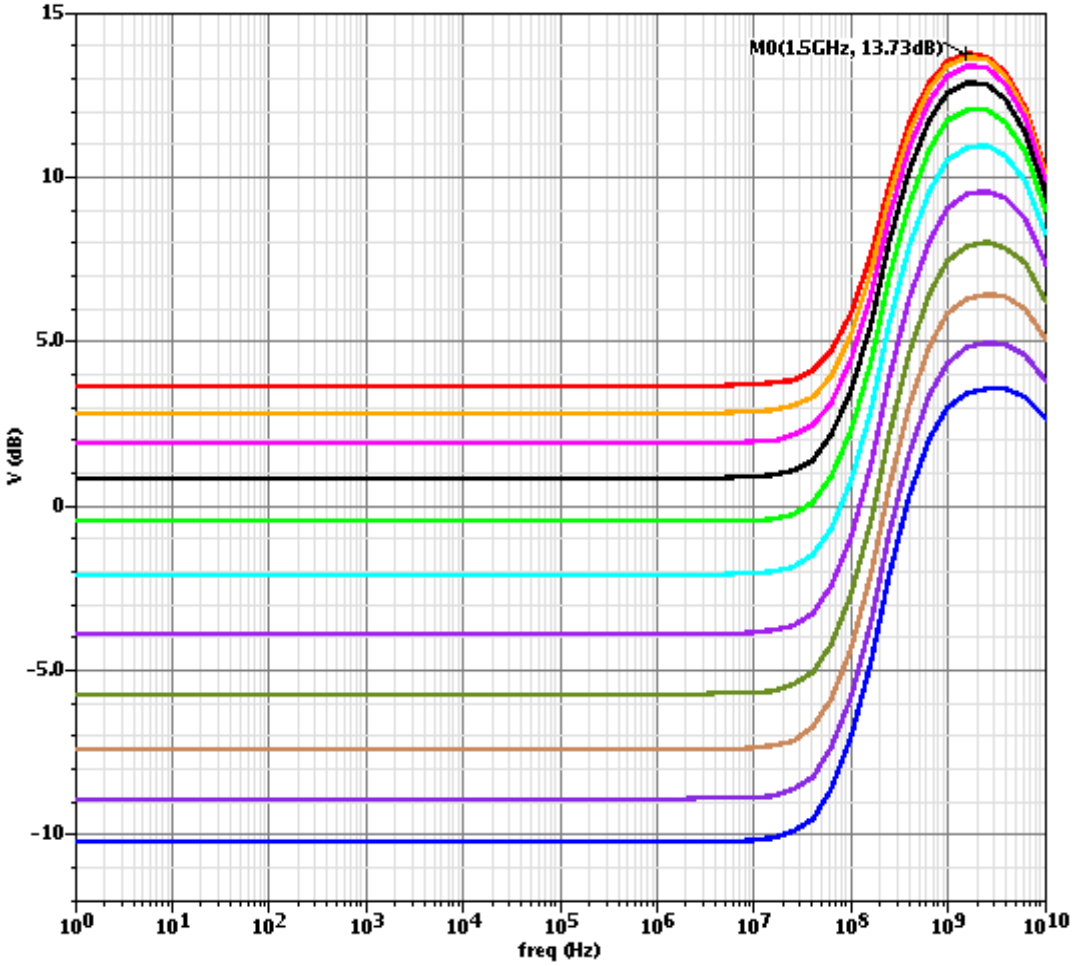

Figure 2.15: High-frequency variable peaking in the response of a differential amplifier

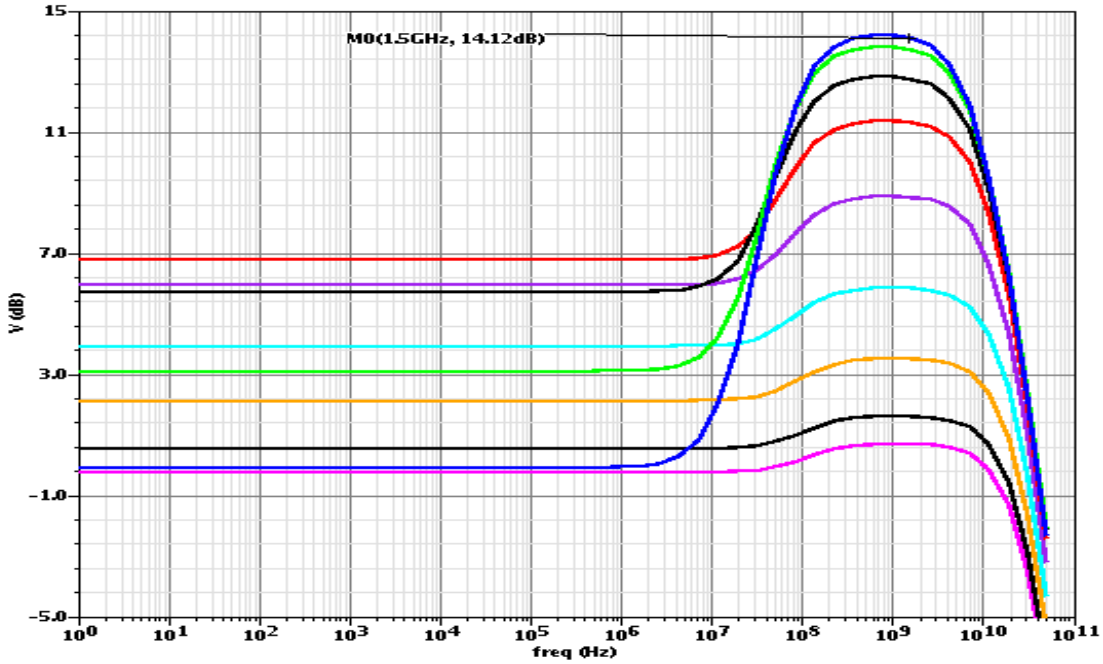

Figure 2.16: Variable gain obtained by varying the control voltage

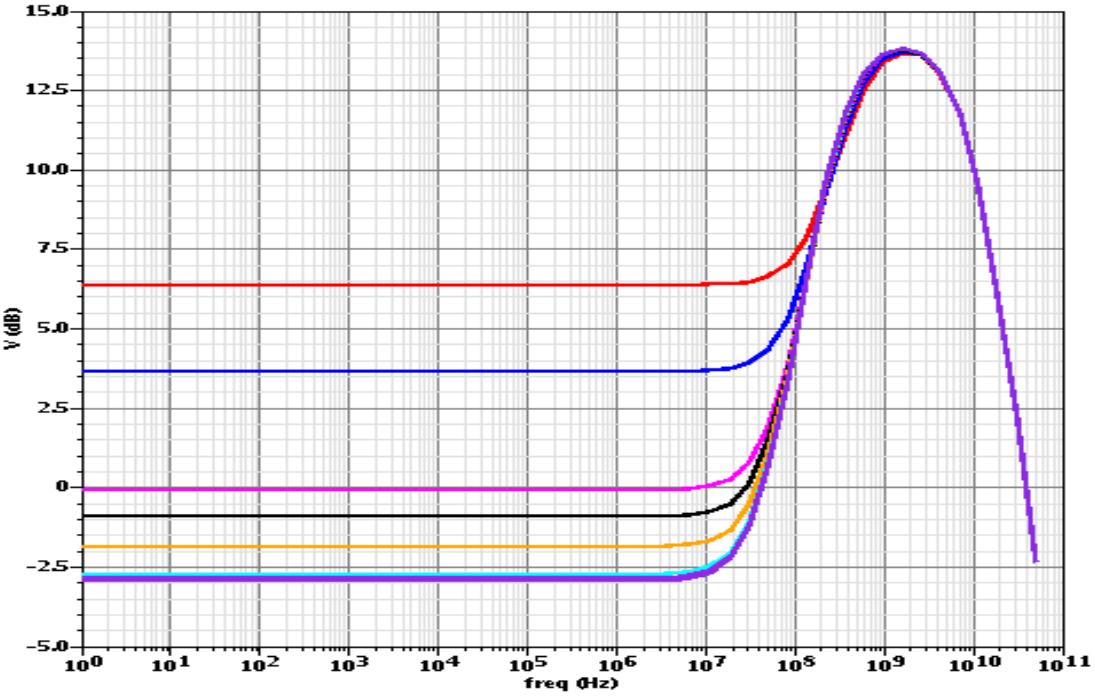

Figure 2.17: Low frequency gain variation by changing the source resistance

The frequency response graphs in Figure 2.15 and Figure 2.16 have been generated by varying the control voltage, which in turn varies the bias current of the differential pair.

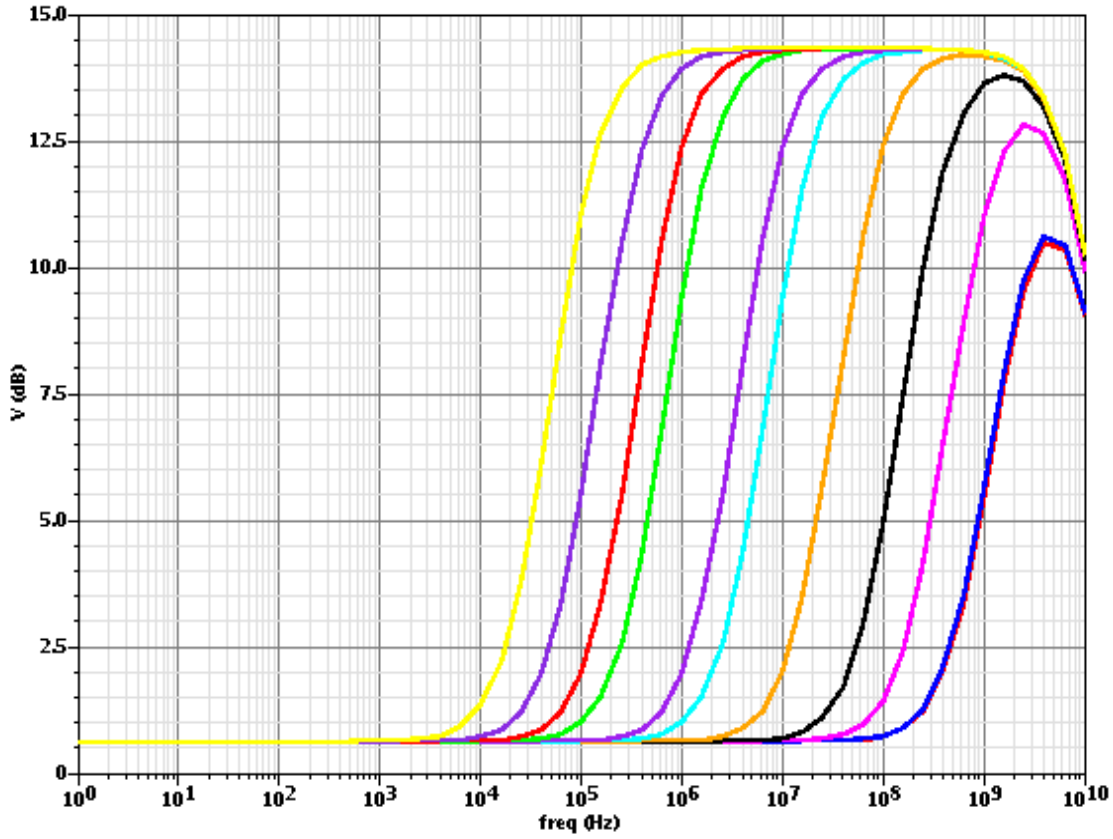

Figure 2.18: Frequency response of the differential amplifier with a variable bandwidth

By keeping the control voltage at a constant level, and varying the source capacitance, the graphs in Figure 2.18 can be obtained. A variation in the value of the source capacitance varies the bandwidth of the amplifier and to some extent even varies the gain of the amplifier. The graphs in Figure 2.17 can be obtained by varying the source resistance values, which varies the gain of the amplifier at low frequencies. This is the same as having a source degenerated common source amplifier, where the value of the source resistance divides the gain of the amplifier. Although having a row of resistors in

the circuit can consume a lot of area, some applications do require low frequency gain variation.

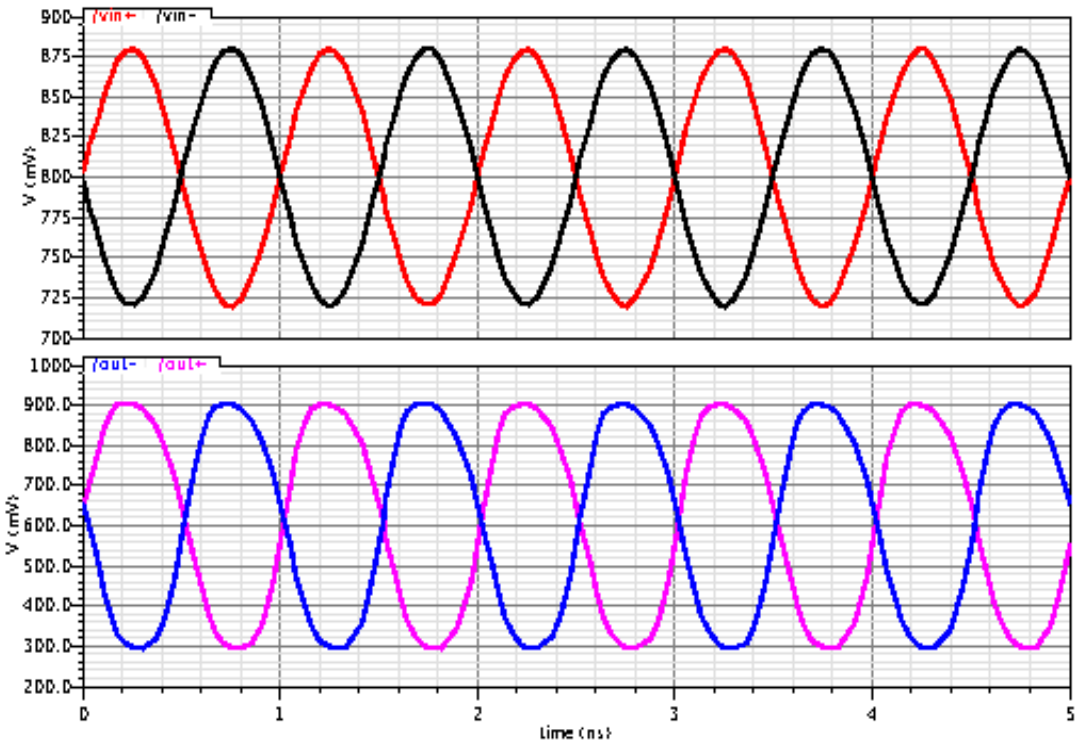

Figure 2.19: Transient response of the input and output signals from the amplifier

The graphs displayed in red and black in the Figure 2.19 are the differential input signals to the amplifier. The input signals are of the magnitude of 100 mV and are opposite in phase as they are differential signals. The graphs in the second half of Figure 2.19 are the output differential signals of the amplifier. The output differential signals can be seen to be amplified in nature as compared to the input differential signals.

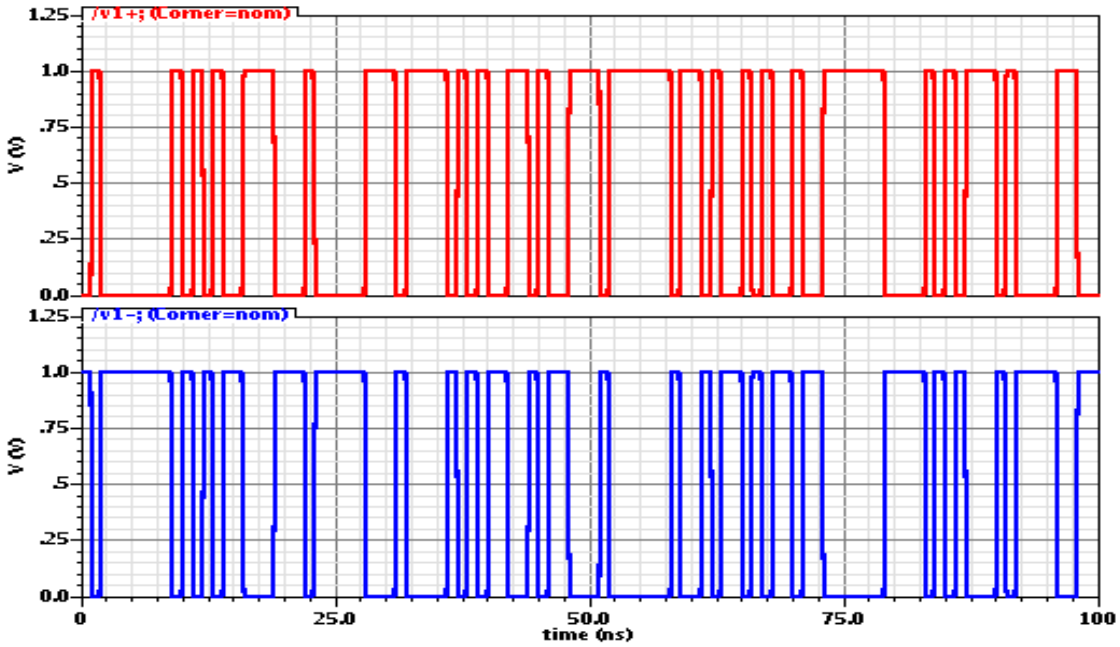

Figure 2.20: Differential PRBS data in cadence (input to the cable)

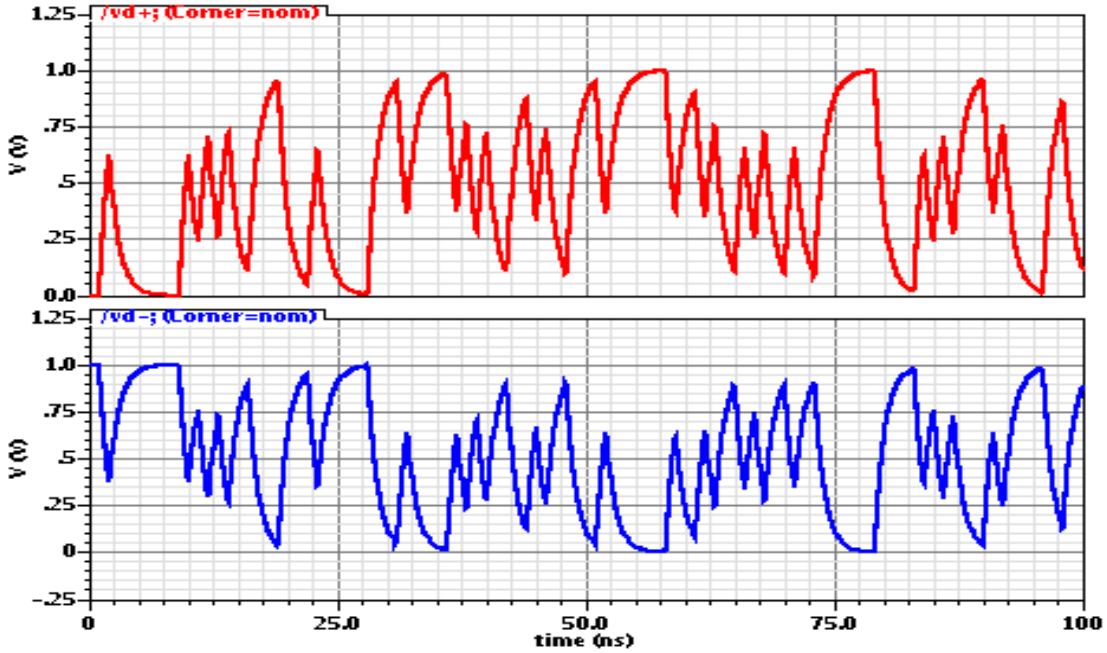

Figure 2.21: Distorted, differential output signals, received from the channel

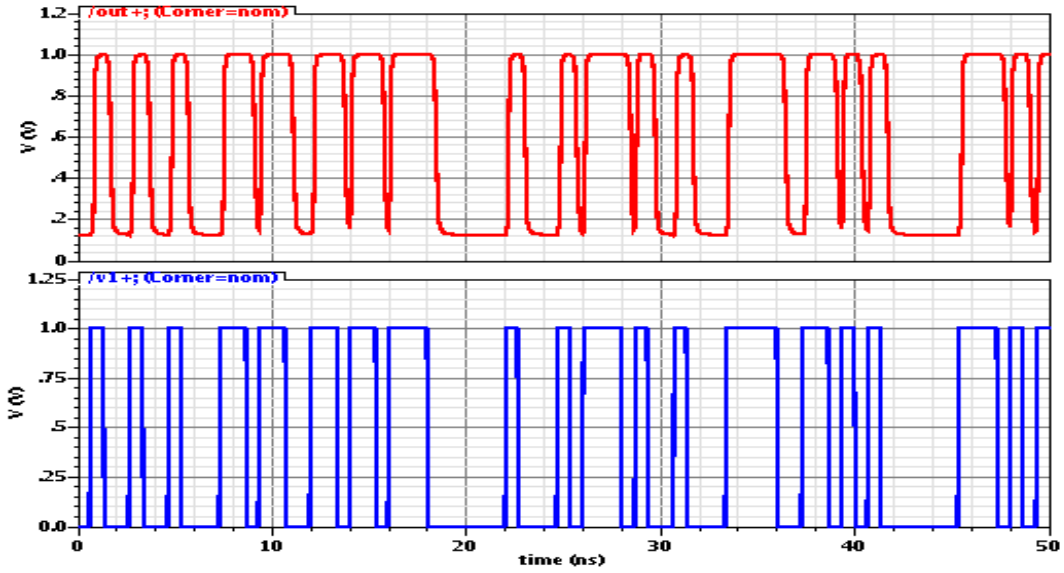

Figure 2.22: Equalized data (in red) and the ideal PRBS data (in blue)

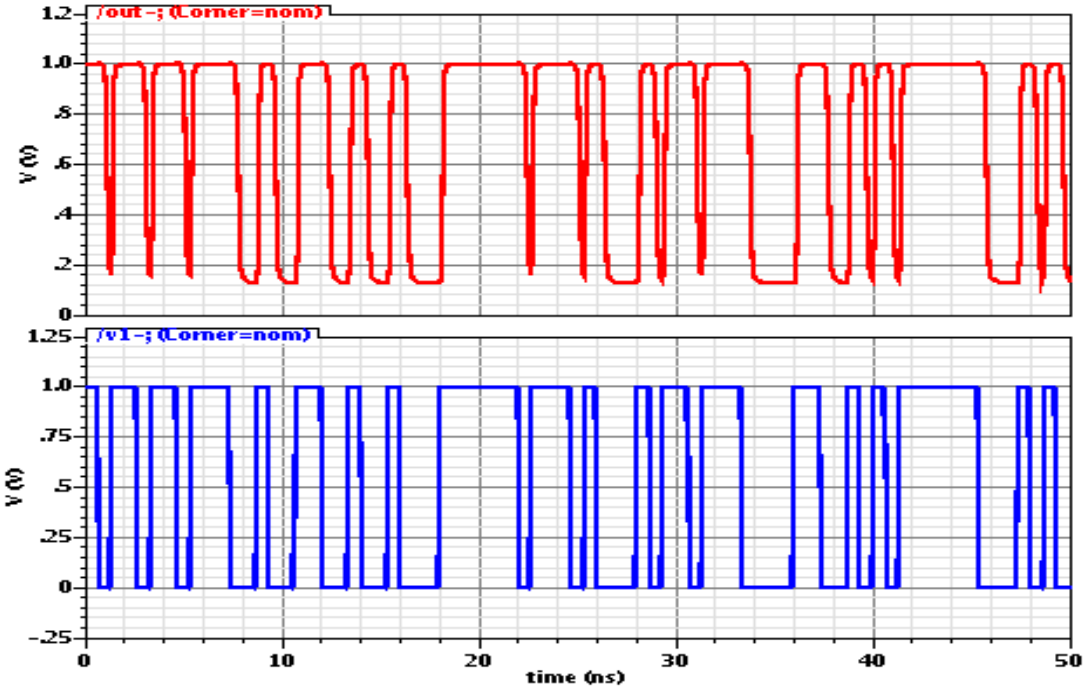

Figure 2.23: Equalized data (in red) of OUT- and the ideal PRBS data (in blue)

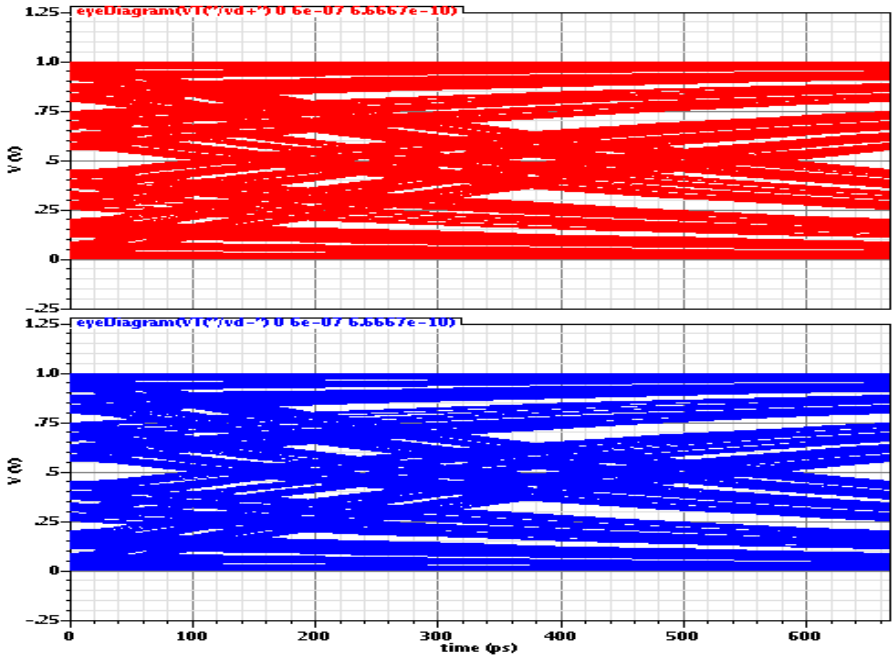

Figure 2.24: Eyediagram of the distorted data shown in Figure 2.21

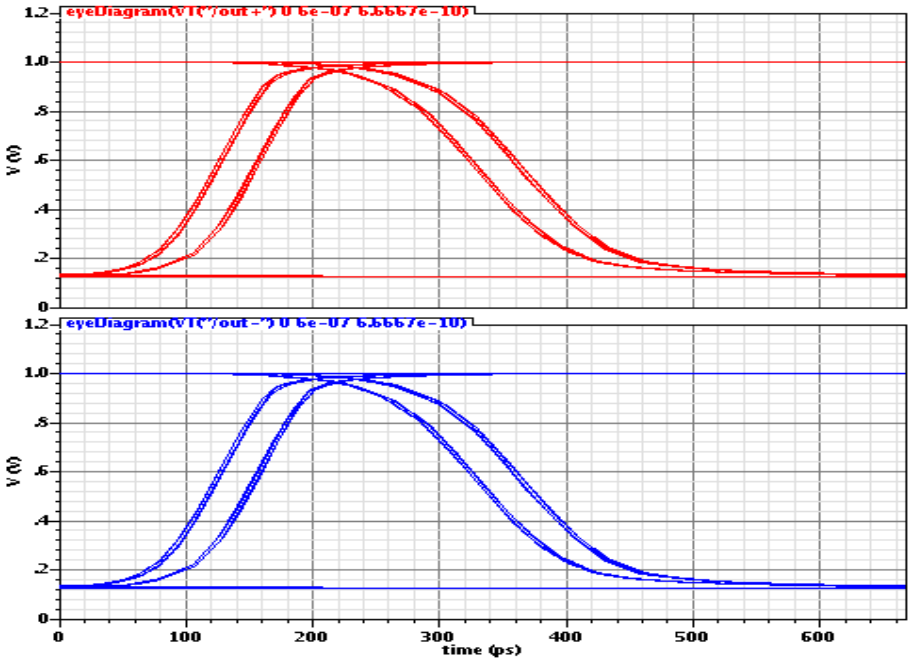

Figure 2.25: Eyediagram of the equalized data shown in Figure 2.22 and 2.23

2.4.4. Gilbert cell

The Gilbert cell proves to be a useful circuit when the gain of the amplifier is to be varied from a negative value to a positive value. This can be done by using two differential amplifiers that amplify the input by gains having the opposite phase i.e.:

$$A_{V1} = \frac{V_{OUT1}}{V_{IN1}} = -gm_1 \times R_1 \tag{1.13}$$

$$A_{V2} = \frac{V_{OUT2}}{V_{IN2}} = gm_2 \times R_2 \tag{1.14}$$

where gm_1 and gm_2 denote the transconductance of each amplifier in equilibrium.

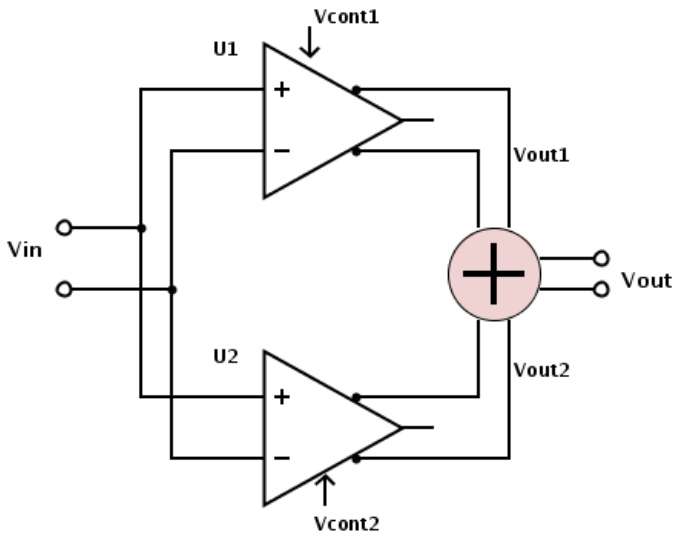

Figure 2.26: Representation of the Gilbert cell

From Figure 2.26,

$$V_{OUT} = V_{OUT1} + V_{OUT2} \tag{1.15}$$

$$V_{OUT} = A_1 \times V_{IN} + A_2 \times V_{IN} \tag{1.16}$$

where, A_1 and A_2 are controlled by V_{CONT1} and V_{CONT2}.

The cross-coupling of the two differential amplifiers allows the gain to range from a negative gain value to a positive gain value, depending on the individual gains of each of the differential amplifiers. Since the differential amplifiers have the same gain when $V_{CONT1} = V_{CONT2}$, the gain of the Gilbert cell is equal to zero. In this design, the biasing current is equal to 1.5 mA and, therefore, each branch is designed to carry a current of 1.5 mA.

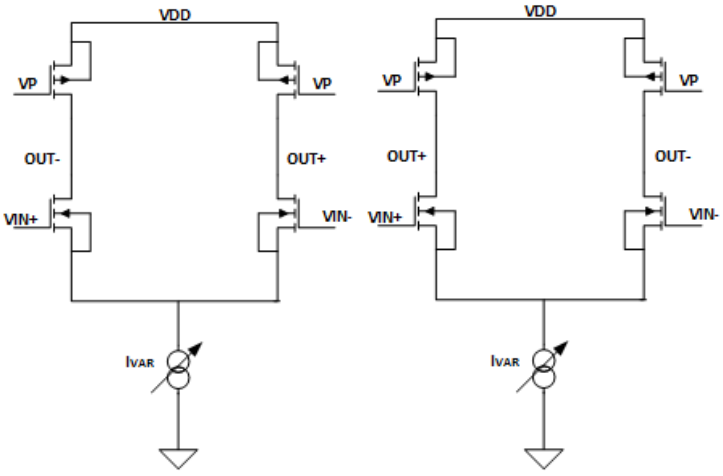

Figure 2.27: Differential amplifiers with a gain of the opposite polarity

Now, in Figure 2.27:

$$V_{OUT1} = R_1 \times I_{D1} - R_1 \times I_{D2} \tag{1.17}$$

$$V_{OUT2} = R_3 \times I_{D3} - R_4 \times I_{D4} \tag{1.18}$$

Therefore, we can conclude that:

$$V_{OUT} = R_D \times (I_{D1} + I_{D4}) - R_D \times (I_{D2} + I_{D3}) \quad (1.19)$$

The above equation becomes true assuming that $R_1 = R_2 = R_3 = R_4 = R_D$

So, instead of adding V_{OUT1} and V_{OUT2}, we can just short the drains of Q_1 and Q_4 to combine ID_1 and ID_3 and short the drains of Q_2 and Q_3 to combine ID_2 and ID_4.

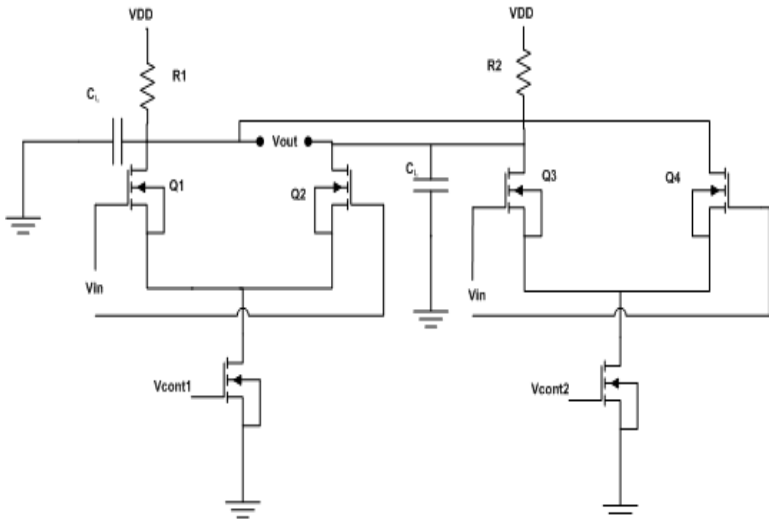

Figure 2.28: Circuit implementation of $V_{OUT} = V_{OUT1} + V_{OUT2}$

In Figure 2.29, if I_1 and I_2 vary in different directions, so do A_{V1} and A_{V2} and, therefore, the circuit acts as a variable gain amplifier. The resistors are replaced with PMOS transistors for higher swing and better gain. The available headroom voltage limits the resistance value of the passive resistors and this in turn limits the gain of the amplifier. The tail currents are replaced with NMOS transistors whose currents will be controlled by V_{CONT1} and V_{CONT2}. The advantage of using a Gilbert cell is that the gain of the variable gain amplifier can vary from a positive gain value to a negative gain value. However, in this design, the need for implementing a negative gain does not exist and, therefore, one of

the branches can be made to have a more positive gain than the other to maintain the gain of the amplifier on the positive side.

When the currents in both the differential tail transistors are the same, the gain of the overall circuit should be zero. As the tail current will modulate, the gain of the circuit should be equal to the difference of the gain of the two amplifiers. To make the relationship between the control voltage and the gain of the amplifier more linear, a linear transconductance amplifier has been implemented before the Gilbert cell, which converts the change in the control voltage to a change in the bias current of the Gilbert cell. The linear transconductance amplifier output is connected to the tail transistors in Figure 2.29 (Q_5 and Q_6).

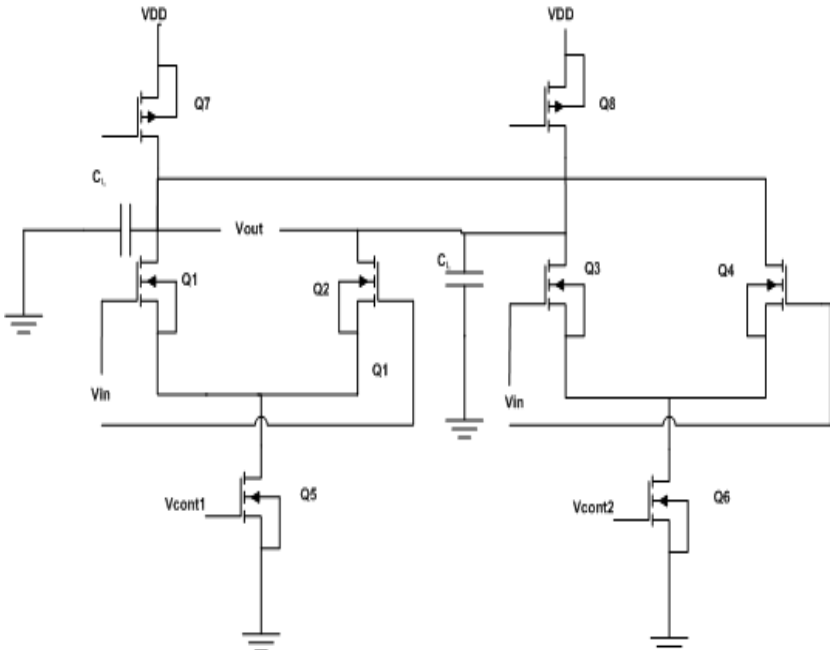

Figure 2.29: Cross-coupled differential amplifiers with an active load

The load to this amplifier is the gate of the transistor of the next amplifier stage. This can be mimicked by placing a simple common source amplifier as the next amplifier stage and simulating the Gilbert cell as the test circuit.

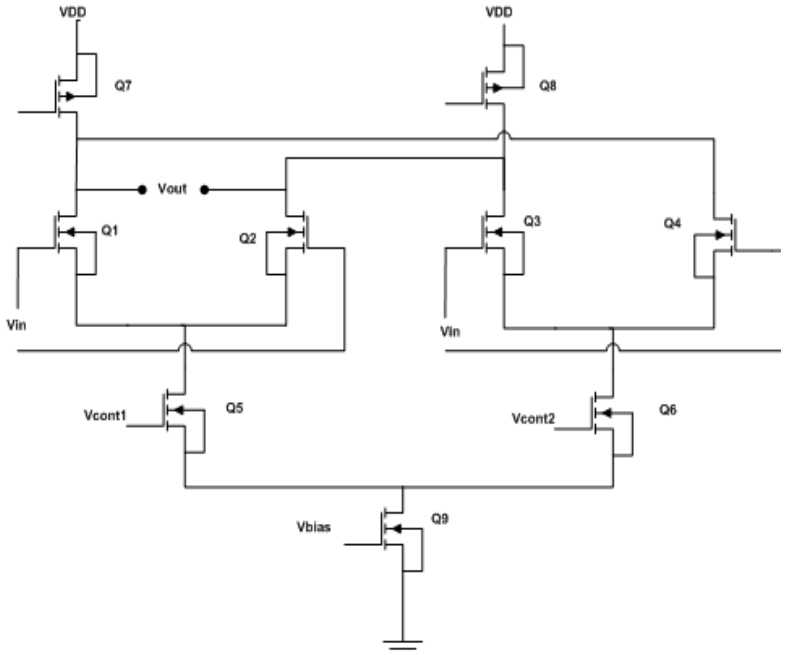

Figure 2.30: Gilbert cell with a voltage control stage for gain control

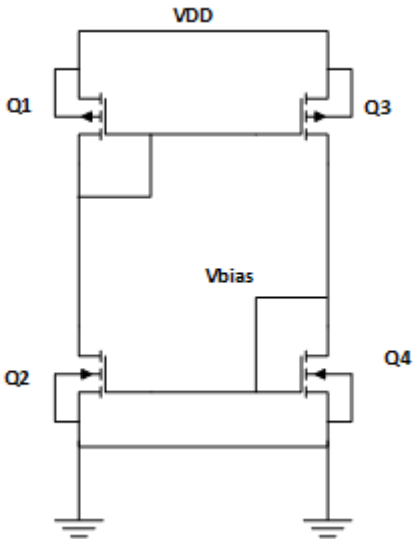

Figure 2.31: Gilbert cell tail bias circuit

The Gilbert cell circuit, shown in Figure 2.30 is implementing the variable gain amplifier using the cross-coupled differential amplifier topology. The V_{CONT} stage helps in varying the gain of the individual amplifier stages and thus varies the overall gain of the amplifier circuit. The tail bias circuit is shown in Figure 2.31, which is designed to bias the tail transistor for a drain current of 6 mA. The V_{CONT1} and V_{CONT2} bias voltages are decided by the linear transconductance amplifier, which acts as the gain control stage. The control voltage, which is applied to the gain control stage, is decided by the amplitude of the input data stream which comes in via the channel (coaxial cable). One of the main issues, while working with this design, was the resistance of the tail transistors, which was as low as 200 Ω due to the large width of the transistors. The large width of the transistor is contributed to a large bias current needed in the tail transistor (6 mA) and the voltage headroom limits the increases in the overdrive (V_{GS} - V_{TH}) voltage. The frequency response graphs for the circuit in Figure 2.30 are displayed in Figure 2.32.

The Gilbert cell provides a gain of 13.96 dB at the operating frequency of 1.5 GHz for a load of 100 fF. The different colored graphs in Figure 2.32 have been obtained by varying the V_{CONT1} and V_{CONT2} control options in the circuit of the Gilbert cell. To obtain high-frequency peaking, a source degenerating resistor and capacitor will be used. The maximum gain of the Gilbert cell is not more than 15 dB, which may prove insufficient to compensate for a cable length of 80 m. A second stage common source amplifier can be used to further amplify the gain of the amplifier and compensate for 80 m cable length as shown in the Figure 2.38. A gain of around 20 dB is needed to compensate for a cable length of 80 m.

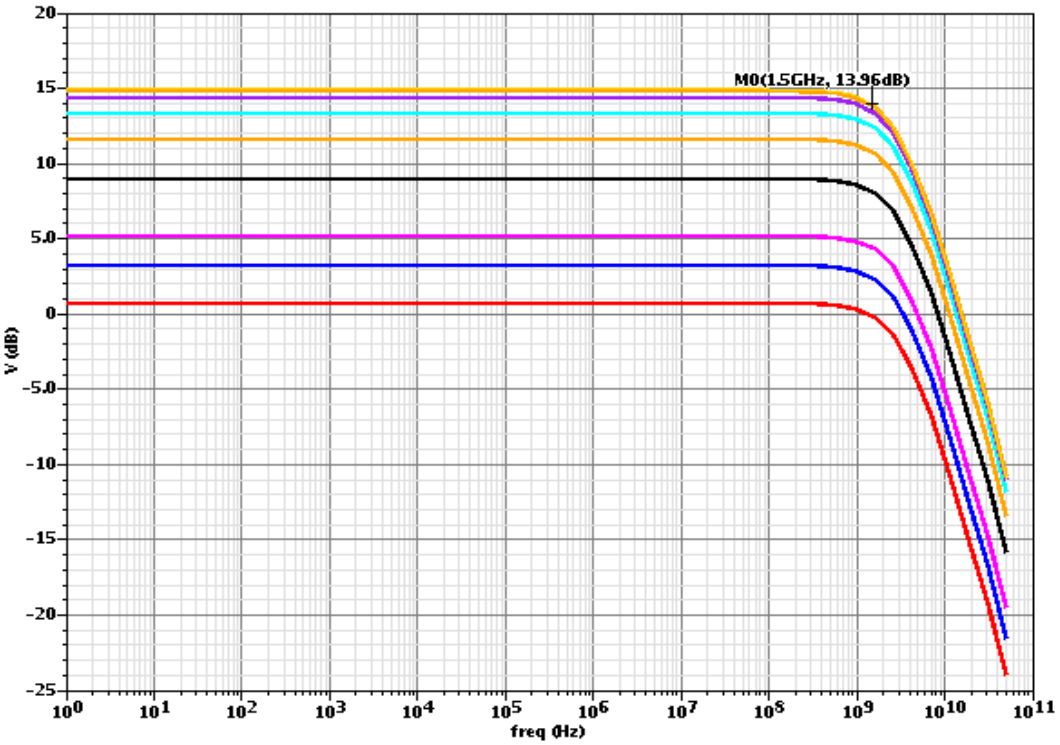

Figure 2.32: Variable gain frequency response of the Gilbert cell

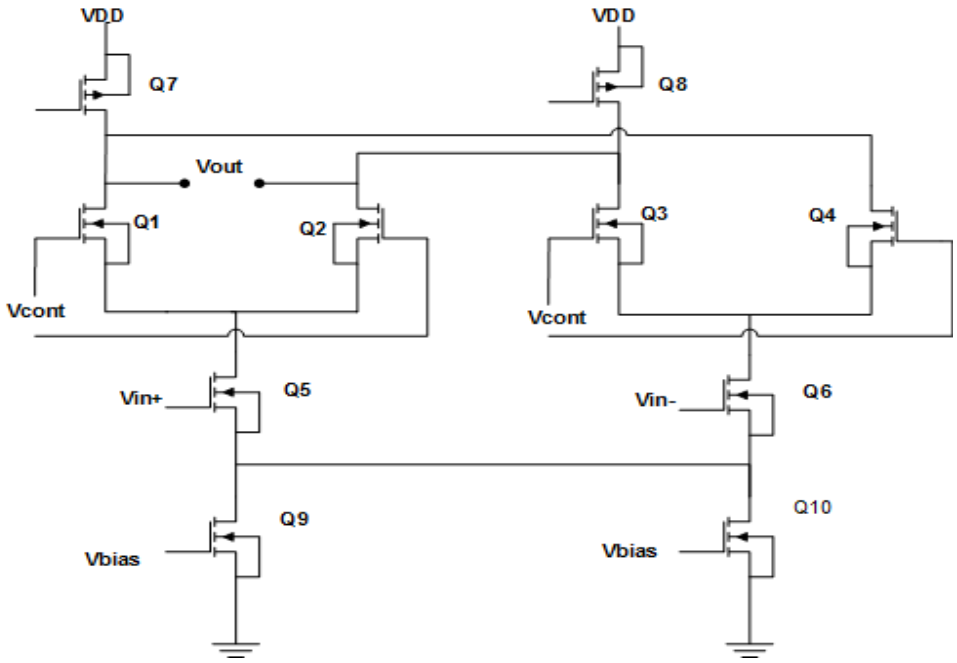

Figure 2.33: Gilbert cell with the control stage as the input pair

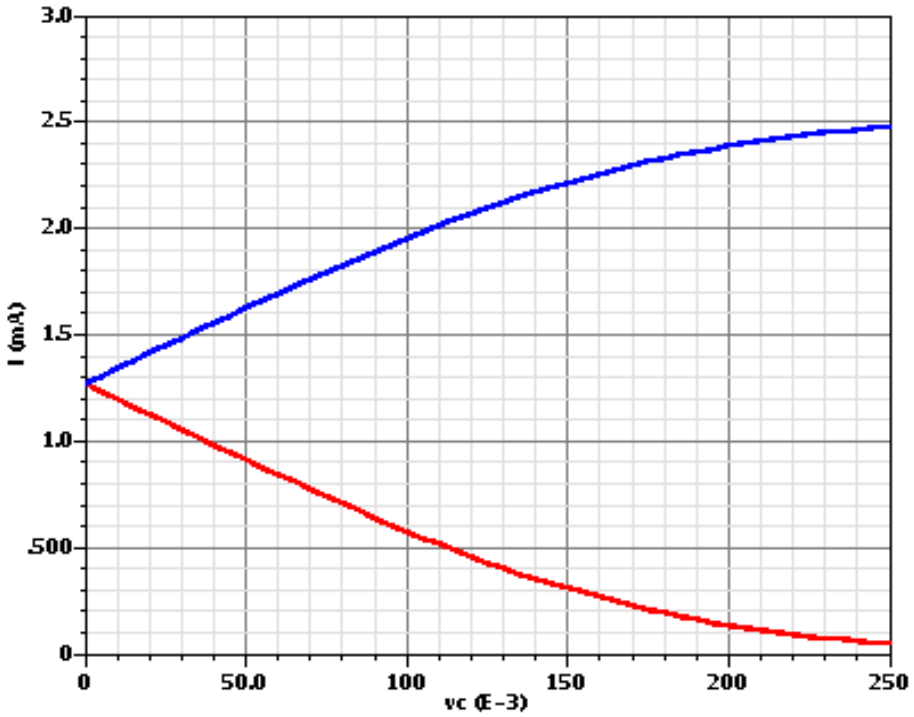

Figure 2.34: Linear current variation by steering the V_{CONT} voltage

The two current graphs in Figure 2.34 are of the drain currents of the transistors Q_1 and Q_3. By changing the V_{CONT} voltage, the current in the branches can be steered such that one of the branches has a higher current flow than the other. This difference in the bias currents causes the gain of one of the differential amplifiers to have a positive magnitude, while the other differential amplifier will have a negative magnitude. Since the gain of the Gilbert cell is the difference of the two differential amplifiers, it will depend on the fluctuation of the gains of each of the differential amplifiers. This gain can be increased or decreased based on the variation of the bias currents in the branches of the Gilbert cell. The higher the difference between the bias currents of the two branches of the Gilbert cell, the greater the gain of the Gilbert amplifier and vice versa.

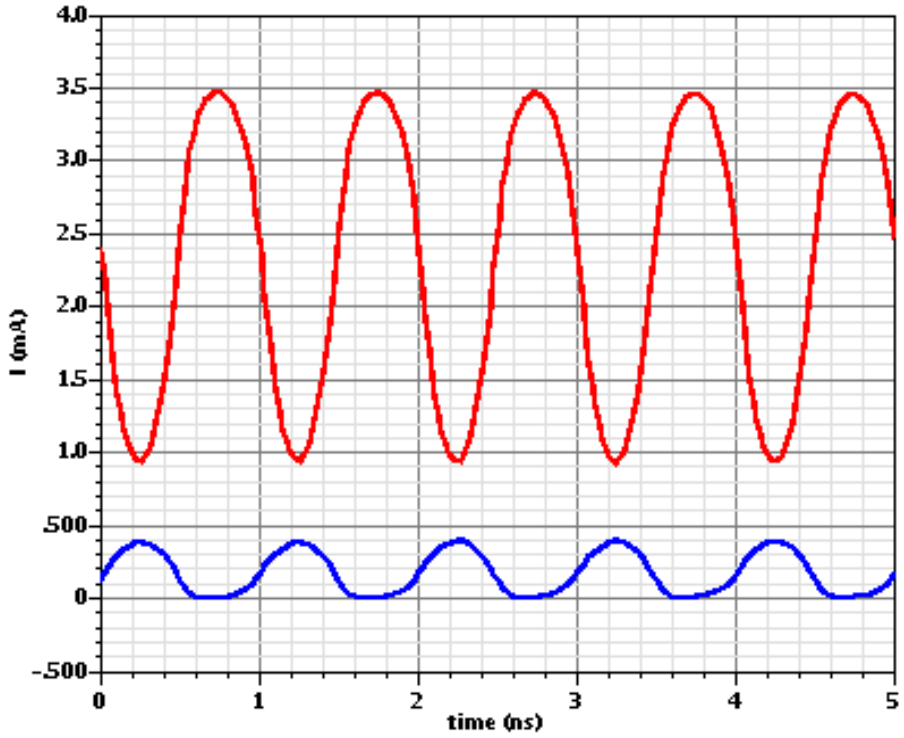

Figure 2.35: Current modulation when one of the Gilbert cell branches has a higher current bias than the other

The transient currents in Figure 2.35 are the drain currents of the transistors Q_1 and Q_3. The transistors are biased at two different current states and the modulation of the two currents is due to the AC input on the transistors. The transistors Q_1 and Q_3 are common gate amplifiers and this cascoded structure in the Gilbert cell increases the gain of the amplifier.

$$GCS = -gm5 * (rds5 \parallel \frac{rds1 + rds7}{1 + gm1 * rds1}) \tag{2.15}$$

$$GCG = -gm1 * (rds1 \parallel rds7) \tag{2.16}$$

$$GV = -gm5 * gm1 * (rds5 \parallel \frac{rds1 + rds7}{1 + gm1 * rds1})(rds1 \parallel rds7) \quad (2.17)$$

Eqn. 2.15, 2.16, and 2.17 are the gain equations of the common source, common gain amplifier, and the cascode amplifier respectively. The transistor Q_5 acts as the common source amplifier, Q_1 is the common gate amplifier, and Q_7 is the PMOS load as shown in Figure 2.36.

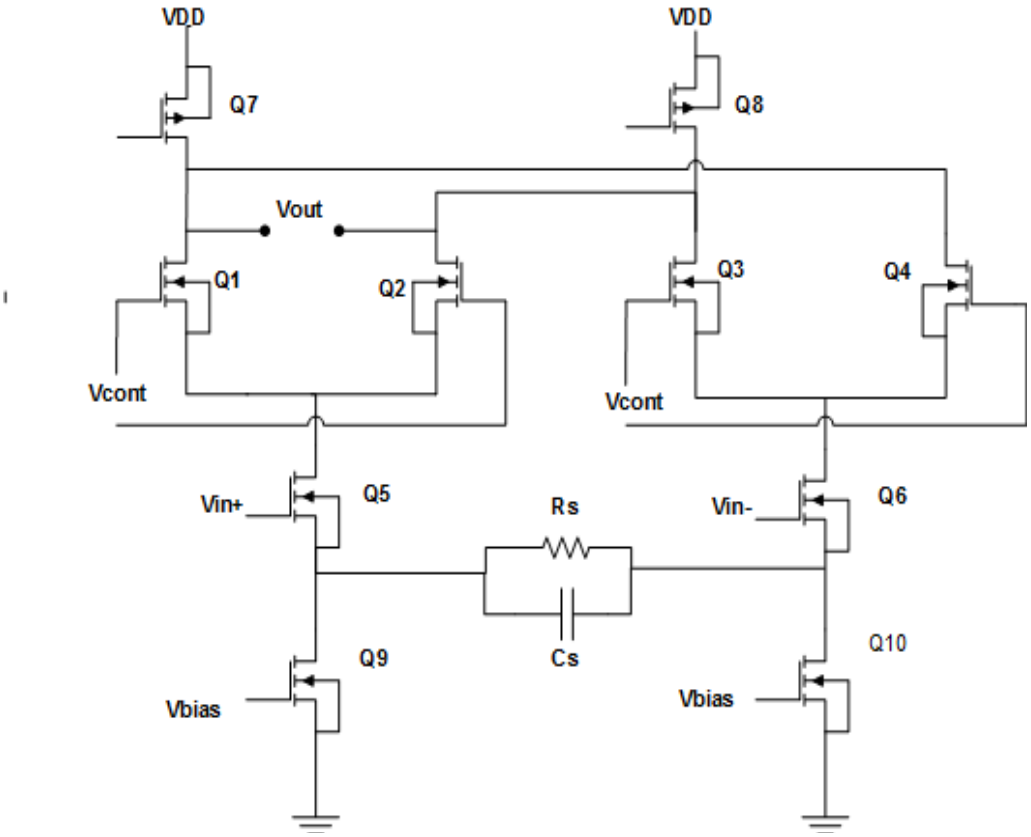

Figure 2.36: Gilbert cell circuit with source degeneration

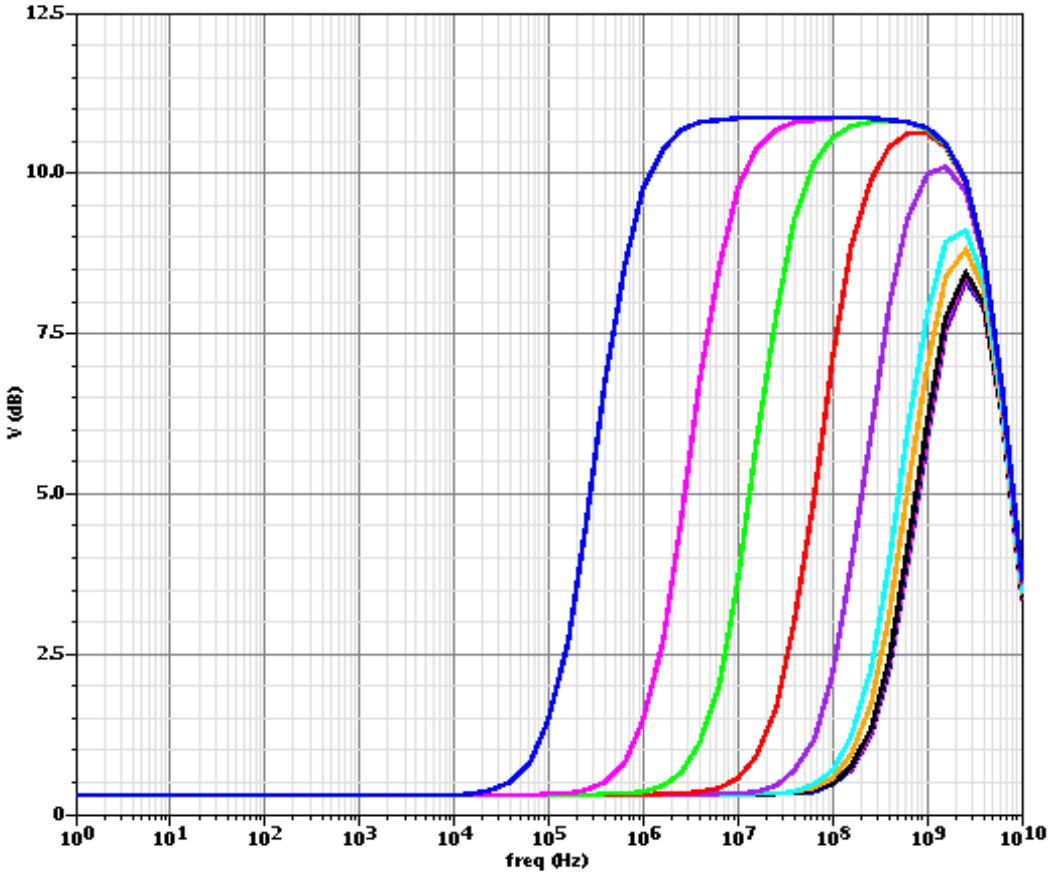

Figure 2.37: Variable bandwidth frequency response of the Gilbert cell

The graphs in Figure 2.37 and 2.38 have been generated by varying the source capacitor as shown in the Figure 2.36. The value of the capacitor determines the location of the zero, which changes the bandwidth of the amplifier. Increasing the value of the capacitor increases the bandwidth of the amplifier; reducing the value of the capacitor reduces the amplifier's bandwidth. Figure 2.38 is the frequency response of the two-stage amplifier, where the second stage of the amplifier is a common source amplifier. The graph in Figure 2.39 shows gain variation due to variation in both the control voltage and the source capacitance. The drawback of this technique is that the low frequency gain of the amplifier does not remain constant over variations in the control voltage. An array of

capacitors can therefore be used to generate a small range of variable gain with a particular control voltage. The ideal graph would display a constant low-frequency gain, which starts boosting near the operating frequency of 1.5 GHz.

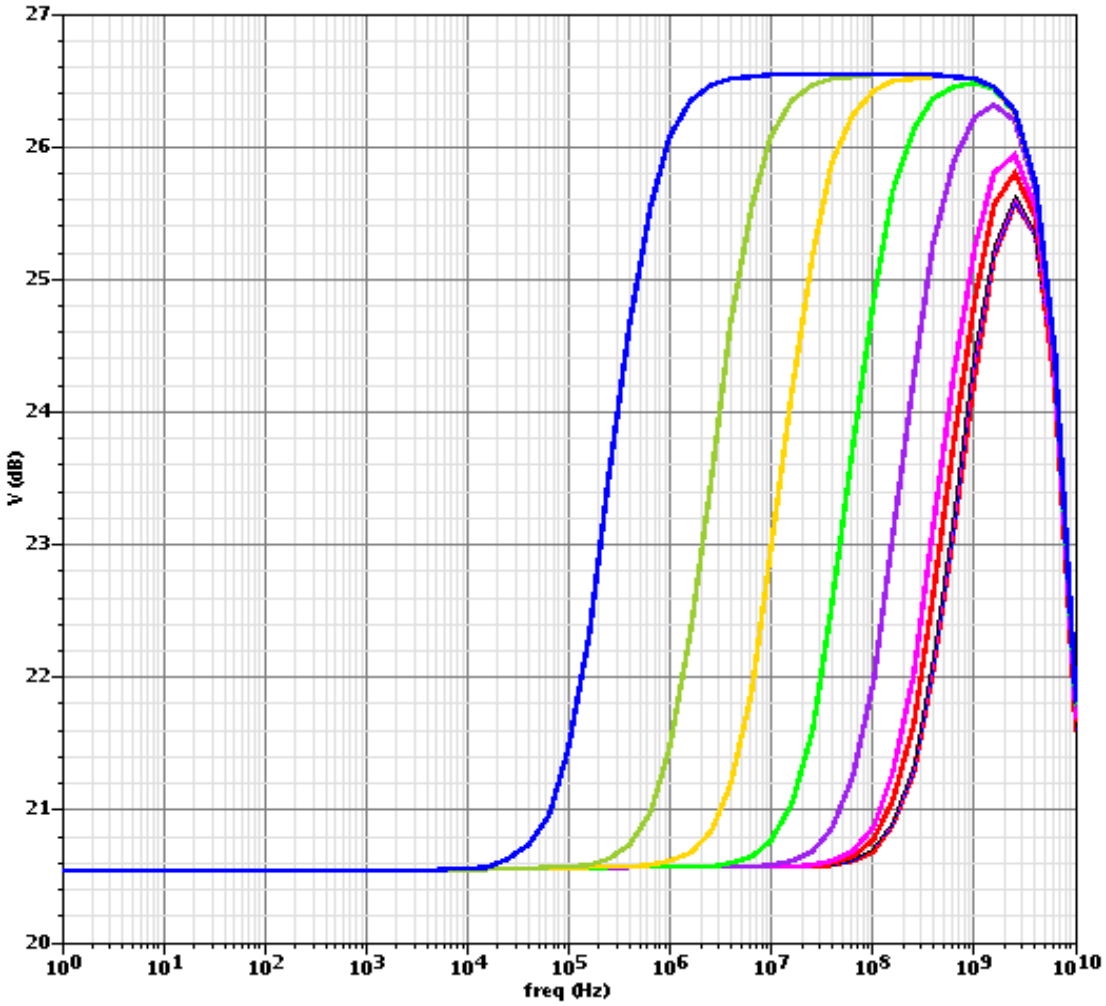

Figure 2.38: Variable bandwidth frequency response of the two-stage amplifier (Increased gain)

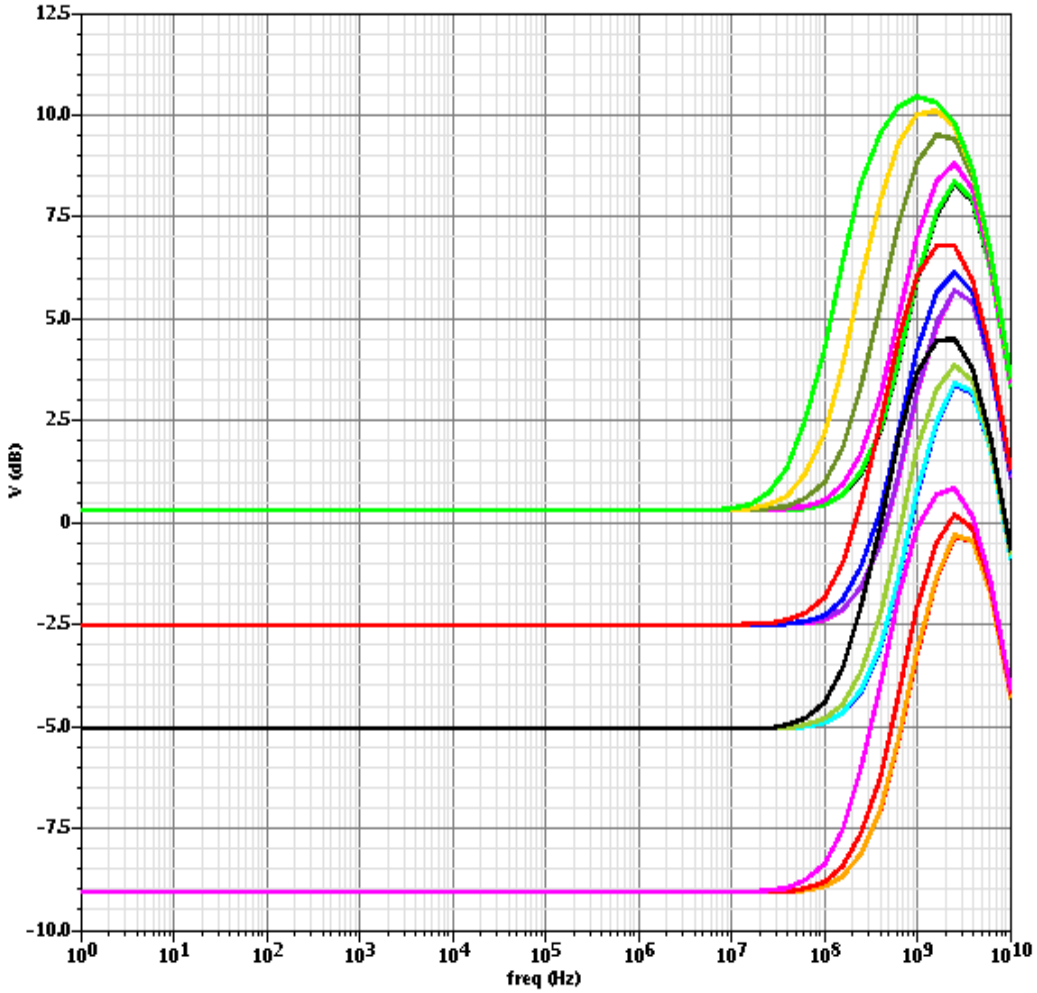

Figure 2.39: Variable gain frequency response with variable source capacitance and variable control voltage

The input to the Gilbert cell is of the order of 10 mV. Since a gain of 20 dB is to be achieved, the output of the differential amplifier is centered at approximately 0.5 V for maximum output swing. The transient output response is shown in Figure 2.40. The graph in Figure 2.41 is that of the peak value of the amplifier gain versus the control voltage. This graph shows the linearity of the amplifier over the control voltage range. At

higher gain values, the graph becomes non-linear as the transistors are almost cut-off due to low bias currents.

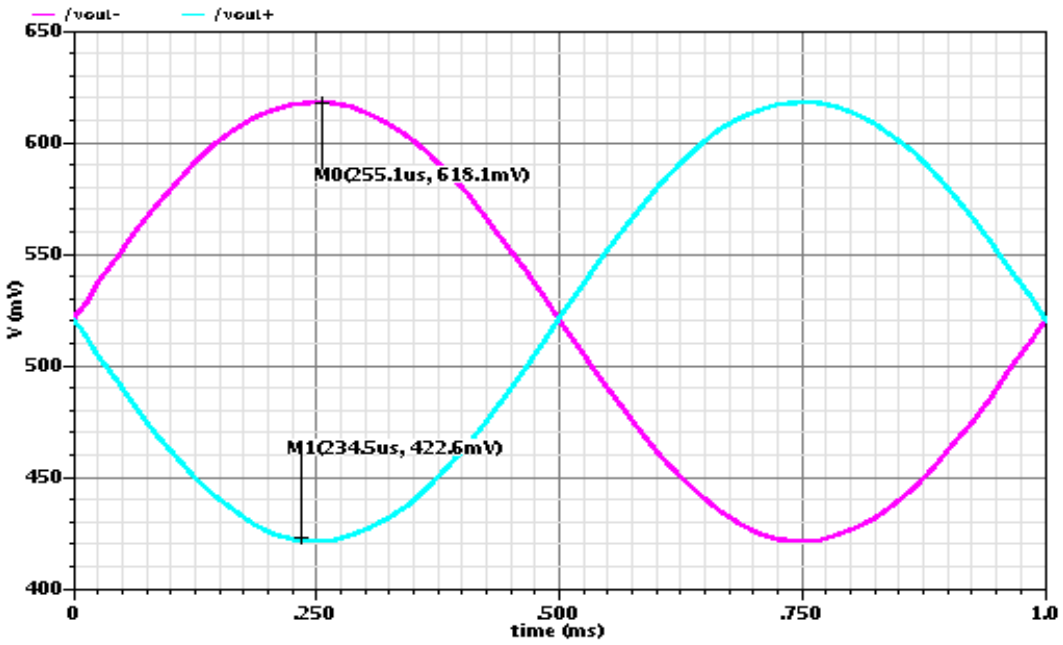

Figure 2.40: Transient output response

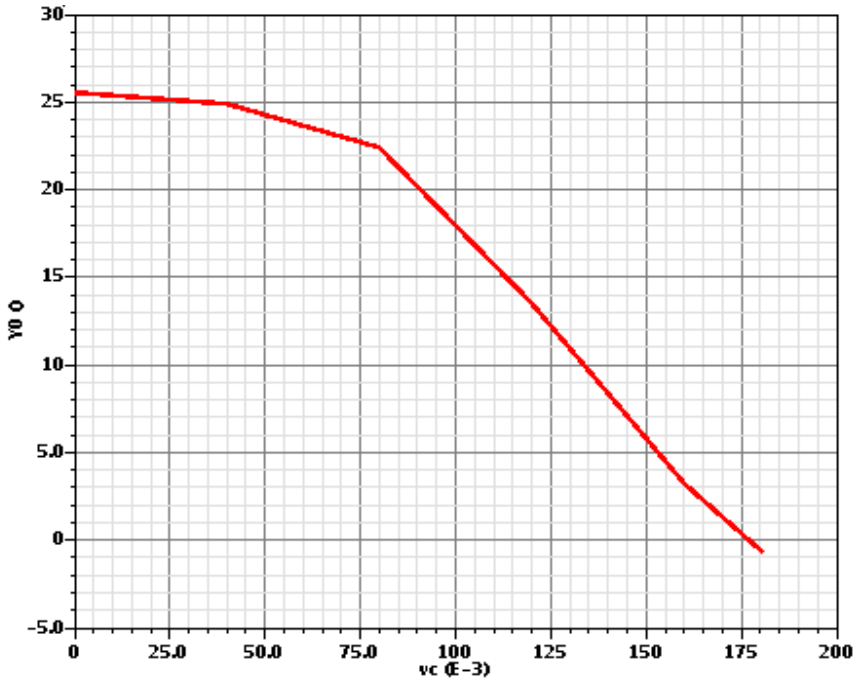

Figure 2.41: Peaking value of the amplifier v/s control voltage

2.4.5. Folded-cascode amplifier

The folded-cascode configuration was designed with the purpose of taking advantage of the voltage headroom that this architecture allows. The folded-cascode amplifier has one less stage than the Gilbert cell and therefore has more headroom, although it does result in less output voltage swing than the Gilbert cell. The higher voltage headroom increases the linearity of the amplifier and thus enhances its performance. The NMOS pair is the input differential pair which acts as the common source amplifier, while the PMOS pair is biased with the control voltage from the gain control stage to vary the gain of the amplifier. However, the folded cascode amplifier frequency response shows the bandwidth limitations of this circuit as shown in the Figure 2.43 and Figure 2.44.

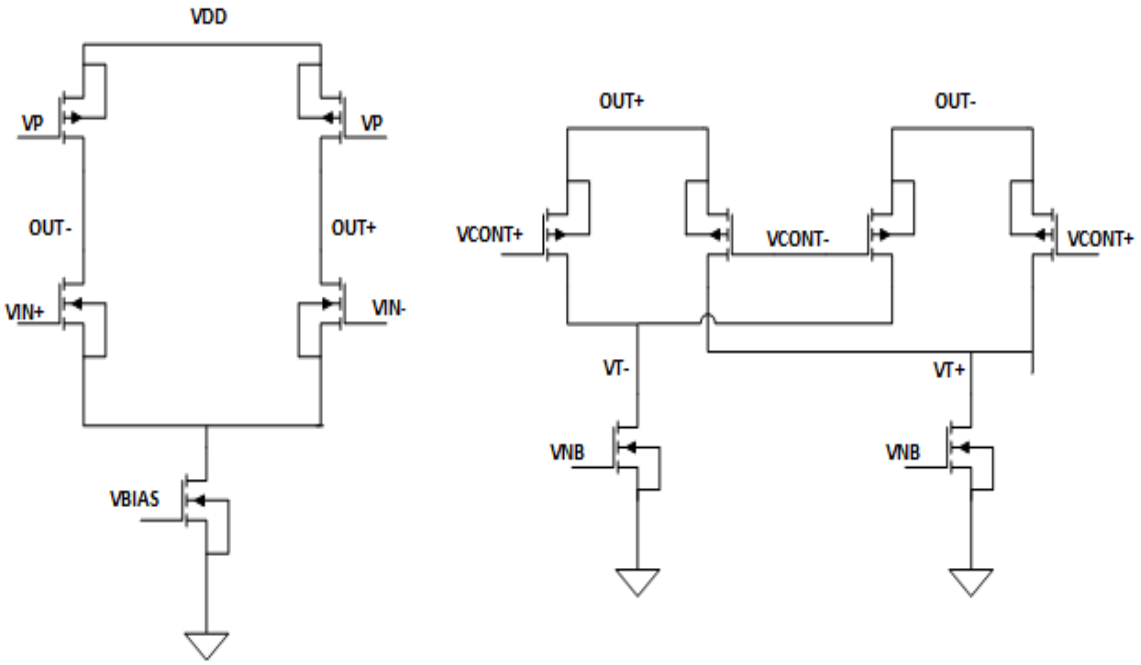

Figure 2.42: Folded-cascode amplifier schematic

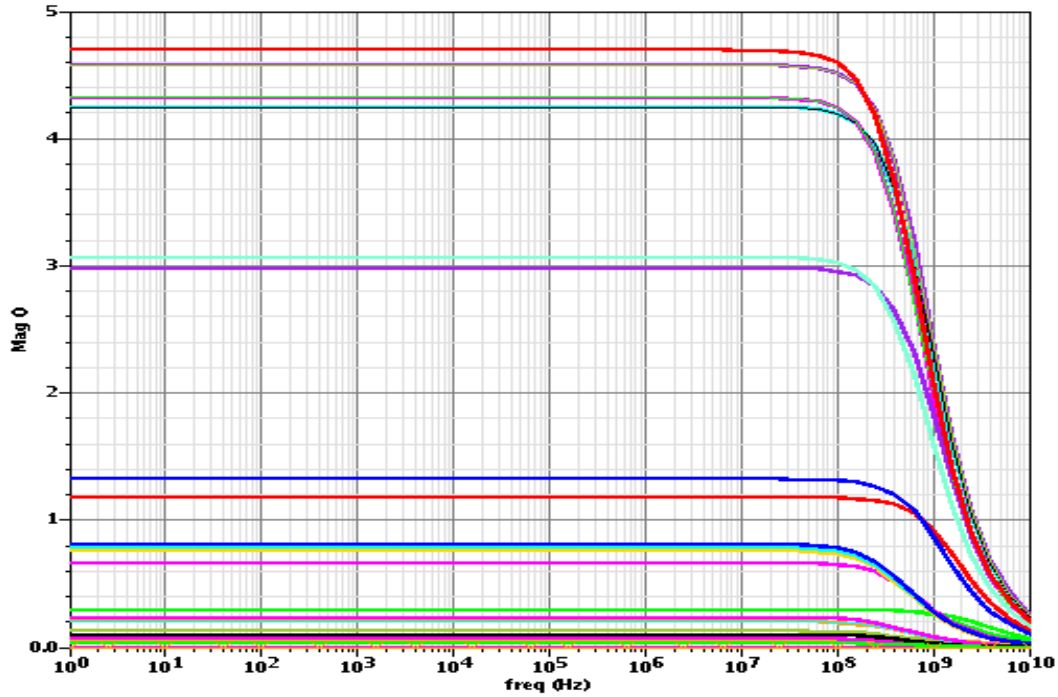

Figure 2.43: Variable gain (V/V) of the folded-cascode amplifier

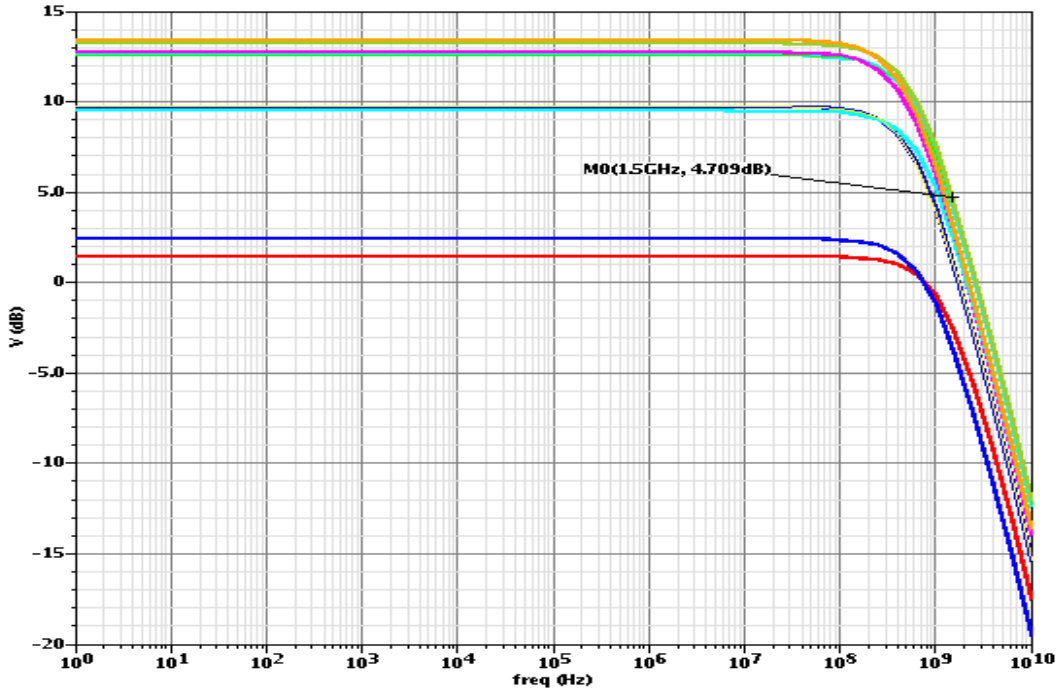

Figure 2.44: Variable gain frequency response of the folded-cascode amplifier

2.4.6. Gain control stage

The objective of the circuit in Figure 2.45 is to get a linear relationship between the control voltage and the biasing current in each branch, which is why this circuit is called a linear transconductance amplifier. This amplifier thus helps to provide a linear relationship between the control voltage and the resulting gain from the variable gain amplifier. The gain control stage is a linear transconductance amplifier and is compared to the linearized CMOS differential transconductance amplifier [14] for design guidance and understanding.

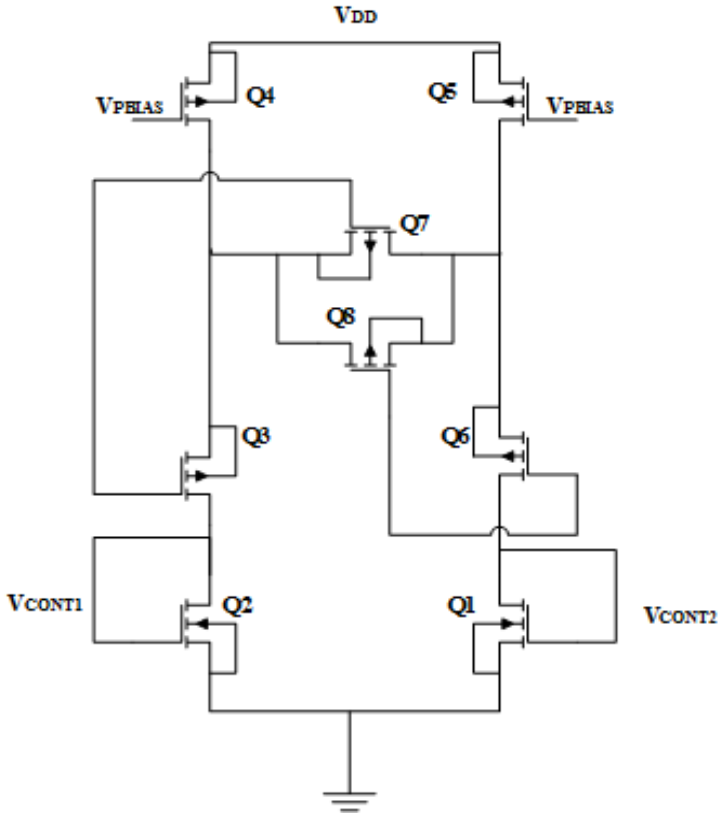

Figure 2.45: Linear transconductance amplifer as a gain control circuit

As a starting point, a differential integrator can be used as a tuning circuit due to its simplicity, tunability, area efficiency, and a good high-frequency performance, which implements the voltage-to-current converter function (as opposed to configurations with multi-stage operational amplifiers which suffer from large amounts of excess phase at high frequency) [14].

Q_3 and Q_6 are the input differential pair whose transfer characteristics are linearized by the voltage controlled degenerating resistors Q_7 and Q_8. The biasing current in each branch is equal to 1.5 mA, as per the previous calculations and to provide the appropriate biasing to the V_{CONT} stage in the Gilbert cell amplifier. The biasing of the V_{CONT} stage shifts as per the control voltage applied on the gate of the Q_7 and Q_8 transistors. This control voltage modulates the biasing point, thus affecting the gain of the Gilbert cell amplifier.

For optimum linear characteristics of the gain control circuit as per the assumptions and observations from [14], we can conclude that:

$$\frac{\beta_7}{\beta_3} = \frac{\beta_8}{\beta_6} = 7 \tag{2.18}$$

To lower the power consumption in the circuit, the biasing current in the current mirror source is kept as 500 uA and the width of Q_7 and Q_8 is increased to get the required biasing current of 1.5 mA. The Q_7 and Q_8 transistors act as resistors and prove instrumental in linearizing the relationship between the steering voltage and the output current biasing.

In the graph in Figure 2.46, the variations of the current can be observed with respect to the control voltage Vc. The V_C voltage is applied between the transistors Q_7 and Q_8 in the circuit shown in Figure 2.45. The x-axis is the range of Vc, where Vcmax = Vc + 0.28 and Vcmin = Vc – 0.28. Therefore, the current variation is almost linear with respect to the control voltage whose range extends from -0.5 V to 0.5 V. The voltages V_{CONT1} and V_{CONT2} are then applied to the amplifier to vary the current in the amplifier and thus modulate the gain of the amplifier. Linearizing the current output becomes difficult as the value of the V_{CONT1} or V_{CONT2} voltage increases beyond 0.8 V. Beyond 0.8 V, the headroom of the PMOS transistors falls enough to drive them away from the saturation region.

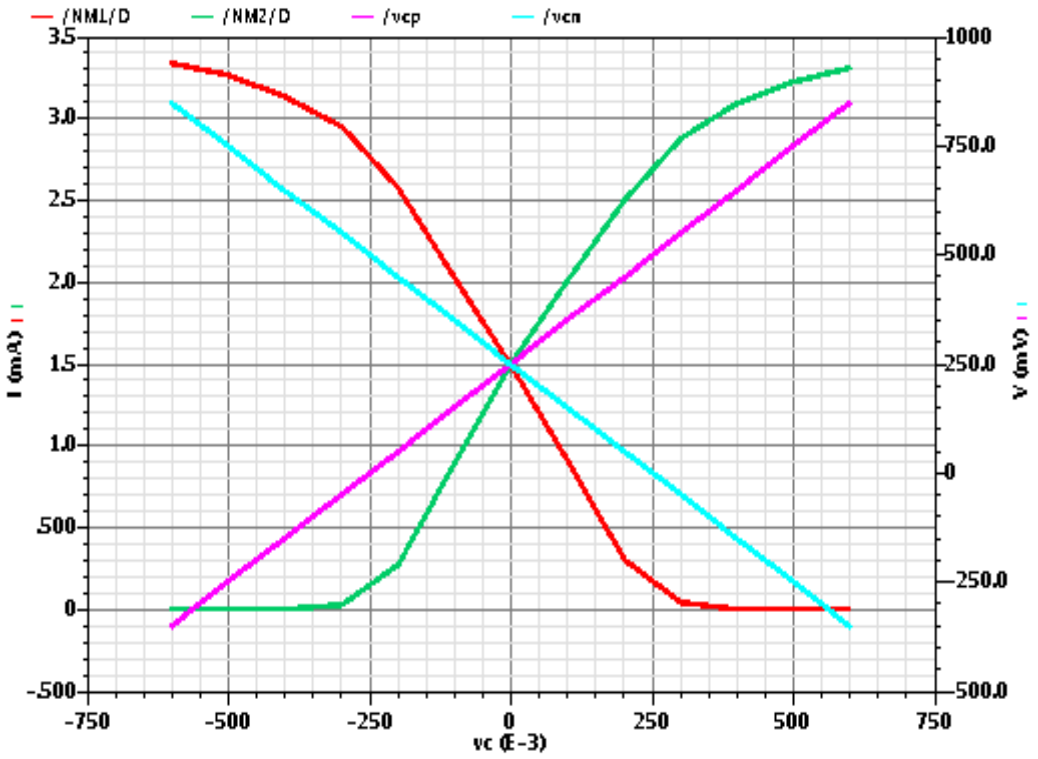

Figure 2.46: Variation of the branch currents with the change in V_{CONT}

2.5. Design verification

The design of the first-order CTLE is to be verified with corner simulations where PVT variations are subjected to the design and the effects are observed. Ideally, even with the PVT variations, the results are expected to be within the design specifications. For the corner simulations, the following PVT variations have been implemented:

Temperature = 125, 25, 0, -40

Corners = TT, FF, SS, FS, SF

V_{DD} = 0.9, 1, 1.1

The critical test points for corner simulations are high temperature parameters and V_{DD} variations. Any variations in the supply voltage changes the gain of the amplifier dramatically, especially when V_{DD} = 0.9 V. The two instances in which the gain changes drastically in Figure 2.48 is when V_{DD} = 0.9 V and the temperature is 125 °C as shown in Figure 2.47.

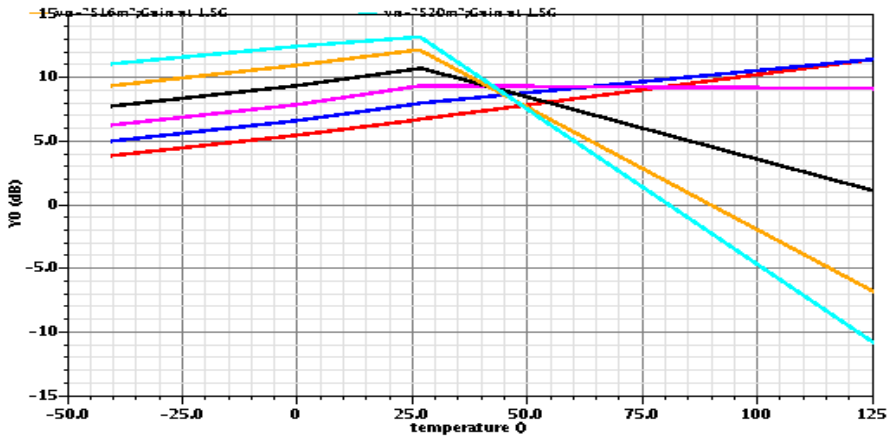

Figure 2.47: Gain variations with variations in temperature

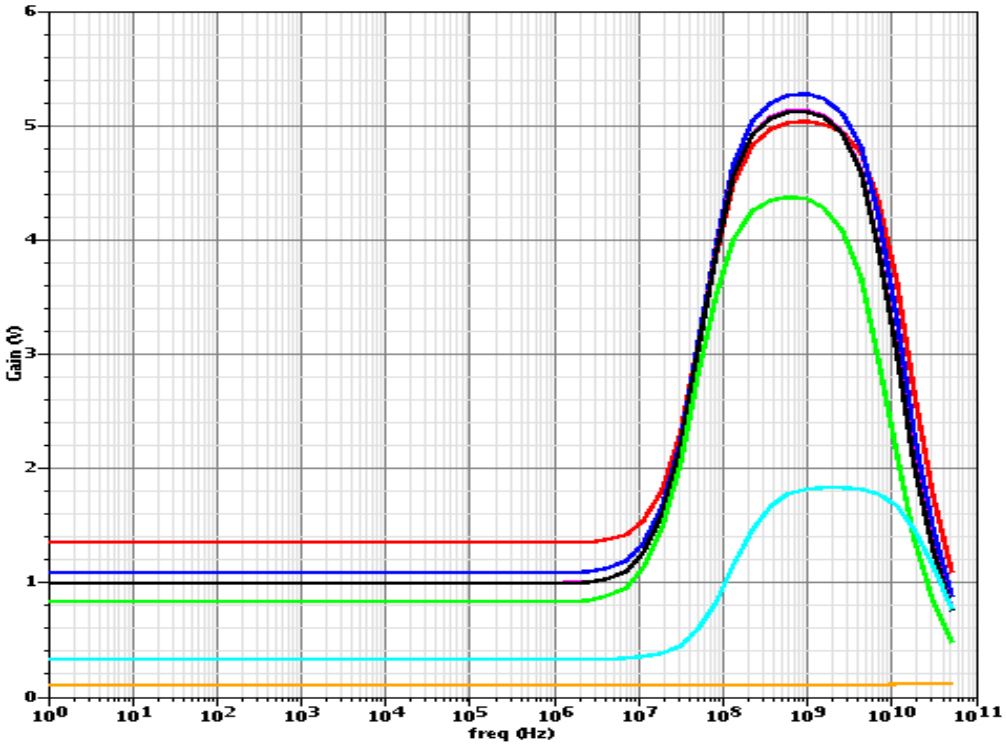

Figure 2.48: Gain variations of the first-order CTLE with changes in temperature (-40, 0, 25 and 125 °C and V_{DD})

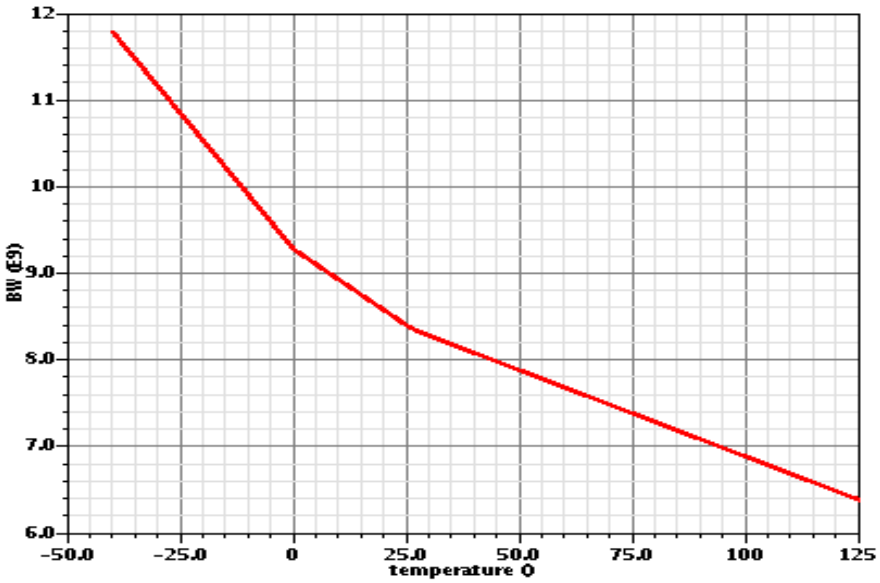

Figure 2.49: Variations of the bandwidth of the amplifier over temperature with V_{DD}=1 V

3. Matlab simulation and results

3.1. Cable response (transient and frequency)

The model of the coaxial cable was simulated in Simulink and the low pass frequency response of the coaxial cable of length 40 m is shown in Figure 3.1. The impedance of the Belden 1694A coaxial cable is 75 Ω. This cable model is used to replicate the behavior of the cable and thus simulate the behavior of the equalizer.

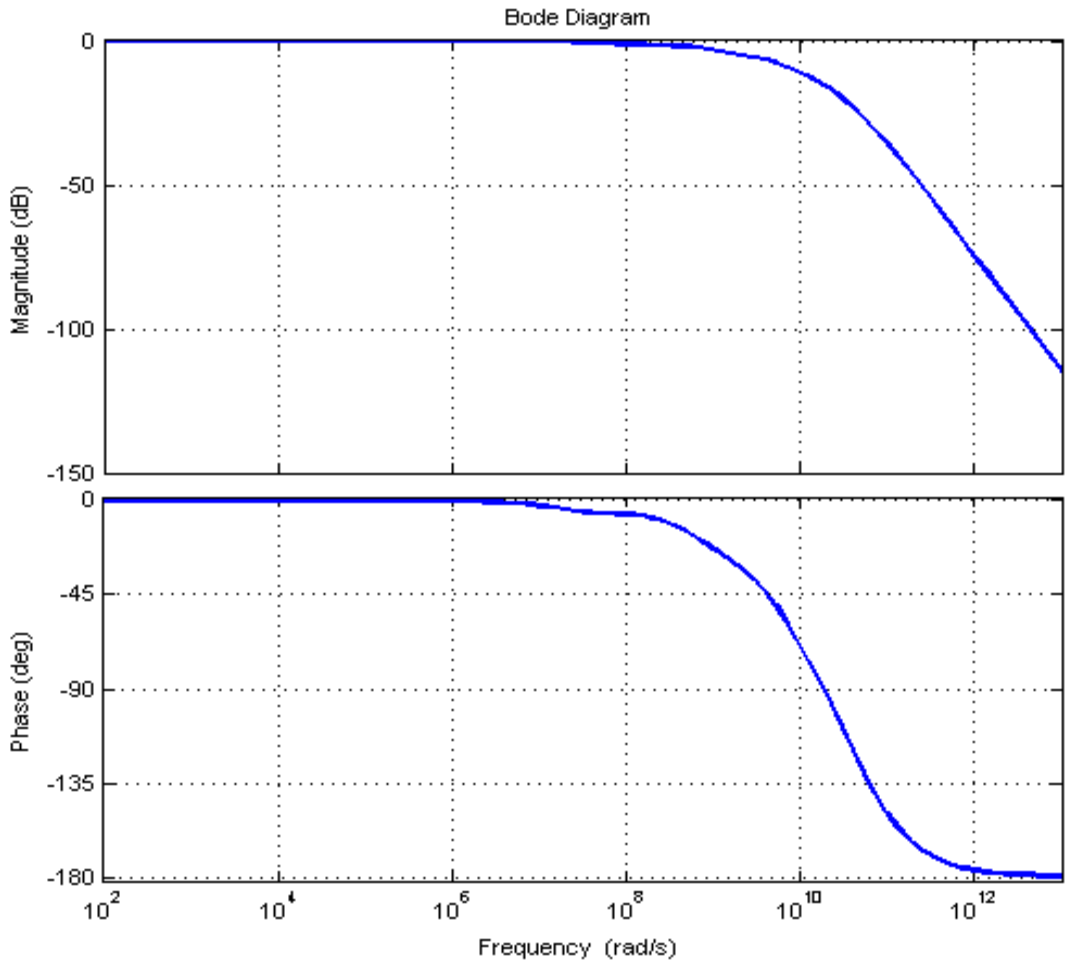

Figure 3.1: Low pass frequency response of a 40 m Belden cable

A PRBS-7 signal, shown in the Figure 3.2 was generated to apply as the input to the cable model to simulate the cable response to a digital input. The data output from the coaxial cable is shown in Figure 3.4 and, as can be seen, the data are attenuated and distorted due to the low pass characteristics of the cable. The eye diagram shown in Figure 3.3 is the eye diagram of the ideal PRBS signal. The eye diagram has an open eye with no jitter and the data edges overlap perfectly. This eye diagram has been shown to highlight the contrast between the eye diagram of an ideal signal and that of a signal that has been propagated through a channel or even a signal that has been equalized. The eye diagrams of the signal propagated through the channel or the equalized signals will not be this wide open and neither will they display this quality of a jitter free diagram. The next section will discuss the anatomy of an eye diagram as well as show the eye diagrams of the equalized signals from a channel of different lengths.

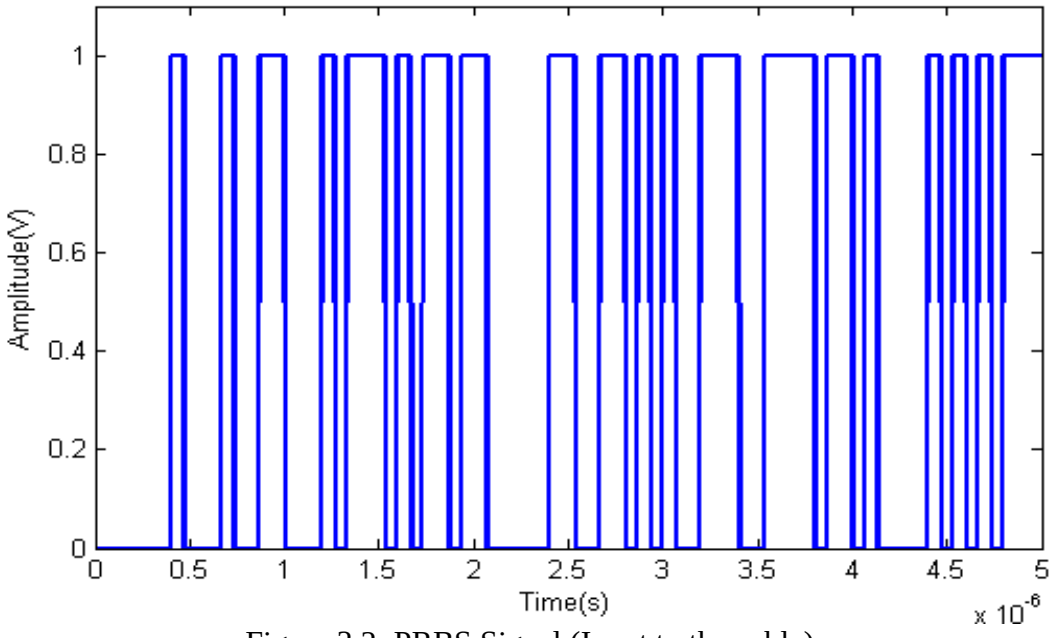

Figure 3.2: PRBS Signal (Input to the cable)

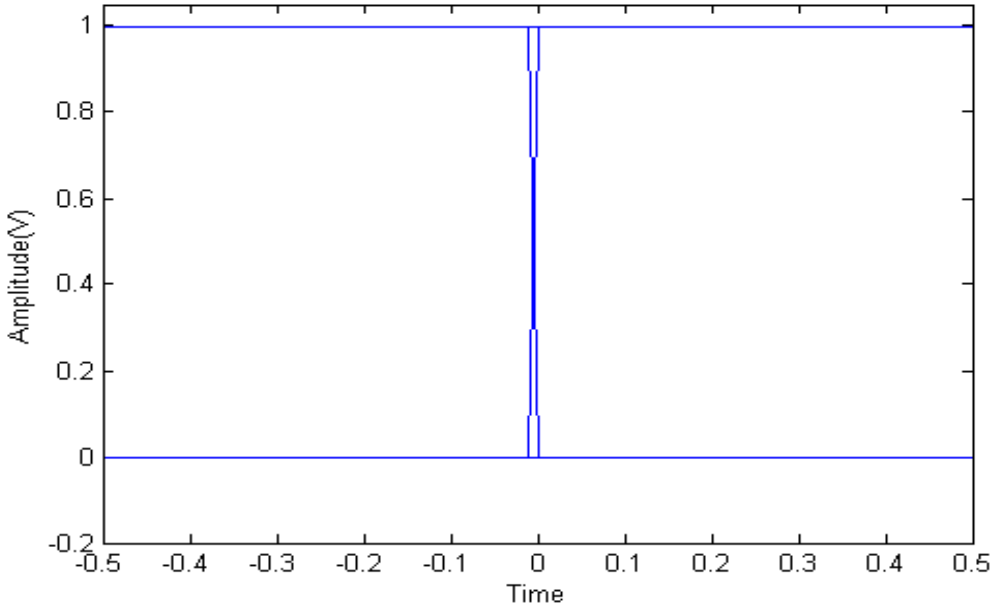

Figure 3.3: Eyediagram of an ideal PRBS signal

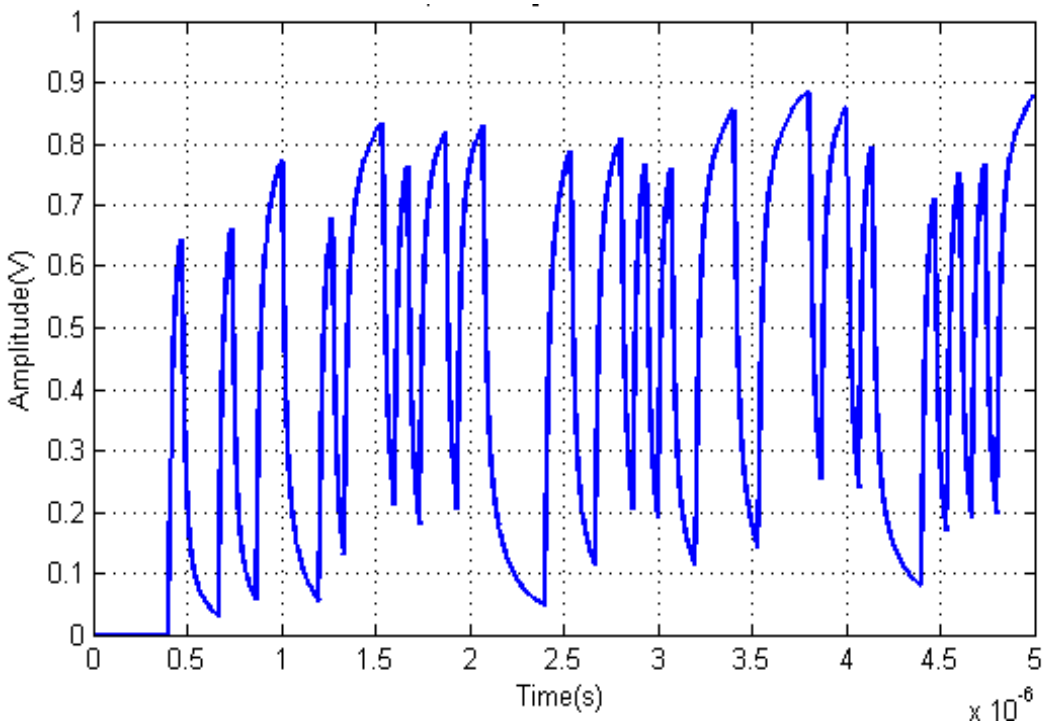

Figure 3.4: Data output from a coaxial cable of length 40 m

3.2. Eyediagram

An eyediagram is an indicator of the quality of the signals in high-speed digital transmissions. The eye diagram is generated by overlapping sections of the digital data stream at periodic intervals and thus creates an opening that looks like an eye. A good method of testing a digital transmission system is to test it with a PRBS signal, which may have random and long runs of either 1's or 0's.

A very useful and important component of an eye diagram is jitter. Jitter occurs when there is a late or early occurrence of the rising and falling edges of the data. Jitter may occur due to reflections, ISI, crosstalk, PVT variations, and some jitter is even random. Some of the eye diagram parameters like noise margin, jitter, eye width and eye length have been highlighted in Figure 3.5. The graphs in Figure 3.5, 3.6 and 3.7 represent the eye diagrams of the data output through a cable of length 20 m, 40 m, and 80 m respectively. It can be observed from the graphs in Figure 3.5, 3.6, and 3.7 that the eye diagram openings get smaller as the length of the cable increases. This is due to the fact that the attenuation at the operating frequency increases as the cable length increases as shown in the previous section.

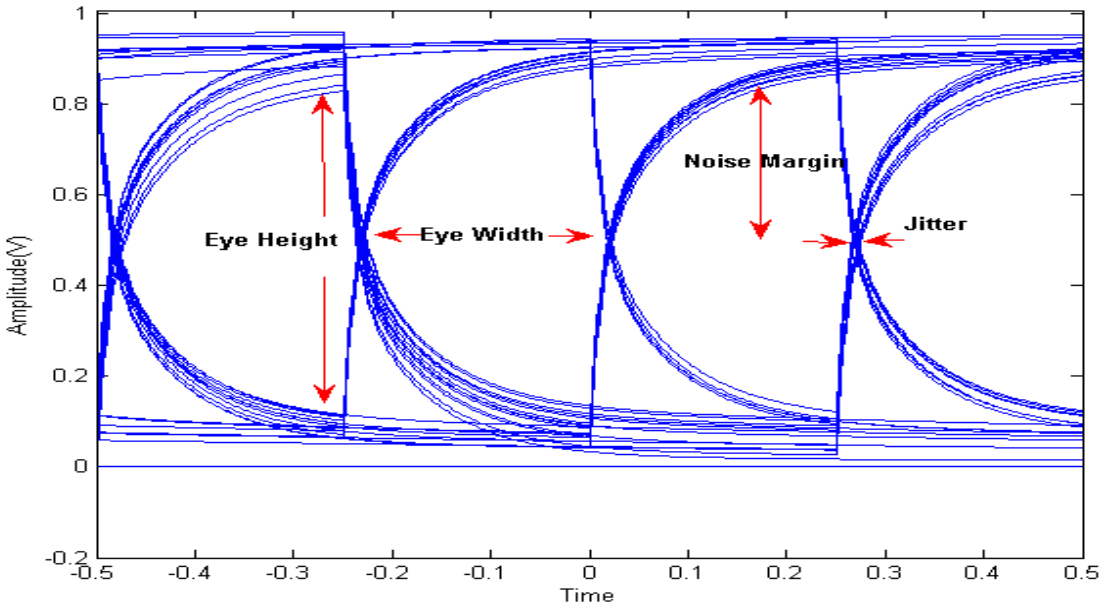

Figure 3.5: Eyediagram of the data through a cable of length 20 m

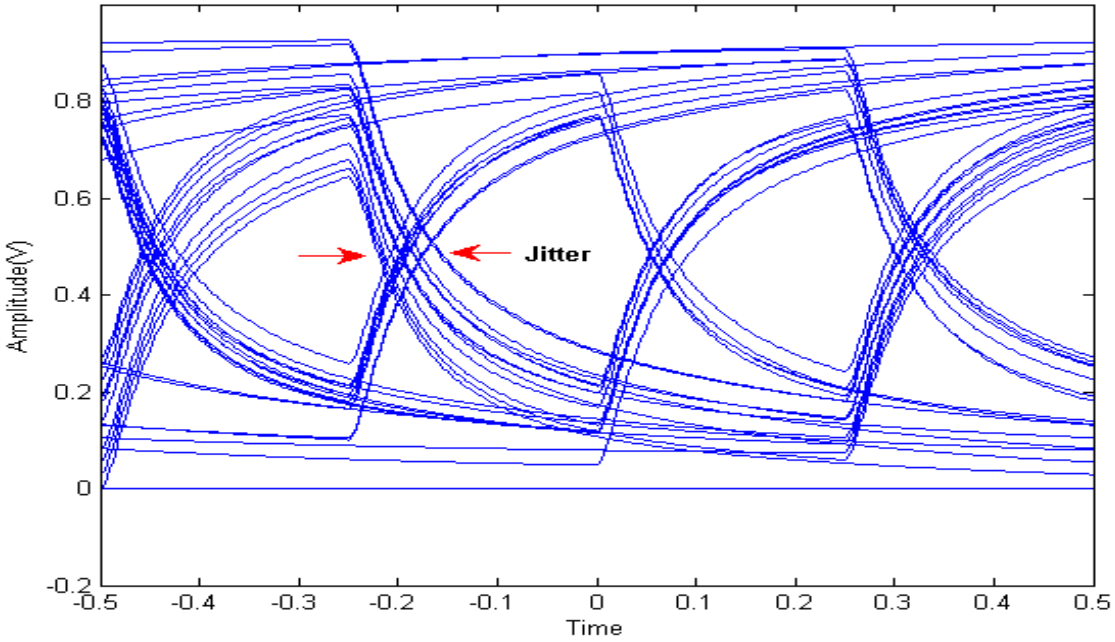

Figure 3.6: Eyediagram of the data through a cable of length 40 m

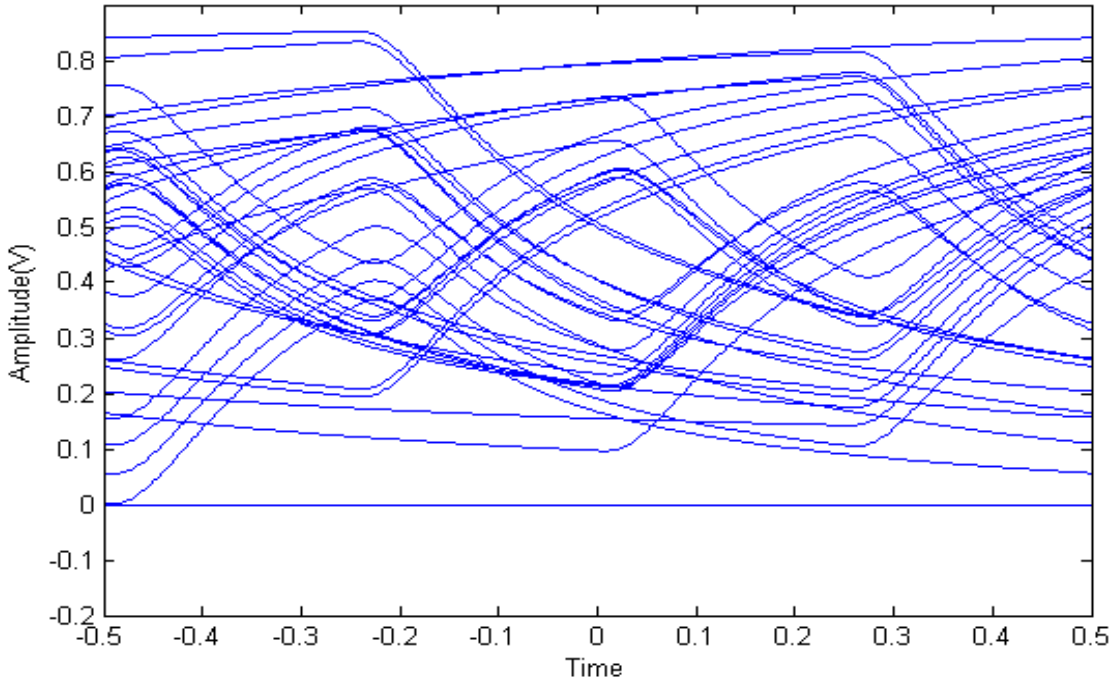

Figure 3.7: Eyediagram of the data through a cable of length 80 m

3.3. Curve matching

To generate the transfer function of the equalizer in Matlab, the frequency response of the amplifier from the Cadence simulations was exported to Matlab. The transfer function of the equalizer was then estimated from the frequency response curve, by estimating the locations of the poles and zeroes in the transfer function of the amplifier. The graphs in Figure 3.8 represent the frequency response of the Belden cable of length 20 m, 40 m and 80 m.

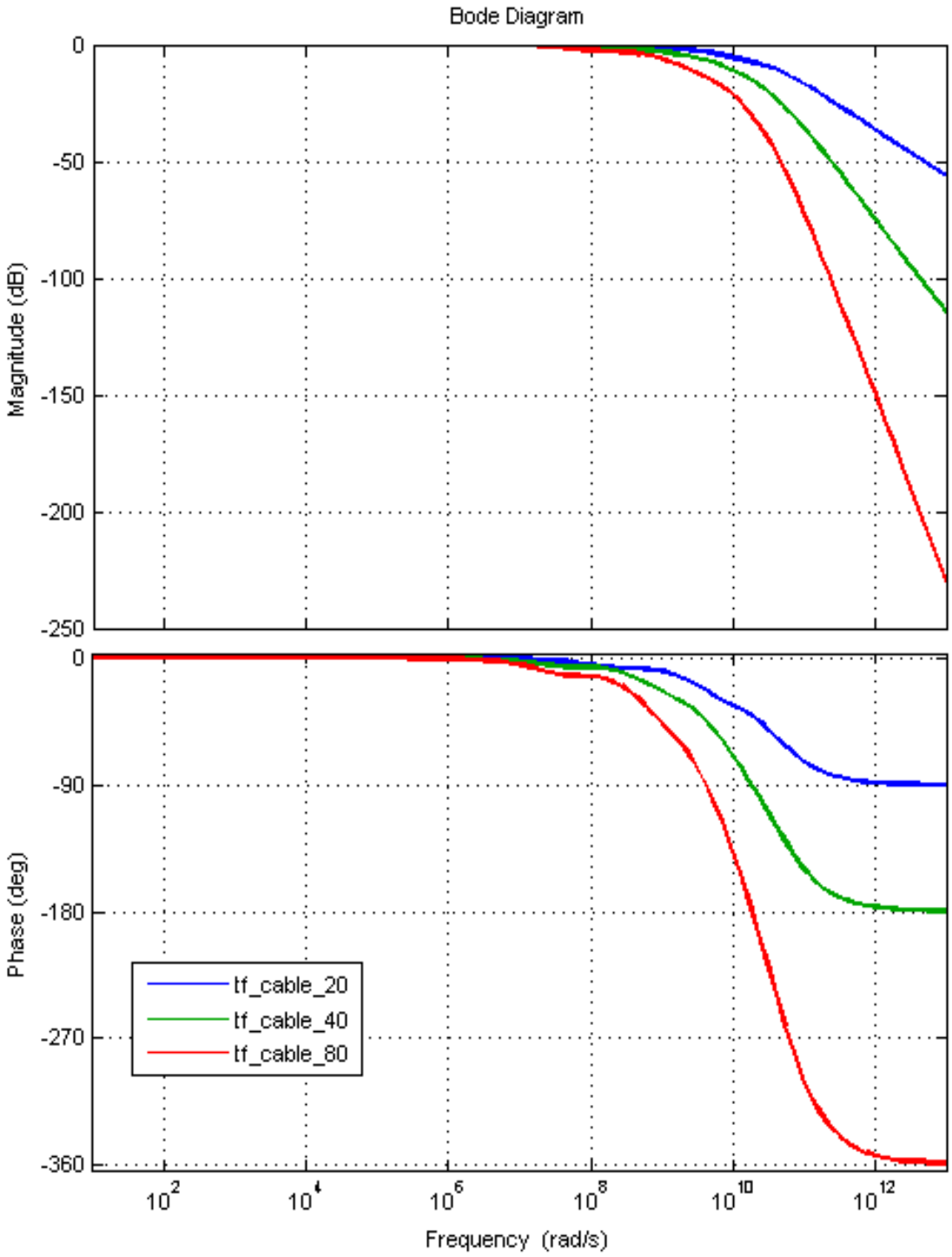

Figure 3.8: Frequency response of the coaxial cable of lengths 20 m, 40 m and 80 m

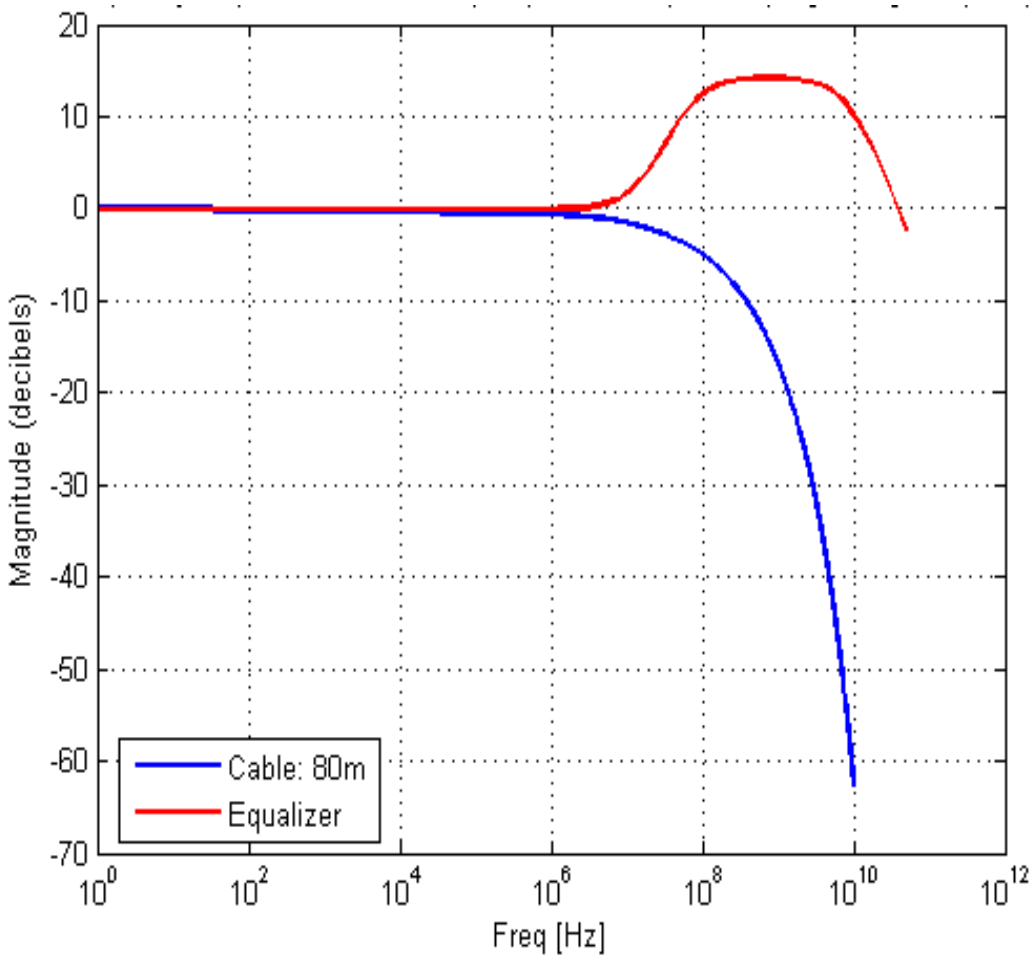

Figure 3.9: Frequency response of the cable (80 m) and the equalizer (single-stage amplifier)

The graph of the equalizer shown in Figure 3.9 is the frequency response of a single-stage amplifier that has been exported from Cadence simulations. The transfer function of the equalizer was then estimated from the frequency response curve by estimating the pole and zero locations. The transfer function of the equalizer should be the inverse of that of the cable to compensate the losses of the cable at appropriate frequencies, and thus reduce the ISI and distortion occurring in the data propagated through the channel.

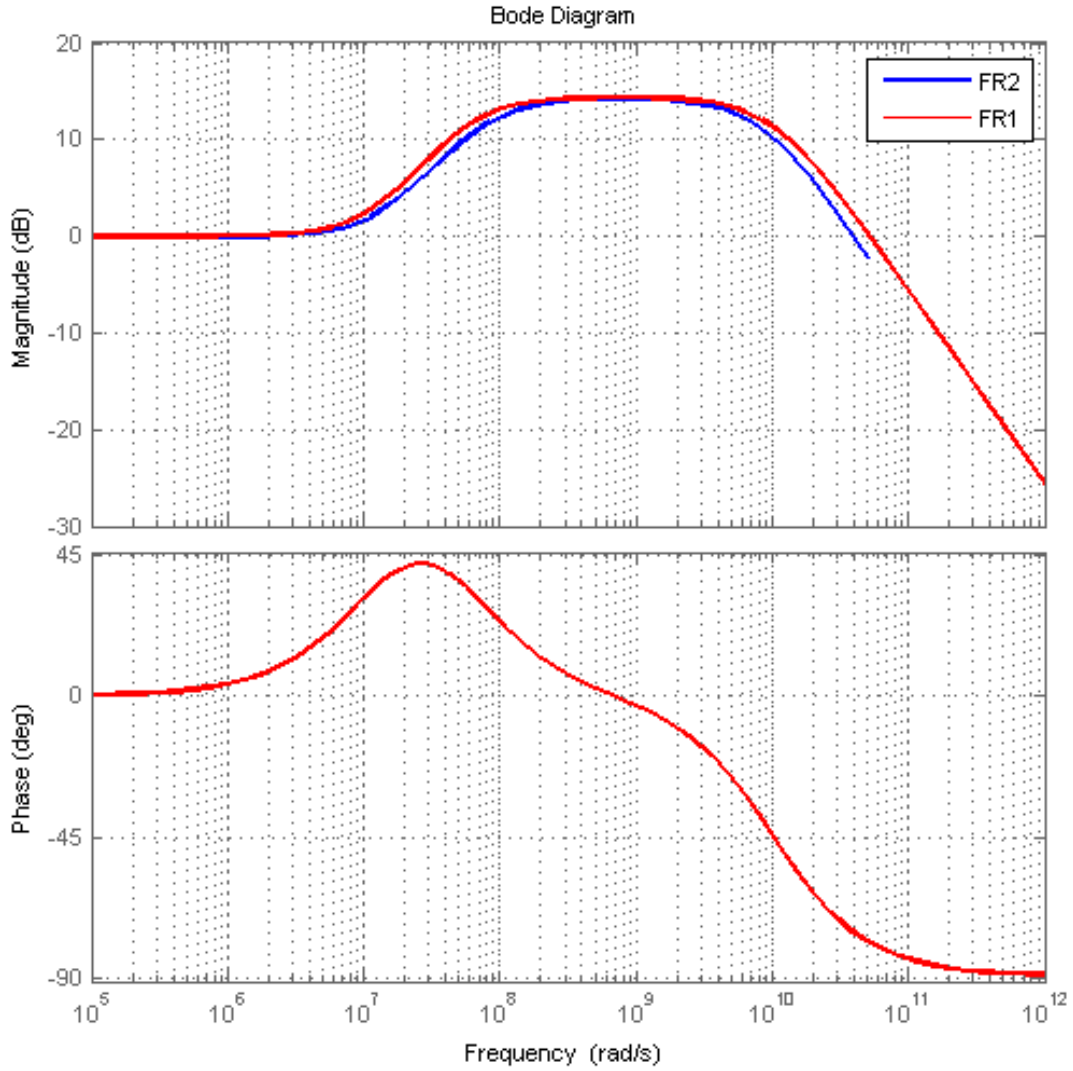

Figure 3.10: Close approximation of the transfer function of the equalizer

The frequency response curve labeled FR1 in the Figure 3.10 is the bode plot of the estimated transfer function from the frequency response curve labeled FR2, which has been exported from Cadence and is the amplifier frequency response. The pole and zero locations were manipulated to match the two curves to each other and thus obtain the transfer function of the equalizer.

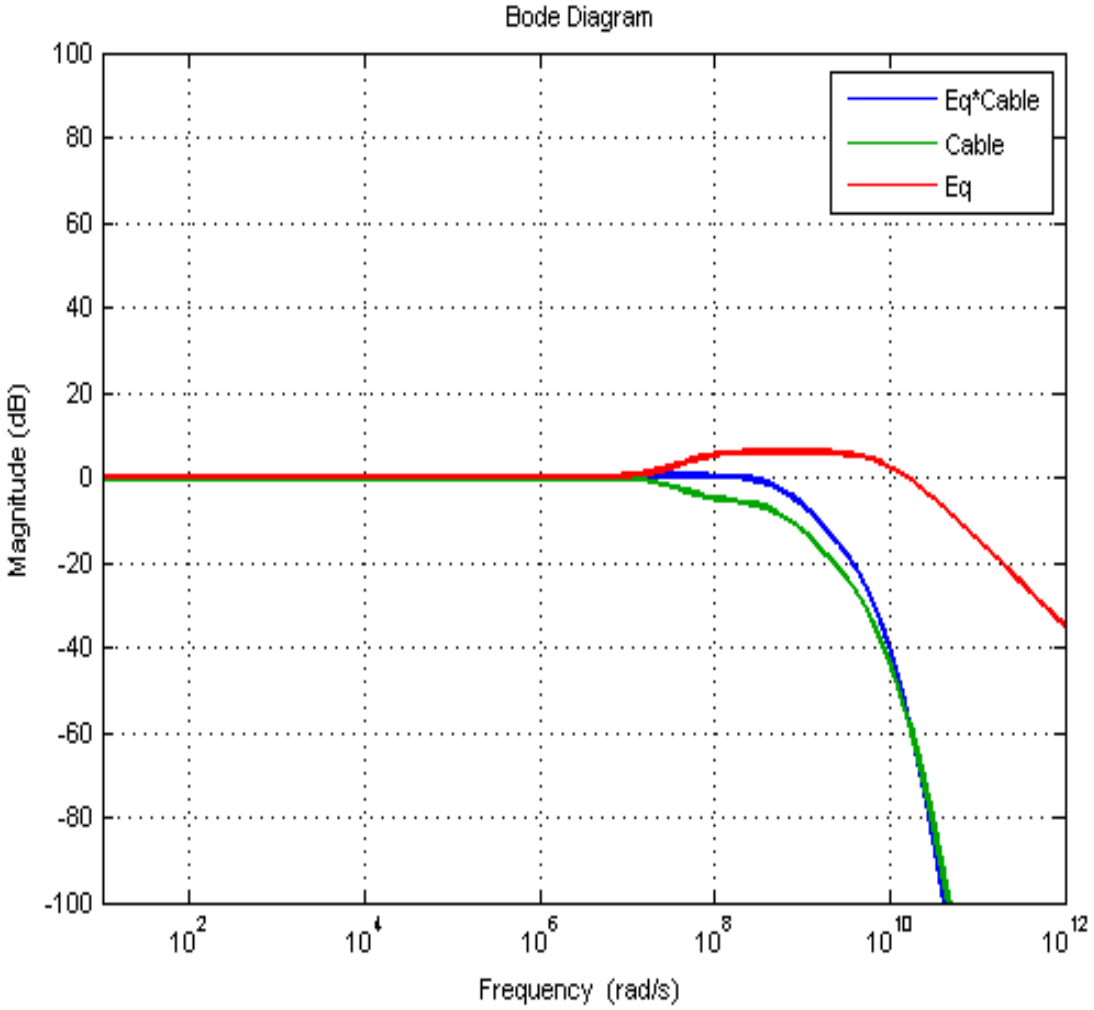

Figure 3.11: Flat frequency band generation using the equalizer

The graphs in Figure 3.11 demonstrate that the equalizer compensates for the losses of the coaxial cable. The curve name Eq is the frequency response of the equalizer filter, while the curve named Cable is the coaxial cable frequency response. When the transfer function of the equalizer and the cable are multiplied together, they generate a flat band frequency response over the operating frequency. A completely flat frequency response is

the ideal response of a digital transmission channel and helps to avoid data attenuation and distortion.

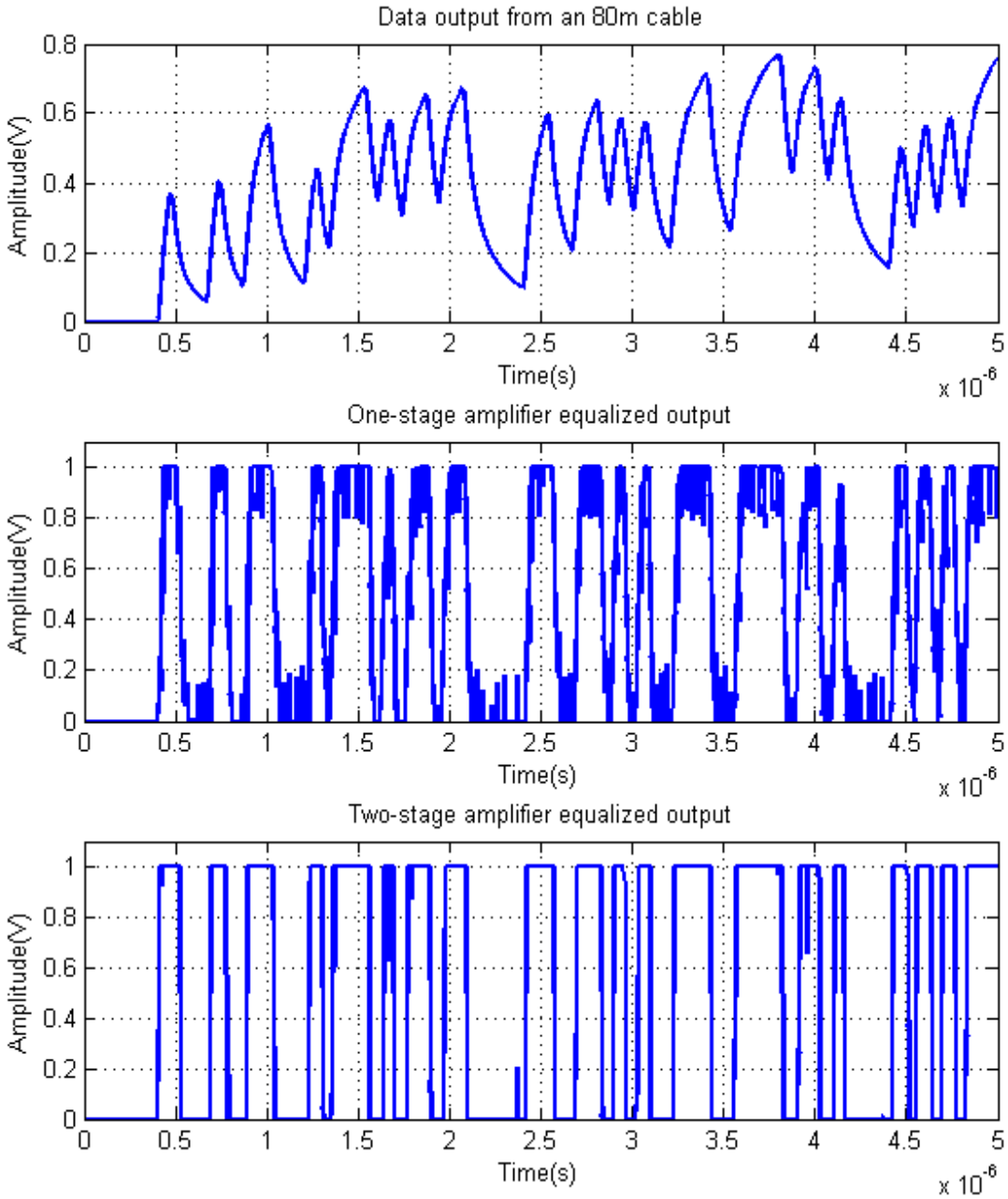

Figure 3.12: Equalization of the data through a cable of 80 m

The graphs in Figure 3.12 show the equalized data plots of the data output from the cable of length 80 m. The two-stage amplifier transient output has less distortion than the single-stage amplifier output.

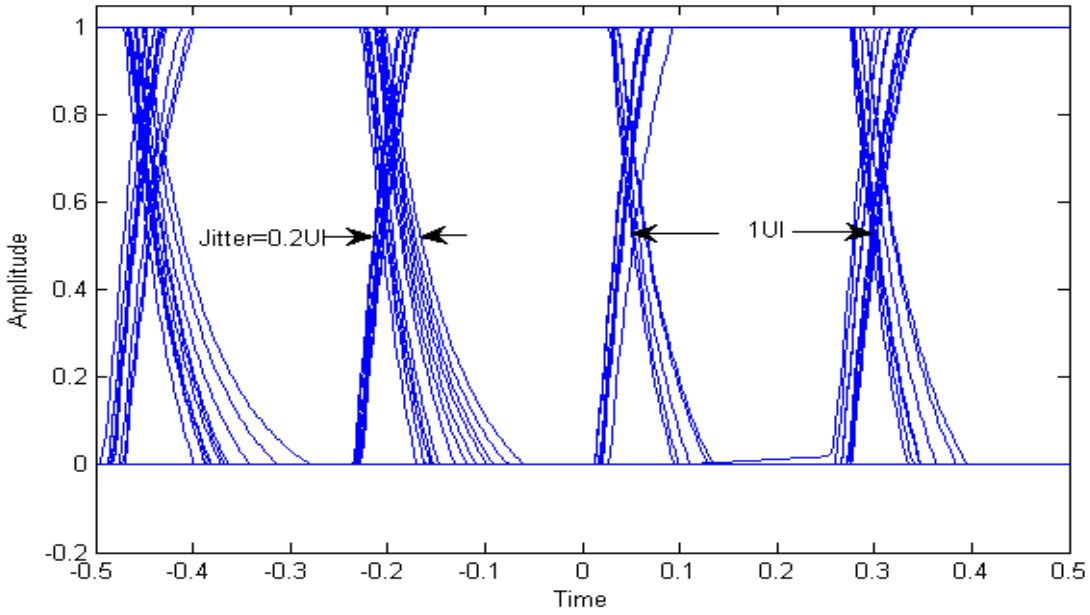

Figure 3.13: Eyediagram of the equalized data through an 80 m cable using a single-stage amplifier

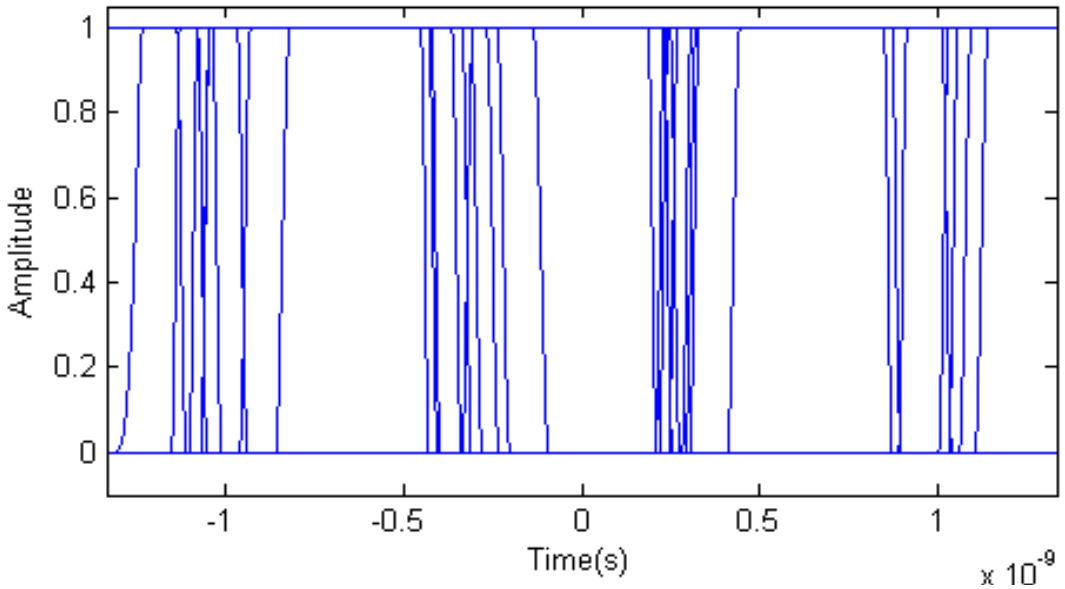

Figure 3.14: Eyediagram of the equalized data through an 80 m cable with a 2-stage amplifier

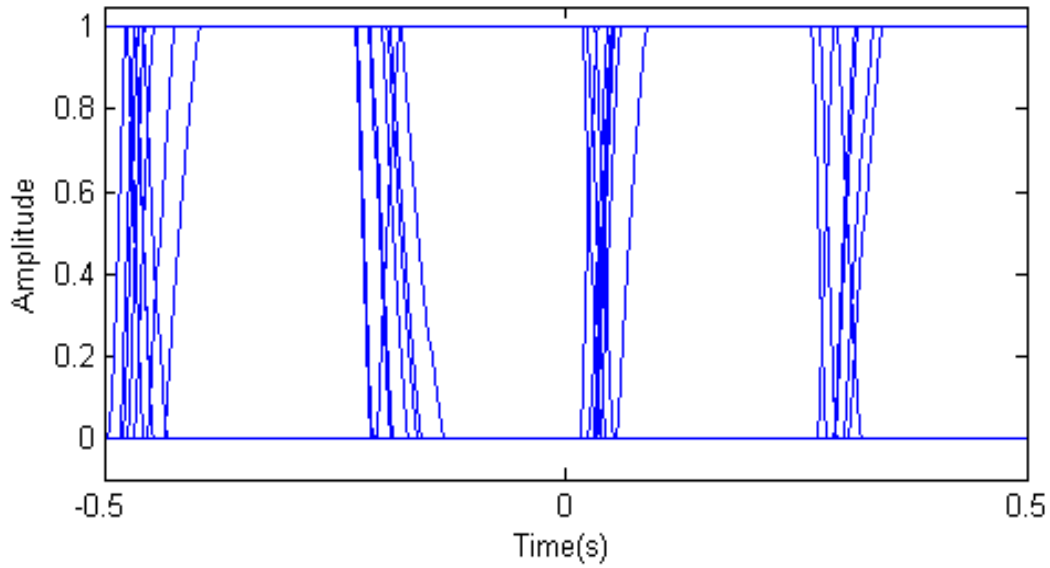

Figure 3.15: Eyediagram of the equalized data through a 40 m cable with a single-stage amplifier

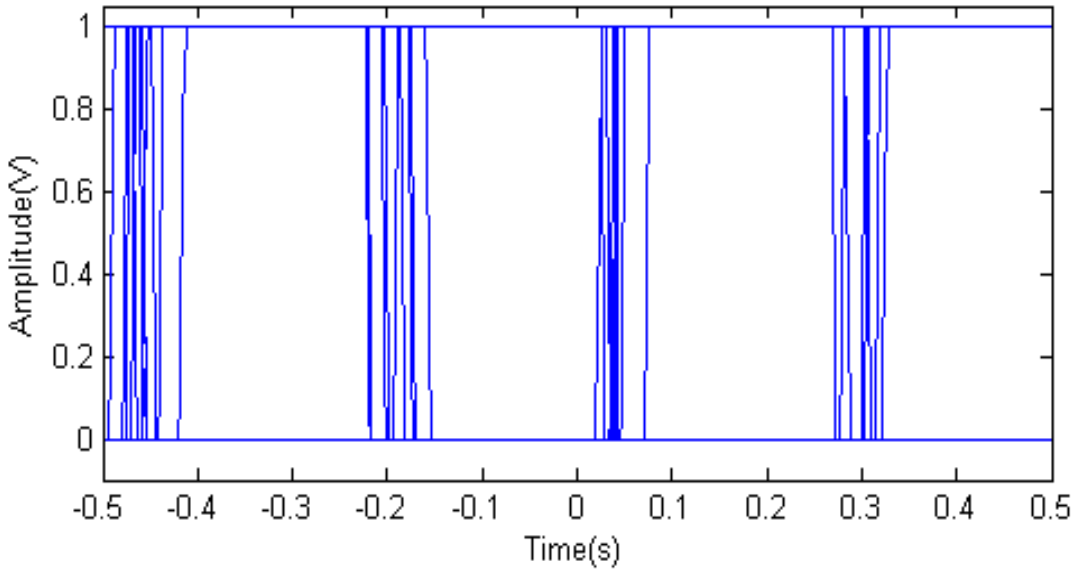

Figure 3.16: Eyediagram of the equalized data through a 40 m cable with a 2-stage amplifier

Although the eye diagrams in Figure 3.13, Figure 3.14, Figure 3.15, and Figure 3.16 have a large eye opening, they show the occurrence of jitter.

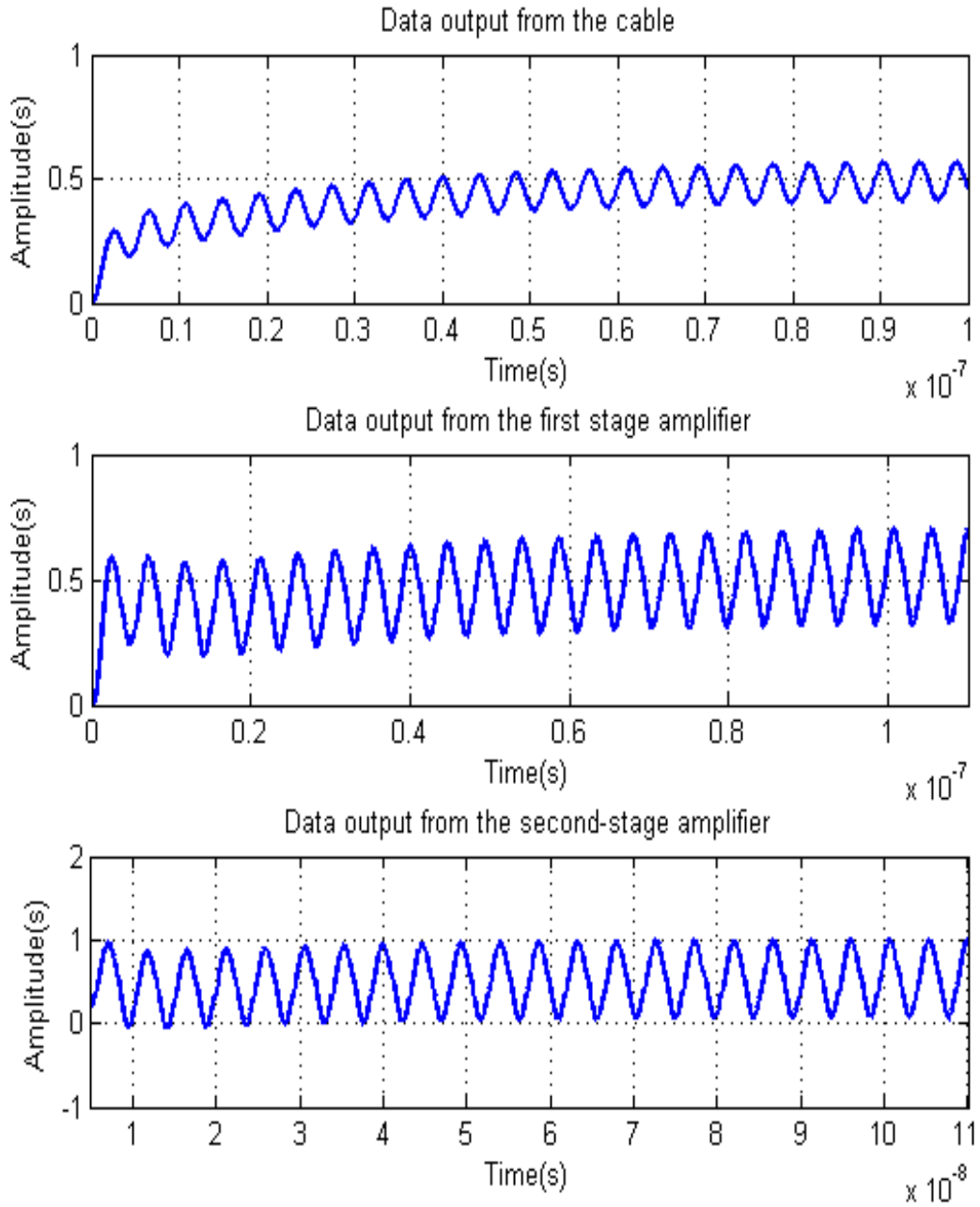

Figure 3.17: Sine wave input equalization

The sine wave input to the cable is attenuated after propagating through the cable. The input also suffers from baseline wander as can be seen in the first transient output in

Figure 3.17. The second transient output and the third transient output are the outputs of the first-stage and second-stage amplifier respectively. The outputs from the first stage amplifier and the second stage amplifier amplify the signals and reduce the baseline wander to a good extent.

4. Conclusion

This work covers the proposal, design, implementation, and verification of the continuous time linear equalizer in the CMOS 45 nm technology. The constraints of the design were the low output resistances of the large width transistors, headroom limitations in cascode amplifier design, and the linearity limitations. Another major issue during the amplifier design was that the load resistance changed with the control voltage, which in turn changed the low frequency gain. A future goal is to design a DC restoring circuit, which will eliminate the baseline wander that occurs due to AC coupling.

The Matlab and Cadence simulations results matched and proved that the equalizer does overcome the attenuation caused by the low pass characteristics of the channel. The goal of achieving a flat band frequency response over the operating frequency using the equalizer was materialized. A future goal is to achieve low jitter in the output data eye diagram of the equalized signals. Thus, a low-voltage equalizer can be designed in a 1 V technology, but with some gain and linearity limitations.

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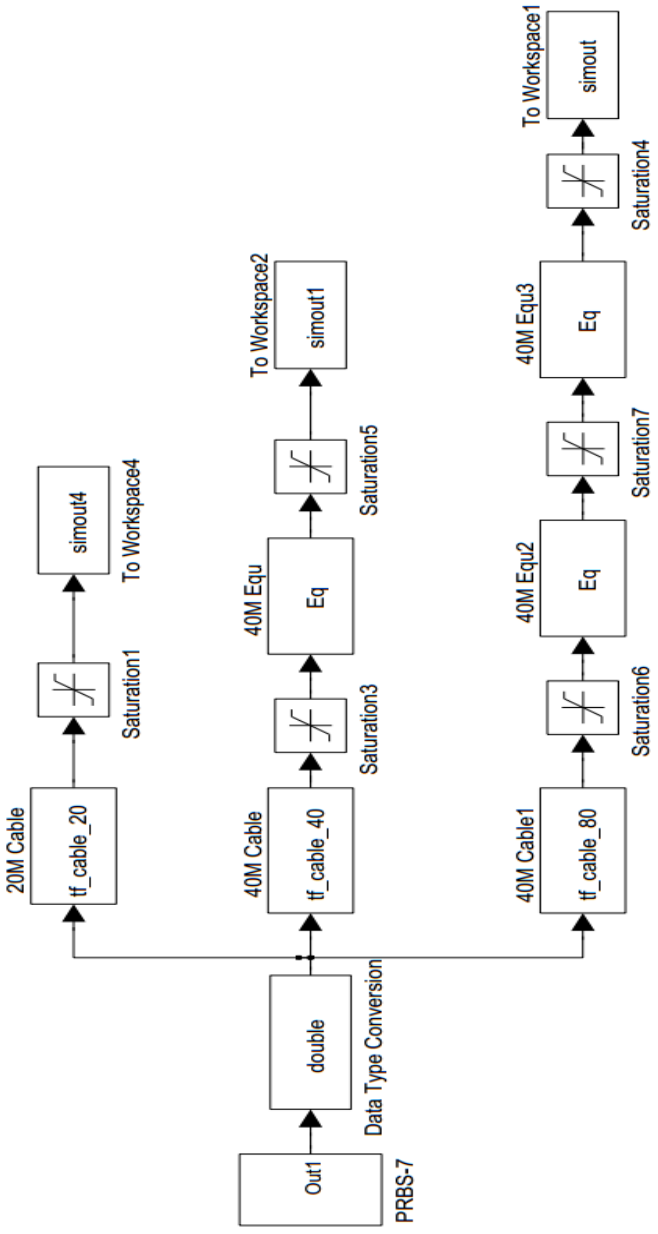
APPENDIX



1: Cable and Equalizer system test model in Simulink