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Modeling of the impact of electrical stressors on the degradation process of Power MOSFETs

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MODELING OF THE IMPACT OF ELECTRICAL STRESSORS ON
THE DEGRADATION PROCESS OF POWER MOSFETS

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San José State University

In Partial Fulfillment

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Master of Science

by

Shompa S. Mahiuddin

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The Designated Thesis Committee Approves the Thesis Titled

MODELING OF THE IMPACT OF ELECTRICAL STRESSORS ON THE
DEGRADATION PROCESS OF POWER MOSFETS

by

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APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

SAN JOSÉ STATE UNIVERSITY

May 2011

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ABSTRACT

MODELING OF THE IMPACT OF THE ELECTRICAL STRESSORS ON THE
DEGRADATION PROCESS OF POWER MOSFETS.

by Shompa S. Mahiuddin

This research focused on building a model based on collection of experimental data

acquired with high electrical stressors at the gate of the power MOSFET under an

isothermal condition to analyze certain deviations of intrinsic properties leading to

degradation. The primary indicators were threshold shift, deviation in switching

characteristics, and significant expansion of the Miller Plateau due to accelerated

stressing of the device from the pristine condition. The intrinsic mechanism associated

with the threshold shift and changes in the parasitic capacitances were observed and

analyzed with mathematical precision and device parameter simulation. It was seen that,

in addition to altered switching behavior and other changes, the threshold voltage shifted

by 172%, the width of the Miller Plateau increased by 525%, and capacitances decreased

by 24~43% at applied stress of 45V to 54V in addition to altered switching behavior and

other changes. This behavior showed deviation; however, degradation did not occur.

The root cause of the modified behavior of a stressed device was also analyzed. The 2D

device-processing software "Sentaurus" correlated the experimental observations.

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I appreciate my husband in supporting my work on the thesis and helping me achieve my dream. Finally, I would like to thank my parents and my brother for giving me confidence, hope, and the dream to become a researcher.

Table of Contents

List of Figures

x

List of Tables

1.   Introduction

Electronics components have an increasingly critical role in on-board, autonomous

functions for vehicle controls, communications, navigation, automotive, and radar

systems [1]. The knowledge of semiconductor degradation within electronics, under

various system and environmental stressors, is important to correlate with the prediction

of a failure mechanism [2]. The Next Generation Air Transportation System (NGATS)

and other future aircraft systems such as electric or green technology aircraft rely on the

semiconductor and solid-state components [1]. A study of the precursors of failure of

semiconductor devices has been proposed in Patil et al. [3]. In addition, the increase in

usage of lead-free technology and micro-electromechanical systems (MEMS) in the

electronic subsystems in the avionic field and NGATS increases the number of electronic

faults with perhaps unanticipated fault modes [4]. To improve the reliability in the

system level of the avionic world, the component level health needs to be assured first.

To reduce the maintenance costs and to avoid any catastrophic disasters, e.g., Challenger

or Columbia space shuttle accidents, it is of the utmost importance to understand the

behavior of degraded components to anticipate failures of embedded electronics [1].

The high power semiconductor device is one of the indispensable parts of switch-mode

power supplies (SMPS) and electrical motor drivers in the space and avionics systems.

Among these components, the insulated gate bipolar transistor (IGBT), power

MOSFETs, and capacitors exhibit the prime and significant degradation problem [4].

1

This research focuses on the analysis of the degradation process of power MOSFETs based on the collection of experimental data under an isothermal electrical overstress condition [5].
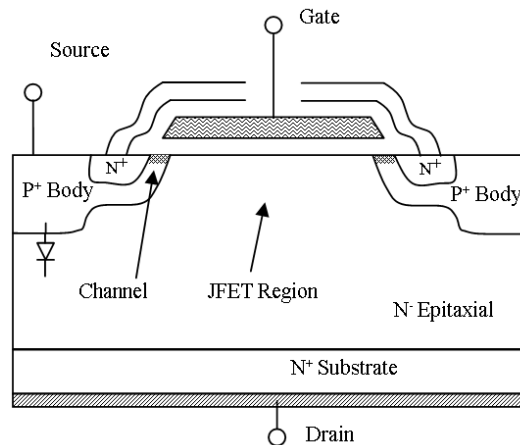
Figure 1—Structure of a typical power MOSFET. The three-terminal transistor is capable of driving high current vertically from drain to source. The doping concentration of N-epitaxial layer controls the breakdown voltage.

The vertical power metal-oxide-semiconductor field-effect transistor (MOSFET) is a three-terminal high power and high voltage transistor [6]. The structure was developed in the mid-1970s to obtain improved performance over existing power bipolar transistors [7]. The insulation at the gate makes the power MOSFET a high input impedance device compared to the bipolar junction transistor [8]. The voltage-controlled transistor is a simplified choice for circuit design over a current-controlled bipolar junction transistor (BJT) [9]. An important concern with the BJT is the inability to switch at high frequencies, leading to a destructive failure. The injected charge in the drift region was the main reason for the failure [7]. In addition, the low current gain does not support the

2

high voltages for faster switching. The Power MOSFET has become popular as it overcomes the switching issues found in circuit designs using BJTs [10]. At present, power MOSFETs with up to 600V of breakdown voltage and a maximum current rating of 28A are available in the semiconductor industry [11]. Power MOSFETs today are the devices of choice for high frequency applications (up to few hundreds of MHz) and voltages below 200V [12].

1.1   Definition of a Power MOSFET

A hexagonal field-effect transistor (HEXFET) is named so because of its hexagonal structure in cell topology, and a vertical-diffused MOSFET (VDMOSFET) is named so because the current flows "vertically" from drain to source. On the contrary, in lateral MOSFETs, the current flows laterally from drain to source. The VDMOSFET is processed with double diffusion in both P-type bases and N^+ source regions [9].

The drain and source N^+ regions are made with high doping concentration [9]. The n^+ polysilicon gate is isolated from the semiconductor by a non-conducting silicon oxide layer (see Figure 1). The semiconductor underneath the gate consists of a P-type base region, an N^- epitaxial layer, and an overlap with the N^+ source regions. The flow of current conducts from the N^+ drain to the N^+ source via the N^- epitaxial layer after the formation of an inverted channel in the P-type region [9].

The HEXFET cell structure enables the cell design to reduce the "internal specific on-resistance" closer to the ideal value. The control of the blocking voltage defines the

3

specific value of the internal resistance [9]. The lowest resistance per unit area depends on how the industry measures the specific on-resistance. The comparison between the different values of specific on-resistance associated with different cell architectures proves HEXFET to be the best structure. Low on-resistance for the vertical structure provides higher switching speed than provided by the lateral MOSFET. Thermal runaway, second breakdown, and minority carrier injection are prevented in the VDMOSFET, as it is a majority carrier device [13].

The vertical structure of the device also provides protection against high blocking voltage. The doping concentration of the N- epitaxial layer and its thickness control the blocking voltage, in contrast to a planar layer power MOSFET in which the high current is a function of both the channel width and length [6], [8]. In the vertical power MOSFET, the process of fabrication usually manipulates the region of doping concentration and the thickness of the N-epitaxial layer, whereas in the planar power MOSFETs, the silicon area is the focus to provide different current ratings [9].

1.2   Cell Topologies for Power MOSFET

The controls of the breakdown voltage and the on-resistance depend on the selection of the surface topology of the cell in a power MOSFET [7]. The improvement of the edge termination with different cell topology varies with floating field rings and field plates. Linear window linear array, square window square array, circular window square array, hexagonal window hexagonal array, hexagonal window square array, and atomic lattice

layout are the different cell topologies used and studied for the power MOSFETs [7]. Because of layout specifications based on the utilization of silicon area and the trade-off in optimization for the on-resistance and breakdown voltage, the HEXFET array for the VDMOSFET is more popular.

1.3   Differences between Lateral MOSFET and VDMOSFET

In lateral MOSFETs, the electrons start to move laterally from drain to source with the trigger of applied gate voltage; the channel depth is proportional to the gate voltage. The lateral MOSFET is a low power device, which requires a low gate signal. The major disadvantage arises from the high resistance of the channel [9]. The source of the transistor is connected to the substrate during normal operations. The pseudo-hemispherical depletion region extension from the N^+ drain without gate bias and the inflexibility of the channel length in maintaining the required ratings of the voltage make the structure unsuitable to meet the specifications for the high rating voltage and low on-resistance values [9]. To be cost-effective, the channel resistance cannot be decreased further with the limited silicon area.

The VDMOSFET or the vertical MOSFET devices are designed to switch faster in ON or OFF states [9]. They provide high impedance between drain to source with no gate bias and thus acts as a voltage-controlled power MOSFET with a high blocking voltage [8]. In the "vertically double-diffused structure," the current-carrying capability increases with reduced "specific on-resistance." It has been conclusively shown that there are

differences in the VDMOSFET and the LDMOSFET in RF (radio frequency) performance. The LDMOSFET requires a smaller silicon area than the VDMOSFET, whereas the VDMOSFET dissipates less power than the LDMOSFET. Thus, the trade-off between the transconductance and internal capacitances, and the presence of junction field-effect transistor (JFET) in series are the deciding factors in choosing between these two [17].

The device used in this research is a commercial power MOSFET from International Rectifier with HEXFET cell topology and vertically double-diffused source structure composed of both the N^+ and P-type base regions. The nomenclature from the International Rectifier of this particular power MOSFET is IRF520Npbf, where "pbf" stands for lead-free technology [14].

1.4 Characteristics of Power MOSFET

Threshold voltage is the minimum gate-to-source voltage to create a strong inversion at the semiconductor surface, large enough to first achieve the flat band condition, then to accommodate the charge in the depletion region, and finally to induce the inverted region [15]. It is noteworthy to mention that the threshold voltage decreases with temperature. Due to gate noise, the power MOSFET is highly prone to spurious turn-on [13].

Breakdown voltage is the voltage at which the body-drift diode breaks down under the reverse bias condition with gate and drain shorted together [18]. The starting of the avalanche multiplication triggers a significant amount of current flow [16]. In most of

the power devices, the N⁻ epitaxial layer supports the high-applied voltage. The thicker

or lightly doped N⁻ epitaxial layer protects the power MOSFET from the high breakdown

voltage. A lower breakdown voltage may originate from the P-type base to the N⁺ source

region for less thick or insufficient doping of the P-type base [6].

Linear region is the region in the I-V characteristics where the characteristics resemble

those of a resistance. The applied gate bias drives the current at low drain bias. Through

the continuous increase in the electric field by keeping the device under the linear region,

the electron velocity approaches saturation [7].

$$I_{DS} = \frac{\varepsilon_{OX}}{t_{OX}}(V_G - V_{TH})v_{sat}Z \tag{1}$$

where

I_{DS}	is the current from drain to source
ε_{OX}	is the dielectric constant for SiO₂
t_{OX}	is the gate oxide thickness
V_G	is the gate bias
V_{TH}	is the threshold voltage
v_{sat}	is the saturated electron drift velocity
Z	is the width of the channel

Active region is the region between saturation (ON) and cutoff (OFF); the saturation

drain current follows the following equation:

$$I_{\text{DS}} = \frac{Z\mu_{\text{ni}}C_{\text{OX}}}{L_{\text{CH}} - \Delta L_{\text{CH}}} (V_{\text{G}} - V_{\text{TH}})^2 \tag{2}$$

where

μ_{ni} is the inversion layer mobility

Cox   is the specific capacitance of the gate oxide

L_{CH} is the channel length

The effective smaller channel length due to an abrupt junction in the source increases the transconductance.

1.4.1   The Output Characteristics of the Power MOSFET

There are three regions of operations in the output characteristics of a power MOSFET. They are defined in terms of the applied bias at the gate and drain. The application of a gate voltage lower than the threshold voltage does not draw any current. This situation resembles the cutoff region. After crossing the threshold voltage, the current starts to flow. With a little increase in V_{DS} (drain-to-source voltage) the current increases proportionately. This is the linear region of operation where the current flows as a resistor. The carriers reach their maximum drift velocity with the increase of V_{DS}, and the current ceases to increase [13]. This is the active region, where the device behaves as a current generator having high impedance.

1.4.2   The Transfer Characteristics of the Power MOSFET

The change in current across drain to source (I_{DS}) with the applied voltage across gate to source (V_{GS}) is visible in the transfer characteristics of the power MOSFET. The constant

rate of change in I_{DS} and V_{DS} for a change in V_{GS} in the output characteristics suggests linear and sharp transfer characteristics [13].

The utility of a power VDMOSFET is very important from the switching characteristics point-of-view. The gate-to-source voltage (V_{GS}) or the drive voltage must exceed the threshold voltage of the device to turn it on. The power MOSFET goes from cutoff to the linear region and then to the active region and thus acts as a switch.

1.5   Literature Review

Several studies identified the leading factors of damage in the device as the precursors to different failure mechanisms. The experimental environment to analyze the degradation differed in this research from that in other studies.

The isothermal electrical stress on electronic components could result in partial damage [4]. The damage accumulated due to the applied repeated stress at the gate under high DC voltage. Moreover, the damage incurred was not large enough to render the device inoperable, but its performance and robustness were diminished [4], [12]. The accumulated stress could result in the degradation of the intrinsic properties of the device.

A model was built based on a collection of experimental observations. The data were acquired by varying environmental parameters that generated certain failure mechanisms [2], [3]. The monitoring of the changes in the intrinsic properties, which led to these

9

types of failure mechanisms, could be used to develop a model to predict the lifetime of power MOSFETs.

This study focused on the deviation of the static properties of the device from its pristine condition. The threshold voltage, the breakdown voltage, and the leakage current were the three different static properties observed. The deviation was also a measured parameter for any signs of changes in characteristics or degradation, if there were any. It also focused on any deviation in dynamic properties.

1.5.1   Prior Research on Die-Attach Damage

The study conducted by Celaya et al. used a methodology based on thermal and power cycling that triggered the accelerated aging methodology of IRF520Npbf power MOSFETs by generating the die-attach failure mechanism [5]. However, the variation of the junction temperature affected the on-resistance (R_{DSon}). In electronics reliability, thermal cycling is typically used for accelerated aging. Thermal cycling is widely used to trigger failure mechanisms related to the package of the device. In reliability, it is a common practice to accelerate a device under the required condition and to age the device to lead to failure.

The differences in the coefficient of thermal expansion (CTE) of copper and silicon generated die-attach degradation [5]. The CTE for copper was 16–18 ppm/ºC, for silicon was 2.6–3.3 ppm/ºC, and for lead-free solders was 20–22.9 ppm/ºC [5]. The flip chip

design of the T0-220 package considered copper as the substrate of the device; the chip was attached to the copper by the lead-free solder (die-attach).

The identification of on-resistance (R_{DSon}) as a precursor of failure mechanism in the die-attach was not preferable in detecting the degradation of the intrinsic parameter. The changes in the on-resistance affected all other device characteristics. This phenomenon motivated the current study that stressed the device under accelerated isothermal electrical overstress (AIEO). AIEO refers to accelerated stressing at constant temperature using electrical high potential.

1.5.2   Gate Charge Behaviors in N-channel

Following is a discussion of a study done by M. Alwan et al. in 2007 for power VDMOSFETs under positive bias temperature instability (PBTI) and high electric field stress (HEFS) [17]. The discrepancies in the result of significant intrinsic properties and inadequacy of the information for these differences provided motivation to have a setup for the AIEO.

During different accelerated tests, the research demonstrated degradation in gate charges, threshold change, and switching time. Moreover, the study was conducted at different temperatures; it analyzed the existence of defects in the gate oxide (SiO_2) and the semiconductor-gate oxide interface (Si/SiO_2) of power MOSFETs [17]. The study of degradation process mostly focused on the positive temperature bias and on the 2-D device simulation software "Atlas."

The penetration of the energetic interface carrier in the SiO_2/Si barrier and creation of charge trapping was the main proposed root cause from their study [17].

On the contrary, the device with a penetrated oxide barrier would not work properly again as a normal operating device, which motivated us to analyze it using a different method, accelerated isothermal electrical overstress (AIEO), where the temperature was held constant.

The smaller threshold shift under 500 hours of life testing and the inconsistent increase in the Miller Plateau were noted [17]. However, tests for this thesis using AIEO resulted in significant shifts in threshold voltage and the Miller Plateau.

With the increase in high gate bias, the amount of gate-to-drain charge of VDMOSFETs increased, and as a result, the Miller plateau expanded horizontally.

To analyze the failure mechanism from the perspective of intrinsic parameter degradation, it was necessary to analyze the device in a discrete manner. Moreover, the temperature variation at 150℃ might instigate package related failure mechanism. However, the research in HEFS and PBTI did not mention that clearly. It also did not have adequate information for the zero or non-zero slope as the device progressed through the degradation process. The focus of this study was to analyze the degradation process without initiating package related damages and to find the root cause of the degrading parameters of the power MOSFET under isothermal electrical overstress.

12

1.6   Hypothesis

The hypothesis of this research was that if the device under test (DUT) was overstressed isothermally with electrical high gate voltage, the behavior would show significant changes in the characteristics. The comparative analysis of the static and dynamic properties between a pristine and a stressed device should help define an approach to physics-based-analysis of the device and thus provide a model for any precursor to the changes.

The gate is the most fragile terminal among the three terminals of a power MOSFET. The hypothesis also assumed that the isothermal environmental condition would persist along the cycle of stressing the power MOSFET.

This research provided a way to determine physics-based-analysis on the rate of deviation from the behavior of pristine devices that led them to cease following ideal characteristics. The shifts in device-physics-parameters such as breakdown voltage, threshold voltage, switching characteristics, and the Miller Plateau helped lead to a decisive conclusion.

In recent years, the motivation for detecting physics-based analysis in power semiconductor devices has been driving the research in prognostics of health, reliability, and product of engineering technology.

1.7   Motivation

The health of semiconductor devices used in aeronautical and space exploration systems plays a critical role in the operation of the system [1]. Power MOSFETs are critical elements of electronic subsystems, e.g., electrical motor drivers and switched-mode power supplies, which will be used extensively in future generations of aircraft. They can handle large amounts of power and have a high switching speed [1]. Research on prognostics, or "the prediction of remaining useful life," of power MOSFETs has received much attention. The airplanes, satellites, and other space-related systems are exposed to different environmental stressors, e.g., pressure, temperature, electrical issues, lightning, radiation, and humidity. The experimental verification compared to a prognostics algorithm for the prediction of future health of the semiconductor device was critical [2].

"Prognostics" is an engineering discipline that focuses on estimation of the health state of a component and the prediction of its remaining useful life (RUL) before failure [5]. The conditions of the device parameter based on the fundamental properties compared to the collected experimental data anticipate the future usage [3].

The current research presents an accelerated isothermal electrical overstress (AIEO) method for gate-controlled power transistors [5]. The objective of the research was to differentiate the characteristics of the pristine device from the stressed device and identify the precursors of physics-based degradation or failure, if any, from the computed

indicators [18]. The development of the physics-based degradation model and the state of the health of the power devices were divided into several steps [3].

The scope of this research was to focus on the accelerated stress testing on the commercial power MOSFETS (IRF520Npbf). Conclusion from the literature review showed that experiments considering stress at the gate with pulse voltage damaged the device gate. In addition, the damage of the device depended on the thickness of the oxide [19].

On the contrary, the motivation for this research was to analyze any deviation from the pristine condition in static and dynamic characterization. The research would provide information without damaging the oxide of the power MOSFET and with high DC bias opposite of applied pulse at the gate.

The range of data collected from the experiment provided guidelines for the reliability and health of the power MOSFET for the normal and extreme operating conditions while maintaining the original input and output characteristics.

1.8   Meters and Test

The experimental part of this research was conducted in the Prognostics Center of Excellence (PCoE) at NASA Ames Research Center. The test bed for the accelerated isothermal electrical overstress (AIEO) provided the platform for the power device to be exposed under the preferred conditions. The Advanced Diagnostics And Prognostics

15

Testbed (ADAPT) at NASA Ames Research Center was the research lab to evaluate the diagnostics and prognostics for electronics, based on accelerated life testing (ALT) and high accelerated life testing (HALT) [2]. The research was done with 22 power MOSFETs manufactured by International Rectifier with a model number of IRF520Npbf. To uniquely identify each of them, they were labeled from "S0" to "S21." Each one was an n-channel power MOSFET with a maximum breakdown voltage rating of 100 Volts and a maximum current across drain-to-source of 9 Amps [14]. The isothermal block was the base of AIEO system shown in Figure 4. The power MOSFET was maintained at a constant temperature on this block by adjusting the current and voltage at the drain.

The hardware and software of the system with a LabView support allowed to measure, evaluate, and mature diagnostic and prognostic health management technologies [5].

The minimum voltage at the gate-to-source region required to turn the power MOSFET on is the threshold voltage. According to the threshold voltage specification for the power MOSFET under test, it is usually measured at the drain-to-source current of $250\mu A$ [6]. Typically, 2-4V is designed for gate drive of 10-15V [14]. The gate-to-source voltage is maneuverable by changing the doping concentration of the channel during the manufacturing process [6]. Breakdown voltage is achieved as the drain-to-source voltage at the turn-off state with a leakage current of 250uA, according to the specification [6].

The static and dynamic characterization of the power MOSFET was measured prior to and after each cycle of AIEO. These measurements were not in-situ, and they were done with Keithley 2410 source and measurement unit, which can measure up to 1100V and 1A 20W power output [5]. Any deviation of the threshold voltage (V_{TH}), the breakdown voltage (V_{BR}), and the leakage current (I_{DSS}) from the pristine condition was compared to the stressed device using the MATLAB simulation [14]. The degradation process in dynamic characteristics was verified with a turn-on circuit shown in Figure 6. The values of the parasitic capacitances were calculated from two different setups of turn-on circuit [20].

The simulation of the 2-D device processing module from "Sentaurus" TCAD tool showed the analysis for the differences in the intrinsic properties between a pristine and a stressed device.

1.9   Description of the Experiment

The reasearch begun with the characterization of a pristine device. The static parameters (threshold voltage, breakdown voltage, and leakage current) were measured with a source measurement unit on a LabView platform. The dynamic parameters (Miller Plateau and switching speed) were measured with an RC circuit following two setups, one with the gate and the drain shorted (diode-connected), and the other one with the gate and the drain not shorted. The device was being stressed under AIEO. Each stress represented a high voltage applied at the gate of the power MOSFET for an hour. After each such

17

stress, its static and dynamic properties were compared against those of a "pristine device." Afterwards, attempts were made to identify the root cause behind the changes in characteristics. The stress was applied repeatedly until a significant deviation in characteristics was observed. As sodium ions and mobile ions react differently at negative applied voltage, at the end, a single negative voltage stress was applied to the device to eliminate one of them from the real root cause of the deviation. The whole process is described in a flow chart in Figure 2.

Modeling of the value of the parasitic capacitances for the power device was calculated using MATLAB simulation and interpolation. The simulation from a TCAD "Sentaurus" module for a cell of a power MOSFET demonstrates the electrostatic potential, doping concentration, and state charge distribution. It also provides information on output characteristics and transconductance. The next chapter explains the experimental setup of this research, where the specification of the settings for this particular "Device Under Test (DUT)" describes the method followed in the experiment.
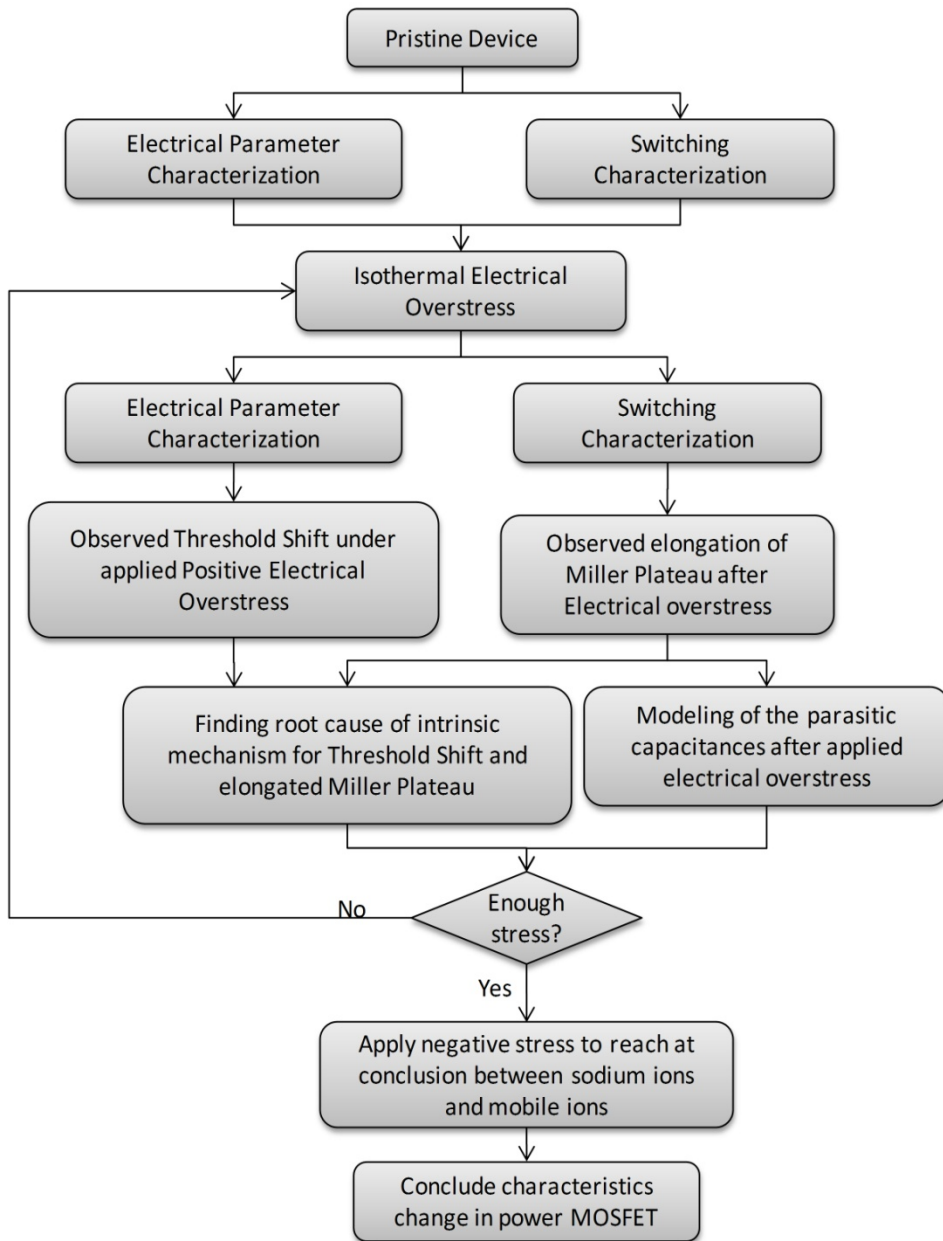
Figure 2—Research flow chart. The figure explains the steps of the experiment and the process of elimination to find the root cause.

1.10   Signs of Degradation

The hypothesis of this research predicted a deviation from the pristine transfer characteristics, structure of the Miller plateau, and switching behavior after applying electrical stresses. A device was considered to be degraded if it did not regain its pristine behavior after removal of the stress. Attempts were made to stress the power MOSFET device electrically using high positive gate voltage and then either was left out for awhile with no applied stress or with a negative stress to watch for reverting its behavior. Figure 3 shows characteristic curves with possible movements.
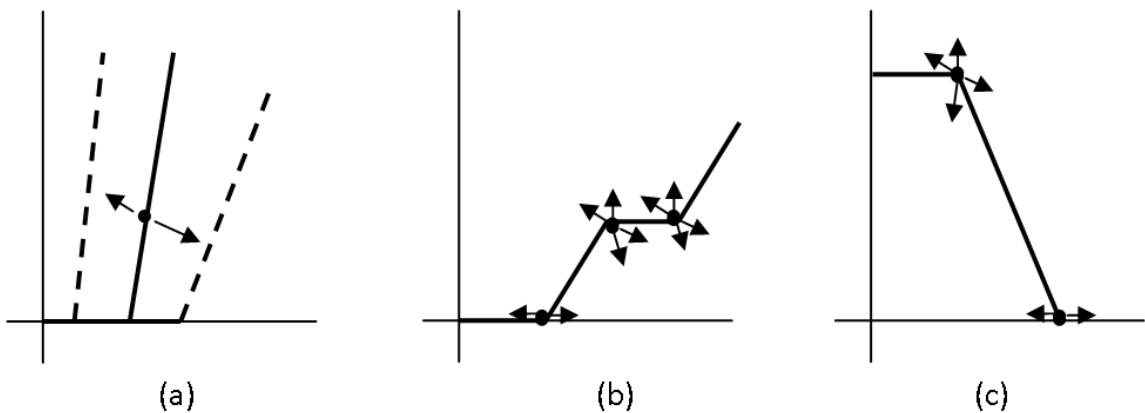
Figure 3—Characteristic curves with possible shifts. The solid line refers to pristine behavior with arrows indicating possible movements. (a) Transfer curve indicating threshold voltage, (b) Miller Plateau is the middle flat region, (c) Drain-to-source voltage indicating switching speed.

20

2   Experimental Setup

2.1   ADAPT Lab

The research was conducted in cooperation with the Advanced Diagnostics and Prognostics Testbed (ADAPT) Lab at NASA Ames Research Center. This chapter describes the hardware and software platform and the concept of operation of the testbed for this experiment. The testbed provided the platform to calculate, determine, and conclude diagnostic and prognostic health management technologies.

2.2   Methodology

The accelerated isothermal electrical overstress (AIEO) method provided manifold view of the degradation of intrinsic parameters of the device at component level. The accelerated stressing mechanism or fast induction of degradation is the most prevalent methodology in the power semiconductor industry to determine the health of the device. In reliability and product engineering, it is a method to follow a life testing for thousands of hours to find the failure mechanism of any device. According to industry specification, at least 70 devices should be stressed for 500 hours each, which would take approximately 4 years with a single test bench. In this research, each of the devices was applied stress up to 90 hours. Completing life tests for 22 devices would take few months with the provided resources. To overcome the limitation of time and resources, three important tasks were performed:

21

a) Accelerate the degradation process by applying high voltage;

b) Follow the degradation process over time after each cycle;

c) Check for reversibility of deviation in device properties after each cycle.

The assessment of the health of a component was based on the analysis under isothermal electrical overstress for this research. Overstress that can cause damage to the power devices can be of any nature, e.g., electrical, thermal, and mechanical. This study defined the isothermal electrical overstress as a setup with a high voltage applied at the electrode of the device under a constant temperature.

To detect the degradation of power devices in this research, it was necessary to parameterize the environment for useful measurement and inference of the data. Therefore, the isothermal electrical overstress had to be maintained throughout the experiment.

It was necessary to avoid failure mechanism due to extrinsic parameters such as damaging the package, by maintaining the junction temperature below the specified maximum. Thermal cycling, as an aging methodology, is regularly used to accelerate the stressing of the devices by cycling among temperatures considerably higher than those seen in normal operation [21]. Mechanical stress introduced through the thermal cycling causes damage to the package of the device.

Isothermal condition satisfies the criterion to overstress the power MOSFET explicitly under electrical stress without damaging the package by limiting maximum junction temperature [14]. In the next section, calculation to determine the junction temperature value for a single setting of applied high voltage is shown. In addition, electrical stress under junction temperature initiated degradation mechanisms due to the changes in intrinsic parameters between the semiconductor and the gate oxide.

The device under test (DUT) for this research was IRF520Npbf manufactured by International Rectifier. The maximum breakdown voltage it could sustain was 100V associated with a current rating of 9A. It was also a lead-free device. The isothermal stressing method is capable of stressing other power devices e.g. "Insulate Gate Bipolar Transistor (IGBT)," power MOSFETs from other manufacturers, and capacitors.
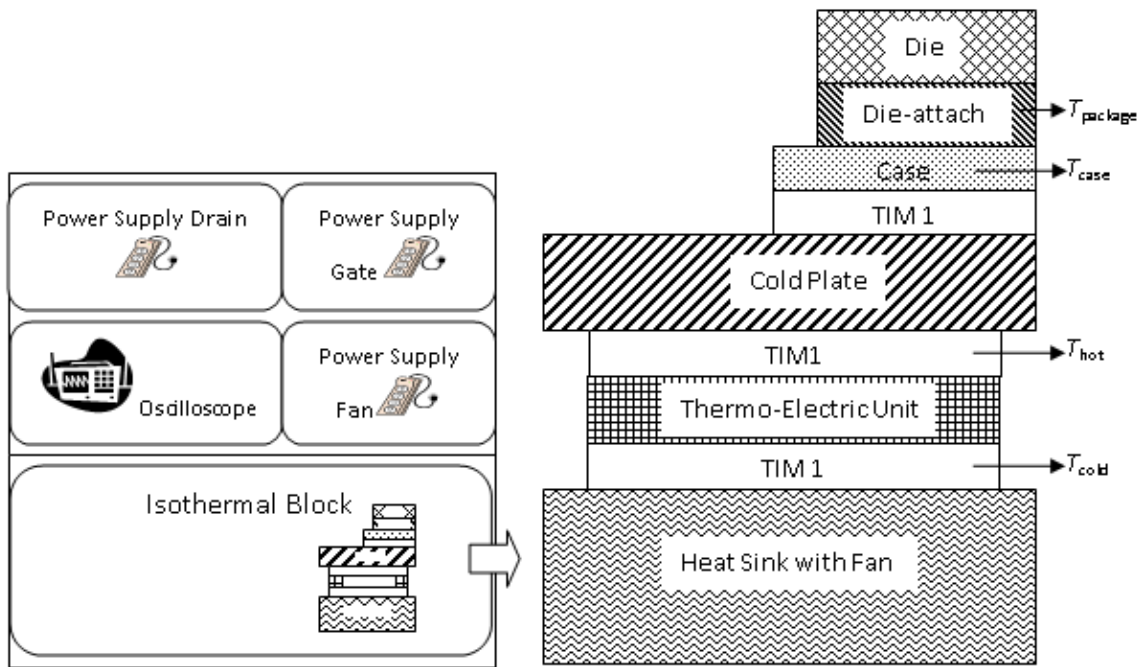
Figure 4—Isothermal setup and interface block of power MOSFET. The left rack is the setup for accelerated stress system at a constant temperature. The interface block is placed on the right side. Cold plate is a block made of copper; heat sink is made of aluminum, and the fan is connected to the heat sink at the bottom of the block. By controlling the thermo-electric unit, it is possible to maintain a constant temperature. This research was conducted at room temperature.

2.3   Isothermal Electrical Overstress Methodology

To identify an optimum gate voltage at which the device would exhibit gradual changes

without damaging the package, different voltage levels in the range of 20V~60V were

applied to four sample devices for different duration in total of 504 hours (3 weeks) under

isothermal condition. Controlling the drain voltage to maintain constant power

dissipation ensured constant junction temperature or isothermal condition.

The experimental method must accommodate controlled junction temperature for the TO-220 package for IRF520Npbf power MOSFET. The datasheet specified range for the junction temperature is -55°C to 175°C. The recommended junction (T_{junc}) temperature should not exceed the maximum specified value provided by the manufacturer to achieve an isothermal electrical condition. This would avoid generation of thermal cycle. The accelerated stressing model was estimated based on the heat conduction formula as [10]:

$$T_{\text{junc}} = T_{\text{case}} + I_{\text{DS}}V_{\text{DS}}R_{\theta\text{JC}} \tag{3}$$

where

T_{junc} is the maximum junction to case temperature of the power MOSFET

T_{case} is the case (flange) temperature of the transistor (from experiment)

$R_{\theta\text{JC}}$ is the thermal resistance for the junction-to-case of the transistor (from Table 1)

I_{DS} is the drain-to-source current (from experiment)

V_{DS} is the drain-to-source voltage (from experiment)

The power dissipation was controlled by modulating the value of V_{DS} and I_{DS}, e.g.,

$$T_{\text{junc}} = 62.58 + 7.43 \times 2.4 \times 3.1 = 117.85°C$$

Table 1—IRF520Npbf specs (thermal resistance)

	Parameter	Typical	Max
$R_{\theta JC}$	Junction-to-Case	—	3.1 °C/W
NOTE 1—This partial list includes only the parameters that are used in this thesis [14].			

Table 2—IRF520Npbf specs (electrical characteristics at T_J=25°C)

Parameter	Min	Typical	Max	Conditions
Drain-to-source Breakdown, $V_{(BR)DSS}$	100	–	–	V_{GS}=0 V, I_D=250 μA
Gate Threshold Voltage, $V_{GS(th)}$	2.0V	–	4.0 V	$V_{DS} = V_{GS}$, $I_D = 250$ μA
Drain-to-Source Leakage Current, I_{DSS}	–	–	25 μA	$V_{DS} = 100V$, $V_{GS} = 0V$
	–	–	250 μA	V_{DS}=80V,V_{GS}=0V,T_J=150°C
NOTE 1—This partial list includes only the parameters that are used in this thesis [14].				

Table 3—IRF520Npbf specs (absolute maximum ratings)

	Parameter	Max
I_D @T_C=25°C	Continuous Drain Current, V_{GS} @ 10V	9.7 A
P_D @T_C=25°C	Power Dissipation	48W
V_{GS}	Gate-to-Source Voltage	±20V
I_{AR}	Avalanche Current☐	5.7A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175°C
NOTE 1—This partial list includes only the parameters that are used in this thesis [14].		

2.4   Accelerated Stressing System Description

The electrical overstress and measurements of the static and the dynamic characterization of power devices were performed in different steps. The accelerated stressing system

was composed of DC power supply for gate bias, DC power supply for drain bias, an isothermal block, and an oscilloscope. The three terminals of the power MOSFET were connected to an NI SCC-68 connector block which was connected to host four SCC-TCO2 thermocouple modules [5]. The four thermocouples provided temperature from four different places on the isothermal block (see Figure 4). The maximum junction temperature was maintained. The oscilloscope, through a data acquisition system, recorded the high-speed measurements.

The data acquisition system was from National Instrument. PXI-1033, chasis and integrated controller was used to host the data acquisition card which was interfaced to the computer running the stressing setup [5]. The drain electrode of the power device was connected to a Xantrex XDC-150-40 DC power supply which is able to supply up to 150V and 40A [5]. The drain current was measured from the voltage output of the Hall Effect sensor.

The Agilent DSO5934A 4-channel oscilloscope measured the gate voltage, the drain-to-source voltage and the drain-to-source current. The power was also measured to assure the maximum limit to maintain the isothermal condition.

The gate electrode of the power MOSFET was connected to an Agilent DC power supply of 60V and a 1.3A rating. The voltage at the gate was the external applied stressor for the device.

The isothermal block prevented the device under test from exposure to different temperatures. As long as the package temperature remained constant within safe limits, power MOSFETs did not encounter thermal cycling, and the test environment stayed limited to electrical stresses only.

The copper plate removed heat from the package of the device and conducted it to the heat sink. The aluminum heat sink was connected to a fan to remove extra heat when necessary. The peltier unit between copper and aluminum was a thermo-electric unit. The thermo-electric unit was capable of changing the constant temperature of the isothermal block. A Tenma 72-5861 DC power supply rated to 35V and 10A was used in the current-controlled mode to regulate the heat flow and control temperature T_c [5]. Figure 5 shows the circuit in the ADAPT lab to stress the device electrically.
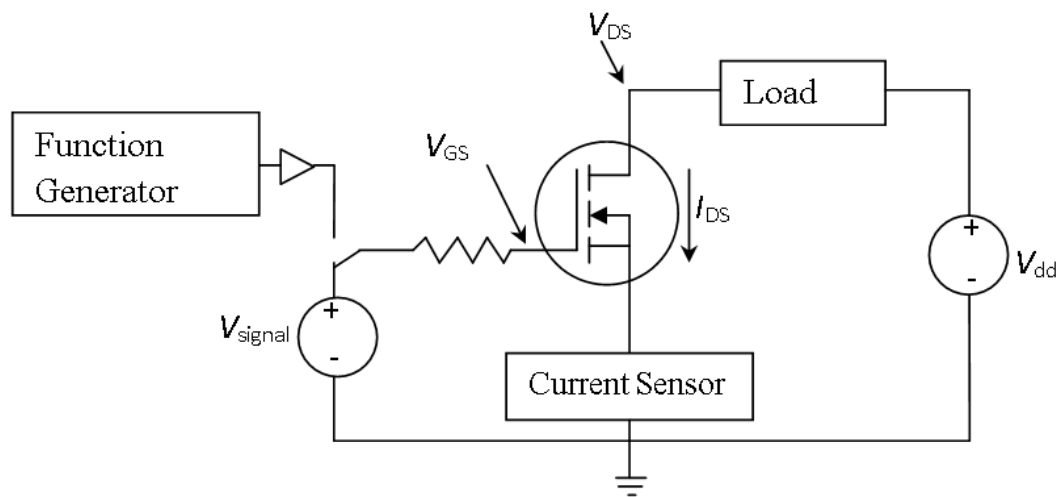
Figure 5—Schematic of stressing circuit. Electrical measurement points are labeled at different nodes and node-pairs.

29

2.5　　　Static Parameter Characterization of Power MOSFET

The following static properties of the device were measured for a pristine device after each stress cycle. The properties were threshold voltage (V_{TH}), breakdown voltage (V_{BR}), and drain-to-source leakage current (I_{DSS}). Readings were taken from a source measurement unit.

2.5.1　Hardware and Software Platform

Electrical parameters of the device were measured periodically prior to and after every stressing cycle to monitor the device degradation.

The measurements were taken using a Keithley 2410 1100V source and measurement unit. In addition, they were not maintained to be in-situ. The data display and logging were monitored by a software platform, which controlled the experiment and data display in LabView. It provided both linear and logarithmic graphical information. The data collected from the software allowed continuous visualization information from the triode region sweep through the active region of the transistor. For further comparison of the pristine device with a stressed device, the data collected from this system can be analyzed offline. See Table 4 for the limiting current and voltage values in setup.

Table 4—Specification for the characterization of the device

Test	Min Voltage	Max Voltage (V)	Current Limit (A)	Spacing	Number of Points
Leakage Current	1	120	250E-06	Linear	200
Breakdown Voltage	80	120	300E-06	Linear	200
Threshold Voltage	2	20	300E-06	Linear	200

Leakage Current is one of the parameters of the device to measure the current flowing from drain to source as the gate was shorted with the source. The gate and source were connected to the negative terminal of SMU, which was essentially the ground.

Leakage current is a parameter indicated in the specification of the device for the IRF520Npbf MOSFET as I_{DSS} [14].

Max I_{DSS}= 25uA for V_{DS}=100V, V_{GS}=0V,

Max I_{DSS}= 250uA for V_{DS}= 80V, V_{GS}=0V, T_J=150°C.

Threshold Voltage is the most critical characteristic of the device. The minimum bias at the gate to turn the transistor on is the threshold voltage. The SMU took measurements across the voltage sweep of the drain current until the point specified by the datasheet [14] at 250uA after which the current grew exponentially.

V_{GSTh}= 2V to 4V for V_{DS}=V_{GS}, I_D=250μA.

Breakdown Voltage limits one of the critical properties of a device under OFF condition. This was the breakdown voltage at which the current started to flow inside the open circuit path between the drain-to-source region under zero bias at the gate. The increase in the current after crossing a breakdown voltage of the drain-to-source provided information regarding the body diode rating.

V_{BRDSS}= Min 100 V for V_{GS}=0V, I_D=250μA.

The data collected from LabView for breakdown voltage, leakage current, and threshold voltage curves was simulated with MATLAB.

2.6   Dynamic Characterization Circuit of Power MOSFET

The following dynamic properties of the device were measured for the pristine condition and stressed condition after each stress cycle. The circuit provided in Figure 6 applied square pulse at the gate of the device. The properties followed are Miller plateau and switching speed.
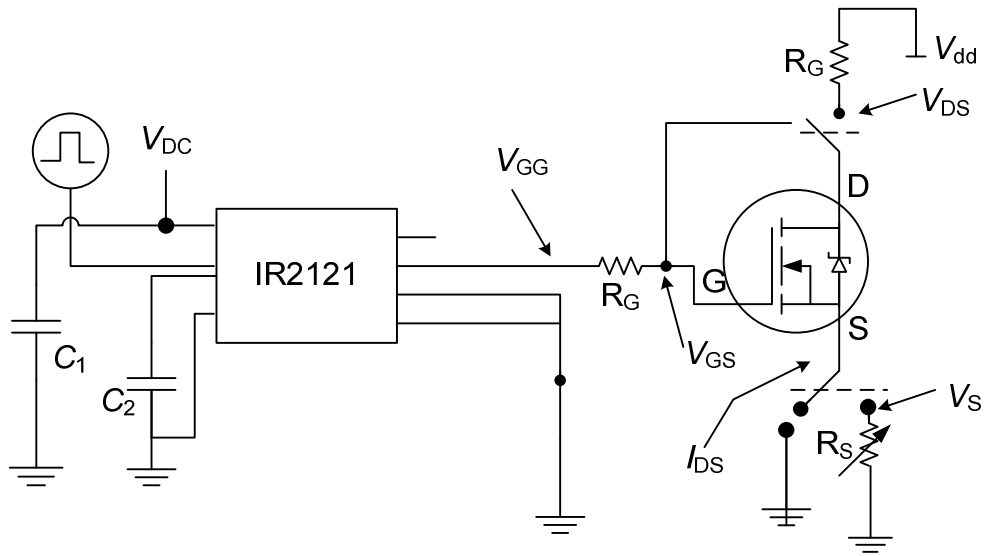
Figure 6—Circuit to verify the switching characteristics. IR2121 is a gate driver for the power MOSFET. By shorting and not shorting the gate to drain, the circuit measures the V_{DS}, V_{GS}, rise time, fall time, and Miller Plateau.

The ability of a power device to switch faster with the high frequency is a key parameter.

The process of degradation affects the switching parameter as the time constants change

over time with electrical overstress. In this part of the experiment, the turn on

characteristics of the device have been measured from two configurations, one with a

diode-connected configuration and the other one by keeping the gate and drain not

shorted. The high speed gate driver for the power MOSFET supplied voltage from 12V

to 18V. The latch immune CMOS technology enabled the circuit with overdriving

current limiting protection [14]. The usage of a circuit provided explicit calculation for

the parasitic gate-to-source and gate-to-drain capacitances.

33

3.   Unidirectional Stress and Static Characterization

The device under test (DUT) was an n-channel device with a P-type base. Positive high voltage at the gate exhibits unidirectional stress.

3.1   Optimum Value of the Electrical Stressor

After applied stress at the gate, the observation and analysis of the intrinsic properties of the power MOSFET (IRF520Npbf) was initiated by locating the "region of degradation" in the threshold voltage for the device [14]. No significant changes were observed in breakdown voltage and leakage current.

Different devices were stressed at different potentials at the gate. The maximum specified value was 20V as provided by the manufacturer. The stress applied at the gate started from 25V up to a maximum of 60V. The duration of stress varied from 30 minutes up to 19 hours.

Table A.1 shows a sample worksheet followed to keep track of stress time, applied voltage at the gate, measured voltage, and current values. The total experiment avoided the damage to the package by keeping the temperature constant and below the maximum specified junction temperature. The device was tested with a wide range of gate voltage. The range from 53V to 55V as the applied gate voltage was just the minimum to exhibit a gradual degradation process.

3.1.1 Movement under Particular Voltage

The Si atom or dopants are attached to the lattice, which requires a certain amount of energy to detach from its structure. Enough applied energy actually causes the ions to move upwards into the lattice [15]. It was observable that below some voltage, there was practically no movement over time (see Figure 23).

3.2 Apply Positive Stress

In this section, the discussion will be focused on device numbers S7, S11, S13, S14, and S15. Positive stress refers to the applied positive bias at the gate of the power MOSFET. The section explains the data collected from five devices out of 22 devices, the scope of this experiment. Electrical overstress spans over 1 hour of stressing at high voltage at the gate of the device. The characterization was compared at the beginning and at the end of each cycle.

3.2.1 Electrical Overstress at S7

Approximately 50 hours of positive stress at the gate of "S7"showed a significant shift in the threshold voltage compared to the deviation measured in breakdown voltage and leakage current. Therefore, successive shifts of threshold voltage were monitored. Figure 7 shows changes in threshold voltage behavior of "S7".

The appearance of anomalous slope and non-uniform shifts in threshold voltage suggested a significant change in the channel length with a high voltage to turn it on (see Figure 9) [19]. Because of repetitive applied positive stresses, more and more acceptors

35

were moving toward the surface with a huge amount of energy that was not uniformly

distributed [21].

ΔV_{TH} is a measure of the difference in V_{TH} values measured after two consecutive stresses

of the device under test (DUT). The movement of the transfer curve appeared to be non-

linear compared to stress time.
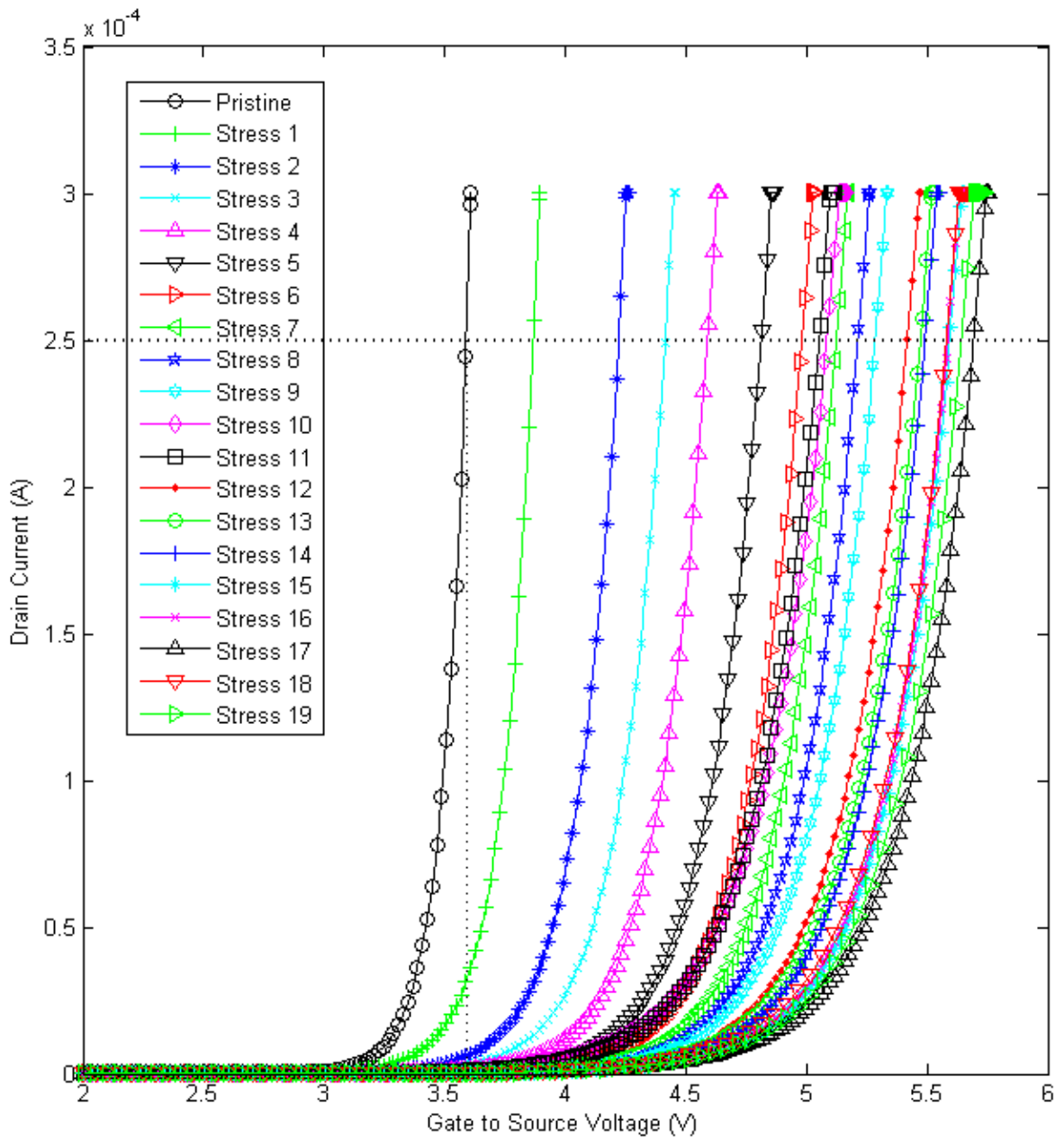
Figure 7—Progression of threshold shift after approximately 50 hours of positive stress (S7). ΔV_{TH} between consecutive stresses became smaller with more stresses. The congested curve demonstrates a channel followed by a non-distributed region of implanted ions after repetitive applied stress.

Near-Zero movement of transfer curves after a certain number of stressing is visible in Figure 7 and Figure 8. After the first few cycles of stressing, the transfer curves of the device moved significantly faster than the later stressing cycles. To an extent after the repetitive stressing, it was expected to show some diminishing returns of the ions [22]. The field strength dropped off until it reached a particular threshold voltage and balanced the applied electrical stress to move the ions further as the field strength became distant from the gate [16].

The electrical potential energy decreased as it went deep into the device and the field dropped off as it followed deep into the silicon. Balancing off between these two is associated with a huge capacitance at a short distance with high field [15].

Essentially, after some point, these ions were not able to move anywhere. They just appeared as a crowded transfer curve, as observed. The theory to support the analysis is that after the repetition of the experiment, ions reach so close to the gate that there is not enough room to move further.

3.2.2 Electrical Overstress at S11

Progression of threshold shifts for "S7" was not distinct enough to identify each progression, especially after several stress cycles. Figure 8 shows a clearer picture with only a few stress cycles for S11.
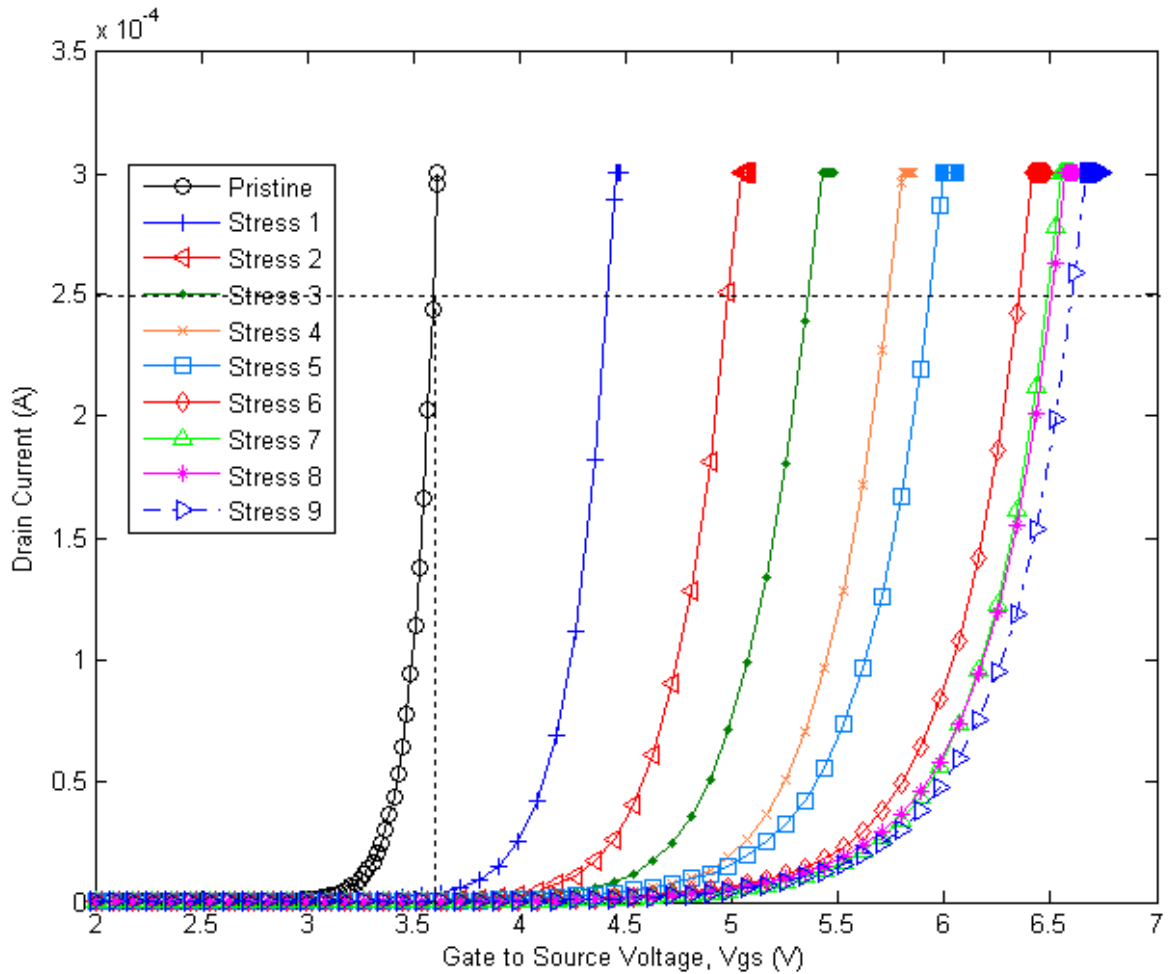
Figure 8—Progression of threshold shift after approximately 10 hours of cumulative positive stress (S11).The accelerated isothermal electrical overstress illustrates a change in the shape of the transfer curve of an n-channel power MOSFET.

The following is a discussion of the analysis made after the observation of the applied

stress at the gate under an isothermal condition for the "S11" device. The decrease in the

slopes of transfer curve with stress in Figure 9 indicates the modification of the

characteristics of the power MOSFET and the redistribution of the ions [22]. The

appearance of the stress cycles with a high threshold voltage and an anomalous slope

suggested a significant change in the channel with a high voltage to turn it on. With the

cumulative applied positive stress, the increased number of acceptor ions moving towards

the surface possessed enough energy with a nonlinear distribution [23]. It made the

change of slope non-uniform as well.
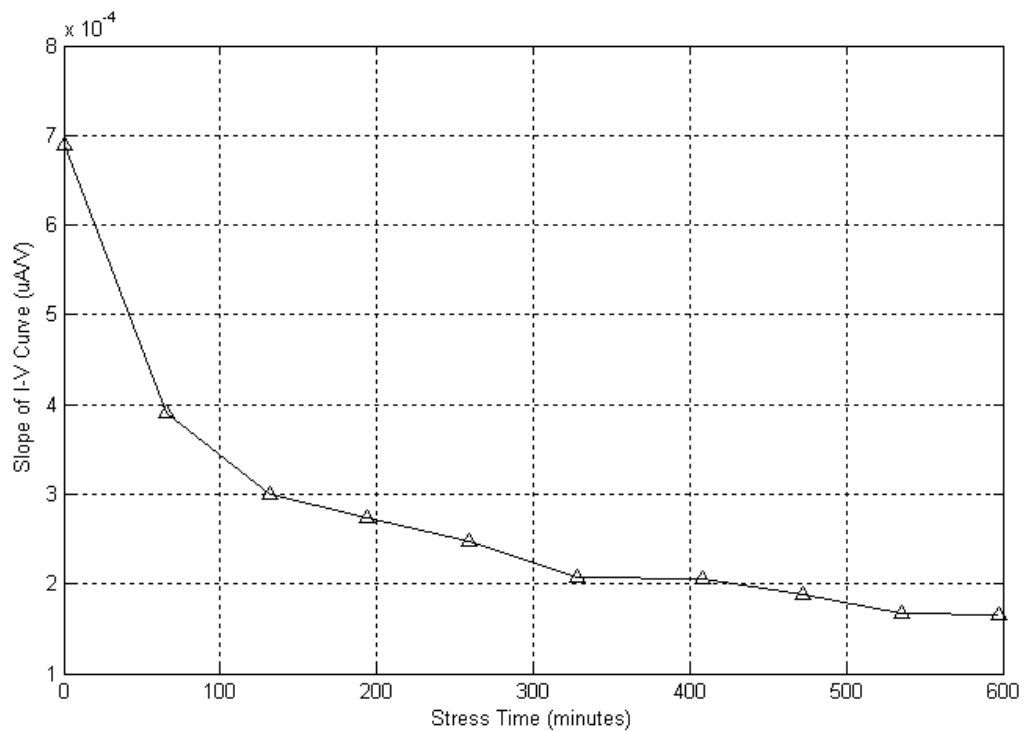
Figure 9—Degradation of slopes in transfer curve over applied stress (S11).

40

3.3 Definition of the Threshold Voltage

The threshold voltage relates to the doping profile of a device, and it depends on oxide thickness and flat band voltage. The ion implantation or the dopant density is not uniformly distributed throughout the bulk of the semiconductor [15]. From the device physics point of view, it is necessary to define the mechanism of the threshold voltage inside the semiconductor, oxide, and polysilicon area. Silicon crystal is a good insulator in its pure form. It has four valence electrons in its outermost shell.

The doping concentration (N_A) is calculated from the measured values of the threshold voltage (V_{TH}) and the analysis of the convergence method, which satisfies the equation of threshold voltage for the power MOSFET [7].

$$V_{TH} = \frac{\sqrt{4\varepsilon_s kTN_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{4}$$

Adding impurity atoms or dopants to the semiconductor changes its conduction properties. Among these dopants, phosphorous, antimony, and arsenic are major donors with five valence electrons in their outer shell to produce n-type semiconductors [15]. The atoms from the group IIIA of the periodic table with 3 valence electrons at the outer shell can accept one electron or can share one 'hole' to produce p-type semiconductor. The most commonly used acceptors are Boron, Aluminum, and Gallium.

In the beginning of the conductivity, a depletion layer is formed when the gate bias is increased from its off state, and the majority carriers are repelled from the surface of the semiconductor. After the diffusion of electrons from the n-side to the p-side of the junction and the formation of space charge regions, the available electrons are repelled by the negative ions on the p-side and attracted by the positive ions on the n-side. The depletion region consists of immobile positive donor ions developed from removing electrons on the n-side and immobile negative acceptor ions created by the filled holes on the p-side by the diffused electrons from the n-side. These ions are locked in the silicon lattice by the Coulomb force and prevent further migrations of free carriers under no added bias through the gate electrode [15]. The balancing and nullifying of the gate charge from both sides of the depletion layer of the space charge region need to be overcome with some additional voltage called threshold voltage. The process of balancing or inhibiting mobile carrier movement continues to cross the depletion region until the threshold is reached [24].

The drain current starts to flow after the channel of electrons is formed under the VDMOSFET gate electrode among the P-base and the N^+ source region [7]. Inversion is a process of conductivity not from the intrinsic n-type semiconductor surface with electrons as a majority carrier. Rather, inverting an originally p-type semiconductor base region under a particular applied bias that has experienced changes in its intrinsic

42

properties by doubling the intrinsic surface potential to its metal-oxide-semiconductor surface potential is the key to the basic functionalities of the power MOSFET.

The scope of this experiment was to stress the gate first at the saturation level and then to drive the device in the linear region. This inversion layer channel provided a path for transport of electrons from the source to the drain when a positive drain voltage was applied [7]. In this experiment, at first, a positive voltage was applied at the drain, which ensured the transportation of electrons after the formation of the channel.

3.4 Fixed and Mobile Trap Charges

The orientation and the density of four different types of charges that are present in both the insulator and the semiconductor-insulator interface of the device also affect threshold voltage of a power MOSFET. The charges are (1) fixed oxide charge, (2) oxide trap charge, (3) alkali metal mobile ionic charge, and (4) interface charge [25].

This research mainly focused on finding the root cause and analyzing the charges present in the interface layer and inside the oxide [15].

3.4.1 Alkali Metal Mobile Ionic Charge

Charges that are incorporated in the oxide from the process of the device are mobile in nature. The presence of these alkali metal ions, depending on the density, orientation, and distance from the semiconductor lattice, induces negative charges in the interface. The problem in the threshold voltage change and net charge transfer caused by the

presence of mobile ions was identified in the mid 1960's. The instability caused by these positive mobile ions was discovered at low temperature range (between 150^0–200^0C) [7]. Among the ionic impurities, sodium (Na+), potassium (K+), and hydrogen (H+) are common. However, sodium is the most commonly available alkali metal ion in the environment. The cleaning solvent for wafers introduces mobile ions like sodium. The human body rejects sodium chloride. In VDMOSFET technology, the use of potassium hydroxide-based etchant solution to prepare the V-groove introduces potassium ions in the gate [7].

3.4.2 Fixed Oxide Charge

Fixed oxide charges are the charges present inside the interface of the oxide. The oxidation step of the cooling process under particular temperature and ambience leaves some of the incomplete Si bonding to form as a sheet of fixed oxide charge. Moreover, they are not reactive to the electrical disturbances. From the study of the interface state charges, it has been determined that the lowest amount of fixed oxide charges is observed with crystal orientation {100} [23].

3.4.3 Oxide Trapped Charge

Due to the imperfections in the SiO_2, the trapped electrons or holes in the bulk of the oxide introduce oxide trapped charges. The process of avalanche injection and ionizing radiation may also induce trapped charges [16].

3.4.4 Interface Trapped Charge

The gray zone between the semiconductor and the oxide is the interface zone. The interface trapped charges may be positive or negative in nature and electrically reactive to the bias. The abrupt discontinuation of the crystal lattice introduces this kind of charge. Structural issues, radiation, oxidation, or other kinds of bonding disruptions are the main causes [25].

3.5 Analyze Threshold Shift from Different Perspectives

3.5.1 Difference in Work Function

Among the four terms in the threshold voltage, the flat band potential consists of work function difference between metal and semiconductor, and fixed oxide charge per specific capacitance of the oxide area. Modern technology with orientation {100} has maintained the elimination of the fixed oxide charges during manufacturing [23]. Also with the applied positive high voltage at the gate, it eliminated the effects in work function difference as well [26].
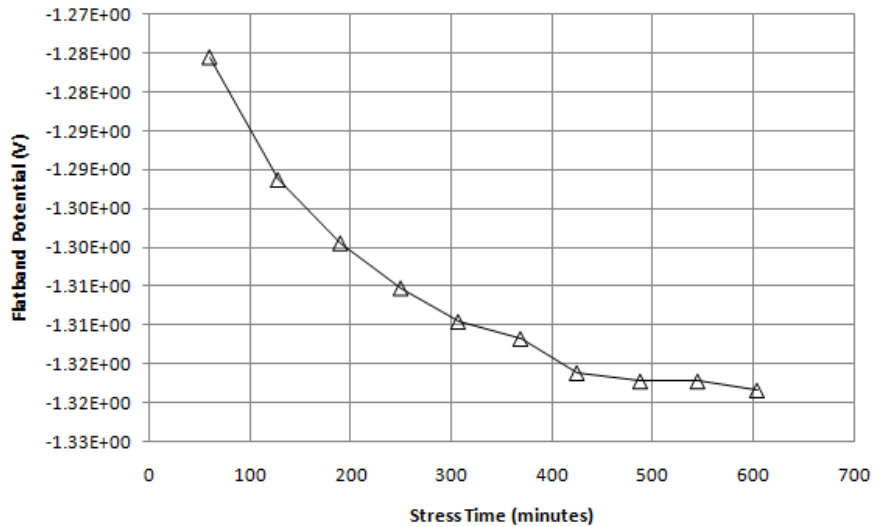
Figure 10—Flat band potential over cumulative stress time (S11). Under accelerated isothermal electrical overstress, the flat band potential does not change significantly to cause any shift in the threshold voltage.

The flat band potential of the stressed device was unchanged after a certain amount of inversion of the channel. The unchanged flat band voltage from the graph assures that the threshold shift due to stressing was not affected by the work function difference.

3.5.2 Polysilicon Material and Effect in Threshold Shift

The n+ polysilicon behaves like a metal for its high doping concentration. It is a common practice to use the n+ polysilicon (usually phosphorous) with the N-type silicon in the power MOSFET architecture. The sustained high temperature during the doping injection allows the process to create submicron channels without high-resolution lithography. The change in the threshold voltage observed in this study was not related to any temperature sustainability error from the already proven refractory polysilicon gate.

46

Moreover, a constant temperature was maintained throughout the experiment, and the device was stressed under a high gate voltage [7].

3.5.3 Impacts of Threshold Voltage Shift on Number of Acceptor Ions

The crowded curves of the shifted threshold voltage over the cumulative stressing might appear from the saturation of the redistribution of the mobile acceptor ions. Electrons transport through the N-drift region after crossing the channel [7]. Across the relatively narrow JFET region after the N^+P region, the electrons encounter increase in internal resistance. The non-uniform distribution of currents throughout the N-drift region increases the probability of non-uniform distribution of the mobile ions or acceptors [23].
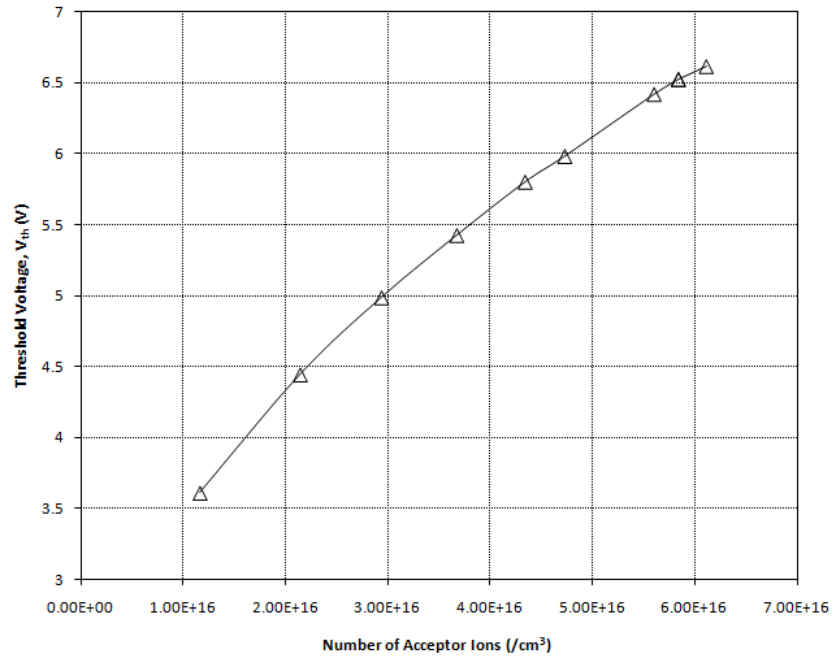
Figure 11—Distribution of mobile career over cumulative stressing.

47

The calculated doping concentration in this experiment was the acceptor level of the P-type base region of the power MOSFET. It is evident from Figure 11 that the doping concentration of the acceptor ions increased over the cumulative stressing time with the threshold voltage. The accommodation of the excess number of acceptors in the region drove the power MOSFET to draw more current to turn the compensated inverted channel.
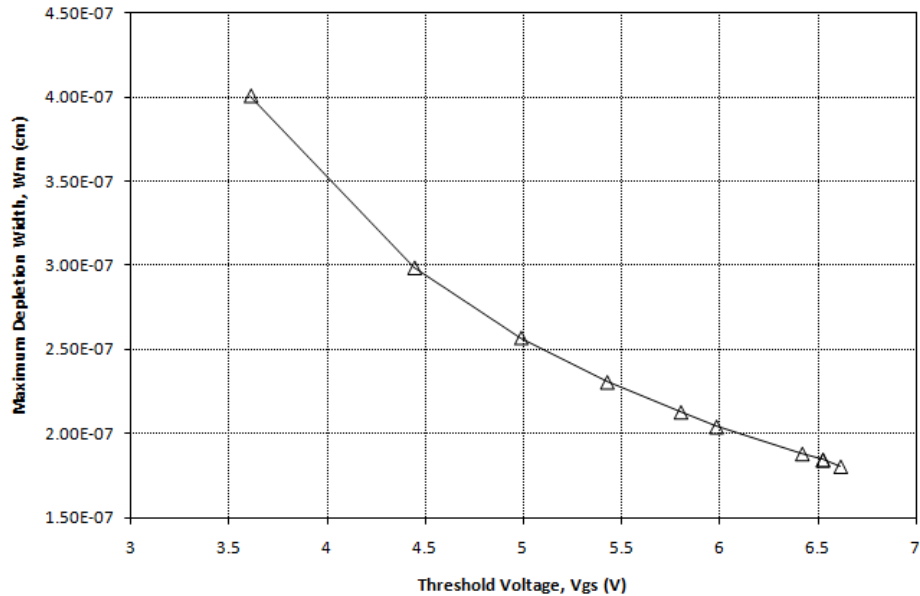
Figure 12—Decrement of depletion layer over increasing threshold voltage.

Maximum depletion width decreased with the electrical stressing over time. The increment in threshold shift after the first stressing was significant, and the increment became smaller with the number of stressing. The width of the depletion layer followed a

pattern of nonlinear decrement. Figure 12 suggests a nonlinear distribution across the device.
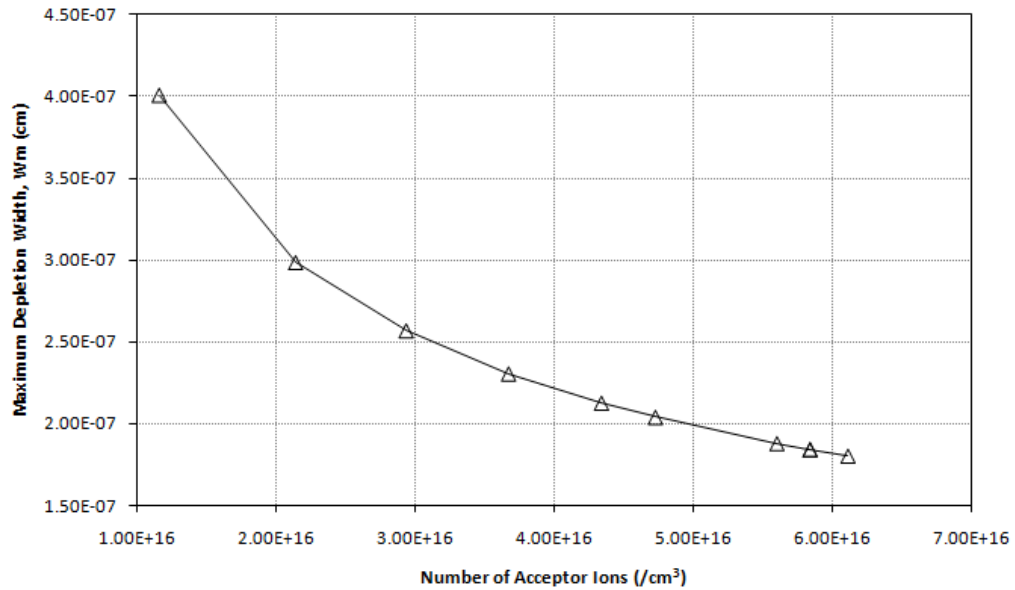
Figure 13—Maximum depletion width versus concentration of acceptor ions.

The width of the maximum depletion region decreased as the number of acceptor ions increased in the region of the device under a particular bias at the gate as depicted in Figure 13. The potential energy across the depletion layer prevented the mobile carrier from crossing from the N^+ to the P-type base region [17]. Under high electric potential after cumulative number of stressing at the gate, the mobile ions acquired enough energy to create a channel.

4.   Unidirectional Stress and Dynamic Characterization

The power MOSFET is popular for the ability to switch faster. The dynamic properties of a device are to measure the turn-on and turn-off transition information, the rise and fall of drain-to-source voltage, and the width and shift of the Miller Plateau [27]. This chapter models different capacitances measured before and after each positive unidirectional stress.

4.1   Definition of the Intrinsic Capacitances

During the on operation of a power MOSFET, the current flow is defined only through one carrier and is called a unipolar device. This carrier is the electron for n-channel. The lack of minority carrier injection at a reduced gate bias, initiates a diminishing current flow. The dielectric relaxation time is the time the majority carrier density takes to return to equilibrium in a semiconductor. It follows the following equation [7]:

$$\tau_{\mathrm{d}} = \frac{\varepsilon_{\mathrm{S}}}{\sigma_{\mathrm{S}}} \tag{5}$$

where

ε_{S} is the permittivity of the semiconductor

σ_{S} is the conductivity of the semiconductor

The relaxation time defines the switching speed of the device. From the architecture of the power MOSFET, it is visible that cells associate with different kinds of capacitances

50

parasitic to the device, which in turn controls the switching speed [7]. The application of the gate voltage changes the channel from accumulation to depletion, then depletion to inversion, and finally leads the device all the way to the region of saturation. The different drain and gate bias account for different capacitances in the device [27]. The increment and decrement of the depletion region of the power MOSFET are associated with turn-on and turn-off conditions. From the basic definition of the capacitance, the stored charge across two capacitor plates resembles the gate electrode and semiconductor separated by the gate oxide.

4.2 Capacitance by Applied Stress

4.2.1 Accumulation Capacitance for the Applied Negative Bias

The n-channel is formed between the N^+ source and the P-type base region of an n-type power MOSFET. Mobile holes move from the substrate towards the semiconductor-oxide interface during the negative applied bias at the gate, which gives rise to an accumulation layer. An accumulation capacitance is measured as the oxide capacitance. Accumulation capacitance would be of importance for this research during the application of negative stress at the gate [7].

$$C_{ACCUM} = C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \tag{6}$$
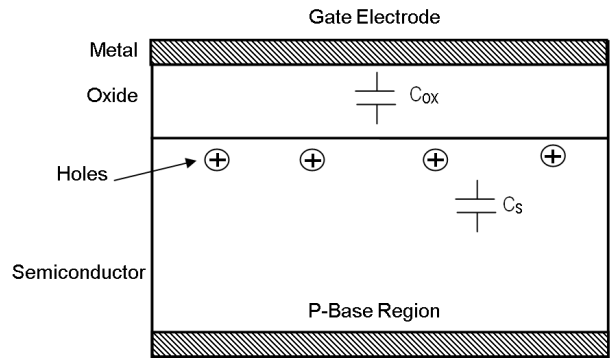
Figure 14—Accumulation with negative bias.

4.2.2   Depletion Capacitance for the Applied Positive Bias

Ionized acceptors or negative charges gather after the application of positive gate bias.

The depletion layer is formed near the P-type base region. The total depletion

capacitance is the series combination of gate oxide capacitance and depletion capacitance

[7].

$$\frac{1}{C_{\mathrm{DEPL}}} = \frac{1}{C_{\mathrm{OX}}} + \frac{1}{C_{\mathrm{S}}} \tag{7}$$
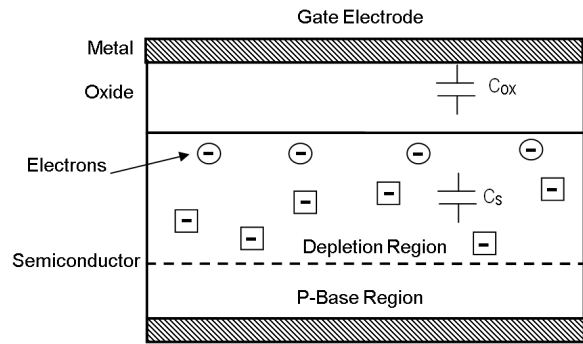
Figure 15—Depletion and inversion at positive bias.

52

4.2.3   Inversion Capacitance for Applied Positive Bias

The inversion layer is formed under the gate oxide region of the power MOSFET. The region of inversion starts through the P-type base region and expands up to the N^+ source region. The current flows from the N^+ source to the P-type base circulating the N^- drift and N^+ substrate by connecting the drain [7]. The gate oxide capacitance also needed to be considered in calculating the inversion region capacitance as the mobile electrons move around just below the oxide. Inside the bulk of the semiconductor, the depletion layer is formed across the N^- drift region even during the inversion. Consequently, the calculation of the capacitance under the inversion effect had to include both the gate oxide capacitance and the bulk depletion capacitance [28]. For the accuracy of the minimum associated depletion capacitance, the maximum depletion width needed to be incorporated [7].

$$\frac{1}{c_{\text{INV}}} = \frac{1}{c_{\text{OX}}} + \frac{1}{c_{\text{SMIN}}} \tag{8}$$

4.3   Modeling of Static and Dynamic Capacitances

First, it was important to define the capacitances from their switching performance of the device. International Rectifier Inc. datasheet for the HEXFET power MOSFET IRF 520Npbf presents the values of the internal capacitances that change with the applied voltage, e.g., C_{gd}, C_{ds}, and C_{gs}. These are the capacitances respectively calculated at the gate-to-source, gate-to-drain, and drain-to-source. These are defined from the structure of the device.

53

Industry specification prefers to determine the different capacitances by measuring them directly from the transistor [9]:

C_{iss} = input capacitance, drain and source terminal shorted,

C_{oss} = output capacitance, gate and source shorted,

C_{rss} = reverse transfer capacitance, gate and source shorted [10].

The relationship between these capacitances is described below:

$$C_{iss}=C_{gs}+C_{gd} \tag{9}$$

$$C_{oss}=C_{gd}+C_{ds} \tag{10}$$

$$C_{rss}=C_{gd} \tag{11}$$

To achieve a fundamental idea of the intrinsic and parasitic capacitances of the power MOSFET, it was important to consider the main capacitances that influence the turn-on and turn-off characteristics of the device.

4.3.1 Gate to Source Capacitance, C_{gs}

This capacitance is comprised of three different components of parallel capacitors. The gate-to-source capacitance is mostly dominant by the overlap capacitance between

polysilicon gate and metal covering the source and the gate region. The source region

has high doping concentration of the N^+ diffusion and the P-type base regions [9].

$$C_{gs}=C_{ovN+}+ C_{ovP}+C_{ovM} \qquad (12)$$

Among the three components, the overlap capacitance between the N^+ diffusion and

metal remained constant, whereas the overlap capacitance between the P-type base and

the polysilicon gate varied with the change in drain and gate bias. The different values of

this capacitance were measured from two combinations of an RC circuit. Figure 16

illustrates the trends of this capacitance before and after the application of the electrical

overstress of the device.

4.3.2 Gate to Drain Capacitance, C_{gd}

The gate-to-drain capacitance is characterized from the dependencies of both the V_{GS}

(gate-to-source voltage) and the V_{DS} (gate-to-source voltage). From the region of

operation, C_{gd} is an important property. The power MOSFET operates from triode,

saturation, and cutoff to work as a switch [28].

$$C_{gd}=C_{gdsi}+C_{gMill} \qquad (13)$$

where

C_{gdsi} is the capacitance that originates from the overlap between the semiconductor regions beneath the polysilicon gate. In this experiment, the values of the capacitances were measured before and after each electrical overstress.

C_{gMill} is the capacitance that varies nonlinearly with the drain voltage and dominates the output switching through the Miller effect. The values of the capacitances at different drain voltages were also measured from the numerical interpolation of the doping concentration of the power MOSFET. This capacitance is associated with the deep depletion region of the N-drift or the JFET region [29]. It depends on the specific capacitance of the gate oxide C_{ox}.

4.3.3 Drain to Source Capacitance, C_{ds}

The capacitance between drain and source varies with the square root of the sum of the drain bias and built-in potential. The depletion layer under the gate-oxide region is larger than the depletion layer across the N-drift region. This depletion arises from the junction of P-type source and N-type drain, which contributes to the reverse transfer capacitance of the power MOSFET.
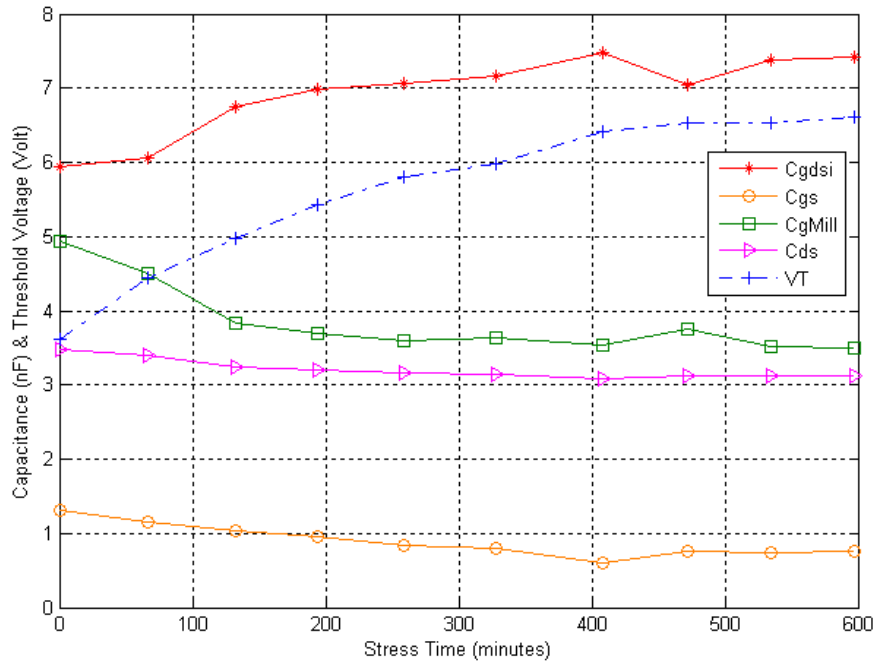
Figure 16—Different types of capacitances over stressing time (S11).

With the increasing value of the threshold voltage over the cumulative stressing, the value of the gate-to-source capacitance C_{gs} decreased. The capacitance right beneath the gate-to-drain with silicon C_{gdsi} increased over the stressing time. The increment of the gate-to-drain with silicon capacitance C_{gdsi} over the stresses showed a significant change in the depletion region [27]. The capacitance reached the maximum value associated with the minimum depletion width.
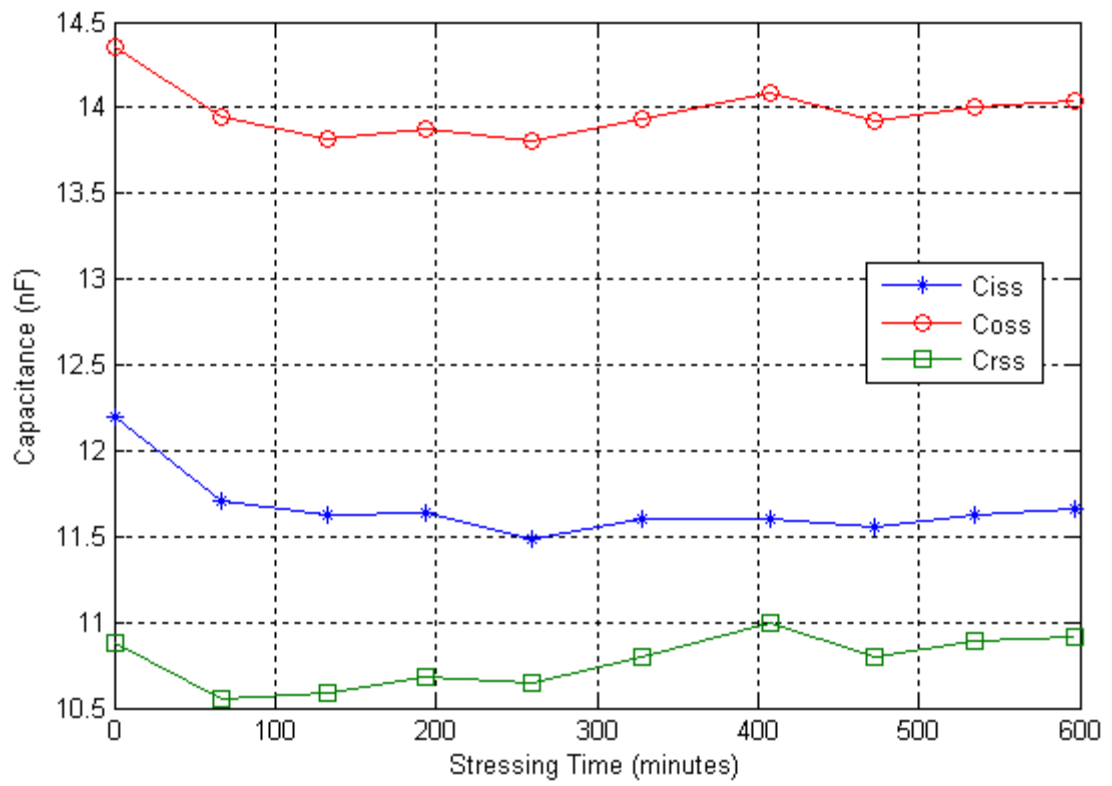
Figure 17—Approximation of C_{iss}, C_{oss} and C_{rss} for the device.
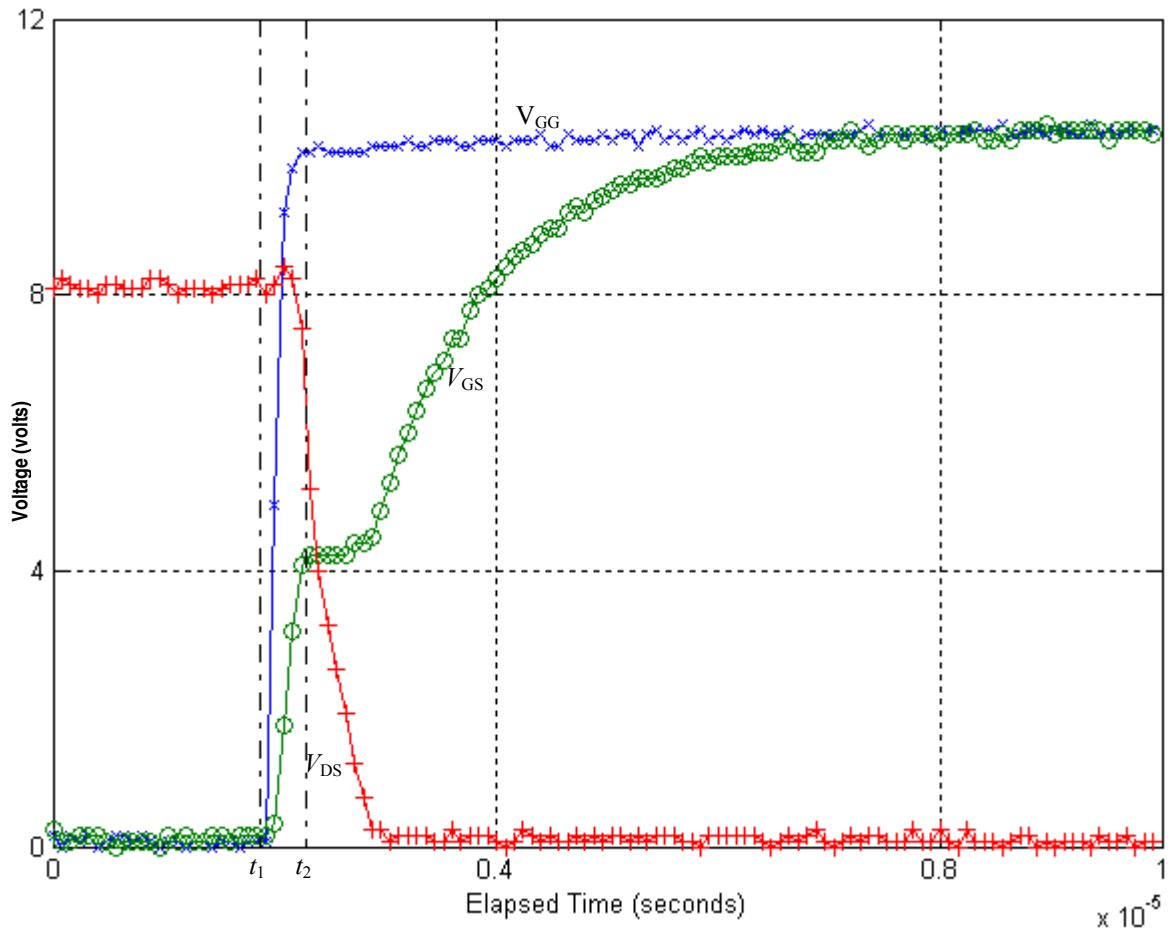
Figure 18—Switching characterization of a pristine device (S19). t_1 is the time when threshold begins and V_{GS} starts to increase. The current I_{DS} also increases linearly. At the beginning of the Miller Plateau, the voltage between drain and source starts to fall and switching begins.

Figure 18 shows an output of the switching circuit with the gate and drain not shorted

showing dynamic characterization of the power MOSFET. The voltage across the drain-

to-source dropped abruptly at the beginning of the Miller plateau from its highest value.

4.3.4 Experimental Values of the Capacitances

Required equations for the capacitance calculation after each stressing cycle were followed carefully [27].

$$t_1 = \left(R_g + R_{gapp}\right)\left(C_{gs} + C_{gdsi}\right)\ln\left(\frac{1}{1-\frac{V_{TH}}{V_{GS}}}\right) \tag{14}$$

$$t_1 = \left(R_g + R_{gapp}\right)\left(C_{gs} + C_{gdsi}\right)\ln\left(\frac{1}{1-\frac{V_{TH}}{V_{GS}}}\right) \tag{15}$$

$$t_3 = \frac{(V_{DS}-V_F)(R_g+R_{gapp})C_{gdsi}}{V_{GS}-V_{GP}} \tag{16}$$

where

t_1 is the time to cross threshold voltage

t_2 is the time to reach the beginning of the Miller Plateau

t_3 is the duration of the Miller Plateau

R_g is the internal gate resistance

R_{gapp} is the external gate resistance

C_{gs} is the capacitance between gate and source

C_{gdsi} is the capacitance between polysilicon gate and semiconductor region

$C_{iss}=C_{gs}+C_{gd}$ =14.75 nF

$C_{oss}=C_{gd}+C_{ds}$ =12.25 nF

$C_{rss}=C_{gd}=11$ nF

4.4   Significance of Change in the Miller Plateau

The ability to switch at high frequency is one of the important properties of a power

MOSFET. The degradation in switching ability provided information for the degradation

of the intrinsic properties of the device [27]. From the experimental observation of the

stressing of the device under high electrical overstress, a change in the Miller Plateau was

significant. The RC circuit to measure the "switch on" characteristics of the device was

used in two different setups before and after each set of the stress cycle:

a) Gate and drain not shorted together

b) Gate and drain shorted together

It was visible that the Miller Plateau in the pristine device was short and flat. As the

threshold shifts appeared to be larger and larger over the stress cycle, the plateau

expanded horizontally associated with a slope. At an extent where the device stopped

switching after reaching a threshold voltage of 9.49V, the Miller Plateau expanded to its

largest elongated length (see Figure 21). The elongated Miller Plateau increased the

61

required time for the drain-to-source voltage to collapse and to proceed for the turn on region. [30]

From the equation $Q=CV$, it is visible that the charge around the Miller Plateau became larger as the value of the capacitance between gate-to-drain increased over the stressing cycle. The length of the Miller Plateau also depended on the value of the applied bias between gate and drain [27]. The drain-to-source current reached at maximum value at the Miller Plateau.

The zero-gradient slope of the pristine device of a Miller Plateau appeared with a non-zero-gradient slope as the number of stressing cycles increased. The zero-gradient slope would assure the total drive current flowing into the gate-to-drain region capacitance. However, the nonzero-gradient slope indicated the sharing of the drive current between gate-to-source capacitance as well. The significant current through the C_{gs} maintained the constant value of C_{gd}. Moreover, the compensation of charges between the gate-to-source capacitance and gate-to-drain capacitance right after V_{DS} (drain-to-source voltage) entered the turn–on region, changed the slope to a less steeper form than the region of t_1 & t_2 [27]. C_{gd} became larger beyond the Miller Plateau compared to its value before reaching the plateau (see Figure 16).

Intrinsically, the capacitance C_{gd} $(=C_{gdsi}+C_{gMill})$ increased with the decrease in the depletion width. The depletion reached maximum at the saturation level of the drain-to-source current.

5.　　Bidirectional Stress and Characterization

Attempts were made to identify the root cause behind the changes in characteristics of power MOSFETs. The stress was applied repeatedly until a significant deviation in characteristics was observed. Unidirectional stressing in the previous chapters was not sufficient to analyze many aspects of the root cause associated with the degradation. Shifts in the threshold voltage and changes in the properties of the transfer curve have a twofold meaning for the researchers. "Alkali metal (sodium) mobile ionic trap charge" and "mobile implanted ions" were the two possibilities [15]. Theoretically, sodium ions and mobile ions react differently at a negative applied voltage. Therefore, the device was stressed under equal and unequal positive and negative stress to eliminate one of the root causes from the possible real root cause of the deviation.

5.1　　Negative Stress

According to the assumption, if a pristine device is stressed under a negative bias, the stress should distort the curve. Because of the channel distribution, the stress cleared out a region of the channel and caused a set of mobile acceptor ions to move deep into the lattice [16]. The ions moved deeper into the region of the high implantation area as the conduction became more intense. As a result, more current was drawn from the zone [19]. At this point, the device characteristics reverted to a pristine transfer curve. Showing threshold change in both directions by applying a positive and a negative stress

might show evidence of the movement of the "field strength" toward positive and

negative as well.
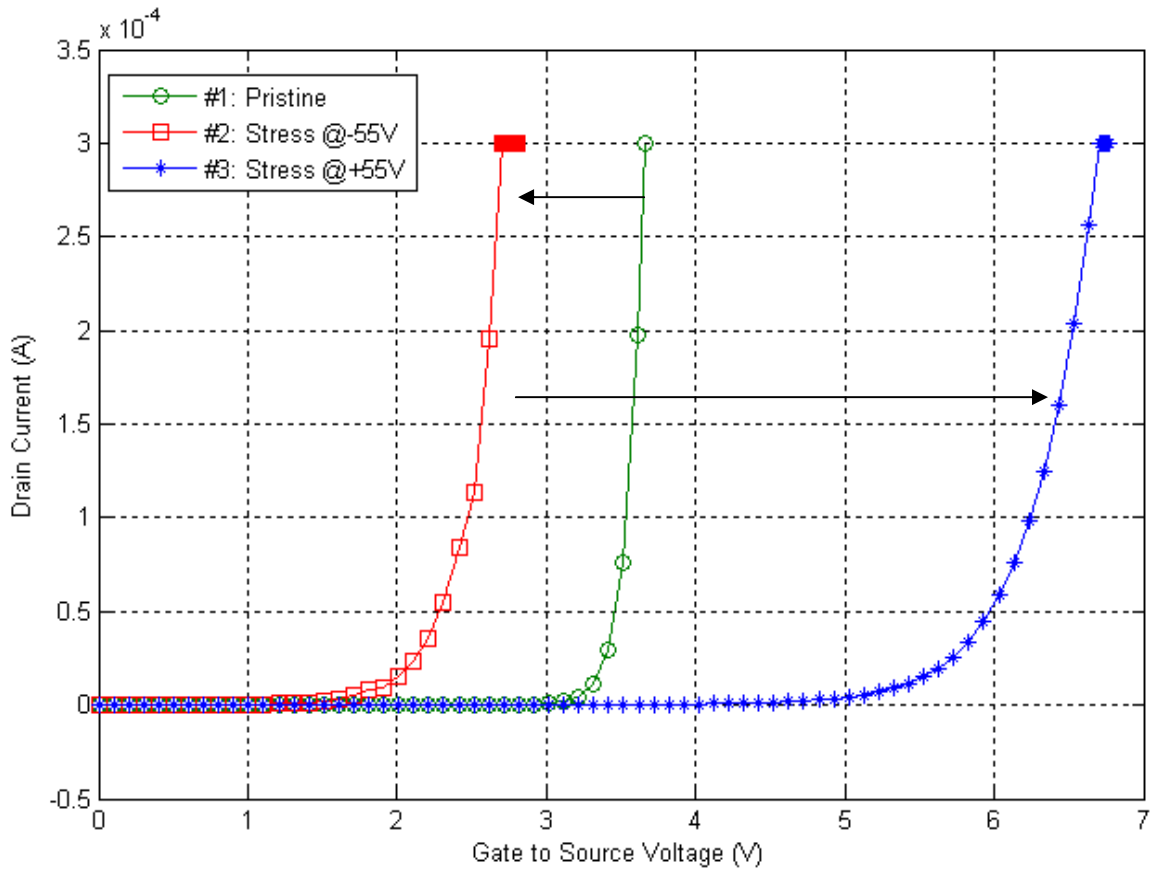
Figure 19—Movement of threshold in opposite direction under opposite polarity stress (S18). Positive Stress refers to the applied positive bias, and negative stress refers to the applied negative bias at the gate. Applying both kinds reduce the errors in concluding the reason for the degradation of the power MOSFET.

Positive stress refers to the applied positive bias, and negative stress refers to the applied

negative bias at the gate. Applying both kinds should help conclude the reason for the

degradation of the power MOSFET by the method of elimination.
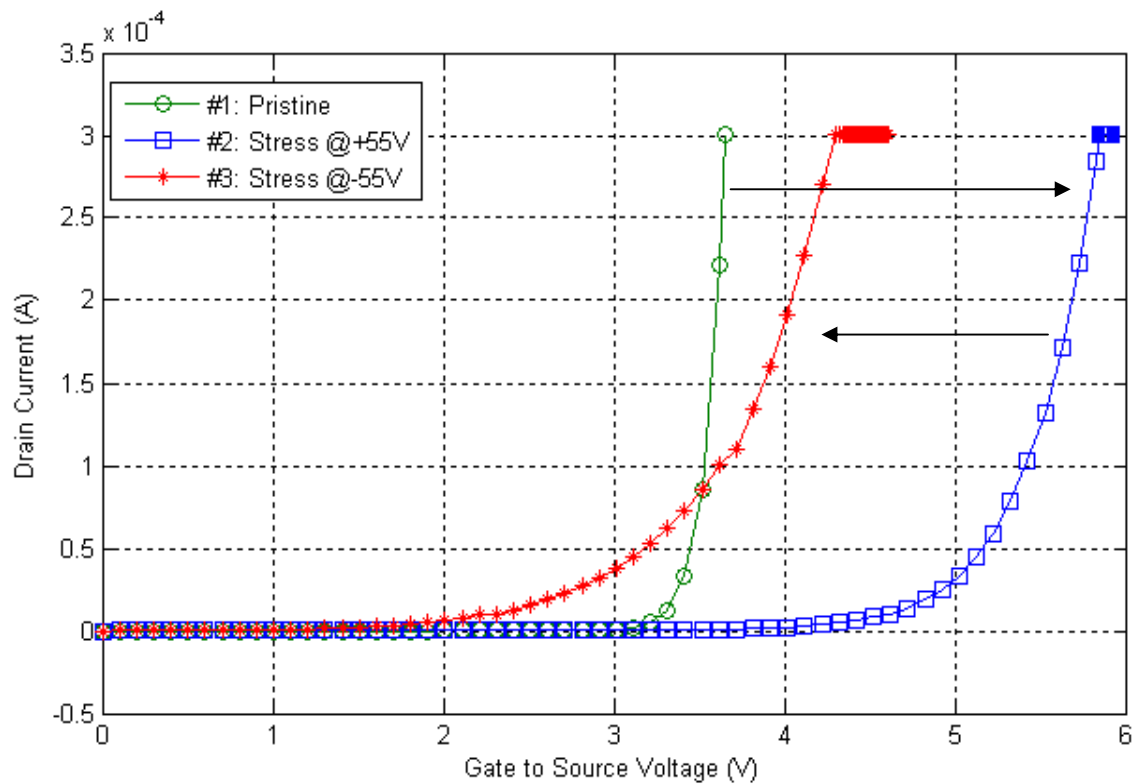
Figure 20—Changes in direction of threshold voltage with opposite polarity stress (S19). Positive Stress refers to the applied positive bias, and negative stress refers to the applied negative bias at the gate. Applying both kinds reduces the errors in concluding the reason for the degradation of the power MOSFET.

5.3.1 Significance of Switching Characteristics

Figure 21 shows reversal of a switching characteristic of "S4." The device went through

an electrical overstress of 60V and stopped switching completely at a point where it

appeared to be a failed device. However, after applying a negative stress at the gate, the

device nearly regained its pristine switching characteristics. The redistribution of the

implanted ions with the applied electric field helped reset the behavior [22]. Figure 21

also shows the reversal of the Miller Plateau close to its pristine characteristics. The

66

phenomenon of switching recovery was contributed by the reversal of the distribution of

mobile ions [23].
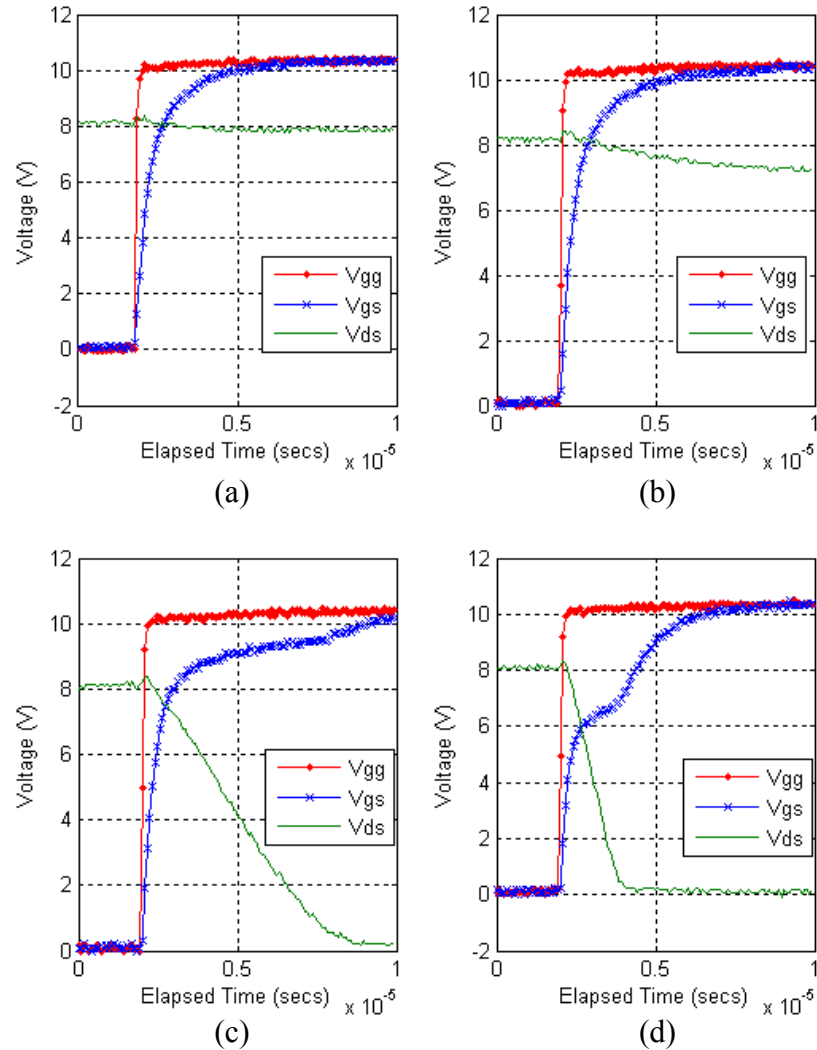
Figure 21—Reversal of switching characteristics in a "stopped switching" device suggests only the changes in parameter due to nonlinear distribution of the implanted ions and not a degradation. (a) Stops switching after 4 hours of stress at 60V; (b) Starts to return at -45V stress; (c) More significant return of drain-to-source voltage at -55V; (d) Complete reversal of switching at -53V.

5.3.2   The Early Turn-On at Negative Stress

Applying negative bias started driving the ions in the opposite direction. The negative

stress moved these negative ions away from the gate deep into the semiconductor region.

However, the negative ions or electrons closer to the surface were removed first. In

addition, the movement was not uniformly distributed [31]. Rather, the stresses smeared

them out in the opposite direction from the channel. The repetitive stresses, in addition to

the already non-distributed ions, created a band in the region, which in turn introduced

more intrinsic carriers in the channel. In the case of accumulation, many intrinsic carriers

or holes gather at the interface [16].
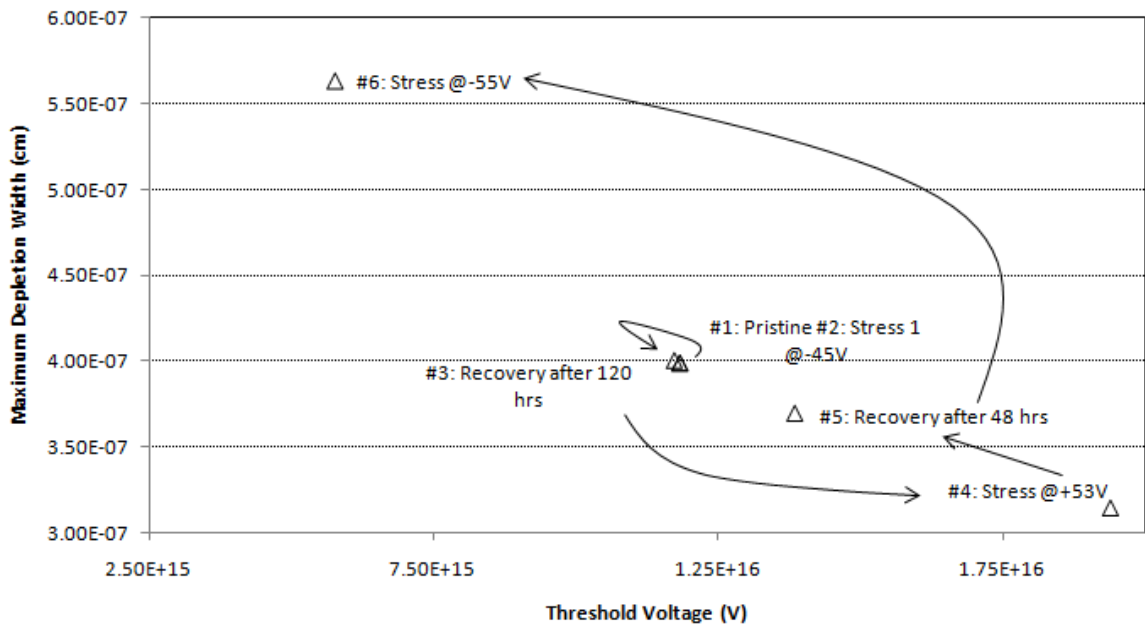
Figure 22—Variation in depletion width over different applied stresses (S17).

The excess number of intrinsic carriers initiated a lower threshold voltage (V_{TH}) in the channel. The early turn-on of the device under a negative bias was due to the lower threshold voltage [26]. Threshold voltage is a function of the electric field on the holes or ionized donors, and the electric field is the function of the depth of the channel [15].
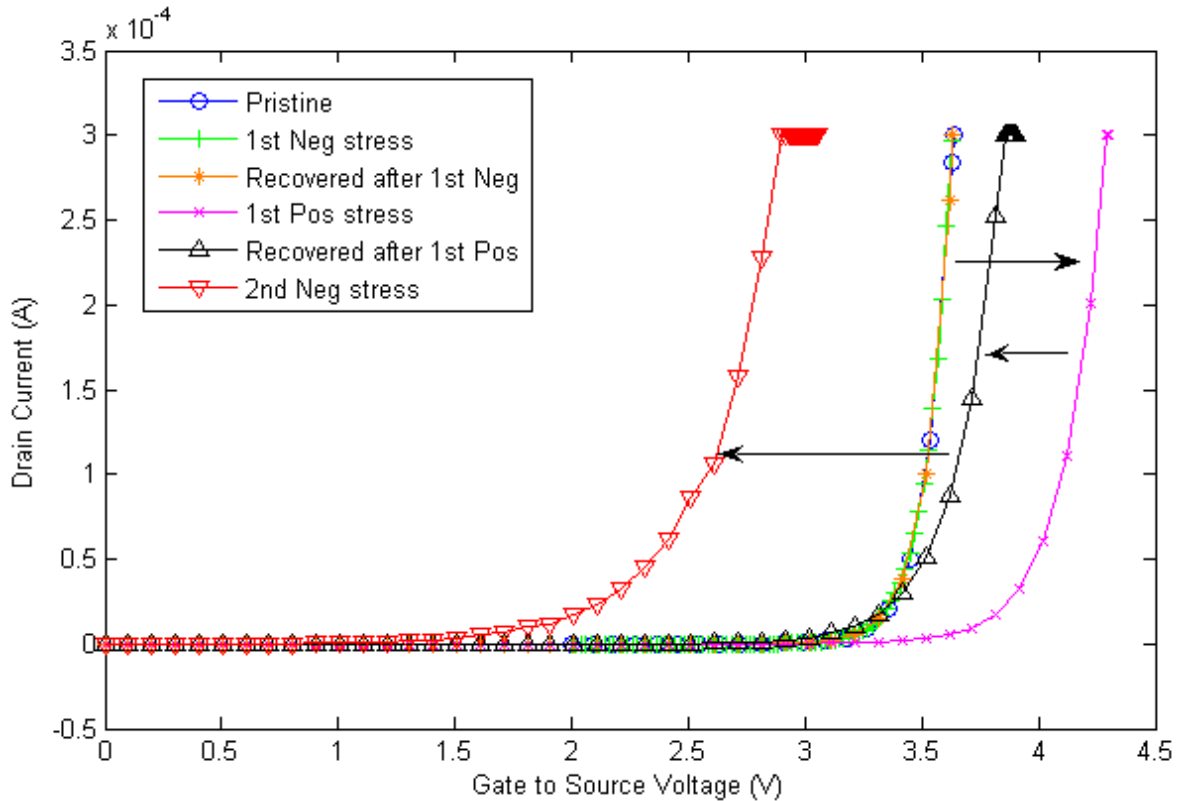
Figure 23—Different amount of bi-directional movement under different stresses with opposite polarity (S17).

Figure 23 demonstrates zero movement in the threshold shift at -45V. A significant shift toward right occurred after a +53V of applied stress. Again, a shift toward left occurred at -55V. After the first applied stress at +53V, the ΔV_{TH} (change in threshold voltage)

69

was 0.6741V, which appeared to be 18% deviation from the pristine condition. Recovery

through the diffusion occurred at ΔV_{TH} of 0.473V which was 11% from the previous

stage. After the application of -55V, a significant change of threshold voltage of 24%

occurred toward left from right. However, it appeared to shift in opposite direction with

an opposite polarity voltage. In Figure 24, it is discernible that the mobile ions or carriers

required adequate energy to move across the lattice and to affect the channel.

Figure 24—Changes of distribution of mobile ions over different threshold voltage (S17).

5.3.3   Differences in Work Function

The work function (ϕ_{ms}) might become negative due to the formation of a depletion region between an n$^+$-polysilicon gate electrode and a P-type base of the transistor. This might lead to the reduction of the threshold voltage when it was stressed under negative bias [26]. The number of acceptor ions was decreased in this region. The increase in acceptor ions from re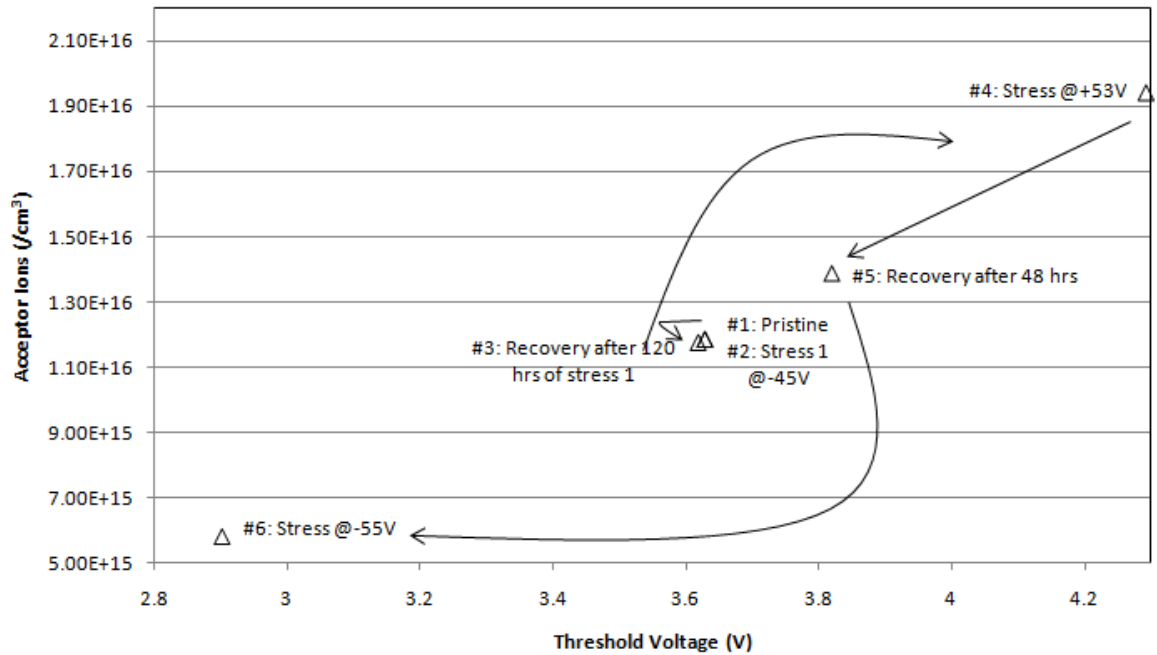gion #1/2/3 to region #4 (electrical overstress at 53V) was observable in Figure 24. The number of acceptor ions in recovery region #5 (after diffusion) was lower than the number in region #6 (electrical overstress at -55V), also observable in Figure 24.

5.3.4   Explanation of Threshold (V_{TH}) Shift

The original hypothesis of leading the power MOSFET to a degradation mechanism was not done by working under the influence of an accelerated stressing system but rather changing the functionality of the device with a threshold shift.

In some hypotheses, it was suggested that if the region had been completely depleted then it could not carry a large current [19]. Following is further analysis to come to the conclusion that it was a threshold shift by the ions and was not due to the trapped sodium charges.

5.4   Exclusion of Sodium Ions as a Root Cause

The trapped sodium fundamentally shifts the threshold voltage; it does not change the characteristics of the channel. However, in this experiment it was observed that the

71

negative stress modified the characteristics of the transfer curve abruptly [31]. The pristine curve was steeper than the stressed curve. The stressed curve followed an elongated path rather than a sharp pristine one under both kinds of stresses. The implanted ions proved to be the reason for the threshold shift associated with a voltage offset and a change in the shape of the transfer curve (see Figure 8).

Ion implantation is mostly used over diffusion for fabrication process to assure a sharp transfer curve [15]. Originally, the profile of the ion implantation provided a neat, sharp transfer curve. The mobile ions were disturbed but were not completely damaged through the stresses. The electrical stress might have modified the channel.

Sodium ions could change the work function but not the current carrying capability of the channel, while the "mobile implanted ions" could change the current carrying capability of the channel (see Figure 8 and Figure 9). The nonlinear redistribution of the ions inside the device was attributed to the different amount of threshold shift under positive and negative stresses as visible in Figure 19 and Figure 20.

In the experiment of applying a negative high stress at the gate, the sodium ions might move toward the gate and oxide interface and eventually might acquire sufficient energy to penetrate the oxide [32]. Damaging the oxide could damage the device as well. However, after removing the high negative stress, the device functioned properly, which excluded the role of sodium ions.

The study of the Na+ ions' concentration and transport mechanism in the oxide layer of a MOSFET through a triangular voltage sweep (TVS) asserted that the sodium ions were relatively stable with a negative bias and very unstable with a positive bias [25]. The observation in this experiment was not consistent with this theory.

Therefore, the sodium ion was not the reason for the changes in characteristics in the devices used in this experiment. The device was stressed with both a positive and a negative bias, and it functioned as a normal device.

The experiment based on the TVS method showed that the ionic transportation was observed at the lower temperature only with high ionic contamination [25]. The data was collected based on the 1990's technology of process and fabrication. The manufacturing has evolved into a more clean and automotive system, which has reduced the amount of contamination in current technology.

Previous studies showed that the early turn-on of the threshold voltage occurred because of sodium ions. At the beginning of the device operation, few positive ions close to the polysilicon gate did not affect the channel much. With cumulative stress, the drift sodium ions in the Silicon-SiO_2 interface attracted more of electrons in the channel. As a result, the transistor turned on prematurely [21].

However, such unpredictable threshold shift was not seen in this experiment as reflected in Figure 8 and Figure 23, from which it can be stated that the device changed the

73

characteristics under the influence of the sodium ions. Rather, the shift became larger

and larger with the applied electrical overstress. This excluded the role of sodium ions as

a root cause for the changes in characteristics.

5.5   Active Role of Mobile Ions

Apparently, the "mobile implanted ions" caused the modification in characteristics. The

emphasis on the channel-induced mobile ions was higher as they stopped at the SiO_2

because they only moved inside the pure silicon lattice; they did not move through the

glass. The different width in the depletion layer under opposite polarity stress with

different magnitude exhibited changes in the distribution of mobile ions at various
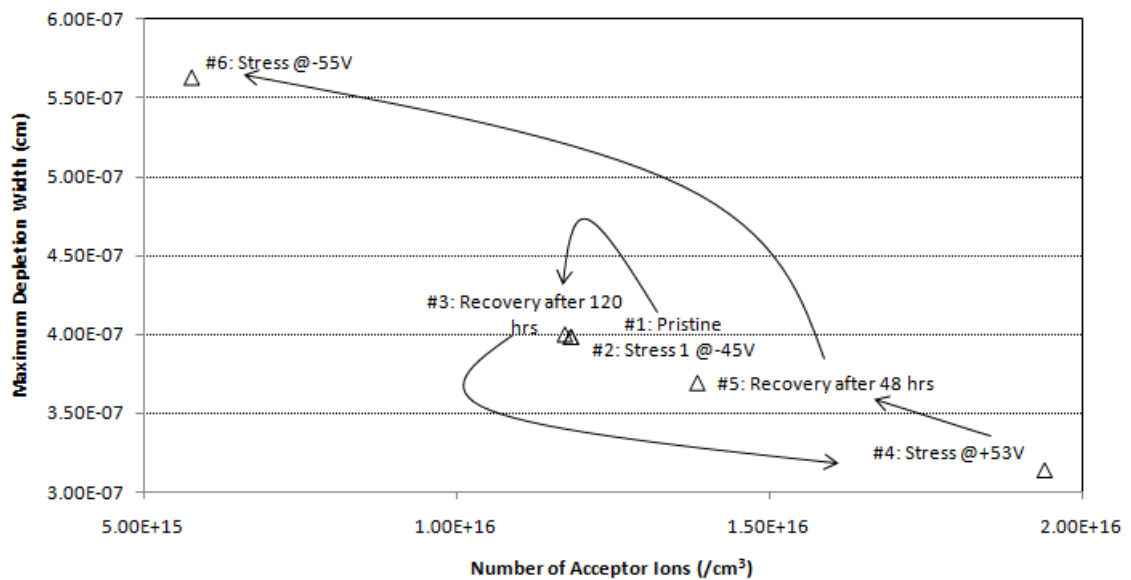
threshold voltages as in Figure 24.

Figure 25—Maximum depletion widths with varying mobile acceptor ions (S17).

Practically, the difference between the movement of trap sodium charges and mobile ions depends on the required strength of the field. Sodium moves at low voltages so easily that even at room temperature under 10 to 20 V, it changes the logic level of the transistor.

If Na+ was the root cause, it would continue to move with the repetitive stressing towards the gate eventually moving into the SiO_2. Reaching at this point would not allow the transistor to turn on or off ultimately. The Na+ ions would have enough energy to reach SiO_2 at this point after reaching the gate with sufficient energy as it has a dominating effect near the gate.

No such deviation in the properties of the power MOSFET was observed under 10 to 20V. To observe any change in the properties of the device under test, the accelerated stress test had to go beyond 53V. Thus, the active role of channel-induced mobile ions was evident.

5.6   Observation after Applied Negative and Positive Stress

Under the negative stress by shifting the threshold voltage lower and lower from the pristine device condition, the device could turn into an intrinsic device [16]. Stress modified the device in a non-destructive way. The negative stress helped recover the threshold voltage but was unable to maintain the same profile for the distribution of the dopants. The applied negative stress at the gate after the application of a positive stress

shortened the previously elongated Miller plateau, attributed by the decreased space charge width.

To prove the hypothesis and to find root cause to any modification in device characteristics, the device was stressed under equal and different amounts of opposite polarity electrical stresses. To eliminate sodium ions from the root cause and to emphasize on the dopants or implanted ions, observing the movement of the transfer curve in both directions was considered a fundamental approach. The curve showed different amount of movements with an equal but opposite amount of stress. The nonlinearity of diffusion over time arose from the nonlinear density across the device [26]. The visible change in slope as seen in Figure 9 was caused by a different gradient of distribution of the channel. The amount of movement across the positive and the negative stress occurred because of the gradient movement across the space, not because of the polarity of the stress. The reason behind the phenomenon was that the transfer curve started at a differently distributed concentration. Due to the mutual repulsive force, the impurity ions diffused out over time. Moreover, it recovered over time even with a non-uniform gradient as illustrated in Figure 22, which in turn appeared as a transfer curve of different shapes [15].

76

6.   Sentaurus Simulation of the Device

The device was parameterized and simulated using Sentaurus TCAD tools, and its I-V
characteristics were observed. The Spice datasheet from the manufacturer provides
information on the channel length and the channel width [33]. The thickness of the oxide
was calculated and verified from the other sources [19]. The doping concentration used
in the simulation was calculated using a mathematical interpolation method.

6.1   Doping Profile

The power MOSFET is an $N^+PN^-N^+$ device. The negative sign in the simulation stands
for the acceptor ions. The green area depicts the N- drift region (see Figure 26). The
calculated value of the doping concentration matched well with that of the other doping
profiles of the cell of the HEXFET. It is visible in the P-type base region.
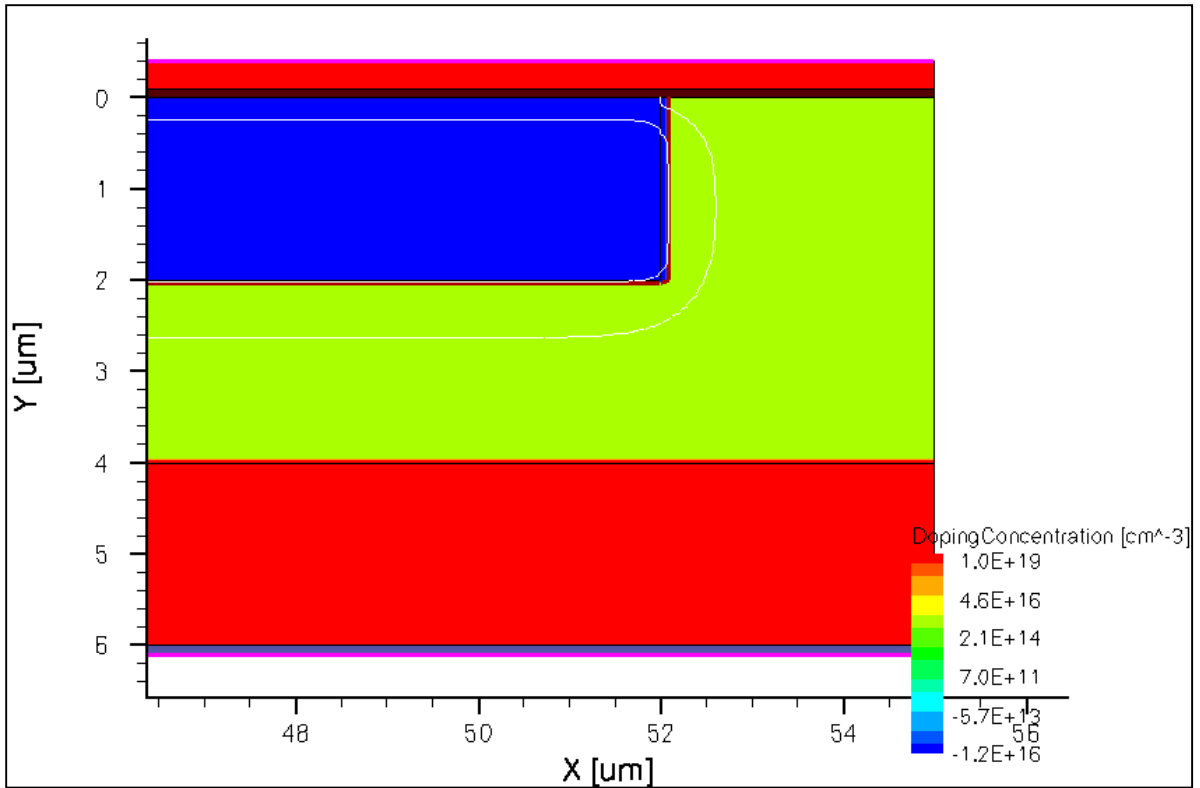
Figure 26—Doping concentration with the current findings.

6.2   Space Charge Distributions

The density of the space charge distributions was the highest in the JFET region [7]. The

density of the space charge increased with the mobile acceptor ions. The mobility of

holes is approximately one-third of the mobility of electrons [16]. Therefore, the

mobility of holes affected the nonlinearity at the applied stress more than that of the

electrons. The yellow and brown colors show the depletion region for the body diode

region with a P-type base and an N- drift region (see Figure 27).
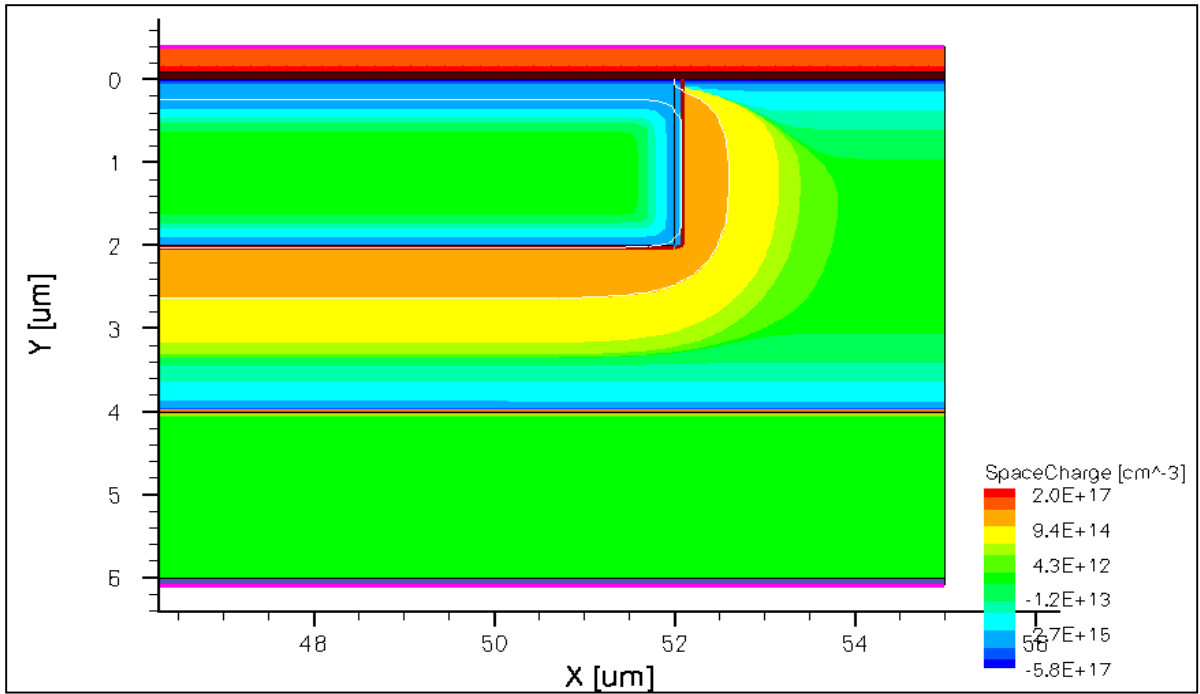
Figure 27—Space charge distribution based on the doping concentration from this research.

6.3 Mobility of Electrons

The N^+ zone exhibited less mobility because of high doping profile [6]. The N^- drift zone

showed the highest mobility zone. The channel was formed in the P-type base. The

current passed straight from drain to source and shifted towards the channel

perpendicular to the JFET region.
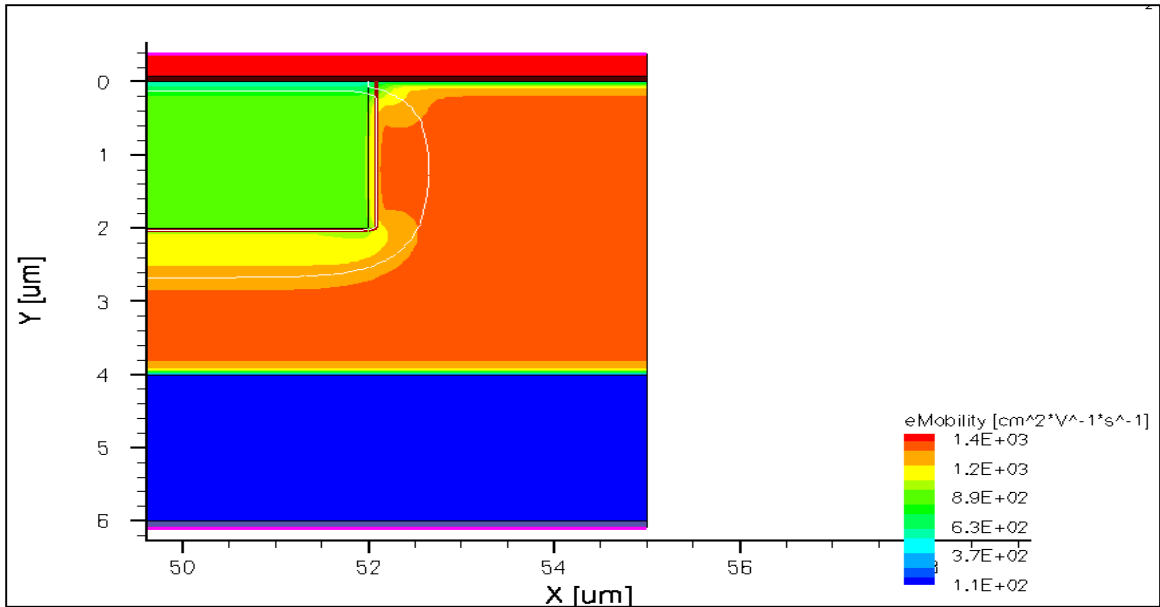
Figure 28—Electron mobility distribution in a power MOSFET cell.

6.4 Transfer Curve of the HEXFET

The maximum drain current the device under test (DUT) was capable of tolerating was

approximately 9A. The graph (Figure 29) was simulated for a channel length of 50 μm,

half of the original cell [33]. The characteristics remained the same as observed in the

experiment for the pristine device once current values were doubled. The result matched

the calculated doping profile for the device. For a HEXFET, hundreds or thousands of

individual cells are usually connected in parallel to reduce the "specific on-resistance"

and increase the amount of current it can drive.

Figure 29—Drain current over gate voltage based on "Sentaurus" simulation.

7.   Summary

7.1   Results

The AIEO or the isothermal instability in threshold voltage and switching characteristics of an n-channel power MOSFET showed a nonlinear distribution of channel-induced acceptor ions at positive and negative electrical overstresses [26].

To analyze the isothermal instability under the positive electrical stress, it is important to analyze the "successive-threshold-shift" from the pristine condition, the discrepancies in the changes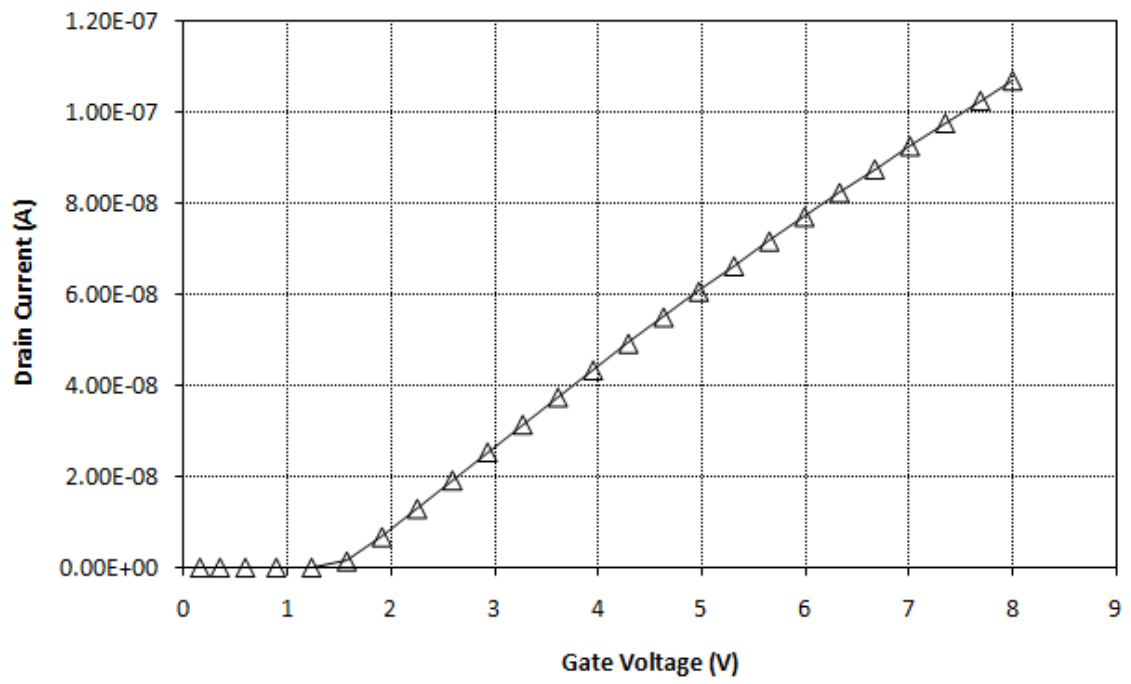 in threshold voltage shift, the saturation of the threshold voltage shift after few stressing cycles, the elongation of the Miller Plateau, and the switch-on characteristics.

The value of the threshold voltage (V_{TH}) increased faster at the beginning of applied stress than in later stress cycles. This change during a positive stress was attributed to the increase in the number of channel-induced acceptor ions. Moreover, the increases in the negative interface state charges caused an increase in the density of these ions [26].

At the beginning of a stress cycle, the semiconductor lattice is evenly distributed [15]. After the first few positive stresses, the negative mobile ions or the carriers moved toward the surface of the interface faster and altered the original distribution of the pristine condition. The high voltage at the gate provided a large enough potential for the electrons to cross the depletion layer and to create an inverted channel. The mobility of

electrons is three times greater than the mobility of holes [16]. Once the device was stressed with a few cycles, the gradient of the threshold shift became the function of the distance from the polysilicon gate. The electric potential energy dropped with the increase in the depth of the semiconductor [15]. Therefore, after a few cycles of stress, less movement between the mobile ions and electrons inside the channel was observed, which created congestion in the transfer curve.

Figure 7 of the "positive electrical isothermal stress" over cumulative stressing time depicted a change in the transfer curve. The pristine curve was sharp and steeper at the beginning. The slowness or flatness in the stressed curves suggested a modification in the characteristics of the power MOSFET.

The illustrations of the flat band voltage showed no change in the work function difference between the polysilicon gate and the semiconductor. Any changes in the flat band might suggest the sodium or mobile impurity ion as a candidate for the root cause to the threshold shift [26]. In addition to the unchanged flat band potential, the threshold shift contributed to the density distribution of the channel-induced acceptor ions.

Progression of the gate-to-drain-silicon capacitance (C_{gdsi}) depicted that the stress had changed the shape of the channel of the VDMOSFET over time. The ions were transported to the side of the channel up to the depletion region, which changed the shape of the channel. With the increase in threshold voltage, the gate-to-source capacitance decreased over the accumulated stress time. On the contrary, right beneath the oxide, the

83

gate-to-drain capacitance increased with the threshold voltage. The ions were driven out of the channel as the stress increased, which modified the effective channel thickness more, and as a result, caused a drop in the capacitance. The expansion of the Miller Plateau continued up to the point when the device stopped switching. The total charge increased over time across the depletion layer between gate and drain [29]. Additionally, the simulation from the "Sentaurus" TCAD tool correlated with the gradient of space charge distribution in the JFET region.

The threshold shift in the opposite direction was observed during negative stress. Moreover, complete recovery of switching was observed after applying multiple negative stress. The early turn on of the device under the application of a negative bias exhibited the behavior of an intrinsic device [16]. The followed path of a threshold shift in both directions emphasized the changes in mobile ion acceptors and the density of the interface of these ions [26]. In addition, the difference in current-carrying capability at the beginning of and during the stress advocated for mobile acceptor ions as a root cause of the characteristics modification of the device.

While the operating condition was not permanently altered, there was no indication of failure, which concluded that the device did not degrade under the AIEO, but instead, only changed its characteristics.

Table 5—Comparison of parameters between pristine and stressed device

	Pristine	Stressed (see NOTE 1)	Δ (Change)	%Change
V_{TH}	3.6V	9.79V	6.19V	+172%
Slope of transfer curve	0.69	0.16	0.53	-77%
V_{GP}	5.92V	7.52V	1.60V	+27%
Miller plateau width	0.8 μsec	5 μsec	4.2 μsec	+525%
Switching time	0.6 μsec	∞	∞	$+\infty$
C_{gMill}	1.43 nF	1.04 nF	0.39 nF	-28%
C_{ds}	1.25 nF	0.95 nF	0.3 nF	-24%
C_{gs}	1.32 nF	0.75 nF	0.57 nF	-43%
NOTE 1—Point of maximum deviation is listed here.				
NOTE 2—Switching time infinity means that no switching is happening.				

7.2   Future Works

As a future work, building a diffusion model based on the distribution of ions for the

isothermal electrical overstress at both positive and negative bias will solve many

questions. Calculation for the turn-on and the turn-off time will also provide more

insights to the switching characteristics of the power MOSFETs.

The devices could be stressed for an extended period and swept over applied voltage,

which is expected to result in some degradation. Other semiconductor devices in the

market can also be used for repeating the same experiment. Stresses other than electrical

can also be applied to monitor impacts. A simulation tool could help identify optimal

material properties that lead to stability and speed.

7.3   Conclusion

Threshold shifts of 22 devices were studied. The accelerated isothermal electrical

overstress (AIEO) applied at the gate of the power MOSFET demonstrated modification

of the characteristics, rather than degradation. After the application of a high negative

bias, the switching performance reverted to a pristine condition, which indicated no

degradation in the device. The values of the capacitances C_{iss}, C_{oss}, and C_{rss} were

calculated as 14.75nF, 12.25nF, and 11nF, respectively. The increase and decrease in

threshold voltage at positive and negative applied voltages were not symmetrical with

respect to pristine behavior. In addition, changes in threshold voltage did not have a

linear correlation with applied voltage. The asymmetric changes in the threshold shift

arose from the nonlinear distribution of the carriers. The dominance of channel-induced mobile ions or acceptors was the reason behind the threshold shift. The result showed a threshold shift of up to 172%. The slope of a sharp pristine transfer curve was 0.69 at the beginning and modified to 0.16 as measured at the point of acceleration. The repetitive stress made the slope 77% flatter. The width of the Miller Plateau changed to 525% of pristine size after a 30-hour stress with 53V at the gate. The charge between gate and drain significantly widened the Miller Plateau.

A pristine device stopped switching after only 4 hours of stress at +60V. However, a consecutive gradual increase of a negative stress helped the characteristics return to normal. This behavior proved mobile acceptor ions as the root cause for the modification of the characteristics. Moreover, a zero movement of the transfer curve before a stress of 45V of both polarities, reversal of switching phenomenon, and evidence of no oxide damage excluded alkali metal ions (sodium ion) as a candidate for the root cause. With the combination of results from this research and previous studies on effects of sodium ions and channel-induced acceptor ions, it was evident that the changes in characteristics occur under the influence of channel-induced acceptor ions. Finally, it is concluded based on the results for the parameters under accelerated isothermal electrical overstress (AIEO) that no degradation occurred.

Appendix A: Worksheets

Table A.1—Data collection worksheet for experiment

Stress Duration (mins)	Gate Voltage (V)	Drain Voltage (V)	Drain Current (A)	Power (W)	T_{case} (^{o}C)	T_{cold} (^{o}C)	T_{hot} (^{o}C)	$T_{package}$ (^{o}C)
62**	53	2.23	8.45	18.74	49.18	25.04	28.96	56.2
-	-	-	-	-	-	-	-	-

NOTE 1—Similar worksheets have been used for each of devices and only a single one has been provided here for illustration purposes.

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