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CHEMICAL VAPOR DEPOSITION OF POLYCRYSTALLINE SILICON IN A RAPID THERMAL PROCESSOR

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Master of Science

By
Jimmy C. Liao
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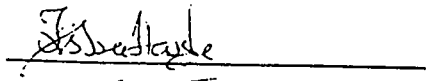

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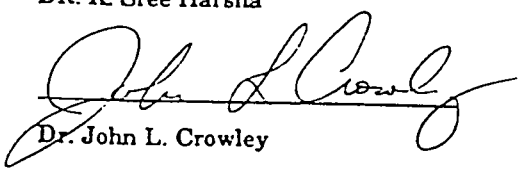

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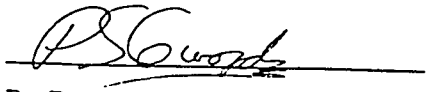

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ABSTRACT

CHEMICAL VAPOR DEPOSITION OF
POLYCRYSTALLINE SILICON IN A RAPID THERMAL PROCESSOR

by Jimmy C. Liao
Dr. K. Sree Harsha, advisor

A rapid thermal processor, which heats silicon wafers with high intensity light, was used to chemically deposit silicon from silane gas. The process was characterized.

The properties of this thin film were investigated. The kinetics of the deposition was determined from a matrix of time, temperature, and silane partial pressure. The amorphous to polycrystalline transition temperature of the deposition process was determined. Film surface roughness and crystallographic texture were also measured.

The optical absorption of the film and its response to the light radiation was measured and modeled as a function of film growth.

Electronic capacitors were made by growing a thermal oxide in the rapid thermal processor, then depositing the silicon electrode in-situ, or in the same chamber. The advantages of in-situ processing were demonstrated to be higher yield and reliability of these devices, due to the carefully controlled environment which did not expose the oxide to air.

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Chapter 1
INTRODUCTION

Polycrystalline silicon (polysilicon, or poly) is a material which is widely used in the fabrication of integrated circuits (ICs) because it is compatible with single-crystal silicon, can possess a wide range of resistivities depending on its dopant concentration [1], and can also be used to form dielectrics [2]. In ICs, it has uses as a MOS gate, resistor, metal contact, and insulation for electrical isolation [3]. Diagrams of some devices are illustrated in figure 1. For IC fabrication, it is typically deposited as a thin film using a technique known as chemical vapor deposition performed in a furnace [4-6].

In an isothermal furnace, a silicon-containing gas, usually diluted with an inert carrier gas, is flowed over a wafer. The gas decomposes into atomic silicon on the wafer. This is typically done under vacuum (< 5 torr) at a temperature range of 500°C - 700°C using silane (SiH_4) or dichlorosilane ($SiCl_2H_2$) [7]. Because vacuum is used in the furnace, the process just described is referred to as low pressure chemical vapor deposition (LPCVD). In this process, the furnace temperature is first allowed to stabilize in an inert ambient. Then, when the desired temperature is reached, the reactive gas mixture is flowed from one end of the reactor and exhausted at the opposite end. Deposition of poly occurs on all surfaces within the reactor, including the furnace walls and the wafer holder. Periodic maintenance of the reactor is required to prevent a

build-up of film on the furnace. There is also a problem with the generation of particulates from homogeneous nucleation reactions within the reactor. The deposition reaction is terminated by cutting off the gas supply and replacing it with an inert gas. Then, the furnace is cooled and the wafers are unloaded.

In this work, poly is deposited from silane under vacuum using a rapid thermal processor to heat the wafer, rather than a resistance-heated furnace. An RTP system uses a lamp to heat the wafer by optical and UV absorption [8], so that the temperature of the wafer varies with the intensity of the lamp light. The direct absorption of light allows rapid temperature changes in the wafer. This can be done in a water-cooled steel, or quartz chamber, where the light is selectively absorbed by only the wafer. Since CVD is a thermally activated process, the deposition occurs only on the wafer, and not on the chamber walls.

With the ability to change temperatures quickly, RTP has many advantages over furnace heating. Drastically reduced transient times (time required to reach temperature) allow ultra thin films (< 100 Å) to be formed. Since CVD is thermally activated, the reaction can be terminated about as quickly as turning off the lamp, rather than waiting for the slow depletion of silane. The reduced thermal exposure also minimizes diffusion between thin film layers, which is time-dependent. The ability to change temperatures rapidly also allows several processes to be carried out sequentially. For example, silicon can be deposited at a low temperature (600°C) and subsequently annealed at a high temperature

(1000°C). This deposition method has been used to control the grain size of the material [9].

By combining RTP with a small chamber volume and a vacuum pump, a wide range of temperatures, ambients, and pressures can be set and quickly changed. As a result, several different processes can be combined in the same chamber (in-situ processing). One application of in-situ processing is the formation of capacitors using rapid thermal oxidation (RTO) of exposed silicon in an oxygen ambient followed by a deposition of polysilicon for the electrode [10]. Typically, this is done in two different machines with a wafer transport step performed by a human operator. By combining the process in-situ, the wafer will be free of airborne particulates and contaminates which could adversely affect device performance if found in the oxide-poly interface. The deposited silicon electrode can either be the full thickness required for the poly step, or merely a thin poly cap to protect the oxide film while it is being transported into a conventional LPCVD furnace. For conventional device geometries which typically require 0.4 - 1.0 μm polysilicon, the latter might be a better approach, since RTP processes are designed for short process times and hence, thinner films. Also, the film thickness uniformity and doping capabilities are well established in a furnace [6].

The first part of this work involves an analysis of the polysilicon deposition process in an RTP environment and a study of the resultant film properties. The deposition is performed at a matrix of time and temperature and two partial pressures of silane in order to determine the

dependence of these variables on growth rate and morphology.

Since RTP is an optical process, the second part of this work will focus on absorption studies. The absorption of the film at various thicknesses is important for both the heating of the wafer and the measurement of temperature during the process, which depends on the emissivity of the wafer. The more energy that is absorbed rather than reflected, the higher the wafer temperature (which in turn affects the deposition rate, as well as the morphology of the film). Thus, the focus of the investigation will be on relating the wafer temperature with the lamp power absorption and resultant film thickness.

Lastly, electronic devices are fabricated to evaluate the advantages of using the new poly material, as well as the advantages of in-situ processing. Two studies of RTO capacitors with polysilicon electrodes are performed using capacitance-voltage (C-V) techniques [11]. In the first study, the in-situ RTCVD capping poly layer is compared to an LPCVD layer of polysilicon. The purpose is to compare the new process with an established one. In the second study, the affect of in-situ vs ex-situ processing was compared directly using RTCVD polysilicon entirely. The purpose was to determine the merits of in-situ processing.

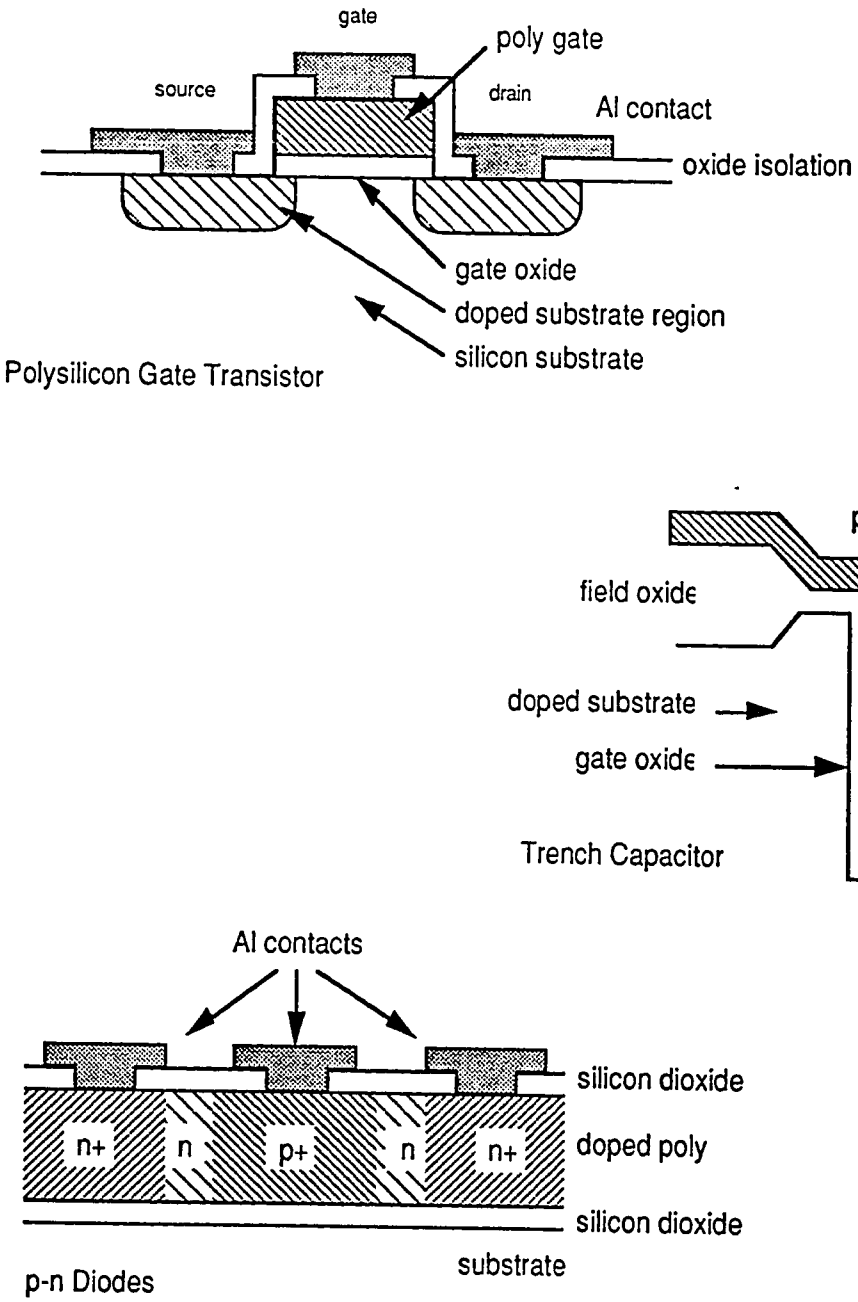


Figure 1 Examples of some applications for polycrystalline silicon.

Chapter 2
EXPERIMENTAL

The rapid thermal processor used in the experiments was a commercially available Peak Systems Inc. ALP 6000 which was modified for vacuum processing by attaching a gate valve and 40 cfm mechanical pump to the exhaust manifold, and adding a silane gas manifold consisting of silane and and inert gas line. The configuration of the RTP chamber is shown in figure 2. The rectangular chamber is water-cooled, polished stainless steel with a volume of approximately 0.7 liters. The wafer is centered in the chamber, thermally isolated by resting on three quartz pins. Gases enter the chamber from the top four corners, and exhaust to a mechanical pump from the corner side walls. The ceiling of the chamber is a half inch thick quartz window, which is transparent to the lamp radiation. The reflector assembly rests on top of the window and is focused on the wafer plane. It is contoured with precision optical design to deliver a distribution of lamp radiation which provides uniform heating throughout the wafer. A 35 KW long arc discharge lamp is mounted in the reflector, surrounded by a quartz water jacket.

The spectral output of the lamp (SP35X) ranges from approximately 0.2 to 1.6 μm. This is shown in figure 3. It is compared to the output of a common tungsten halogen lamp, which also gives off high intensities of infrared (IR) as well as visible light. The SP35X lamp, on the other hand, is a xenon arc discharge lamp which cuts off abruptly in the near IR. These

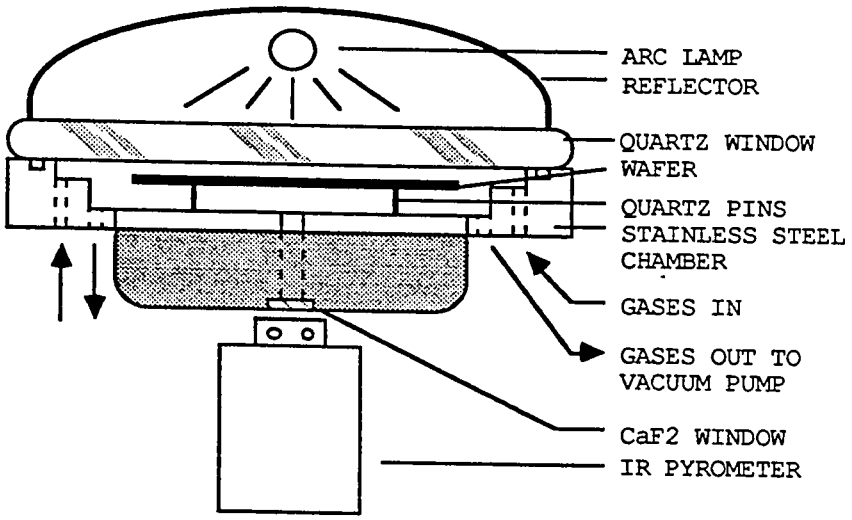


Figure 2 Cross sectional diagram of the RTP chamber, looking along the length of the long arc discharge lamp.

outputs are plotted as relative intensity on the right ordinate axis. On the left ordinate axis, plotted on the same coordinate, is the relative absorption of silicon. At short wavelengths, below 1.2 μm, the mode of absorption is direct excitation of silicon electrons. This absorption has a sharp edge, above which absorption is carried out by free carriers. Direct band to band

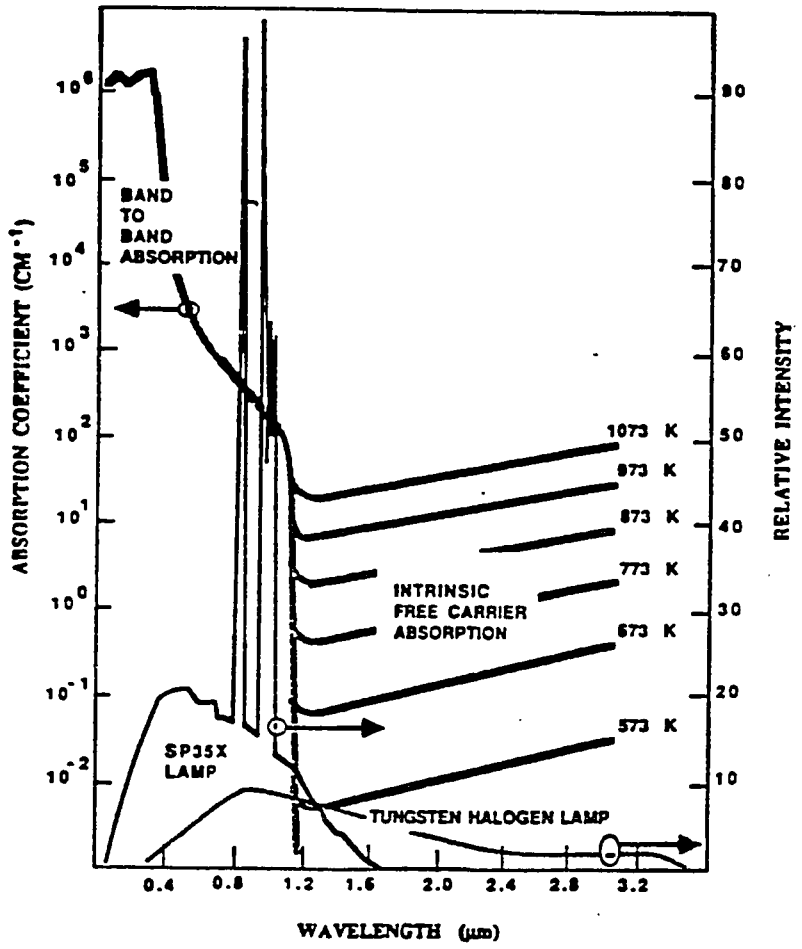


Figure 3 Spectral output of the SP35X xenon arc lamp compared to tungsten halogen lamps, plotted as relative intensity vs wavelength. Superimposed on the ordinate axis is the absorptivity of silicon at various wavelengths. An absorption edge occurs around 1.2 μm, above which only free carriers are absorbed.

absorption is preferable to free-carrier absorption because the heating efficiency is not dependent on the dopant concentration in the material or on the temperature of the wafer, making for a more repeatable process. Therefore, the output of the arc lamp is more specifically tuned for silicon heating than the tungsten halogen filament lamp.

Centered on the floor of the chamber (refer to figure 2) is a quarter inch aperture, sealed with a thin calcium fluoride (CaF_2) window, which is transparent to infrared absorption. The temperature of the wafer is measured and monitored by an IR pyrometer mounted below. Emitted radiation from the hot wafer is collected by an indium-arsenide photodetector in the pyrometer, which drives the lamp current in a closed loop PID control until the desired temperature is reached. The detection band of the InAs detector is 2.5-3.5 μm, which is completely out of the range of the lamp's spectral output, so that the temperature of the wafer can be measured without radiative interference from the lamp. The sampling rate for the control loop is 10 milliseconds. The temperature setpoint is programmed in the software and temperature ramps can also be controlled to 1 °C/sec. A central computer stores and executes process recipes which integrate temperature and inert gas flow. The vacuum gate valve and the silane gas manifold are manually controlled.

When the pyrometer is used to feed back to a controller, it is known as "closed-loop control." An alternate mode of processing in "open-loop control." In this mode, a fixed lamp power is set, regardless of the wafer temperature, for a set period of time. The pyrometer in this case can be

used as a passive IR monitor.

The substrates used were p-type boron-doped (100)-oriented silicon wafers. The diameter of the wafers was 100 mm. The resistivities of the starting silicon was greater than 10 Ω-cm.

2.1 Kinetic and Material Analysis (Experiment 1)

Before polysilicon deposition, 100 nm thermally grown oxide was formed on the wafers in a separate tube furnace to allow for easier thickness measurement of the subsequent polysilicon film using a UV-visible spectrophotometer (200-800 nm) [12], as well as to prevent epitaxial realignment of silicon at higher temperatures [13].

For a study of deposition kinetics, silane was mixed with argon at volume ratios of approximately 1:20 and 1:3 at a pressure of 2.0 torr. (This translates to an approximate partial pressure of 0.1 torr and 0.5 torr of silane, respectively). Depositions were carried out at temperatures from 600 to 1100°C and deposition times of 10 to 300 seconds. The matrix variables are given in Table 1. One wafer was processed per condition. A diagram of the typical process recipe is shown in figure 4, which depicts temperature, relative pressure, and gas status as a function of time. In the gas diagram, a lightly shaded bar indicates a much lower flow than a darkly shaded bar. The recipe begins with a pump down to a base pressure of 10 millitorr, then a purge with argon gas in order to eliminate oxygen

Table 1

EXPERIMENTAL MATRIX

Temperature, °C	time, seconds	SiH_4 partial pressure, torr	
600	300	0.1	
650	120	0.1	
650	300	0.1	
700	120	0.1	
700	300	0.1	
800	60	0.1	
800	120	0.1	
800	300	0.1	
900	30	0.1	
900	60	0.1	
900	120	0.1	
1000	10	0.1	
1000	30	0.1	
1000	60	0.1	
1000	120	0.1	
600	120	0.5	
600	300	0.5	*
650	120	0.5	
650	300	0.5	*
700	60	0.5	
700	120	0.5	
700	300	0.5	*
800	60	0.5	
800	120	0.5	
800	300	0.5	*
900	10	0.5	
900	30	0.5	
900	60	0.5	
900	120	0.5	
1000	10	0.5	
1000	30	0.5	
1000	60	0.5	
1100	10	0.5	*

* Samples submitted for X-ray analysis

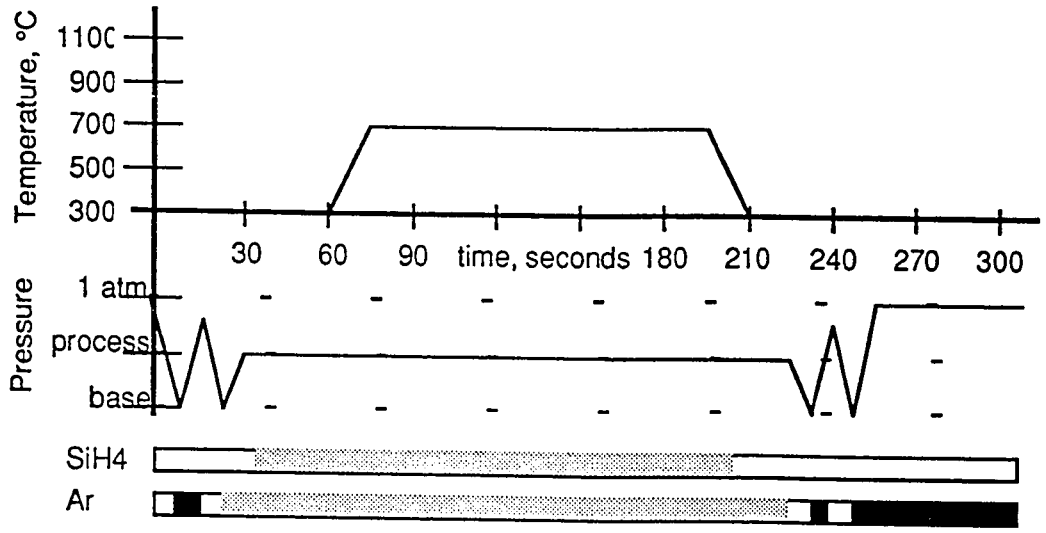


Figure 4 Graphical presentation of a typical process recipe for the deposition experiments of experiment 1.

from the chamber. Oxygen would readily combust with the silane causing a highly dangerous situation. After the purge, the set process pressure of 2 torr was established with the required ratio of silane to argon. After gas stabilization, the lamp was ignited and ramped in closed loop until the temperature was reached. Typical ramp rates were 75 °C/sec. After holding at the desired temperature for the desired time, the lamp was idled and turned off, allowing the wafer to radiatively cool. The deposition gas was then turned off, and the chamber was flushed with inert gas before being opened to the atmosphere for wafer handling.

After deposition, the thicknesses of the grown polysilicon films were measured with a spectrophotometer. Five measurements were taken for each wafer at different sites across the wafer, then averaged. However, if the film thickness uniformity was poor in a certain location on a wafer (as evidenced by a color difference of more than one interference order), then that area was avoided during measurement. The deposition rate was calculated by dividing the mean polysilicon film thickness with the deposition time.

In addition to film thickness, the spectrophotometer was also used to measure the reflectivity of the surface [14]. In this set-up, a deuterium lamp source was passed through a chopper which contained a cut-out section on one half and a silicon reference on the other. The light which passed through the chopper wheel was reflected off the surface of the polysilicon sample. Both signals were sent to a detector to determine the difference in signals. There was found to be a linear correlation between this difference and the root-mean-square surface roughness, which is characteristic of the grain size of the polycrystalline silicon. The reflectance was measured at two wavelengths; 200 and 321 nm (extracted from a spectrum of data, from 200 to 800 nm). The surface roughness parameter, (h) was evaluated using the equation [15]

$$h = C \lambda (\Delta A)^{0.5}$$

where $C = 0.099$ is a geometrical factor

λ is the wavelength

$$\Delta A = -2 \log_{10} (R / R_{Si})$$

R is the reflectance of the sample

R_{Si} is the reflectance of single-crystal silicon.

Since single-crystal silicon has characteristic absorption peaks at 280 and 370 nm [16], some information about the crystallinity of the deposited poly can also be determined by the spectrophotometer. In the reflectance mode described above, the difference of the two signals would mask the peaks at 280 and 370 nm if the sample were crystalline, and the peaks would show up if the sample were amorphous.

Samples deposited at different temperatures were analyzed with X-ray diffraction, using a GE XRD-700 X-ray diffractometer. These samples are highlighted in Table 1 with an asterisk. The radiation source was a copper $K\alpha$ tube operated at 35 KV. This analysis was used to determine the amorphous-polycrystalline transition temperature range, as well as the dominant crystal texture of the grains.

2.2 Optical Absorption Analysis (Experiment 2)

In this experiment, the absorption of the substrate (and therefore, the temperature of the wafer) of the RTP lamp was studied verses the film thickness of polysilicon. Since the deposition of the thin film changes the reflectivity of the surface, it is logical to assume that the emissivity of the

wafer will also change, thus varying the signal of IR sent to the optical pyrometer. To eliminate this source of variance, an independent temperature measurement is needed. A sample wafer with 100 nm thermal oxide (same type used in experiment 1) was instrumented with a C-type thermocouple (the junction is composed of W-5% Re on one side, and W-26% Re on the other). This was done by using an electron beam to fuse the wire into a pool of locally melted silicon, so that the TC junction is within the bulk of the wafer. The wire was then insulated with alumina tubing and fed out of the chamber through a vacuum feedthrough to a digital thermometer. The thermometer amplifies the TC bias which is then wired to a chart recorder to plot TC temperature vs time. In this arrangement, the temperature of the bulk silicon can be accurately measured while it is being processed in a CVD environment.

Since the temperature is monitored by the thermocouple, the pyrometer is not used to control temperature. Instead, open-loop processing is used. Two power settings were used. The first was at 14% lamp power (4900 watts), and the second at 20% power (7000 watts). For each power level, two charts were plotted. In the first chart, the lamp was ignited in an inert ambient (argon) at 2 torr, so that no deposition occurred. This plot gives the basic heating response of the oxide wafer to a fixed intensity of light. After allowing the wafer to cool, the recipe was repeated, but with silane and argon at a mixture of 1:3, so that deposition occurred. A different instrumented wafer was used for the other power level, repeating first the dry run, then following with the CVD run.

An absorption model was developed to account for the variation of temperature measured by the thermocouple. The assumption of the model is that radiation is either reflected or absorbed by the wafer, so that a calculation of the reflectivity due to deposited film thickness can infer the power absorption of the wafer, and therefore, its temperature.

Cross section transmission electron microscopy was used to evaluate the film thickness and develop a correlation between temperature and growth rate, determined previously in experiment 1. A JEOL 200 CX microscope was used.

2.3 Electrical Evaluation of POS Capacitors (Experiment 3)

Capacitors were fabricated by growing a thermal oxide on bare silicon, and then capping the oxide with the deposited polysilicon. The oxide was formed by rapid thermal heating of a bare silicon wafer in an oxygen ambient [17]. These polysilicon-oxide-silicon sandwich structures will be referred to as POS capacitors, similar to metal-oxide-semiconductor (MOS) structures, in which a metal such as aluminum is used as an electrode. MOS electrical techniques were then used to evaluate the electrical integrity of the capacitors. Two different comparisons were made; RTCVD vs LPCVD, and in-situ RTCVD vs ex-situ RTCVD.

In-situ processing refers to the process in which the RTO layer is grown on the oxide-isolated pads of bare silicon, then, without removing

the wafer from the chamber, a new set of process conditions (gas ambient, temperature, and pressure) is made and a second process is performed on the wafer. In this case, the ambient is changed from oxygen to a silane mixture while the lamp is idled at a low power, so as not to incite a premature deposition reaction. Since silane and oxygen are dangerously incompatible, there are a series of nitrogen purge steps in between the gas change. A diagram of a sample in-situ process is shown below in figure 5.

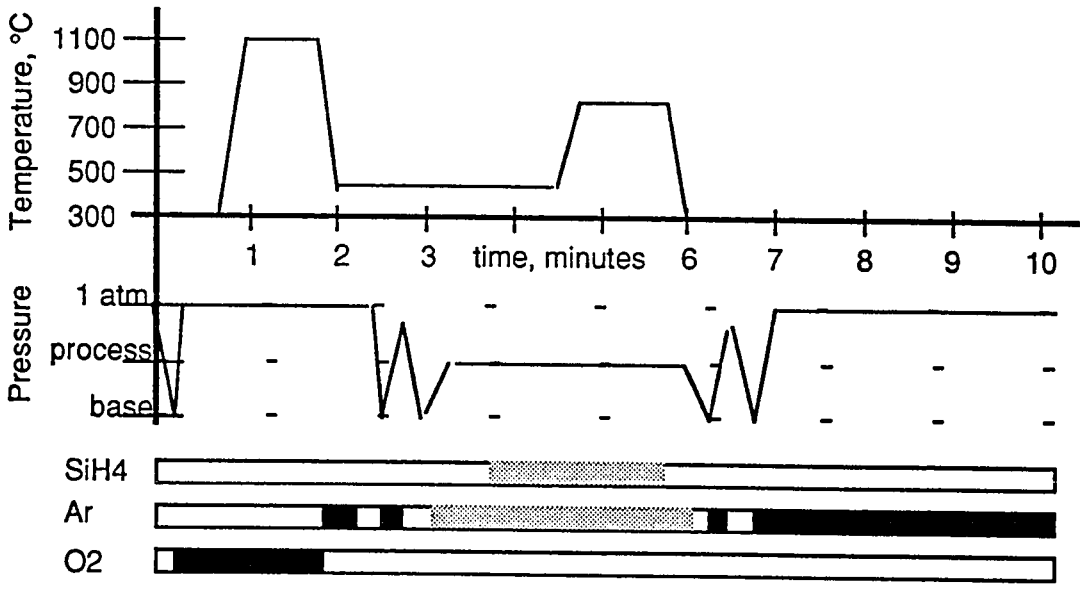


Figure 5 Graphical representation of a typical in-situ RTO/RTCVD process. The intial sample structure is bare silicon. After this process, a thin layer of oxide and a thin capping layer of polysilicon are added.

Since the oxidation reaction, the gas switch, and the deposition reaction require such drastically different temperatures, rapid thermal processing is ideally suited for in-situ processing. A typical tube furnace would not be able to modulate the temperature as rapidly.

2.3.1 RTCVD *vs* LPCVD

In the first POS evaluation, standard LPCVD polysilicon deposited in a furnace was compared to in-situ RTCVD polysilicon. The starting material was chemically cleaned p-type (100) silicon. On it, 500 nm thick SiO_2 was thermally grown in a tube furnace. Then, using common photolithography techniques, a pattern of holes was etched through the oxide down to the bare silicon substrate. This type of structure is commonly referred to as LOCOS isolation, as the thick oxide is used to electrically isolate the capacitor sites from each other. After pattern isolation, the wafers entered the RTP chamber for the dielectric oxidation. The thermal recipe of the rapid thermal oxidation (RTO) process was 1100 °C for 40 seconds in an oxygen ambient followed by a post-oxidation anneal at 950 °C for 60 seconds in argon. The purpose of the post-oxidation anneal is to improve the electrical properties of the capacitor by reducing interface trap concentrations [18]. The thickness of the oxide grown was 10 nm, the time and temperature calculated from previously published RTO kinetics investigations [19].

For the in-situ RTCVD process, the wafer was left in the RTP chamber after oxidation while the oxygen was pumped out and the lamp was idled at low power (<500 watts). Then, 25 v/o silane and 75 v/o argon was introduced at a pressure of 2 torr and the lamp was re-ramped to the process temperature of either 675 or 800 °C. Thus, the entire structure was formed from patterned bare silicon to poly-capped capacitor in one chamber. The capping protects the sensitive dielectric from contamination from airborne particles as it is removed from the chamber and carried away for further processing. Approximately 100 nm of polysilicon was deposited, with the deposition time calculated from the kinetics experiment of part 1. Afterwards, the RTCVD poly-capped wafer was brought to a tube furnace for deposition of an additional 200 nm LPCVD polysilicon. The purpose of the additional polysilicon is to produce a gate thickness which is commonly used. The reason that the entire 300 nm thickess was not deposited in the RTCVD system will be explained later in the discussion section. It has to do with the fact that the thermal budget of the RTP process has to be kept low in order to prevent unwanted deposition in the chamber and optical surfaces.

In the case of LPCVD silicon, the oxidized wafer was removed from the RTP chamber and placed in a standard tube furnace, where the same thickness of polysilicon (300 nm) was deposited. The intent of this experiment was to compare new in-situ RTCVD polysilicon to an existing polysilicon process.

Both types of wafers (RTCVD and LPCVD) were then implanted with

$^{31}P^{+}$ ions (31 amu phosphorus atoms with valence +1) into the polysilicon film and then annealed. Reactive ion etching was used to define the capacitor sites, with the polysilicon gate larger than and overlapping the dielectric. The area of the capacitors was 1.83 mm^2. The backside of the wafer was electrically contacted by sputtering an aluminum film, then annealing at 400 °C.

Pulsed capacitance-voltage (C-V) measurements were used to determine the flatband voltage and high frequency (1 MHz) and quasi-static C-V was used to determine the interface state density (D_{it}) [20]. Voltage ramping was used to measure the oxide breakdown voltage (V_{bd}) distribution. Breakdown was defined as the voltage needed to produce a current of 2 μA across the dielectric.

2.3.2 in-situ RTCVD *vs* ex-situ RTCVD

In the second POS experiment, in-situ RTCVD polysilicon was compared to ex-situ RTCVD polysilicon. In the latter case, the wafers were removed from the RTP chamber following oxidation, allowed to sit in a clean room for several hours, then put back into the RTP chamber for the deposition of polysilicon. The intent of this experiment was to determine the advantages of in-situ processing verses any possible delitrious affects of exposure to a clean room environment. The clean room storage environment in this case was rated "class 100," or 100 particles per cubic

foot. The smallest measurable particle diameter was 0.5 μm.

As with the LPCVD *vs* RTCVD experiment, the starting material was high resistivity (> 10 Ω-cm) p-type (100) silicon with LOCOS oxidation. However, in this case, a larger size capacitor (7.3 mm^2) was also evaluated along with the 1.8 mm^2 capacitors. The target RTO gate dielectric thickness was 15 nm, grown at 1100 °C in pure oxygen. The deposition conditions were 850 °C for 45 seconds in 1 v/o silane to 3 v/o argon at a total pressure of 2 torr. The target polysilicon thickness was 200 nm. The ex-situ wafers were stored in the class 100 environment for 12 hours in between the RTO and the RTCVD polysilicon. To eliminate process variations, the process sequence alternated between in-situ and ex-situ splits, by having the gate oxide of the ex-situ wafers prepared in advance.

After poly deposition, the poly was doped with phosphorus, using diffusion doping techniques with $POCl_3$ [21]. Then, reactive ion etching was used on the polysilicon to define the gate structures. Following etch, a thick passivation layer of silicon dioxide was deposited over the entire wafer and contact holes were etched to expose the doped poly gates. Then, a blanket layer of 60 nm thick titanium was sputtered on the wafers. They were annealed in the rapid thermal processor at 850 °C for 45 seconds in an argon ambient, in order to react the Ti with the polysilicon, forming $TiSi_2$. The unreacted Ti was then selectively wet-etched away in a 50 °C, 15 minute bath in selective etch solution (1 part 2% hydrogen peroxide, 1 part ammonium hydroxide, 5 parts de-ionized water). Finally, the capacitors, consisting of a dual-layer doped poly + $TiSi_2$ gate, were annealed at 400 °C

in forming gas (N_2 w/ 10% H_2), the purpose of which was to minimize the contact resistance of the surface metal by removing oxygen from the surface of the gate.

The electrical evaluation consisted of quasi-static and high frequency capacitance-voltage (C-V) measurements combined with high field Constant Current Stressing (CCS) [22]. Automated current-voltage (I-V) measurements were performed on 500 capacitors to obtain a statistical distribution of the oxide breakdown voltage (V_{bd}). V_{bd} was defined as the voltage needed to produce 1 μA per cm^2 of leakage current.

One comment on the reason for the differences in capacitor processing between the LPCVD *vs* RTCVD experiment and the in-situ *vs* ex-situ RTCVD experiment. These were carried out at different times, with the cooperation of different companies. In the former case, the collaboration was done with the IBM corporation in Burlington, Vermont. In the latter case, fab processing (aside from RTO and RTCVD) was performed at Intel corporation in Santa Clara, California. Each facility has its own recipe for making electrical test structures and its own set of testing procedures. It is therefore more valid to compare the results of the splits within each experiment than to compare one test to the other.

Chapter 3
RESULTS

3.1 Kinetic and Material Analysis

3.1.1 Growth Kinetics

The results of the Table 1 time, temperature, and partial pressure matrix is shown in figure 6, which plots the polycrystalline silicon film growth rate as a function of inverse temperature. The error bars on each data point represents the standard deviation of all of the measurements (5 per wafer) for the different length depositions at the same temperature. The slope of this Arrhenius plot indicates that the activation energy for both partial pressures of silane is 1.5 eV at temperatures below 800 °C. This is identified as the surface reaction-limited regime, since the growth rate is determined by the temperature of the wafer surface. Above that temperature, there is much less temperature dependence on growth rate. This is identified as the gas phase-limited regime, because the deposition rate on the wafer surface is so high that the reaction is controlled by the transport of new silane to the wafer. The lower partial pressure of silane results in a lower deposition rate because there are less reactive species present. However, the activation energy and transition temperature between growth mechanism changes appear to be the same.

The assertion of a change in mechanism is further substantiated by observing the uniformity of the polysilicon film thickness across a wafer.

Under 800 °C, there is fairly good uniformity, as seen by the lack of many color changes across the wafer. The color changes are the result of interference affects when light passes through the layer of poly and the layer of oxide, which has a different refractive index. For poly films which were 100 nm thick, a yellowish gold color resulted. For films between 200 and 600 nm thick, alternating reds and greens appeared. As measured by the spectrophotometer, the 5 points across the wafer were within 5% standard deviation.

By contrast, the films deposited above 800 °C showed concentric color fringes. The 5-point thickness measurements showed that the center film thickness was on the order of half the edge film thickness. This is characteristic of the gas transport in the RTP chamber, as the gas distribution is radially delivered from the 4 corners of the rectangular chamber.

All other common RTP processes occur with an excess of ambient gas (such as oxidation and anneal in an inert ambient), so the chamber has been optimized to deliver the best temperature uniformity possible, while the gas delivery has not been optimized.

3.1.2 UV-Visible Reflectometry

The reflectance spectrum of a film deposited at 650 °C is compared to the spectrum of one deposited at 700 °C in figures 7a and 7b. They indicate

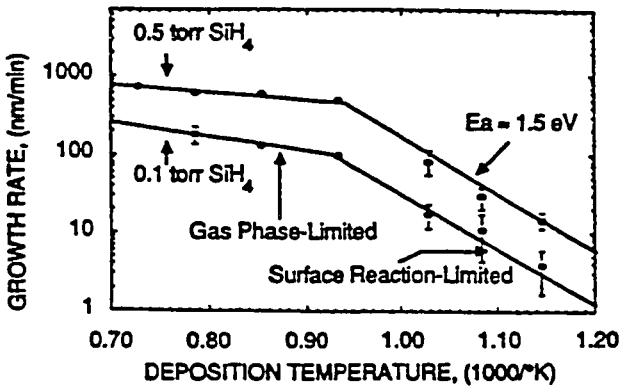


Figure 6 Deposition rate for polysilicon deposited in a rapid thermal processor as a function of reciprocal deposition temperature for two partial pressures of silane in argon. The total deposition temperature is 2.0 torr.

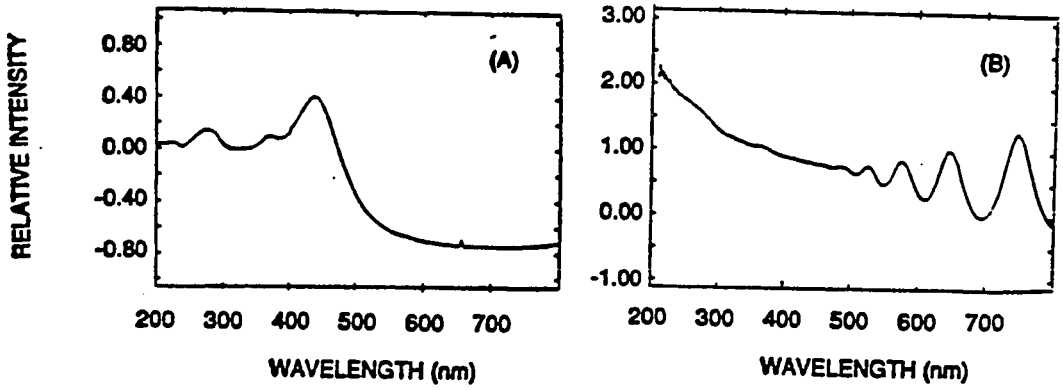


Figure 7 Optical reflectance spectra of polysilicon on 100 nm SiO_2. The samples are referenced to single-crystal silicon. Presence of peaks at 270 and 380 nm suggest a partially amorphous film. Deposition temperatures are (A) 650 °C and (B) 700 °C.

that there is a transition from amorphous to crystalline material, as evidenced by reflectance peaks at 270 and 380 nm in the 650° sample which disappear at 700 °C. Since the spectra are relative reflectivities when compared to a single-crystal silicon sample, these peaks, which are characteristics of a crystalline silicon structure, should not be prominent unless the sample is not crystalline. These results were representative of all of the samples. They were further confirmed by removing the chopped signal and using a mirror reference to provide a measurement of the reflectivity of the sample. In this case, amorphous character was determined by the absence of the characteristic absorption peaks.

The surface roughness *vs* film thickness is plotted in figures 8a and 8b for various deposition temperatures. The two values for each thickness, measured at 200 and 321 nm, are in reasonable agreement with each other. Surface roughness increases with increasing film thickness. It also generally increases with increasing deposition temperature. However, figure 8b shows that the surface roughness increases rapidly from 650 to 700 °C, decreases from 700 to 900 °C, then increases with increasing temperature above that. This trend has previously been observed for polysilicon deposited in an LPCVD reactor between the temperatures of 550 to 750 °C [6]. The films deposited in a rapid thermal processer have a smoother surface than LPCVD films having the same thickness and deposition temperature.

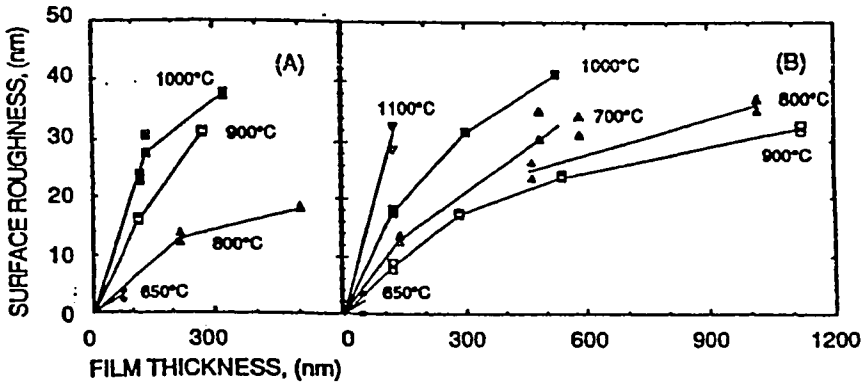


Figure 8. Surface roughness vs film thickness and deposition temperature for 2 partial pressures of silane; (A) 0.1 torr, (B) 0.5 torr.

3.1.3 X-Ray Diffraction

Studies of the X-ray samples confirm the transition temperature from amorphous to polycrystalline films. The diffraction intensity *vs* Bragg angle for various deposition temperatures is shown in figure 9. The sample deposited at 600 °C showed no diffraction peaks (not shown). The sample deposited at 650 °C showed the onset of characteristic peaks, but their heights were too small to measure accurately. The samples deposited at 700 °C and above exhibited the characteristic (111), (220), and (311) peaks 23-26.

The raw data typified in figure 9 were normalized to determine the dominant orientation of the grains. The peak intensity is first normalized with respect to a completely random powder pattern using a factor of;

I/I_{pp} = 1.0, 0.6, and 0.35 for the (111), (220), and (311) peaks, respectively, where

I = the measured peak height

I_{pp} = the intensity from randomly oriented polysilicon [27].

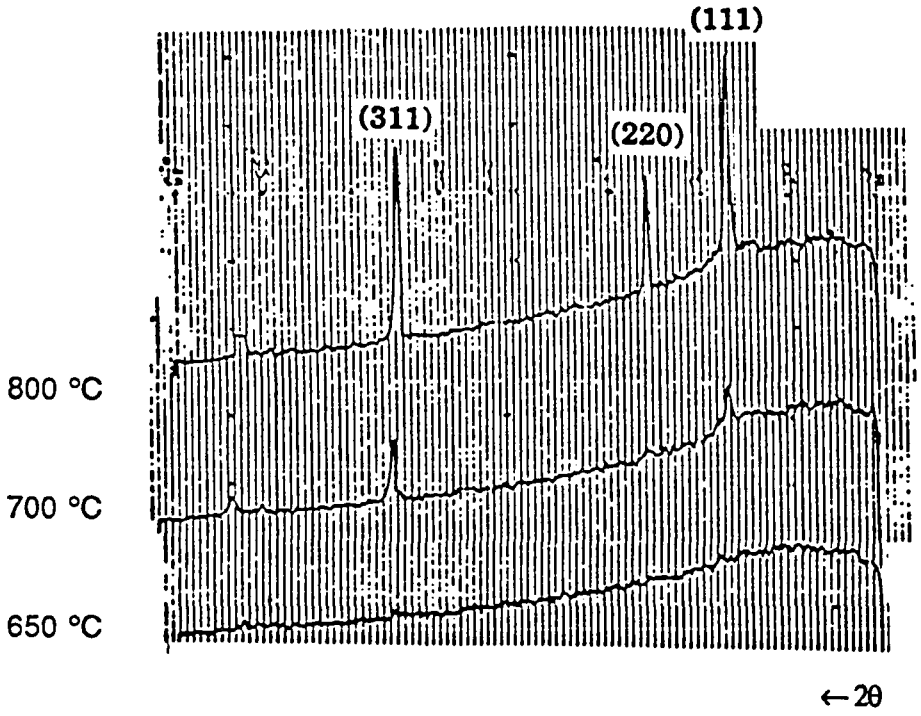


Figure 9. Raw X-ray diffraction data for 3 deposition temperatures.

Then, the samples are also normalized for the finite film thicknesses by dividing by a correction factor, G [28];

$$G = 1 - \exp(-2\mu t/\sin\varnothing)$$

where t = film thickness

$\mu = 143.1\ cm^{-1}$ is the x-ray absorption coefficient

$\varnothing$ is the Bragg angle of the X-ray peak.

Using this analysis, the dominant grain orientation is found to be (100) for the samples deposited at 700 and 800 °C, and (311) for the sample deposited at 1100 °C. These results are shown in figure 10.

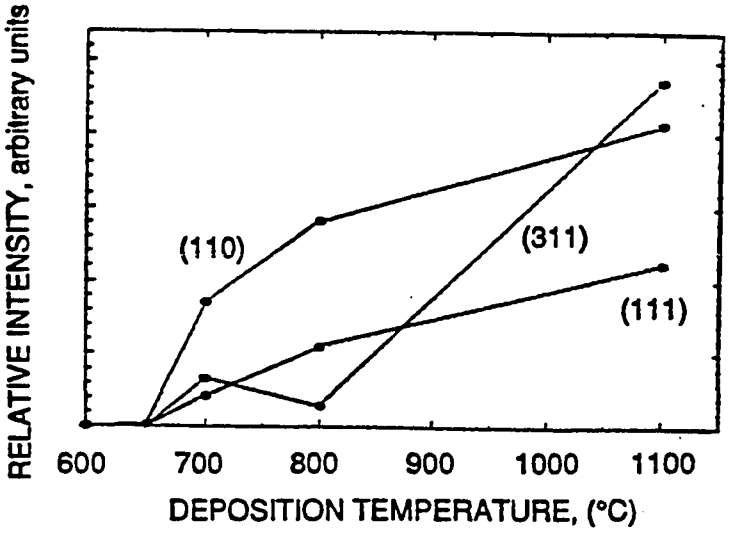


Figure 10 Normalized X-ray diffraction intensities of 3 crystallographic orientations for 5 films, deposited at 600, 650, 700, 800, and 1100 °C.

3.2 Optical Absorption Analysis

3.2.1 Thermocouple Measurements

The temperature curves for the two lamp power settings are shown in figures 11 (14% power) and 12 (20%), where thermocouple temperature is charted as a function of time. In each figure, 2 curves are shown. In the case of heating in an inert ambient, no deposition occurs. The wafer initally heats up quickly, then levels off in temperature. Naturally, this leveling off occurs at a higher temperature when 20% power is used compared to 14% power. The gradual increase in temperature can be explained by the gradual heating of the quartz window which forms the ceiling of the chamber. Although it is transparent to the lamp radiation, it can be heated by infrared radiation emitted from the hot wafer.

In the case of open-loop polysilicon deposition, the temperature is seen to vary widely as the film growth occurs. The temperature swing is approximately 120 °C in the case of figure 11, and 80 °C in the case of figure 12. When the initial poly is deposited, the thin film is golden yellow in color, and highly reflective. This was observed in Part I, by observing the thin films deposited at low temperatures and short times, as well as by the surface reflectance data. As the reflectivity increases, the absorbed lamp radiation, and therefore, the wafer temperature, decreases. As the film thickness increases, so too does the roughness. The film becomes less reflective and more absorptive to the lamp radiation. There are a few small temperature variations in the latter part of figure 11, caused by changes in

absorption due to interference effects. As mentioned previously, as the thickness of the film increases in the 20-40 nm thickness range, it alternates colors between green and red. In figure 12, the temperature recovery occurs much faster, since the film is deposited at a faster rate at the higher temperature.

In figure 11, the temperature of the open-loop deposition is seen to vary between 580 °C and 700 °C. Since it was reported in Part 1 that the amorphous to polycrystalline transition temperature was within that range, some interesting morphology should be expected. Cross-section TEM, shown in figure 13, confirms the existence of an amorphous phase sandwiched between two polycrystalline phases. Using the 100 nm underlying SiO_2 as a reference, the total film thickness is approximately 500 nm.

The measured temperature of the figure 11 deposition can be used to calculate the deposition rate of the deposited film. Using the Arrhenius equation,

$$R = R_0 \exp(-E_a / k T),$$

where

R = rate

R_0 = a constant

E_a = the activation energy of 1.5 eV, calculated from Part 1

k = the Boltzmann constant

T = the absolute temperature of the deposition,

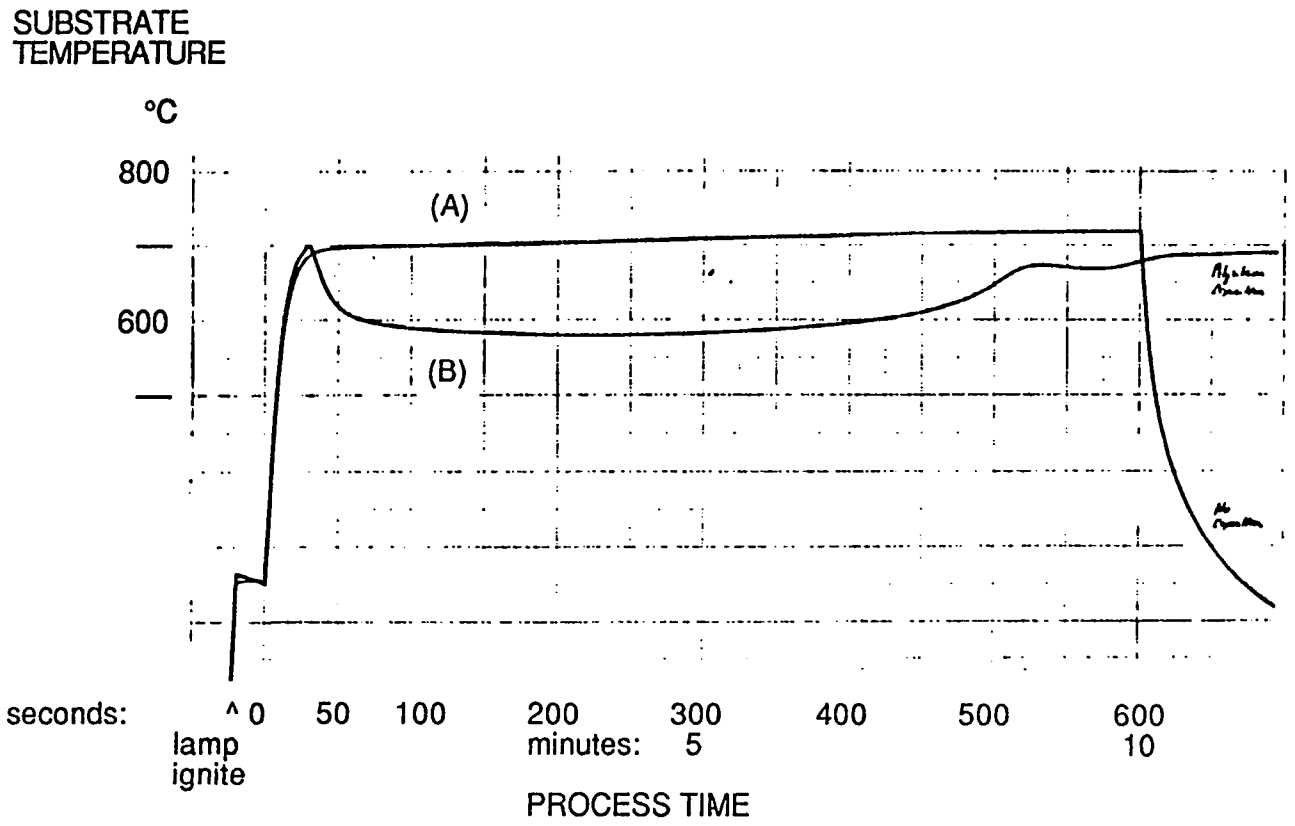


Figure 11 Substrate temperature as a function of time as measured by an embedded thermocouple. The lamp power was constant at 4.9 KW. The two curves shown are (A) no deposition, and (B) during silicon deposition. In the case of (A), the lamp was turned off after 10 minutes.

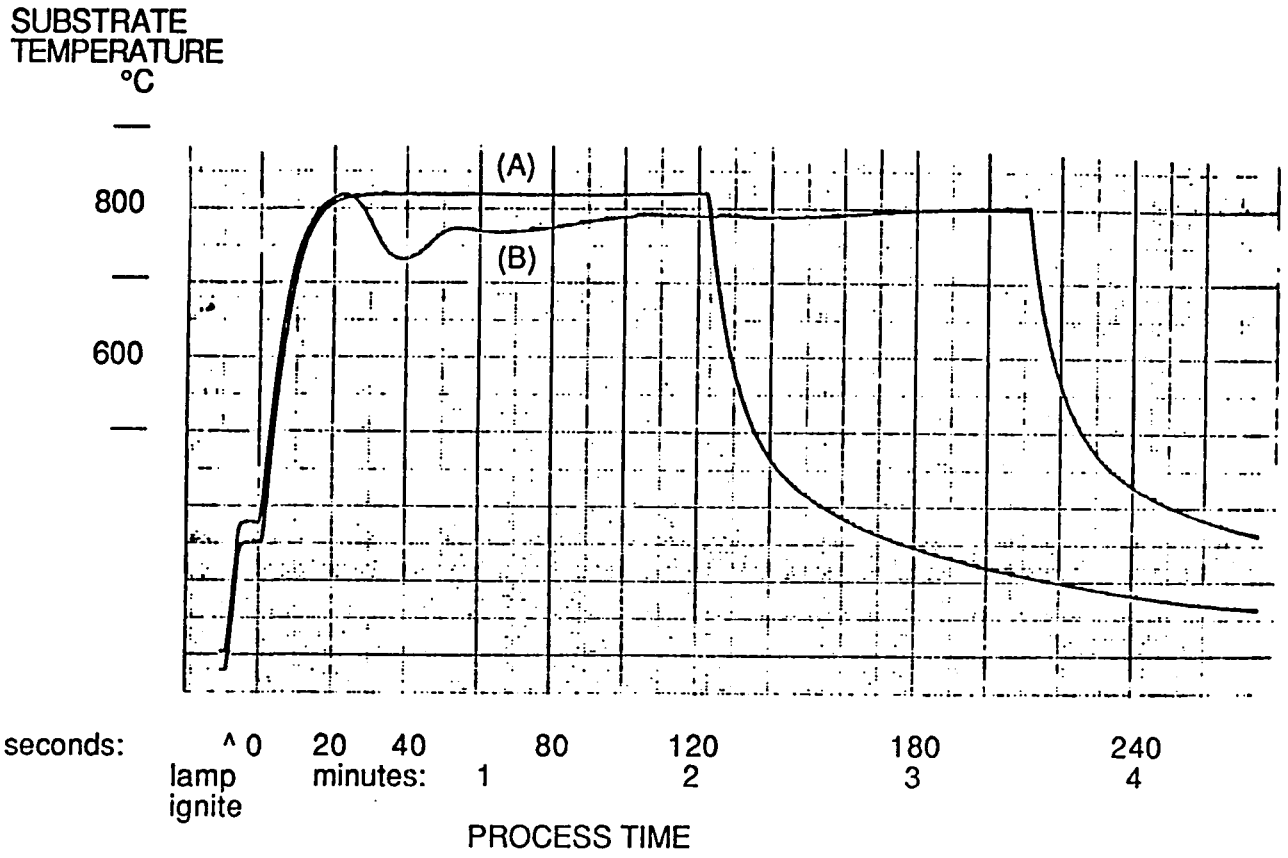


Figure 12 The constant lamp power was set to 7.0 KW. The two curves are (A) no deposition, and (B) silicon deposition. In the case of (A), the lamp was turned off after 2 minutes. In the case of (B), after 3.5 minutes.

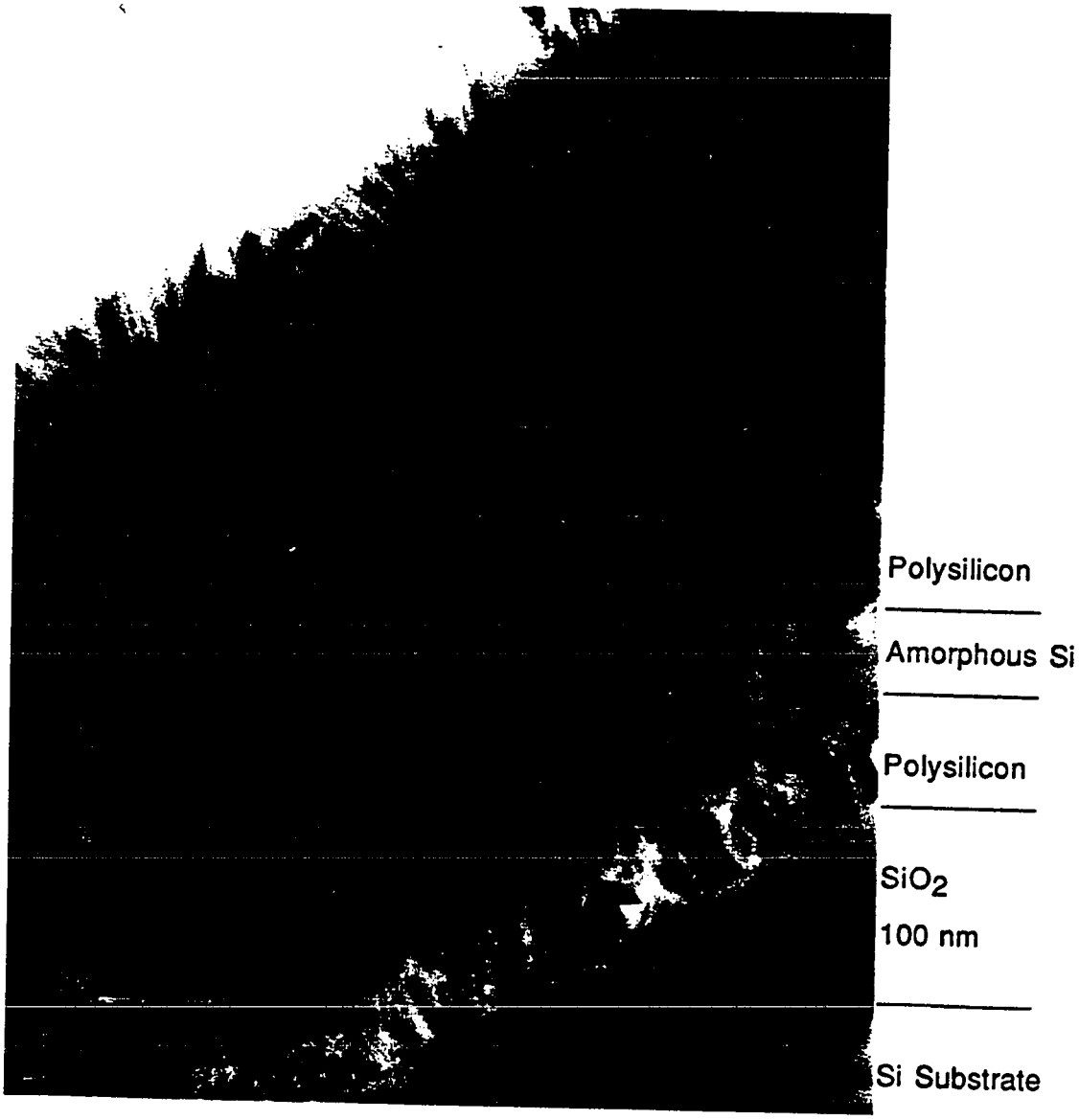


Figure 13 Cross-section transmission electron micrograph of the silicon film deposited at fixed 4.9 KW lamp power. The change of silicon phase during film growth is caused by the drop in temperature as a result of a reduction in absorptivity of the substrate.

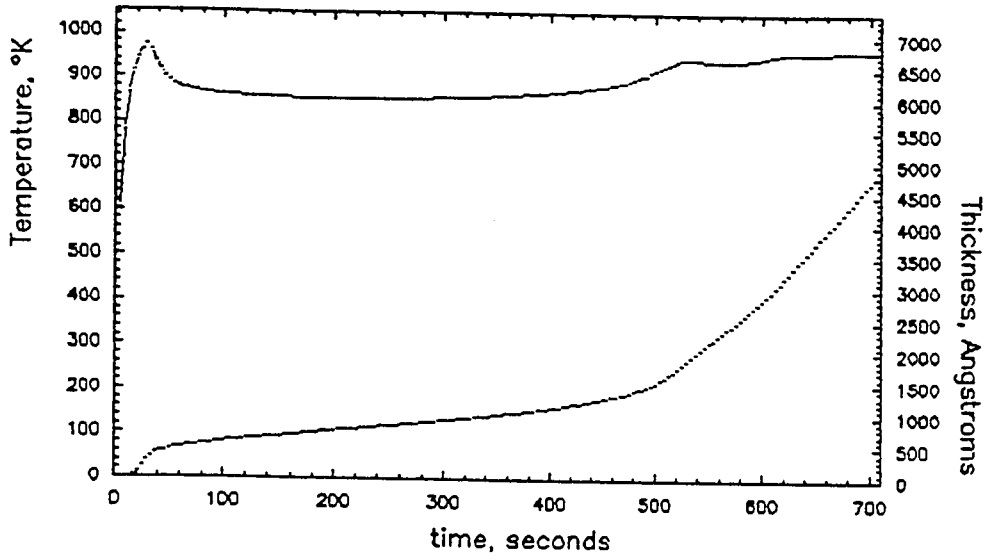


Figure 14 Combining the kinetics data of figure 6 with the temperature data of figure 11 (which is duplicated on the top portion of the above graph), the film thickness vs time can be calculated. Initially, there is a fast growth, followed by a long period of slow growth, followed by an increase in growth rate.

the calculated thickness is plotted *vs* time in figure 14, superimposed under the thermocouple-measured temperature. The total thickness of the film, as well as the thickness of the low temperature amorphous layer, are in reasonable agreement with the TEM micrograph. Any underestimation of the amorphous layer thickness can be attributed to self-crystallization, as the temperature increased for the final stages of the deposition.

3.2.2 The Model

3.2.2.1 Calculations

The change in wafer absorption causing the large change in wafer temperature during deposition can also be modeled by an understanding of the layered system as it forms as well as by understanding the spectral output of the lamp. Because the wavelength dependence of optical properties of silicon films is not well understood, the calculations are only qualitative.

The basic model consists of calculating the reflectance of a 3-layer structure consisting of a silicon film of varying thickness, a fixed thickness of silicon dioxide, and a lightly doped silicon substrate. The index of refraction of the deposited polysilicon film is taken to be the same as the substrate. Both the real and imaginary parts of the index are considered, using the values given in a reference [29]. The refractive index of the oxide is taken to be 1.46 over the entire wavelength considered.

The overall reflectance of the 3-layer system at a given wavelength is calculated from the expression [30,31] :

$$R = \frac{r1 + r2 \exp(-2j\partial 1) + \exp[-2j(\partial 1 + \partial 2)] + r1\, r2\, r3 \exp(-2j\partial 2)}{1 + r1\, r2 \exp(-2j\partial 1) + r1\, r3 \exp[-2j(\partial 1 + \partial 2)] + r2\, r3 \exp(-2j\partial 2)}$$

where $r1 = (n_{i-1} - n_i) / (n_{i-1} + n_i)$ is the Fresnel coefficient of the ith interface, $\partial i = 2\pi n_i\, di / \lambda$, and normal incidence is assumed.

The fraction R of the incident power reflected from the sample at a given wavelength is then calculated from the expression:

$$R = |R|^2.$$

All of the energy not reflected is transmitted into the sample where it is assumed to be absorbed by the silicon film or the silicon substrate and contribute to the wafer heating. This is a reasonable assumption because; 1) the substrate is relatively thick, 2) the spectral output of the lamp radiation is in the visible range, and 3) the temperature during deposition is above 600 °C. Under these conditions, there is not expected to be any transmission of the radiation through the wafer [32]. The total power absorbed is then found by integrating the power absorbed at each wavelength and weighting the values with the amount of incident radiation at each wavelength. The spectral output of the lamp is taken from reference (33) for a Xenon plasma. Only the wavelength range between 200 and 800 nm is considered, since it contains most of the lamp power. The longer wavelengths are also reduced by the cooling water surrounding the lamp. The shorter wavelength intensities are reduced by the titanium-doped quartz water jacket used to contain the cooling water.

The result of the model is shown on figure 15, which plots the fraction of power absorbed as a function of the deposited silicon film thickness. Roughly, it can be seen to correspond to the observed changes in temperature observed by the thermocouple readings. As the initial poly is

deposited, the absorption of lamp radiation decreases rapidly to a minimum. As the thickness increases, there are periodic oscillations of absorption levels. However, because of the broad spectrum of the incident lamp light, subsequent minima are of less magnitude.

3.2.2.2 Discussion of the Model

The calculated power absorption values shown in figure 15 are only qualitative because of the assumptions in refractive indices. It was assumed in the calculations that the index of refraction of the deposited polycrystalline silicon was the same as that of the single-crystal substrate. However, because of its less perfect structure, the wavelength dependence of the refractive index is expected to be weaker, especially at shorter wavelengths. Also, the refractive indices were assumed to be temperature independent. Both real and imaginary components of the refractive index of silicon increase with increasing temperature. This has been shown to hold for longer wavelengths [34-36], although the trend is not well characterized for shorter wavelengths.

Also, the model didn't consider what happens to the refractive index as the film morphology changes. Refractive index is expected to be different for amorphous films. At longer wavelengths, it is expected to be greater than for crystalline silicon. However, the characteristic structure in the refractive index of crystalline silicon at shorter wavelengths is

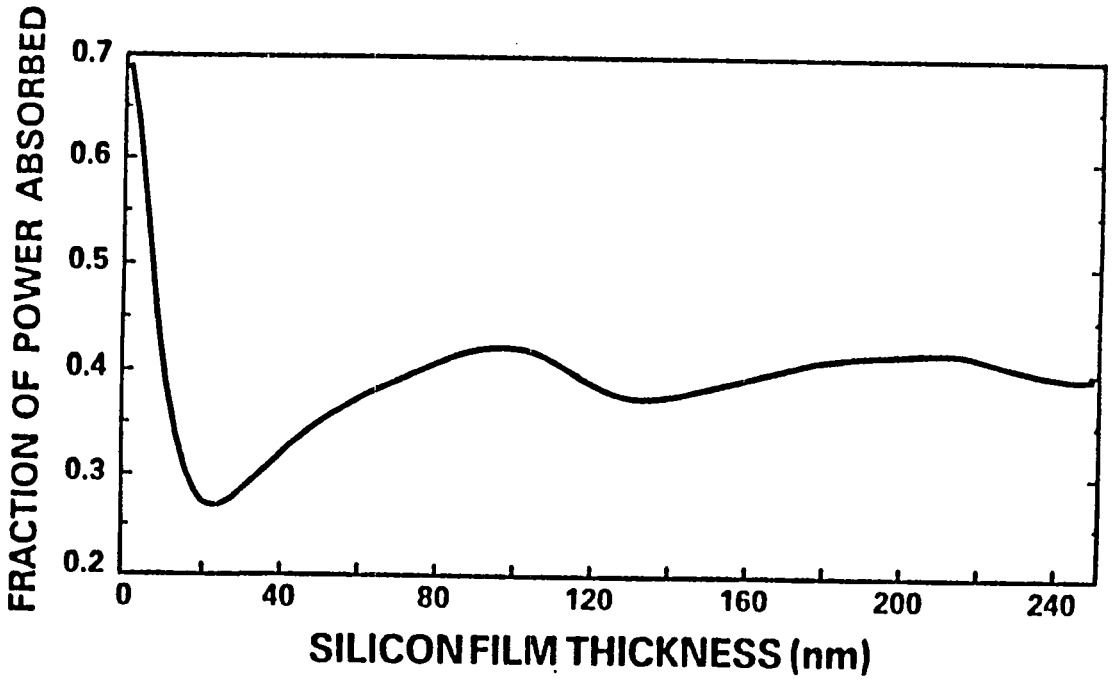


Figure 15 Calculated relative power absorbed *vs* deposited silicon thickness.

expected to be almost completely absent in amorphous silicon, and the index of refraction would be lower than that of crystalline silicon at some wavelengths. Attempts to model the thin amorphous layer were frustrated by the sensitivity to its index of refraction, especially near the critical wavelengths of 370 and 280 nm associated with the structure of crystalline silicon.

If the index of refraction of the amorphous layer is higher at wavelengths with the most incident power, the overall reflectance should increase when the depositing film becomes amorphous, further diminishing the power absorbed. Thus, when a phase change occurs during the deposition, the temperature swing is expected to be greater than in a deposition which is purely polycrystalline. This prediction is confirmed in figures 11 and 12, where the larger temperature drop of 120 °C occurs at the lower power, while a drop of only about 80 °C occurs at the higher deposition.

3.3 Electrical Evaluation of POS Capacitors

3.3.1 RTCVD *vs* LPCVD

The uniformity of the RTO thickness was evaluated by measuring the capacitance (C_{max}) at accumulation (-3 V) [37], and the deviation was found to be less than 4%, which is consistent with measurements made on bare unpatterned silicon wafers which were oxidized using the same RTO

recipe and measured on a mapping ellipsometer.

The results of the C-V analysis are shown in Table 2, which lists the flatband voltage (V_{fb}) and trap density at the sustrate-oxide interface (D_{it}) for the three split conditions. All the results are comparable, indicating that the RTCVD polysilicon deposition does not induce any additional interface charges compared to a standard process. Some C-V plots are shown in figures 16 and 17. There are no observed electrical anomalies found in the RTCVD samples, indicating that even though fast heating and cooling cycles are involved in the RTCVD, the original SiO_2/Si interface is not disturbed.

However similar their C-V properties, different dielectric breakdown behaviors were found for the standard *vs* `in-situ POS structures. These are shown in figures 18 (for the LPCVD capacitors) and 19 (for the in-situ RTCVD capacitors). Each figure shows the results of capacitors from 4 different wafers. Each wafer contained approximately 70 capacitors. The capacitors without an in-situ polysilicon capping layer have a wide distribution of breakdown voltages from 6 to 13 MV/cm^2. 10% of the devices failed, meaning that they broke down below this range. These results are indicated by the white bars of figure 18. For the second ramp, there was a tremendous degradation rate, as indicated by the black bars of figure 18.

By contrast, the POS capacitors fabricated with in-situ RTCVD polysilicon showed a tight distribution of breakdown voltages between 11 and 13 MV/cm^2, as shown in figure 19. Only 2% experienced low voltage field failures. After the second ramp, 97% of the in-situ capacitors tested

Table 2
C-V RESULTS

Electrode description	V (Volts)	D_{it} (/ cm^2 / eV)
LPCVD Poly Si (300 nm)	-0.85	1.8×10^{10}
LPCVD Poly Si (200 nm) over 675 °C RTCVD poly Si (100 nm)	-0.86	2.1×10^{10}
LPCVD Poly Si (200 nm) over 800 °C RTCVD poly Si (100 nm)	-0.87	1.7×10^{10}

showed the same or higher breakdown voltage (the increase, seen in about 2% of the devices, can be attributed to residual charge caused by the trapping of electrons from the first ramp).

The width of the initial breakdown distributions indicates that defects are generated in the devices as a result of transporting the freshly oxidized wafers from one lab to another for subsequent processing. Even in a cleanroom environment, the exposed oxide can be contaminated with airborne particulates or mobile ions from contacts with metal surfaces, such as wafer tweezers or wafer transport handlers. The degradation observed in the ex-situ wafers between ramps indicates that not only is performance and yield affected by these factors, but also reliability. The thin polysilicon capping layer has been demonstrated to provide sufficient

protection to the devices during transport. No difference in behavior was found between wafers processed with RTCVD polysilicon at 675 or 800 °C.

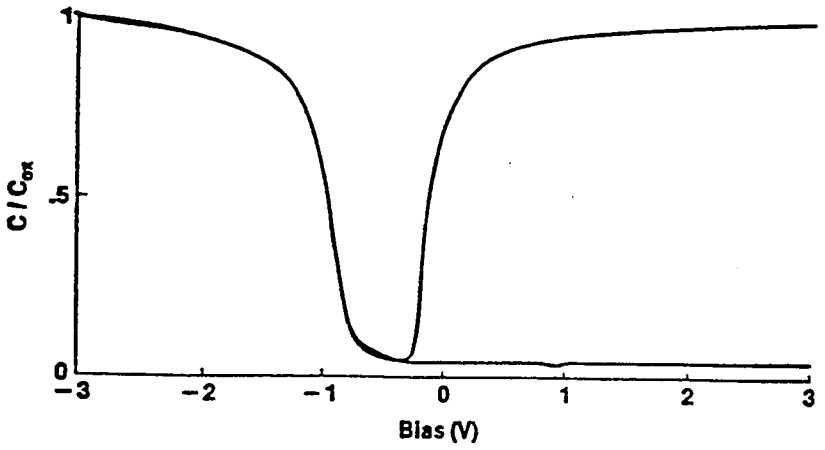


Figure 16 High frequency (1 MHz) and Quasi-static C-V plot for a thin SiO2 film with in-situ RTCVD polycrystalline silicon deposited at 800 °C.

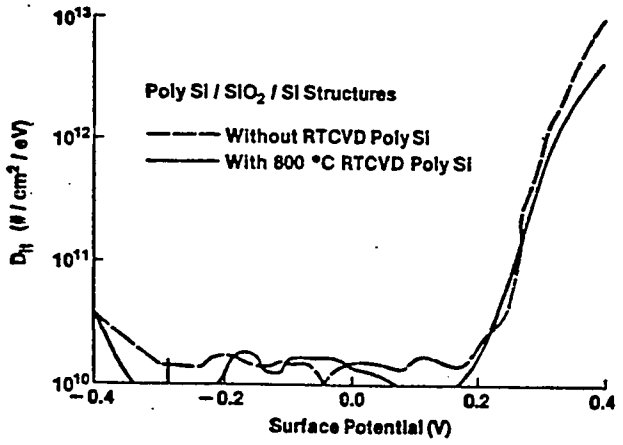


Figure 17 Comparison of interface state density as a function of surface potential for ex-situ LPCVD poly electrode and 800 °C in-situ RTCVD poly electrode.

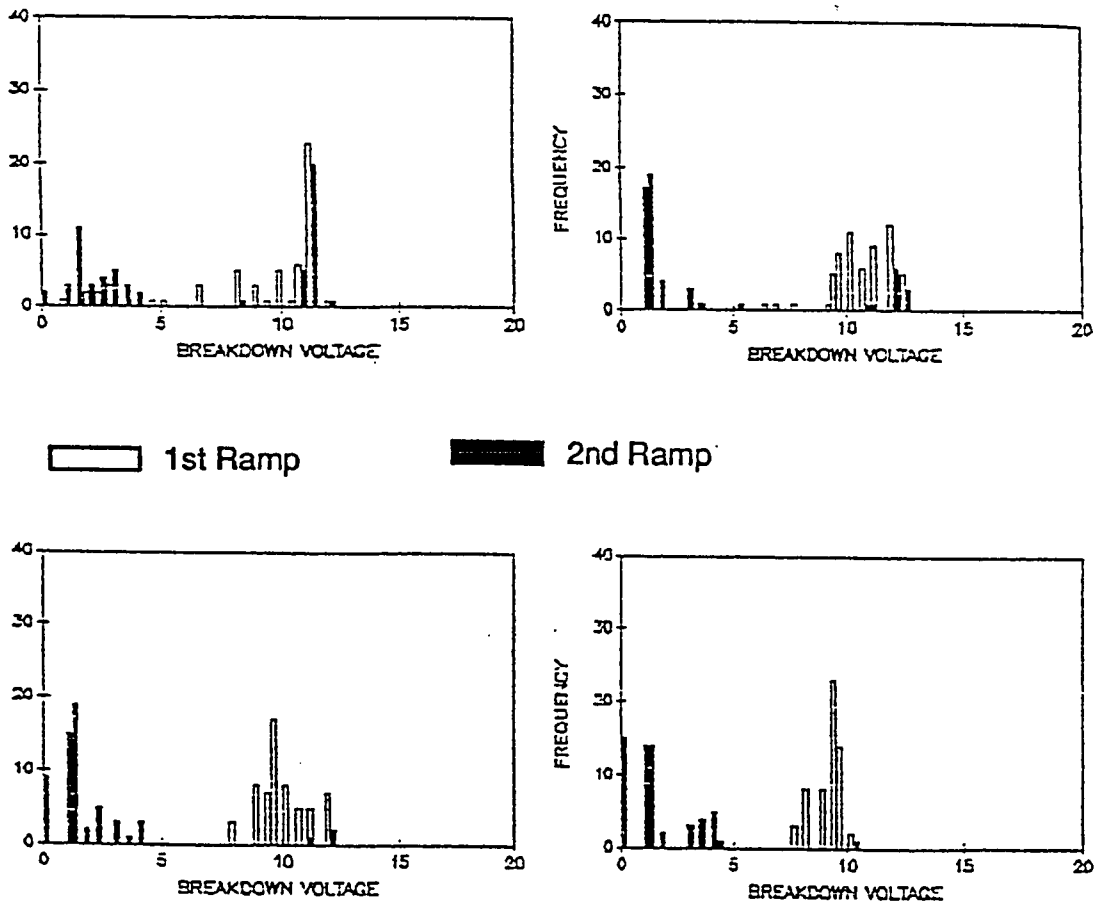


Figure 18 The breakdown distributions of capacitor sites on 4 wafers processed with ex-situ LPCVD polysilicon. V_{bd} is in units of MV/cm^2, and frequency is in unit capacitor devices.

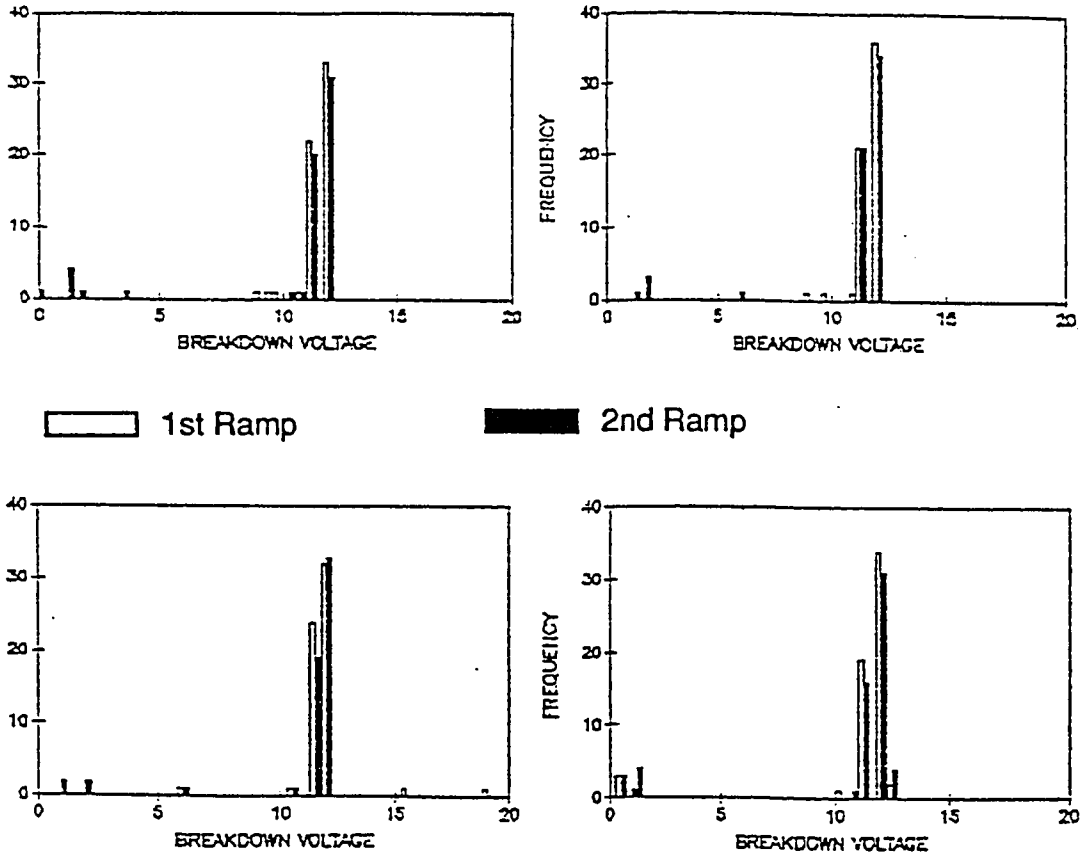


Figure 19 The breakdown distributions of capacitor devices on 4 wafers processed with in-situ RTCVD polysilicon as a protective capping layer, then supplemented with LPCVD polysilicon. Compared to the ex-situ case, the distributions are narrower with a lower incidence of early failure. The reliability is dramatically improved, as evidenced by the lack of degradation after first ramp.

3.3.2 In-situ *vs* Ex-situ RTCVD Polycrystalline Silicon

Similar results to the previous comparison were made, indicating that the properties observed have more to do with the in-situ *vs* ex-situ processing and not the nature of the polysilicon deposition. For instance, figure 20 shows a comparison of the in-situ (a) and ex-situ (b) C-V curves. They are similar. Both exhibit respectable levels of oxide charge (N_{ox} ~ 5 x $10^{10}/cm^2$) and mid-gap interface state densities (D_{it} ~ 5 x $10^{10}/cm^2$) with no current stress. After high field substrate injection (constant current stress at 0.5 mA/cm^2 for 1000 sec) the interface state generation appears identical in both cases. This is shown in figure 21. Electron trapping characteristics were obtained by monitoring the gate voltage as a function of injected charge. Both the in-situ and ex-situ capacitors were found to exhibit identical trapping behavior.

The comparison of breakdown histograms again shows an improvement with the in-situ case. The small area capacitors are compared in figure 22 and the large area capacitors in figure 23. In the case of the small area devices, the in-situ distribution was narrow. Furthermore, the yield was 100% (There were no shorts through the dielectric). By contrast, the distribution of the ex-situ capacitors was wider, and exhibited a bimodal distribution (a significant number of capacitors broke down around 6 MV/cm^2). There were also 3 capacitors which failed, indicating that perhaps particulate contamination between the oxide and the poly caused a mechanical breakdown in the dielectric. The bimodal

distribution may be an indication of a critical size or species of particle. A similar result is seen for the large area capacitors. Again, the distribution was wider for the ex-situ process, which had a bimodal distribution. Again, the in-situ capacitors provided a 100% yield compared to 7 failures of ex-situ capacitors. The greater incidence of failure is expected if it is caused by particle contamination, since a larger area device would statistically accumulate more particles.

3.3.3 Summary

In both comparisons, devices produced using RTO SiO_2 and in-situ RTCVD Si exhibit the same C-V characteristics as ex-situ processes. The first comparison showed that there was no electrical difference between the polysilicon produced in a rapid thermal processor and the polysilicon produced in a low pressure tube furnace as far as could be determined by C-V analysis. The second comparison showed that the in-situ process did not change these characteristics over the ex-situ case.

The big difference in both cases was the improvement in capacitor performance as a result of in-situ processing. Because a polysilicon protective film is placed on the wafer before it is exposed to the air, there is less of a chance for contamination of the oxide layer. This exposure of unprotected oxide is believed to be responsible for yield loss and degradation in dielectric strength and reliability.

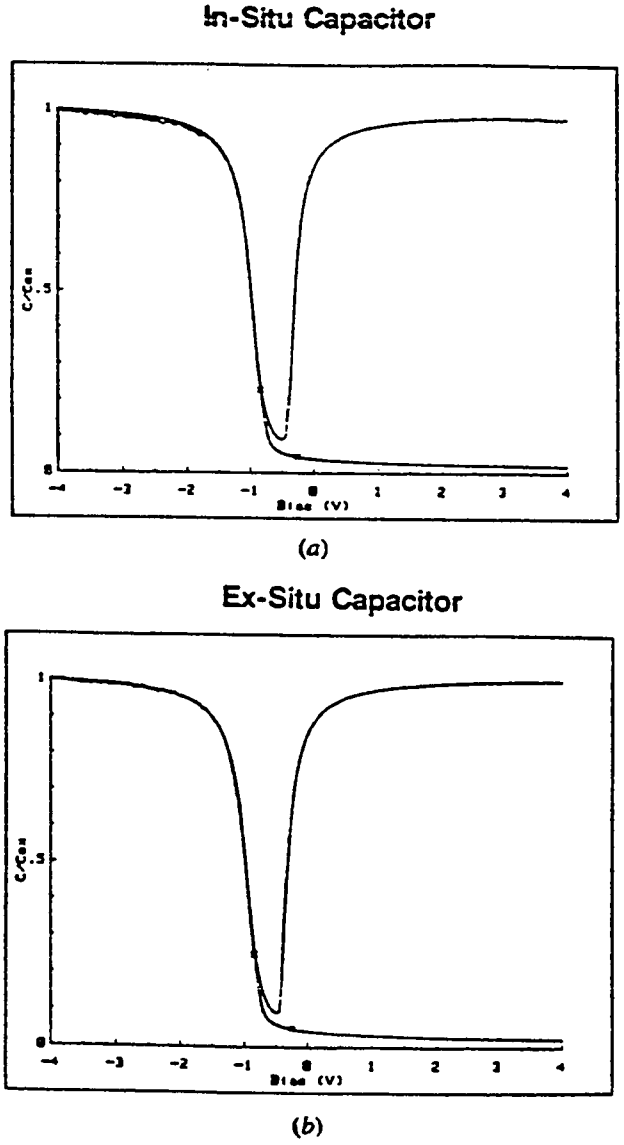


Figure 20 High frequency and quasi-static C-V characteristics of electrically unstressed (a) in-situ and (b) ex-situ capacitors.

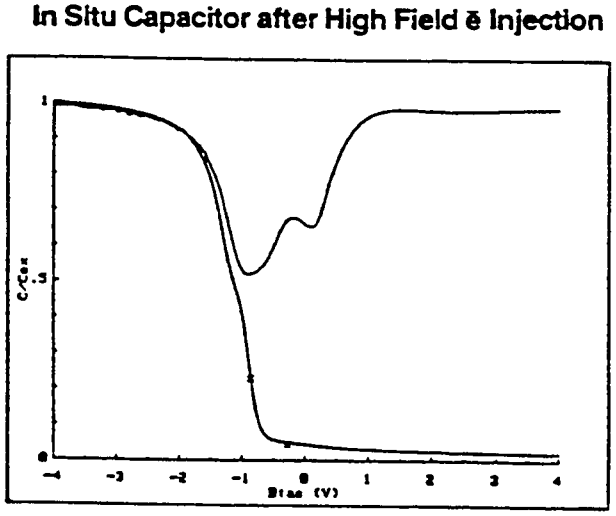
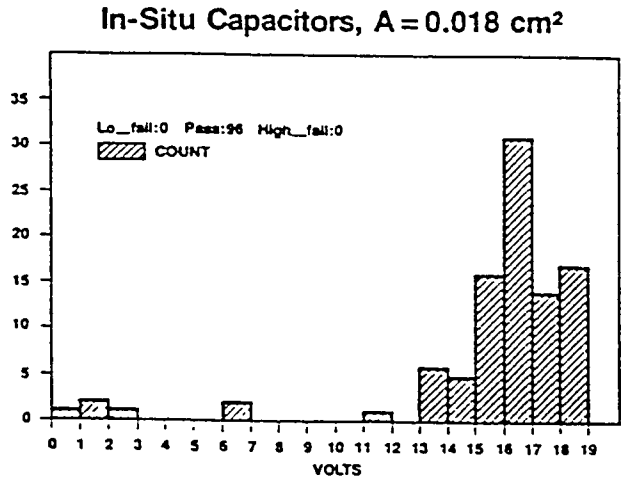
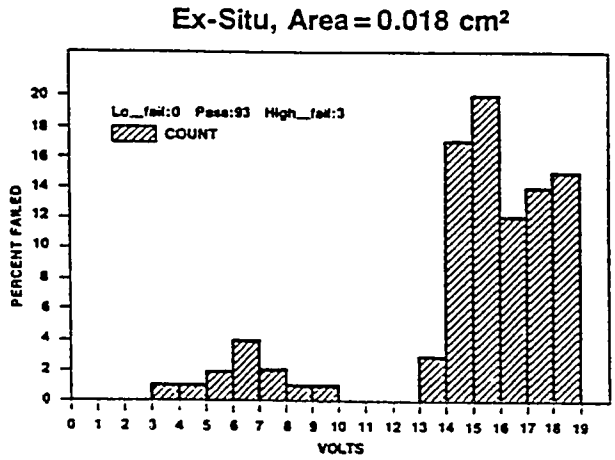


Figure 21 High frequency and quasi-static C-V characteristics of (a) in-situ and (b) ex-situ capacitors after constant current stressing at 0.5 mA/cm^2 for 1000 seconds.

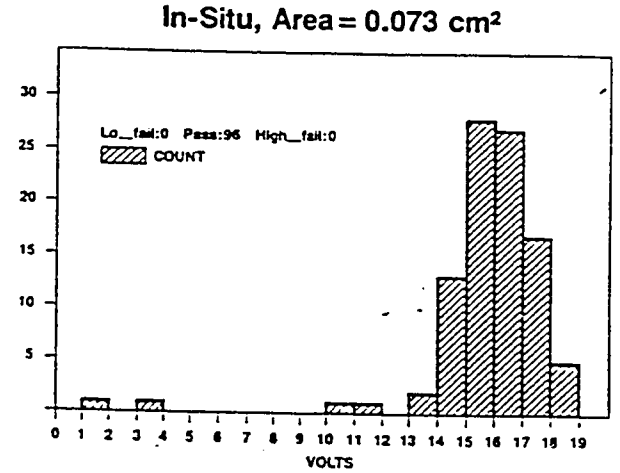


(*a*)

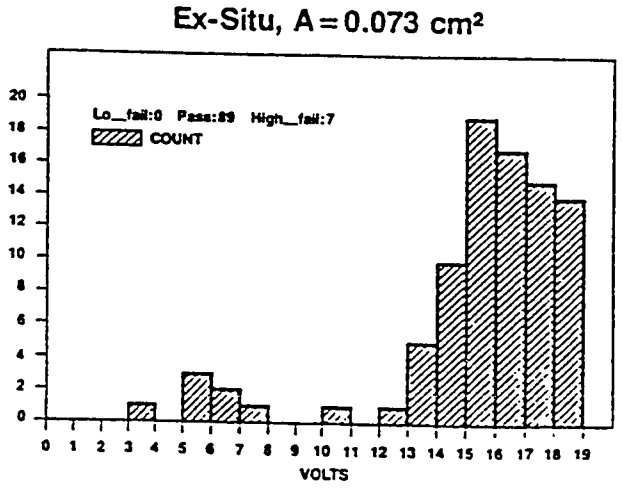


(*b*)

Figure 22 Breakdown voltage distribution of (a) in-situ and (b) ex-situ small area (0.018 cm^2) capacitors. The fail criterion within the graph refers to early failures caused as a result of shorts across the dielectric.



(*a*)



(*b*)

Figure 23 Breakdown voltage histograms of (a) in-situ and (b) ex-situ large area (0.073 cm^2) capacitors.

Chapter 4
DISCUSSION

4.1 Morphology

Although capacitors formed with RTCVD polysilicon behaved no differently than those made with standard LPCVD poly, there was clearly a morphological difference. Using plan-view TEM techniques to evaluate the columnar grains from above, the grain diameter was found to be on the order of 20 nm, small in comparison with typical LPCVD poly grown at the same temperature. Clearly, the lower thermal budget required in rapid thermal processing is instrumental in preventing prolonged grain growth.

As a result, polysilicon films grown using RTP are much smoother and therefore provide more conformal coverage over the topographies used in integrated circuit design.

The lower thermal budget also increases the amorphous to polycrystalline transition temperature. Since there is little time for crystal growth, RTCVD poly films do not crystallize until approximately 700 °C, as compared to LPCVD films which are known to crystallize at 550 °C. The trend in surface roughness observed in figure 8b, which shows the roughness increasing with temperature, then dropping at around 700 °C, then increasing at higher temperatures, has been observed for LPCVD films, except at a lower temperature range. The reversal of increasing roughness with increasing deposition temperature is caused by the phase

change, which occurs at a higher temperature in RTCVD.

The negative side to having smaller grains is the increase in grain boundary area. Grain boundaries are paths for contamination through the film thickness, which can lead to contamination of the dielectric below. Such contamination could take the form of mobile ions, such as sodium, which adversely affect the switching properties of a transistor gate, for example, by contributing unwanted positive charges. Grain boundaries in silicon are also surfaces where oxidation can occur. Silicon oxidation will increase the contact resistivity of a doped polysilicon electrode, interfering with its intended ohmic properties. It will prevent the diffusion of dopants such as phosphorus into the highly resistive intrinsic polysilicon.

The largest drawback of these experiments was the large amounts of oxygen contamination present in the polysilicon films. In experiment 3, in which in-situ RTCVD was compared to ex-situ RTCVD, secondary ion mass spectroscopy (SIMS) was used to profile the oxygen concentration throughout the thickness of the film. The result was compared to conventional LPCVD poly SIMS data. The two plots are shown in figure 24. While typical LPCVD polysilicon has oxygen contamination in concentrations of 10^{19} atoms/cm^3, the RTCVD poly had concentrations which were 2 orders of magnitude greater. In experiment 2, in which a thermocouple-instrumented wafer was used to measure open-loop temperatures during deposition, SIMS was also used to evaluate oxygen concentration in the poly film. Interestingly, the concentration oscillated in inverse proportion to the deposition temperature. When the

temperature was lowest (growing amorphous material), the oxygen concentration [O] was 4 times greater than in material grown during the final stages of film growth. That [O] depends on deposition temperature can be explained by two mechanisms. First, the lower deposition rate at lower temperatures means that a constant rate of oxygen incorporation (from oxygen in the ambient) exists. Second, there is a correlation between deposition temperature, film roughness caused by grain size, and oxygen incorporation.

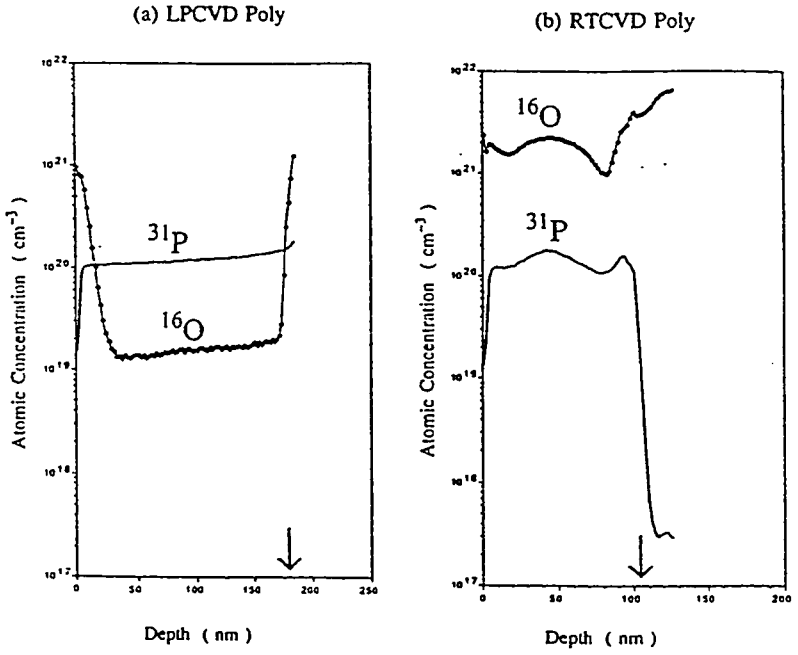


Figure 24 SIMS depth profiles of phosphorus doped polysilicon films deposited in (a) a conventional LPCVD reactor and (b) the RTCVD system. An arrow in each figure indicates the position of the polysilicon-oxide interface. Excessive amounts of oxygen are observed in the RTCVD polysilicon.

4.2 Optical Monitoring

In part 2, wild temperature oscillations on the order of 100 °C were shown to occur during deposition, due to the variation of absorption. It may therefore be a serious problem to control the temperature during an RTCVD process. Furthermore, this revelation may seem to invalidate the deposition kinetics displayed in figure 6.

Neither was found to be the case, although the phenomenon does introduce some noise into the measurement. The difference between the depositions in part 1 and part 2 is that the former was done in closed-loop monitoring mode, while the latter was performed under open-loop conditions of a fixed lamp power. In closed-loop processing, a pyrometer monitors the emitted infrared radiation and adjusts the lamp power to produce the amount of emission from the wafer that it would expect at a given temperature. Therefore, when the temperature drops due to the loss of absorption, the drop is detected by the pyrometer, which drives the control loop to give the lamp more current.

It is true that the emissivity of the wafer surface (amount of infrared radiation emitted at a given temperature) would vary as a film was deposited, thereby rendering the calibration of the pyrometer inaccurate. However, the loss of emissivity is accompanied by a loss of absorptivity in the film, so the lamp is driven to higher currents in closed-loop control.

Figure 25 is a chart of an instrumented thermocouple wafer, identical to the specimens used in part 2 of the study. Again, the open-loop

inert process is used for comparison, in this case, 14% power. Under these conditions, the temperature levels off at approximately 700 °C. Superimposed on this curve is a trace of the temperature profile of a closed-loop RTCVD polysilicon deposition, with a temperature set-point of 700 °C. If no deposition occurred, the curve would look like a trapezoid, similar to figure 4. There is slight variation from this ideal case, caused by the fact that the pyrometer band width is different from the absorption band of silicon, but the variation is on the order of ± 15 °C about the setpoint. Even though this introduces variability in the process, the variation appears to be somewhat symmetrical about the setpoint, and is in any event not as large as the open-loop case.

4.3 In-situ Capacitors

In both experiments of Part 3, the in-situ RTCVD depositions proved superior in terms of breakdown characteristics of processed capacitors. The reason was concluded to be the lack of exposure of the gate oxide to the outside environment. It should be noted that the clean room conditions in which the RTP took place were dirtier than one might find in a state-of-the-art wafer fab, where the improvement would not be as pronounced. However, even the most sophisticated production facilities suffer from airborne particulates. The present trend in semiconductor processing equipment is the cluster tool, which is composed of a central

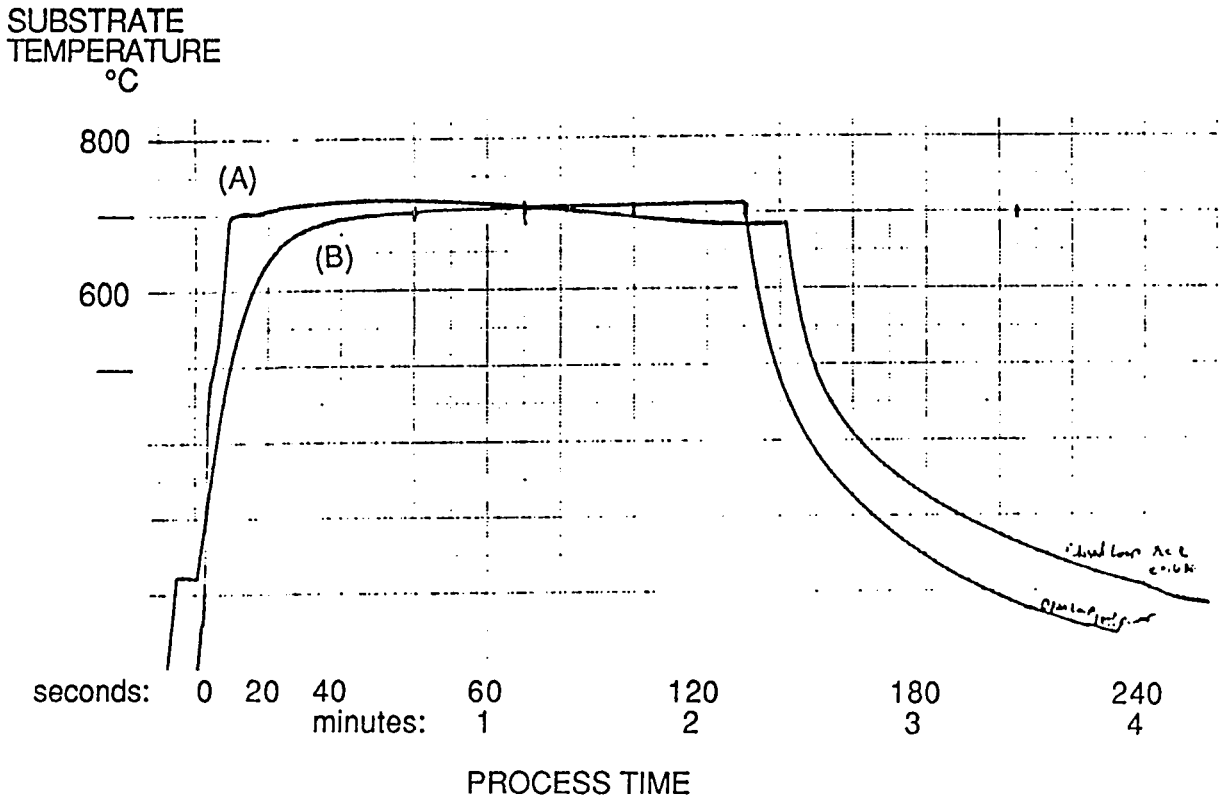


Figure 25 Closed-loop wafer temperature as measured by an embedded thermocouple. The recipe calls for a holding of 700 °C for 150 seconds while silicon is deposited (A). The other curve (B) is a constant lamp power of 4.9 KW with no deposition occurring.

wafer transport surrounded by a number of separate processing chambers, all sealed in an ultra-clean vacuum environment. Performing a number of processes in the same chamber, as was done in this work, is a simpler solution, since it simplifies the equipment requirements and improves the throughput of the process. Care must be taken, however, to insure that the processes are compatible, in that they do not cross-contaminate each other or in any other way degrade the properties of the process or resultant material.

4.4 Equipment Design

Lastly, a word must be said about equipment design to deal with some of the serious process issues. It should be noted that the work described in this study was performed on an existing, commercially available RTP system with minor safety modifications to accomodate silane gas. It was not designed for chemical vapor deposition, and yet, promising results were demonstrated because it was designed for maximum flexibility in process parameters.

For a dedicated RTCVD machine, some design modifications are recommended. First, the gas flow, not usually an issue in RTP processes, must be designed properly. In the current system, the wafer top surface is 1/4" below the quartz window, while 1/2" above the bottom of the chamber. The small gap on top yields a low conductance path for process gases to

flow. Therefore, it would be prudent to provide a wider clearance on the wafer top surface, as well as to perhaps better direct the incoming gas stream by means of nozzles or showerhead apertures. As a design consideration, any additional hardware must be compatible with high intensity visible radiation, corrosive gases, high temperatures, and wafer purity standards.

Placing the wafer farther away from the window also has the advantage of keeping the window cooler. The window is transparent to the intense lamp radiation. However, it absorbs the infrared emitted from the hot wafer. In typically short duration RTP processing, window heating this is not a problem. However, under CVD conditions, a hot window will cause unwanted deposition on it if it reaches a sufficient temperature. In RTP, where the radiation must pass through the window to get to the wafer, deposition on the window would be catastrophic in terms of being able to heat the wafer as well as maintaining any sort of temperature uniformity. Window deposition would compound itself, as the unwanted deposition would absorb lamp radiation and get hotter, allowing for more deposition. Thus, this problem must be addressed by preventing the window from heating up or by cooling the window.

Window deposition is one reason why a thin protective RTCVD polysilicon layer was used on the capacitors, rather than an entire thick layer electrode. Thin polysilicon films cause no problem to the system, because the thermal budget requirements are minimal. However, in order to produce more than 200 nm, high temperatures and/or long deposition

times are required. Both of these variables contribute to window heating. The amount of RTCVD which can be deposited is limited to the time and temperature of the deposition. In a production mode, it will also depend on how long the machine can wait and cool between wafers, as the heating capacity of 1/2" thick quartz is very slow.

The wafer was placed farther from the window by lowering the height of the quartz pins which support the wafer. This simple modification was tried, and showed that good film thickness uniformity can extend to higher temperatures, which are limited by gas transport. However, under extensive testing, deposition was found to occur on the chamber base below the wafer. While not as serious as window deposition, films deposited on the chamber base change the reflectivity of an optical surface, and, therefore, the temperature uniformity of the wafer varies with time. Since IR reflectivity is also affected by the deposition, the effective emissivity (counting rays that are emitted from the wafer, reflected off the chamber base, and reflected into the pyrometer aperture) will change with time, polluting the temperature calibration. Deposition on the chamber also presents a particulate contamination and maintenance problem. It is clear that a compromise distance between window and base must be found. Both distances can be increased by increasing the depth of the chamber. However, the farther the wafer is from the radiation source, the less effective the heating.

Another problem with the process is the preponderance of oxygen incorporated into the films. In Experiment 3 comparing in-situ with

ex-situ RTCVD silicon, the oxygen content of the film was so high that conventional doping techniques using the diffusion of $POCl_3$ did not incorporate enough phosphorus for an adequately conductive electrode. It was necessary to supplement the polysilicon with a layer of titanium, which upon anneal, reacted with the poly to form titanium disilicide.

The problem of oxygen contamination can most adequately be addressed by incorporating better vacuum equipment and a tighter chamber. With the chamber volume being much smaller than a conventional tube furnace, the improvement should be straightforward. Since oxygen was found in high concentrations regardless of whether an RTO step preceded an RTCVD step, the problem is assumed to be in the vacuum integrity of the chamber, and not in the in-situ process itself. With an adequate pump and a chamber designed with no virtual leaks, there should be no problem evacuating the oxygen gas used in the RTO process before the RTCVD process begins.

Finally, a dedicated RTCVD machine would need better temperature control than is found in existing RTP systems, because of the emissivity and absorptivity changes which occur on the wafer during deposition. Several approaches are proposed:

4.5 Suggested Modifications

4.5.1 Prevent Deposition on the Wafer Backside

In the existing system, the pyrometer monitors infrared emissions from the backside of the wafer. The chamber and gas flows could be redesigned to prevent deposition on the wafer backside, thereby allowing the standard temperature measurement scheme using the pyrometer in closed-loop control. One approach to accomplishing this task is to surround the wafer edge with a curf area. Many single-wafer CVD systems on the market place the wafer on a platen in order to prevent backside deposition. Another, less extensive solution is to allow the wafer to rest on a quartz cylinder, centered in the chamber base. The cylinder would be hollow inside (cross section of a straight tube) in order to allow IR radiation from the backside to be piped directly to the pyrometer aperture. The tube would prevent gas flow inside the pyrometer sampling area of the wafer backside. Care must be taken, however, to keep the tube relatively cool, so it does not contribute its own infrared signal.

4.5.2 Closed-loop Recording / Open-loop Playback

In this approach, a recipe which produces polysilicon with desired characteristics is executed on a test wafer. While the recipe is running, a data logger records the lamp power levels used during the recipe. On

subsequent wafers, the lamp power can be replicated, hopefully to yield a repeatable process from wafer to wafer. The advantages of this technique is that it is simple and does not require the pyrometer to make judgements on each wafer. However, the assumption is that the same light intensity history will produce the same result. This is only true if the starting wafer surfaces are identical in all cases. In a typical wafer lot, this is usually the case. Another disadvantage to this technique is that it assumes that all conditions in the chamber are the same from wafer to wafer. If unwanted deposition occurs on any chamber surface, or if the lamp degrades with time, this assumption may prove to undermine the process.

4.5.3 Absorption Model and Feedback

Another approach in temperature control is to model the absorptivity of the material during the deposition, as was done in Experiment 2. Then, a detector which measures the reflectivity of the surface can infer the absorption and therefore the temperature. The disadvantages to this technique are the complexity and accuracy of the model. Depending on the initial surface and the number and type of stacked films, a different model may be needed for each batch of wafer. The refractive indices of various materials, and its temperature dependences are not well understood. Another problem with this approach is that the reflectivity measurement, consisting of a source and a detector, would suffer from noise problems

while the lamp is on and the wafer is hot.

4.5.4 Emissivity-Independent Temperature Measurement

Perhaps the most straightforward approach to monitoring the temperature during RTCVD is to select a method which does not depend on emissivity. For instance, thermocouples are used in tube furnaces. However, a thermocouple suffers from contact problems in an RTP system. Unlike the furnace, which is entirely isothermal, a thermocouple in an RTP system must make good contact with the wafer itself. Not only is this a problem (especially maintaining the same contact from wafer to wafer) in itself, but it is compounded when deposition occurs on the thermocouple. Also, direct contact of metal alloys with the wafer is not desireable as it may result in mobile ion contamination.

Another temperature measurement approach is to measure the expansion of the silicon wafer. Knowing the coefficient of thermal expansion, the temperature can be measured without regards to changes in the emissivity during deposition. The simplest way to measure expansion is to brace the wafer on one edge, and measure the deflection on the opposite edge. The contact can be made with quartz rods, which can adequately transfer the expansion information to the metering instrument. Since silicon is an isotropic crystal, all (100) wafers would have the same thermal expansion regardless of oriented direction.

Chapter 5
SUMMARY

Polycrystalline silicon has been chemical vapor deposited from silane gas onto silicon wafers by thermal decomposition in a rapid thermal processor. The advantages of this process over a standard LPCVD furnace are 1) the small thermal budgets required, 2) single wafer processing for improved process control and reduced batch risk per process, and 3) the ability to modulate the process parameters quickly, so that in-situ processing is possible. RTCVD films were analyzed for their process parameters, morphology, optical properties, and electrical properties.

The thickness of the deposited polysilicon films was measured by UV-visible spectrophotometry to determine the deposition rate at deposition temperatures between 600 and 1100°C. The mechanisms of film formation were identified as surface reaction-limited below 800°C and gas transport-limited above 800°C. The activation energy of the reaction was found to be approximately 1.5 eV.

The structure of the films were analyzed using X-ray diffraction, transmission electron microscopy (TEM), and reflectance spectrophotometry. The preferred grain orientation of the polycrystalline silicon was found to be (100) for films deposited at 700 and 800°C, and (311) for films deposited at 1100°C. It was found by X-ray diffraction that the film is amorphous when deposited below approximately 700°C and polycrystalline at higher temperatures. Both phases of silicon have been formed

sequentially by varying the temperature above and below 700°C during deposition.

The surface properties of the deposited silicon were examined using uv-visible spectrophotometry to measure the surface roughness, which was smoother for films deposited at lower temperatures. The reflectance within this spectrum was also compared to a single crystalline standard to determine the amorphous to crystalline transition temperature. Studying samples deposited at different temperatures, the results were in agreement with the X-ray study.

The absorption of light from the thin film was also analyzed by measuring the temperature of the wafer during deposition with a thermocouple (TC) welded to the wafer. The starting TC wafer had a 100 nm SiO_2 film, which is highly absorbing to the RTP light source. Under a constant lamp intensity, the temperature was found to decrease abruptly as the initial layers of silicon were deposited, and gradually increase as the layer became thicker. Two simple models, a kinetic growth model and a film absorption model were constructed to describe the resultant deposition, as observed by cross-section TEM. Since the absorption characteristics and resultant wafer temperature varied above and below the amorphous to polycrystalline transition temperature, the alternating layers of the two phases could be observed and the thicknesses measured with the TEM micrographs.

Finally, polysilicon-oxide-semiconductor (POS) capacitors were fabricated in-situ by growing a rapid thermal oxide (RTO) on single-crystal

silicon and immediately capping it with rapid thermal CVD polycrystalline silicon (in-situ RTCVD silicon). The electrical properties of these structures were evaluated using capacitance-voltage (C-V) and current stress techniques. The results were compared to capacitors formed by RTO (for the gate oxide) and LPCVD (for the poly electrode), as well as capacitors formed by RTO and ex-situ RTCVD silicon. In both cases, the in-situ POS structure improved the voltage breakdown properties of the capacitor. The voltages were high and the distribution was tighter with less incidence of early failure. The reliability of these capacitors after a second current stress was dramatically improved. This was attributed to the lack of wafer handling in between RTO and CVD, which causes particulate and mobile-ion contamination.

It was demonstrated that rapid thermal processing can be used to form the key processes in an MOS device. By growing a high quality gate oxide and immediately capping it with an in-situ RTCVD polysilicon gate, the integrity of integrated circuit performance can be remarkably enhanced.

Although the experiments were performed on a commercially available RTP system, it was not optimized for CVD processes. Some design changes are proposed in order to improve gas flow, reduce oxygen levels in the poly film, and improve the temperature measurement and monitoring.

Chapter 6

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