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Design and analysis of an ultra low power UHF RFID front-end

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DESIGN AND ANALYSIS OF AN ULTRA LOW POWER UHF RFID FRONT-END

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by

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ABSTRACT

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by Maryam Tabesh

Recently, Ultra High Frequency (UHF) Radio Frequency Identification (RFID) has been coined as the next wave of technology that will revolutionized many industry sectors and applications, such as supply chain management, access control, public transportation, library checkout and airport baggage control.

This thesis describes the design of an ultra low power analog front-end circuitry for UHF passive RFID transponder. The overall circuits include voltage multiplier, voltage regulator, demodulator, power-on-reset, ring oscillator, and matching and backscatter modulator.

This thesis presents a novel charge-pump circuit for improved voltage gain and power efficiency of RFID tags. The charge pump is fully integrable and takes advantage of both passive and active multiplication to reduce the required input power. The minimum required input power for a 1.2V supply voltage in the case of a 50Ω antenna is −20.45dBm. Simulation results using a .13μm Atmel CMOS process shows that the analog front-end consumes only 1.828μW of power.

ACKNOWLEDGEMENTS

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CHAPTER 1. INTRODUCTION

This chapter is about the Radio Frequency Identification (RFID) standards and its applications in the era of automatic identification systems. Section 1.1 introduces the RFID system and describes the block diagram of RFID tag and reader briefly. Section 1.2 discusses the RFID applications. Section 1.3 provides overview of different kinds of RFID tags in term of power supply. Section 1.4 discussed about the available frequency ranges for RFID technology. Finally, section 1.5 gives the overview of main objectives of the thesis.

1.1 Introduction to RFID Systems

Radio frequency identification (RFID) is a term that is often utilized for systems which transmit the ID of a certain object using wireless technology. Previous to RFID systems, barcode technology was widely used for the purpose of identification. However, barcodes fail to provide many strategic advantages and are currently being replaced in many areas. Barcodes are very cheap but their main disadvantage is due to the low capacity and the fact that they cannot be programmed. A feasible solution to the problem of data capacity is putting the data on chips. The ideal case would be the contactless data transfer between the device (product) and the reader. The required power to operate the chip could also be transferred using radio waves. This would lead to the concept of RFID technology.

Some of the advantages of the RFID systems over the barcodes are non-line of sight communication, ability to identify moving elements, large area of coverage and automatic integration with back end solutions which provides end to end integration of data in real time.

The RFID systems are more expensive compare to the barcodes. Also, they are bulkier, due to embedding of electronic components in the tag. Furthermore, the RFID system tags should be designed for specific applications because they are prone to electrical/physical damages due to the environmental conditions [1].

In a general RFID system, the tag generates a signal containing the required information used by the tag reader. This signal is passed to the digital processor section for further processing depending on the specific application [2]. An RFID system is shown in Figure 1.1.

A typical RFID system contains these three main blocks:

- RFID tag or transponder
- RFID reader or transceiver
- Data processing subsystem

The tag consists of the antenna, the wireless transponder circuitry and also the encapsulating material. The RFID tag systems could be active or passive depending on the specific application. The active tags have power supply embedded in them. The passive tags however, have on chip transducers that transform the incoming RF power to the required DC power. The RF power may be transferred by magnetic coupling or far

field electromagnetic radiation. Passive tags tend to be cheaper and have theoretically infinite life time. Their range is lower (typically less than ten meters) and they are more sensitive to regulatory constraints.

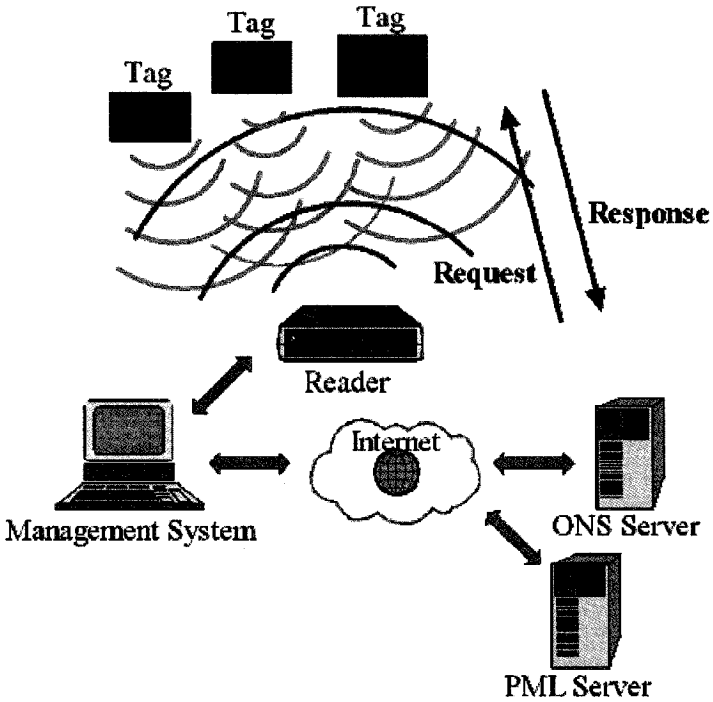


Figure 1.1. The RFID system

An RFID reader (or integrator) consists of an antenna, an RF transceiver and a decoder, which sends periodic signals to inquire about any tag in vicinity. It detects the tags in the working range and identifies their ID signals. This could be used to look for a specific product, create an inventory list or even program the tags.

The data processing subsystem also provides the means of processing and storing the data [2].

1.2 RFID Applications

There are two main areas of applications, defined as short range and long range. Long range applications can be categorized as track and trace applications but RFID technology can provide extra functionality for specific product tracking and even authentication. RFID is a big step towards the automation of data collection process. Companies spend a great deal of time and effort to identify the objects in their inventory. RFID technology can help these companies organize their search with a lot less effort.

RFID helps the companies transfer their data safely. Companies use independent suppliers, data from each of these suppliers are to be carried on tags and then uploaded to the Company's central system securely.

Companies will have a great deal of control over the product throughout the life cycle. Product failures could be detected and better understood through effective tracking. In cases where product recall is necessary because of some unanticipated problem, RFID technology can ease the process significantly.

With this technology becoming more and more popular, there would be better data about the performance of products after they are produced. As an example, a car could have individually tagged parts. The essential date could be collected at the point of accident for processing of the source of failure or even for statistical purposes.

The eventual aim of RFID in retail and manufacturing is eliminating the intermediary. A perfect supply chain would require no distribution center. Products would be delivered directly from the factory to the retail center [2].

RFID systems have been used in hospitals for tracking patient's location and also to provide effective localization of doctors and nurses. Expensive equipment in hospital environments could be tracked using RFID technologies.

RFID chips are used for animals where devices are injected under the animal's skin. Under a government initiative to control rabies, all Portuguese dogs must be RFID tagged by 2007 [3]. The tag contains critical information regarding the dog's history and also the information on the owner of the dog.

The Orlando/Orange County Expressway Authority (OOCEA) is using an RFID based traffic-monitoring system, which uses roadside RFID readers to collect signals from transponders that are set up in almost 1 million E-Pass and SunPass customer vehicles [3].

Different RFID applications are shown in Figure 1.2. It shows that RFID applications are increasing in different areas.

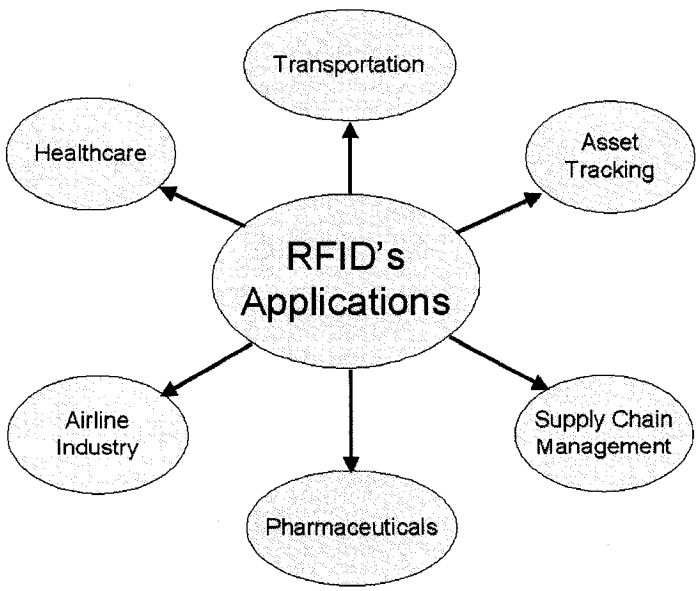


Figure 1.2. RFID application chart

1.3 Active and Passive RFID

As it was briefly described in the previous section RFID tags are categorized into three main types: Passive, Semi-Passive and Active. Passive RFID tags have no internal power supply in the chip. Energy is transferred through radio waves and is then rectified on the chip once it is absorbed by the antenna or the coupling medium. The tag circuitry must consume as little energy as possible in order for the power transfer to be feasible. Most passive tags use backscatter as method of communicating with the reader. The antenna is designed to be able to work in two modes, one where power is absorbed and the other in which it is reflected. Through the change of the reflection coefficient of the antenna, the tag communicates with the reader. The response of a passive RFID tag is not just an ID number (GUID): tag chip can contain nonvolatile EEPROM (Electrically Erasable Programmable Read-Only Memory) for storing data [4].

Semi-passive RFID tags have an additional small battery. This battery allows the tag IC to be constantly powered. The small battery removes the need for power recovery circuits that are employed in passive tags. In this case the antenna could be optimized for backscatter operation. Semi-passive tags operate in longer distance scenarios and are faster to respond, however their life time is limited and also they cost more.

Unlike passive and semi-passive RFID tags, active RFID tags (also known as beacons), have their own internal power source which is used to power any ICs and generate the outgoing signal. They are often called beacons because they broadcast their own signal instead of using backscatter modulation for their communication. Active tags have longer range as well as being able to send information independently. They have a

better data processing power and generally contain larger memory arrays. Many active tags have practical ranges of tens of meters, and a battery life of up to 10 years [4]. Passive, active, and semi-passive RFID systems are shown in Figure 1.3.

The choice of active versus passive tags has consequences for overall system cost, initial tag cost, tag life and battery life.

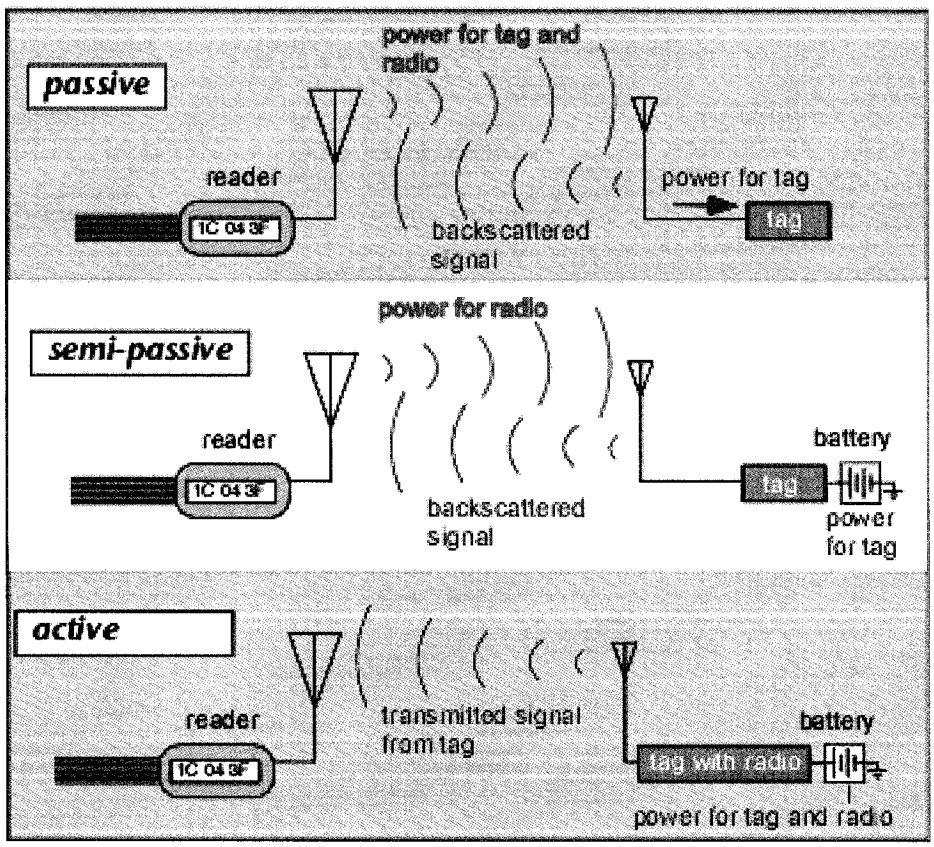


Figure 1.3. Passive, active, and semi-passive RFID systems
(Courtesy of Dr. Daniel Dobkin, Enigmatics, Sunnyvale, CA)

In comparison, passive tags have a lower cost due to low-cost tags and long tag life. They are also easier to mount and install on packages and products. The passive tags

have indefinite lifespan as they do not operate on batteries. The choice between active tags and passive tags is related to other system design issues. Active tags support higher data rates and can have larger memories, but passive tags also support acceptable bit rate and data handling capabilities required by many applications. Active tags can send data at any instance of time that they need to and this provides them with a great deal of flexibility. One disadvantage of passive RFID tags is the fact that some countries do not permit enough radiation power and also suitable frequency bands for the support of these tags [3].

Active tags generally cost more and a part of this is due to the cost of battery and its connection. Battery life causes reliability issues for the tags and this will raise the overall cost. An overall view of tag cost must definitely take into account the whole tag or in some other cases the battery replacement costs [5]. A comparison between active and passive RFID tags is illustrated in Table 1.1.

1.4 RFID Frequency Range

RFID tags fall into many different sub-categories based on their operating frequency, coupling method and the expected range of the system. RFID systems operate in the frequency range of 135kHz to 5.8GHz. Electric, magnetic and electromagnetic fields are used for the physical coupling. The range of the system varies from a few millimeters to above 15m depending on various parameters [6].

Table 1.1. Characterization of passive and active RFID tags

	Active RFID	Passive RFID
Tag power source	Internal to tag	Energy transferred from the reader via RF
Tag battery	Yes	No
Availability of tag power	Continuous	Only within field of reader
Required signal strength from reader to tag	Low	High
Available signal strength from tag to reader	High	Low
Communication range	Long range (100m)	Short range (up to 15m)
Data storage	Large read/write data storage	Small read/write data storage

Systems that achieve a small range (less than 1cm) are generally known as close coupling systems. These systems require the tag to be inserted into the reader or to be brought to close proximity of it. Close coupling systems generally operates in frequencies between DC and 30MHz and are coupled using electric and magnetic fields (capacitive and inductive coupling).

RFID Systems that have ranges close to one meter are known as remotely coupled systems. Most of remotely coupled devices operate based on magnetic (inductive) coupling mechanisms. Usual frequencies for these systems are from 135kHz to 13.56MHz.

RFID systems with ranges above 1m are known as long-range systems. Nearly all of these RFID systems work using electromagnetic far-field radiation of waves in the UHF and microwave range. A great percentage of these systems are widely known as backscatter systems. Most of these tags are operating in the UHF bands (868MHz in Europe and 915MHz in USA) and at lower microwave frequencies of 2.4GHz and 5.8GHz. Inductive coupling and backscatter systems are shown in Figure 1.4.

System level constraints and applications dictate the use of specific tag systems. For example, the UHF RFID tags are generally utilized for long range or high data rate applications. The frequency ranges and their applications are listed in Table 1.2 [1].

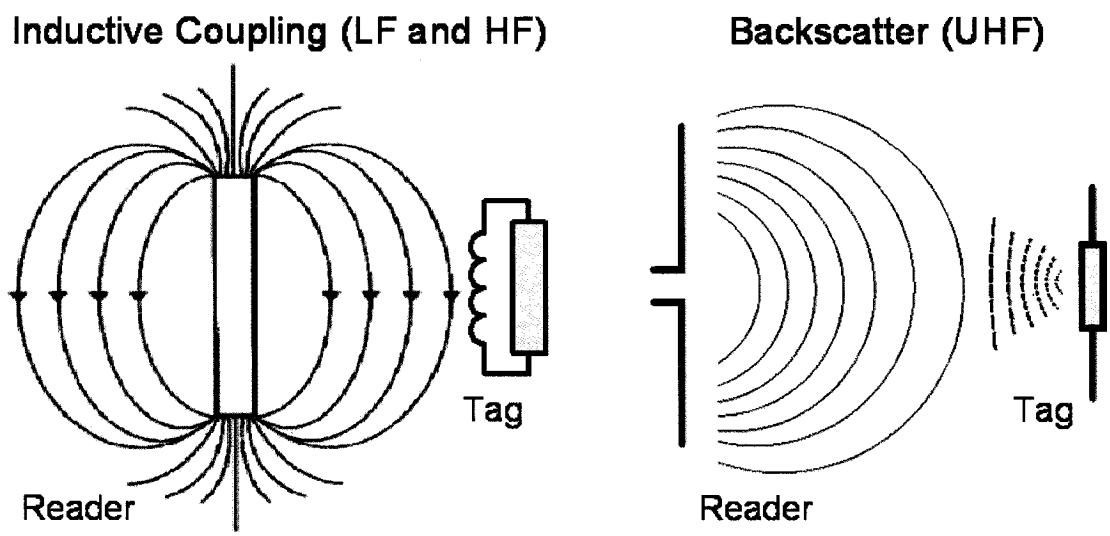


Figure 1.4. Inductive coupling and backscatter RFID systems

Table 1.2. Different RFID frequency ranges and their applications

Frequency range	Description	Typical applications
<135KHz	Low Frequency, Inductive coupling	Access Control & Security Widgets identification through manufacturing processes Ranch animal identification OEM applications
13.56 MHz	High Frequency, Inductive coupling	Access Control Library books Laundry identification OEM applications
868 to 870 MHz 902 to 928 MHz	Ultra High Frequencies (UHF), Backscatter coupling	Supply chain tracking
2.400 to 5.8 GHz	SHF, Backscatter coupling	Asset tracking Highway toll tags Vehicle tracking

1.5 Objectives

This thesis mainly focused on the UHF RFID front-end for long range applications. The main challenges in the passive RFID tags are supply voltage generation and power efficiency. So, most parts of the circuit operate in subthreshold to operate in low power regime. The 2.4GHz frequency is chosen for this project to achieve high data rate and small antenna size.

Chapter 2 of the thesis talks about the RFID transponder architecture and explains the RFID transponder fundamentals and its important specifications. Chapter 3 illustrates the

RFID tag's front-end schematic design and simulation results. Chapter 4 starts with the layout issues and discusses the inductor design analysis and post-layout simulation results achieved using Atmel .13μm CMOS technology. Chapter 5 concludes the thesis and summarizes the results.

CHAPTER 2. RFID TRANSPONDER ARCHITECTURE

The block diagram of an RFID system is shown in Figure 2.1. In this chapter a brief description of each block is presented. Section 2.1 is about the antenna part. Section 2.2 discussed about the V_{DD} generator block. Section 2.3 leads to the detail description of the demodulator part. The modulator and matching blocks are described in section 2.4. Section 2.5 discusses about the clock and power-on-reset generator and finally an overview of the digital part is provided in section 2.6.

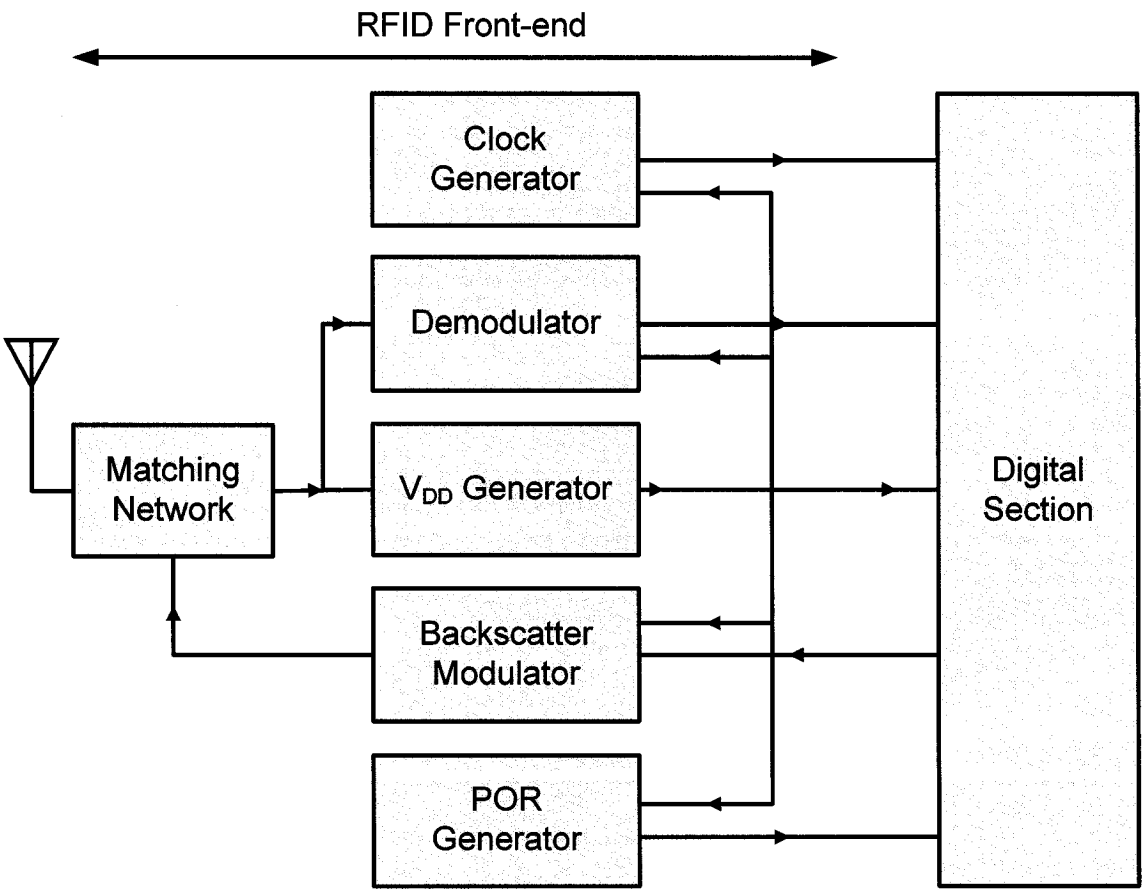


Figure 2.1. Block diagram of RFID transponder

2.1 Antenna

As discussed in chapter one, depending on the application and the frequency of operation, the tag antenna can either operate in the near-field (coupling) or far-field regions. In near-field operation the tag usually communicates using inductive coupling mechanism. In the far-field operation, electromagnetic radiation of radio-frequency waves transmits the required data and energy between the tag and the antenna.

In high frequency RFID systems, the far-field antennas have been used. The block diagram of such systems is shown in Figure 2.2. One of the most important characteristics of RFID systems is their operation range and this is greatly affected by the antenna design. The read range is also sensitive to the specific tag orientation, the material that the tag is placed on, and to the propagation environment between the tag and the reader [7]. The read range can be calculated using Friis free-space formula as

$$R = \frac{\lambda}{4\pi}\sqrt{\frac{P_t G_t G_r \tau}{P_{th}}} \qquad \text{(Eq. 2.1)}$$

Where λ is the wavelength, P_t is the power transmitted by the reader, G_t is the gain of the transmitting antenna, G_r is the gain of the receiving antenna, P_{th} is the minimum threshold power necessary to provide enough power to the RFID tag chip, and τ is the power transmission coefficient given by [7]

$$\tau = \frac{4R_{chip}R_{ant}}{\left|Z_{chip} + Z_{ant}\right|^2} \qquad \text{(Eq. 2.2)}$$

Where $Z_{chip}=R_{chip}+jX_{chip}$ is chip impedance and $Z_{ant}=R_{ant}+jX_{ant}$ is antenna impedance.

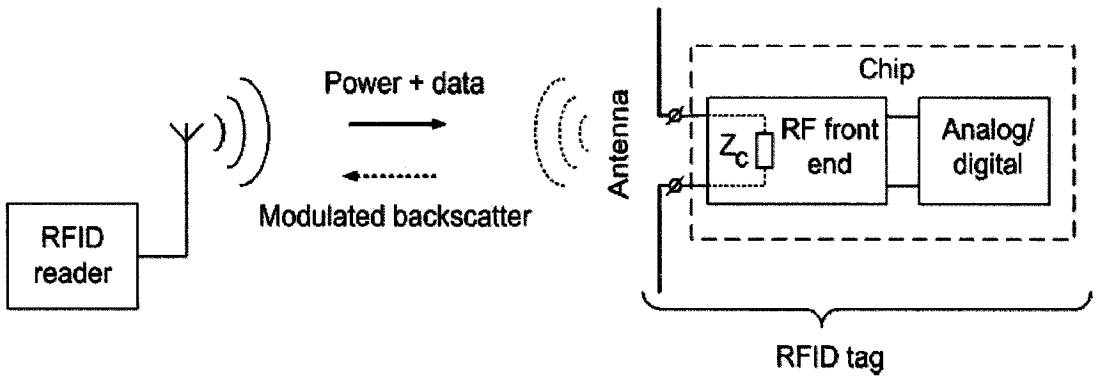


Figure 2.2. Block diagram of a far-field RFID system
(Courtesy of Dr.Seshagiri Rao from paper "Antenna Design for UHF RFID Tags: A Review and a Practical Applications," *IEEE Transactions on Antennas and Propagation.* © IEEE 2005. Reprinted with permission)

Qualitative behavior of antenna impedance, chip impedance, and read range for a typical RFID tag is illustrated in Figure 2.3 as a function of frequency [7]. A tag range bandwidth can be defined as being the frequency bandwidth over which the tag sustains an acceptable minimum range.

In general the range of an RFID system is mostly determined by the τ and its dependency on frequency. The best achievable range occurs in the case where the antenna is matched to the input impedance of the chip. Contours of constant range are plotted on gain-transmission coefficient plane as a function of their normalized value to R_0 in Figure 2.4 [7]. R_0 is the maximum range when the antenna impedance is totally matched to the chip impedance.

The RFID tag antenna design process involves inevitable tradeoffs between antenna gain, impedance, and bandwidth as well cost issues with the size of the antenna and the substrate being used.

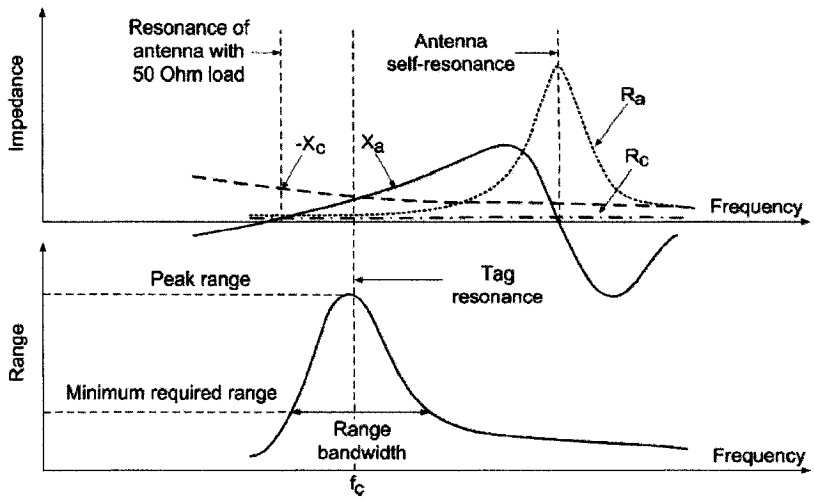


Figure 2.3. Antenna impedance, chip impedance, and range as a function of frequency for a typical RFID tag
(Courtesy of Dr.Seshagiri Rao from paper "Antenna Design for UHF RFID Tags: A Review and a Practical Applications," *IEEE Transactions on Antennas and Propagation.* © IEEE 2005. Reprinted with permission)

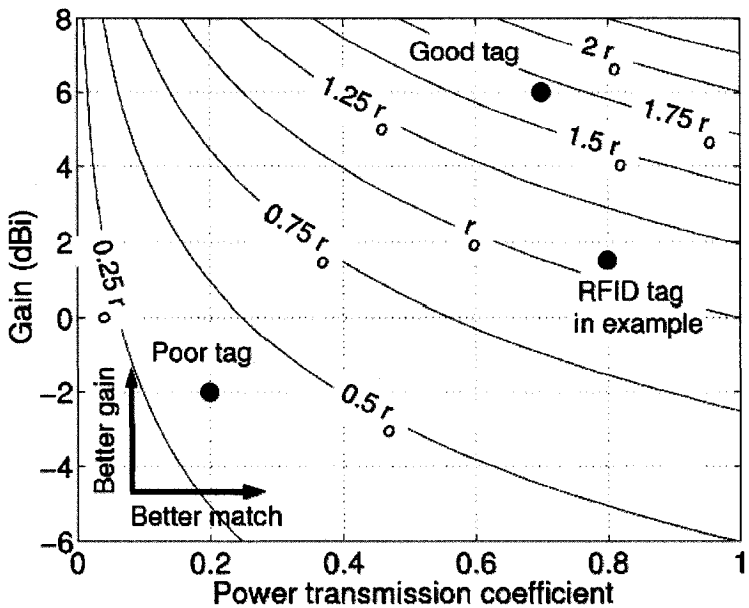


Figure 2.4. Contours of constant range on gain-transmission coefficient plane as a function of their normalized value to R_0
(Courtesy of Dr.Seshagiri Rao from paper "Antenna Design for UHF RFID Tags: A Review and a Practical Applications," *IEEE Transactions on Antennas and Propagation.* © IEEE 2005. Reprinted with permission)

There are various types of antennas that can be used for RFID applications. The most popular one is the well known dipole antenna. The radiation resistance of a short electric dipole of length l, which operates at a specific frequency for which the free space propagation constant has magnitude β, is given by (under the assumption that the current distribution of the antenna is uniform and equal to the feed point current)

$$R_r = 20(\beta l)^2 \quad \Omega \qquad \text{(Eq.2.3)}$$

The other types of antenna are loop antennas. Also, sometimes for decreasing the size of the antenna some fractal patterns may be used that employ self-similar structures.

In general low frequency passive tags use an induced voltage for their operation. Figure 2.5 shows a simple geometry of an RFID inductive system. As described in the figure, in close proximity operation of the tag and the reader, the time varying magnetic field strength induces a voltage on the tag coil. The induced voltage is given by

$$V_{induced} = -N\frac{d\psi}{dt} \qquad \text{(Eq. 2.4)}$$

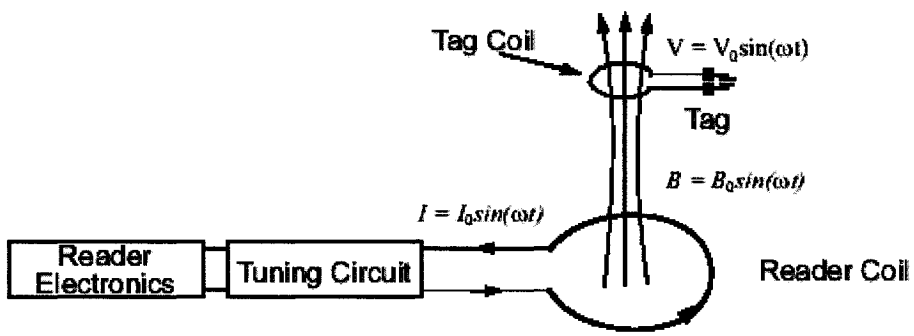


Figure 2.5. Block diagram of a near-field RFID system
(Courtesy of Microchip Technology Inc., Chandler, AZ)

Where

$$\psi = \int B.dS \qquad \text{(Eq.2.5)}$$

Where S is the surface area of the coil and N is the number of turns in the coil.

To operate with maximum induced voltage, the two coils should be placed in parallel so that the flux coupling is optimized. This condition will result in the maximization of the coupled voltage and from there the read range of the tag.

From the equation (2.4) and by substituting the magnetic field formula, the induced voltage in tags coil can be as follows [8]

$$V_{induced} = -N_{tag}\frac{d\psi}{dt} = -N_{tag}\frac{d}{dt}(\int B.dS) = -\left[\frac{\mu_0 N_{tag} N_{reader} a^2(\pi b^2)}{2(a^2+r^2)^{3/2}}\right]\frac{di_{reader}}{dt} = -M\frac{di_{reader}}{dt} \qquad \text{(Eq.2.6)}$$

Where "a" is the radius of the reader coil, "b" is the radius of tag coil, r is the distance between the two coil and M is the mutual inductance between the tag and reader coil.

The above equation shows that the tag coil voltage is largely dependent on the mutual inductance between the two coils. Mutual inductance is a function of tag position and the distance between the coils. The induced voltage in the tag coil decreases with r^{-3}. Therefore, the read range also decreases in the same way.

2.2 V_{DD} Generator

The V_{DD} generator block diagram is shown in Figure 2.6. The blocks in the V_{DD} generator are RF-clamp circuit (RF-limiter), voltage multiplier (rectifier), DC-limiter, and regulator.

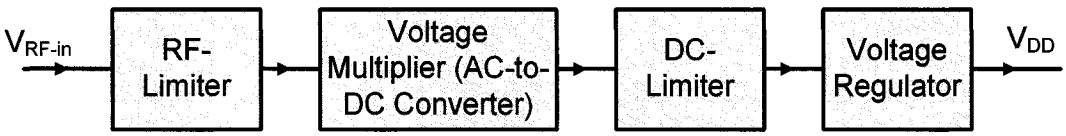


Figure 2.6. Block diagram of V_{DD} generator

2.2.1 RF-Limiter

The voltage at the input of the voltage multiplier can change from 350mV to 20V, depending on the vicinity of the reader to tag. To prevent any damage to the chip transistors in high voltage levels, an RF-limiter is used to ensure that under large RF power levels the voltage swing at the chip input is limited to a fixed value. The RF-limiter acts like a bypass system for the extra current during the large input power.

2.2.2 Voltage Multiplier

The voltage multiplier converts a part of the incoming RF signal power to DC for power supply for all active circuits on the chip. One of the most popular voltage multipliers are charge pump circuits. Charge pumps are circuits that generate a voltage larger than the supply voltage from which they operate. To see how they work, we consider the simple circuit in Figure 2.7.a that consist a single capacitor and three switches [9].

During clock phase ϕ, switches S_1 and S_3 are closed and capacitor is charged to the supply voltage, V_{DD}. Next, during the $\bar{\phi}$ switch S_2 is closed and the bottom plate of the capacitor assumes a potential V_{DD}, while the capacitor maintains its charge of $Q=V_{DD}.C$ from the previous phase. This means that based on charge conservation we will have

$$(V_{out} - V_{DD})C = V_{DD}C \qquad \text{(Eq.2.7)}$$

or

$$V_{out} = 2V_{DD} \qquad \text{(Eq. 2.8)}$$

Thus, in the absence of a DC load, an output voltage has been generated that is twice the supply voltage.

In order to accommodate a load at the output, the circuit would be modified by adding an output capacitance as shown in Figure 2.7.b.

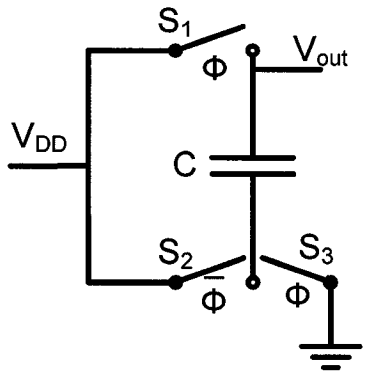
In this case, the ideal output voltage is given by

$$V_{out} = \frac{C}{C + C_{out}} 2V_{DD} \qquad \text{(Eq.2.9)}$$

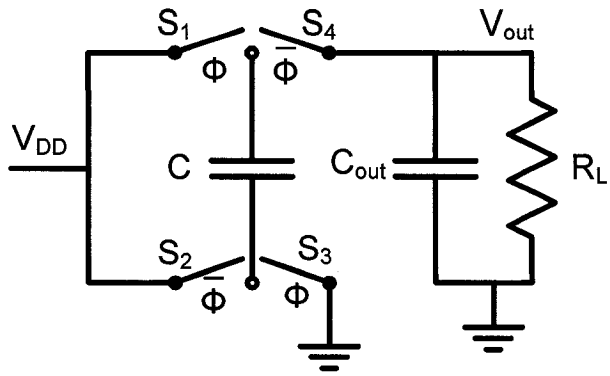
If a load R_L is presented, then a ripple voltage, V_R, is generated at the output. The ripple voltage can be reduced by making C_{out} sufficiently large so that V_R is negligible compared to V_{out}. Voltage multiplication greater than twice the supply voltage can be achieved by cascading more than one capacitor in series.

The switches in the Figure 2.7 can be implemented by diodes that characterized by their forward bias voltage V_D. This multiplier is called Dickson rectifier. Figure 2.8 shows a six-stage Dickson charge pump circuit using for RFID applications. The multiplier operates by pumping charge along the diode chain as the capacitors are successively charged and discharged during each period of the input RF signal.

A single stage charge pump circuit is shown in Figure 2.9. When the input signal of a single stage voltage multiplier is in the negative cycles, the voltage V_{c1} across capacitor C_1 is charged through D_1 diode to the peak of the input signal. In the positive cycles, D_1



(a)



(b)

Figure 2.7. Simple circuit of voltage multiplier (a) without loading (b) with loading

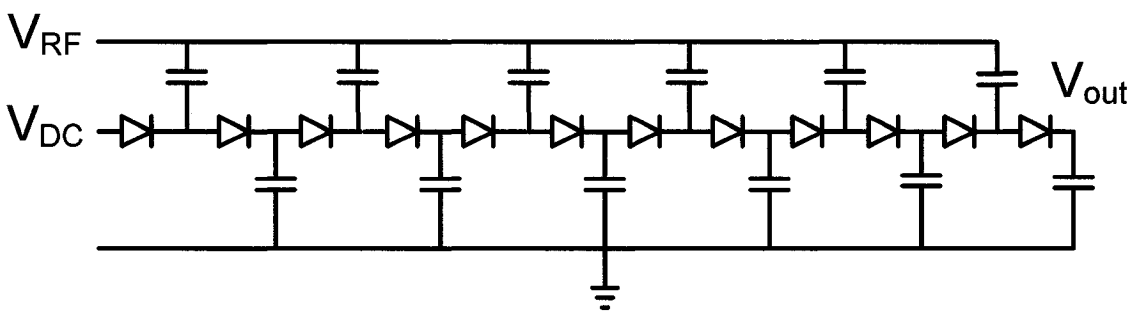


Figure 2.8. A 6-stage charge pump voltage multiplier

is OFF and D_2 rectifies the voltage sum of the V_{c1} and V_{in} and produces a DC voltage (V_1) equal to twice the peak of the input signal (V_p) minus the ON voltage drop (V_D) across the two diodes. The output voltage provided by the single stage voltage multiplier can be expressed by

$$V_{1-Stage} = 2(V_P - V_D) \qquad \text{(Eq. 2.10)}$$

The operations of the n^{th} stage of the voltage multiplier in negative and positive cycles of input RF signal are shown in Figure 2.10.

In the negative cycles, the first diode ($D_{1,n}$) becomes ON and charges the capacitor $C_{1,n}$ to

$$V_{C1,n} = -(V_P - V_{D1,n} + V_{n-1}) \qquad \text{(Eq.2.11)}$$

Where V_{n-1} is the output voltage from the $(n-1)^{th}$ stage.

In the positive cycles, the second diode ($D_{2,n}$) becomes ON and rectifies the voltage seen from capacitor $C_{1,n}$ to

$$V_n = V_p - (V_{C1,n}) - V_{D2,n} = 2(V_p - V_D) + V_{n-1} \qquad \text{(Eq. 2.12)}$$

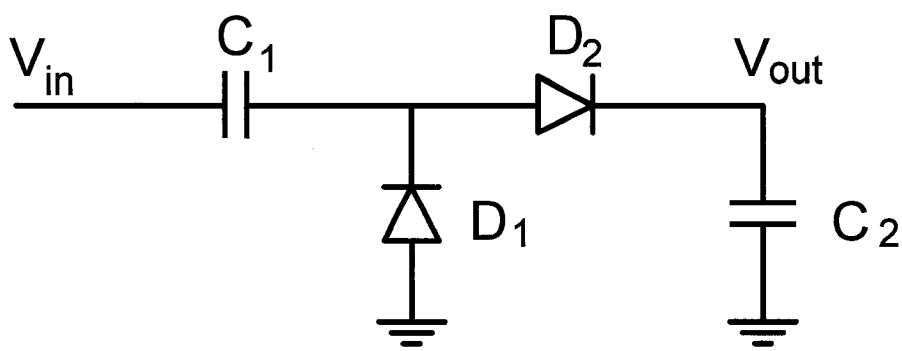
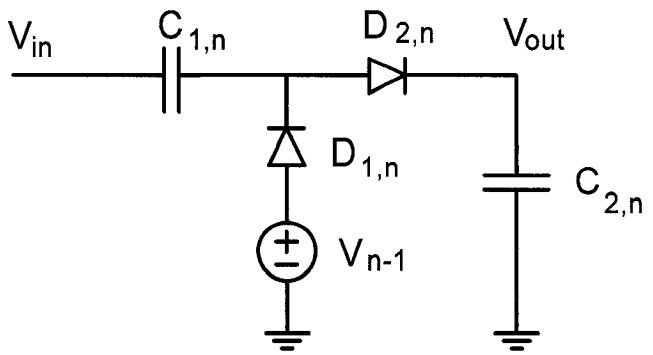
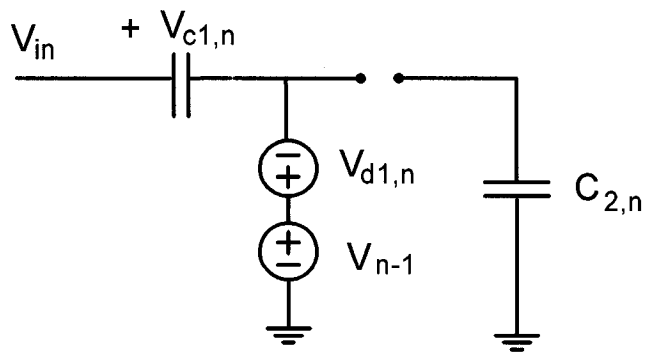


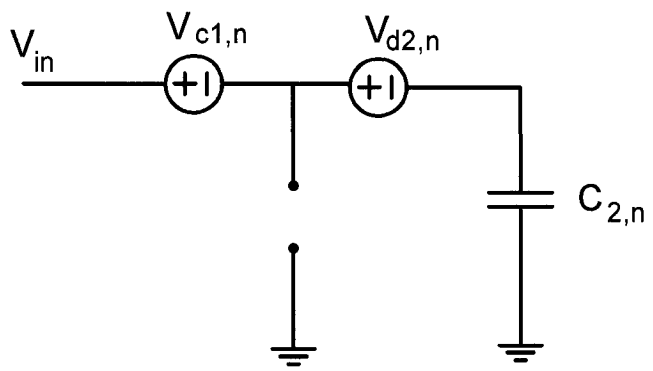
Figure 2.9. A single stage voltage multiplier



(a)



(b)



(c)

Figure 2.10. The n^{th} stage of the voltage multiplier (a) general topology (b) In negative cycles of the input voltage (c) In positive cycles of the input voltage

Considering the input of the first stage is only an RF signal and by replacing V_{n-1} recursively, the following formula for an n-stage voltage multiplier can be extracted

$$V_n = 2n(V_{in} - V_D) \qquad \text{(Eq. 2.13)}$$

2.2.3 DC-Limiter

The output voltage of the voltage multiplier depends on the RF input voltage so varies in a wide range. To limit the range of the changes in the output of the charge pump, a DC limiter is used. During the low power input, the limiter does not change the output of the voltage multiplier. In the high RF energy periods, the limiter makes a bypass path for current and limits the output voltage to a certain value. The limiter bounds the rectifier output voltage variation to 1V.

2.2.4 Regulator

The regulator circuit comes after the DC limiter. The regulator does two major functions. One is to regulate the front-end output voltage to a preferred value and within a preferred range. The other is to protect the inner circuits from breaking at high RF input power. The output of the voltage regulator will be used as the circuit's V_{DD} voltage.

2.3 Demodulator

There are different modulation schemes for sending data to an RFID transponder such as ASK, PSK, PWM or OOK. ASK involves the simplest form of RF detection, using a

basic envelope detector, implemented by a diode-capacitor network. An ASK demodulator demodulates information in the form of amplitude changes or "dips." The demodulator is actually an edge detector. PSK is not usually used in an RFID system's forward link because PSK demodulation employs superheterodyne detection, which calls for a local-oscillator (LO), mixer and filter circuits. Such circuits are complex and require large die area. OOK (ON_OFF_Keying) is the simplest digital modulation where the amplitude of the carrier corresponds to one of two digital states. Nonzero amplitude represents a digital one while zero amplitude is a digital zero. OOK has the advantage of simplicity and low cost but it looses the power up signal for the whole symbol period. The PWM (Pulse Width Modulation) is an OOK signal with different duty cycles for digital signal "zero" and "one" and cause not loosing the power during the whole "zero" signal so it is more power efficient than the OOK modulation.

In this project, a PWM signal which is modulated with ASK is used for forward link.

2.3.1 PWM Signal

Pulse-width modulation (PWM) of a signal involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load. Three different types of pulse-width modulation (PWM) are possible. In the first method the center of the pulse may be chosen to be fixed to the center of the time window. In this method both edges of the pulse move to change the width of the pulse. In the second method, the leading edge of the pulse is held tied to the

leading edge of the pulse and the tail edge is modulated for pulse with variations. In the third method the tail edge is fixed and the lead edge is modulated.

The block diagram and waveform of a system that generates PWM signal is shown in Figure 2.11. The system employs a comparator and a sawtooth-wave generator. The output of the comparator is zero except when the message waveform exceeds the sawtooth wave, in which case the output is a positive constant.

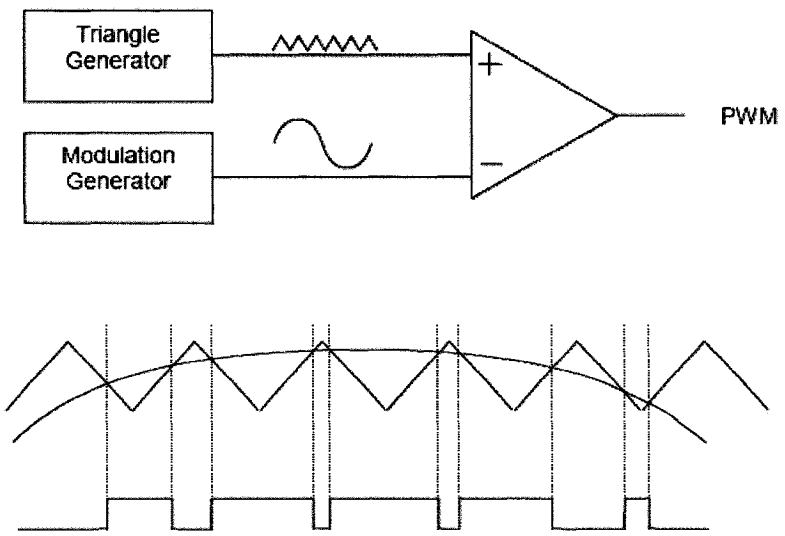


Figure 2.11. Block diagram and waveform of PWM generator

2.3.2 Demodulator Block Diagram

Figure 2.12 demonstrates the block diagram of the demodulator section. The transponder uses an envelope detector and a pulse width demodulator for demodulation. The input carrier waveform is passed through a rectifier and an envelope detector to extract the envelope of the signal. To filter out the ripple on this signal, usually a low-pass filter is employed. The current sink after the envelope detector together with the

lowpass filter capacitor determine the minimum width of gaps that can be detected by the circuit. The signal is then fed to a hysteresis comparator to generate the input to the integrator. The integrator integrates the signal to distinguish between the zero and one signals. The signal will be compared with a reference voltage and this procedure determines the data bits.

Two factors must be considered during edge-detection design: the hysteresis level of the comparator, and comparator sensitivity. The RFID reader determines the lowpass filter parameters during the tagging of the data rate, coding, and the envelope mask. The filter bandwidth should be smaller than the signal bandwidth. Specifications for the data envelope are described in the RFID air interface protocol.

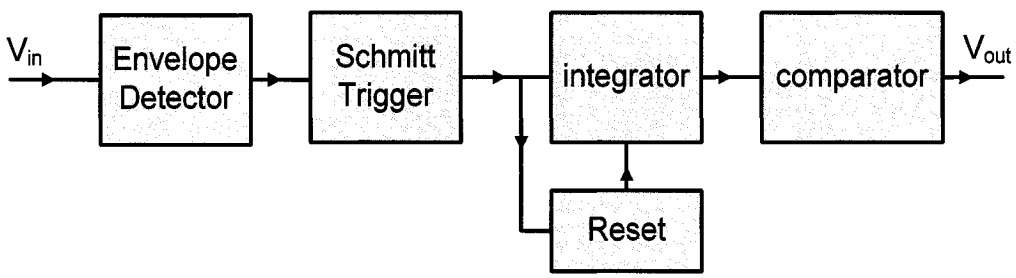


Figure 2.12. Block diagram of demodulator section

2.4 Modulator

The modulation in RFID systems is based on backscattering. Backscatter enables the tag to reader communication by varying the impedance presented to the transponder's antenna in order to modulate the reflected power.

The backscatter modulation can be phase or amplitude modulation (PSK or ASK). These modulation types are different in term of available power to the IC and the backscatter power. In the next section we will show these parameters and the tradeoffs for both modulation schemes.

2.4.1 Power Efficiency and Backscatter Modulated Power

The backscatter modulation is achieved by changing the input impedance between two different states: $Z_1=R_1+X_1j$ and $Z_2=R_2+X_2j$. Two important things that need to be taken into account for choosing the modulation scheme are power efficiency and backscatter modulated power. Power efficiency is shown by the RF power available for DC supply power generation. Backscatter modulation power is the power of signal obtained from the demodulation of the voltage directly applied to the radiation resistance of the antenna [10].

The input power available to the rectifier for DC voltage generation is given by [11]

$$P_{RF,in,1,2}=\frac{1}{2}\mathrm{Re}(v^{*}_{in}.i_{in})=\frac{1}{2}\mathrm{Re}(\frac{v_0{}^2(R_{1,2}-jX_{1,2})}{\left|R_{1,2}+R_{ant}+j(X_{1,2}+X_{ant})\right|^2})=\frac{v_0{}^2}{8R_{ant}}(1-\left|\frac{Z_{1,2}-Z_{ant}{}^*}{Z_{1,2}+Z^*{}_{ant}}\right|^2) \quad \text{(Eq. 2.14)}$$

Where v_{in} is the peak voltage at the IC's input, i_{in} is the peak current flowing between antenna and IC and v_0 is the peak source voltage that would be observed if the antenna where not loaded by the IC.

The available power from the antenna and the reflection coefficient from the antenna have the following equations

$$P_{avail} = \frac{v_0^{\,2}}{8R_{ant}} \qquad \text{(Eq.2.15)}$$

$$\Gamma_{1,2} = \frac{Z_{1,2} - Z_{ant}^{\,*}}{Z_{1,2} + Z_{ant}^{\,*}} \qquad \text{(Eq. 2.16)}$$

So by using equations (2.15) and (2.16) in equation (2.14), the input RF power would simplify as

$$P_{RF,in,1,2} = P_{avail}(1 - |\Gamma_{1,2}|^2) \qquad \text{(Eq. 2.17)}$$

Because of the need for two different impedances, the input RF power could have different amount and the average input power becomes important. If the IC is in state 1 and 2 for a fraction of p_1 and p_2 of the time, the average input power available for the power supply is [11]

$$P_{RF,in} = p_1 P_{RF,in,1} + p_2 P_{RF,in,2} = P_{avail}[p_1(1 - |\Gamma_1|^2) + p_2(1 - |\Gamma_2|^2)] \qquad \text{(Eq. 2.18)}$$

To find the modulation backscatter power, we will assume that both states are active an equal amount of time. The modulation backscatter power is found to be [10]

$$P_{bs} = \frac{(V_{bs1} - V_{bs2})^2}{8R_{rad}} = \frac{|i_2 - i_1|^2}{8} R_{rad} \qquad \text{(Eq.2.19)}$$

Where $i_{1,2}$ are the complex amplitude of the current flowing between antenna and IC for two states 1 and 2 and R_{rad} is the radiation resistance of the antenna.

The current flowing between antenna and IC can be obtained by following equation

$$i_{1,2} = \frac{v_0}{Z_{ant} + Z_{1,2}} = \frac{v_0}{2R_{ant}}(1 - \Gamma_{1,2}) \qquad \text{(Eq.2.20)}$$

By assuming that the antenna is lossless ($R_{ant}=R_{rad}$) and using equation (2.20), the equation (2.19) can be expressed in term of reflection coefficients [11]

$$P_{bs} = \frac{P_{avail}}{4}\left|\Gamma_1 - \Gamma_2\right|^2 \qquad \text{(Eq.2.21)}$$

Equation (2.21) shows the total power of the two sidebands of the backscatter wave, excluding the carrier power.

2.4.2 Different Types of Backscatter Modulation

There are two types of backscatter modulation: amplitude and phase shift keying. The first one modulates the signal by changing the real part of the IC impedance. In the PSK the signal would be modulated by changing the imaginary part of the input impedance. The advantages and disadvantages of each modulation scheme will be discussed in this section.

2.4.2.1 ASK

There are two different ASK backscatter modulation. At one of them the power will be matched in one of the two states and in the other state the power reflects totally. The other ASK modulation scheme has an equal amount of mismatch in both states.

When we have total reflection in one of the states, the input is shorted or opened so the input impedance is zero or infinity ($Z_1=0$ or $Z_1=\infty$). By using equation (2.20), $|\Gamma_1|=1$. As the antenna is matched in the other state, the reflection coefficient of state 2 is zero ($|\Gamma_2|=0$).

By equations (2.18) and (2.21) and also assuming equal amount of activation time for both states, the RF input power and backscatter power are [11]

$$P_{RF,in,ask,on\_off} = p_1 P_{avail} \quad \text{(Eq. 2.22)}$$

And

$$P_{bs,ask,on\_off} = \frac{P_{avail}}{4} \quad \text{(Eq.2.23)}$$

From the above equations, it is obvious that 50% of the available power is available for rectification, 25% is used as backscattered modulated power and the remaining 25% is wasted.

In the ASK with the same amount of power mismatch, the reflection coefficient in both states are real and given by

$$\Gamma_{1,2} = \frac{R_{1,2} - R_{ant}}{R_{1,2} + R_{ant}} \quad \text{(Eq. 2.24)}$$

To have equal mismatch in both states, it is sufficient to choose $R_2=R^2_{ant}/R_1$ [10]. In this case $\Gamma_1=-\Gamma_2=m$, where m is the modulation index. In such a condition, in both states, the same power is transferred from the antenna to the load. This situation can be easily achieved by switching a resistor in series or parallel to the IC's input.

By equation (2.17) the input power in states 1 and 2 are given by

$$P_{RF,in,ask,1} = P_{RF,in,ask,2} = (1-m^2)P_{avail} \quad \text{(Eq. 2.25)}$$

One of the main disadvantages of this kind of modulation compared to the PSK is the power lost in the series or parallel transistor. Here we assume that $R_2>R_1$ and we use a parallel resistance for modulation ($R_1=R_2 \parallel R_{MOD}$). In this case, when R_{MOD} is not connected, the antenna sees a resistance R_2 and all the power $P_{RF,in,ask,2}$ used for rectification. But when the resistor R_{MOD} is connected, the antenna sees resistor R_1 and

only a fraction of the power transferred from the antenna to the load can be used for rectification. So the input power that can be used for DC supply generation can be obtained as [10]

$$P_{rec,2} = P_{avail} \frac{4R_{ant}R_2}{(R_2 + R_{ant})^2} \quad \text{(Eq. 2.26)}$$

$$P_{rec,1} = P_{avail} \frac{4R_{ant}R_1}{(R_1 + R_{ant})^2} \frac{R_{MOD}}{R_{MOD} + R_2} \quad \text{(Eq.2.27)}$$

The backscatter power for the state 1 and 2 and also for both sidebands are given by [10]

$$P_{bs2} = P_{avail} \frac{R^2_{ant}}{(R_{ant} + R_2)^2} \quad \text{(Eq. 2.28)}$$

$$P_{bs1} = (\frac{R_2}{R_{ant}})^2 P_{sb2} \quad \text{(Eq.2.29)}$$

And

$$P_{bs} = m^2 P_{avail} = P_{avail} (\frac{R_2 - R_{ant}}{R_2 + R_{ant}})^2 \quad \text{(Eq. 2.30)}$$

2.4.2.2 PSK:

In the PSK modulation, the real part of the input impedance should be equal to the real part of the antenna impedance and the imaginary part will be modulated. In this case, the reflection coefficient becomes purely imaginary. By choosing two states symmetric by respect to zero the reflection coefficients in state 1 and 2 become equal in amount and different in phase ($\Gamma_{1,2}=\pm jm$).

In this case, from (2.17) and (2.21), the backscattered power and RF input power are found to be

$$P_{bs,psk} = m^2 P_{avail} = P_{avail} \frac{X^2}{4R^2_{ant} + X^2} \quad \text{(Eq.2.31)}$$

And

$$P_{RF,in,psk,1} = P_{RF,in,psk,2} = (1-m^2)P_{avail} = P_{avail}\frac{4R^2_{ant}}{4R^2_{ant}+X^2} \qquad \text{(Eq. 2.32)}$$

Where X is the imaginary part of the IC's impedance.

Here we see that all power in PSK is used either for rectification or for backscatter. Also the input power remains constant in both cases.

2.4.3 Matching Network

Matching network is used to deliver maximum power to the V_{DD} generator circuit. If a circuit is not perfectly matched, less power will be transferred. If a circuit is perfectly matched, maximum possible power will be transferred from the antenna to the load.

If we assume that an appropriate series reactance has been interposed between a source of impedance Z_S and a load of impedance Z_L to provide zero total series reactance, we can define a reflection factor from the load back to the source as shown in equation (2.16).

It has been shown that with a perfect matching between the antenna and the circuit, there will be a maximum power transfer. Also, a prefect match will result in 0 voltage reflection factor.

However, if a wider bandwidth compared with the bandwidth of a matched circuit is required, the antenna resistance can be increased to obtain a wider bandwidth. By doing this, there will be (of course) some reduction in the amount of power transferred, but

usually the amount is small and is in an acceptable level. Figure 2.13 is an equivalent circuit for the combined RFID antenna and the RFID circuit:

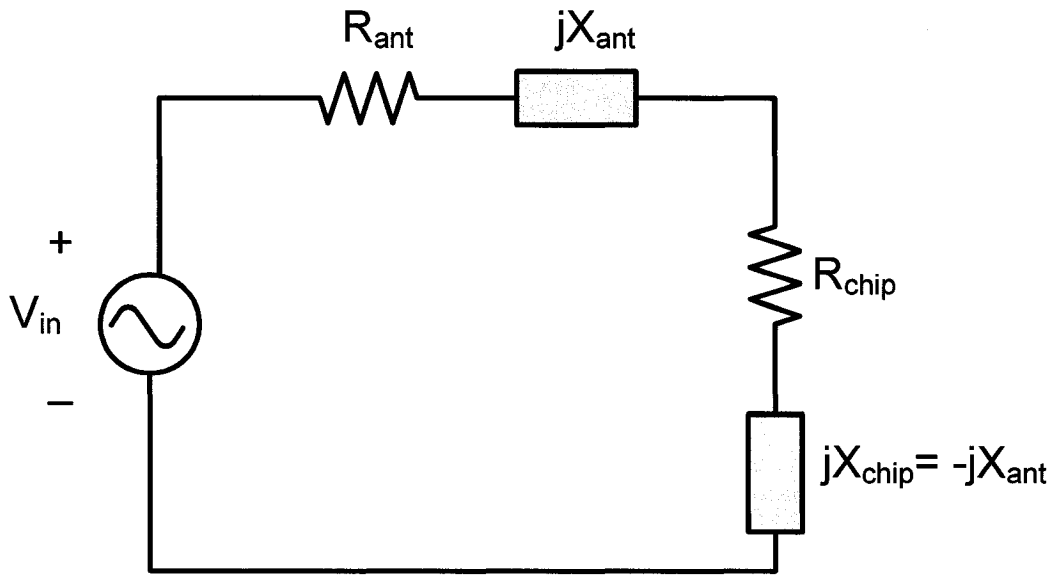


Figure 2.13. The equivalent circuit for the antenna and circuit

If $R_{ant} = R_{chip}$, the circuit is considered matched and has a voltage reflection factor of 0. In other words, 100% of the maximum possible power will be transferred to the load. The quality factor will be ½ of Q_{chip}, where Q_{chip} is the quality factor for just the chip.

If R_{ant} is increased to $2R_{chip}$, the voltage reflection factor will be -1/3 and 1/9 of the power will reflected and the efficiency will be around 89%. The quality factor will be 1/3 of Q_{chip}.

This shows that by increasing the value of R_{ant}, the quality factor will reduce and hence the bandwidth will increase. The trade-off is that the efficiency will decrease but may still be within the acceptable range.

2.5 Clock and POR Generator

2.5.1 Clock Generator

The base-band digital section of the chip needs a system clock to be able to run the state machine or to decode the data. All RFID systems require a clock generator. Some use a modulation on their carrier signal for the clock signal transmission and others generate the clock signal on chip [12].

For HF system, it is generally relatively easier to detect and extract the required clock signal from the carrier wave using dividers. The reason for which this is possible is that the data rate is relatively close to the carrier frequency and this allows the extraction of clock.

In the UHF systems, the direct extracting approach can not be utilized. This is because the carrier signal is operating at a high frequency and the power consumption of the chip will increase significantly once any part of the circuit starts to work with this carrier [12]. In this case, we have to implement an on chip oscillator to generate the system clock in UHF tag chips. The oscillator should be very low power and less sensitive to V_{DD}. The other option would be to modulate the carrier signal with an AM or FM signal that transfers the clock frequency.

2.5.2 Power on Reset

The power on reset circuit has two main functions that are essential for the correct operation of the chip. One is generating the reset signal for the digital section of the chip

and the other function is to disconnect the chip when the required power falls below a critical level.

The POR circuit measures the power supply level and then compares this level to a certain required threshold. If the power supply voltage exceeds the required threshold, the POR circuit generates the required command signals so that the operation of the chip would begin. The POR circuit has a delay element that generates a timing difference between the time that the supply is no longer adequate and that where the reset disable signal is set [12].

2.6 Digital Section

The baseband section of the RFID transponder can have different structures based on the RFID applications. The three most important parts in RFID digital section are sequencer and data encoder, anti-collision circuit, and EEPROM.

The sequencer and data encoder provide signals to address the memory array and to encode the output data, respectively.

In order to read multiple transponders simultaneously, the anti-collision feature is applied. The anti-collision scheme is shown in Figure 2.14. The transponder starts transmission of the data packet after receiving its power in a different time slot selected randomly by each ID itself, and then goes into sleep mode after sending a data packet [13].

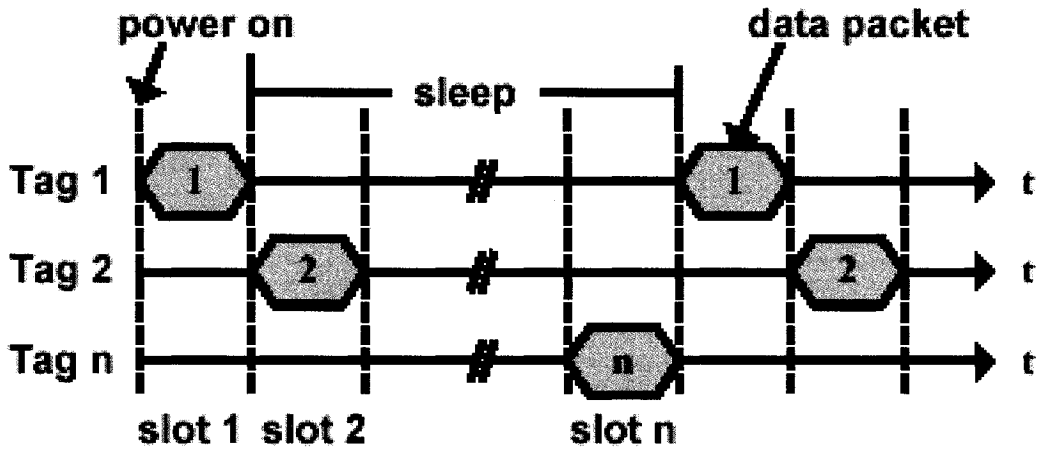


Figure 2.14. Anti-collision scheme

The EEPROM is used to save the tag ID that may later be used for the identification purposes of the tag in many applications. As an example in consumer product bar code applications, the lot number, product number, expiration date and etc could be saved on the tag.

CHAPTER 3. RFID FRONT-END DESIGN

In this chapter the RFID front-end schematic and the simulation results are described. Section 3.1 presents the V_{DD} generator part. Section 3.2 discusses the demodulator block. Section 3.3 leads to the detail description of the clock generator. The power on reset circuit is described in section 3.4. Finally, section 3.5 discusses the modulator and matching network.

3.1 V_{DD} Generator

The block diagram of V_{DD} generator section was shown in Figure 2.6. As discussed previously, the passive RFID tags derive their power supply from the incoming power instead of a battery. At the first stage of the V_{DD} generator, a RF-clamp circuit limits the amplitude of the input RF voltage to prevent any damage to the reset of the circuit caused by the high input power (breaking down of the transistors). Then a voltage multiplier produces a DC voltage based on the amplitude of the input RF voltage. Due to the huge variation of the rectified voltage (by as much as ten volts), a voltage limiter is employed at the output of the rectifier. The limiter at the rectifier output clamps the rectifier voltage to a narrower range. A fine regulator, then, regulates the supply voltage to a value of one volt.

The operation of different blocks of V_{DD} generator and their simulation results are described in this section.

3.1.1 RF Clamp Circuit

The input voltage of the RFID system can vary from several millivolts to tens of volts based on the distance between the reader and the transponder. In CMOS technology, the breakdown voltage of the MOS transistors is approximately 1.5-2 volts with the 0.13μm technology. The excessive voltage on the RF input of the tag could easily damage the chip structure. On the other hand, when the input voltage is large, the output voltage of the rectifier circuit will have a large variation (perhaps a decade) and the regulator design would be more challenging with the voltage overhead and the power consumption budget in hand. This shows the necessity of having an RF clamping circuit that will limit the RF input signal to approximately 1 volt. Of course the voltage regulator can then stabilize this voltage to a desired value once the variation is limited.

The schematic of proposed RF clamp circuit is shown in Figure 3.1. The designed voltage clamp uses feedback to sense the input voltage at the RF port and to close the loop in such a way that the input voltage could not exceed one volt. The design consists of a one stage voltage multiplier and two series transistors at the input RF to clamp the voltage. The gate of the clamp transistors are controlled by the output of the one stage rectifier followed by a low pass filter that cleans the high frequency variations on the signal. When the input signal experiences a large value of swing (say in orders of volts) the one stage rectifier and filter produces a large voltage and in turn this will turn on the clamp transistors. The clamp transistors will draw a large current from the input based on their gate voltage and this will result in the limitation of voltage. The sizing of the transistors and the rectifier design is such that the input is clamped to approximately one

volt. On the other hand the clamp circuit should be designed so that in the case of small input voltages the performance of the rectifier circuit is not affected. This means a good turn off of the clamp devices when the input has not exceeded the set level. The voltage after using a clamped circuit as a function of the amplitude of the input signal is shown in Figure 3.2.

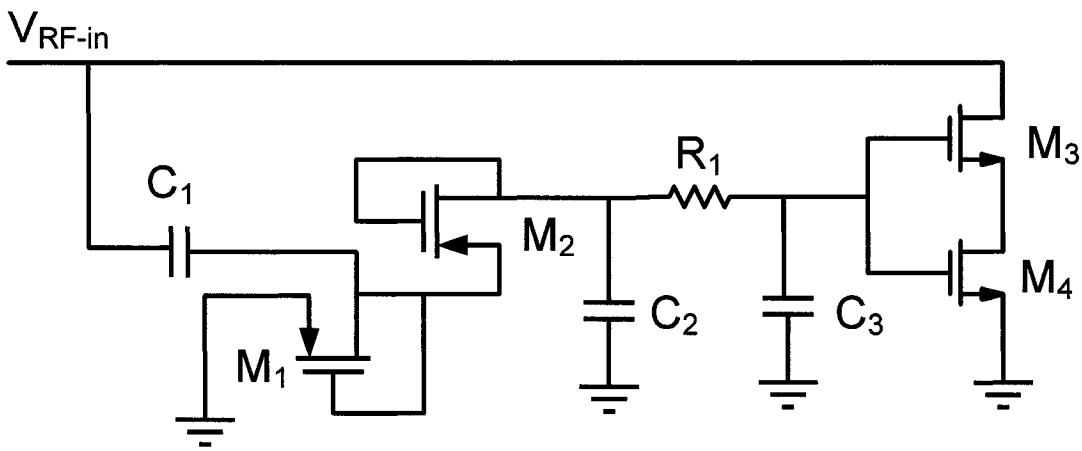


Figure 3.1. RF clamp circuit

Unlike any other parts of the circuit, the transistors in the clamp section should be able to withstand currents in the order of tens of milliamps. This requires careful layout and the use of large transistors so that the spike DC current does not cause damage to the transistor or metal layers. Also, having the clamp transistors in series helps improving the break down voltage limit of the devices. The component values of the RF clamp circuit are presented in Table 3.1.

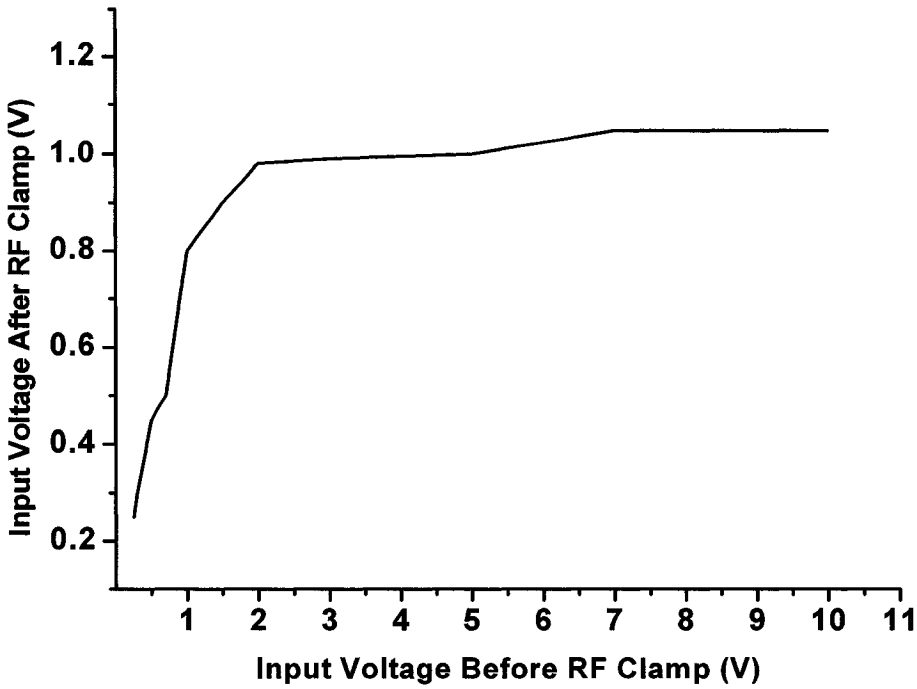


Figure 3.2. Input voltage after RF clamp circuit

A final plot of the RF-limiter layout is shown in Figure 3.3. The large block at the right of the layout is the one-stage voltage multiplier. The capacitor at the top-left side is the lowpass filter capacitor and the transistors at the bottom-left side are the current bypass transistors.

3.1.2 Voltage Multiplier (Rectifier)

The charge pump circuit of an RFID system, also called a voltage multiplier, converts the received input signal to a stable DC voltage. In the following sections, the design issues of a charge pump circuit and the proposed architecture is described.

Table 3.1. The component values of the RF clamp circuit

M_1-M_2	PMOSLVT, 30μm/.13μm, No. of Fingers=15
M_3-M_4	NMOSHVT, 20μm/.13μm, No. of Fingers=1
C_1	1pF
C_2-C_3	1.5pF
R_1	1KΩ

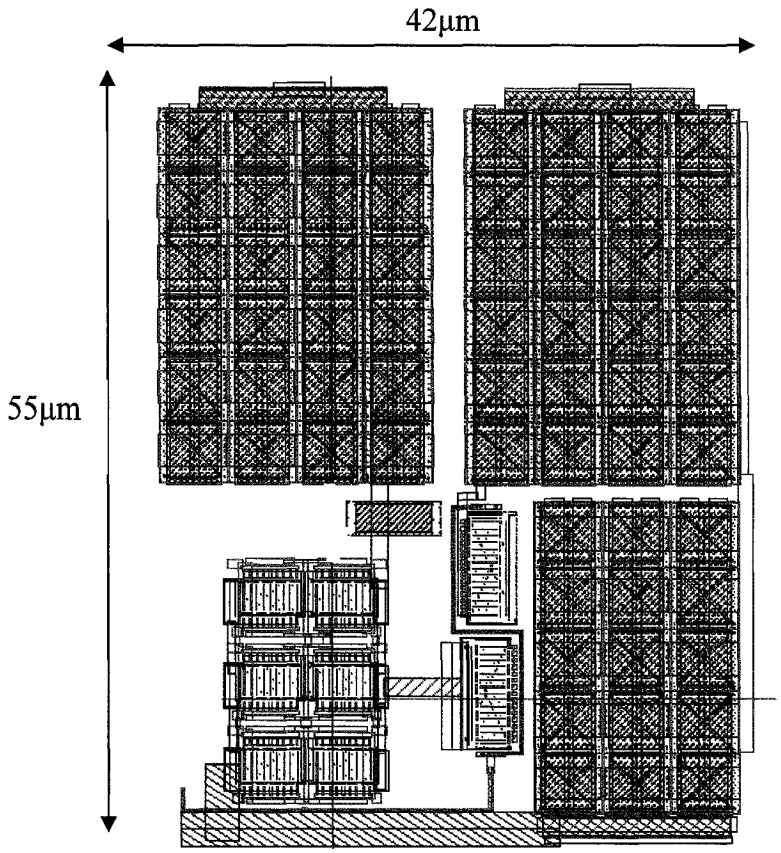


Figure 3.3. RF-limiter layout

3.1.2.1 Design Issues

One of the most important factors in design of RF to DC converters in RFID systems is the minimum required DC voltage to ensure proper operation of the digital and analog circuits. Given the range specifications and also the FCC power level requirements in the 2.4GHz band, the required DC voltage level determines the number of stages in the charge pump circuit. Using double polarity supply voltage circuits ($\pm V_{dd}/2$) instead of single polarity (V_{dd}) decreases the required input signal level by half. The well known equation expressing the voltage level (V_{rf}) of an RF signal at antenna is given by

$$V_{rf} = \sqrt{8P_r R_{ant}} \qquad \text{(Eq. 3.1)}$$

Where P_r is the received power at the antenna and R_{ant} is the equivalent antenna impedance.

Using double polarity for supply voltages decreases the required number of stages to reach $V_{dd}/2$ and this improves the overall efficiency of the charge pump circuit. However, the disadvantage would be increasing the area because two charge pumps are required for the positive and negative supply circuits.

The power efficiency of charge pump circuits describes how much power is lost during the RF to DC conversion process. This efficiency depends on the number of stages, the performance of the diodes and also the input power of the multiplier. It is interesting to note that a decrease in the input power level of the charge pump circuit, decreases the efficiency and significantly lowers the output voltage. For diode based charge pumps, the efficiency could be described by [14]

$$\eta = \frac{V_{dd} I_{laod}}{2nI_s V_p B_1(\frac{V_p}{V_T})\exp(\frac{-V_{dd}}{2nV_T})} \qquad \text{(Eq. 3.2)}$$

Where V_{dd} is the generated output DC voltage, I_{laod} is the output DC current, I_s is the saturation current, V_p is the peak of the input signal, V_T is the thermal voltage, n is the number of stages and $B_1(x)$ is the first order modified Bessel function.

Designing a voltage multiplier to operate from low RF power levels, as is the case here, leaves a very limited choice of variables considering the constraints. The ratio of the output DC voltage to the input AC voltage determines the impedance transformation of the charge pump which is also affected by the loss factor of the circuit. The input resistance (R_{in}) of the charge pump voltage multiplier, shown in Figure 3.4, can be described by

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{R_{load}}{n^2_{eff}}\eta \qquad \text{(Eq. 3.3)}$$

and

$$\eta = \frac{V_{dd} I_{load}}{V_{in} I_{in}} = \frac{n_{eff}}{m} \qquad \text{(Eq. 3.4)}$$

Where n_{eff} is the effective voltage gain of the multiplier, m is the output to input current ratio and R_{load} is the load resistance at the output of the voltage multiplier. The value of R_{load} can be obtained by the power consumption of the baseband circuits. The input impedance (R_{in}) of the voltage multiplier can be calculated using (3.3) and (3.4) when R_{load} and the current and voltage ratios are known. For most cases, R_{load} and R_{ant}

are not equal which mandates using a matching network and in turn, alters the voltage at the input of the voltage multiplier.

Another factor in designing the charge pump is the time constant associated with the discharge of the capacitors. This time constant must be sufficiently larger than the signal period to ensure the change in the supply voltage caused by transistors activity is minimal.

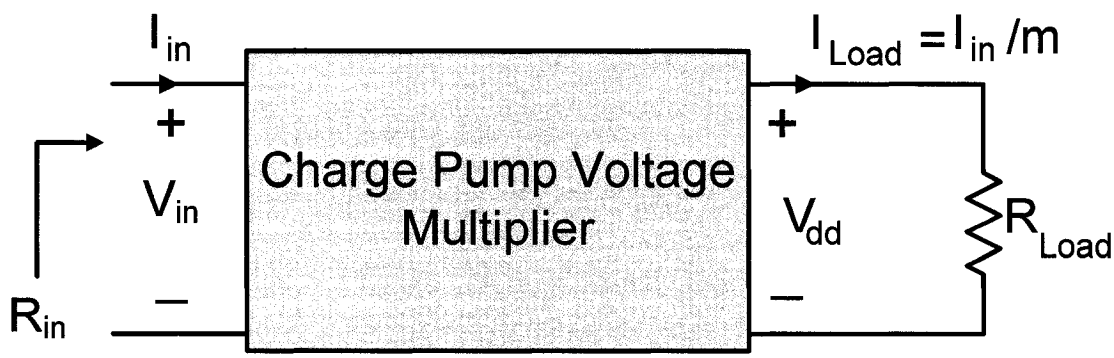


Figure 3.4. The input and output modeling of the charge pump voltage multiplier

3.1.2.2 Proposed Rectifier Circuit

In conventional charge pump circuits, RF signals of the different stages are equal to the input RF signal (taking the matching network effect into account). For the case when the RF signal applied to the last stage of the voltage multiplier is k times larger than the RF signal applied to other stages, equation (2.13) can be rewritten as

$$V_n = 2[(n + k - 1)V_p - nV_D] \qquad \text{(Eq. 3.5)}$$

As seen from (3.5), increasing the input signal V_P at the last stage by k factor will increase the output voltage V_n .

The above analysis shows that the increase in the amplitude of the RF signal at the last stage of the charge pump has a tremendous effect on the DC voltage level of the output. This suggests that using a highly efficient RF amplification at the n^{th} stage could be very beneficial to achieve higher DC voltage at the output of the voltage multiplier. Using an amplifier in the n^{th} stage to achieve this objective will introduce a considerable loading to the charge pump circuit. Furthermore, the gain of a tuned amplifier in a low power RFID front-end is usually too low in the subthreshold region to introduce a noticeable voltage difference at the output of the voltage multiplier.

A novel technique to increase the RF signal level is to use passive tuned elements at the input of the voltage multiplier. This technique will introduce no extra loading on the multiplier stages and also does not need any biasing current. The voltage (V_c) across the capacitor C of a simple series RLC circuit is given by

$$V_C = \frac{I}{j\omega C} = \frac{V_{in}}{R + j\omega L + (j\omega C)^{-1}} \cdot \frac{1}{j\omega C} \qquad \text{(Eq. 3.6)}$$

At the resonance frequency, the impedance of the RLC circuit becomes equal to the resistance R and the voltage across the capacitor becomes

$$V_C = jV_{in}Q \qquad \text{(Eq. 3.7)}$$

Where Q is the quality factor of the series RLC circuit.

This analysis shows that if an RC circuit is connected to a source, the RF signal across the capacitor can be boosted by a factor of Q if a series inductor is placed between the source and the load. This will help to increase the output voltage of a charge pump since the load can be effectively modeled by an RC circuit.

The schematic of the first stage of the charge pump circuit by replacing the diodes with MOS transistors and also using inductive elements to boost the voltage is shown in Figure 3.5.

The AC small signal models of a single stage multiplier in the two positive and negative signal cycles are shown in Figure 3.6. Using parallel to series transformation, as shown in Appendix, the input capacitance and series resistance of the circuit can be extracted. The addition of an inductor to the charge pump circuit with respect to the R and C values derived in Appendix, improves the gain of the voltage multiplier. The

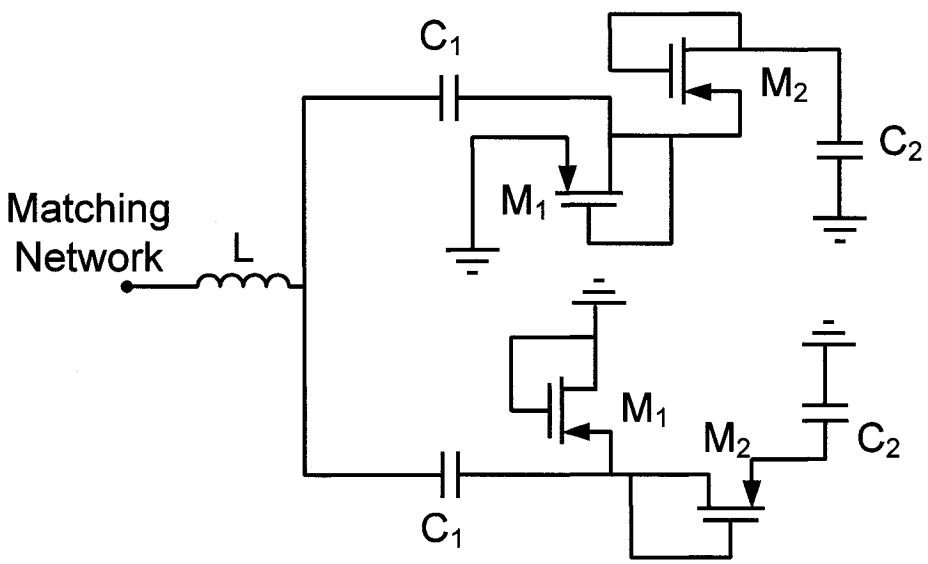


Figure 3.5. Schematic of the first stage of the charge pump with inductor

simulation result of single stage voltage multiplier with the input power of -19.5dBm both with and without the inductor is shown in Figure 3.7. As can be seen in this figure, the DC output voltage is larger by a factor of 4.2 when the inductor is used.

In the same manner the input capacitance and resistance of a multi-stage charge pump circuit could be derived. These values are used to derive the size of the inductance used for the passive multiplication at 2.4 GHz which is 2.1nH for the 6-stage charge pump used in this work. The gain at input of the charge pump circuit after the addition of the inductors is shown in Figure 3.8.

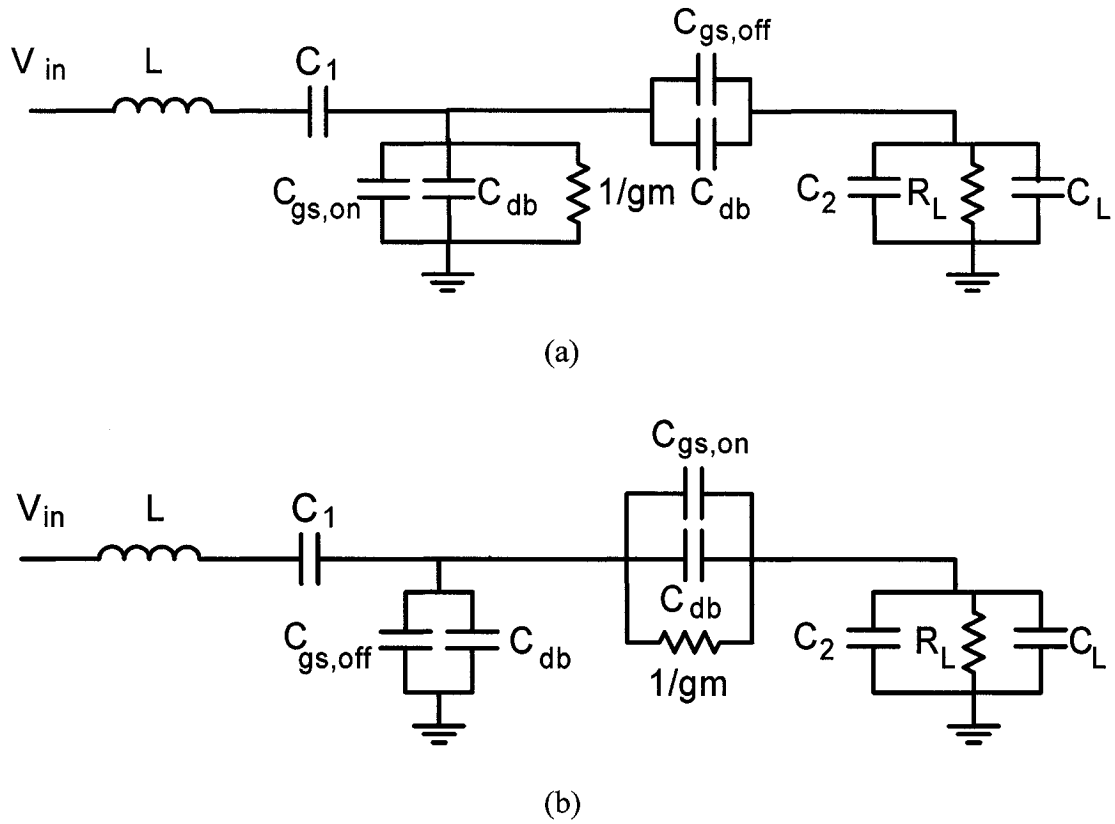


Figure 3.6. Equivalent circuit of a single stage voltage multiplier (a) Negative cycles of the input voltage (b) Positive cycles of the input voltage

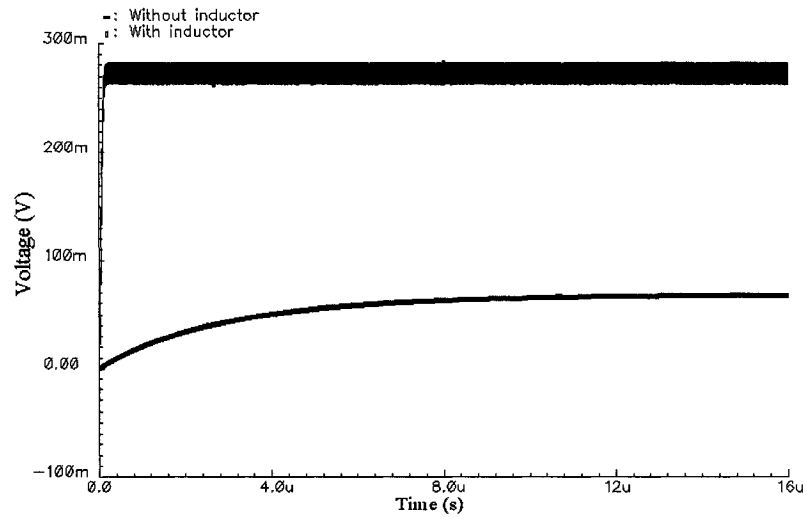


Figure 3.7. Output of the 1-stage voltage multiplier with and without inductor

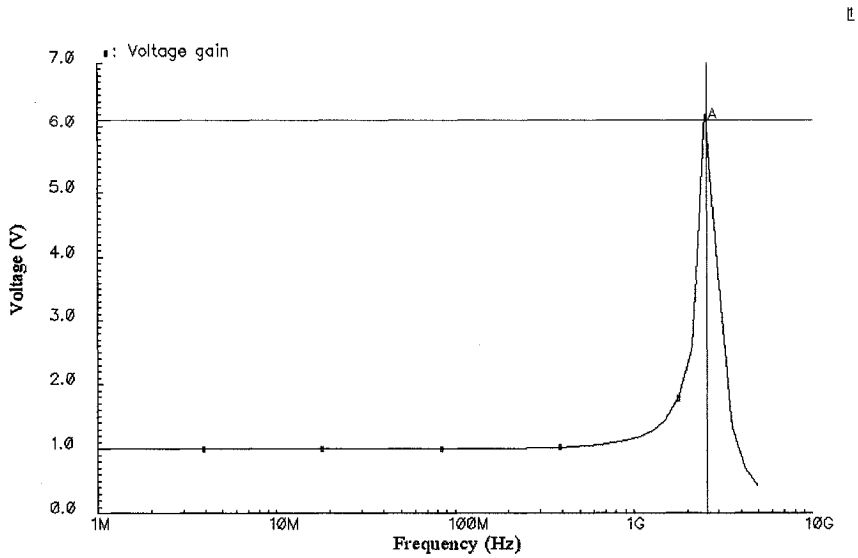


Figure 3.8. Voltage gain after inductor

In the proposed topology, the series inductor also helps in bringing the input impedance level closer to the 50Ω of the antenna. Generally one of the main issues with a typical charge pump circuit in an RFID application is with the input matching. The real

part of the input impedance is low at the source side and needs to be increased with a matching network. In this topology, the two effects of voltage multiplication and impedance transformation are achieved at the same time because of the embedded LC matching network.

The minimum input voltage required to obtain a 1.2V DC voltage at the output of the 6-stage multiplier used in this work is 60mV (peak) which corresponds to -20.45dBm incident power at the antenna. The output DC voltage of the charge pump with a 1MΩ load with respect to the received power at the antenna is shown in Figure 3.9. The settling time and behavior of the output voltage of the 6-stage multiplier is illustrated in Figure 3.10 for an input power of -19.1dBm and 1MΩ load. The generated DC voltage at the output of different charge pump stages is shown in Figure 3.11 with the same power and load.

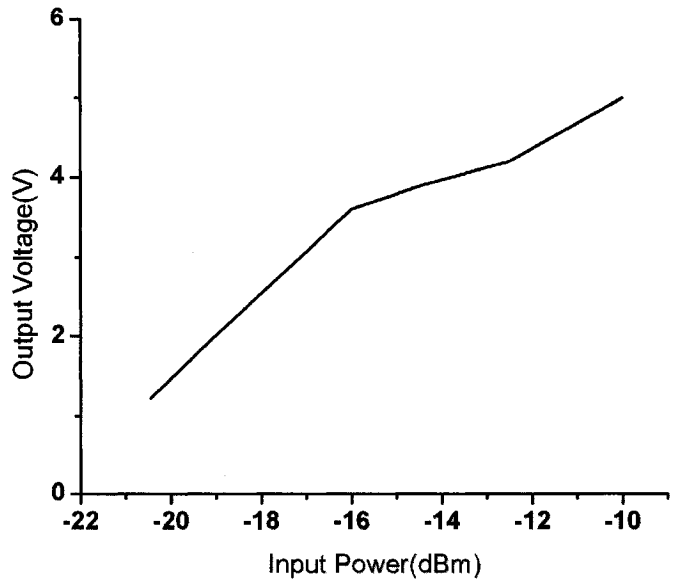


Figure 3.9. Output voltage of the multiplier as a function of input power

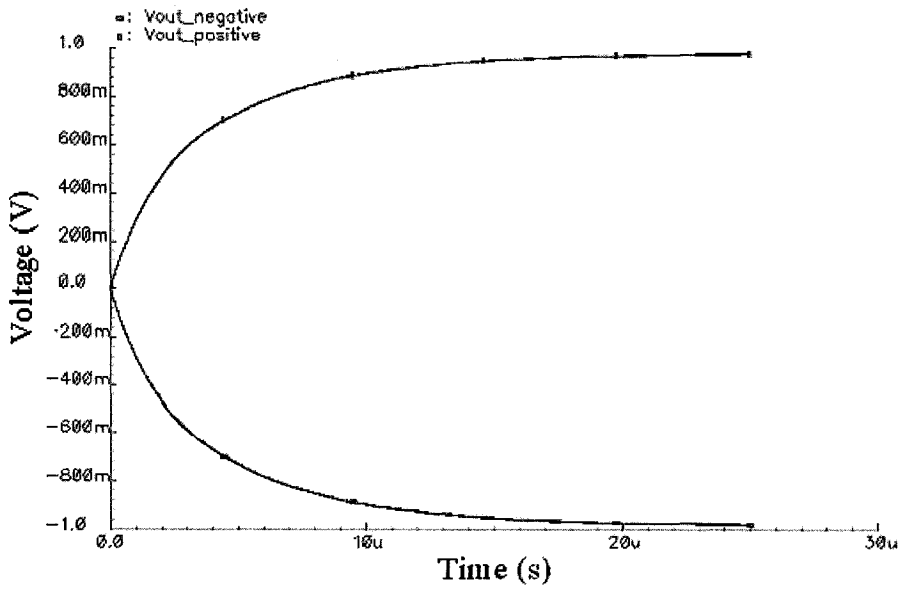


Figure 3.10. Output voltage of the multiplier for input power of –19.1dBm and R_{load} of 1MΩ

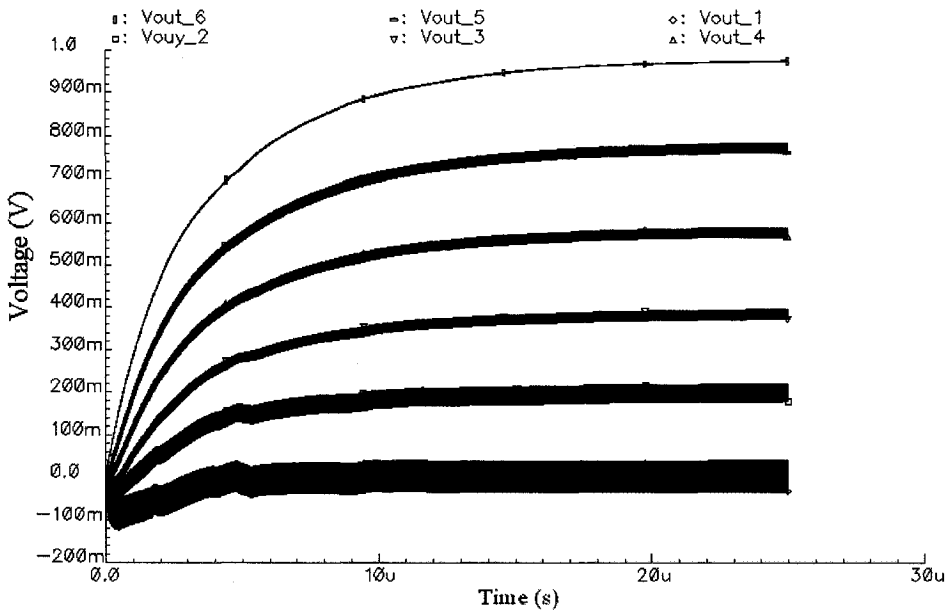


Figure 3.11. Output voltage at different stages of the multiplier

The output DC voltage of the charge pump is shown in Figure 3.12 as a function of the load presented by the circuit. From the output DC voltage (1.2V) and the DC current (or the effective DC resistance), the power efficiency of the charge pump with a 1MΩ effective load and an input power of -19.1dBm is 20.1%. In comparison with [15] with a reported efficiency of 11%, the efficiency of this design is better by 9% and also the minimum input power for a 3V rail to rail DC generation is better by 42μW (20.25μW compared to the reported 63μW in [15]). The performance comparison of the proposed RFID front-end and the best previous reported works is summarized in Table 3.2. The operating ranges of the RFID circuits are expressed in terms of wavelengths instead of frequency to make the comparisons relevant. The rectifier component values are presented in Table 3.3.

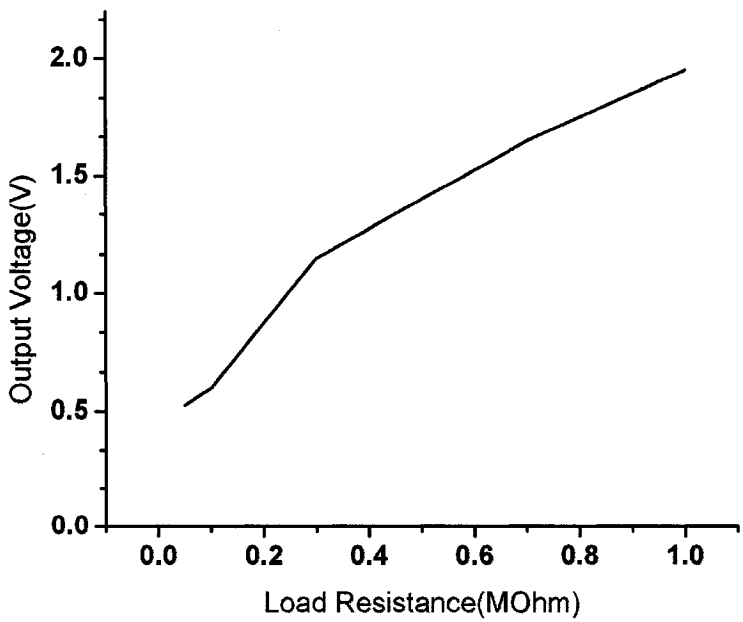


Figure 3.12. Output voltage as a function of the load resistance

The layout of the positive-voltage rectifier is shown in Figure 3.13. The capacitor at the top is a 20pF capacitor to store the charge.

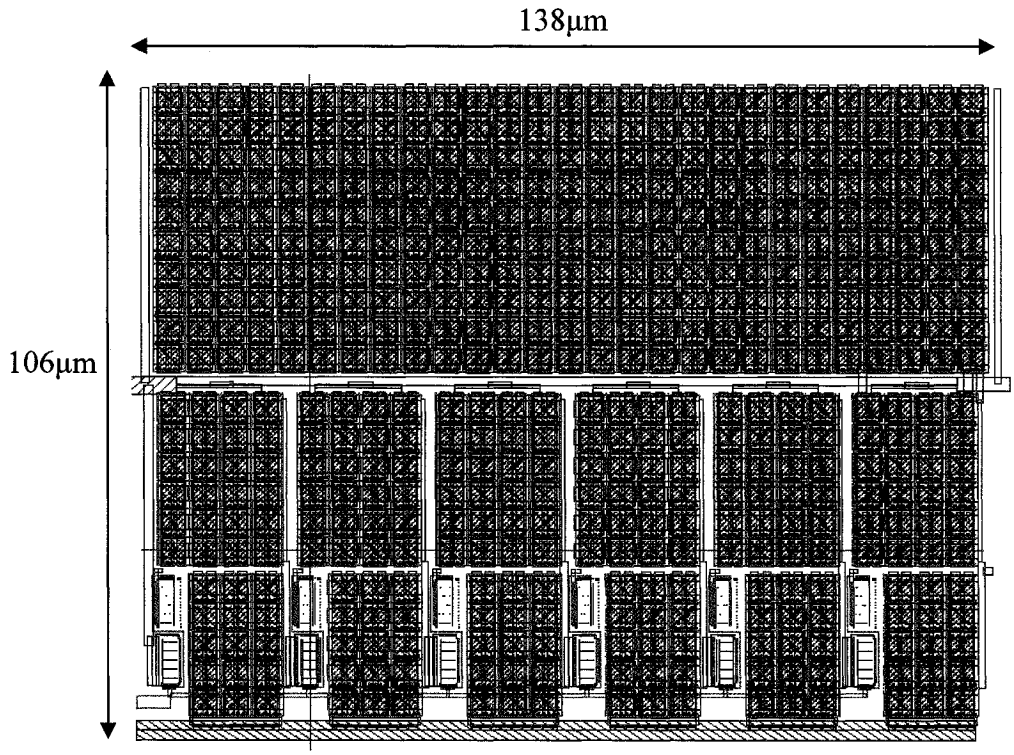


Figure 3.13. Voltage rectifier layout

Table 3.2. Performance comparison of RFID charge pump

Parameters	Efficiency	Min. Input Power For Generating 3V DC	Range
Proposed Charge-Pump	20.1%	20.25μW	37.6λ
[15]	10.94%	63 μW	21.32λ
[11] –Schottky diodes	14.5%	–	28.2 λ

Table 3.3. The component values of the rectifier circuit

M_1-M_2	PMOSLVT, 30μm/.13μm, No. of Fingers=15
C_1	1pF
C_2	1.5pF
L	1.8nH, Q=6

3.1.3 DC-Limiter

The limiter circuit for the positive part of the voltage multiplier is shown in Figure 3.14 [12]. The circuit shown uses a specified fraction of the generated output voltage to control the gate voltage of transistor M_3. This transistor acts very similar to a tunable load. The load current of the system is varied through the gate voltage that is set on the M_3 transistor.

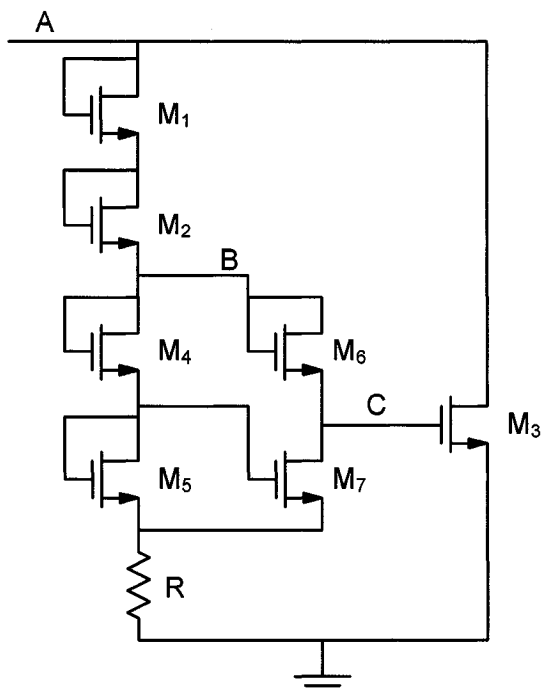


Figure 3.14. The crude clamp circuit acting as the positive voltage limiter

The size of M_5 is set to be larger than that of M_7. This will lead to the fact that most of the current will choose the path that consists of transistor M_5. This will result in the drain-source voltage of transistor M_6 to be smaller than that of M_4. Based on this analysis M_7 will also work in the saturation region and therefore the voltage on node C will follow that of node B by a threshold voltage. If we neglect the substrate bias then we can safely say that transistor M_3 can be turned on when the voltage of node A goes above four threshold voltages. With the substrate bias, the turn on voltage will even be higher.

As shown in Figure 30, the voltages at node C and B can be described as follows

$$V(C) = V(A) - V_{gs1} - V_{gs2} - V_{gs6} = V(A) - 3V_{gs1} \quad \text{(Eq. 3.8)}$$

$$V(D) = V(A) - V_{gs1} - V_{gs2} - V_{gs4} - V_{gs5} = V(A) - 4V_{gs1} \quad \text{(Eq. 3.9)}$$

$$V(D) = I(M_1)R \quad \text{(Eq. 3.10)}$$

$$I(M_1) = \frac{1}{2}\beta_{M1}(V_{gs1} - V_{th})^2 \quad \text{(Eq. 3.11)}$$

Where

$$\beta_{M1} = \mu_n C_{ox}(\frac{W}{L})_{M1} \quad \text{(Eq. 3.12)}$$

By using equations (3.9),(3.10) and (3.11), we can get the V_{gs1}, which is given by

$$V_{gs1} = V_{th} - \frac{2}{k} + \frac{1}{k}\sqrt{k[V(A) - 4V_{th}] + 4} \quad \text{(Eq. 3.13)}$$

Where $k = \frac{1}{2}\beta_{M1}R$

By equation (3.13) we can derive

$$\frac{\partial V_{gs1}}{\partial V(A)} = \frac{1}{2\sqrt{k[V(A) - 4V_{th}] + 4}} \quad \text{(Eq. 3.14)}$$

From equation (3.14), the resistor R acts as an attenuator besides limiting the current flow of the reference branch. Without this resistor, gate-source voltage of M_1 will be ¼ of V_A (neglecting the bias voltage of the substrate) and also V_C will follow V_A with the ratio of ¼. Resistor R will attenuate the variation on the gate-source voltage of M_1 that is caused by V_A. When this attenuation is in place, V_C can now follow V_A with an effectively larger ratio. If we let R go towards infinity, then the gate-source voltage of M_1 will remain almost constant and V_C tends to follow V_A. Therefore, given this analysis, once we look at this from a whole circuit perspective, the attenuation on V_{gs1} looks very similar to a gain [12].

By equation (3.13), current of transistor M_3 can be given by

$$I(M_3) = \frac{1}{2}\beta_{M3}[V(A) - 4V_{th} - \frac{3}{k}\sqrt{k[V(A) - 4V_{th}] + 4} + \frac{6}{k}]^2 \quad \text{(Eq. 3.15)}$$

Substitution with two limits of k, we can get:

$$I(M_3) = \frac{1}{2}\beta_{M3}[\frac{1}{4}V(A) - V_{th}]^2, R = 0 \quad \text{(Eq. 3.16)}$$

$$I(M_3) = \frac{1}{2}\beta_{M3}[V(A) - 4V_{th}]^2, k = \frac{1}{2}\beta_{M1}, R = \infty \quad \text{(Eq. 3.17)}$$

With the given analysis one can now choose the transistor sizes given the specific system specifications. A good staring point would be the input RF dynamic range which is given by regulatory issues and the power consumption. The maximum operation range of the tag affects the minimum chip power consumption.

In the next step, one needs to determine the maximum output voltage. This value is determined by the number of stacked NMOS transistors. If transistors M_1 and M_2 are replaced by their PMOS counterparts, the effect of the substrate bias voltage will be reduced to some extent and from that the voltage required for turn-on will be decreased.

After deciding the turn-on voltage of the limiter and the output voltage variation that can be tolerated, the size of transistor M_3 can be found by use of equations (3.16) and (3.17).

The limiter circuit for the negative part of the rectifier is the same as for the positive one, but instead of using NMOS transistors, the effective same size PMOS transistors are used.

The sum output voltage at the output of the rectifiers before and after voltage limiter as a function of input power is shown in Figure 3.15. The layout of the voltage limiter is shown in Figure 3.16. The component values of positive and negative voltage limiter are presented in Table 3.4.

3.1.4 Regulator

The output voltage of the limiter circuitry is heavily dependent upon the threshold voltage changes on the MOS transistors and therefore is not constant. Analog and digital circuitries require the supply voltage to be constant to function properly and therefore, a voltage regulator is required to resolve the issue. Due to the limitations on available

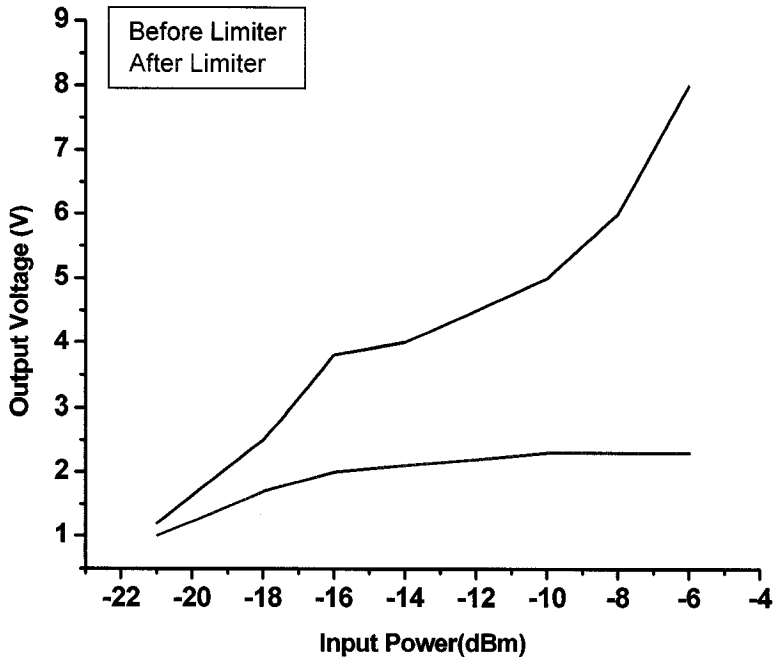


Figure 3.15. Rectifier output voltage before and after using limiter as a function of input power

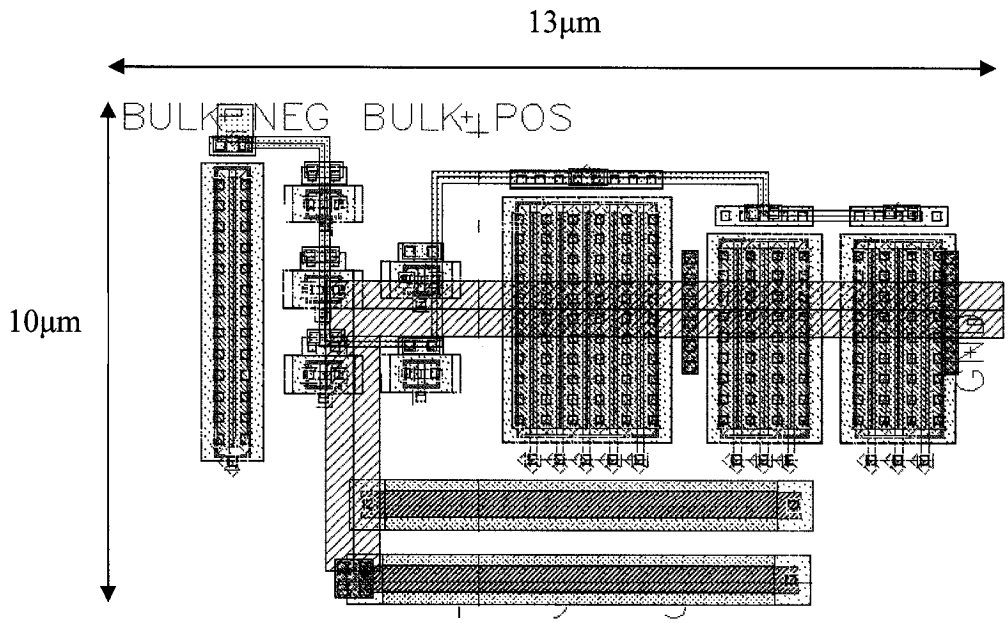


Figure 3.16. DC-limiter layout

Table 3.4. The component values of the positive (negative) DC-limiter circuit

M_1- M_2-M_4-M_6-M_7	NMOSLVT (PMOSLVT), .15μm/.13μm, No. of Fingers=1
M_5	NMOSLVT (PMOSLVT), 5μm/.13μm, No. of Fingers=1
M_3	NMOSLVT (PMOSLVT), 40μm/.13μm, No. of Fingers=10
R	10KΩ

power, the regulator in RFID systems must be extremely power efficient and work with low current levels. Also, the regulator must have a very good power supply noise rejection (PSNR) to filter out all fluctuations of the supply voltage observed by other circuits. Furthermore, it should have a good temperature stability to prevent changing of reference voltage by the temperature changing. The block diagram of the positive voltage regulator is shown in Figure 3.17.

The reference voltage generator block will produce a constant voltage and current which are independent of the limiter output voltage. These voltage and current are fed to series voltage regulator as the reference voltage and bias current [16].

3.1.4.1 Reference Current and Voltage Generator

The essence of the operation of the reference voltage generator is to use a self-biased current reference that drives the current into a stack of diodes, presenting a voltage at the

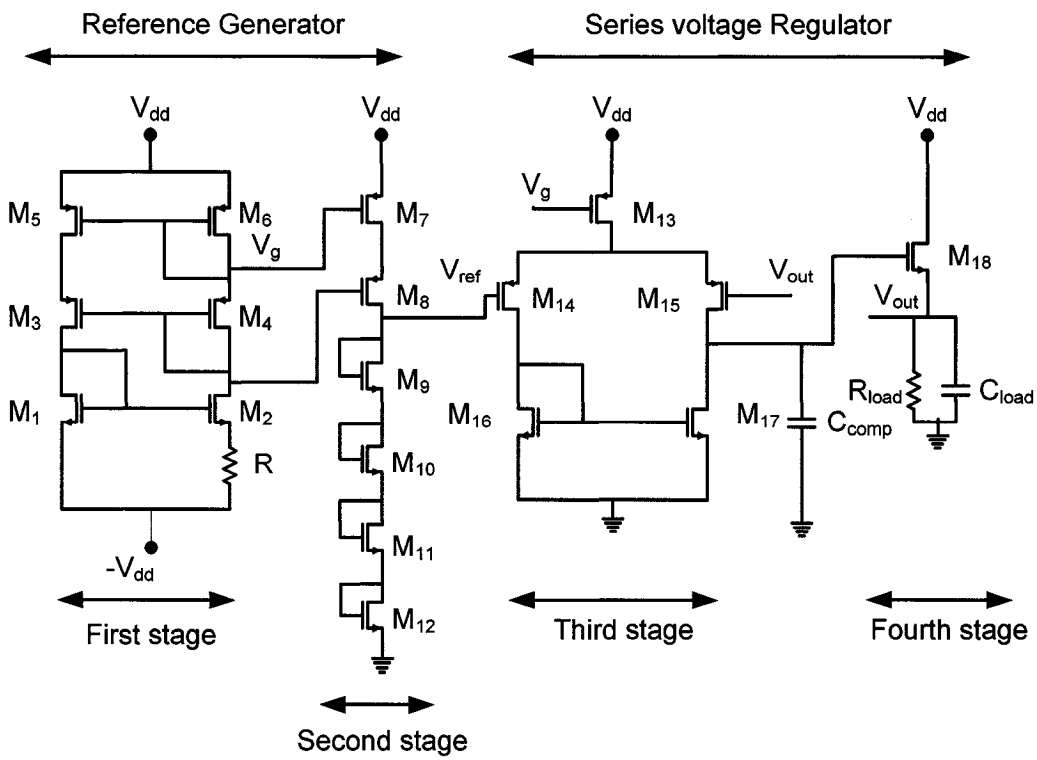


Figure 3.17. The circuit of the voltage regulator

input of the series regulator. The self-biased current source is formed by connecting a current source to a current mirror. The block-diagram of a self-biasing current source and its characterization plot are shown in Figure 3.18 [17]. The two key variables here are input and output currents. The relation between these variables is governed by both the current source and the current mirror characteristics. From the standpoint of the current source, the output current is almost independent of the input current for a wide range of the input currents. From the standpoint of the current mirror input current and output current are equal (assuming that the gain of the current mirror is unity). The

operating point of the circuit must satisfy both constraint and hence is at the intersection of the two characterizations [17].

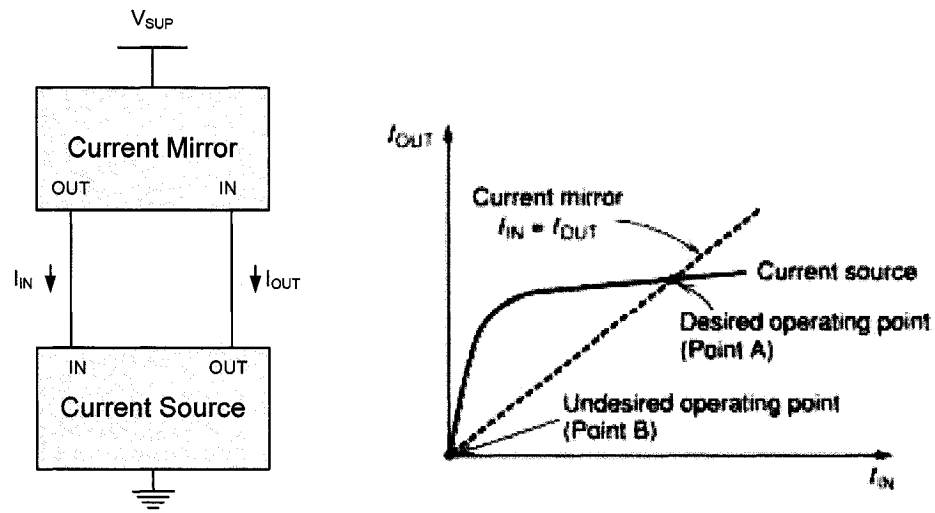


Figure 3.18. Block diagram of a self-biasing current source and its characterization plot

In this project, the self-biased current source consists of a cascode PMOS current mirror stacked on top of a Widlar current source. As shown in Figure 3.17, the gate-source voltage of transistor M_1 is equal to the gate-source voltage of Transistor M_2 plus the voltage drop across the resistor R.

$$V_{gs1} = V_{gs2} + RI_{out} \qquad \text{(Eq. 3.18)}$$

And because the transistors acts in subthreshold region, V_{gs} is given by

$$V_{gs} = V_{th} + nV_T \ln\left(\frac{I_d}{(W/L)I_t}\right) \qquad \text{(Eq. 3.19)}$$

Where I_t represents the drain current with $V_{gs}=V_{th}$ and depends on the device parameters such as doping and subthreshold slope and V_T is the thermal voltage.

By substituting equation (3.19) in equation (3.18), we can drive the equation below that shows the relation between I_{in} and I_{out} of the Widlar current source.

$$nV_T \ln(\frac{(W/L)_2}{(W/L)_1}.\frac{I_{in}}{I_{out}}) = RI_{out} \qquad \text{(Eq. 3.20)}$$

In the current mirror part, to decrease the effect of channel length modulation, a cascode current mirror is used. Cascode current mirrors increase the output resistance and therefore are less susceptible to current mismatches between transistor pairs. In the cascode structure, the variation of the drain voltage of transistor M_5 will be shield by transistor M_3. The variation of the drain voltage of M_5 by the change of V_{DD} can be describes as follows [18]:

$$\Delta V_{d5} = \frac{\Delta V_{DD}}{(gm_3 + gmb_3)Ro_3} \qquad \text{(Eq. 3.21)}$$

Where gm and gmb are the transconductance and the body transconductance respectively and Ro is the output resistance of the transistor.

For I_{in} be equal to I_{out} we need $V_{gs3}=V_{gs4}$ and $V_{ds5}=V_{ds6}$. From Figure 3.17 we have $V_{gs3}+V_{ds5}=V_{gs4}+V_{ds6}$. Thus, if $(W/L)_6/(W/L)_5= (W/L)_4/(W/L)_3$, then $V_{gs3}=V_{gs4}$ and $V_{ds5}=V_{ds6}$. This result holds even if M_3 and M_4 suffer from body effect.

So by choosing cascode structure and equal (W/L) for the transistors M_3 to M_6, the I_{in} and I_{out} will be equal to each other. By using this fact in equation (3.20), the output current (I_{out}) of the current mirror can be obtained in the subthreahold region by [19]

$$I_{out} = \frac{nV_T}{R} \ln(\frac{(\frac{W}{L})_2}{(\frac{W}{L})_1}) \qquad \text{(Eq. 3.22)}$$

To make the power consumption of the regulator as low as possible, the reference current should be in the order of 10-20nA. Based on equation (3.22) to reduce I_{out} either resistance R can be increased or the width to channel length ratio of the transistors can be selected close to unity. Although the latter looks attractive in terms of layout area reduction and matching improvement, it may not be a desirable choice in terms of the sensitivity of I_{out} to this ratio, which can be calculated from the following general equation in subthreshold region

$$V_{gs} = V_{th} + nV_T \ln\left(\frac{I_{out}}{\left(\frac{W}{L}\right)I_t\left[1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right]}\right) \qquad \text{(Eq. 3.23)}$$

We can find the output current in the presence of channel length modulation as

$$I_{out} = \frac{V_{gs1} - V_{gs2}}{R} = \frac{nV_T}{R}\ln\left(\frac{(W/L)_2[1-\exp(-V_{ds2}/V_T)]}{(W/L)_1[1-\exp(-V_{ds1}/V_T)]}\right) \qquad \text{(Eq. 3.24)}$$

From equation (3.24) and (3.22) the sensitivity of the current source can be find as follows

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\ln\left(\frac{1-\exp(-V_{ds2max}/V_T)}{1-\exp(-V_{ds2min}/V_T)}\right)}{\ln\frac{(W/L)_2}{(W/L)_1}} \qquad \text{(Eq. 3.25)}$$

In which the V_{ds2} is the drain-source voltage of M_2 given by

$$V_{ds2} = V_{dd} - 2V_{diode} \qquad \text{(Eq. 3.26)}$$

Therefore the feasible option seems to be increasing the value of resistor R instead of choosing the width to channel length ratio close to unity. The W/L ratio is chosen to yield the desired sensitivity from equation (3.25). In this project the $(W/L)_2/(W/L)_1$ is

chosen to be 2.3 to ensure a small change in the output current with the change in the input voltage. Resistor R is chosen to be 20kΩ to give the desired amount of current (11.5nA). The performance of the regulator in terms of the variations in the reference current with the change of V_{dd} is shown in Figure 3.19.

Another important aspect of the self-biasing circuit is its dependence on temperature which can be shown by its fractional temperature coefficient TC_F. Fractional temperature coefficient is most conventionally expressed in term of the fractional change in output current per degree centigrade of temperature variation [17]. By using equation (3.22) we can find the TC_F of the current source as follows

$$TC_F = \frac{1}{I_{out}} \frac{\partial I_{out}}{\partial T} \qquad \text{(Eq. 3.27)}$$

$$\frac{\partial I_{out}}{\partial T} = \ln\left(\frac{(W/L)_2}{(W/L)_1}\right)\left[\frac{n}{R}\frac{\partial V_T}{\partial T} - \frac{nV_T}{R^2}\frac{\partial R}{\partial T}\right] = \ln\left(\frac{(W/L)_2}{(W/L)_1}\right)\left[\frac{nk}{Rq} - \frac{nV_T}{R^2}\frac{\partial R}{\partial T}\right] \qquad \text{(Eq. 3.28)}$$

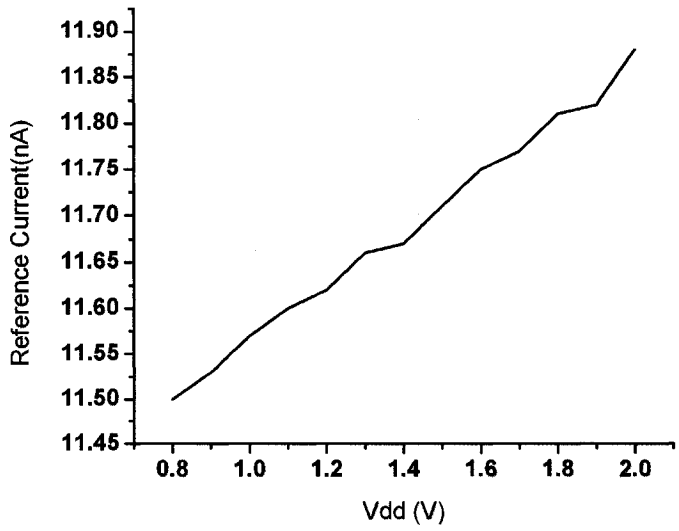


Figure 3.19. Reference current as a function of DC voltage variation

So by using equations (3.28) and (3.22) TC_F can be find as

$$TC_F = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T} \qquad \text{(Eq. 3.29)}$$

At the above equation the fractional sensitivities of both V_T and the high resistive poly resistor are positive and tend to cancel each other.

Then the current will be mirrored and flow through a ladder of diode connected transistors. The current in the ladder of diodes is fixed and is determined by the ratio of $(W/L)_7/(W/L)_6$. To fix the drain voltage of transistor M_7 with respect to the change in the V_{DD} voltage, a cascode configuration is used.

The reference voltage as a function of DC voltage variation is shown in Figure 3.20. The reference current as a function of temperature is shown in Figure 3.21.

3.1.4.2 Series Voltage Regulator

The series voltage regulator, shown in Figure 3.17, is simply a differential amplifier with feedback. The feedback senses the output voltage and compares it with the V_{ref} provided by the voltage reference of the second stage. For the differential amplifier, a PMOS amplifier is chosen with an NMOS active load. The effect of the bias current on the output voltage at DC is as follows [16]

$$\frac{\Delta V_{reg}}{\Delta I_{bias}} \cong \frac{\dfrac{r_{o15} \parallel r_{o17}}{2}\dfrac{gm_{18}R_L}{1+gm_{18}R_L}}{1+\dfrac{r_{o15} \parallel r_{o17}}{2}gm_{15}\dfrac{gm_{18}R_L}{1+gm_{18}R_L}} \cong \frac{1}{gm_{15}} \qquad \text{(Eq. 3.30)}$$

Where r_o is the output resistance and gm is the transconductance of the transistor.

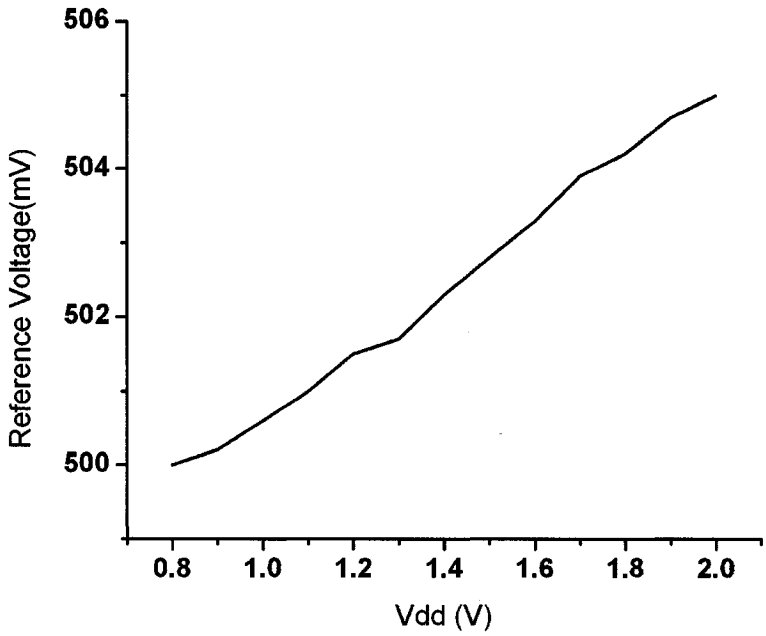


Figure 3.20. Reference voltage as a function of DC voltage variation

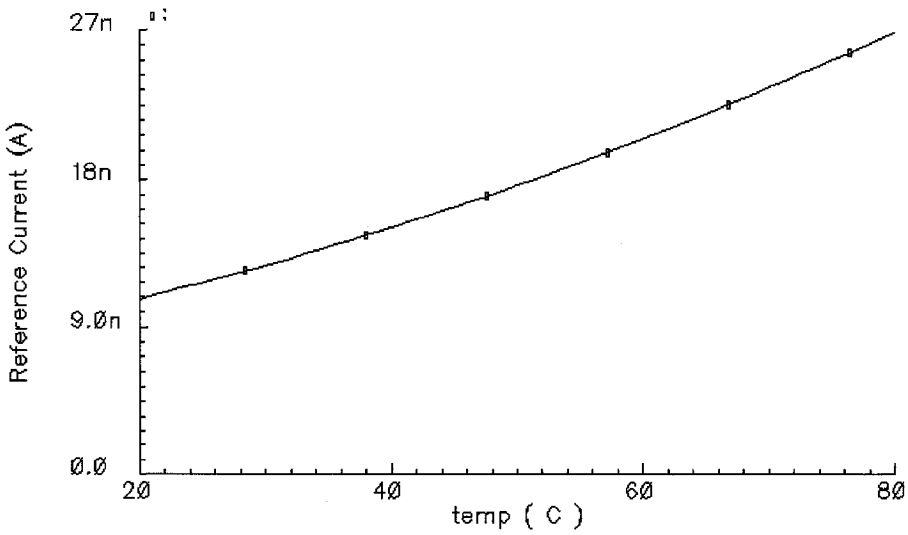


Figure 3.21. Reference current as a function of temperature

To ensure very small power consumption, the bias current should be very small and based on equation (3.30) lowering the power increases the sensitivity of the regulated voltage with respect to the bias current. This increased sensitivity requires the bias current be constant and independent from the V_{DD}. For this reason, the bias of the differential amplifier is derived to be a multiple of the fixed current of the self-bias source.

Also, the dimension of the differential amplifier is in a way that most of the supply voltage and its variation drops on the NMOS active load. So, variation of the drain-source voltage of M_{13} is very small leading to a very small channel length modulation effect on the current mirror ratio. Furthermore, the channel length of transistors M_{14} and M_{15} should be large to reduce the channel length modulation effect [16].

The PSNR of the series regulator can be obtained as follows [16]

$$\frac{\Delta V_{reg}}{\Delta V_{DD}} = \frac{\dfrac{R_L \| r_{o18}}{1 + gm_{18}R_L + R_L / r_{o18}}}{1 + \dfrac{r_{o15} \| r_{o17}}{2} gm_{15}} \cong \frac{2}{gm_{15}(r_{o15} \| r_{o17})} \frac{1}{gm_{18} r_{o18}} \qquad \text{(Eq. 3.31)}$$

To reduce the variation of V_{reg}, the transistor M_{18} should have a large channel width to increase the amount of $gm_{18}.r_{o18}$. The PSNR of the voltage regulator as a function frequency is shown in Figure 3.22.

Stability is also a critical aspect for such kind of circuits, especially in the case of small load currents when the pole associated with the output node, given by gm_{18}/C_{load}, could become comparable with the pole at the output of the differential amplifier. As a

consequence, frequency compensation is required and is obtained by placing capacitor C_{comp} at the output of the differential amplifier.

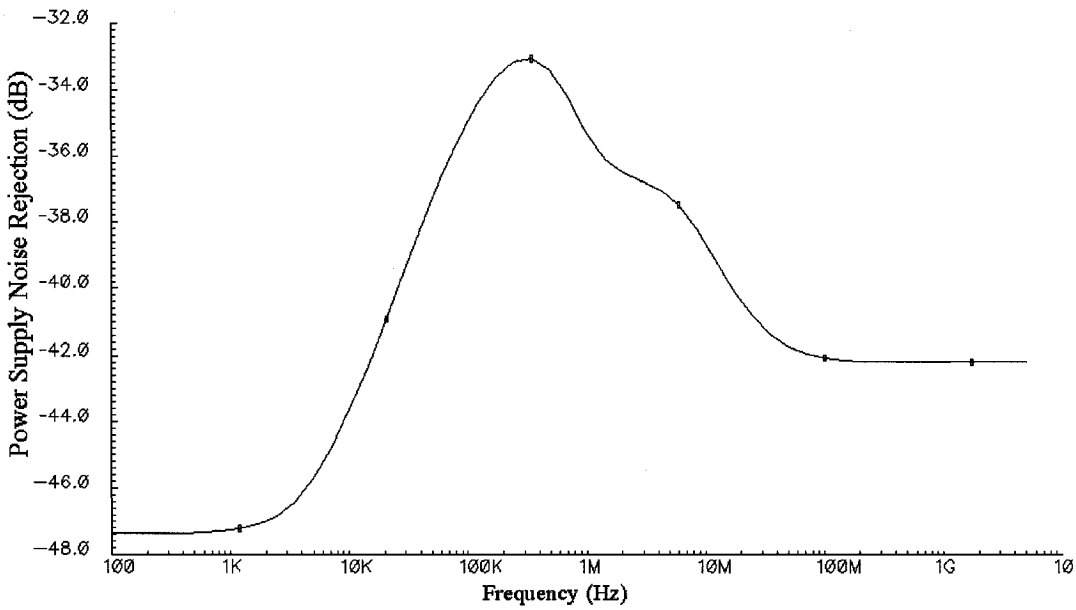


Figure 3.22. The PSNR of the regulator

The output voltage of the positive (negative) series regulator circuit is 500mV (-500mV). The positive output of the voltage regulator as a function of temperature is shown in Figure 3.23. As can be seen in Figure 3.23, the output voltage increases by rising the temperature. The reason is that the reference current and V_{ds} of diode connected transistors and consequently the reference voltage of regulator increase with the temperature. To reduce the temperature effect on the output voltage, the circuit of Figure 3.24 can be used.

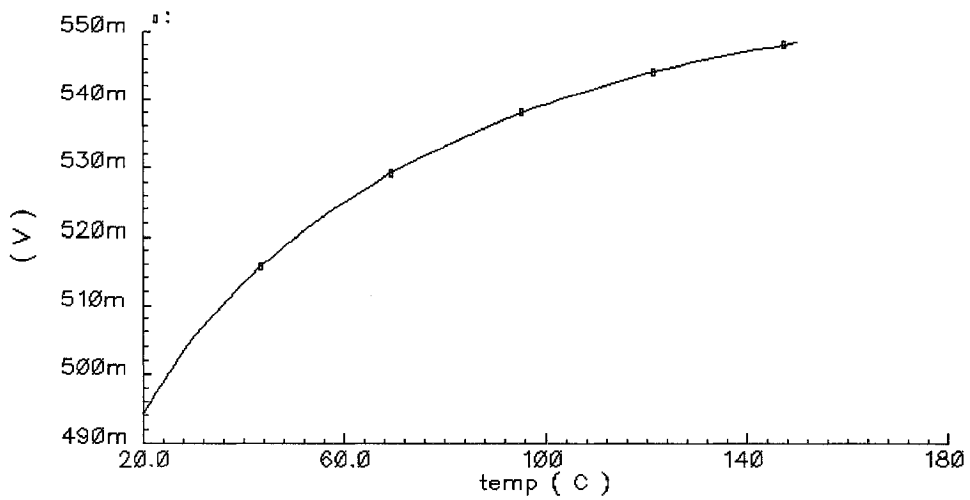


Figure 3.23. The positive output of the voltage regulator as a function of temperature

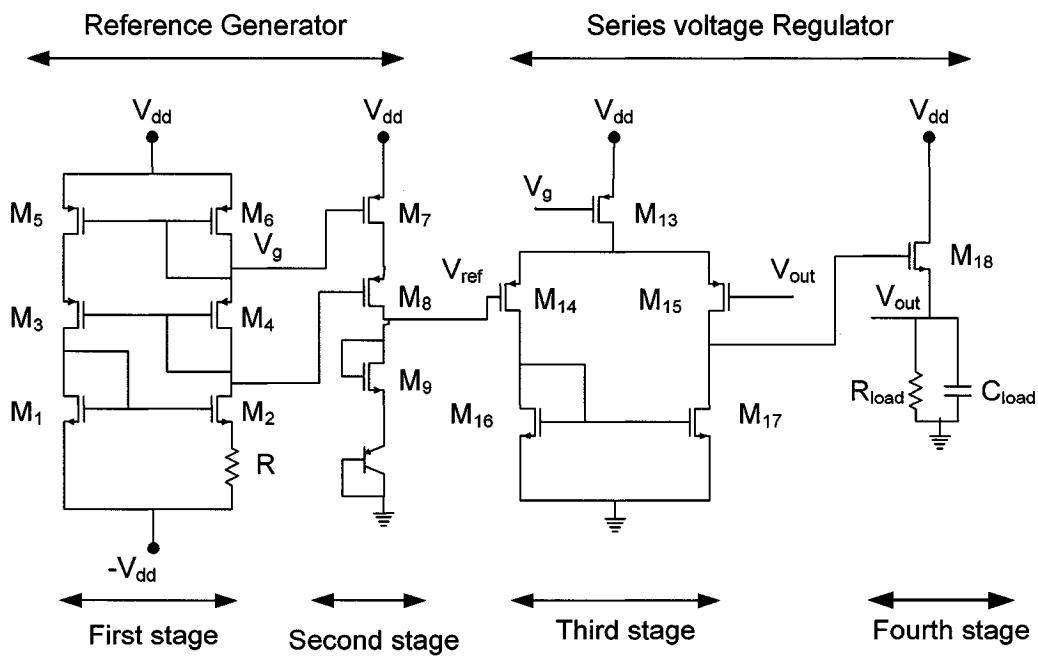


Figure 3.24. Circuit of less-temperature sensitive voltage regulator

In Figure 3.24, a combination of PNP and MOS diodes are used as the reference voltage generator. Since the temperature coefficient of a PN junction is negative, it will cancel the positive temperature coefficient of the current source and the diode connected transistor. The temperature coefficient of such circuit is shown in Figure 3.25. By using circuit of Figure 3.24, the temperature coefficient decreases to .07mV/C.

The regulator circuit for the negative part of the rectifier is the same as for the positive one, but the type of transistors in the diode ladder and series voltage regulator are changed. The layout of the positive part of the voltage regulator is shown in Figure 3.26.

The component values of the voltage regulator circuit are presented in Table 3.5. The voltage regulator characteristics are listed in Table 3.6.

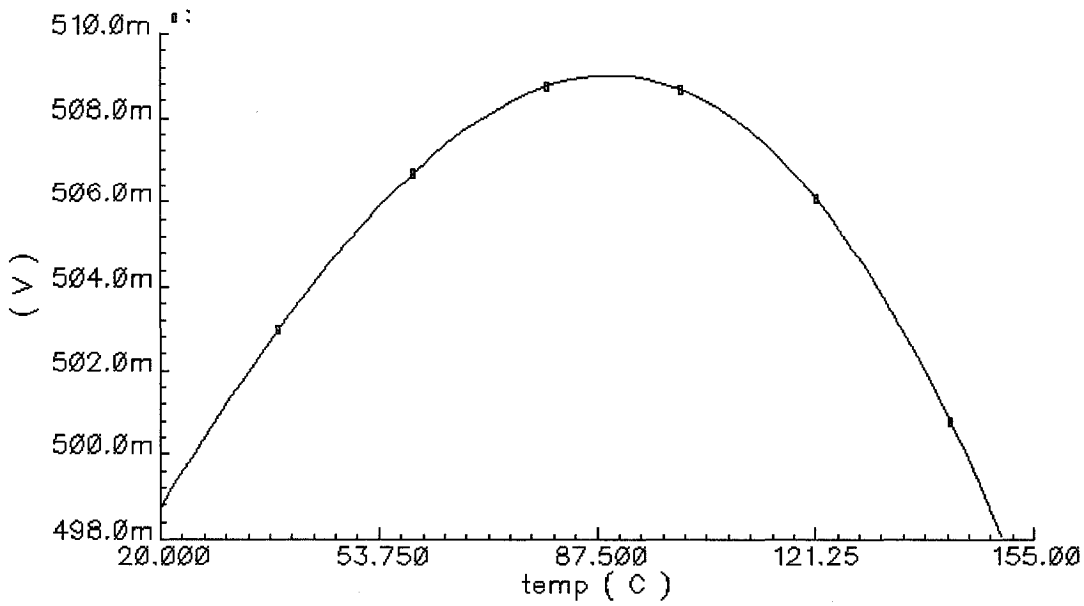


Figure 3.25. The output voltage of less-temperature sensitive voltage regulator as a function of temperature

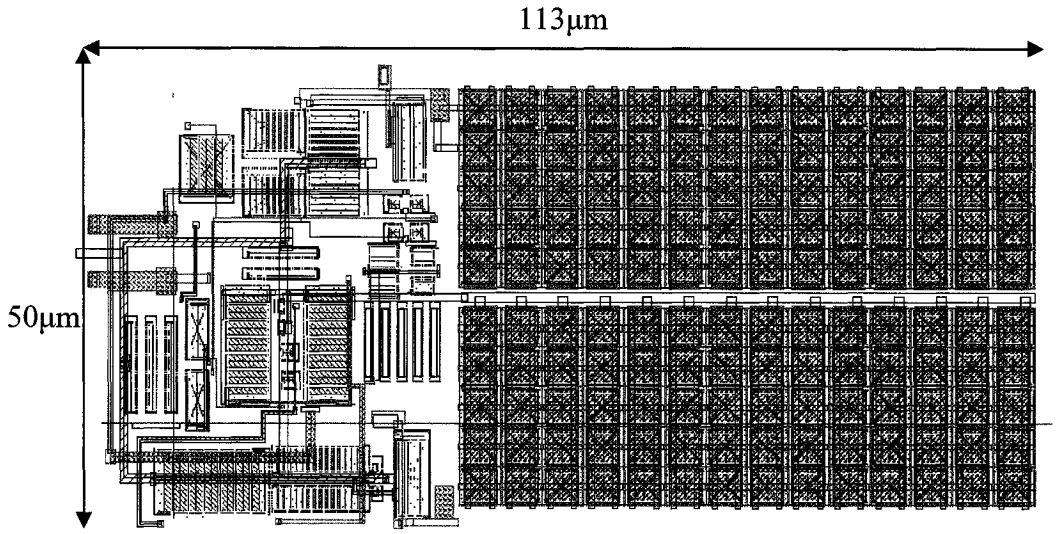


Figure 3.26. Layout of the positive part of regulator circuit

Table 3.5. The component values of the regulator circuit

M_1	NMOSLVT, 7μm/.26μm, No. of Fingers=3
M_2	NMOSLVT, 16μm/.26μm, No. of Fingers=5
M_3-M_4-M_5-M_6	PMOS, 1μm/1.04μm, No. of Fingers=1
M_7-M_8	PMOS, 6μm/1.56μm, No. of Fingers=1
M_9-M_{10}-M_{11}-M_{12}	PMOSHVT, 10μm/.13μm, No. of Fingers=1
M_{13}	PMOS, 20μm/1.56μm, No. of Fingers=3
M_{14}-M_{15}	PMOS, 40μm/.39μm, No. of Fingers=9
M_{16}-M_{17}	NMOS, 40μm/.39μm, No. of Fingers=7
M_{18}	NMOSLVT, 60μm/.13μm, No. of Fingers=7
R	20KΩ

Table 3.6. Regulator parameters

Output voltage	Power	PSNR	Temperature coefficient
±500mV	602nw	-32dB to -48dB	.38mV/C

3.2 Demodulator

The block diagram of the demodulator part was shown in Figure 2.12. The input to the demodulator is a PWM signal which is ASK modulated. The bit period of the PWM signal is 16μsec and the zero part of the bit for "zero" and "one" levels are 8μsec and 4μsec, respectively. In the demodulator section, the envelope of the PWM signal is extracted using an envelope detector. The Schmitt trigger then produces a constant envelope PWM signal ready for detection. The integrator and comparator measure the duration of each pulse and decide whether the pulse is "zero" or "one". A reset circuit denotes the arrival of the new bit and resets the integrator and comparator circuits.

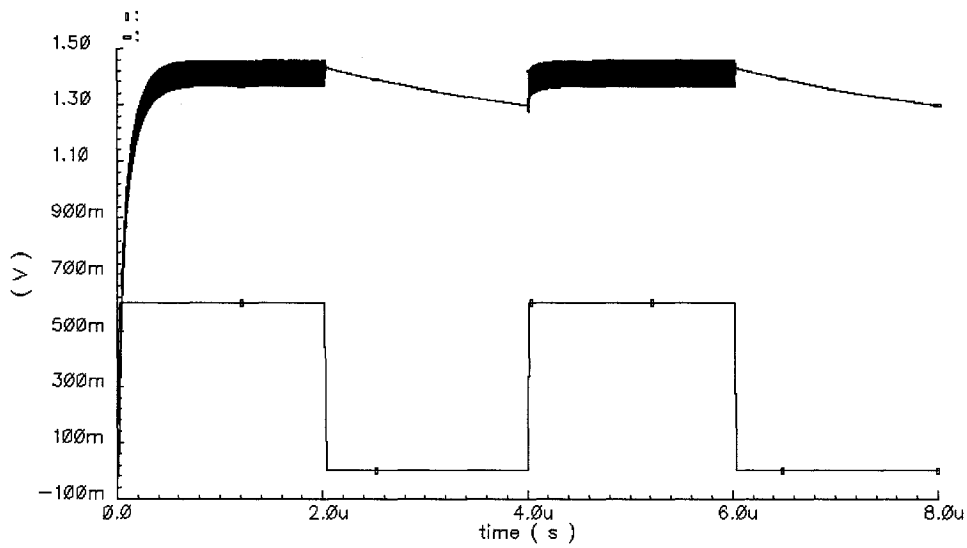
The operation of different blocks of demodulator and their simulation results are described in this section.

3.2.1 Envelope Detector

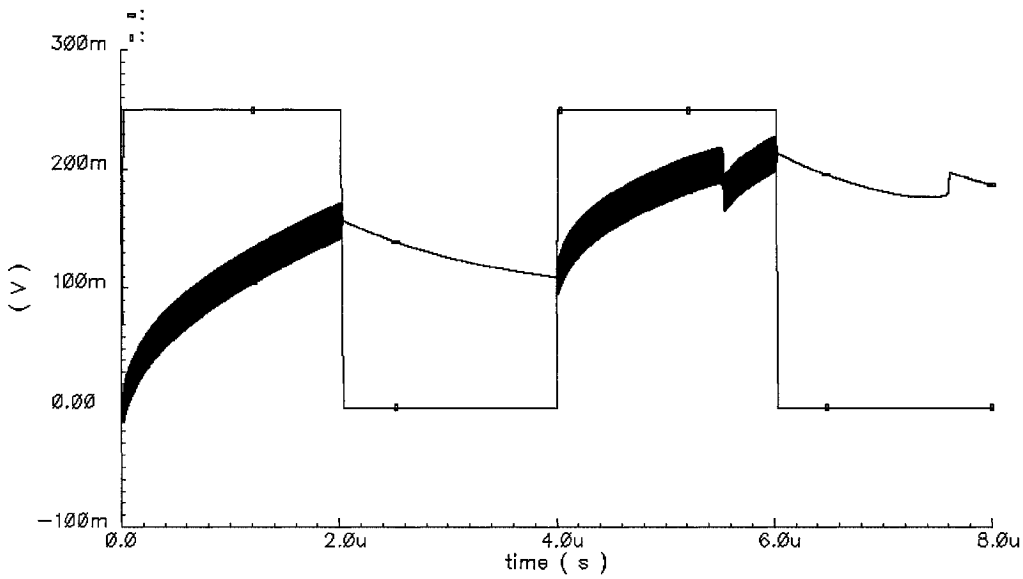
As discussed previously the envelope detector is the first block in the PWM demodulator which is followed by a hysteresis circuit. The envelope detector structure is similar to the rectifier but with different sizing of transistors and capacitors to optimize a different goal. The main problem with using only a rectifier circuit as an envelope detector is the difference in the tracking time constant between the minimum and

maximum input voltages. The input range of the RF voltage is from approximately 250mV to one volt. If the envelope detector is designed in such a way that it follows the input envelope with the required precision of the 250mV case, it will fail to track a one-to-zero transition in the case of the maximum input envelope. This is because, with the designed high gain in the envelope detector rectifier, the maximum voltage of the one state would be too high to be brought down to the threshold within the time gap for the zero state. On the other hand if the design is in such a way that in the maximum case the one state does not charge up too high so that it could be brought down easily, then in the minimum voltage case we will have a problem in the zero-to-one transition. This is because the rectifier is designed with a lower gain and this would not be enough to bring up the voltage in a zero-to-one transition with the minimum input voltage. The transition problems for two case of high and low voltage gain are shown in Figure 3.27.a and b. In Figure 3.27.a, the high gain voltage multiplier is used and as described above, with the case of high input voltage, the one-to-zero transition can not reach the zero threshold of the hysteresis circuit. On the other hand, by using a low gain voltage multiplier, such as in Figure 3.27.b, the zero-to-one transition would be difficult in the case of minimum input voltage.

To solve this issue the circuit has been designed for the minimum input voltage and uses a negative feedback loop to ensure that the maximum voltage does not go too high for the maximum voltage case. The envelope detector circuit is shown in Figure 3.28. The low pass filter helps "clean" the signal of any HF variations. Then the diode ladder section is used to create control voltages in proportion to the input voltage. This ladder



(a)



(b)

Figure 3.27. Input voltage envelope and output voltage of the envelope detector for (a) high input voltage and high gain multiplier (b) low input voltage and low gain multiplier

network controls the gate voltages of clamping devices. At the low input voltages, points A and B will have low voltages and would not be able to turn on the clamp devices. This ensures that the performance of the envelope detector is not compromised in the low voltage case. At medium voltage values, voltage A will be high enough to turn on M_A and this will limit the input to the desired value. Transistor M_B however will remain off in this case. At high input voltages, both V_A and V_B will exceed the turn on voltages of the clamp devices and this will ensure that the input is limited to the desired voltage once again. The devices are sized appropriately to be able to clamp the voltage accordingly. The number of control voltages could be increased to expand the domain of the input range that the envelope detector operates in.

The outputs of envelope detector for two cases of "one" and "zero" inputs with high input voltage are shown in Figure 3.29.a and 3.29.b. The layout of the envelope detector circuit is shown in Figure 3.30. Also, the component values of envelope detector are presented in Table 3.7.

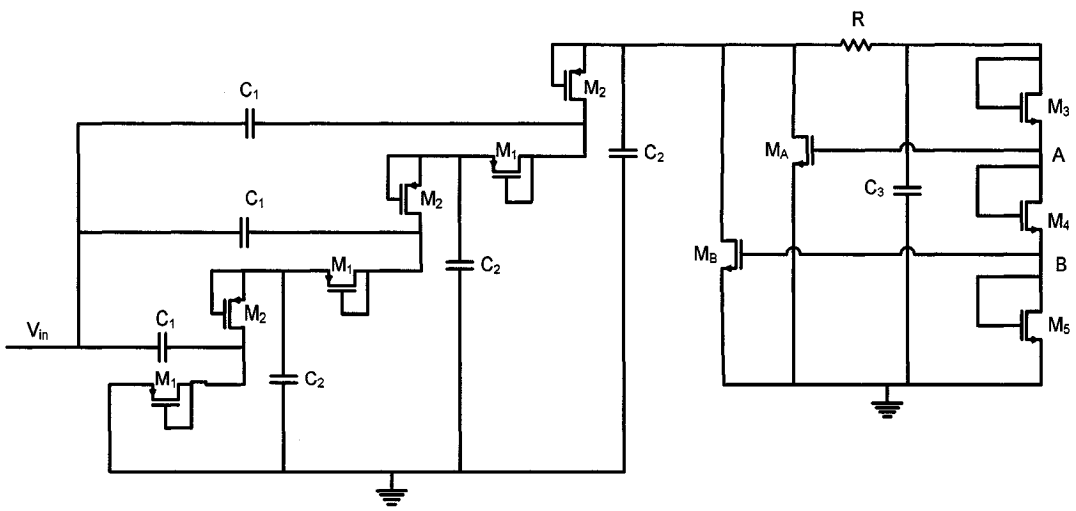
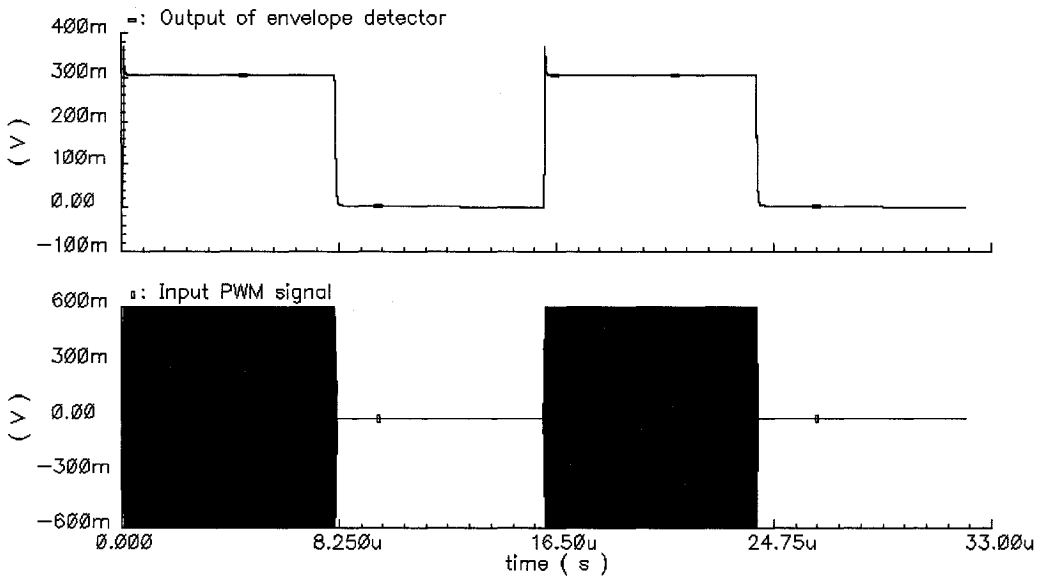
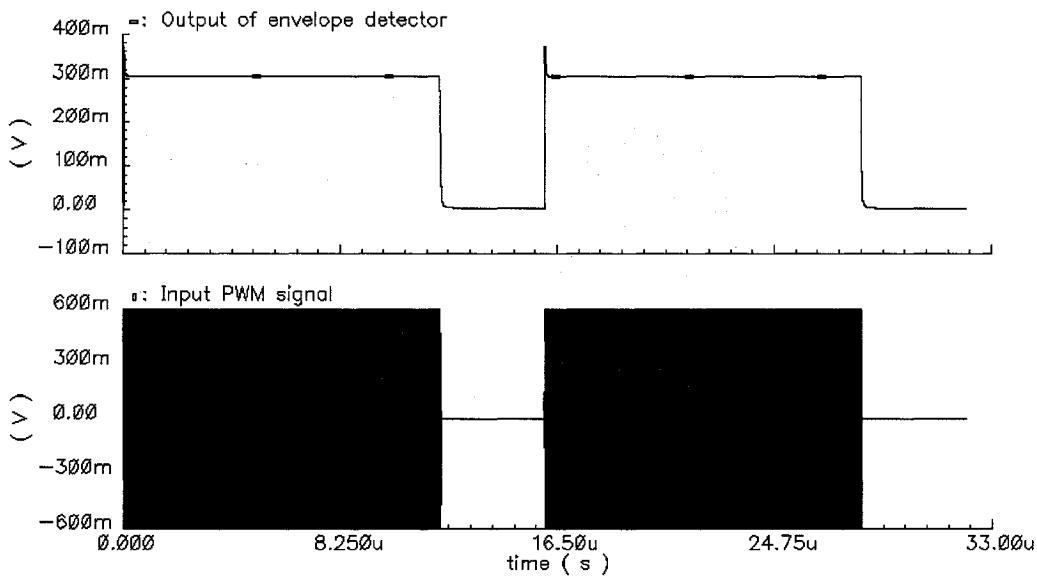


Figure 3.28. The envelope detector circuit



(a)



(b)

Figure 3.29. Input PWM signal and output of envelope detector for (a) "zero" input (b) "one" input

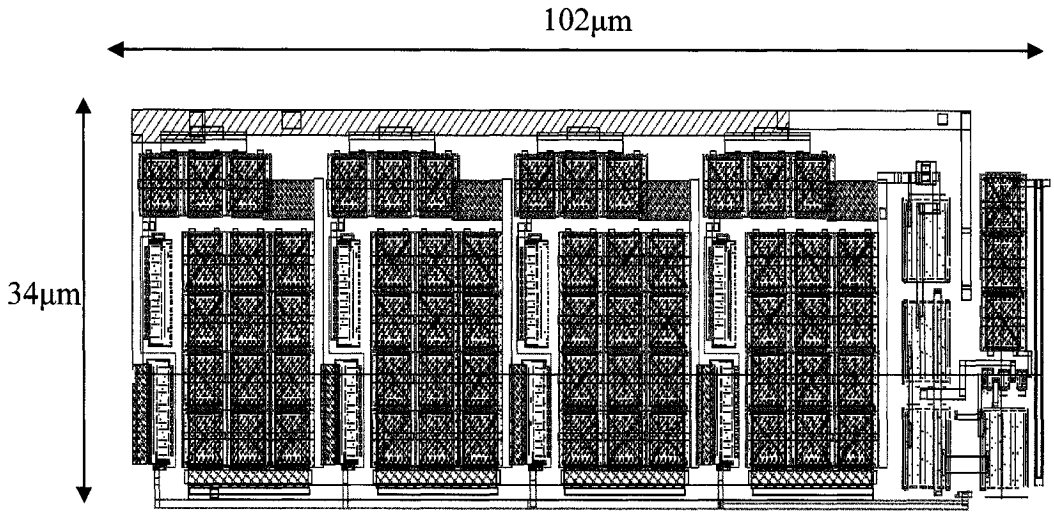


Figure 3.30. Envelope detector layout

Table 3.7. The component values of the envelope detector circuit

M_1-M_2	PMOSLVT, 15μm/.13μm, No. of Fingers=15
M_3-M_4-M_5	NMOSLVT, 1μm/.13μm, No. of Fingers=1
M_A	NMOSHVT, 20μm/.13μm, No. of Fingers=5
M_B	NMOSHVT, 30μm/.13μm, No. of Fingers=10
C_1	800fF
C_2-C_3	200fF
R	15kΩ

3.2.2 Schmitt Trigger

A Schmitt trigger is a comparator circuit that incorporates positive feedback. When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. The input and output signal of a Schmitt trigger circuit are shown in Figure 3.31. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called hysteresis, and implies that the schmitt trigger has some memory.

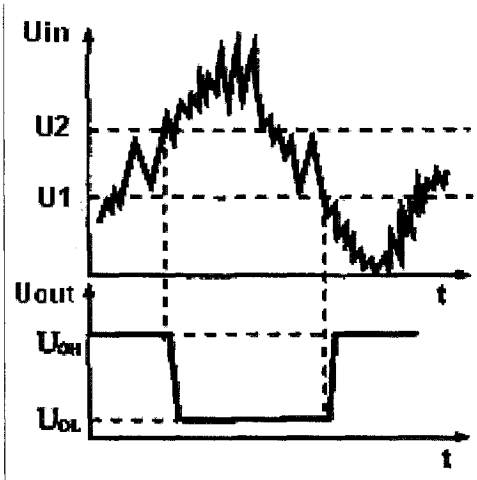


Figure 3.31. Input and output waveform of a schmitt trigger circuit

The benefit of a Schmitt trigger over a circuit with only a single input threshold is greater stability (noise immunity). With only one input threshold, a noisy input signal near that threshold could cause the output to switch rapidly back and forth from noise alone. A noisy Schmitt Trigger input signal near one threshold can cause only one switch

in output value, after which it would have to move to the other threshold in order to cause another switch.

The standard CMOS Schmitt Trigger circuit design is shown in Figure 3.32 [21]. The operation of the Schmitt trigger circuit is as follows. Initially, V_{in}=0 V, the two stacked PMOS (M_1 and M_2) will be ON. Hence V_{out1}=V_{DD}. When V_{in} rises to $V_{th,N}$, M_4 is ON but M_3 is still OFF since M_6 is ON and source voltage of M_3 is V_{DD}. Now M_4 and M_6 form an inverting NMOS amplifier. Thus, source voltage of M_3 is falling with increasing V_{in}. When source voltage of M_3 drops to $V_{th,N}$, M_3 is ON. Now both M_3 and M_4 are ON, V_{out1} approaches 0V rapidly and M_6 becomes OFF. When V_{in} approaches V_{DD}, the two stacked NMOS (M_3 and M_4) will be ON. Hence V_{out1}=0. When V_{in} falls to $V_{th,P}$, M_1 is ON but M_2 is OFF since M_5 is ON and source voltage of M_2 is 0V. Now M_1 and M_5 form an inverting PMOS amplifier. Thus, source voltage of M_2 is rising with decreasing V_{in}. When source voltage of M_2 rises to $V_{th,P}$, M_2 is ON. Now both M_1 and M_2 are ON, V_{out1} approaches V_{DD} rapidly and M_5 turns OFF. The voltage transfer characteristic exhibits a typical hysteresis behavior as shown in Figure 3.33.

In Figure 3.33, V_{OH} is the maximum output voltage and V_{OL} is the minimum output voltage. V_{hl} is the input voltage at which output switches from V_{OH} to V_{OL}. V_{lh} is the input voltage at which output switches from V_{OL} to V_{OH}. V_{hw} is called the hysteresis width. The voltages V_{hl}, V_{lh} and V_{hw} are given by [22]

$$V_{hl} = \frac{V_{DD} + RV_{th,N}}{R+1} \qquad \text{(Eq. 3.32)}$$

$$V_{lh} = \frac{RV_{th,P}}{R+1} \qquad \text{(Eq. 3.33)}$$

$$V_{hw} = V_{hl} - V_{lh} = \frac{V_{DD} + R(V_{th,N} - |V_{th,P}|)}{R+1} \qquad \text{(Eq. 3.34)}$$

Where the ratio R is

$$R = \sqrt{\frac{\beta_n}{\beta_p}} \qquad \text{(Eq. 3.35)}$$

Where β_n and β_p are NMOS and PMOS transconductance parameters.

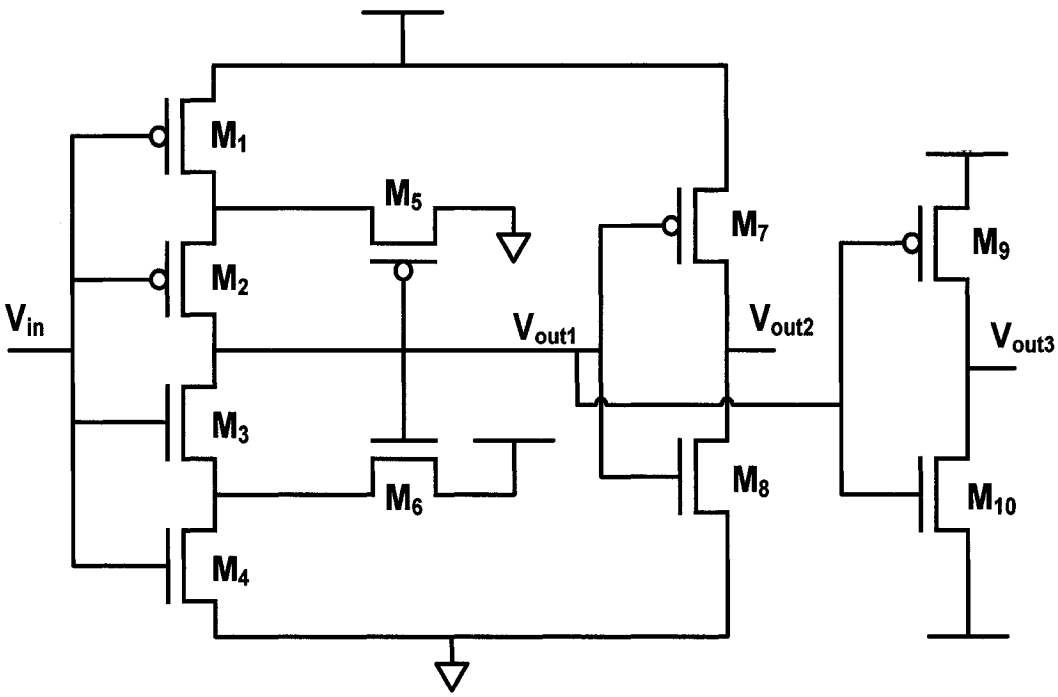


Figure 3.32. A standard CMOS Schmitt Trigger circuit

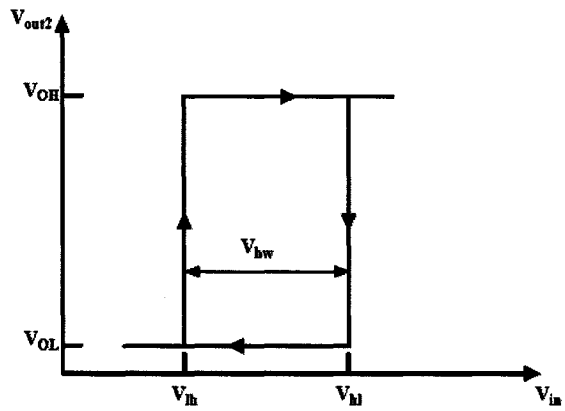


Figure 3.33. CMOS Schmitt Trigger voltage transfer characteristic

The high-to-low and low-to-high thresholds can alter by changing the W_1/W_5 and W_3/W_6 ratios. By increasing W_1/W_5, V_{hl} increases because the transistor M_1 will turn ON faster. Also, increasing W_3/W_6 decreases V_{lh}. The high-to-low and low-to high thresholds as a function of W_1/W_5 and W_3/W_6 are shown in Figures 3.34 and 3.35.

The Schmitt trigger circuit has two outputs: V_{out2} which is unipolar and between 0 and 500mV and V_{out3} which is bipolar and between -500mV and 500mV. The input of the Schmitt trigger circuit (output of envelope detector) and its outputs for the "one" and "zero" input signals are shown in Figure 3.36.a and 3.36.b. The layout of Schmitt trigger circuit is shown in Figure 3.37.

The component values of the Schmitt trigger circuit are presented in Table 3.8. The Schmitt trigger characteristics are listed in Table 3.9.

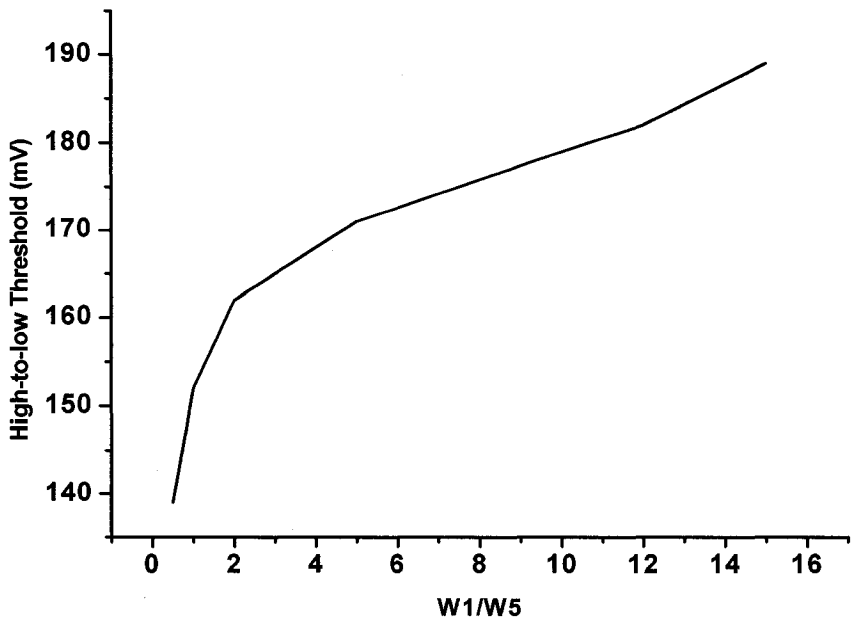


Figure 3.34. High-to-low voltage threshold as a function of W_1/W_5

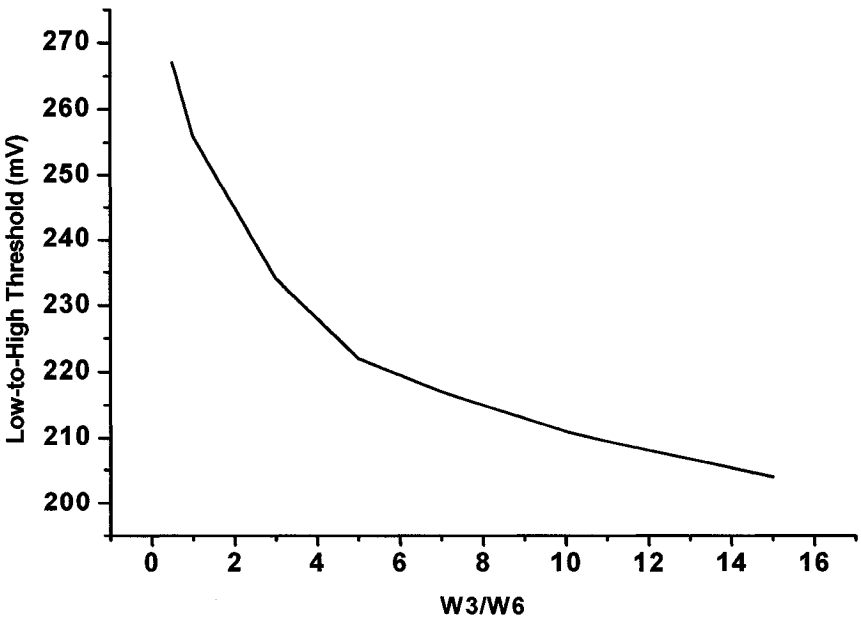
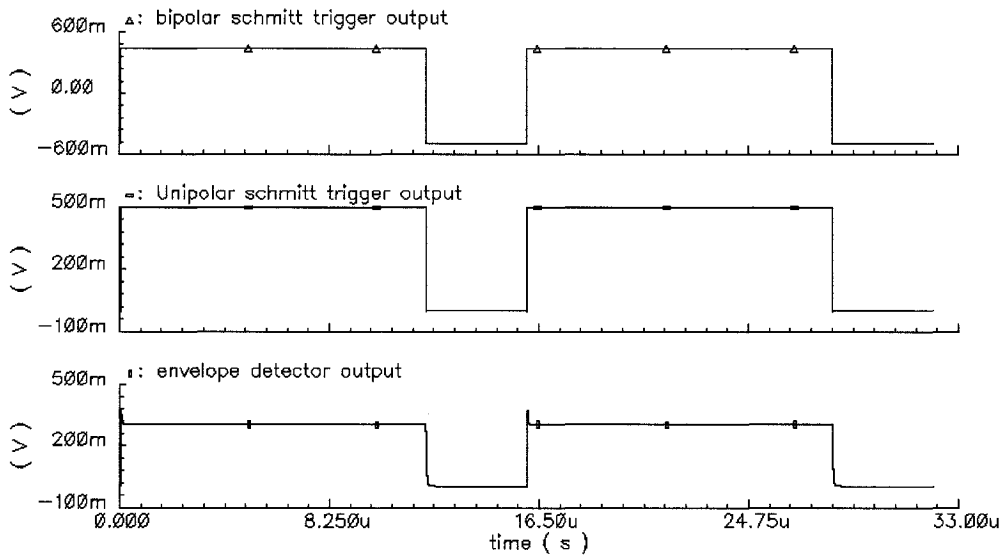
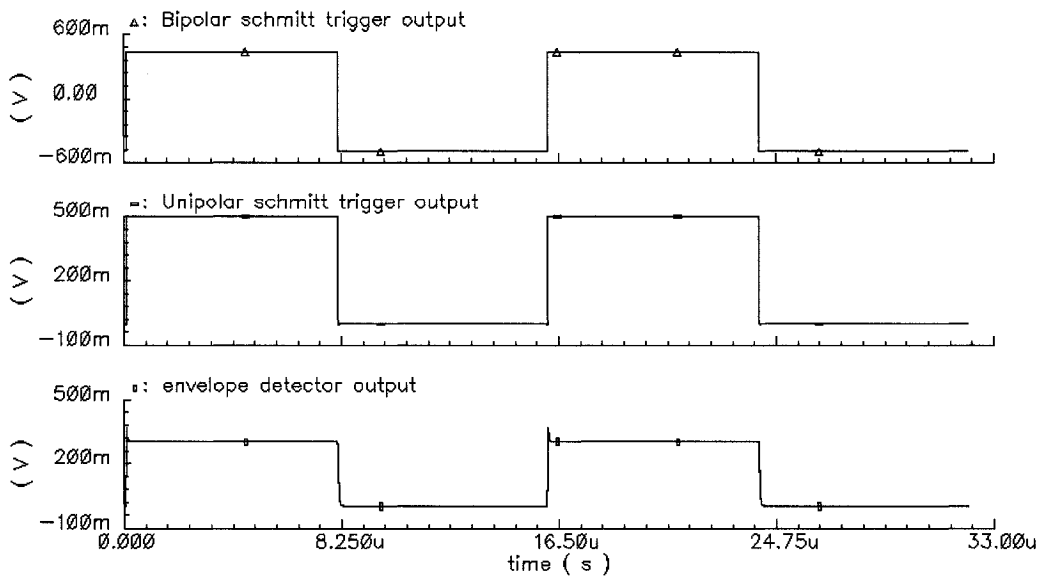


Figure 3.35. Low-to-high voltage threshold as a function of W_3/W_6



(a)



(b)

Figure 3.36. Input and output signals of Schmitt trigger circuit for (a) "zero" input (b) "one" input

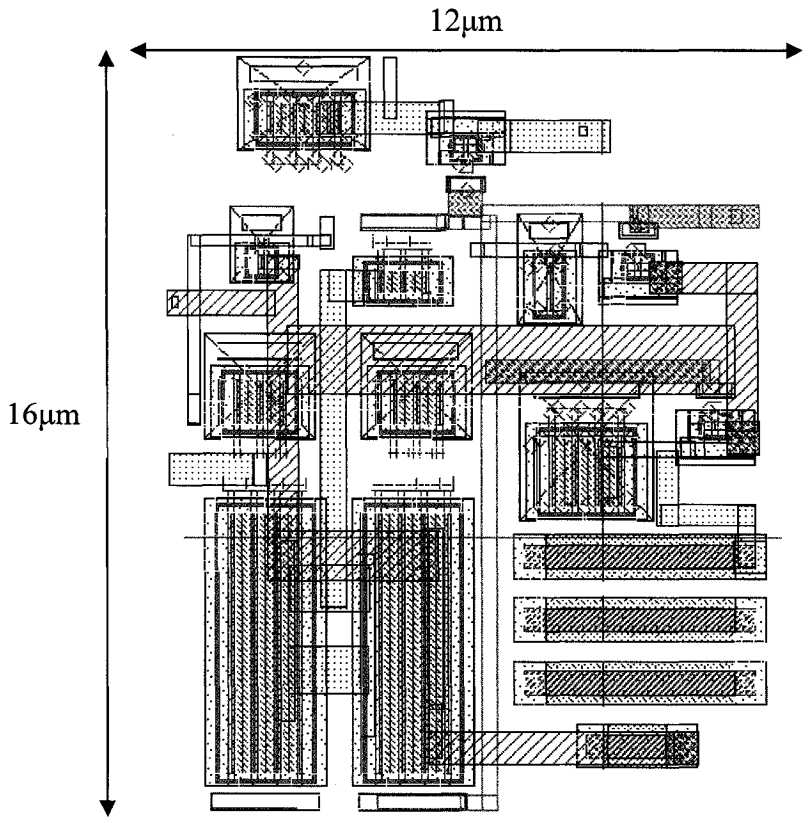


Figure 3.37. Schmitt Trigger layout

Table 3.8. The component values of the Schmitt trigger circuit

M_1-M_2-M_9	PMOSLVT, 3μm/.13μm, No. of Fingers=3
M_3-M_4	NMOSLVT, 22μm/.13μm, No. of Fingers=4
M_5-M_7	PMOSLVT, .3μm/.13μm, No. of Fingers=1
M_6	NMOSLVT, 1.5μm/.13μm, No. of Fingers=3
M_8-M_{10}	NMOSLVT, .15μm/.13μm, No. of Fingers=1

Table 3.9. Schmitt trigger parameters

Power Consumption	High-to-Low Threshold	Low-to-High Threshold	Hysteresis Width
95nW	172mV	204mV	32mV

3.2.3 Integrator

Figure 3.38 shows an integrator circuit which is implemented using an op-amp. The resistor R_1 is used to develop a current I that is proportional to the input voltage. This current flows into the capacitor C, whose voltage is proportional to the integral of the current I with respect to the time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time. The output voltage of the integrator is as follows [17]

$$V_{out}(t) = -\frac{1}{R_1 C}\int_0^t V_{in}(\tau)d\tau + K \qquad \text{(Eq. 3.36)}$$

Where K is the output voltage at the start time (t=0)

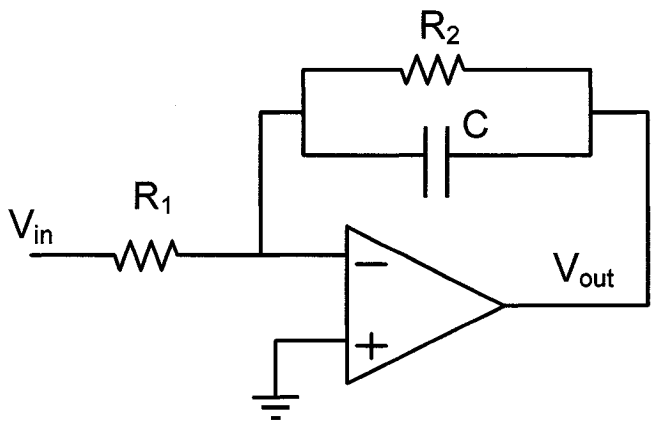


Figure 3.38. Integrator circuit

When V_{in}=0, the integrator works as an open loop amplifier. This is because the capacitor C acts as an open circuit to the input offset voltage. This input offset voltage and the part of the input current charging capacitor C produce the error voltage at the output of the integrator. Therefore in an integrator, to reduce the error voltage at the output, a resistor R_2 is connected across the feedback capacitor C. Thus R_2 limits the low frequency gain and hence minimizes the variations in the output voltage. The addition of the resistor also corrects the stability and low frequency roll-off problems. Considering the frequency response, the limiting frequencies are defined as follows. The frequency at which gain is 0dB is given by

$$f_b = \frac{1}{2\pi R_1 C} \qquad \text{(Eq. 3.37)}$$

And the gain limiting frequency is given by

$$f_a = \frac{1}{2\pi R_2 C} \qquad \text{(Eq. 3.38)}$$

The circuit acts as an integrator in the frequency range f_a to f_b. The value of f_a and in turn R_1C and R_2C values should be selected such that $f_a<f_b$. So the resistor R_2 is much bigger than resistor R_1.

The most important part of an integrator circuitry is its op-amp circuit. The op-amp parameters that are important in the integrator circuit are gain, frequency response, input resistance, output swing and power consumption. More gain and larger input impedance make the op-amp closer to an ideal one. Also the first pole of op-amp should be greater than the input voltage frequency to avoid the instability in the feedback loop. The output

swing of the op-amp define the range of the input voltage for which the integrator works correctly (does not go to saturation regime). Furthermore, because of the fluctuation in the V_{DD} voltage during the reception of the PWM signal, the PSRR of the op-amp is another issue in RFID systems. The following section will discuss the op-amp structure which is used in this project and also its important parameters.

3.2.3.1 Op-amp

The schematic of the two-stage op-amp which is used in the integrator is shown in Figure 3.39. The circuit provides good voltage gain, output swing and sufficient bandwidth and PSRR.

To make the power consumption of the op-amp low, the op-amp is fed through a low-power current source which produces a 10nA current. The current source is similar to the one that is used in the regulator circuit.

The overall voltage gain of the amplifier is given by [17]

$$A_v = -g_{m6}(r_{o7} \parallel r_{o9})g_{m11}(r_{o11} \parallel r_{o10}) \qquad \text{(Eq. 3.39)}$$

Where g_m is the transconductance and r_o is the output resistance of the transistor.

To increase the gain, the output resistance of the transistors should increase. Two ways of increasing the output resistance are larger channel length and smaller bias current. Decreasing the bias current has less effect because it decreases the g_m. So the former is the solution for increasing the r_o.

The first pole of the op-amp is at the output of the first stage. The dominate pole of the system is as follows

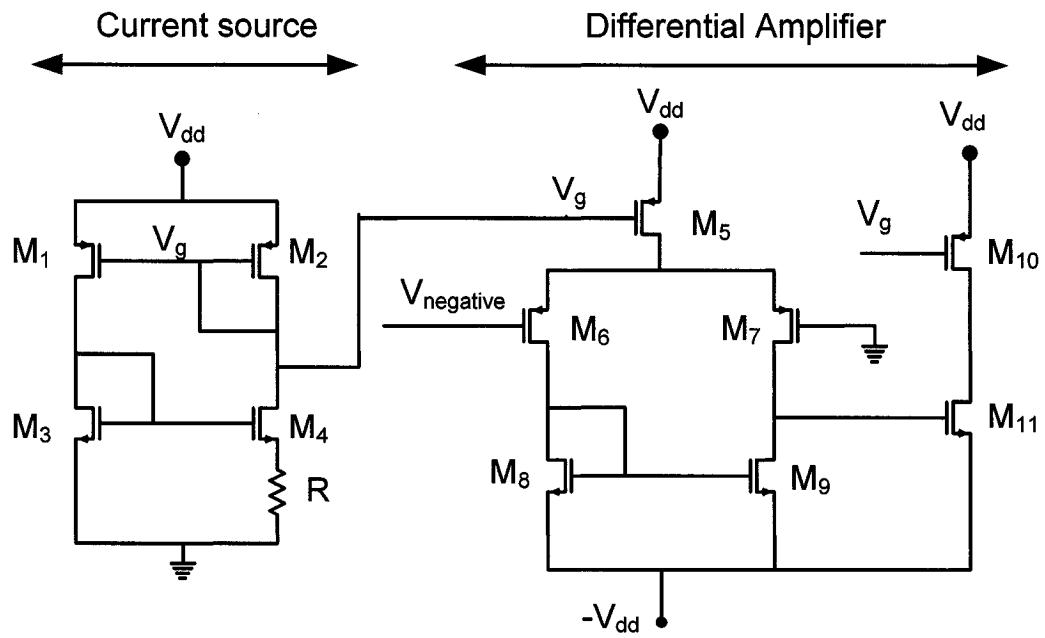


Figure 3.39. The schematic of the two-stage op-amp circuit used in integrator

$$P_1 \approx \frac{1}{2\pi(r_{o7} \parallel r_{o9})(C_{gs11} + C_{gd11}(1 + g_{m11}(r_{o11} \parallel r_{o10})) + C_{gd7} + C_{gd9})} \qquad \text{(Eq. 3.40)}$$

To increase the BW, larger bias current is needed. The gain and frequency response of the op-amp is shown in Figure 3.40.

The output swing is defined by the range of the output voltage for which all transistors operate in the active region and the gain is approximately constant and given by (3.39). From Figure 51, M_{11} operates in the triode region if the output voltage is less than V_{ov11}-(-V_{DD}) and M_{10} operates in the triode region if the output is more than V_{DD}-$|V_{ov10}|$. Therefore the output swing is [17]

$$V_{ov11} + V_{DD} \le V_{out} \le V_{DD} - |V_{ov10}| \qquad \text{(Eq. 3.41)}$$

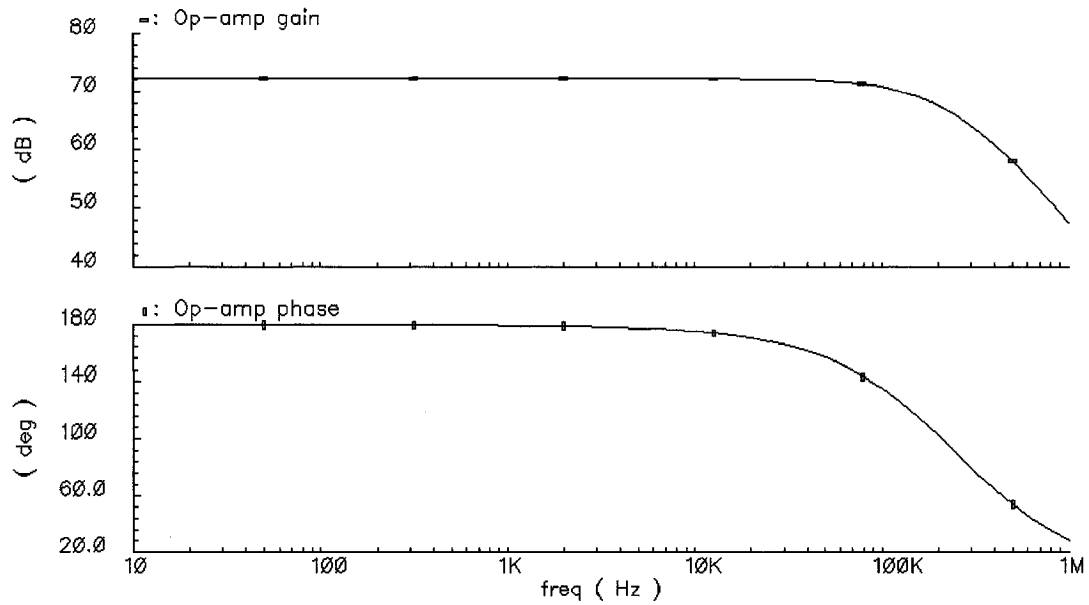


Figure 3.40. Gain and phase response of the op-amp as a function of frequency

The positive voltage source PSRR can be obtained as follows [17]

$$PSRR^{+} = \left(\frac{\dfrac{r_{o11}}{r_{o11}+r_{o10}} - \dfrac{g_{m11}(r_{o10} \parallel r_{o11})}{2g_{m5}r_{o5}}}{A_v}\right)^{-1} \qquad \text{(Eq. 3.42)}$$

The positive PSRR goes toward infinity for low frequencies with perfect matching because the coupling from V_{DD} to the output from the first stage cancels that through the second stage. In reality, mismatch can increase the common-mode transconductance of the first stage disrupting the cancellation and decreasing the low frequency $PSRR^{+}$. The negative supply voltage PSRR is given by [17]

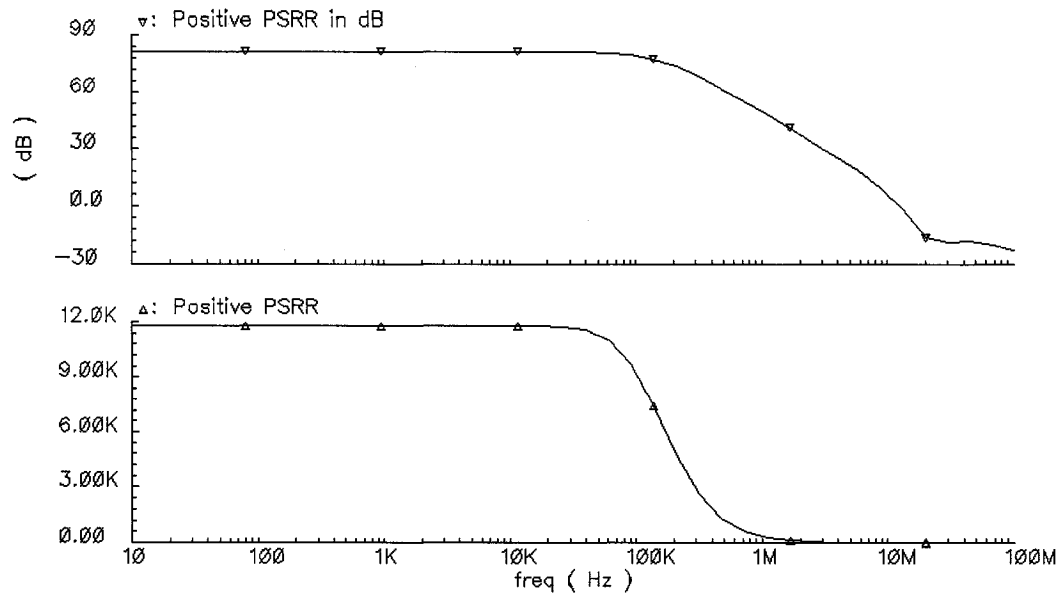
$$PSRR^{-} = \frac{A_v}{\frac{r_{o10}}{r_{o10} + r_{o11}}} \qquad \text{(Eq. 3.43)}$$

The positive PSRR remains relatively constant with increasing frequency but the negative PSRR decreases with frequency and reaches unity at the frequency where $|A_v|=1$. The reason is that as the frequency increases, the impedance of the C_{gd11} decreases effectively shorting the gate of M_{11} to its drain. If the gate-source voltage on M_{11} is constant, the variation of the negative supply is fed directly to the output and the gain from the negative supply voltage to the output becomes one [17]. So by increasing the frequency, the A_v and consequently the negative PSRR decrease.

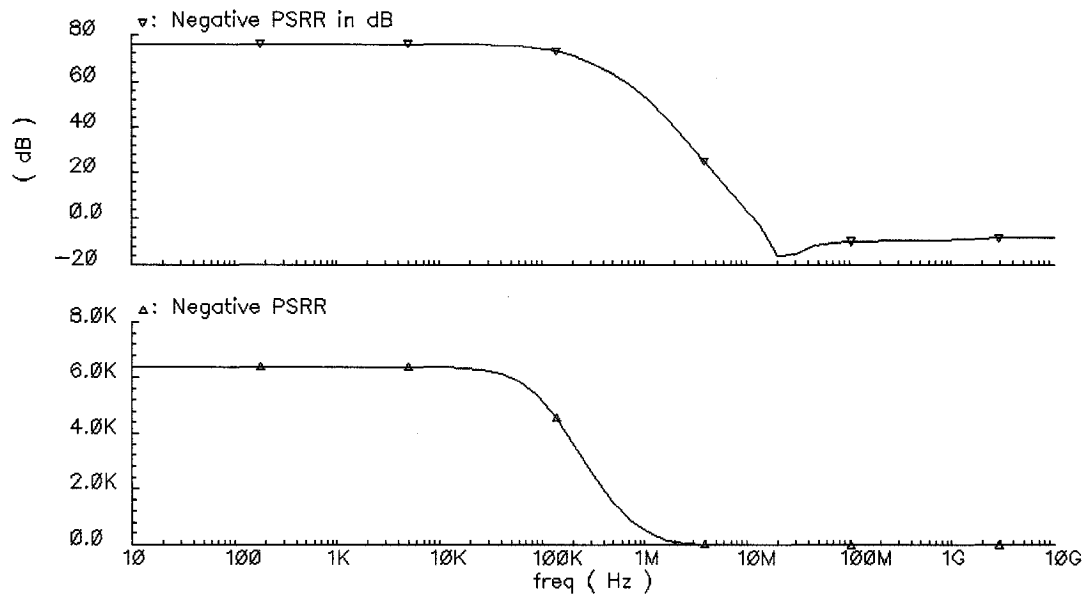
The positive and negative PSRR of the designed op-amp are shown in Figure 3.41.a and 3.41.b.

3.2.3.2 Integrator Simulation Results

The output of integrator will become saturated if the input signal is too high. For preventing this problem, the unipolar output of the Schmitt trigger circuit goes through a voltage divider which consists of two resistors. The output of the voltage divider is the same as the output of unipolar Schmitt trigger but with 50mV voltage swing instead of 500mV. Also for best result, the input of the integrator is the inverted version of the voltage divider circuit. The output of integrator circuit for two cases of "zero" and "one" inputs are shown in Figure 3.42.a and 3.42.b. The layout of Integrator circuit is shown in Figure 3.43.

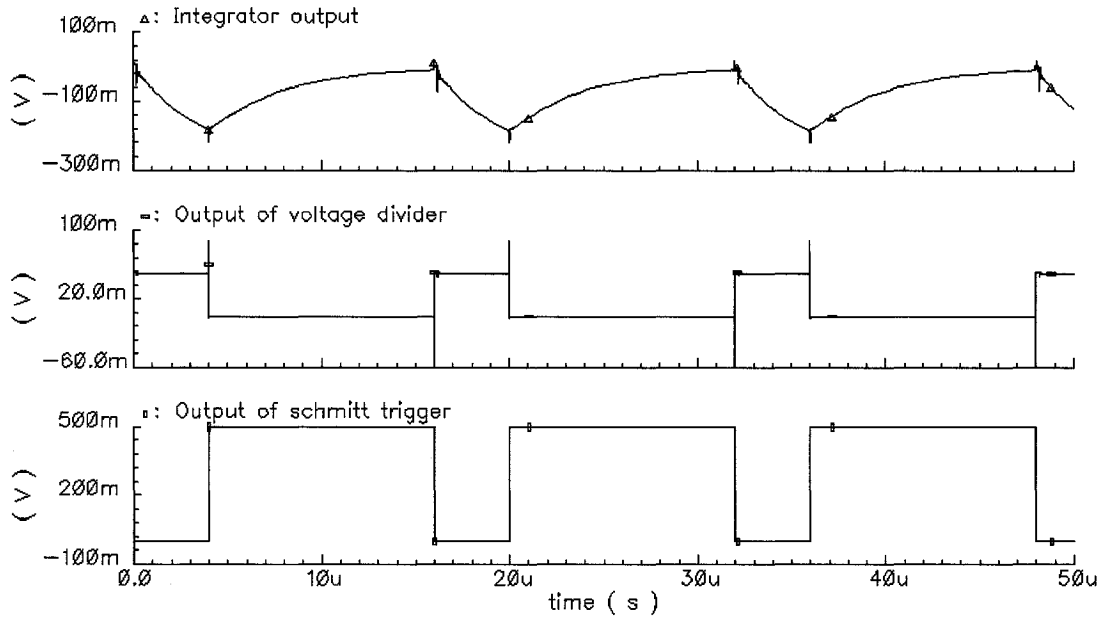


(a)

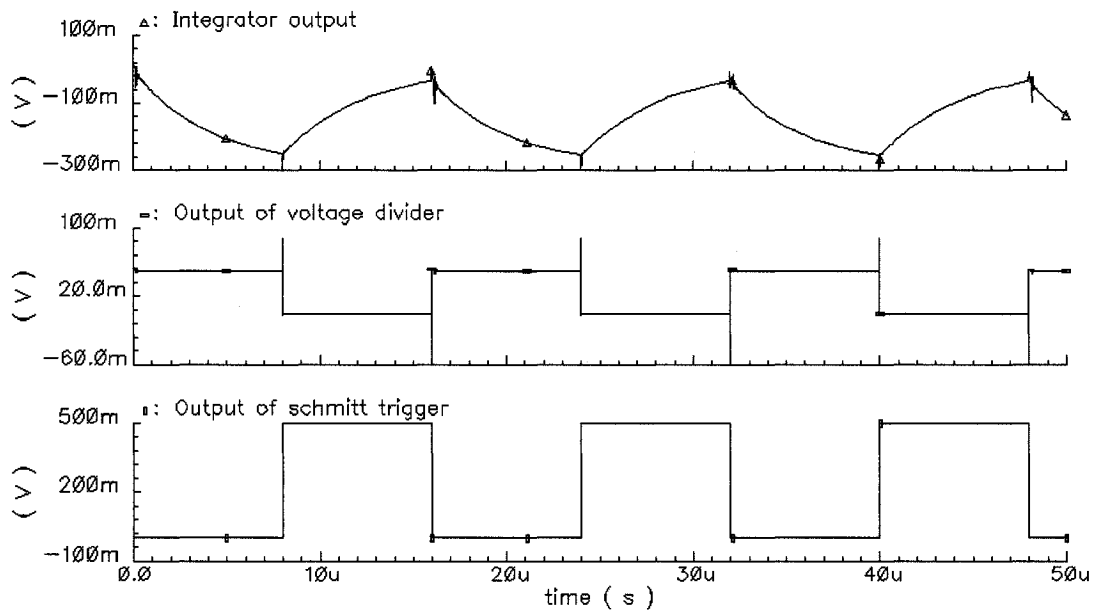


(b)

Figure 3.41. PSRR of the op-amp (a) positive PSRR (b) negative PSRR



(a)



(b)

Figure 3.42. Output of integrator circuit and voltage divider for (a) "one" input (b) "zero" input

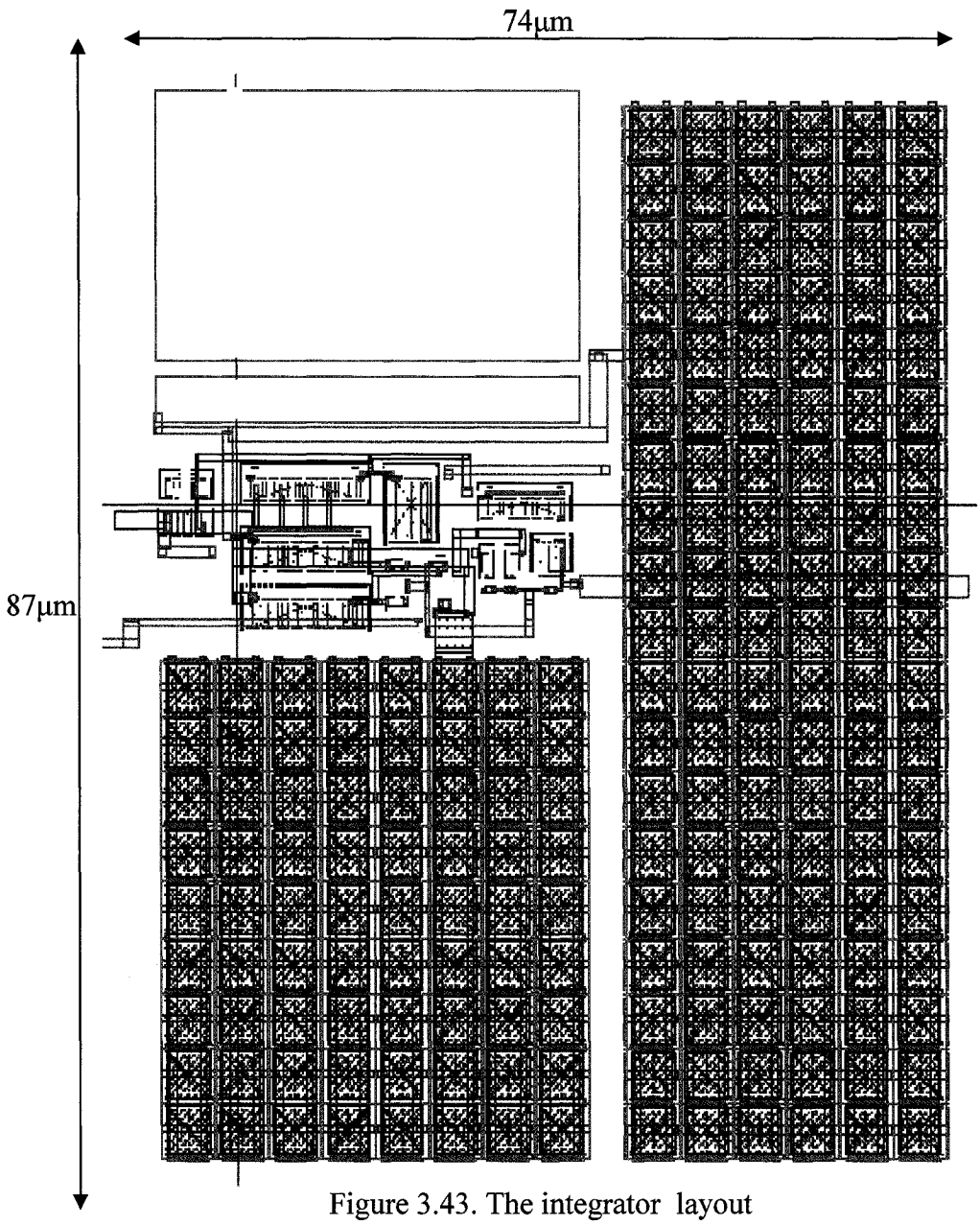


Figure 3.43. The integrator layout

The component values of the integrator circuit are presented in Table 3.10. The integrator characteristics are listed in Table 3.11.

Table 3.10. The component values of the integrator circuit

M_1-M_2	PMOS, 1μm/.78μm, No. of Fingers=1
M_3	NMOS, 8.5μm/.26μm, No. of Fingers=4
M_4	NMOS, 3.5μm/.13μm, No. of Fingers=2
M_5	PMOS, 15μm/.78μm, No. of Fingers=10
M_6-M_7	PMOS, 17μm/1.04μm, No. of Fingers=8
M_8-M_9	NMOS, .15μm/1.04μm, No. of Fingers=1
M_{10}	PMOS, 15μm/1.04μm, No. of Fingers=3
M_{11}	NMOS, .15μm/.52μm, No. of Fingers=1
R	3KΩ
R_1	100KΩ
R_2	600KΩ
C	8pF

Table 3.11. Integrator parameters

Power Consumption	Positive PSRR	Negative PSRR	Op-amp BW
248nW	85dB	76dB	12.8MHz

3.2.4 Reset Circuit

The output of the integrator circuit has to be sent to the comparator after each signal period (16μsec). For this reason there is a switch between the integrator output and the comparator input. The switch should be connected after each period for about 100-150nsec. This means that we need a circuit to generate a 100-150nsec pulse with the period of 16μsec. As we know, at the beginning of each period of the PWM signal there is a falling edge. So a narrow pulse should be generated at each falling edge of the input signal. Such a reset circuit is shown in Figure 3.44.

When the input signal of the reset circuit is high, the voltage at node B will be high too. The voltage at node A will be opposite to that of the input voltage so it becomes low and the output of the NOR gate will be low. In the transition from high to low, the voltage at node B follows the input voltage immediately but the voltage at node A remains high for some amount of time that is related to the propagation delay and the number of inverters. During this time, the voltage at node A keeps its previous state (low) and the output of NOR gate becomes high. After s specific time which takes the signal to propagate through, the voltage at node A becomes high so the output goes back to the low state. The width of the output pulse can be found as

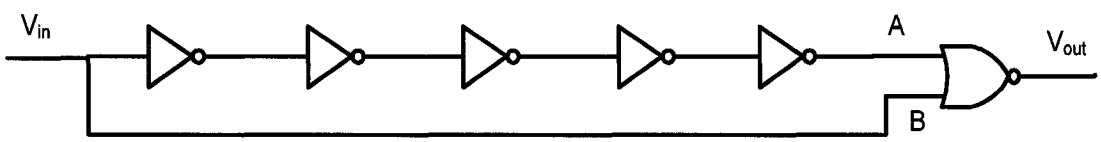


Figure 3.44. Schematic of the reset circuit

$$T_{reset,pulse} = N\tau_d \quad \text{(Eq. 3.44)}$$

Where N is the number of inverters and τ_d is the average delay of each inverter.

To control the delay of each inverter cell and also to control the power of the reset circuit, current-starved inverters are used instead of conventional inverters. One stage of the current-starved inverter is shown in Figure 3.45. The (W/L) of transistors M_1 and M_4 are minimized to decrease the current flowing in the inverter cell increasing its delay. Decreasing the current reduces the power consumption, too. Also, to introduce more delay, the L of transistors M_2 and M_3 are increased. Sizing down the transistors M_2 and M_3 also decreases the dynamic power consumption through decreasing the gate capacitors. The output pulse width as a function of width of transistor M_4 (half of the width of transistor M_1) and length of transistor M_3 (M_2) are shown in Figures 3.46 and 3.47. The power consumption of reset circuit as a function of W_3=W_4/2 is shown in Figure 3.48.

The total power consumption of an inverter cell can be found as

$$P_{total} = P_{dyn} + P_{dp} + P_{stat} \quad \text{(Eq. 3.45)}$$

Where P_{dyn} is dynamic power dissipation, P_{stat} is static power dissipation and P_{dp} is the power dissipation due to the direct-path current.

The dynamic power consumption can be kept low by reducing the size of transistor M_2 and M_3. The formula for dynamic power dissipation is given by [23]

$$P_{dyn} = C_L V_{DD}^2 f \quad \text{(Eq. 3.46)}$$

Where C_L is the switched load capacitor and f is the frequency of the input signal.

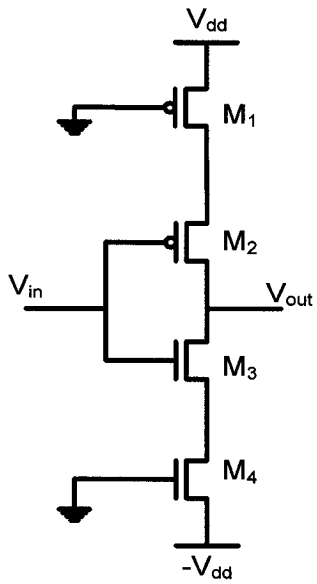


Figure 3.45. The current-starved inverter used in reset circuit

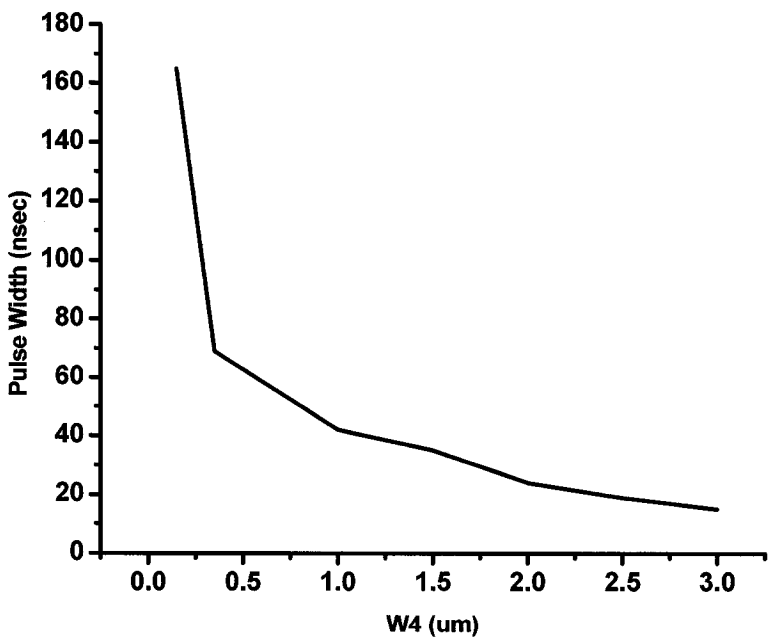


Figure 3.46. The pulse width as a function of W_4

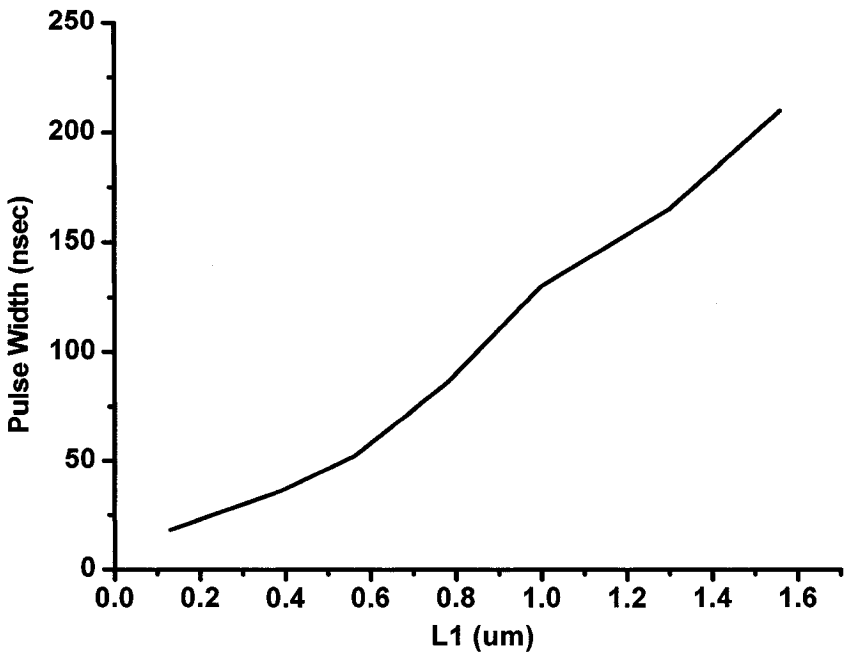


Figure 3.47. The pulse width as a function of L_1

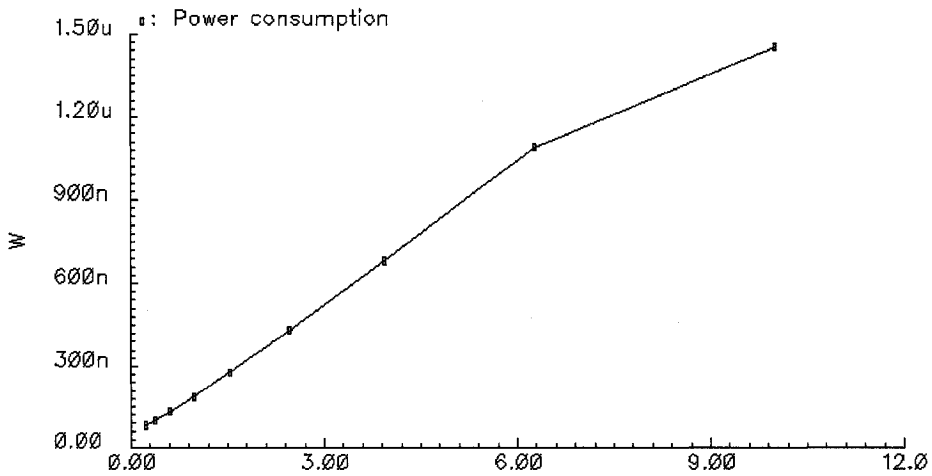


Figure 3.48. The power consumption of reset circuit as a function of W_3

P_{dp} is due the finite slope of the input signal which causes a direct current path between V_{DD} and GND for a short period of time during switching. The power dissipation due to the short-circuit current is minimized by matching the rise/fall times of the input and output signals. At the overall circuit level, this means that rise/fall times of all signals should be kept constant within a range. The direct-path power dissipation is as follows [23]

$$P_{dp} = t_{sc} V_{DD} I_{peak} f \qquad \text{(Eq. 3.47)}$$

Where t_{sc} represents the time both transistors M_2 and M_3 are conducting and I_{peak} is determined by the saturation current of the transistors M_2 and M_3 and is hence directly proportional to the size of transistors.

The static power is related to static current which is the current that flows between the supply rails in the absence of switching activity. This is due to leakage current of the reverse-biased diode junctions of the transistors and is as follows

$$P_{stat} = I_{stat} V_{DD} \qquad \text{(Eq. 3.48)}$$

The NOR circuit is shown in Figure 3.49. The input and output voltages of reset circuit are shown in Figure 3.50. The layout of the reset circuit is illustrated in Figure 3.51. The reset circuit provides a 165nsec pulse at each falling edge of the input signal. Its power consumption is 192nW. The component values of reset circuit are presented in Table 3.12.

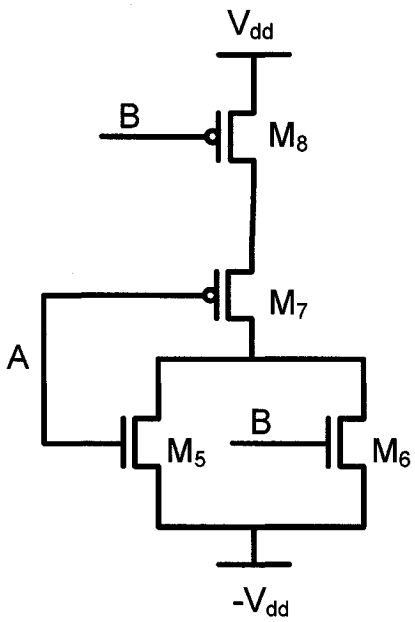
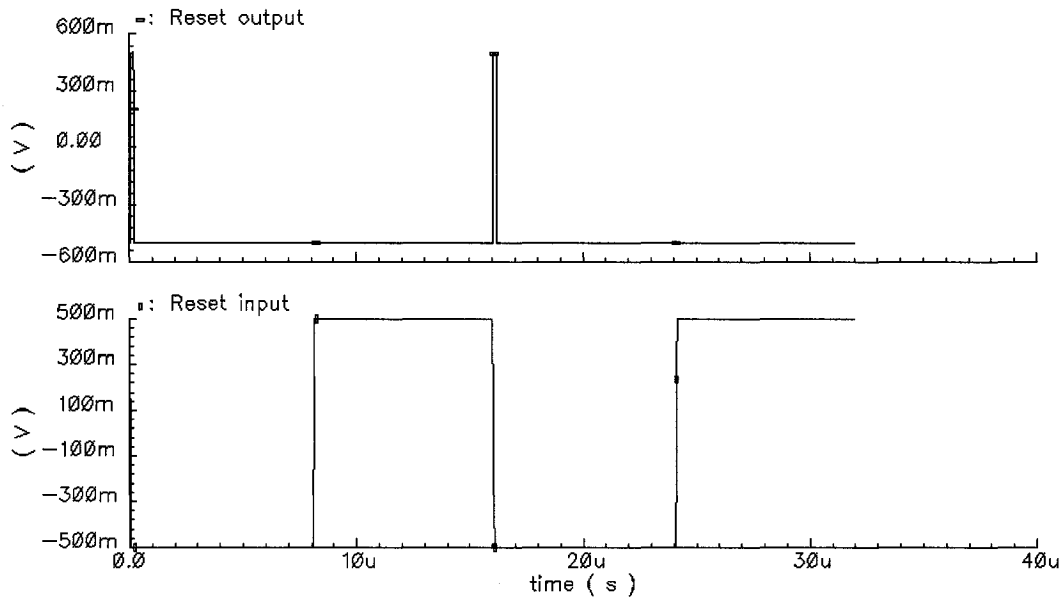


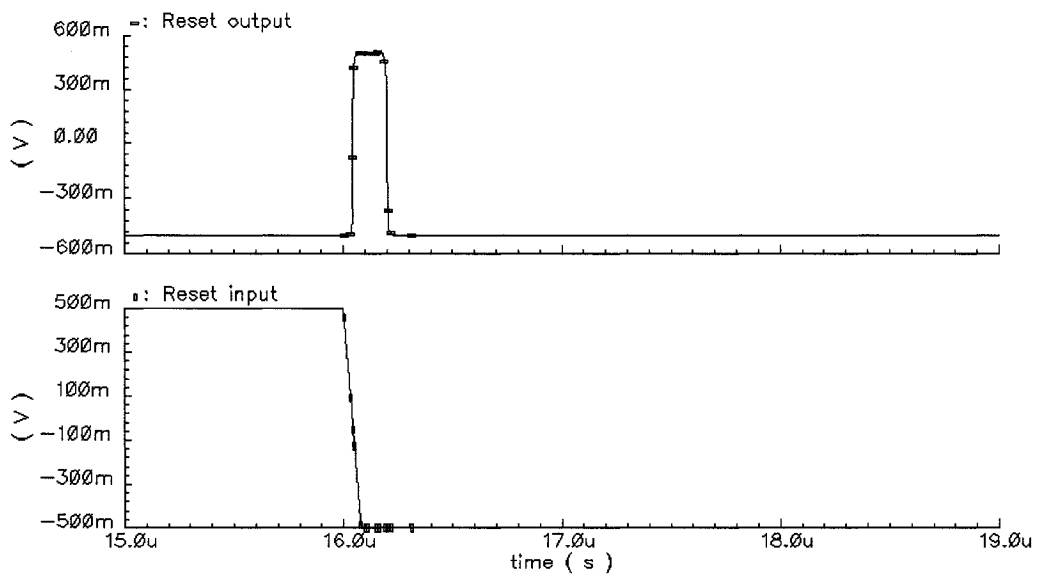
Figure 3.49. Schematic of NOR gate

Table 3.12. The component values of the reset circuit

M_1	PMOS, .3μm/1.3μm, No. of Fingers=1
M_2-M_7-M_8	PMOS, 2μm/1.3μm, No. of Fingers=1
M_3-M_5-M_6	NMOS, 1μm/1.3μm, No. of Fingers=1
M_4	NMOS, .15μm/1.3μm, No. of Fingers=1



(a)



(b)

Figure 3.50. Input and output of the reset circuit (a) zoom out (b) zoom in

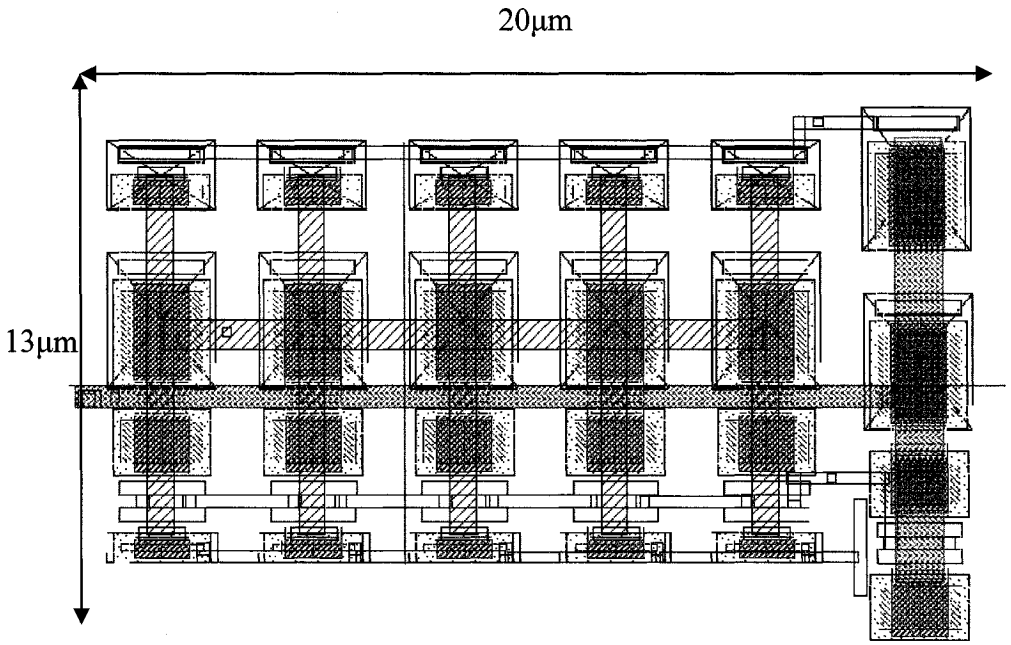


Figure 3.51. The reset layout

3.2.5 Comparator

The comparator circuit comes after the integrator to detect the data. The input to the comparator is from a switch that samples and holds the output of the integrator every 16μsec (the period of the input data). The gate of the switch is connected to the output of the reset circuit. Then the input voltage would be compared with the zero voltage and the difference would be amplified. This is necessary because the outputs of the integrator for "zero" and "one" inputs are close to each other and can not be determined by a simple inverter.

The schematic of the comparator circuit is shown in Figure 3.52. The bias current to the comparator is coming from the current source in the integrator circuit. The

comparator is a one-stage differential amplifier with the active load to increase the gain and output swing. The size of capacitor C determines the time that the sampled voltage can be hold. The gain of the amplifier is given by

$$A_{comp} = -g_{m3}(r_{o3} \parallel r_{o5}) \qquad \text{(Eq. 3.49)}$$

The gain and the frequency response of the comparator are shown in Figure 3.53.

The output of the amplifier goes to an inverter circuit to make the final output data. The inverter transistors are sized so that the threshold voltage is set to be at zero volts. The power consumption of comparator is 220nW. Layout of the comparator is shown in Figure 3.54. Table 3.13 shows the size of the transistors in comparator circuit.

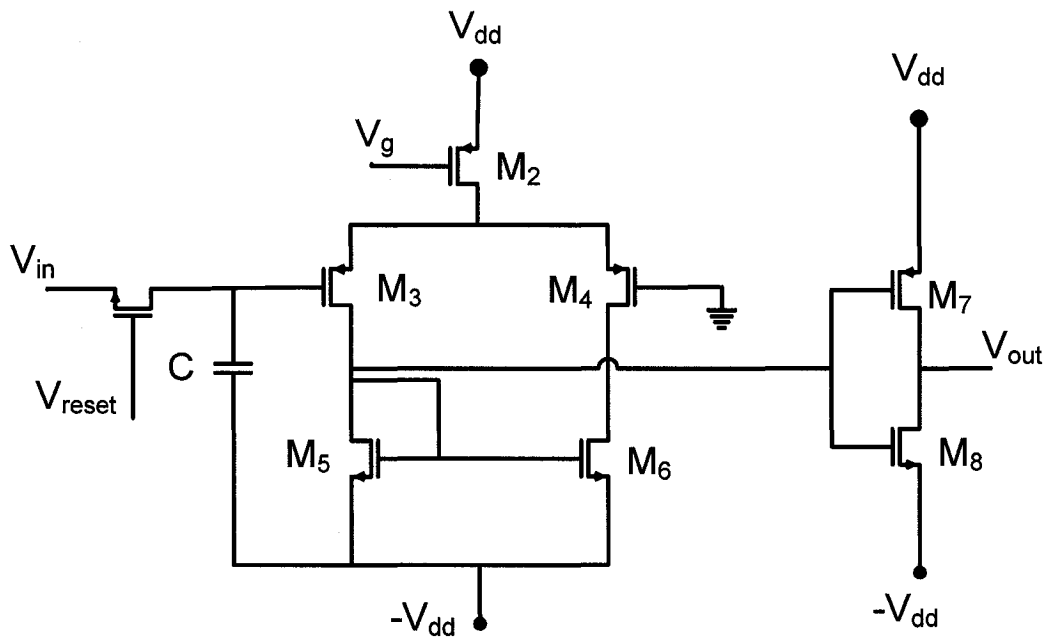


Figure 3.52. The comparator circuit

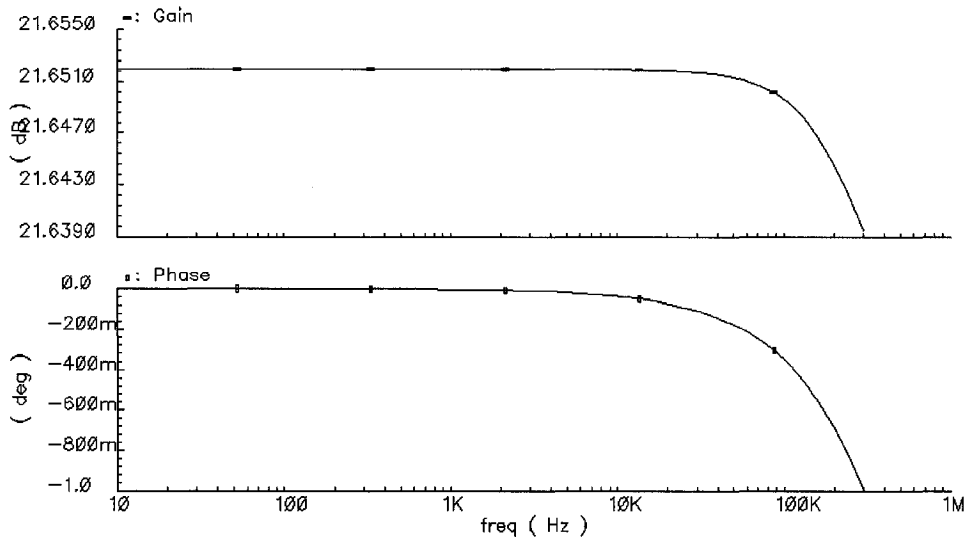


Figure 3.53. Gain and phase of the comparator circuit

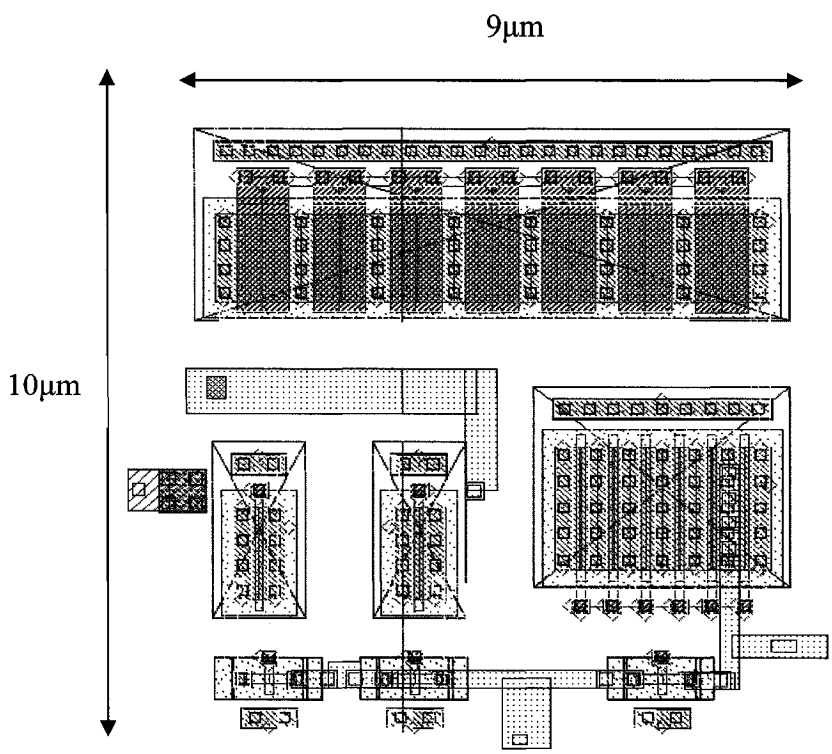


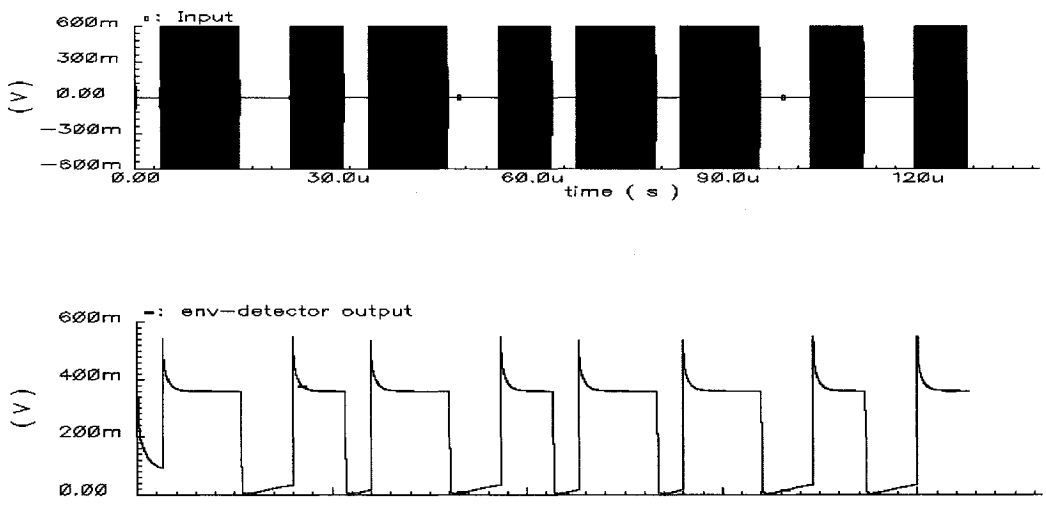
Figure 3.54. The comparator layout

Table 3.13. The component values of the comparator circuit

M_1-M_5-M_6-M_8	NMOS, .15μm/.13μm, No. of Fingers=1
M_2	PMOS, 10μm/.78μm, No. of Fingers=7
M_3-M_4	PMOS, 1.5μm/.13μm, No. of Fingers=1
M_7	PMOS, 12μm/.13μm, No. of Fingers=6
C	5pF

3.2.6 Demodulator Simulation Result

The demodulator output result for the input signal of [1 0 1 0 1 1 0] is shown in Figure 3.55. The demodulator output has a delay of 16μsec from the input signal. The waveforms of different parts of the demodulator circuit are illustrated in Figure 3.55.



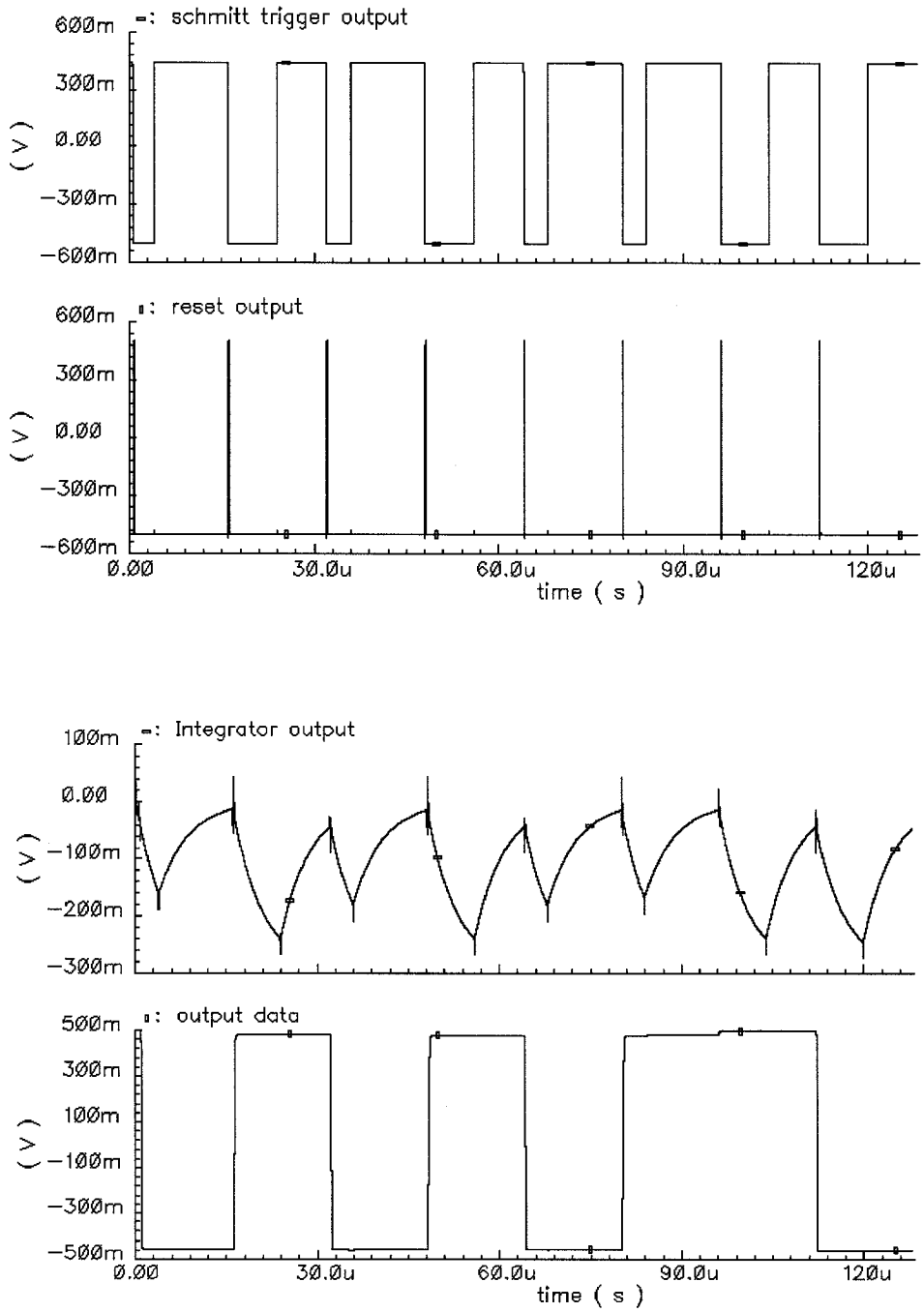


Figure 3.55. Demodulator simulation result

3.3 Clock Generator

To generate the clock in the UHF RFID transponders, an on-chip oscillator is needed. The oscillator structure should be low power and occupy a small area. To achieve the mentioned characteristics, a ring oscillator is used for clock generation.

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gate at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc conversion. This means that for an oscillator with single-ended delay stages, an odd number of stages is necessary for the dc inversion [24]. The most popular delay cells are inverters. The block diagram of a five-stage ring oscillator (RO) is shown in Figure 3.56.

The most important output parameters of ROs are output frequency (f_{osc}), duty cycle (DC) and phase noise.

For calculating the output frequency and duty cycle, assume each inverter stage as two dependent current source as shown in Figure 3.57. The rise time and the fall time of the inverter can be expressed as follows [25]

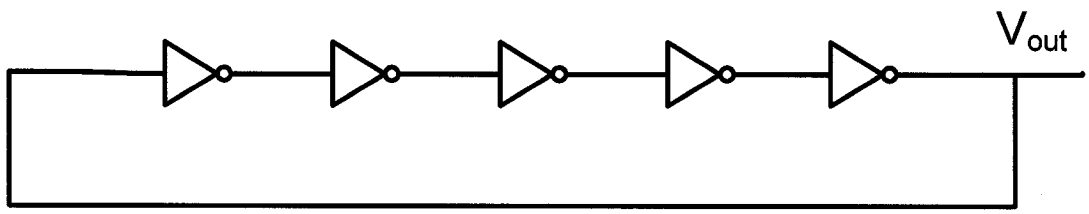


Figure 3.56. The five-stage ring oscillator

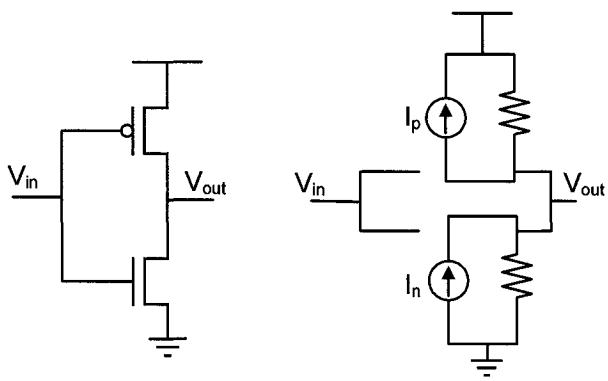


Figure 3.57. Model of an inverter circuit

$$\tau_r = \frac{C_L \Delta V}{I_p} \qquad \text{(Eq. 3.50)}$$

$$\tau_f = \frac{C_L \Delta V}{I_n} \qquad \text{(Eq. 3.51)}$$

Where C_L is the capacitance at V_{out} and ΔV is the total voltage swing of C_L.

So the frequency of oscillation can be derived as follows

$$f_{osc} = \frac{1}{N(\tau_r + \tau_f)} \approx \frac{1}{2N\tau_d} \qquad \text{(Eq. 3.52)}$$

Where N is the number of inverters and τ_d is average delay of each stage which is given by

$$\tau_d = \frac{\tau_f + \tau_r}{2} \qquad \text{(Eq. 3.53)}$$

The duty cycle of the output waveform can be defined as $\tau_r/(\tau_r+\tau_f)$ and therefore can be modified by introducing asymmetry to I_n and I_p as shown from [25]

$$DC = \frac{\tau_r}{\tau_r + \tau_f} = \frac{I_n}{I_n + I_p} \qquad \text{(Eq. 3.54)}$$

There are different ways to change the frequency and duty cycle of the ring oscillator. The first one is by changing the output capacitance. The output capacitance of each stage contains two times of the gate-drain capacitance plus the gate-source capacitances of the next stage. So the C_L can be written as

$$C_L = 2C_{gd} + C_{gs} \qquad \text{(Eq. 3.55)}$$

Sizing up the transistors will increase the C_{gs} and C_{gd} and consequently increasing the average delay which cause a lower oscillation frequency.

Another important factor in determining the delay of the inverter cell is the PMOS and NMOS currents. One way to control the currents of transistors is by changing the (W/L). Changing the size of transistors does not help as much as required because increasing (decreasing) the transistor size also increases (decreases) the diffusion capacitance and hence changes C_L [23].

Another way is using the current-starved inverter. The schematic of a current-starved inverter is shown in Figure 3.58.

In the current-starved inverter, the charging and discharging current of the output capacitance of transistor M_2 and M_3, are controlled by two NMOS and PMOS transistors at the source of M_2 and M_3 [26]. The current can be controlled by the size of transistors M_1 and M_4 and also by their gate voltages which controls the current that flows in M_1 and M_4. Also, the effective resistance and capacitance at the source of M_2 and M_3 are changed by transistors M_1 and M_4. Increasing the channel length of M_1 and M_4 puts a higher resistance and a larger parasitic capacitance at the source of M_2 and M_3. A larger

resistance increases the delay; however, a larger parasitic capacitance decreases the delay. The charge sharing effect causes the load capacitance to be discharged faster [26].

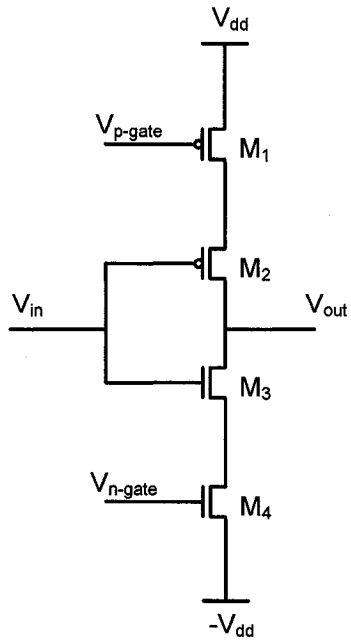


Figure 3.58. The current-starved inverter

To decrease the oscillator power consumption, the current flow in the inverters is restricted by using a current sink which is connected to a very low current source. The schematic of the ring oscillator circuit is shown in Figure 3.59. The transistors S_1 to S_4 act as switches. When the V_{dd} is not produced, the POR signal is high, so the S_2 and S_3 switches connect the V_{dd} of the ring oscillator to the ground and cause the circuit to be OFF. When the V_{dd} is produced, the POR signal becomes low and the V_{dd} connects to the oscillator circuit and turn it ON.

During the demodulation, the V_{dd} ($-V_{dd}$) signal changes between 450mV to 500mV (-450mV to -500mV). The ring oscillator should be designed in a way that changing the V_{dd} does not change the frequency of oscillation. As the current mirror is V_{dd} independent, the frequency of oscillation changes from 393KHz to 395KHz (200Hz). The frequency of oscillation as a function of V_{dd} is shown in Figure 3.60.

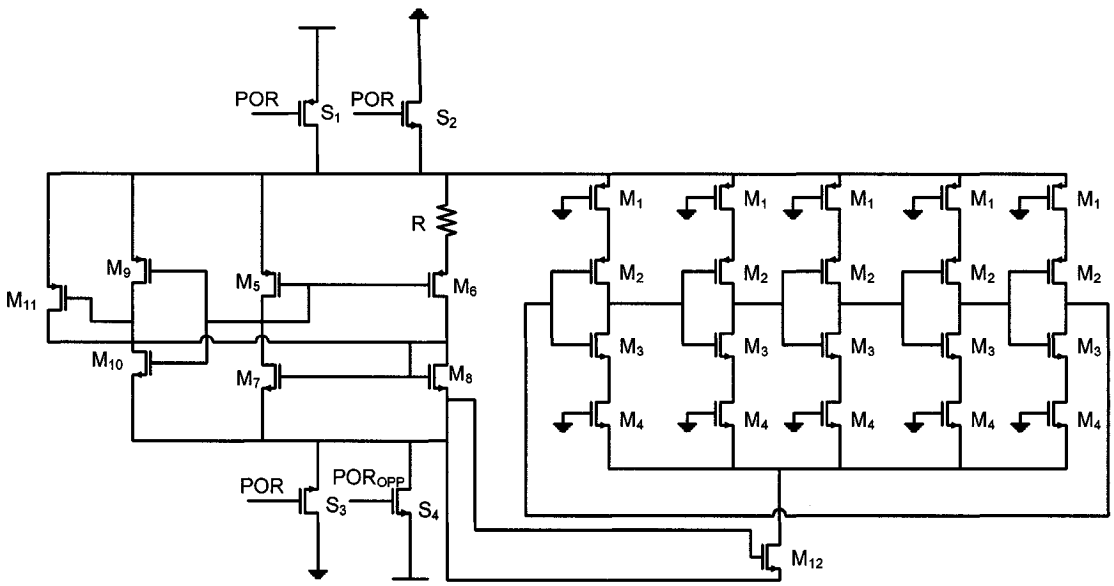


Figure 3.59. The schematic of ring oscillator

Also, the frequency of oscillation should not have a lot of variation with the temperature changes. The frequency of oscillation as a function of temperature is shown in Figure 3.61.

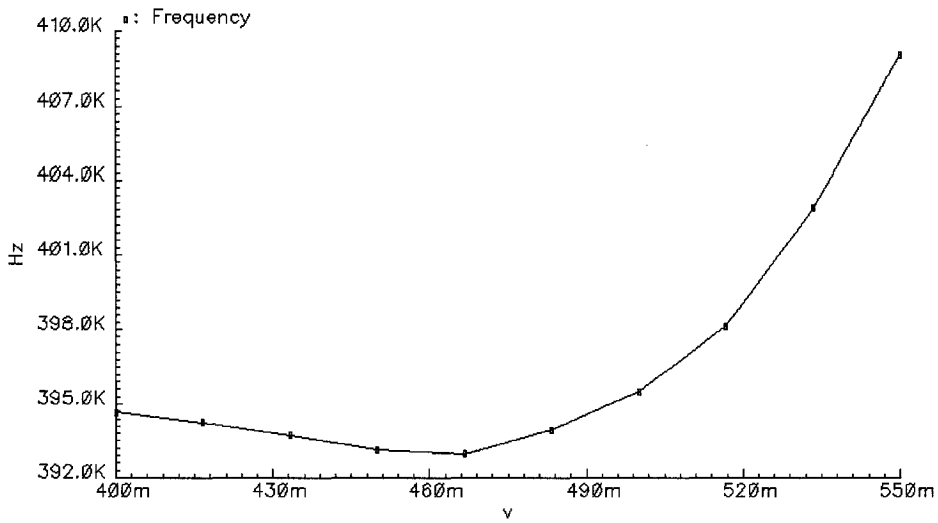


Figure 3.60. The frequency of oscillation as a function of V_{dd}

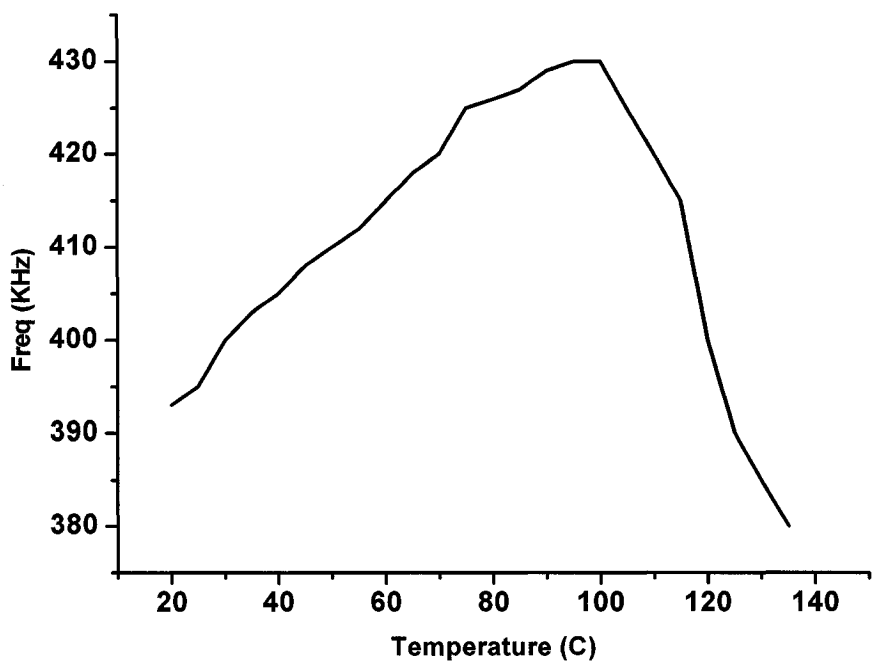


Figure 3.61. The frequency of oscillation as a function of temperature

The oscillator output is illustrated in Figure 3.62. The layout of the clock generator is shown in Figure 3.63. The component values of oscillator are presented in Table 3.14. Oscillator parameters are summarized in Table 3.15.

Table 3.14. The component values of ring oscillator

M_1	PMOS, .3μm/1.3μm, No. of Fingers=1
M_2	PMOS, 2μm/1.3μm, No. of Fingers=1
M_3	NMOS, 1μm/1.3μm, No. of Fingers=1
M_4	NMOS, .15μm/1.3μm, No. of Fingers=1
M_5-M_6	PMOS, 11μm/1.04μm, No. of Fingers=10
M_7-M_8	NMOS, 1μm/1.04μm, No. of Fingers=1
M_9	PMOS, .3μm/.13μm, No. of Fingers=1
M_{10}	NMOS, .15μm/.13μm, No. of Fingers=1
M_{11}	PMOS, 20μm/1.3μm, No. of Fingers=10
M_{12}	NMOS, 20μm/1.3μm, No. of Fingers=10
S_2-S_3-S_4	NMOSHVT, .15μm/.13μm, No. of Fingers=1
S_1	PMOSHVT, .15μm/.13μm, No. of Fingers=1
R	20KΩ

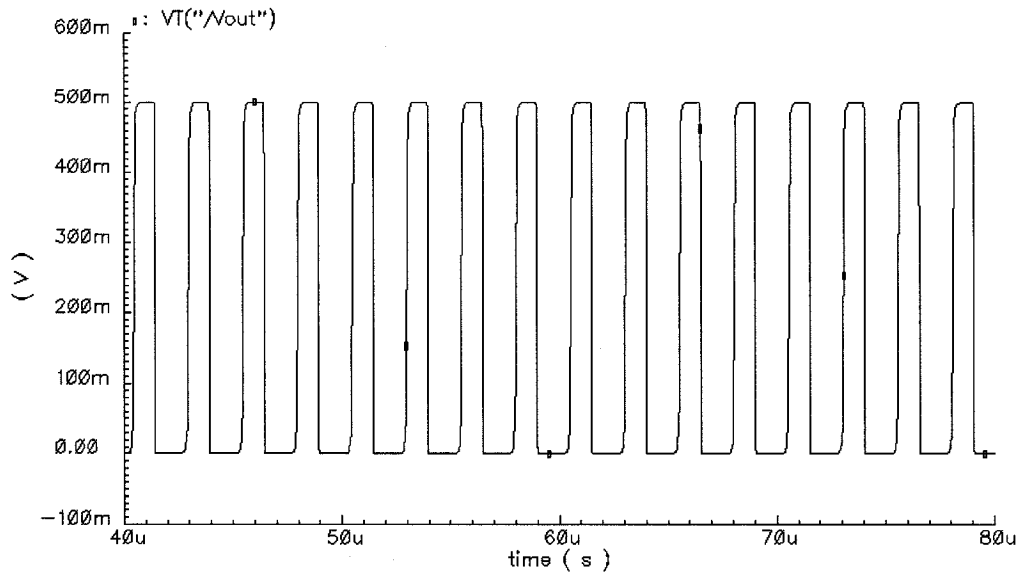


Figure 3.62. Output of the ring oscillator

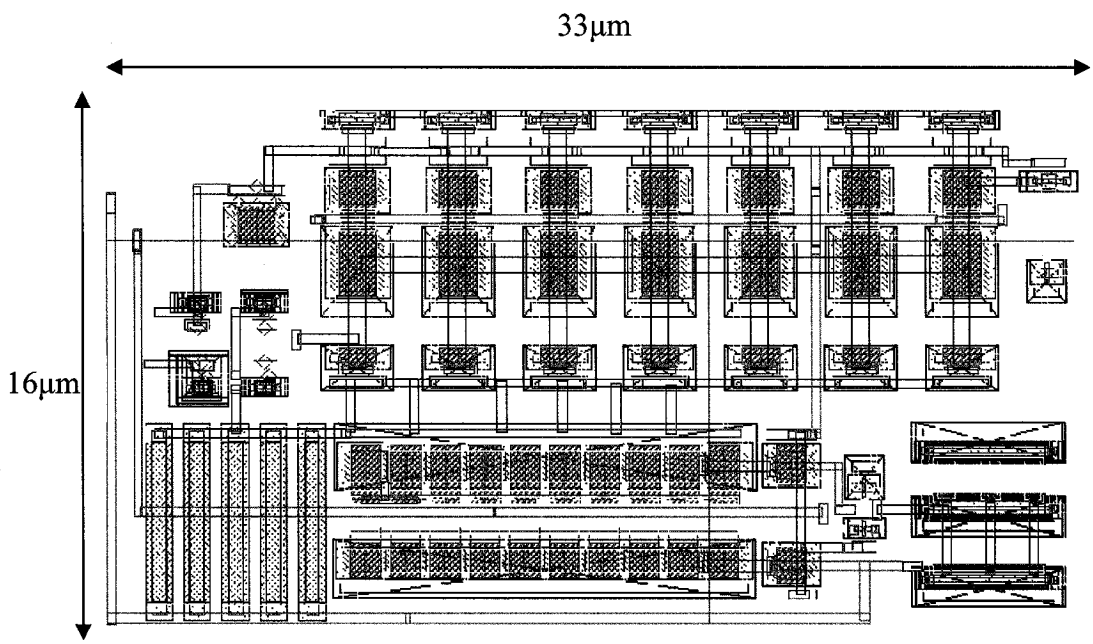


Figure 3.63. Ring oscillator layout

Table 3.15. The ring oscillator parameters

Oscillation Frequency	Duty cycle	Power consumption
395KHz	42%	126nW

3.4 Power-on-Reset

The power on reset circuit has two main functions that are essential for the correct operation of the chip. One is generating the reset signal for the digital section of the chip and the other function is to disconnect the chip when the required power falls below a critical level.

The POR circuit measures the power supply level and then compares this level to a certain required threshold. If the power supply voltage exceeds the required threshold, the POR circuit generates the required command signals so that the operation of the chip would begin. The POR circuit has a delay element that generates a timing difference between the time that the supply is no longer adequate and that where the reset disable signal is set [12].

The power on reset circuit is shown in Figure 3.64. POR is composed of a cross-coupled pair of transistors and a NOR gate. It is a nonstable system and when the circuit powers up, one branch (M_3, M_4 or M_5, M_6) dominates. The NOR gate compares the two gate signals insuring a power on reset for the logic blocks. The capacitor C allows a slow charging of node A to force a delay between the rise of the voltage supply and the power on reset. In addition, it damps the circuit to avoid parasitic oscillations [27]. The threshold of the circuit is determined by the inverter sizes (inverter thresholds). The

output signal of the power on reset circuit is shown in Figure 3.65. The layout of the POR circuit is shown in Figure 3.66. The power consumption of POR is 345nW. The component values of POR are presented in Table 3.16.

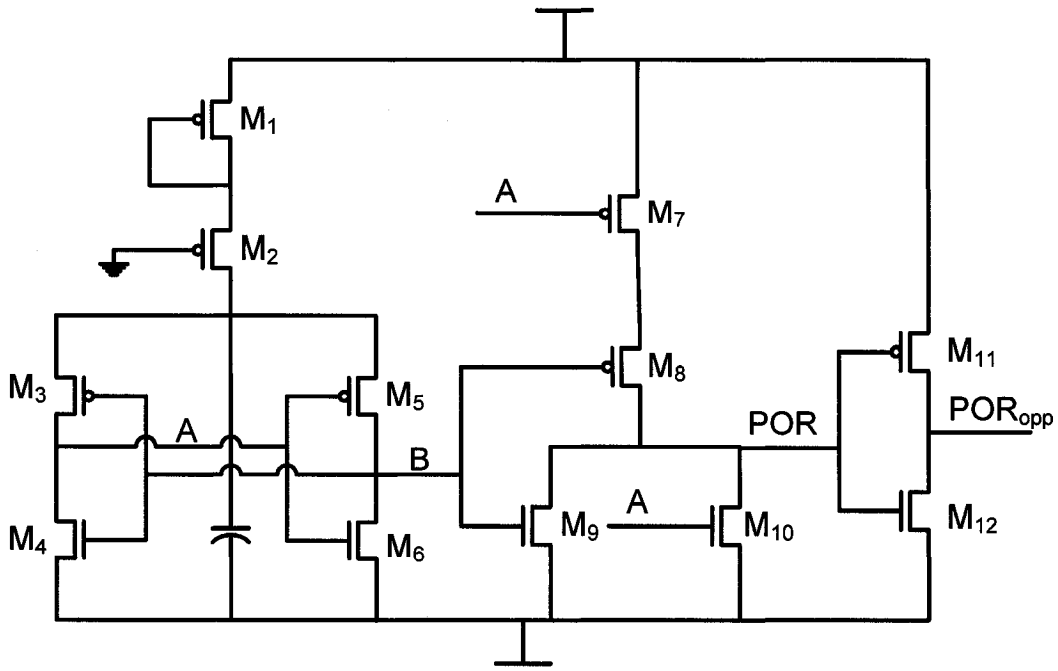


Figure 3.64. The power on reset circuit

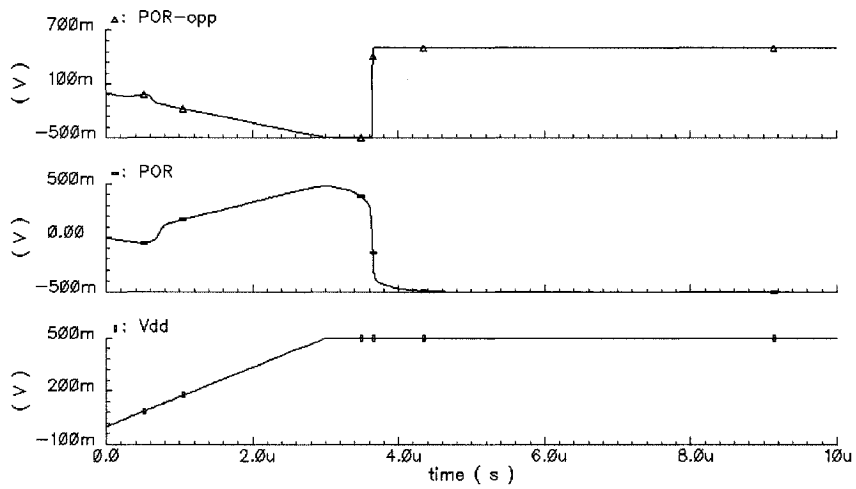


Figure 3.65. The output signal of the power on reset circuit

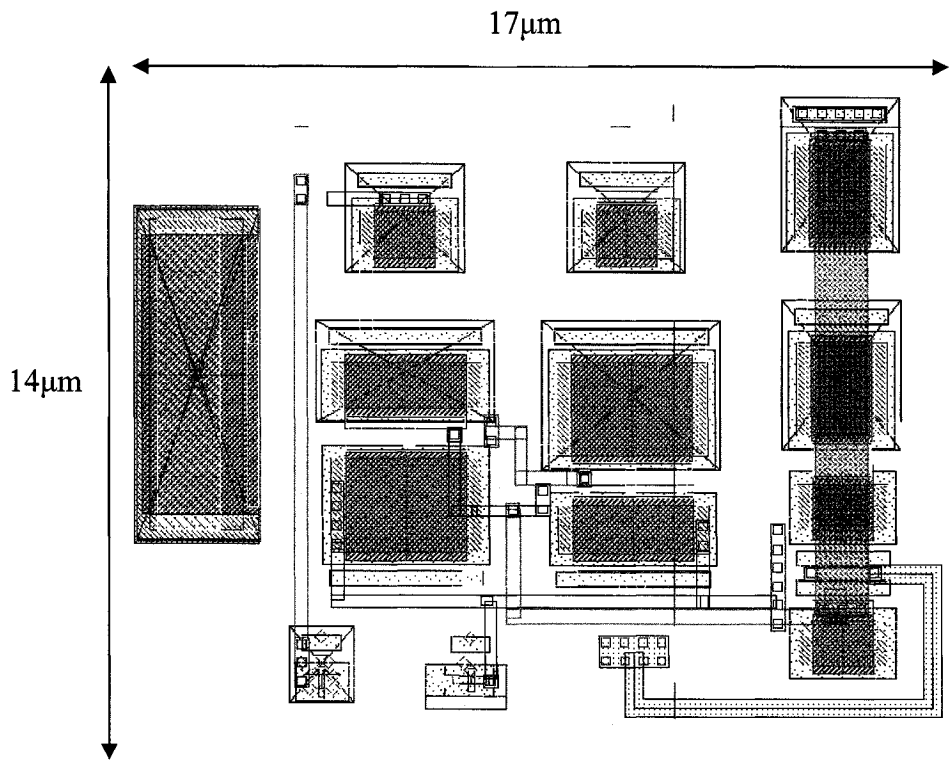


Figure 3.66. POR layout

Table 3.16. The component values of POR circuit

M_1-M_2	PMOS, 1μm/1.3μm, No. of Fingers=1
M_3	PMOS, 1μm/2.6μm, No. of Fingers=1
M_4	NMOS, 2μm/2.6μm, No. of Fingers=1
M_5	PMOS, 2μm/2.6μm, No. of Fingers=1
M_6	NMOS, 1μm/2.6μm, No. of Fingers=1
M_7-M_8	PMOS, 2μm/1.3μm, No. of Fingers=1
M_9-M_{10}	NMOS, 1μm/1.3μm, No. of Fingers=1
M_{11}	PMOS, .3μm/.13μm, No. of Fingers=1
M_{12}	NMOS, .15μm/.13μm, No. of Fingers=1
C	50fF

3.5 Backscatter Modulation and Matching Network

The backscatter is the way that the tags communicate with the reader. It enables the tag to reader communication by varying the input impedance of the transponder. There are two modulation types: ASK and PSK. In PSK modulation, the available power to the tag is kept constant during both states. This is the advantages of PSK over ASK. However, the simple fact that the components are lossy makes it impossible to achieve an 180° modulation angle between two states. As a result, the communication in terms of bit error rate is degraded. So there is a tradeoff between power available to the tag and the power devoted to the communication. It is shown [11] that an ASK modulation scheme, where one of the two states is active most of the time, is a good choice in term of power efficiency. Also, the ASK modulator input impedance is independent of the frequency so it can be implemented without reactive elements with a simple switch.

The average power available at the input of the transponder at ASK and PSK cases are given by [29]

$$P_{in-ASK} = (1 - DC)P_{avail} \qquad \text{(Eq. 3.56)}$$

And

$$P_{in-PSK} = \frac{4R^2_{ant}}{4R^2_{ant} + X^2_{in}} P_{avail} \qquad \text{(Eq. 3.57)}$$

Where DC is the duty cycle of the ASK modulation signal.

The input power as a function of the duty cycle for the case R_{in}=X_{in} is shown in Figure 3.67 [29]. It shows that for low duty cycles, the ASK power efficiency is improved compared to PSK.

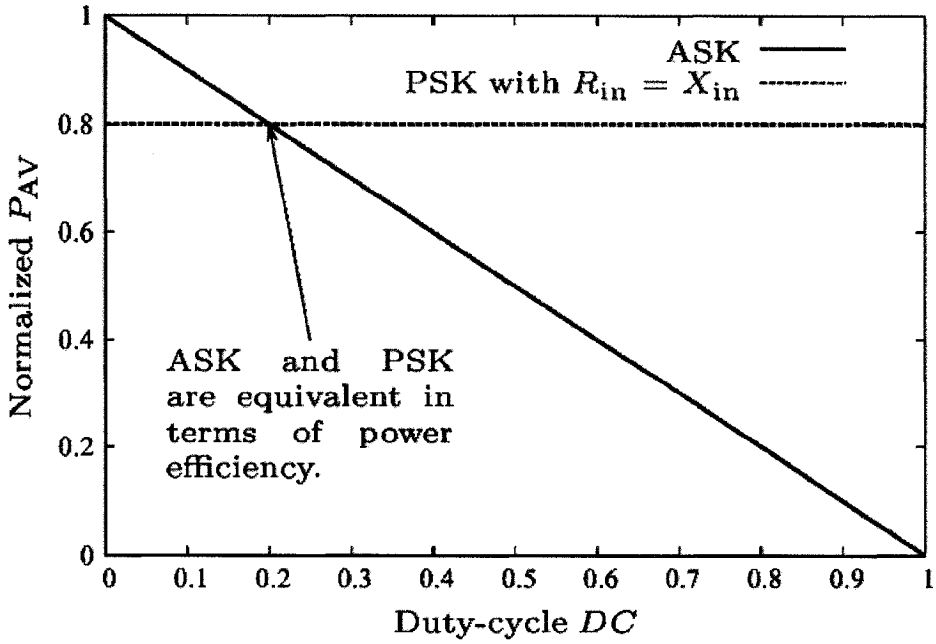


Figure 3.67. Average available input power as a function of DC normalized to P_{av} (Courtesy of Dr. Jari-Pascal Curty from paper "Remotely Powered Addressable UHF RFID Integrated System," *JSSC*. © IEEE 2005. Reprinted with permission)

As a result, the ASK modulation with low duty cycle is chosen for this thesis to maximize the operating range and operate at multiple frequencies. This means that the modulator and the IC input must either be perfectly matched to the antenna impedance or be equivalent to a short circuit. Such a behavior is easily realizable with the help of a switch and a matching network [29]. Figure 3.68 shows the configuration of the modulator and matching network.

An ideal switch does not exist and in every configuration it is associated with a parasitic capacitance and conductance. In our case, the parasitic capacitance can be taken into account when designing the matching network. When the switch is closed, the power losses can not be compensated. However, they occur at a moment where the

rectifier can not absorb any power since the goal is to reflect as much power as possible. These losses induce a decrease in term of modulation depth. Practically, the switch is realized using two minimum-length (1μm wide) NMOS and PMOS transistors in parallel to linearize the switch resistance in the large dynamic range of the input signal.

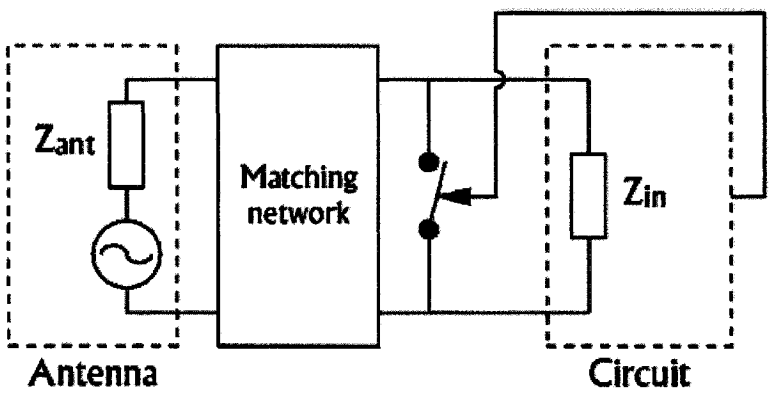


Figure 3.68. Parallel modulator configuration
(Courtesy of Dr. Jari-Pascal Curty from paper "Remotely Powered Addressable UHF RFID Integrated System," *JSSC*. © IEEE 2005. Reprinted with permission)

The equivalent input impedance of the IC can be modeled as a series combination of resistance and capacitance. To match the input impedance to the 50Ω antenna, an inductor had been used. The matching network is shown in Figure 3.69. The series resistance and capacitance can be converted to a parallel combination by using the following equations

$$R_{parallel} = R_{series}(1+Q^2) \qquad \text{(Eq. 3.58)}$$

$$X_{parallel} \approx X_{series} \qquad \text{(Eq. 3.59)}$$

Where Q is given by

$$Q = \frac{1}{R_{eq} C_{eq} \omega} \qquad \text{(Eq. 3.60)}$$

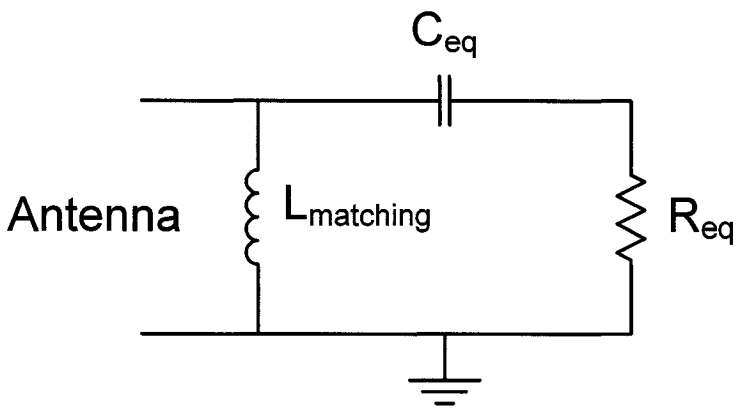


Figure 3.69. The matching network

The inductor should be selected somehow to resonate with the parallel capacitance. The size of inductance that is used in this project is 1.65nH with the quality factor equal to 6. The input S_{11} is shown as a function of frequency in Figure 3.70. The S_{11} at 2.4GHz is around -22dB which illustrate a good matching at that frequency.

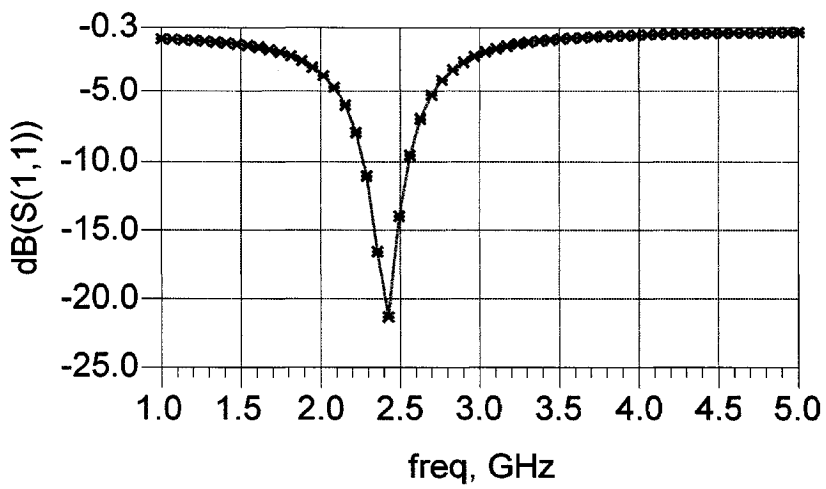


Figure 3.70. The input S_{11} as a function of frequency

CHAPTER 4. LAYOUT

4.1 General Layout Issues and Precautions

Correct and thoughtful layout out of the chip components is very critical to the final performance of the systems. Special attention needs to be paid to components which experience the RF frequency at the input stages of the RFID front-end. These blocks include the rectifier, RF-Clamp, Envelope detector and their peripherals. In this section the important points that were taken into account during layout are described.

The RF-Clamp circuit contains transistors that should be able to draw currents in the milliampere range. This is in contrast with the rest of the chip which works with currents in the order of nanoampere or at most microampere. The clamp circuit comes into action in the cases where the reader is located close to the tag and therefore the signal levels at the RF stage rise to several volts. This section is responsible for bringing the signal levels down to below one volt. To have transistors that can allow this much voltage and current custom NMOS devices were laid out. These devices have wide source and drain regions and have multiple fingers to support DC currents up to around 7mA. Multiple contacts and vias are places to support this level of current. Devices are placed in series to increase the voltage handling capability of deices.

Another important part of the design in the RF section is the voltage rectifier section. This section consists of MOS diodes and MOS capacitors. The MOS diodes are laid out in a way to decrease any series resistance in the forward path. This is achieved by using multiple fingers to have parallel source and drain sections. Also, the use of shorter finger

width transistors reduces the gate resistance and aids the high frequency operation of the device. PMOS devices are used as diodes for their superior performance in terms of lower threshold voltages.

The MOS capacitors need to withstand voltages close to one volt and need to be laid out using the high threshold voltage option where the oxide thickness is greater than the nominal devices. This option decreases the capacitor density of the chip and should be avoided wherever possible (e.g. when operating voltages do not exceed the breakdown voltage of nominal MOS device). In the designed RFID system large MOS capacitors in the order of 20pF are used to store the recovered energy. With such large capacitors the die area of one capacitor could exceed 50μm by 50μm. The series resistance of poly sheets used to implement such large capacitors can easily degrade the performance at RF frequencies and therefore special precautions need to be taken. A MOS capacitor cell (70fF) containing properly connected peripherals was designed and all the large MOS capacitors are instantiations of this cell. Metal layers are used to connect the relevant gates and source/ drain contacts of the parallel capacitors reducing the series resistance dramatically. This method produces some extra capacitance between the two terminals of the capacitor which is usually orders of magnitude smaller than the overall capacitance and therefore could be neglected. In the cases where smaller capacitors are designed this extra component needs to be accounted for using extraction tools. Also, most sections are designed in such a way as to be relying only upon the ratio of the capacitors and less so to the exact values. This reduces the sensitivity of the design to the layout and increases the robustness of these blocks.

The incoming signal from the RF pad to the matching network is operating at 2.4GHz. Care must be taken so that the parasitic capacitances and also the series inductance are small enough to be neglected. The parasitic capacitances result either from wide traces leading to metal-metal mutual capacitances or through substrate coupling. This effect can be predicted through first order parallel plate approximations. The inductance however cannot be predicted unless a well defined return path is presented through the use of closely spaces ground lines. In general at these frequencies, the parasitic inductance is an order of magnitude smaller than the on chip spiral inductors and could be neglected. Still, coplanar lines can be used to connect the probe pad to the various stages of the matching network to mitigate this undesired effect.

Latchup is another undesirable effect that can degrade the performance and in some cases even damage the chip [23]. To mitigate the chances of a Latchup, substrate contact rings are placed around PMOS devices and in the cases where the NMOS and PMOS devices are in close proximity, they are separated by substrate contacts.

The final RFID front-end layout is shown in Figure 4.1.

4.2 Inductor Design and Layout

Spiral inductors are used for matching and voltage enhancement purposes. The design of on-chip inductors and various issues and parameters that are involved will be discussed in this section.

A loop or a ring inductor is a good option for integrated circuits where planar structures or at most multi-level patterns are preferred. The inductance of a loop inductor

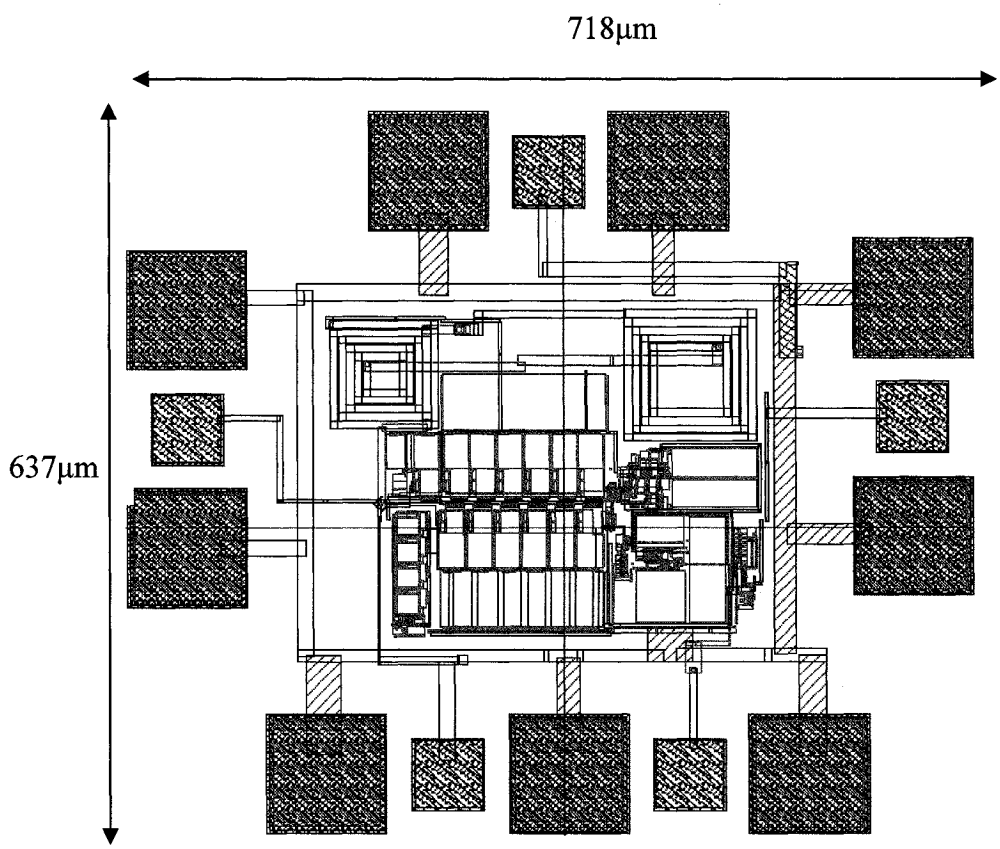


Figure 4.1. The RFID front-end layout

is proportional to the area of the loop. The resistance however is proportional to the perimeter and therefore a structure with the maximum area to perimeter ratio is desirable. A circle has the maximum area to perimeter ration among planar structures. However, because of constraints on the layout of metal traces usually approximations to a circle (e.g. hexagonal) are implemented. The quality factor of an inductor is defined to be

$$Q = \frac{\omega.L}{r} \qquad \text{(Eq. 4.1)}$$

Another important factor in designing on-chip inductors is the self-resonant frequency of the loop. This is the frequency at which the inductor seizes to be an inductor and starts acting similar to a capacitor. Figure 4.2 shows the general model for a spiral inductor including the substrate network model. The self-resonant frequency of the inductor is the frequency at which the capacitor C_s and the inductor L_s in Figure 4.2 resonate. The main physical parameters that affect the SRF of a spiral inductor are the spacing and widths of the turns, number of turns, number of metal levels used and the distance to substrate. Spiral inductors having multiple turns have inductances proportional N^2. This is with the assumption that the areas of all the loops remain the same. The limit to having multiple turns is the SRF being lowered by the mutual capacitance between different loop windings. SRF of a single loop inductor can be as high as several tens of gigahertz even approaching 100GHz. This value drops quickly with each added turns going down to a few gigahertz for closely packed inductors with N=3, 4.

Most modern IC processes offer many metal layers that could be used to design more complicated three dimensional structures with multiple levels. For instance, two or more spirals on different layers can be placed in series to increase the inductance. The spirals

should be wound correctly for the magnetic flux to add. To calculate the total inductance the self and mutual inductances of all the layers need to be accounted for. The upper bound of the inductance boost assuming a very good coupling of loops is N^2.

To understand the loss mechanisms of a spiral inductor we need to know the loss mechanisms in this element.

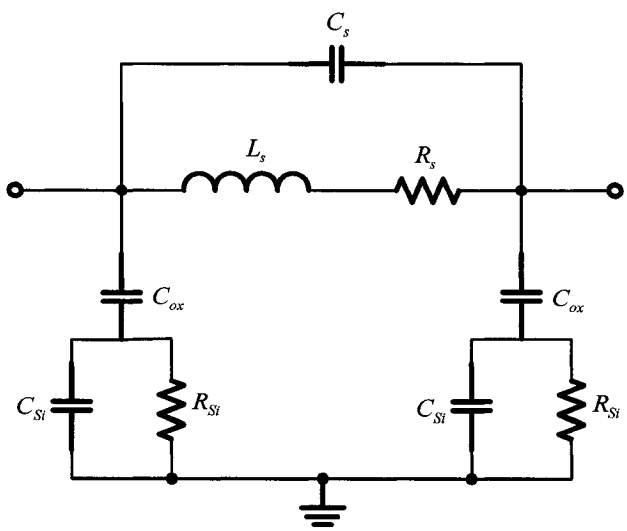


Figure 4.2. The inductor pi model

The planar inductor layout is implemented using ASITIC and Advanced Design System (ADS). The inductor layout specifications are given in Table 4.1.

Table 4.1. The inductors layout specifications

Inductor Name	Width (μm)	No. of Turns	Spacing (μm)	Outer Diameter
Rectifier-Ind	6.5	4.25	.5	110
Matching-Ind	6.2	5	.5	90

The extracted inductor parameters r,L, and Q are shown in Figures 4.3 and 4.4 for rectifier and matching inductors. The rectifier inductor layout is shown in Figure 4.5. The inductors extracted pi model parameters are presented in Table 4.2. The required inductors parameters are illustrated in Table 4.3.

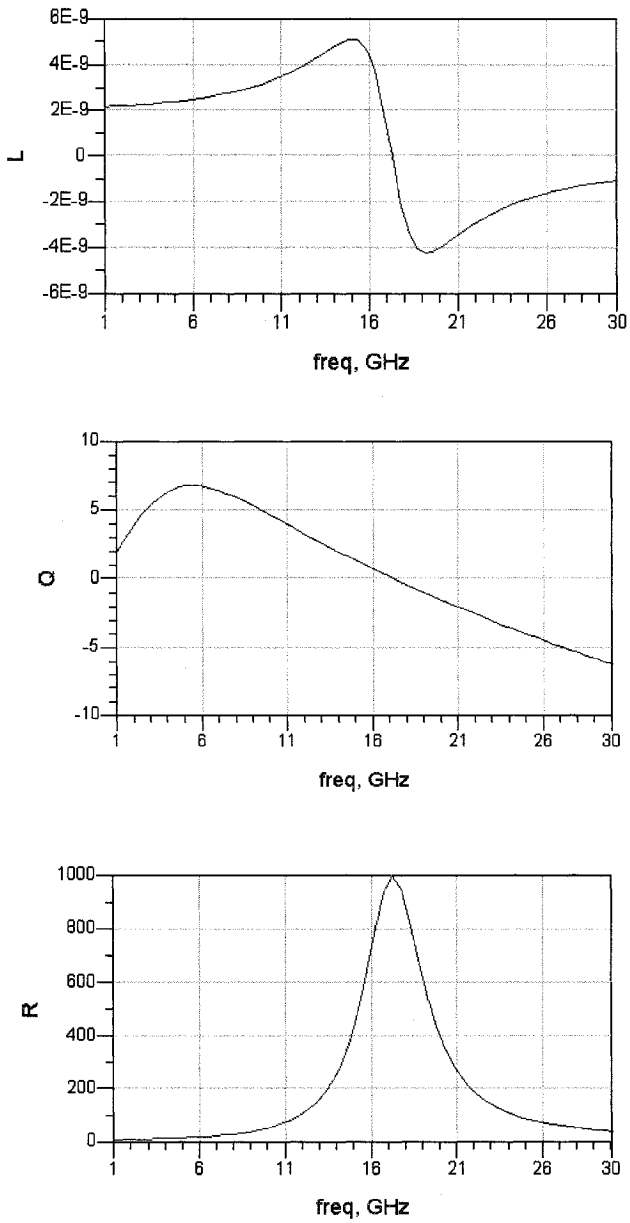


Figure 4.3. The simulated L,Q and R of the rectifier inductor

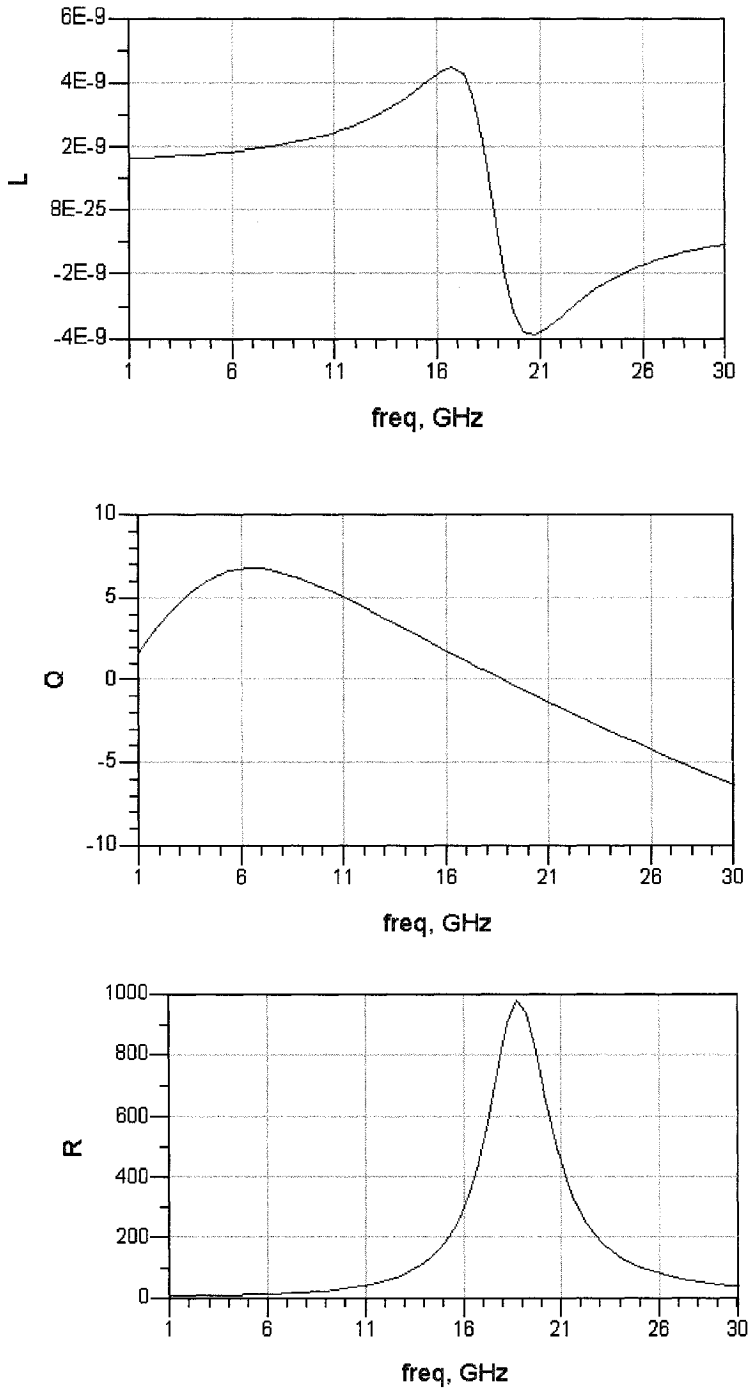


Figure 4.4. The simulated L,Q and R of the matching inductor

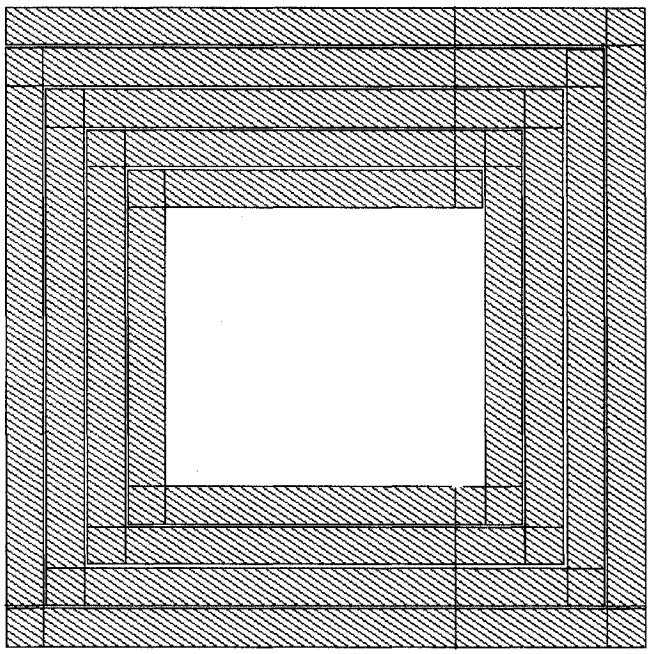


Figure 4.5. Rectifier-inductor layout

Table 4.2. Inductors extracted pi model parameters

Ind-Name	L(nH)	R (Ω)	C_s(fF)	C_{si1}(fF)	R_{si1}(kΩ)	C_{si2}(fF)	R_{si2}(kΩ)
Rectifier-Ind	2.15	5.17	37.98	37.85	1.121	34.75	1.325
Matching-Ind	1.65	4.5	42.21	34.62	1.168	31.25	1.428

Table 4.3. Inductor parameters

Ind-Name	L(nH)	R(Ω)	Q	SRF (GHz)
Rectifier-Ind	2.15	5.17	6.2	17.62
Matching-Ind	1.65	4.5	5.85	19.08

CHAPTER 5. CONCLUSION

This thesis focused on the design and analysis of the RF section of a passive RFID tag operating in the 2.4GHz band. The system is designed in a 0.13μm 1P6M Atmel CMOS process. The designed blocks include the on-chip matching network, voltage multiplier, regulator, envelope detector, power on reset, backscatter modulator and PWM demodulator. The charge pump is fully integrable and takes advantage of both tuned passive and also charge pump multiplication to reduce the required input power. The minimum required input power for a 1.2V supply voltage in the case of a 50Ω antenna is –20.45dBm. The efficiency is 15.95% for a 1MΩ load. The regulator consumes 602nW DC power and keeps the reference voltage in a 1.1% range with V_{dd} changing from 0.8V to 2V. The PSNR of the regulator is -42dB in around 2.45GHz frequency and stays better than -32dB from 100Hz to 10GHz frequencies. The PWM demodulator is used to extract the input data. The ring oscillator produces a 395kHz clock for the digital section.

Future directions of this project could be towards the design of on-chip integrable antennas and also the integration of base-band circuitry for any transfer of data with the chip. One of the main advantages of a 2.4 GHz UHF tag is with the antenna size and the possibility of having integrable miniaturized antennas. The co-design of antenna together with that of the matching network and the power recovery circuitry can lead to better solutions.

Other possibilities of future work are on circuitry to improve the efficiency of the voltage multiplier even further than what was presented. Schottky diodes that are compatible with the digital CMOS process have been proposed and could be used to

decrease the voltage drop on the diodes in the charge pump and therefore increase the overall effectiveness of the multiplier.

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APPENDIX

In this appendix we will derive the input impedance of a one-stage voltage multiplier shown in Fig.7. Two different signal cycles shown in Fig.7a and Fig.7b are analyzed and the average input resistance and capacitance are derived.

The input resistance and capacitance in the negative cycles of the input voltage are

$$C_{equal1} = \frac{C_1 C'}{C_1 + C'} \tag{A.1}$$

$$R_{equal1} = \left(\frac{R_{load}(1+Q^2{}_2)}{(1+Q_1{}^2)} \middle\| \frac{1}{g_m}\right).(1+Q_3{}^2)^{-1} \tag{A.2}$$

Where

$$C' = C_{on} + \frac{C_{load}{}' C_{off}}{C_{load}{}' + C_{off}} \tag{A.3}$$

$$C_{on} = C_{gs,on} + C_{db} \tag{A.4}$$

$$C_{off} = C_{gs,off} + C_{db} \tag{A.5}$$

$$C_{load}{}' = C_{load} + C_2 \tag{A.6}$$

$$Q_1 = R_{load} C_{load}{}' \omega \tag{A.7}$$

$$Q_2 = \frac{(1+(R_{load} C_{load}{}' \omega)^2)(C_{load}{}' + C_{off})}{R_{load} C_{load}{}' C_{off} \omega} \tag{A.8}$$

$$Q_3 = \left(\frac{R_{load}(1+Q^2{}_2)}{(1+Q_1{}^2)} \middle\| \frac{1}{g_m}\right) C' \omega \tag{A.9}$$

Similarly the input resistance and capacitance in the positive cycles of the input voltage are

$$C_{equal2} = \frac{C_1(C_{off} + C_{eq,2})}{C_1 + C_{off} + C_{eq,2}} \tag{A.10}$$

$$R_{equal2} = \frac{R_{eq,1}(1 + (\frac{1}{R_{eq,1}C_{eq,2}\omega})^2)}{(1 + Q_4^{\ 2})} \tag{A.11}$$

Where

$$C_{eq,2} = \frac{C_{load}^{\ \prime} C_{eq,1}}{C_{load}^{\ \prime} + C_{eq,1}} \tag{A.12}$$

$$C_{eq,1} = \frac{(1 + (C_{on}\omega)^2)g_m}{C_{on}\omega^2} \tag{A.13}$$

$$R_{eq,1} = \frac{R_{load}}{1 + (R_{load}C_{load}^{\ \prime}\omega)^2} + \frac{g_m^{\ -1}}{1 + (C_{on}\omega)^2} \tag{A.14}$$

$$Q_4 = R_{eq,1}(1 + (\frac{1}{R_{eq,1}C_{eq,2}\omega})^2)(C_{eq,2} + C_{off})\omega \tag{A.15}$$

In general the time-averaged impedance would be described by the following equation

$$C_{equal} = \frac{C_{equal1} + C_{equal2}}{2} \tag{A.16}$$

$$R_{equal} = \frac{R_{equal1} + R_{equal2}}{2} \tag{A.17}$$

Subject: Re: Copyright Permission request for MS Thesis Dissertation (San Jose State Univ)
From: j.hansson@ieee.org
Date: Tue, 7 Aug 2007 11:59:40 -0400
To: "Maryam Tabesh" <maryam.tabesh@gmail.com>
CC:

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Figures Number 1, 2 and 3.

Curty, J.-P.; Joehl, N.; Dehollain, C.; Declercq, M.J., "Remotely powered addressable UHF RFID integrated system," Solid-State Circuits, IEEE Journal of , vol.40, no.11, pp. 2193-2202, Nov. 2005
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RF-ICS Laboratory, EE Department,
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Tel: (510) 845-1715

Subject: RE: Question About your paper:"Antenna Design for UHF RFID Tags"
From: "Rao, KVS" <KVS.Rao@intermec.com>
Date: Sun, 5 Aug 2007 11:50:40 -0500
To: "Maryam Tabesh" <maryam.tabesh@gmail.com>

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From: Maryam Tabesh [mailto:maryam.tabesh@gmail.com]
Sent: Fri 8/3/2007 4:41 PM
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From: "Jari Curty" <jari.curty@gmail.com>
Date: Mon, 20 Aug 2007 16:25:20 +0200
To: "Maryam Tabesh" <maryam.tabesh@gmail.com>

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Direct Phone: 480-792-7894
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Date: Fri, 03 Aug 2007 22:33:11 -0700 (PDT)
To: Maryam Tabesh <maryam.tabesh@gmail.com>

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