2008

RF modeling of passive components of an advanced submicron CMOS technology

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RF MODELING OF PASSIVE COMPONENTS OF AN ADVANCED SUBMICRON

CMOS TECHNOLOGY

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Electrical Engineering

by

Nidhi Vashisht

May 2008

UMI Number: 1458155

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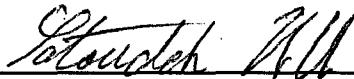
APPROVED FOR THE

DEPARTMENT OF ELECTRICAL ENGINEERING

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04/30/08

ABSTRACT

RF MODELING OF PASSIVE COMPONENTS OF AN ADVANCED SUBMICRON CMOS TECHNOLOGY

by Nidhi Vashisht

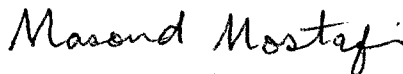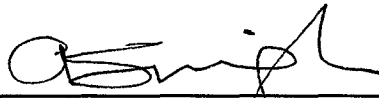The rapid development of wireless communication market has fueled a large demand for the use of high performance passive circuits in the design of radio frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs). Passive elements are a crucial part of any RF circuit, which has prompted a great deal of effort towards the use of on-chip passive components. In this dissertation, in-depth study on various characteristics of on-chip passive devices based on fundamental electromagnetic principles is performed. It encompasses activities of modeling passive devices, performing iterative techniques used to optimize the layout, and analyzing various performance limitations in complementary metal oxide semiconductor (CMOS) technologies. In addition the impact of different geometries on the passive device performance is analyzed.

ACKNOWLEDGEMENTS

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Chapter 1

Introduction

1.1 Radio Frequency Integrated Circuits

For decades, radio frequency (RF) transceivers have been successfully implemented on printed circuit boards. On printed circuit boards discrete active components (transistors on semiconductor substrate) and passive components (spiral inductors, capacitors, and transformers) are easily combined for proper impedance matching and optimum performance.

As the commercial and military systems sophistication grows, integrating multiple microwave/RF functions into a single housing increases. The tremendous growth in commercial wireless and wired communication markets has generated huge interest in RFICs [1]. Silicon integrated circuits provide low-cost, high yield, small form factors, and potential to combine analog and digital circuits. These advantages suit well to meet the emerging demand for highly integrated devices required in consumer electronics and this is the reason why consumer market favors silicon technology.

In the field of wireless radio frequency circuit design and fabrication, with emphasis on highly integrated transceivers for modern technology, the challenge for the design engineer is to house as many components on a single chip while maintaining the performance and standards. Basic architecture of a traditional transceiver system is shown in Figure 1. The quest for low cost solutions in the

commercial market has spurred a desire to implement RFICs in standard CMOS

technology. Although the CMOS RFICs have many advantages of low cost, low

power, and high integration, they suffer from the poorer quality factor for passive

components than the gallium arsenide (GaAs) technology. The poor performance

of silicon substrate is attributed to the low substrate resistivity. The silicon

resistivity for CMOS can minimum go to 0.01Ω-cm and for bipolar its 1Ω-cm

depending upon the dopant concentration in silicon wafer. Range for typical

resistivity of silicon is 1Ω-cm to 10Ω-cm for bipolar technology and 0.01Ω-cm to

1Ω-cm for CMOS technology. Currently, submicron CMOS technologies exhibit

sufficient performance for radio frequency applications in the 1-5GHz range,

making them ideal for commercial RFICs applications.
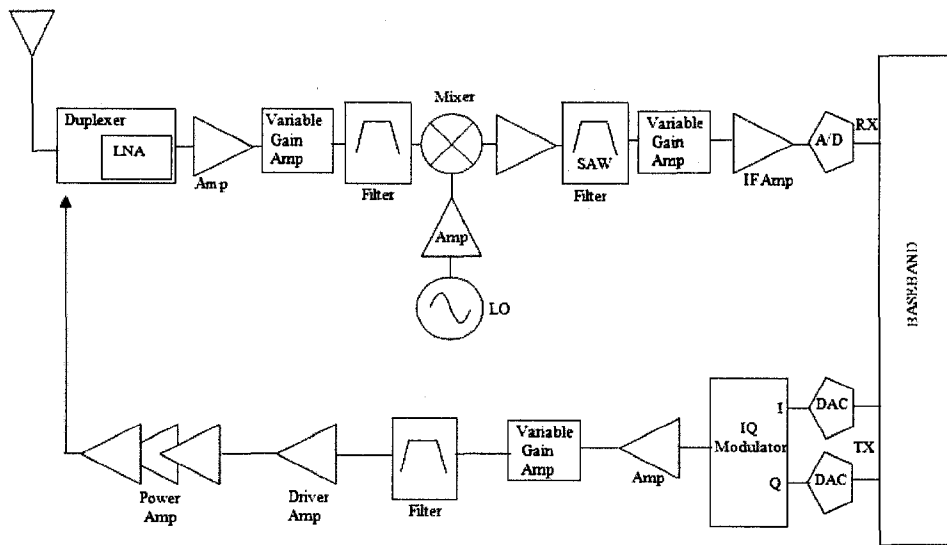
Figure 1: Traditional Transceiver Architecture

The advantages of integrating radio frequency circuits are few external components, the smaller size of the circuit board and lesser power consumption. These advantages are especially significant in the rapidly expanding communication services market where portability and long battery life are essential. The common circuit elements (transistors, diodes, and resistors) are easily integrated on the chip but high quality on-chip inductors, transformers, and large capacitors are not commonly available. All major components in a transceiver front-end system, as shown in Figure 1, need inductors, capacitors, and transformers for input/output and interstage matching. These components account for a large fraction of the area and cost of RFICs and, therefore, need to be accurately modeled and optimized.

1.2 Passive Components in RFIC- The Bottleneck

Driven by compact handsets and portable electronics, on-chip passive components continue to exploit the advances in semiconductor process to reduce the occupied space with higher performance at lower cost. Historically, passive components got little attention compared to the active devices. The new era of RF CMOS technology altered this scenario completely. The RF circuits generally have many passive components required for input/output impedance matching. Passive devices like interconnect, inductor, capacitor, and transformer are new to the silicon technology. Successful RF design depends critically on the detailed understanding of the passive device characteristics.

Radio frequency integrated circuit designers have a very limited palette of passive devices. This thesis examines design and optimization of on-chip interconnects, inductor, capacitor, and transformer. The optimization of passive devices includes maximizing the quality factor through a reduction of the resistive losses and the capacitive or inductive parasitic.

1.3 Purpose and Organization of the Thesis

This thesis is focused on modeling RF passive components using a $0.13\mu m$ CMOS technology. The characteristics of the passive component are verified with lumped model and layout of the test structures in Cadence. The electromagnetic (EM) simulation approach is followed in the thesis for generating component S-parameters. Models of component structures are provided to the simulator along with material properties and port definitions. The EM simulations are used to determine the component performance over the frequency range of interest and to provide lumped model S-parameters. Lumped mode circuits are designed with ideal capacitors, inductors, and resistors to accurately represent the embedded RF module components with all the related properties. Variations between data from various geometries for different parts are evaluated by comparing the component values, quality factors, and resonant frequencies.

Chapter 2 provides the electromagnetic theory and the wave propagation analysis on silicon substrate. It also explains the loss mechanism in silicon

substrate along with a CMOS substrate example. Substrate model is defined in the simulation software and different simulation modes are discussed.

Chapter 3 is devoted to the passive components design and analysis with Agilent Momentum. The Agilent ADS layout for passive components is performed with the simulation results in the form of S-parameters. Lumped circuit is developed for all the passive devices and the optimized values for the equivalent circuit components are obtained.

Chapter 4 focuses on the layout of passive components in Cadence 0.13μm CMOS process. Ground-Signal-Ground (G-S-G) type of probing is explained and de-embedding techniques are discussed. Design example of low noise amplifier using inductor test structures lumped model is also presented in this chapter.

Chapter 5 concludes the thesis. It summarizes the contributions and future work of the RF passive component modeling.

Chapter 2

EM Theory and Silicon Substrate Characteristics

This chapter reviews the electromagnetic theory based on Maxwell's equations [2]. Section 2.2 explains the wave propagation models on silicon along with the various loss mechanisms in substrate. Section 2.3 examines the CMOS substrate used for this thesis and substrate model definition in simulation software. Section 2.4 highlights the modeling techniques used for this thesis.

2.1 Electromagnetic Plane Waves

Maxwell's equations describe electromagnetic waves interacting throughout space and can potentially describe the on-chip metallization, the substrate, and even the oxide layers. Maxwell's equations imply that charge distribution and current flow cannot occur without influence from and influence upon the distribution of charges and currents in the neighborhood. The principles of EM waves are based on relationships between electricity and magnetism. A changing magnetic field will induce an electric field and a changing electric field will induce a magnetic field.

In the far field of free space, electric and magnetic waves are always perpendicular to each other and both are normal to the direction of propagation of the wave. This type of wave is known as the Transverse Electromagnetic (TEM) wave.

Maxwell's equations in time domain are defined by:

$$\nabla \times E = -\delta B / \delta t \qquad (2.1)$$

$$\nabla \times H = J + \delta D / \delta t \qquad (2.2)$$

$$\nabla \cdot D = \rho \qquad (2.3)$$

$$\nabla \cdot B = 0 \qquad (2.4)$$

$D = \varepsilon E$ represents electrical induction, E is the electric field, $B = \mu H$ is the magnetic induction, H is the magnetic field, $J = \sigma E$ is the current density, and ρ is the charge density.

2.2 Silicon as Substrate

Silicon technology is, at present, the most popular choice for RFIC design. The dielectric constant of silicon is high and its variation with temperature and frequency is minimal. Silicon has better surface smoothness, good thermal conductor (three times compared to GaAs), multi-interconnect metal layers, low cost, and can achieve higher chip integration [3]. Multi-interconnect metal layers are an important aspect of silicon process. These multi layers helps in building RF passive devices such as interconnects, spiral inductors, capacitors, and transformers.

On the other hand RF designs on silicon substrate has to deal with the substrate losses. This disadvantage leads to high power consumption. Another drawback with higher level of integration is to cope with crosstalk and parasitic electromagnetic signal propagation through the substrate. The lower resistivity of

silicon substrate compared to GaAs is a major disadvantage. The silicon substrate is prone to RF losses in contrast to GaAs. At frequencies beyond 1GHz, the skin depth for 10Ω-cm silicon exceeds the typical substrate thickness so that RF losses extend over the entire substrate. Thus RF systems on a silicon chip have considerable substrate losses because parasitic EM signal propagation is present through the substrate [4].

2.2.1 Wave Propagation in Silicon Substrate

Based upon the various resistivity values associated with losses in silicon substrate and frequency ranges, wave propagation mode in silicon can be divided into three regimes [5].

- Quasi-TEM Mode: This mode is very close to TEM mode where the product of frequency and silicon resistivity is high and substrate acts as a dielectric with small dielectric loss tangent.

- Slow-Wave Mode: In this mode the product of frequency and silicon resistivity is moderate and surface wave propagates along the transmission line with propagation velocity lower than the Quasi-TEM mode.

- Skin-Effect Mode: Silicon substrate in this mode acts like a lossy conductor or a ground plane because the product of frequency and silicon conductivity is very high.

CMOS RF applications fall within the Slow-Wave Mode or the Skin-Effect Mode.

2.2.2 Losses in Silicon Substrate

The lack of an accurate model for on-chip passive devices presents one of

the most challenging problems for silicon based RFIC designers. For passive

component design and optimization, a compact physical model is required. The

difficulty of physical modeling comes from the complexity of radio frequency

phenomena like the eddy current effect and the substrate losses in the CMOS

process [6]. The various loss mechanisms in the CMOS technology are

summarized in Figure 2. These effects are not understood completely thus it is

very difficult to model all the loss mechanisms. A lumped element approach is

used to model these effects.
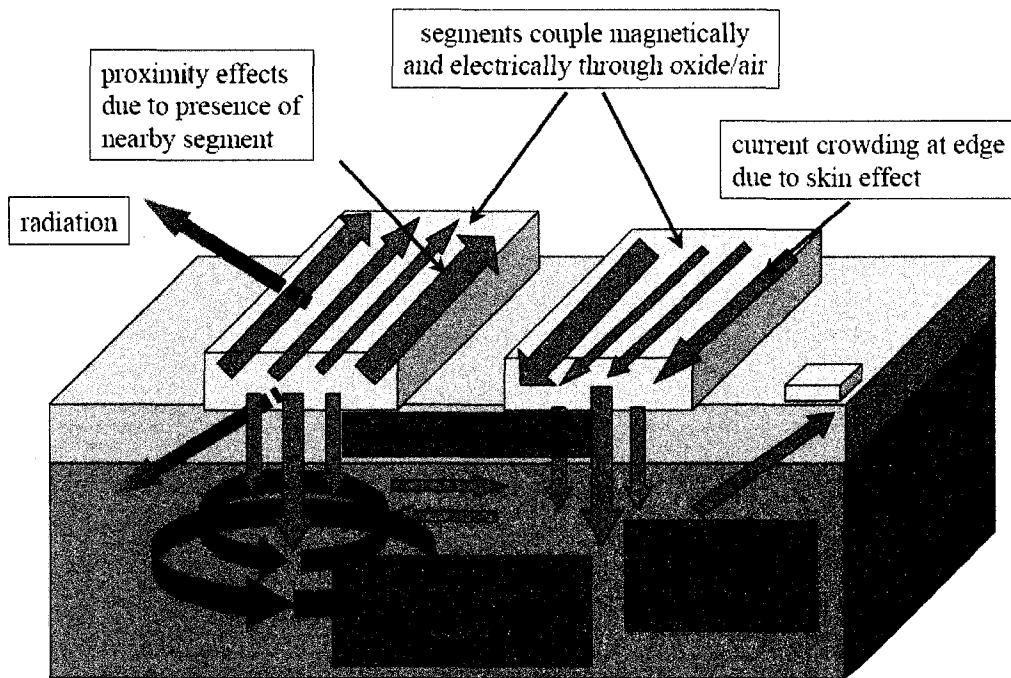
Figure 2: Losses in Silicon Substrate

- Metal Losses: At low frequencies, the current density is distributed uniformly in the metal trace. At high frequency, the current distribution in the metal layer changes due to the eddy current, also known as skin effect [7, 8]. Metal trace resistance (R) is defined by:

$$R = \rho \frac{L}{tW} = R_s \frac{L}{W} \qquad (2.5)$$

Loss due to metal trace can be minimized by using metals with very low resistivity, increasing the cross sectional area of the trace (tW) or reducing the overall trace length (L). Metals primarily used in silicon process are aluminum or copper. Process used for this thesis employs copper for all metal layers.

- Skin Effect Losses: Skin effect is the effect in which the effective cross-section of the conductor shrinks with the increase of the frequency. At low frequencies, the magnetic energy of the EM waves is stored inside as well as outside the conductors. As frequency increases, the current flow is mostly concentrated near the surface of the conductor and the EM fields attenuate substantially when they pass through the conductor. Currents tend to accumulate at the skin of conductors as the alternating currents take the path of least impedance shown in Figure 3. Skin depth, where μ and σ stand for the permeability and the conductivity of the conductor respectively, ω represents the angular frequency, which is the product of 2π and the operating frequency is defined by:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \frac{1}{\sqrt{f\pi\mu\sigma}}$$ (2.6)

The series resistance of the metal trace becomes frequency dependent and

inductance value reduces as the frequency increases.
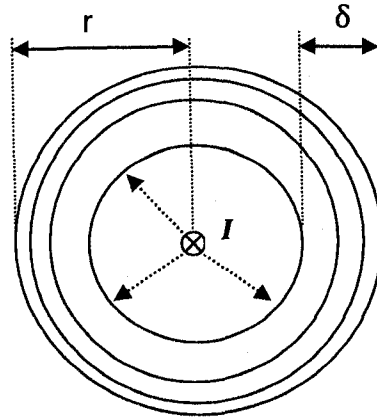
Figure 3: Skin Effect in Circular Cross-Section Conductor

- Substrate Losses: Silicon resistivity varies from nonconductive (ρ ~10kΩ-

  cm) for lightly doped silicon to conductive (ρ ~10-3Ω-cm) for heavily

  doped silicon. The conducting nature of the silicon substrate leads to

  losses. Current gets injected into the substrate through various

  mechanisms shown in Figure 4. Large passive devices such as inductors,

  capacitors, and transformers introduce displacement current in the

  substrate. The resistors and capacitors in the shunt block are used in

  lumped models to account for this displacement current effect. The

  current flowing through the conductor induces eddy currents in the

  substrate. This magnetic field penetrates through the substrate.
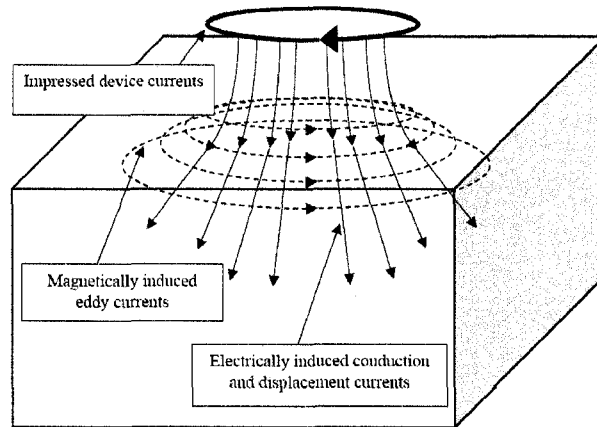
Figure 4: Currents Induced in Silicon Substrate

In Figure 5, metal traces carrying eddy current are shown from the
outermost turn to the innermost turn. The current carried in the trace is
I_{ind}, which flows in the direction as indicated. The intensity of the
magnetic field is highest at the center of the spiral and oriented
perpendicular to the page. Eddy currents flow in direction so as to oppose
the original change in magnetic field.
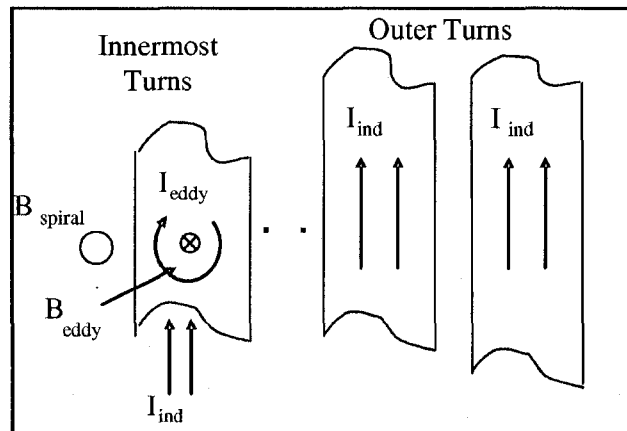
Figure 5: Eddy Current in Inductor Metal Trace

2.3 Modeling Techniques

Agilent Momentum is used for the modeling of various test structure designs performed in this thesis. Modeling is achieved by creating discrete elements that took account of the substrate properties [9].

Agilent Momentum is based on a numerical technique called Method-of-Moments. This technique is used to solve Maxwell's equations for planar structures embedded in a multilayered dielectric substrate. The Method-of-Moments technique starts from an integral equation formulation of Maxwell's equation with the currents flowing on the metallization as basic unknowns [10]. The concept of Green functions is used to characterize the behavior of the substrate. Momentum can operate in two simulation modes: Full-Wave Mode and Quasi-Static Mode. Full-Wave Mode includes microwave radiation effect using general frequency dependent Green functions that fully characterize the substrate. Quasi-Static Mode is used for designs that are geometrically complex, electrically small, and do not radiate.

2.4 Substrate Definition

Technology process parameters such as substrate resistivity, number of metal layers, distance between metal layers, and metal layer thickness are all set by technology and cannot be altered [11].

Eight metal layer (M1-M8) CMOS substrate for 0.13μm technology of a foundry is used for this thesis as shown in Figure 6. Modeling substrate is

initiated by defining the substrate. The substrate definition includes the number of layers, position of each layer, and composition of each layer. Silicon substrate permittivity and conductivity value are required. For metal layers the required parameters are conductivity and metal thickness. The metal layers are interspaced by a dielectric layer of via (via1-via7), where via thickness equals that of the metal. For the thesis, the metal layer is copied into seven horizontally identical layers. The metal layers are interspaced by vias with a thickness equal to that of the metal layer. Finally, the backing plate of the silicon substrate is represented by the closed boundary (ground). At the top of silicon substrate the free space is set to an open boundary. This completes the substrate model.

For the thesis design purpose, Quasi-Static Mode is used, which provides accurate electromagnetic simulation performance at radio frequencies. The initial step is to choose the desired layout design for a passive component. Some physical parameters of the process are required to perform an EM simulation using Agilent ADS. The metallization layers needed to create the inductors have to be mapped to the silicon process technology. In order to reduce the loss and improve the quality factor (Q), the metallization layer with the lowest loss is chosen for the design.

Passivation	
IMD M8	Cu M8
IMD V78	V7
IMD M7	Cu M7
IMD V67	V6
IMD M6	Cu M6
IMD V56	V5
IMD M5	Cu M5
IMD V45	V4
IMD M4	Cu M4
IMD V34	V3
IMD M3	Cu M3
IMD V23	V2
IMD M2	Cu M2
IMD V12	V1
IMD M1	Cu M1

PMD   WCN
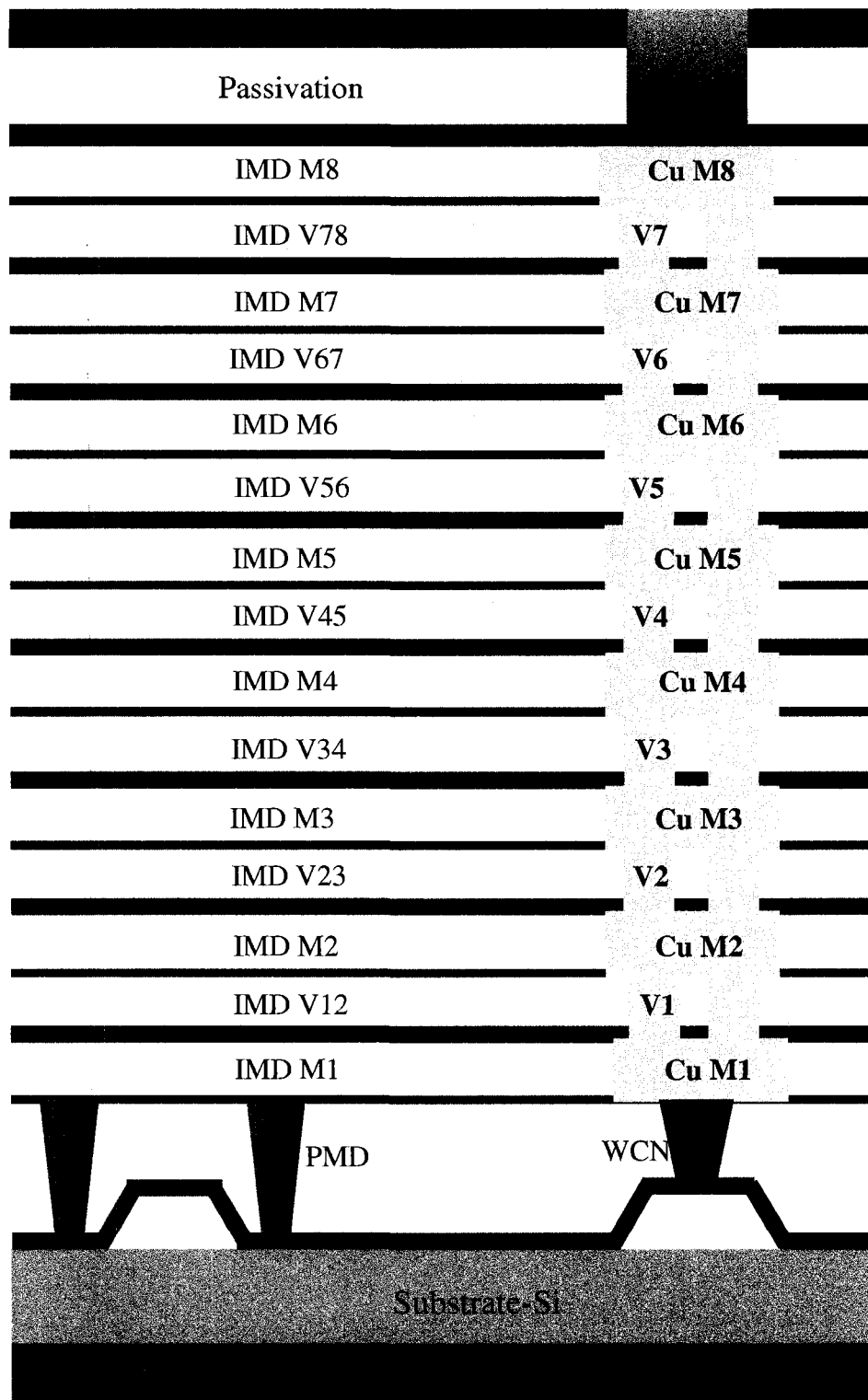
Substrate-Si

Figure 6: CMOS Substrate for Designing Test Structure

In this thesis, the passive structures are realized on the top metal layer to reduce eddy current losses in the substrate and to reduce the capacitive coupling to the substrate. It is also advantageous to choose the metal layer as far away from the silicon substrate, which positions magnetic fields laterally to the substrate. In submicron CMOS technologies, the top metal layer conductivity due to its largest thickness is higher than other metal layers.

In the simulation setup two internal ports are inserted, one on each side of the passive device. The finite thickness of the metal trace is taken into account during the simulation where both layers are connected using vertical metallization planes (via). The layout in ADS is simulated and S-parameter is generated, which contains sufficient information to characterize each individual component.

A simple fully scalable lumped element model is advantageous in describing the electrical device characteristics and for accurate simulation of on-chip passive devices. The behavior of RF passive component is characterized by frequency independent lumped model. Parameter extraction technique is used to obtain the lumped model parameters, which requires selection of initial values for the model and then modifying them iteratively until the differences or error between the calculated S-parameters and the measured ones reach a bare minimum. The lumped model can be used rapidly to optimize the electrical performance for RFIC applications. In the thesis, the accuracy of the lumped element model is evaluated for variations in metallization thickness and length on silicon substrate [12].

Equivalent lumped circuit model help in cost and performance evaluations to be performed early in the design process. Usually, the lumped element model cannot be used in very broad frequency band. Ideally, lumped element model should account for eddy current effect in the metal conductor, substrate losses of the silicon substrate, capacitance between the metal trace and the substrate, substrate ohmic loss, and substrate capacitance [13, 14], as defined in Section 2.2. Thus, a model based on a lumped element equivalent circuit is an efficient and accurate way of representing a passive device.

2.5 Parameters of Interest for Passive Structures

2.5.1 Energy Storage

Energy stored in inductor and transformer is magnetic energy with i_L the instantaneous current through the spiral is defined by:

$$E_L = \frac{1}{2} L i_L^2 \qquad (2.7)$$

For inductor structures, as frequency increases, the series combination, shown in Figure 7, becomes more reactive and the phase difference between V_s and I_s approaches 90° [15].
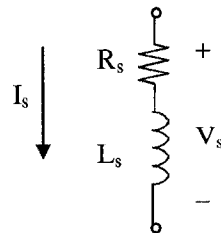
Figure 7: Loss in Inductor Structure

Energy stored in capacitor is electrical energy with v_c the instantaneous voltage across the capacitor is defined by:

$$E_C = \frac{1}{2} C v_c^2 \qquad\qquad (\,2.8\,)$$

The sinusoidal steady state of capacitor as a storage element can be presented as shown in Figure 8.
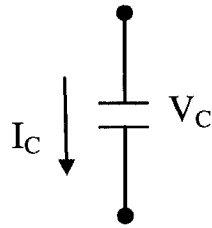
Figure 8: Capacitor Structure as Storage Element

2.5.2 Self-Resonant Frequency

The frequency at which quality factor (Q) vanishes to zero is defined as self-resonant frequency (Fsr). A device is said to be self-resonant when the peak magnetic and electric energies are equal. Beyond this frequency, the component exhibits a negative reactance where it is useless. For inductors, at self-resonant frequency the inductance (L) value passes through a zero and capacitive effects start to dominate the behavior of the inductor. In most of the on-chip spiral inductors, quality factor reaches a maximum value at about half the self-resonant frequency. For capacitors, at frequencies above the self-resonant frequency, no net electric energy is available from a capacitor to any external circuit.

The self-resonant frequency of a passive component can be affected by two factors: device capacitance to the substrate and capacitance between the different turns.

2.5.3 Quality Factor

Quality factor can be defined as 2π times the ratio of energy stored to the energy dissipated in each cycle for a transformer modeled with RLC tank circuit. Material with high dielectric constant helps in achieving higher capacitance density. Quality factor is given by:

$$\text{Quality Factor} = \frac{\text{Energy Stored}}{\text{Energy Lost per Cycle}} \qquad (2.9)$$

2.6 Summary

This chapter covered the principle of electromagnetic theory for transmission lines. The fast growing demand of using silicon as a substrate is being discussed and wave propagation modes are explained. Substrate losses and substrate model definition are also included in this chapter. The defined substrate model and loss effects will be utilized in the next chapter to develop the test structure model for various passive components.

Chapter 3

Passive Structures

Chapter 2 introduced the electromagnetic theory behind the transmission line structures and the major losses encountered using silicon as substrate. The CMOS substrate was defined, which will be used as substrate model for test structures. The purpose of this chapter is to design, simulate, and characterize passive structure lumped models using ADS Momentum. The structures developed in this chapter will be used in Chapter 4 to layout the structures in Cadence for fabrication purpose.

3.1 On-Chip Interconnect

With high operating frequencies, it has become important to account for magnetic field effect and skin effects for on-chip interconnect. In the past, interconnect structures were modeled as a single lumped capacitor with a capacitance value proportional to the area of the wire. With technology improvements, the line widths got smaller and the resistance of interconnect increased. Inductance of on-chip interconnects has to be considered during circuit simulation. Interconnect delay is the main bottleneck for increasing the operating frequency of a fully integrated circuit [16]. Hence, highly accurate interconnect analysis has become essential.

The microstrip transmission line structure on silicon consists of a metal trace above a conducting or ground plane with the substrate and intermetal oxide layers sandwiched between the two conductors, as shown in Figure 9.
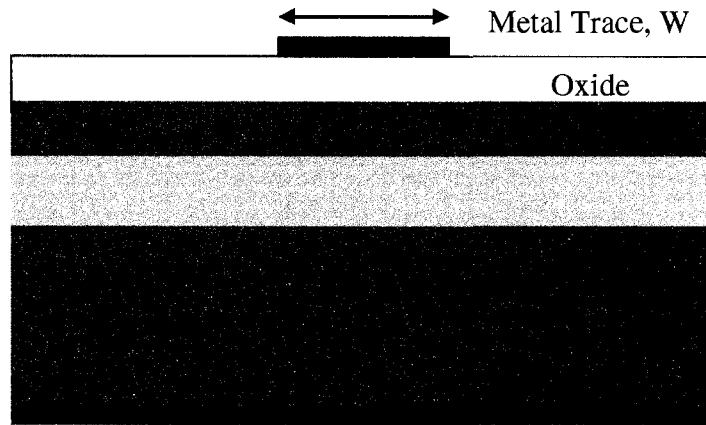
Figure 9: Microstrip Interconnect on Silicon

3.1.1 Test Structure Design of Interconnect

Interconnect test structure on silicon substrate with resistivity of $19\Omega cm$ is developed using conductor lengths (l) of $200\mu m$ or $400\mu m$ and widths (w)$10\mu m$ or $20\mu m$. The topmost metal layer has lower sheet resistance and suffers less loss from the substrate because of its higher thickness. Also it is commonly utilized for routing critical high frequency paths. Therefore, test structures are designed on the top metal layer using $0.13\mu m$ CMOS process.

The two-port scattering parameters of interconnect are directly computed from the circuit simulation in Agilent Momentum over the frequency range of DC to 200GHz. The plots are presented in Figures 10-12. Considering the symmetry

of the interconnect test structure (Sij = Sji and Sii = Sjj), only S11 and S21 magnitude/ phase are presented.

As the length and the operating frequency increases for interconnect test structure the total impedance of the interconnect increases. S11 is proportional to the length of metal trace as well as the frequency. S12 measures the signal transmission and follows an opposite trend of S11. As a result, the reflection increases and transmission decreases.
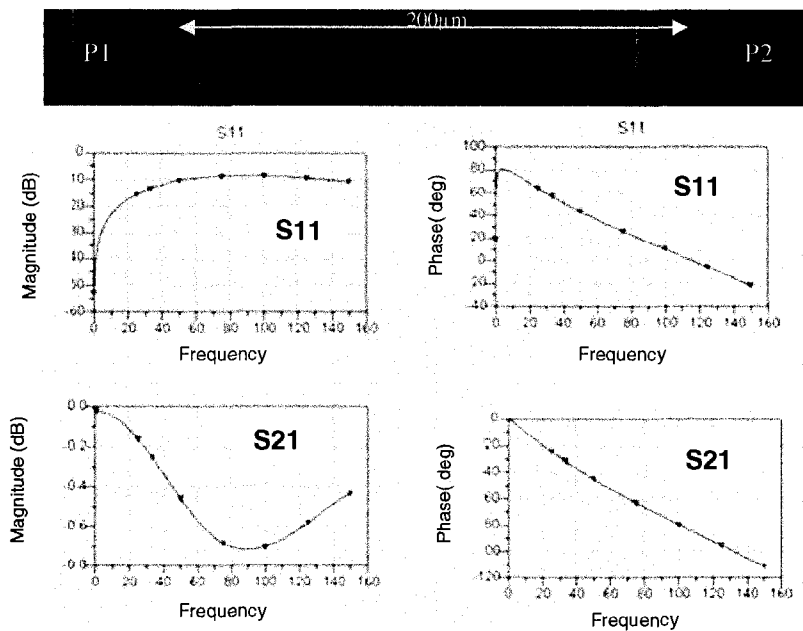
Figure 10: Interconnect Layout and Simulated S-parameter (Length=200μm and Width=10μm)
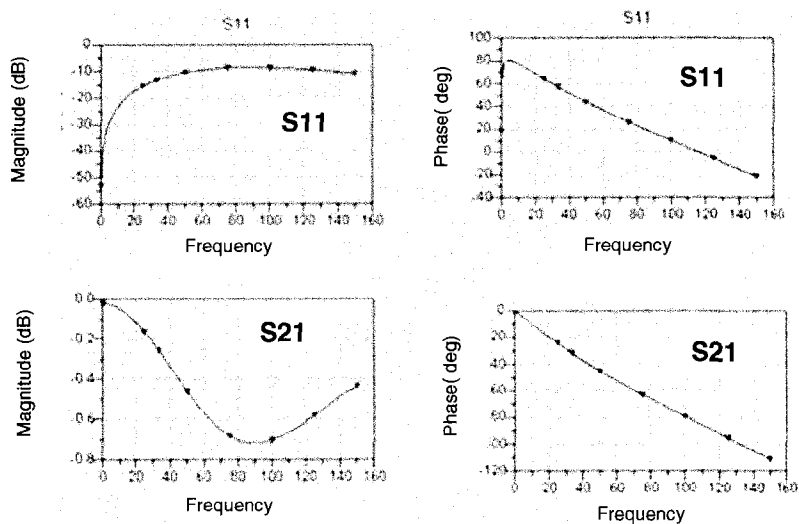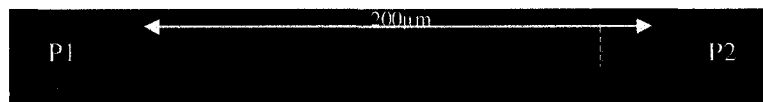
Figure 11: Interconnect Layout and Simulated S-parameter (Length=400μm and Width =10μm)
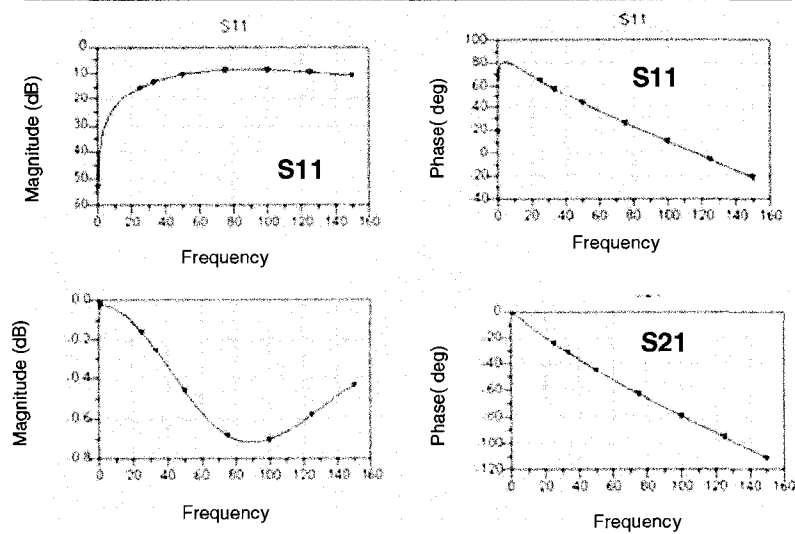
Figure 12: Interconnect Layout and Simulated S-parameter (Length=200μm and Width=20μm)

3.1.2 Interconnect Lumped Model

Equivalent circuit model parameters are extracted from the frequency

dependent quasi-static solution of the interconnect characteristics. The model of

the shunt admittance (Y) is based on the physical substrate structure and consists

of ideal R, C, and L components. The abstract schematic view in Figure 13

represents the physical structure of interconnects.
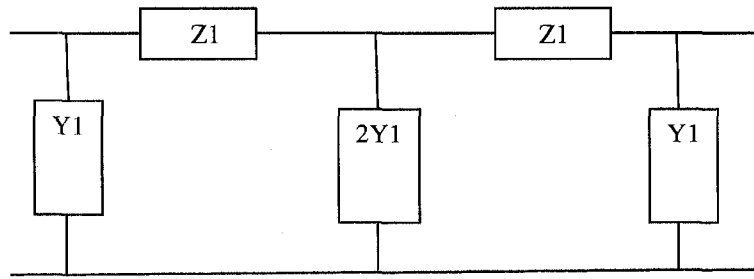
Figure 13: Two-π Schematic Block Diagram

Interconnects can be modeled as single-π circuit or double-π circuit. In

the RF region, single-π is not suitable for long interconnect lines as the distributed

effect begins to appear. According to the notion described by Edwards and Steer

[17], when the length of interconnect is less than 1/20 of the wavelength, the

signal can be deemed to be constant along the entire length.

The model used for the thesis is based on the single-π model, by cascading

two lumped blocks together, as illustrated in Figure 14. This double-π model is

adequate in representing RF effects with better accuracy and is also continuous

across different physical dimensions of interconnects. Referring to Figure 14, Ls1

and Ls2 describe the ideal series inductance. Rs1 and Rs2 represent ideal series

resistance on the metallization. The series components Rsk1, Rsk2, Lsk1, and

Lsk2 characterize the skin effect as well as the eddy current effects. At low

frequencies, the currents mostly pass through Lsk, while as the frequency rises,

more currents shift through the Rsk. At very high frequencies the substrate losses

also dominate. Substrate loss for interconnect is modeled by the resistor and

capacitor network that consists of Cox1, Cox2, Csub1, Csub2, Rsub1, and Rsub2.

Cox1 and Cox2 represent the oxide layer capacitances between the conductors

and the bulk substrate. The capacitive losses and resistive losses in the silicon

substrate are shown by a parallel combination of Csub1 or Csub2 and Rsub1 or

Rsub2. Cf1 and Cf2, accounts for the fringing effect in the oxide layer and the

substrate. Fringing effect comes into play when the height of the conductor is

similar to its width.

Single π
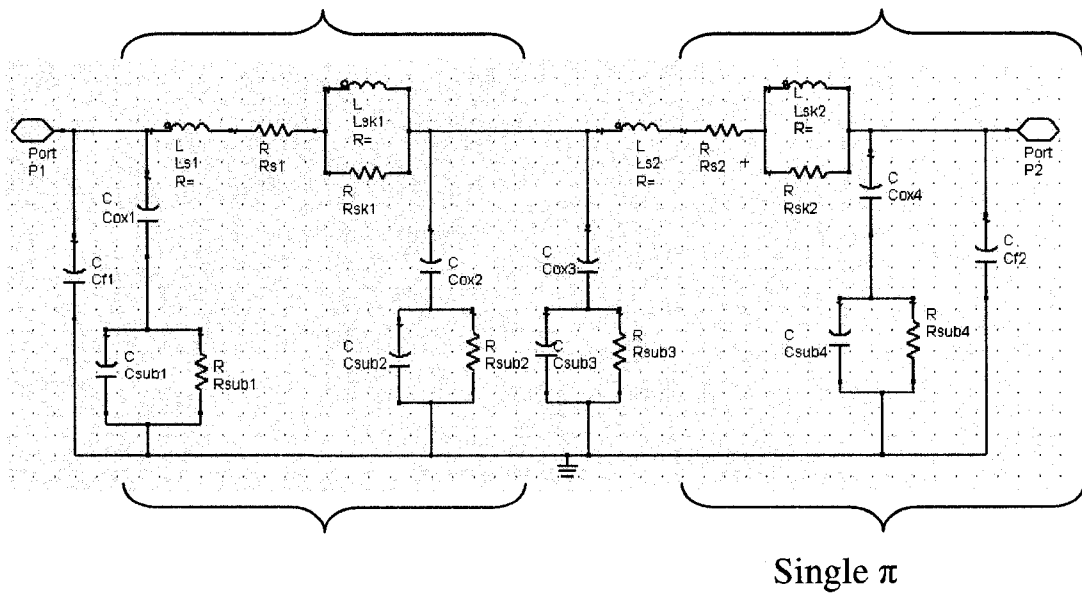
Figure 14: Two-port Lumped Model for Interconnect Test Structure

The parameter extraction technique starts with an initial value for all the

ideal components in the lumped model and updating the values until a good match

is obtained between the simulated and extracted S-parameter. The fit frequency

range is appropriate before the self-resonant frequency. A good agreement is

obtained between the EM simulations and interconnect lumped model up to the

self-resonant frequency, as summarized in smith chart shown in Figure 15. By

optimizing the simulated S-parameters to the cascaded single-π lumped model S-

parameters, the value of each component are obtained for interconnect test

structures. The final values of lumped model components obtained by extraction

technique are given in Table 1.
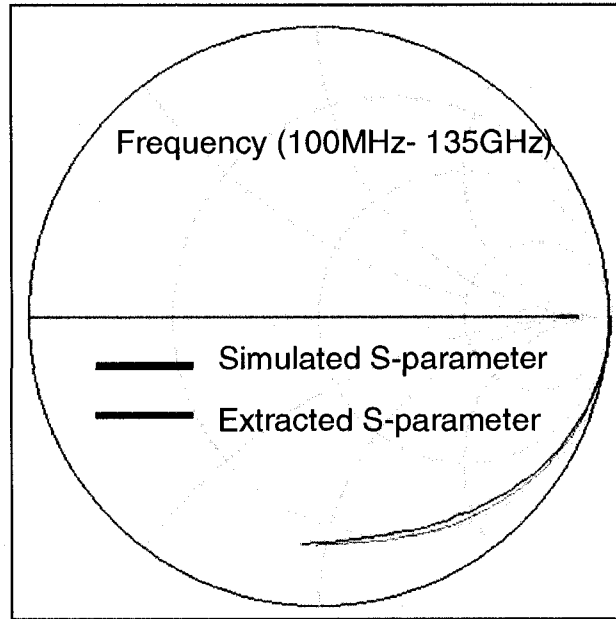
Figure 15: Comparison of Simulated S-parameter and Lumped Model Extracted
S-parameter for Interconnect Test Structure

The important parameters for interconnect are inductance (L), quality

factor (Q) and series resistance (R) [18]. They can be defined as:

$$L = \frac{\text{imag}\left[Z11 - \frac{Z12 * Z21}{Z22}\right]}{2\pi f} \qquad (3.1)$$

$$Q = \frac{\text{imag}\left[Z11 - \frac{Z12 * Z21}{Z22}\right]}{\text{real}\left[Z11 - \frac{Z12 * Z21}{Z22}\right]} \qquad (3.2)$$

$$R = \text{real}\left[Z11 - \frac{Z12 * Z21}{Z22}\right] \qquad (3.3)$$

Table 1: Extracted Parameters for Interconnect Lumped Models

Parameter	Units	l:200μm w:10μm	l:400μm w:10μm	l:200μm w:20μm	l:400μm w:20μm
Fsr	Hz	1.31E+11	6.02E+10	1.16E+11	5.40E+10
Ls1	nH	0.09	0.20	0.08	0.19
Rs1	Ω	0.24	0.43	0.08	0.27
Lsk1	nH	0.005	0.130	0.001	0.10
Rsk1	Ω	0.514	0.424	0.85	0.4
Ls2	nH	0.09	0.20	0.08	0.19
Rs2	Ω	0.16	0.27	0.11	0.15
Lsk2	nH	0.007	0.019	0.008	0.014
Rsk2	Ω	2.76	2.98	2.83	2.97
Cox1	F	1.13E-15	3.18E-15	1.57E-15	3.23E-13
Cox2	F	1.48E-12	1.23E-12	1.12E-12	1.58E-12
Cox3	F	5.74E-14	1.16E-13	5.06E-15	1.07E-14
Csub1	F	2.77E-13	5.92E-12	5.57E-12	6.49 E-15
Csub2	F	4.47E-14	1.1 E-16	1.39 E-14	2.49 E-14
Csub3	F	4.7E-15	2.96 E-14	9.26 E-14	1.41 E-12
Rsub1	Ω	4993	6882	7776	5000
Rsub2	Ω	3956	3580	4030	5000
Rsub3	Ω	3053	5000	5000	3500
Rsub4	Ω	1107	2547	2597	1720
Cf1	F	2.56E-15	5.8 E-15	1.7 E-15	6.73 E-15
Cf2	F	2.3E-15	1.68 E-15	1.8 E-15	1.05 E-14

3.1.3 Interconnect Parameter/ Result Analysis

Inductance, quality factor, and resistance of interconnect test structures are compared, as shown in Figure 16.
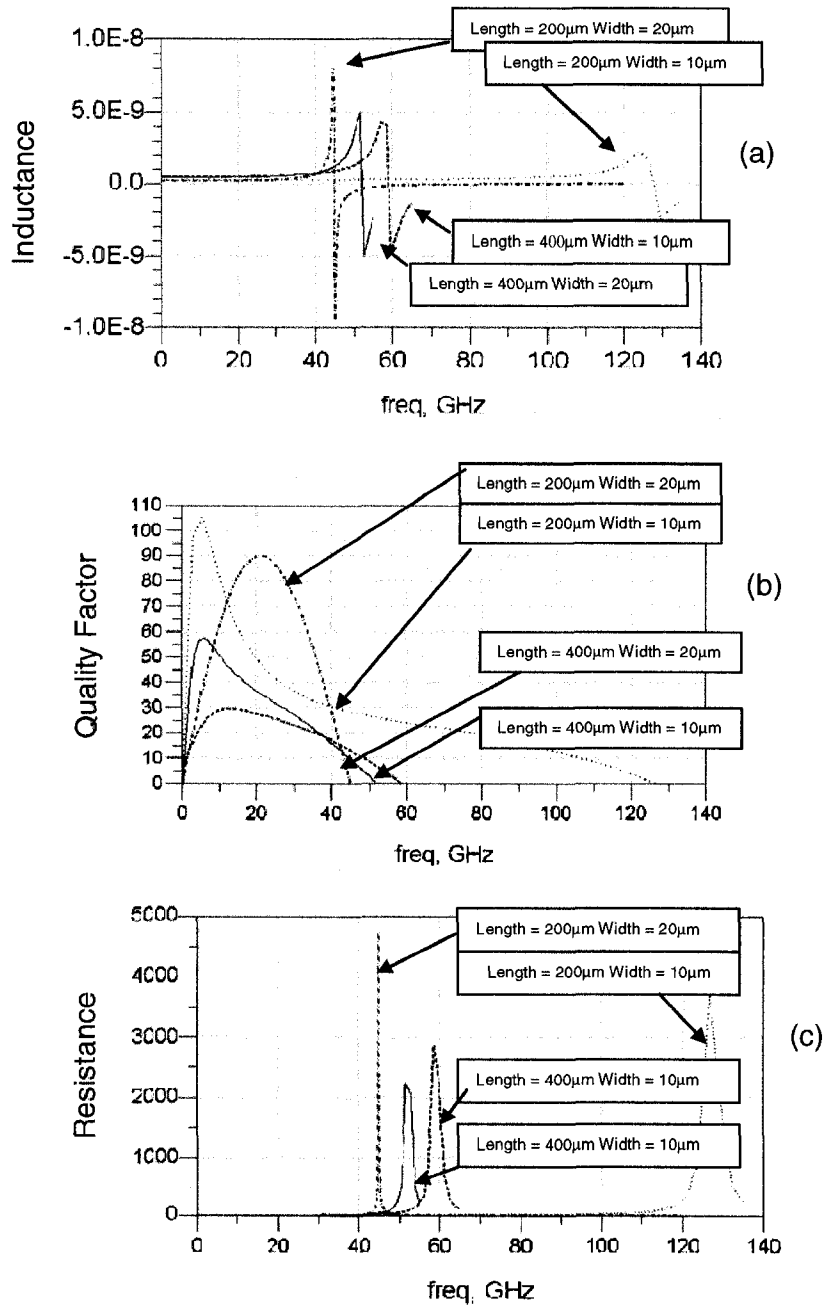
Figure 16: Interconnect (a) Inductance (b) Quality Factor (c) Resistance

Table 2 compares Ls and Lsk. They are proportional to the length and inversely proportional to the width of interconnect. When the length of the interconnect increases, the magnetic flux linkage and inductance increases.

Table 2: Comparison of Ls and Lsk vs. Length and Width of Interconnect

Length	Width	Ls1	Ls2	Lsk1	Lsk2
200 μm	10 μm	0.09 nH	0.09 nH	0.005 nH	0.007 nH
400 μm	10 μm	0.2 nH	0.2 nH	0.13 nH	0.019 nH
200 μm	20 μm	0.08 nH	0.08 nH	0.001 nH	0.008 nH
400 μm	20 μm	0.19 nH	0.17 nH	0.10 nH	0.014 nH

Table 3 compares the Rs and Rsk. They are proportional to the length and inversely proportional to the width. Series resistance increases with operating frequency.

Table 3: Comparison of Rs and Rsk vs. Length and Width of Interconnect

Length	Width	Rs1	Rs2	Rsk1	Rsk2
200 μm	10 μm	0.24 Ω	0.16 Ω	0.51 Ω	2.76 Ω
400 μm	10 μm	0.43 Ω	0.27 Ω	0.42 Ω	2.98 Ω
200 μm	20 μm	0.08 Ω	0.11 Ω	0.85 Ω	2.82 Ω
400 μm	20 μm	0.27 Ω	0.15 Ω	0.4 Ω	2.97 Ω

Analysis shows that Cox and Csub are proportional to the length and the width. Rsub is inversely proportional to both of the length and the width of metal strip because interconnect with a larger physical dimension has larger substrate losses. Cf, the fringing effect reduces when the area of interconnects decreases.

3.2 On-Chip Inductor

On-chip inductors are the largest silicon area consuming device for RFICs and play a crucial role in performance characteristics. The inductor is one of the key elements in RFIC designs. Scalable and accurate characterization of the behavior of spiral inductors is therefore invincible for RFIC designers [19].

Active inductors use active elements to transform the impedance of a capacitor to inductive impedance. The inductance of active inductors can be tuned but the noise generated by the active elements requires the use of an excessive amount of power to achieve low noise specs. Bond wires are also used as inductors, which exhibit higher quality factor. The very low series resistance of gold bond wires allows the feasibility of the unmatched phase noise performance but the range of realizable inductances, large parasitic capacitances and also the repeatability of the bonding process limit the use of bond wires. Therefore, the semiconductor industry is still hesitant to use the bond wire technique.

Passive inductors, designed in this thesis, are implemented with high characteristic impedance microstrip lines fabricated on an insulating (SiO2) layer that lies on top of a silicon substrate and lower ground plane. They exhibit good matching and permit a large range of inductances to be realized. On the other hand, they possess smaller quality factor values and a lot of substrate and metal layer parasitic effects make difficult modeling. The basics for the inductance calculation of the planar inductors were developed by Greenhouse in 1974 [20].

3.2.1 Test Structure Design of Inductor

The design process for inductors on silicon starts with the choice of a

spiral shape. The basic vertical and lateral geometries of the on-chip inductor

layout, shown in Figure 17, can result in numerous trades off.
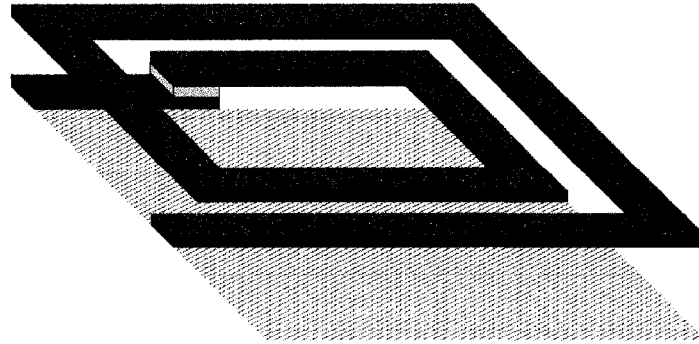
Figure 17: 3-Dimensional View of Spiral Inductor

Rectangular spiral, shown in Figure 18, is most popular in inductor design

because of the ease of their layout, and they have higher losses as compared to

polygon geometry. Polygonal spirals are octagonal, hexagonal, and circular.

Octagonal shapes can only be designed if technology allows 45 degree angles.
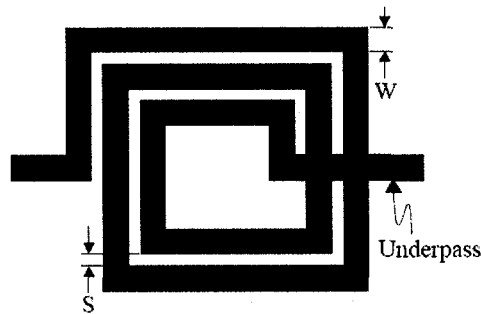
Figure 18: Rectangular Spiral Inductor

Inductor design parameters are completely specified by the physical

parameters as in Figure 19. Referring to Figure 19, n is the number of turns, w is

the metal width, s presents the edge-to-edge spacing between adjacent turns, dout

is the outer diameter and din is the inner diameter. Average diameter can be

calculated as davg = 0.5 (dout + din) or the fill ratio is defined as ρ = (dout-din)/

(dout+ din).
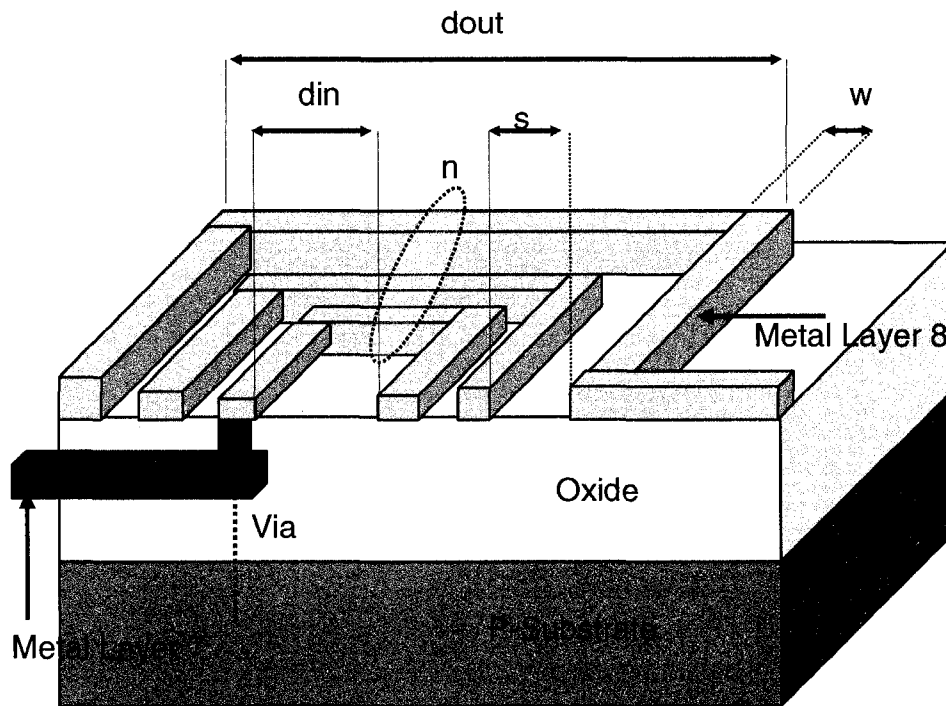
Figure 19: Design Parameters for Inductor Test Structure

For design with eight metal layers in CMOS technology, the top layer is

used for forming the spiral inductor and the next lower layer is for routing the

inner turn outward. The top layer increases the oxide thickness from the ground

so that the substrate effects are reduced and the self-resonant frequency improved.

The metal layers are separated from the silicon substrate with an oxide layer.

Typical sheet resistance of top metal layer is 20mΩ/sq and lower metal layers is

55mΩ/sq for the technology used for this thesis. The metal widths used in

inductor test structures are 10μm and 20μm, the separation between the different

windings is 0.5μm or 1μm and number of turns 2.5, 3.5, and 4.5. Each additional

turn adds to the magnetic field in phase with the previous turn. The magnetic

energy is stored mostly in the inner core of each winding.

The test structures are measured and simulated using Agilent Momentum

in 0-50GHz frequency range. In this frequency band, the structure is electrically

small, which justifies the usage of the momentum RF mode. The momentum

layouts for rectangular spiral inductor and simulated S-parameter are shown in

Figures 20-21. The momentum layouts and S-parameter for octagonal spiral

inductor are shown in Figures 22-23.
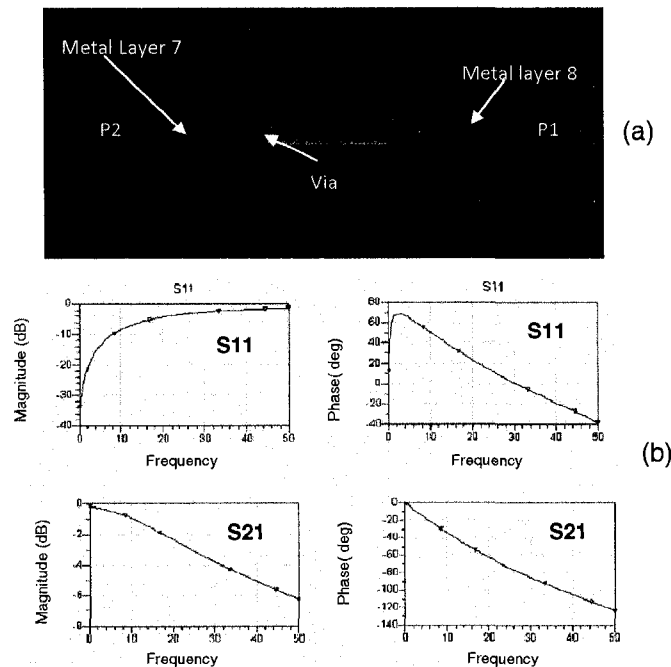
Figure 20: Rectangular Spiral Inductor (a) ADS Layout (b) Simulated S-parameter
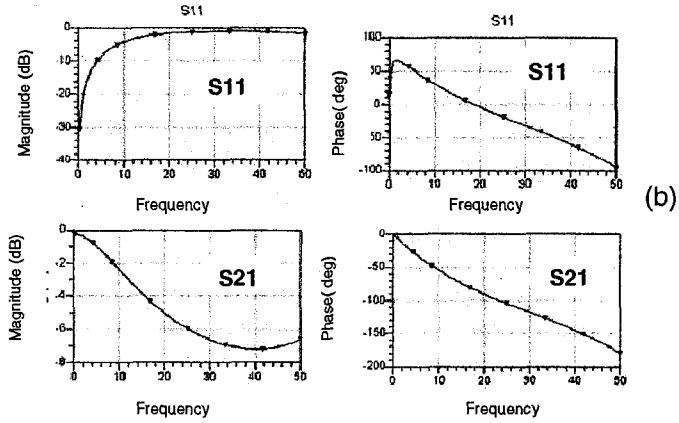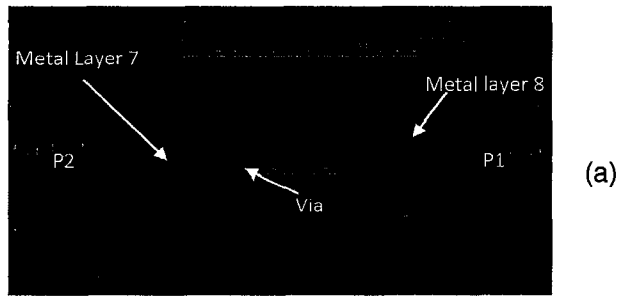
Figure 21: Rectangular Spiral Inductor (n=3.5; Width =10μm; Spacing =0.5μm)
(a) ADS Layout (b) Simulated S-parameter
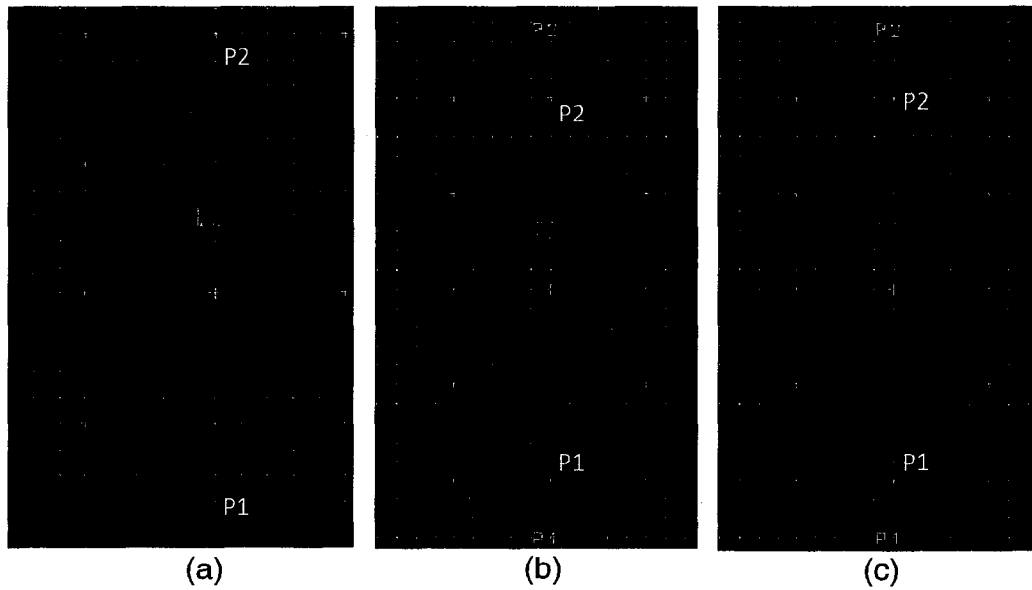
Figure 22: Octagonal Spiral Inductor ADS Layout (a) n=2.5; Width=10μm;
Spacing=0.5μm (b) n=3.5; Width=10μm; Spacing=0.5μm (c) n=3.5;
Width=20μm; Spacing=0.5μm
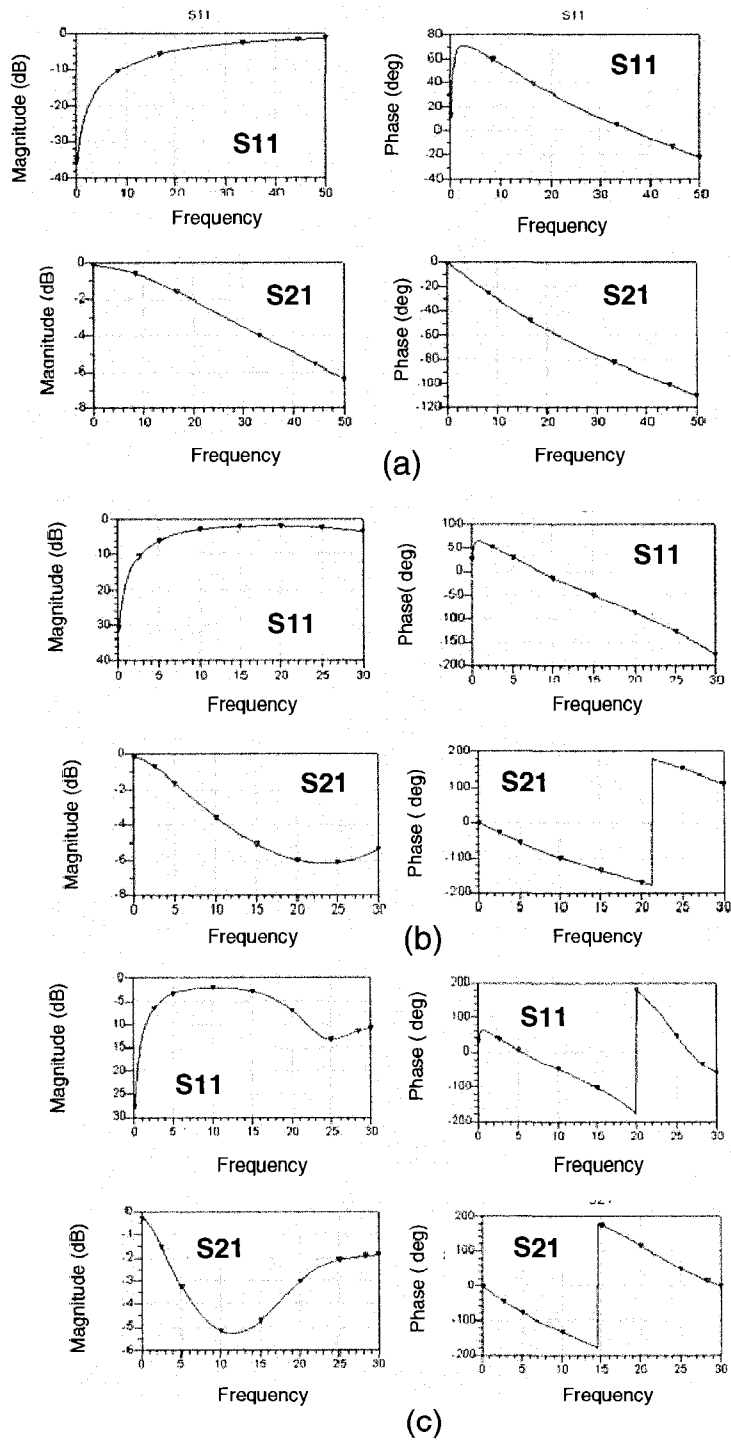
Figure 23: Octagonal Spiral Inductor S-parameter (a) n=2.5; Width=10μm; Spacing=0.5μm (b)n=3.5;Width=10μm;Spacing =0.5μm (c)n=3.5;Width = 20μm;Spacing=0.5μm

3.2.2 Inductor Lumped Model

The inductor lumped model is shown in Figure 24. Referring to Figure 24, the inductance of the spiral and underpass is represented by the series inductor (Ls) between port 1 and port 2, which takes into account the skin depth of a conductor with finite thickness. The conductor loss in metal trace is characterized by resistor (Rs), which is in series with the inductor. This resistance is frequency dependent due to the skin effect and the current crowding. Current crowding is the change in current density resulting from the magnetic field that allows direct capacitive coupling between the two terminals of the inductor. This capacitance between the top metal and the metal underpass to connect the inner end of the spiral inductor to the port is represented by Cp. The silicon substrate is modeled by Csub and Rsub. Csub and Rsub are proportional to the area covered by the spiral. The capacitance due to the substrate gives resonance frequency above which the inductor can no longer be used as an inductor thus parasitic capacitance to the substrate makes the inductor to self-resonate at a certain frequency. Oxide capacitances are added to the lumped model to represent the RF signal flow through the silicon substrate. Cox represents the parasitic capacitance between the spiral and the substrate.
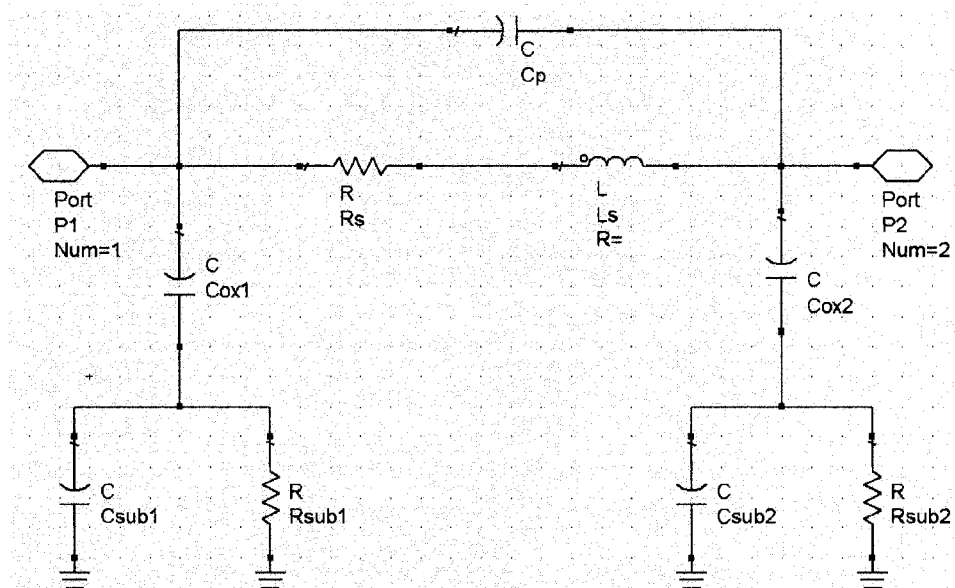
Figure 24: Two-port Lumped Model for Inductor Test Structure

The lumped circuit modeling of any passive component breaks down at higher frequencies. The model is accurate up to the self-resonance frequency of the individual ports, which is the useful range for inductor applications. The close match between measured and modeled S-parameter over a wide range of inductance and quality factor confirms the accuracy and robustness of the model. The S-parameter obtained from layout simulations show a very good agreement with those obtained from the lumped model, as shown in Figure 25.

Performance of the test structures are analyzed using inductance, quality factor, and resistance. Expressions used to measure these parameters are based on S-parameters. The extracted values of lumped models for rectangular and octagonal structures are given in Tables 4-5.
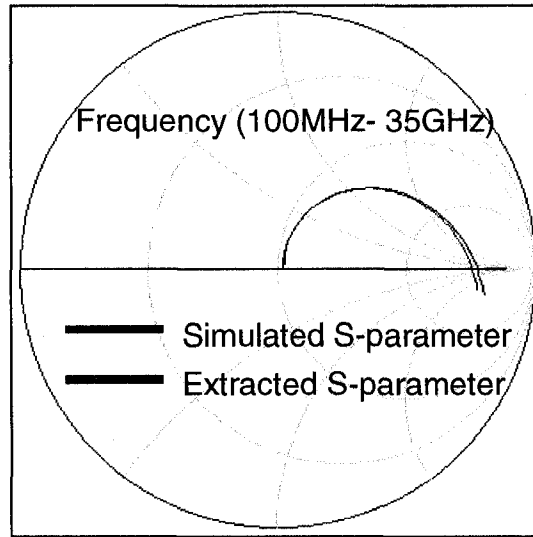
Figure 25: Comparison of Simulated S-parameter and Lumped Model Extracted S-parameter for Inductor Test Structure

Table 4: Lumped Model Parameters for Rectangular Inductor Test Structure

Parameter	Units	w:10μm s:0.5μm n: 2.5	w:10μm s:1μm n: 2.5	w:20μm s:0.5μm n: 2.5	w:20μm s:1μm n: 2.5
Fsr	Hz	3.23E+10	3.13E+10	1.26 E+10	1.25 E+10
Din	μm	50	50	100	100
Dout	μm	112	114	222	224
Cp	F	9.1E-22	6.14 E-25	3.75 E-21	9.88 E-22
Cox1	F	3.39 E-14	3.67 E-14	1.23 E-13	1.25 E-13
Cox2	F	1.96 E-12	6.35 E-11	1.12 E-13	1.49 E-13
Csub1	F	3.81 E-13	4.47 E-13	1.76 E-12	1.71 E-12
Csub2	F	3.46 E-14	3.33 E-14	6.47 E-11	4.78 E-13
Rs	Ω	2.84	2.75	2.64	2.56
Rsub1	Ω	13.36	11.34	10	10
Rsub2	Ω	4997	4999	4787	4974
L	H	7.71 E-10	7.68 E-10	1.4 E-09	1.39 E-09

Table 5: Lumped Model Parameters for Octagonal Inductor Test Structure

Parameter	Units	w:10μm s:0.5μm n: 2.5	w:10μm s:1μm n: 2.5	w:20μm s:0.5μm n: 2.5	w:20μm s:1μm n: 2.5
Fsr	Hz	3.68 E+10	3.7 E+10	1.47 E+10	1.47 E+10
Din	μm	50	50	100	100
Dout	μm	101.45	103	210.42	202.92
Cp	F	3.63 E-24	5.09 E-23	3.92 E-21	5.37 E-22
Cox1	F	2.9 E-14	2.96 E-14	7.31 E-13	1.02 E-13
Cox2	F	5.3 E-14	4.8 E-14	2.1 E-13	1.34 E-13
Csub1	F	4.0 E-13	3.9 E-13	1.1 E-13	1.3 E-13
Csub2	F	5.61 E-14	6.17 E-14	1.88 E-13	3.1 E-13
Rs	Ω	2.68	2.58	1.81	2.39
Rsub1	Ω	11.86	12.76	16.4	10
Rsub2	Ω	4458	4840	4872	4997
L	H	6.89 E-10	6.8 E-10	1.22 E-09	1.03-09

- Inductance (L)

  Higher number of turns or trace length leads to higher inductance value [21]. At low frequencies, the shunt parasitic has little effect and consequently the inductance increase with frequency. The measured inductance stays relatively constant up to a frequency and then it starts to rise as the device heads towards a self-resonant state caused by the parasitic capacitance.

- Quality Factor (Q)

  The quality factor dependency on frequency is caused by the influence of the parasitic resistance and capacitance. At low frequency, quality factor is determined by the series resistance of inductor turns while at higher

frequency skin effect reduces the effective area for the current flow and thus increase the heat dissipation losses.

- Self-Resonant Frequency (Fsr)

Above self-resonant frequency, the inductance value and quality factor becomes negative. This indicates that above Fsr, the capacitive effects dominate the behavior of the inductor. More number of turns increases the net inductor area that results in high inductance value and proportionally higher series resistance thereby reducing the inductor self-resonant frequency [22].

3.2.3 Inductor Parameter/ Result Analysis

In this section, designed inductors are analyzed. Using the simulation based methodology, parameter changes can be made to the spiral design. This section examines the effect of changing some of the basic spiral parameters (length, width, spacing, and number of turns) on the frequency dependent inductance and quality factor. Inductance value of 0.14-0.7nH and quality factor of 8-16 is achieved with rectangular inductor structures designed for this thesis. Also, inductance value of 0.68-3.8nH and quality factor of 9.5-18 is achieved with octagonal inductor structures.

3.2.3.1 Metal Width

The width of the metal trace affects the performance of the inductor to very large extent, as shown in Figures 26-27. The quality factor decreases with increasing metal width because of the skin effect in the metal layer that leads to current crowding to the edges of the conductor. The lower self-resonant frequency due to larger metal width occurs because of larger capacitive coupling of the spiral metallization to the substrate. Therefore, the metal width should be as wide as possible so as to achieve a low series resistance. Larger width implies larger area inductor and hence larger parasitic capacitance, skin effect, and substrate loss. The width of the coil conductor should only be large enough to reduce the ohmic loss in the inductor structure [23].
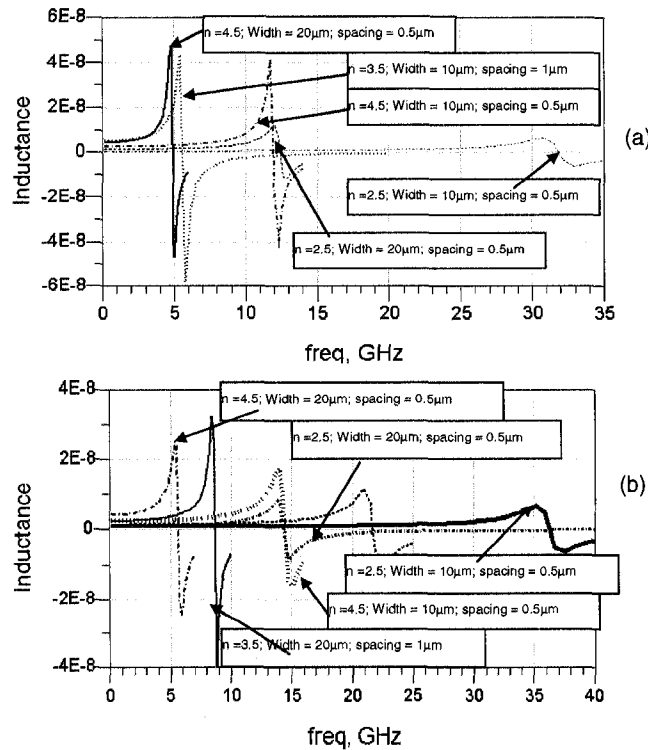
Figure 26: Inductance of Inductor Test Structure (a) Rectangular (b) Octagonal
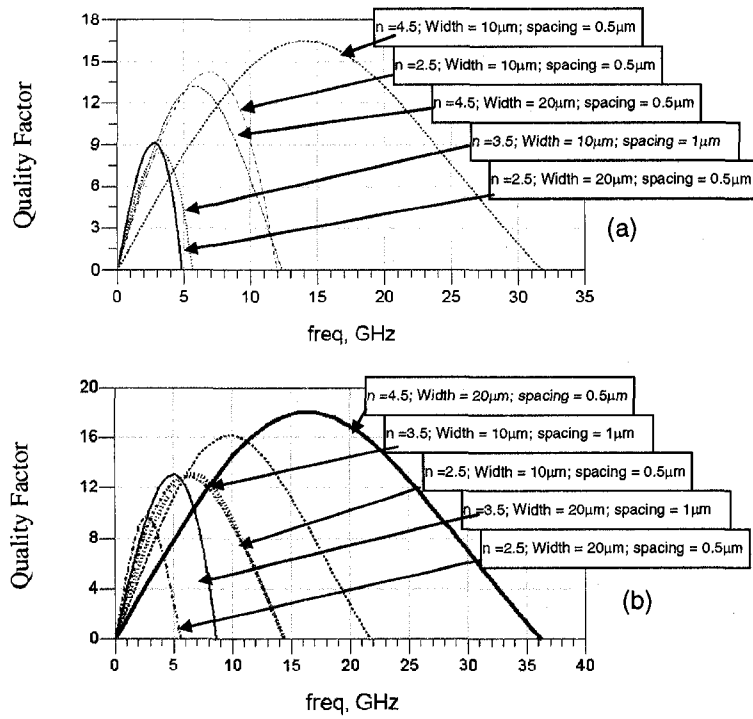
Figure 27: Quality Factor of Inductor Test Structure (a) Rectangular (b) Octagonal

3.2.3.2 Spacing

Increased spacing between the metal traces leads to lower inductance due to decreased magnetic coupling between the segments and increased spiral resistance. Smaller spacing results in smaller inductor area that leads to higher quality factor, shown in Figure 28. Spacing between the metal lines should be kept minimum, which depends upon the technology.
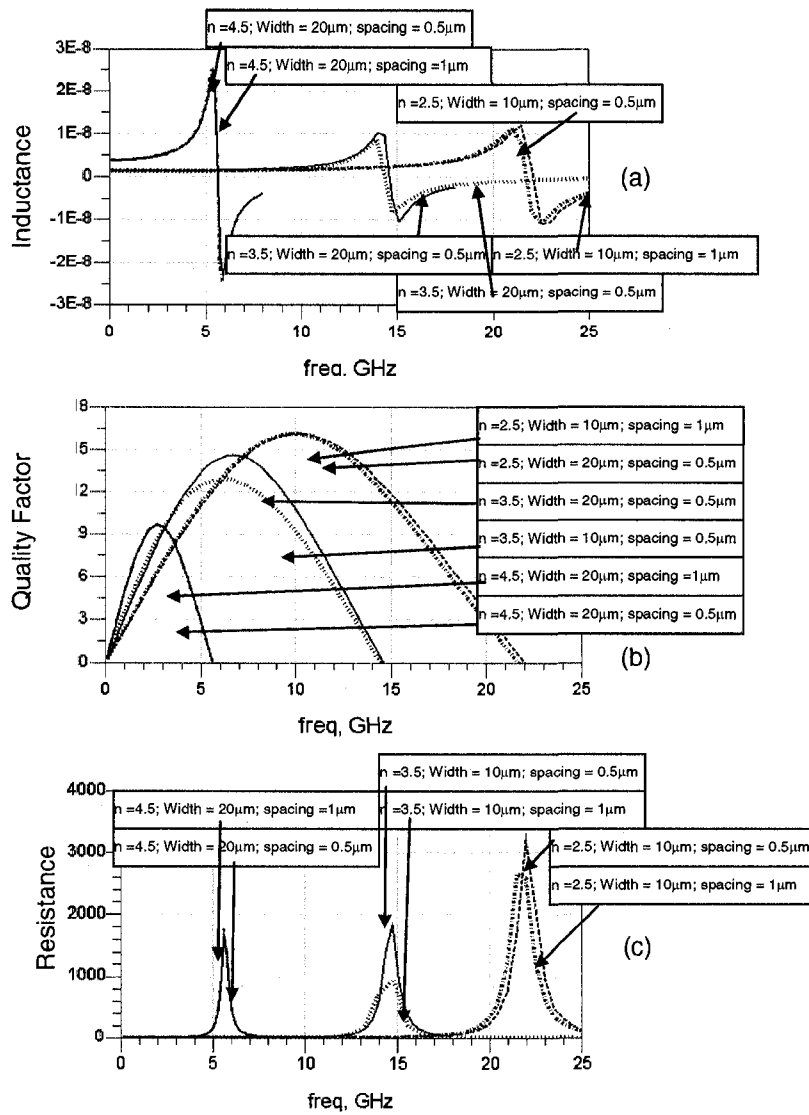
Figure 28: Octagonal Inductor Test Structure (a) Inductance (b) Quality Factor (c) Resistance

3.2.3.3 Inner and Outer Core Diameter

At high frequencies, inner core of the spiral inductor has higher resistance than the outer turns because of eddy currents. Quality factor and inductance decreases with lower inner core diameter. Therefore, the spiral center should be kept hollow. The outer diameter increases the area occupied, which leads to

increased parasitic inductance between the metal and substrate. This also reduces

the self-resonant frequency of the inductor.

3.2.3.4 Number of Turns

The inductance value increases when the spiral has more turns. The self-

resonance frequency decreases significantly for each new turn added because of

the increased capacitive coupling between the turn and the substrate. The

maximum quality factor also decreases incredibly with increasing turns due to the

increased surface area and proportional increase in parasitic of the inductor.

3.2.3.5 Inductor Geometry

This parameter depends upon the technology specifications. Table 6

compares the maximum quality factor achieved with rectangular and octagonal

geometries. The octagonal spiral achieves the best quality factor. This

improvement comes at the expense of a slightly more complicated layout

procedure.

Table 6: Quality Factor Comparison Based on Inductor Geometry

Number of Turns	Width	Spacing	Maximum Q	
			Rectangular	Octagonal
2.5	10 μm	0.5 μm	16.0	17.8
2.5	20 μm	1.0 μm	14.3	15.4
3.5	10 μm	0.5 μm	12.7	14.9
3.5	20 μm	1.0 μm	10.1	11.8
4.5	10 μm	0.5 μm	11.0	12.5
4.5	20 μm	1.0 μm	8.6	9.7

3.3 On-Chip Capacitor

Capacitors are one of the crucial elements in integrated circuits and are used extensively in many integrated circuit applications. In many of these applications, capacitors consume a large fraction of the chip area. Therefore, capacitors with higher capacitance density are very desirable.

In RF applications, it is essential for the capacitors to have self-resonance frequencies well in excess of the frequency of interest and high quality factor. Nonlinear capacitors (gate capacitors and junction capacitors) with high capacitance density have been used in many applications so as to improve the area efficiency and require a dc bias voltage to operate. Metal-to-metal and metal-to-poly capacitors are linear and have small temperature variations [24]. However, they suffer from a low capacitance density that determines the capacitance [25].

Passive device capacitors are constructed from two layers of metal (aluminum or copper and polysilicon layer). The conductivity of metal layers plays an important part in determining the quality factor of capacitor, especially at lower frequencies. A capacitor is constructed by placing two metal conductors in close proximity. Parallel plate capacitor, shown in Figure 29, consumes a large fraction of die area. Parallel plate capacitor structures designed for the thesis are analyzed for various component properties such as capacitance, parasitic capacitances, and quality factor as a function of frequency [26].
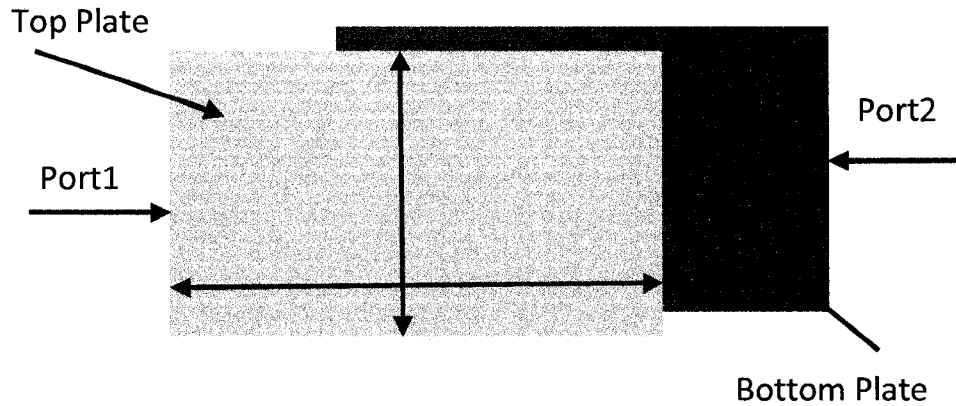
Figure 29: Parallel Plate Capacitor

3.3.1 Test Structure Design of Capacitor

Several physical parameters are available when designing on-chip capacitors, like plate length, plate width, number of plates, and distance from the ground. More the number of substrate layers between lower ground and the capacitor plate, lower the port parasitic capacitance. But this increases RF module height and cost. Therefore, for designing test structures the top two metal layers are used. For the thesis, capacitor test structures are designed for 0.1pF, 1pF, and 10pF capacitance value, using 0.13μm RF CMOS technology. Metal layer 8 and metal layer 7 are used as top and bottom plates of the capacitor. The layout of the capacitor test structure is shown in Figure 30 along with the simulated S-parameter.
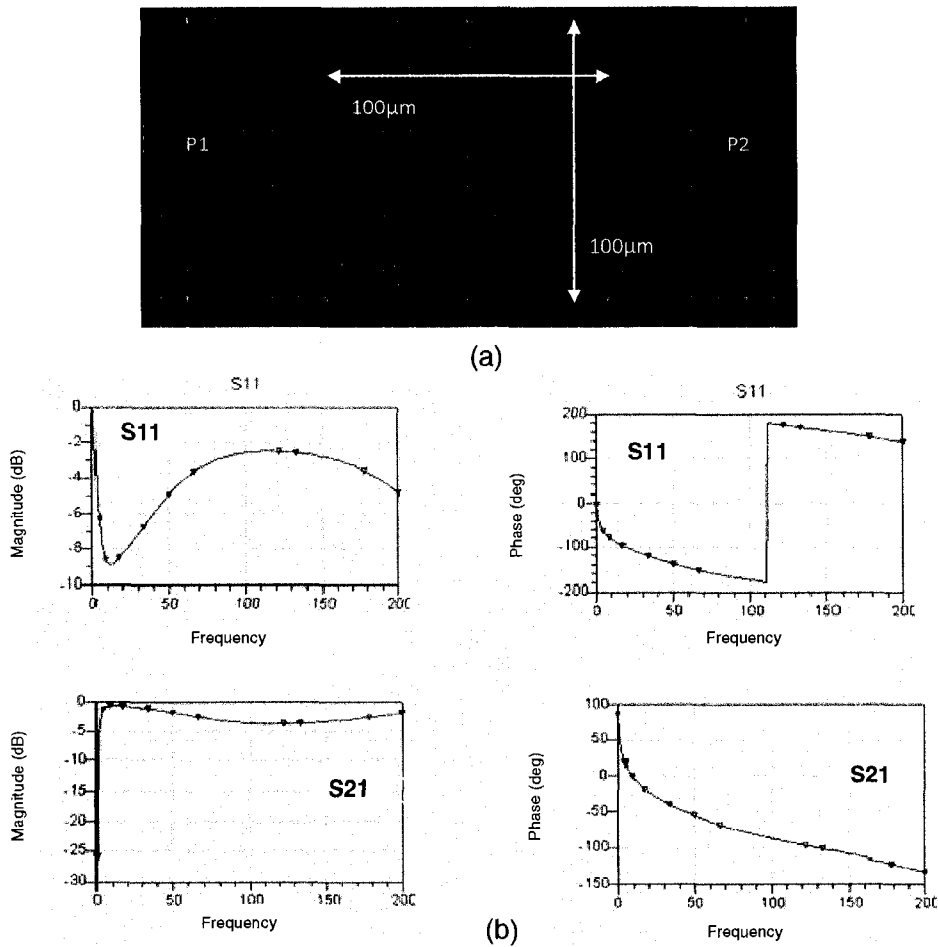
Figure 30: Capacitor Test Structure Capacitance (a) Layout (b) S-parameter

3.3.2 Capacitor Lumped Model

Equivalent circuits provide an interface between EM simulation and circuit simulation. Two-port lumped model shown in Figure 31 represents the performance of passive capacitor [27]. Cp represents the primary series capacitor that depends on plate size and number of plates. Series resistor (Rs) and inductor (Ls) represent the parasitic from the metal plates and dielectric losses. Since the metal layers are not infinitely conductive, energy is lost to heat in the volume of

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the conductors. This loss is represented by a resistor placed in series with the capacitor. Csub and Rsub are added to regenerate the parasitic effects between the bottom metal plate and silicon substrate. Shunt capacitor Cox is the parasitic between the top metal plate and silicon substrate.
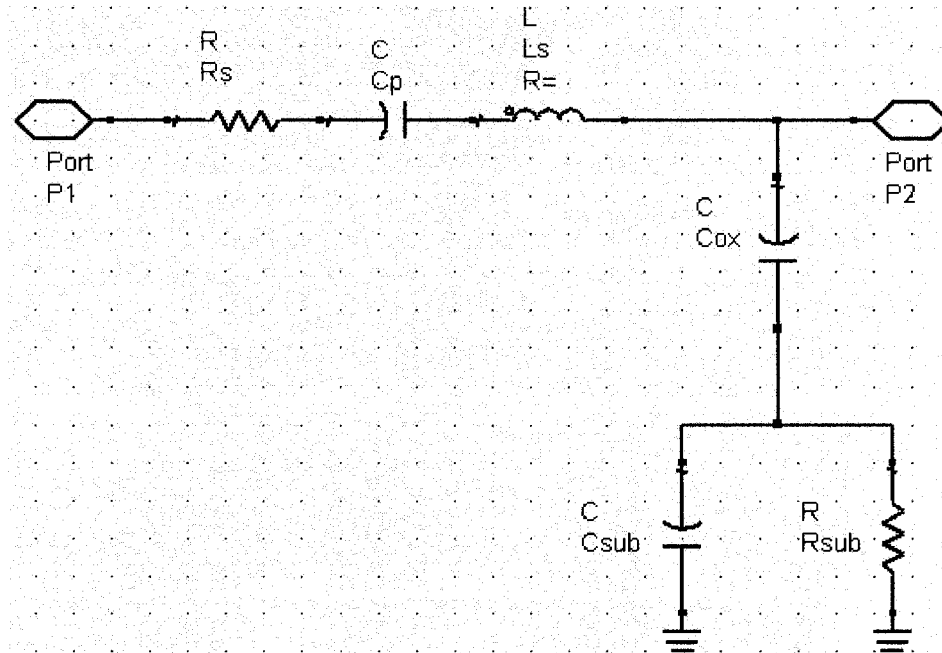
Figure 31: Two-port Lumped Model for Capacitor Test Structure

The value of all lumped elements can be extracted from the Y-parameters, which are converted from the measured S-parameter through iterative simulations to reduce the mismatch error. To obtain the simulated parameters, the initial values of all the lumped elements are chosen. The performance of the simulated S-parameter is compared with equivalent lumped circuit extracted S-parameter. Capacitance, quality factor, and resistance of the capacitor test structures are obtained by:

$$Q = \frac{\text{imag} [Y_{in}]}{\text{real} [Y_{in}]} \qquad (3.4)$$

$$C = \frac{\text{imag} [Y_{in}]}{2\pi f} \qquad (3.5)$$

$$R = \text{real} [Y_{in}] \qquad (3.6)$$

Table 7: Lumped Model Parameters for Capacitor Test Structure

Parameter	Units	w:150μm l:150μm	w:100μm l:100μm	w:44μm l:44μm
Fsr	Hz	1.3 E+11	1.88 E+11	6.27 E+11
Rs	Ω	0.67	0.88	1.41
Ls	nH	0.023	0.020	0.007
C	pF	1.00	0.51	0.10
Cox	pF	0.218	0.065	0.014
Csub	pF	0.267	0.291	0.142
Rsub	Ω	1114	1206	1467

3.3.3 Capacitor Parameter/Result Analysis

Capacitor test structure designed with top two metal layers result in different physical dimensions as given in Table 8.

Table 8: Physical Dimension of Capacitor Test Structure

Capacitance	Width	Length	Resonant Frequency
0.1pF	150 μm	150 μm	1.1E+11 Hz
0.5pF	100 μm	100 μm	1.88E+11 Hz
1pF	44 μm	44 μm	6.27E+11 Hz

For a given capacitor value, smaller physical dimensions result in a smaller series resistance and series inductance. Also, a higher self-resonance frequency and higher quality factor is obtained. An increase in capacitance value decreases both quality factor and resonant frequency as shown in Figure 32.
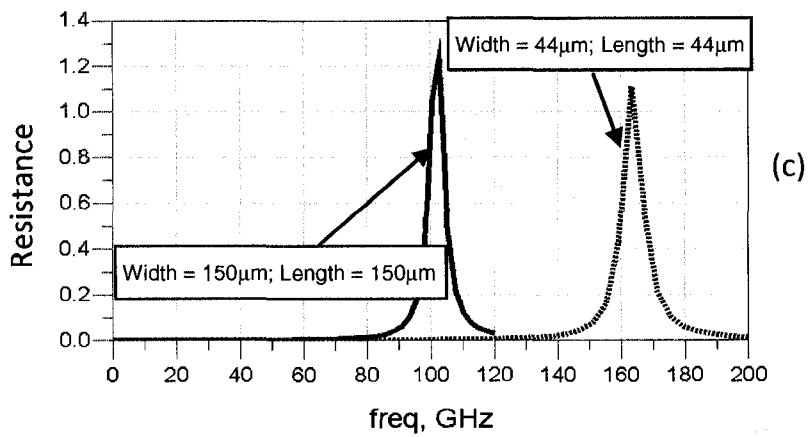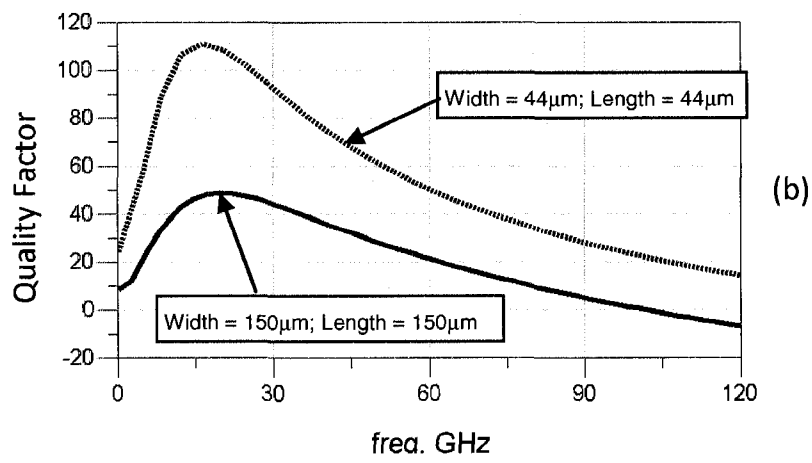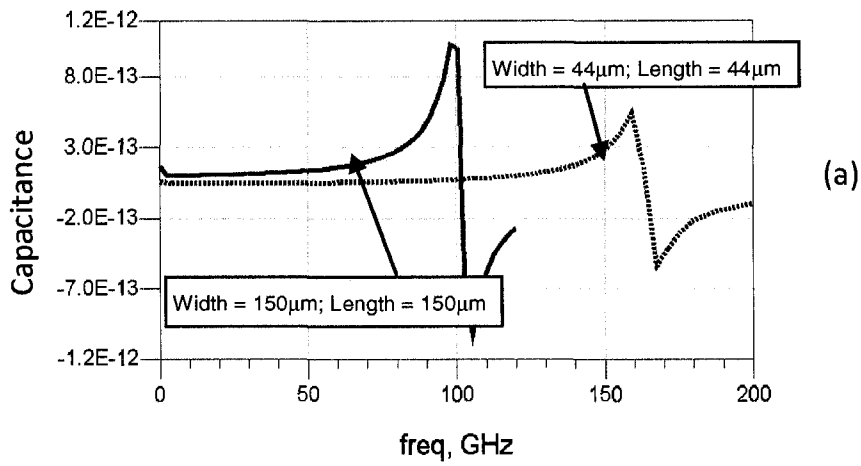
Figure 32: Capacitor Test Structure (a) Capacitance (b) Quality Factor (c) Resistance

3.4 On-Chip Transformer

Transformers have been used in radio frequency circuits since the early days of telegraphy. The transformers are important elements in many different applications such as power combining, signal coupling, bandwidth enhancement, and common-mode rejection.

The operation of a passive transformer is based upon the mutual inductance between two or more conductors [28]. The transformer is designed to couple alternating current from one conductor to the other. The current and voltage transformation between windings in an ideal transformer are related to the turn ratio (η), as given by:

$$\eta = \frac{v_s}{v_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}} \tag{3.7}$$

On-chip transformer design is very similar to on-chip inductor. A planar transformer can be constructed from interwound metal conductors in the same plane or overlaid metal. The various transformer configurations are possible and can be configured as two or four port terminal devices.

3.4.1 Test Structure Design of Transformer

The transformer test structures are designed using ADS Momentum. The key geometrical parameters are number of primary and secondary turns (η) =2.5, spacing between the traces (s) =0.5μm and 1μm, width of metal traces (w) =10μm and 20μm, and configuration (rectangular or octagonal). The transformers

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designed for this thesis uses two metal layers connected in parallel through intermetal vias in between, as shown in Figures 33-34.
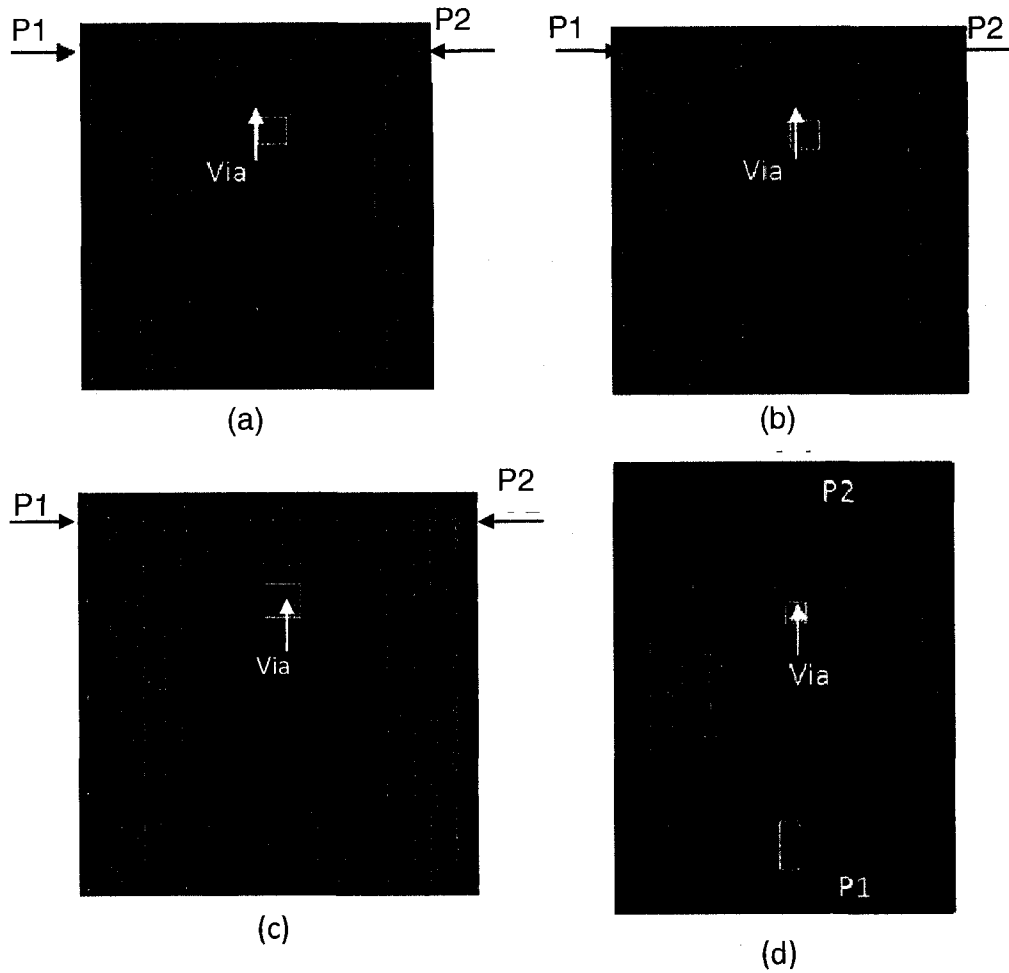
Figure 33: ADS Momentum Layout for Transformer Test Structures (a) Rectangular;Width=10μm; Spacing=0.5μm (b) Rectangular; Width=10μm; Spacing=1μm (c) Rectangular; Width=20μm; Spacing=0.5 μm (d) Octagonal; Width=10μm; Spacing=1μm
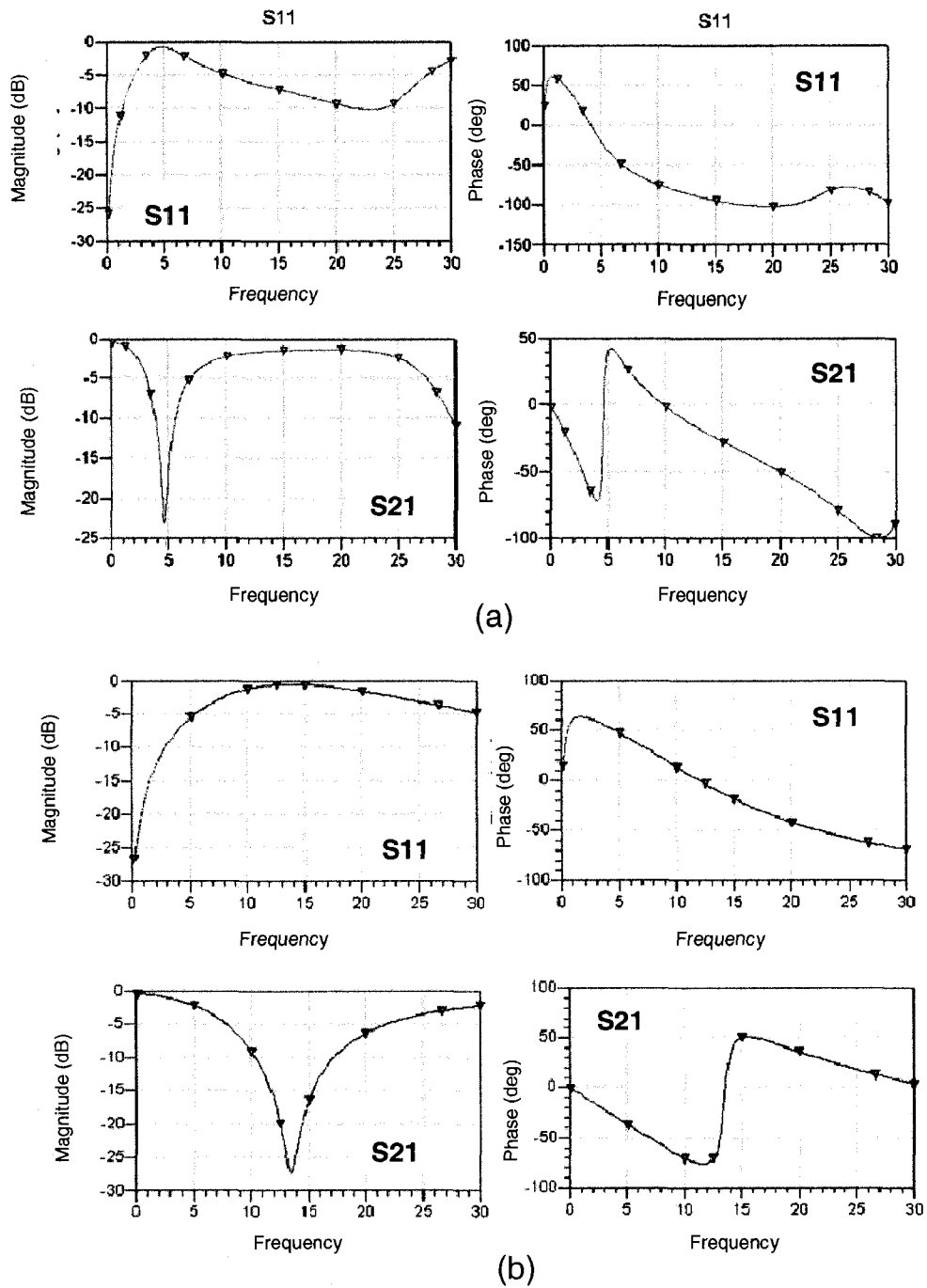
Figure 34: S-parameter for Transformer Test Structures (a) Rectangular; Width=10μm; Spacing=0.5 μm (b) Rectangular; Width=10μm; Spacing=1μm (c) Rectangular; Width=20μm; Spacing=0.5 μm (d) Octagonal; Width=10μm; Spacing=1μm

3.4.2 Transformer Lumped Model

Transformers are represented by a network of lumped elements as shown in Figure 35. The model of two-port transformer consists of inductors, capacitors, and resistors. The lumped model includes stray capacitances and inductances that give good characterization of the RF transformer. Referring to Figure 35, Lp and Ls represent the self-inductance of primary and secondary inductor. Lm is the mutual inductance between the primary and secondary inductors. Resistors Rp and Rs represent the resistive loss and the loss in the ferrite core. They represent the conductor resistance at low frequency. Rsub_p and Rsub_s give the substrate resistance at high frequencies. Cp and Cs are distributed elements between turns of each winding. Cox_m is the capacitance between the two ports. Csub_p and Csub_s represent capacitance between the device and the substrate. Cox_p and Cox_s show the capacitance due to oxide layer.
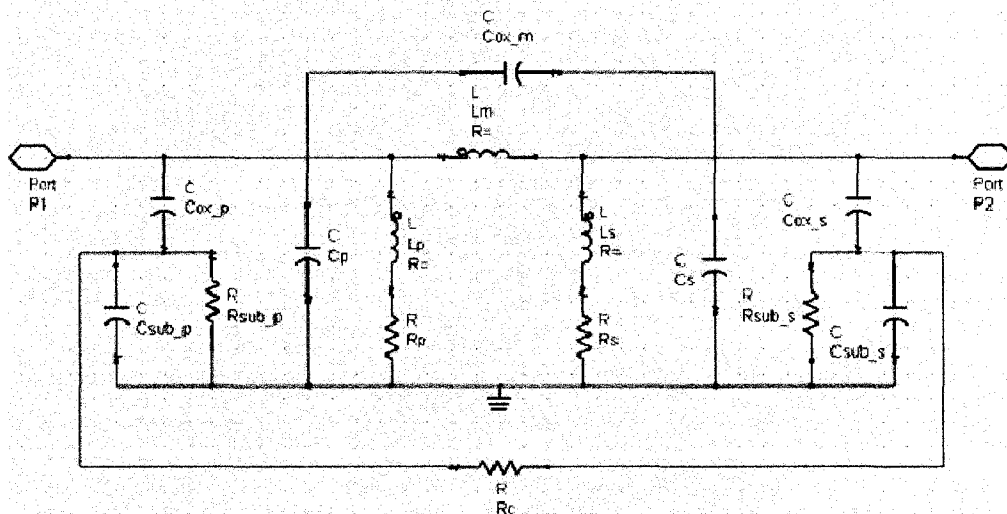
Figure 35: Two-port Lumped Model for Transformer

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S-parameter contains sufficient information to characterize each individual component of the circuit presented in two-port lumped model of the transformer. Method to obtain the model parameters is parameter extraction technique. The fit frequency range is appropriate before the self-resonant frequency. The extracted values for transformer lumped model parameters are given in Table 9.

3.4.3 Transformer Parameter/Result Analysis

Inductance, quality factor, and coupling coefficient as function of frequency, are used to evaluate the performance of the transformer. The width and thickness of the metal layer limit the transformer quality factor because energy is dissipated by finite resistivity of metal layer as well as in the conductive silicon substrate. Increasing the thickness of the metal trace improves quality factor. The quality factor initially rises with frequency as the reactive component of the impedance increases and then decreases due to increasing energy dissipation at higher frequency.

The transformers with more numbers of turns and higher inner diameter have lower self-resonant frequency and higher magnetic coupling coefficient because of the longer metal length and the larger total area. Although the larger transformers have higher inductance, they may also suffer from the lower quality factor due to the larger capacitance to the substrate (Csub/Cox) and the higher series resistance in the metal conductor. Inductance and resistance plots for transformer structure are presented in Figure 36.

Table 9: Lumped Model Parameters for Transformer Test Structure

Parameter	Units	w:10μm s:0.5μm	w:10μm s:1μm	w:20μm s:0.5μm	w:10μm s:1μm
Geometry		Rectangle	Rectangle	Rectangle	Octagonal
Turns		2.5	2.5	2.5	2.5
Fsr	GHz	12.1	11.9	4.0	14.2
Lp	nH	5.1	18.1	5.7	18
Ls	nH	19.9	10.5	19.9	10.4
Lm	nH	1.9	1.8	3.2	1.8
Rp	Ω	7911	4999	4932	4499
Rs	Ω	5479	2579	4999	2579
Cp	pF	0.4	0.7	27.5	970
Cs	pF	0.57	0.3	31.3	970
Cox_p	pF	0.12	0.18	0.6	0.05
Cox_s	pF	0.25	0.19	1.84	0.05
Cox_m	pF	2.34	4.9	0.85	4.6
Csi_p	pF	0.03	0.15	0.08	9.6
Csi_s	pF	0.04	0.001	0.15	996
Rsi_p	Ω	4998	4999	5000	5000
Rsi_s	Ω	4995	4999	5000	4916
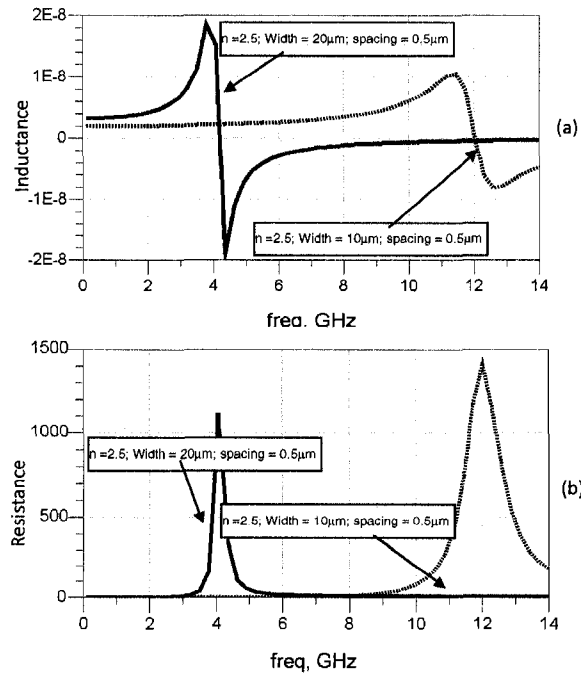
Figure 36: Transformer Test Structure (a) Inductance (b) Resistance

3.5 Summary

In this chapter of the thesis, passive structures in ADS Momentum were designed and simulated. Lumped models were presented for each passive device and iterative technique was used to reach the optimum performance.

In the following chapter the finalized design and optimized passive structures are layout using Cadence 0.13μm CMOS technology and low noise amplifier (LNA) is simulated utilizing inductor test structures.

Chapter 4

LNA Design

This chapter presents the Cadence layout of passive test structures designed and analyzed in the earlier chapter. Section 4.1 provides the procedure for converting the ADS Momentum layout to Cadence layout. Probing pads are used in Cadence layout designs. Next section is devoted to the de-embedding procedure for probing pads. Finally, low noise amplifier (LNA) schematic design and simulation results are discussed.

4.1 Test Structure Layout in Cadence

Successful design of RFIC passive structures on silicon substrate needs various precise parameters like device dimensions, layout, and on-wafer small signal measurement. Ground-Signal-Ground (G-S-G) probes are used to measure the on-wafer test structures, therefore probing pads need to be introduced in layout for fabrication. G-S-G probe consists of probe contact between two ground probes and connects the device under test to the test instrument like network analyzer. Probing pads are used to ensure that the substrate is effectively grounded. Dimensions for the G-S-G configuration used for the thesis are as in Figure 37.
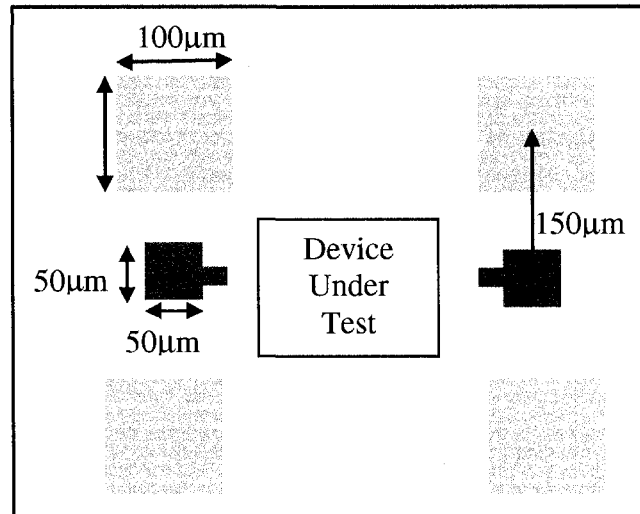
Figure 37: Dimensions for Ground-Signal-Ground Probing Pads

Test structure designs in ADS Momentum, as presented in Chapter 3, are layout for fabrication purpose in Cadence. Design rules followed for the layout are 0.13μm CMOS technology. Final layouts for the inductor and transformer contain G-S-G probing pads. Unfortunately, due to lack of resources these layouts were not fabricated.

Inductor test structure layout in Cadence uses metal layer 8 for the spiral and metal layer 7 as an underpass, as shown in Figure 38. Signal pads are connected to the end of the metals for on-wafer testing purpose. Intermetal vias are used to connect two metal layers and a lower metal layer is utilized for connecting the ground pads to the intermetal vias to ensure accurate substrate grounding.
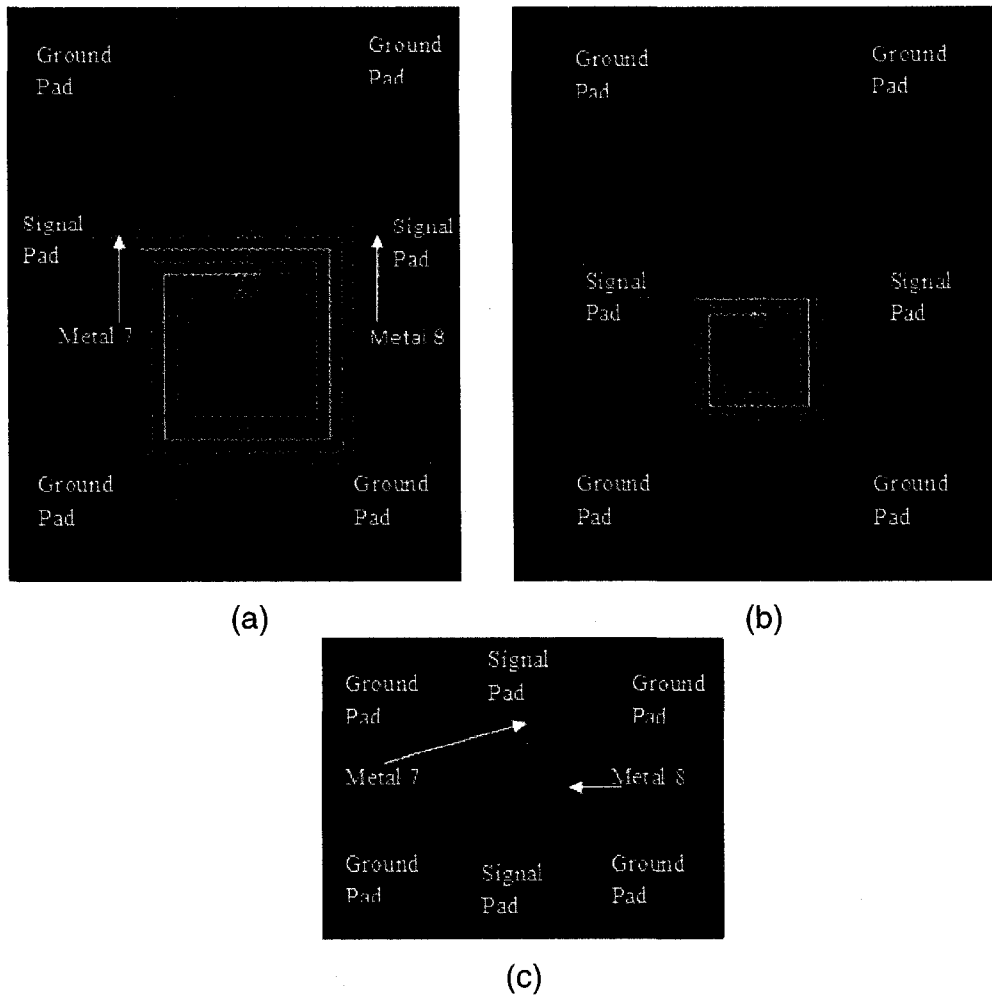
Figure 38: Cadence Layout (a) Rectangular Transformer n=2.5 (b) Rectangular Transformer n=3.5 (c) Octagonal Transformer n=3.5

4.2 De-embedding G-S-G Probing Pads

As the design process technology shrinks, the contact pads and transmission line widths also scaled down. The series resistance and inductances due to the contact pads cannot be ignored.

Test structures layout in Cadence shown in Section 4.1 includes the probing pads for measurement purpose. Figure 39 shows the on-wafer

measurement setup of two-port passive device. A network analyzer and a probing

station are required during the measurements.
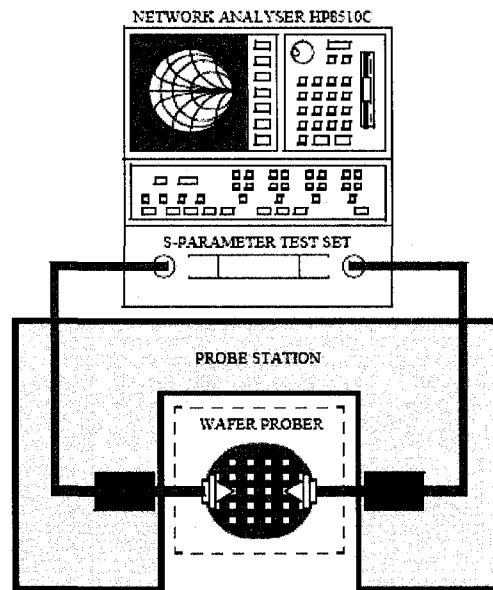
Figure 39: On-Wafer Measurement Setup with Network Analyzer and Ground-
Signal-Ground Probe Station

The measured data collected using network analyzer in the form of S-

parameter relates the electromagnetic waves scattered from the device under test

to those waves incident upon the network. Because the performance of passive

devices is very sensitive to the dimensions, the probe pads need to be de-

embedded very accurately. Most frequently adopted de-embedding procedure is

based on S-parameter measurements of reference standards (shorts, opens, and

thru). The de-embedding procedure consists of converting the S-parameter

measurement of standards to Y-parameter and Z-parameter. Then subtracting the

Y-parameters of the on-wafer open standard and de-embedding the Z-parameter

of short and thru standard from the test structure measurement. On-wafer

standard can be layout as shown in Figure 40.

OPEN   THRU

SHORT   SHORT
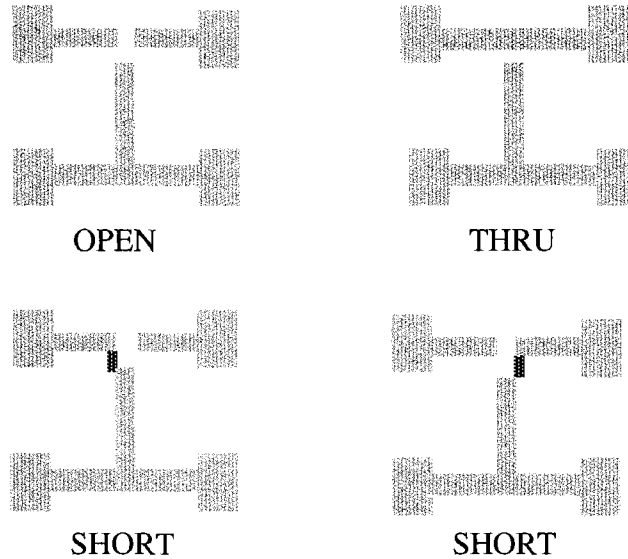
Figure 40: Layout of On-Wafer Standards

4.3 Application Circuit LNA

4.3.1 LNA Schematic

The design specifications for low noise amplifier designed for the thesis

are not very demanding (compared to the industry) due to the reason that this

design application was to implement the passive component test structures. The

inductor test structure designed and characterized in earlier chapters is utilized in

LNA schematic. The amplifier performed reasonably well for the required

frequency band (2.4GHz-2.5GHz) on the tests of gain, return loss, stability, and

noise figure. The low noise amplifier is the first stage of receiver, which is

responsible for providing reasonable power gain and linearity, while not

degrading the signal-to-noise ratio [29].

A complete schematic of single-ended 2.4GHz LNA using 0.13μm

technology in Cadence is shown in Figure 41. Transistor M0 forms a current

mirror with M1, where its width is a small fraction of the width of transistor M1

in order to minimize the power overhead of the bias circuit. Amplifier design

uses cascoding transistor M2, which provides a good isolation between the input

and the output stages. The inductors Lc and Lg are used to provide the desired

input resistance. The output impedance matching is obtained by tuning the

inductor L1. The inductor structures used in the schematic are based upon

lumped model developed earlier during the thesis. Both input and output are

matched to 50 ohms [30].
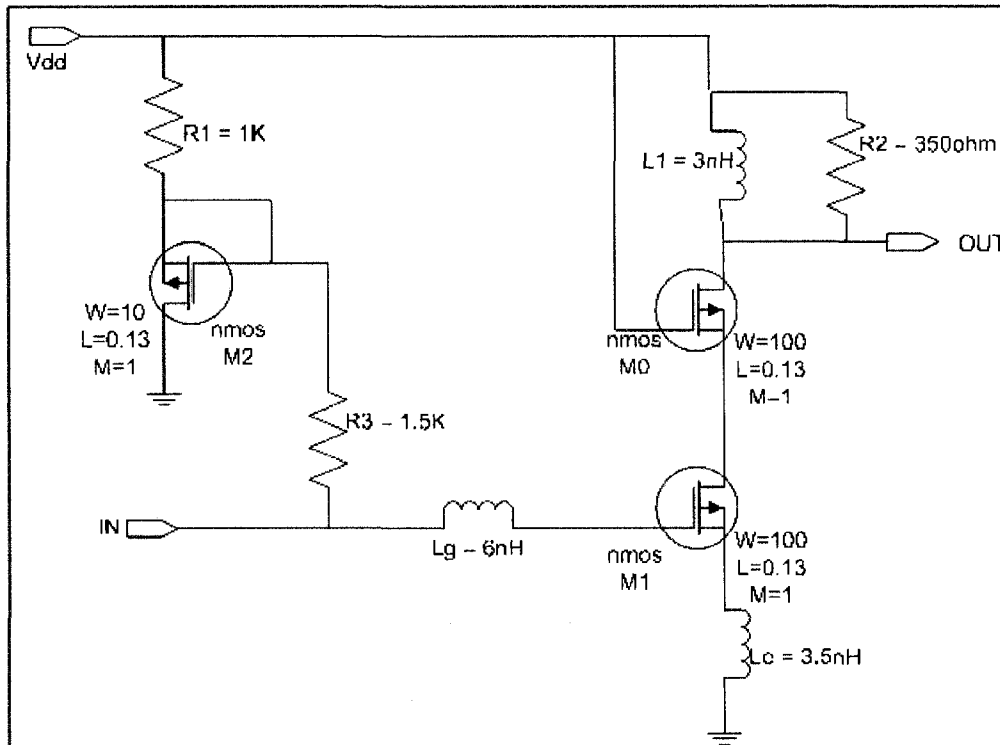
Figure 41: Schematic of Single-Ended LNA

4.3.2 LNA Figure of Merit

- Gain

  Transducer power gain, GT, is defined as the ratio between the power delivered to the load and the power available from the source. Operating power gain, GP, is defined as the ratio between the power delivered to the load and the power input to the network. Available power gain, GA, is defined as the ratio between the power available from the network and the power available from the source.

- Noise

  According to the cascaded stages, the overall noise figure is mainly determined by the first amplification stage, provided that it has sufficient gain. LNA noise performance depends upon the low noise transistor, DC biasing point, and noise-matching at the input.

- Stability

  The Stern stability factor (K) characterizes circuit stability. When K>1, the circuit is unconditionally stable. That is, the circle does not oscillate with any combination of source and load impedances. The stability for the LNA designed over a wide frequency range (1GHz-10GHz) shows that K remains greater than one at all frequencies. Stability can also be defined in terms of auxiliary stability factor (Bf).

4.3.3 Simulation Results

The simulations for the LNA schematic are shown in this section. For generating these simulation results, lumped models of the equivalent value inductor test structure were utilized. With a supply of 3.3V at 2.45GHz, input return loss is 5dB, output return loss is 4dB, gain is 14dB, and noise figure is 2.2dB. The calculated stability factor (K = 2.8) indicates unconditional stable circuit. Figure 42 shows the simulated gain performance in terms of magnitude (Mag) for the LNA. The stability curves are plotted with respect to frequency sweep in Figure 43.
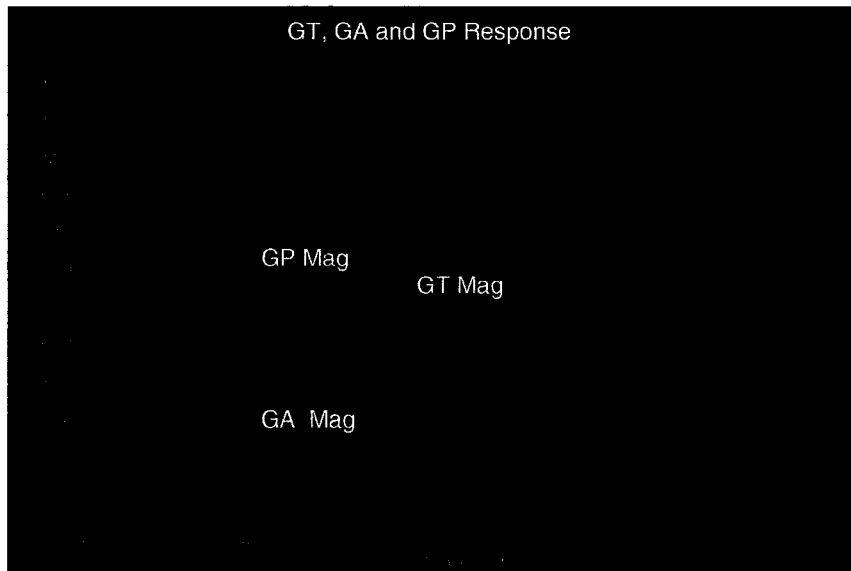
Figure 42 : Gain Measurements of LNA
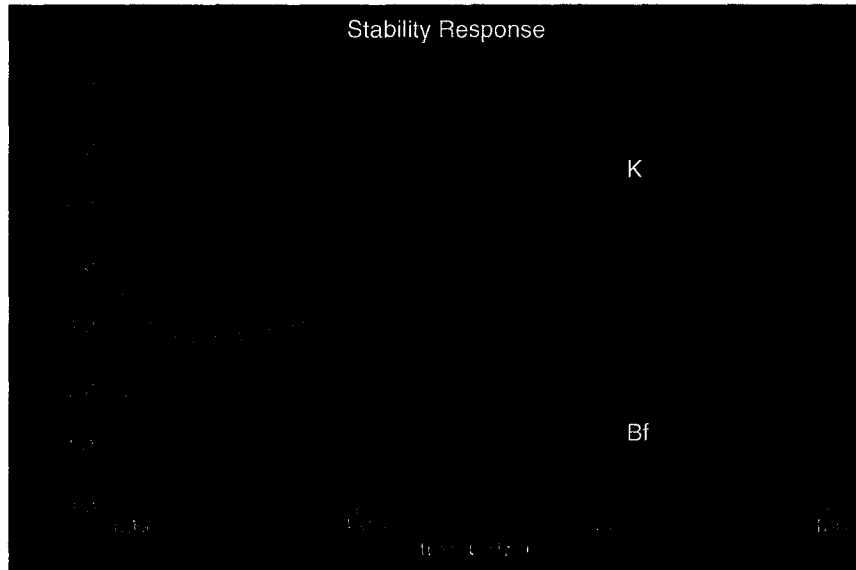
Figure 43: Stability Factor of LNA

Small signal noise can be obtained using Spectre when the input power

level is low and the circuits are considered linear. Noise figure results for the

LNA schematic are shown in Figure 44. Noise analysis provides the noise figure

(NF) and the minimum noise figure (NFmin).
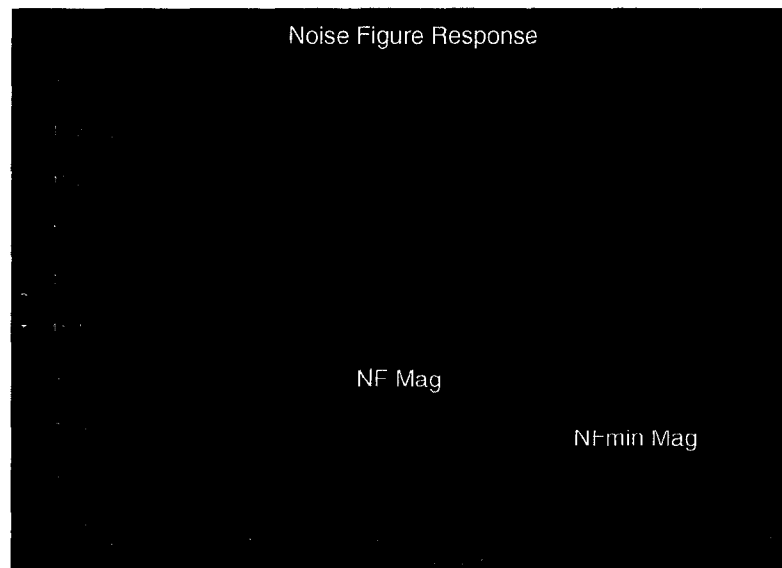
Figure 44: Noise Figure and Minimum Noise Figure for LNA

4.4 Summary

In this chapter, Cadence layout for passive device test structure was developed and Ground-Signal-Ground probing pads for measurement were purposed. The general procedure for de-embedding the probing pads was presented. Finally, low noise amplifier is designed using Cadence Spectre. Although unable to get these layout fabricated during the course of this thesis, in the future one can use these layout files for fabrication and measure on-wafer parameters.

Chapter 5

Conclusion

This thesis examines passive components (interconnect, capacitor, inductor, and transformer) design on silicon substrate and modeling these passive component test structures using $0.13\mu m$ CMOS technology. This chapter summarizes the major contributions of the work done and identifies areas that merit future study.

5.1 Contributions

A substrate model was defined for the technology to be used in ADS Momentum simulator. Substrate definition includes number of layers, composition of each layer, and position of each layer. Layout and lumped element model for each passive structure was developed. Closed-form expressions based on S-parameters are applied to calculate component values of passive components. These expressions, which exhibit typical errors of 2-4% with respect to simulations of EM solver, are then incorporated into respective lumped circuit models. Final layout of the test structures for fabrication purpose is performed in Cadence using $0.13\mu m$ CMOS technology. Single-ended low noise amplifier was designed in Cadence Spectre as an application circuit.

5.2 Future Work

The test structures designed in the thesis could be fabricated. Test structures are layout in Cadence using G-S-G probe pads for on-bench measurements. If results match well, then the developed lumped model will be useful when doing simulations for complex circuits. Once the test structures are verified and matches well with their corresponding lumped model and ADS simulation results, these models can be used as pre-defined design library for complex system designs. On-wafer measurement can be done on the fabricated test structures and then probing pads can de-embed for accurate measurements. A network analyzer and G-S-G probing station are required during the measurements.

5.3 Summary

This thesis has contributed to a better understanding of on-chip interconnects, spiral inductors, capacitors, and transformers. The focus of this thesis has been the design and analysis of passive devices in silicon RF $0.13\mu m$ CMOS process. This thesis has provided lumped models and engineering insight, which facilitates the design and optimization of on-chip passive components.

References

[1]   D. M. Pozar, *Microwave Engineering.* New York: Wiley, 1998.

[2]   G. A. Deschamps, "Electromagnetics and differential forms," *IEEE Journal of Solid State Circuits,* vol. 69, pp. 676–696, June 1981.

[3]   H. Hasegawa, "Properties of microstrip line on Si–SiO system," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-19, pp. 869–881, Nov. 1971.

[4]   R. E. Amaya, P. H. R. Popplewell, M. Cloutier, and C. Plett, "Analysis and measurements of EM and substrate coupling effects in common RF integrated circuits," *Custom Integrated Circuit Conference,* pp. 363–366, Oct. 2004.

[5]   Mina Danesh, "Monolithic Inductors for Silicon Radio Frequency Integrated Circuits", M.Sc. Thesis, University of Toronto, January 1999.

[6]   Stanford Microwave Integrated Circuit Laboratory, Available: Stanford Website, http://smirc.stanford.edu/spiralCalc.html [Accessed: June, 2007].

[7]   J. C. Rautio, "An investigation of microstrip conductor loss," *IEEE Microwave Mag.,* pp. 60–67, Dec. 2000.

[8]   A. E. Kennelly, F. A. Laws, and P. H. Pierce, "Experimental researches on skin effect in conductors," *Trans. AIEE,* vol. 34, pp. 1953–2018, 1915.

[9]   R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE Journal of Solid-State Circuits,* vol.31(3), pp. 344–53, March 1996.

[10]   Robert E. Collin, *Field Theory of Guided Waves.* New York: IEEE Press, 1990.

[11]   C. P. Yue and S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon," *IEEE Transactions on Electron Devices,* vol.47, no.3, pp.560-568, Oct. 2000.

[12]   J. Zheng, Y. C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microwave Theory Tech.,* vol. 48, pp. 1443–1451, Sept. 2000.

[13]   J. Zheng, V. K. Tripathi, and A. Weisshaar, "Characterization and modeling of multiple coupled on-chip interconnects on silicon substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1733–1739, Oct. 2001.

[14]   A. Scudder, T. Biondi, E. Ragonese, and G. Palmisano, "A Scalable Model for Silicon Spiral Inductors," *IEEE MTT-S Microwave Symposium*, pp.2117-2120, June 2003.

[15]   A. Weisshaar and H. Lan, "Accurate closed-form expressions for the frequency-dependent line parameters of on-chip interconnects on lossy silicon substrate," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, May 20–25, 2001, pp. 1735–1756.

[16]   T. C. Edwards and M. B. Steer, *Foundations of Interconnect and Microstrip Design*. New York: Wiley, 2000.

[17]   X. Shi, J. Ma, B. H. Ong, K. S.Yeo, M. A. Do, and E. Li, "Equivalent circuit model of on-wafer interconnects for CMOS RFICs," in *Proc. IEEE RAWCON*, Atlanta, GA, pp. 95–98, Sep. 2004.

[18]   J. R. Long and M. A. Copeland, "Modeling, characterization and design of monolithic inductors for silicon RF IC's," in *Proc. Custom Integrated Circuits Conf. (CICC)*, pp. 185–188, Oct.1996.

[19]   Y. K. Koutsoyannopoulos and Y. Papananos, "Systematic analysis and modeling of integrated inductors and transformers in RFIC design," *IEEE Trans. Circuits Syst.*, vol. 47, no. 8, pp. 699–713, Aug. 2000.

[20]   G. F. Zhang and J. L. Gautier, "Broad-band, lossless monolithic microwave active floating inductor," *IEEE Microwave Guided Wave Lett.*, vol. 3, pp. 98–100, Apr. 1993.

[21]   J. N. Burghartz, M. Souyer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 100–104, Jan. 1996.

[22]   A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RFIC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 1470–1481, Oct. 1998.

[23]   S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419-1424, Oct. 1999.

[24]   G. Bartolucci, F. Giannini, E. Limiti, and S. P. Marsh, "MIM capacitor
         modeling: A planar approach," *IEEE Trans. Microwave Theory Tech.*, vol.
         43, pp. 901–903, Apr. 1995.

[25]   A. Sutono, A. H. Pham, J. Laskar, and W. R. Smith, "RF/Microwave
         characterization of multilayer ceramicbased MCM technology," *IEEE
         Trans. Advanced Packaging*, vol. 22, pp. 326-331, Aug. 1999.

[26]   B. Berker, G. Cokkinides, and A. Templeton, "Analysis of microwave
         capacitors and IC packages," *IEEE Trans. Microwave Theory Tech.*, vol.
         42, pp. 1759–1764, Sept. 1994.

[27]   B. Lakshminarayanan, H. C. Gordon, and T. M. Weller, "A substrate
         dependent CAD model for ceramic multi-layer capacitors," *IEEE Trans.
         Microwave Theory Tech.*, vol. 48, pp. 1687–1693, Oct. 2000.

[28]   D.T. S. Cheung, J. R. Long, R. Hadaway, and D. Harame, "Monolithic
         transformers for Silicon RF IC design," *IEEE Bipolar and BiCMOS
         Technology*, pp. 105–108, Sept. 1998.

[29]   A. Boulouard and M. Le Rouzic, "Analysis of rectangular spiral
         transformers for MMIC applications," *IEEE Trans. Microwave Theory
         Tech.*, vol. 37, pp. 1257–1260, Aug. 1989.

[30]   T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuit*.
         New York, Cambridge University Press, 1998.