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Modeling and noise parameter extraction of nano-wire transistors

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MODELING AND NOISE PARAMETER EXTRACTION OF NANO-WIRE TRANSISTORS

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ABSTRACT

MODELING AND NOISE PARAMETER EXTRACTION OF NANO-WIRE TRANSISTORS

Pallavi Deshmukh

Since the CMOS technology is advancing rapidly, there are several new device structures being invented to counter the disadvantages of the previous generation. One of the attractive devices in this realm is Nano-wire Surrounding Gate FET (SGFET) which is built vertically and has gate wrapped all around the channel. This thesis will investigate the noise performance of transistor at high frequencies for its application in designing RF Low Noise Amplifiers. This is the first time that a study has been done on noise characteristics of SGFET.

The thesis presents a novel approach for noise parameter extraction of MOSFET. This method, called Direct Matrix Analysis, can be used for very complex models which makes the analysis easier.

The scaling of planar MOSFET's was done to compare the noise characteristics of 3-D and planar devices. Various scaling theories were investigated and then Constant Field Scaling Theory was applied to scale down the MOSFET's.

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CHAPTER 1

INTRODUCTION

As the transistors are being scaled down, the issue of short channel effects becomes more severe and critical. Hence some alternative approaches have already started coming up, one of the attractive options being Nano-wire surrounding gate FET (SGFET). This structure has a lower subthreshold swing as compared to FinFETs. Also since the gate is wrapped around the channel, corner effect impact is minimized. SGFET's have an advantage of immunity to short channel effects, suppression of floating body effects and improved transport properties. SGFET's have reduced scattering and better gate control as compared to other device structures. They also have enhanced current densities. Since this device has scope of applications in RF, Microwave domains as Low Noise Amplifier, Mixer, noise characterization is very important for analysis of this device. At high frequencies, the induced gate noise and the channel noise are correlated which is difficult to model. Hence they have to be extracted directly from the scattering parameters of the noise model for a device. This was the approach used to analyze noise in SGFET's.

The thesis includes an analysis of SGFET based on the following points:

1) High frequency noise model of the SGFET

2) Noise Corrélation Matrix and Noise Parameter extraction

3) Equations for individual noise sources in the model

4) Comparison in different configurations

5) Discussion of dominant noise sources

6) Comparison of noise parameters of SGFET with scaled bulk CMOS model

The noise model of SGFET consists of active two ports, passive components and some noise voltage or current sources. The accuracy of noise modeling depends on the topology of small signal model combined with the accurate values for the model elements which can precisely predict the electrical performance of the device.

The accurate small signal model was already available for SGFET. Hence the approach chosen for noise modeling was Direct Matrix Analysis. MATLAB was used to implement the algorithm and analysis was done for three different configurations of SGFET – Common Source, Common Gate and Common Drain configurations.

1.1 Types of Noise

MOSFET devices have different types of noises:

1) Thermal Noise
2) Flicker Noise
3) Induced Gate noise
4) Channel Noise

1.1.1 Thermal Noise

At high frequencies, the dominant noise source in the channel is thermal noise. This noise arises due to random thermal motion of carriers in the channel of the device. It is broadband white noise and gets worse with increase in temperature and resistance.

H. Nyquist showed in his paper, [1] that to find the noise amplitude, the energy of electrical oscillation along the shorted transmission line has to be added. This transmission line is connected by two resistors R. The frequency interval is assumed to be Δf and P is the available power from each resistor.

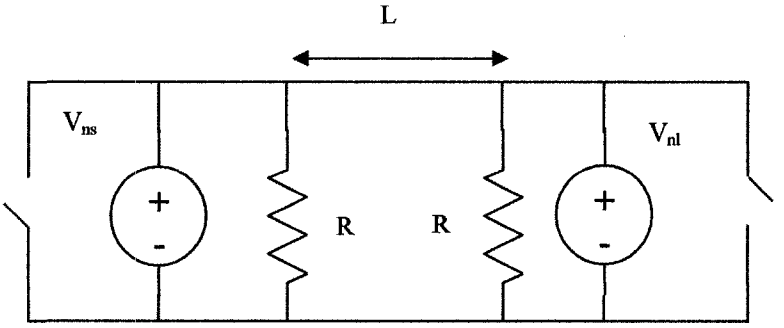

Fig.1-1 Ideal Transmission line with characteristic impedance R

$$P = V_{ns}^2/R \tag{1.1}$$

Where V_{ns} is the input noise voltage. Then the energy from the resistor on left can be given by:

$$E = \int P\, dt = P\, \Delta t = P\, L/v \tag{1.2}$$

Where Δt is the time required to travel on the line and v is the propagation velocity of the wave. Total energy on line is 2PL/v. The equipartition law of thermodynamics states that every mode of oscillation contributes approximately kT average energy.

This can be shown easily. When the both ends of transmission line are short circuited, normal modes are excited and it forms a quantum harmonic oscillator. The natural frequency is then nv/2L. Density of states in frequency will be $dn = (2L/v)\, df$ and the number of states in frequency interval Δf are: $N = (2L/v)\, \Delta f$.

$E = hf(n+1/2)$ is the energy per photon in each level.

Hence, average energy per mode will be

$$Eav = hf/(\exp(hf/KT) - 1) \approx kT \qquad (1.3)$$

This is based on the assumption that $hf/KT << 1$.

Hence the total energy on line: $2PL/v = kT\Delta f$. If the following circuit is considered, $P = i_n^2 R = V_{ns}^2/4R$.

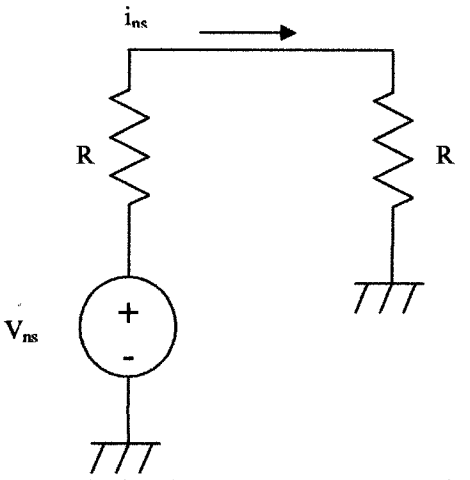

Fig.1-2 Transmission line model after shorting the line

Therefore, $kT\Delta f = V_{ns}^2/4R$

Hence,

$$V_{ns}^2 = 4KRT \qquad (1.4)$$

which is the thermal noise generated by a resistor.

1.1.2 Flicker Noise

Flicker noise is the low frequency noise which affects the performance of device and can be neglected at very high frequencies, but it cannot be neglected in case of mixers, oscillators or frequency dividers which up convert low frequency noise to high

frequency, thus giving inferior phase noise or SNR. Flicker noise dominates noise at low frequencies. The exact cause for flicker noise is not known and they are still under discussion. The traps at Si-SiO_2 interface play an important role in contribution to flicker noise. There have been many models to characterize flicker noise, of which unified theory is the most popular.

In case of SGFET, the flicker noise models which are used for submicron MOSFETS need some modification in the values fitting factors KF and AF. Since the channel length is in nanometer range, the number of carriers in the channel is less which helped us to predict a lower value of flicker noise in SGFET as compared to the MOSFET's.

The following model which is available in the HSPICE simulator for flicker noise was used to model flicker noise in SGFET [1].

In terms of transconductance of the device:

$$Sid = \frac{KF * G_m^2}{C_{ox} * L_{eff} * W_{eff} * f^{AF}} \qquad (1.5)$$

Where $W_{eff} = 2*pi*R$, R: Radius of the channel, KF: Fitting factor, AF: Fitting factor
The fitting parameters KF and AF change in case of SGFET.

For planar devices, it has been seen that flicker noise in a device with 1.5nm gate oxide thickness is lower than that in devices with thicker gate oxides. It means the noise behavior of the devices has been improved with decreasing the gate oxide thickness for short channel transistors.

With this it can be predicted that SGFET will have a lower flicker noise as compared with other device structures, since the oxide thickness is around 2nm.Some measured data needs to be taken to verify this behavior. More extensive further work is needed to validate the flicker noise models for SGFET and develop more advanced models for switch biasing and RF applications.

A channel width W and length Δx is considered. The fluctuations in channel carrier and mobility are given by

$$\left(\frac{\delta I_d}{I_d}\right) = \left(\frac{1}{\Delta N}\frac{\Delta\delta N}{\Delta\delta N_t} + \frac{1}{\mu}\frac{\delta\mu}{\Delta\delta N_t}\right)\Delta\delta N_t \tag{1.6}$$

(1.6)

Where $\Delta N = NW_{\Delta X}, N_t = N_t W\Delta_X$, N and N_t are respectively the number of channel carriers and occupied traps per unit area. The typical mobility equation is

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_1} = \frac{1}{\mu_0} + \alpha N_t$$

(1.7)

Where μ_I is the mobility limited by oxide charge scattering. It is expected that the scattering coefficient α is bias dependent due to carrier screening effect.

$$\frac{\delta I_d}{I_d} = -\left(\frac{1}{N} + \alpha\mu\right)\frac{\delta\Delta N_t}{W_{\Delta X}}$$

(1.8)

$$S_{\Delta I_d}(f) = \frac{I_{d^2}}{(W^2\Delta X^2)(\frac{1}{N} + \alpha\mu)^2 S_{\Delta N_t}(f)}$$

$$= \frac{\frac{I_{d^2}}{(W\Delta_X)(\frac{1}{N} + \alpha\mu)^2}(N_T(E_F)kT}{\gamma f} \tag{1.9}$$

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta I_d}(f)\Delta x dx$$

$$= \frac{kTI_{d^2}}{\gamma f W L^2}\int_0^L N_T(E_F)(\frac{1}{N(x)} + \alpha\mu)^2 dx \tag{1.10}$$

$$S_{\Delta I_d}(f) = \frac{kTI_{d^2}}{\gamma f W L^2}\int_0^L \frac{A + BN + CN^2}{N^2} dx \tag{1.11}$$

where A,B,C are technology dependent model parameters. A, B, C can be determined by fitting the measured noise data. It is noted that A+BN+CN2 is the apparent oxide trap density extracted from the noise measurement if one ignores the contributions from the mobility fluctuation.

1.1.3 Channel Noise

Channel noise occurs in the channel due to the channel resistance rds and is combination of flicker noise and thermal noise due to the channel resistance.

This channel noise is correlated to the gate induced noise at high frequencies and this correlation can be neglected at low frequencies. There are many models for MOSFET predicting the channel noise and its correlation with gate induced noise. Van Der Zeil model gives following equations for the channel noise [1]:

$$ids^2 = 8/3*k*T*gm \tag{1.12}$$

But when this model is directly used for SGFET, it predicts a lower noise figure; hence, a new model needs to be formulated. This model can be derived using a MOSFET model in saturation.

The drain current for MOSFET in a strong inversion region is given by:

$$I_D(x) = W_{eff}. Q_I(x).v(x) \tag{1.13}$$

Where x is position along the channel, W_{eff} is the effective channel width, $Q_I(x)$ is the inversion layer charge per unit area, and v(x) is the carrier drift velocity in the channel.

For short channel devices, the carrier drift velocity is expressed as

$$v(x) = \frac{\mu_{seff}. E(x)}{(1+E(x)/Ec)} \qquad E(x)<Ec$$

$$= v_{sat} \qquad E(x) \geq Ec \tag{1.14}$$

Where Ec is the critical filed at which carrier velocity saturation occurs. E(x) = dV(x)/dx is the lateral electric field. The critical field and effective surface mobility are given by

$$E_c = \frac{2v_{sat}}{\mu_{seff}} \tag{1.15}$$

$$\mu_{seff} = \frac{\mu_0}{(1+\Theta(V_{GS,int} - V_{T0})} \tag{1.16}$$

μ_0 is low field mobility, Θ is mobility degradation coefficient due to vertical channel field, V_{T0} is the threshold voltage at source with zero source-substrate bias, and $V_{GS,int}$ is the voltage drop between gate and source for the intrinsic device. Substituting v(x) in Eq.1.13 with Eq.1.14, the drain current becomes

$$I_D(x) = (\mu_{seff} . W_{eff} . Q_I(x) - I_D(x)/Ec).dV/dx \qquad (1.17)$$

Integrating this current over the effective channel length and solving for I_D gives the equation shown below:

$$I_D = 1/L_{eff} \int_{V_{S,int}}^{V_{D,int}} (\mu_{seff} . W_{eff} . Q_I (V) - I_D/Ec).dV \qquad (1.18)$$

$V_{D,int}$ is the channel potential on the drain side of the intrinsic device. For a time-varying voltage fluctuation due to thermal noise in unit length segment of the channel, the current fluctuation is given by

$$\Delta i (t) = 1/L_{eff} . (\mu_{seff} . W_{eff} . Q_I (V) - I_D/Ec) . \Delta v(t) \qquad (1.19)$$

Q_I (V) being negligibly small, it is nearly constant and independent of $\Delta v(t)$. The mean square value of $\Delta i (t)$ will be given by

$$(\Delta i)^2 = 1/L_{eff}^2 . (\mu_{seff} . W_{eff} . Q_I (V) - I_D/Ec)^2 . (\Delta v)^2 \qquad (1.20)$$

Thus the resistance of the small element of the channel and the mean square value of voltage across this resistor are given by

$$\Delta R = \Delta x/ (\mu_{seff} . W_{eff} . Q_I(x_1) - I_D(x_1)/Ec) \qquad (1.21)$$

$$(\Delta v)^2 = 4kT_e(x_1).\Delta x . \Delta f/ (\mu_{seff} . W_{eff} . Q_I(x_1) - I_D(x_1)/Ec) \qquad (1.22)$$

Where $T_e(x_1)$ is the effective electron temperature. Similarly mean square value of current will be as follows:

$$(\Delta i)^2 = 4kT_e(x_1)/L_{eff}^2 . (\mu_{seff} . W_{eff} . Q_I(V) - I_D/Ec)^2 . \Delta x . \Delta f \quad (1.23)$$

To obtain the effective channel thermal noise, this current needs to integrated along the length of the channel as shown below. Then solving Equations 1.24 – 1.26 gives the overall value of channel thermal noise.

$$i^2_d = (4k/L^2_{eff}.I_{D)} \int_{V_{S,int}}^{V_{D,int}} T_e(x).(\mu_{seff} . W_{eff} . Q_I(V) - I_D/Ec)^2 \, dV \quad (1.24)$$

$$1+E(x)/E_c = (\mu_{seff} . W_{eff} . Q_I(V))/\mu_{seff} . W_{eff} . Q_I(V) - I_D/Ec \quad (1.26)$$

Thus the channel thermal noise equation is given by

$$i^2_d = (4kT/L^2_{eff}.I_{D)} \int_{V_{D,int}}^{V_{D,int}} (\mu_{seff} . W_{eff} . Q_I(V))^n \times (\mu_{seff} . W_{eff} . Q_I(V) - I_D/Ec)^{2-n} dV \quad (1.27)$$

1.1.4 Induced Gate Noise

At high operating frequencies, the random potential fluctuations in the channel, results in the channel noise, which gets coupled to the gate terminal through the gate oxide capacitance and causes induced gate noise. Induced gate noise is correlated to the channel noise at high frequencies. Eq.1.26 is the wave equation of a distributed line representing a MOSFET.

$$\frac{d}{dx}[\Delta I_D(x)] = j \omega W_{eff} C_{ox} \Delta v(x) \quad (1.28)$$

$\Delta v(x)$ is the AC voltage fluctuation along the channel. This equation can be expanded for $Y_{gs\ to}$ get

$$Y_{gs} = 1/(1/j \omega C_{gs} + R_i) \quad (1.29)$$

For frequency $\omega^2 R^2 C^2 << 1$, C_{gs} and Ri can be solved to get the equations 1.30 and 1.31.

$$C_{gs} = (2/3)W_{eff} L_{eff} C_{ox} \quad (1.30)$$

$$Ri = 1/5g_{m0} \quad (1.31)$$

Where $g_{m0} = (\omega L_{eff}^2)/[\mu_{seff}(V_{GS,int}-V_{T0})]$

The total gate noise current flowing out of the gate is obtained by integrating along the effective channel length.

$$\Delta i_g = j\,\omega\, W_{eff} C_{ox} \int \Delta v(x) \quad (1.32)$$

Thus the gate induced noise equation is given by Eq.1.33.

$$i^2_g = [(4KT\omega^2 W_{eff}^2 C_{ox}^2)/ I^3_D] \int_{V_{S,int}}^{V_{D,int}} (\mu_{seff} . W_{eff} . Q_I (V))^n \times (\mu_{seff} . W_{eff} . Q_I (V) - I_D/Ec)^{2-n} \times (Vas-V)^2 dV \quad (1.33)$$

1.2 Noise Parameter Extraction Method

The noise Figure is the ratio of signal to noise ratio at input and signal to noise ratio at output. It can be represented in terms of the equivalent noise resistance of the circuit (R_n), optimized source conductance (G_{opt}), and optimized source susceptance (B_{opt}) [1].

For a two port network, the noise parameters can be calculated using the following equations:

$$R_n = R_u \quad (1.34)$$

$$G_{opt} = sqrt(G_i/R_n - B_{cor}^2) \quad (1.35)$$

$$B_{opt} = -B_{cor} \quad (1.36)$$

$$NF_{min} = 1+2Rn\,(G_{opt}+G_{cor}) \quad (1.37)$$

For a 2-port network, the admittance nodal equations can be written as follows:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} B \\ D \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (1.38)$$

Where [B] = [1 0] and D = [0 1]. The noise correlation matrix [C] is defined as:

$$[C] = \begin{vmatrix} \overline{i_1 i_2^*} & \overline{i_1 i_2^*} \\ \overline{i_2 i_2^*} & \overline{i_1 i_2^*} \end{vmatrix} \quad (1.39)$$

Using the y-parameters, B, C and D matrices, R_u, G_i, Y_{cor} can be calculated for any network using the expression given below [1].

$$R_u = (1/4kT\,\Delta f) \times \mathrm{Re}\,\{1/\mathrm{abs}\,(Y_{21})^2 \times [D]^* \times [C] \times [D]^T\} \quad (1.40)$$

$$G_i = (1/4kT\Delta f) \times \mathrm{Re}\,\{([B]-Y_{11}/Y_{21} \times [D])^* \times [C] \times ([B]-Y_{11}/Y_{21} \times [D])^T\} \quad (1.41)$$

$$Y_{cor} = G_{cor} + jB_{cor} \quad (1.42)$$

$$Y_{cor} = (-1/4kT\Delta f\, Rn Y_{21}^*) \times \{[D]^* \times [C] \times ([B] - Y_{11}/Y_{21} \times [D])^T\} \quad (1.43)$$

These expressions can be applied to any noise model having correlated noise sources. Traditional MOSFET analysis use direct matrix analysis which can also be applied to the SGFET noise model.

This method needs the noise model of the device which can then be transformed to an equivalent graph for network analysis. The nodal equations are then written corresponding to each node to form a Y parameter matrix for the noise model. Also an [A] matrix is formed which represents the current sources in the network.

The matrices are then reduced to represent a 2-port network considering all the noise sources and resistances. These Y parameters can then be used and substituted in the equations to get the noise parameters of the circuit. Equations (1.44) and (1.45) are used for matrix reduction. [Y] Matrix is reduced to 2x2 matrix from 7x7 for SGFET and 6x6 for MOSFET. [A] Matrix is reduced to 2x7 matrix for SGFET and 2x6 for MOSFET.

$$Y_{ij}' = Y_{ij} - \frac{(Y_{im} * Y_{nj})}{Y_{mn}} \tag{1.44}$$

$$A_{ij}' = A_{ij} - \frac{(A_{im} * Y_{nj})}{Y_{mn}} \tag{1.45}$$

Where mxn is the order of the matrix and i, j represent the rows and columns respectively.

[A] matrix is used to form the [B] and [D] matrices. The correlation matrix shown in equation can be used here to calculate the parameters. MATLAB program was used to calculate the noise parameters.

This method was then implemented for Common Gate and Common Drain configurations. Using Direct Matrix Analysis simplifies the analysis part. In case of Common Gate Configuration, the gain characteristics are same as in Common Source configuration, whereas the noise characteristics change. It can be seen from the graphs in next section that at low frequencies, flicker noise doesn't contribute much to noise figure

as was seen in CS configuration. The minimum noise figure increases with increase in operating frequencies.

In case of Common Drain configuration, gain is approximately one, since it acts as a source follower.

The noise figure is high at low frequencies, then goes to a minimum value and again increases at high frequencies.

1.3 Noise Correlation Matrix Formation

There are three types of representation for Noise correlation matrix.

1) Admittance representation which is based on noise currents
2) Impedance representation based on noise voltages
3) Wave representation based on noise waves

In case of noise modeling of SGFET, since we have characterized the model using current sources, the admittance representation was used.

The formation of noise correlation matrix depends on the currents at each node. The diagonal elements in the matrix are equal to the sum of the noise current of each element connected to the corresponding node. So the first diagonal element is the sum of noise currents connected to node 1, the second diagonal element is the sum of noise currents connected to node 2, and so on.

The off diagonal elements are the negative noise current of the element connected to the pair of corresponding node. Therefore a noise current source between nodes 1 and

2 goes into the matrix at location (1, 2) and locations (2, 1). If a noise current source is grounded, it will only have contributed to one entry in the noise correlation matrix at the appropriate location on the diagonal. If it is ungrounded it will contribute to four entries in the matrix two diagonal entries (corresponding to the two nodes) and two off-diagonal entries. Since SGFET noise model has seven nodes and seven noise sources, the matrix which is formed is 7x7 and it is 6x6 for MOSFET.

1.4 Summary

Thus various types of noise, their equations, and the extraction method called Direct Matrix Analysis were discussed in this chapter. The application of this theory is shown in forthcoming Chapters 3 and 4. This method is used for noise analysis of SGFET and MOSFET's. It can be applied to any complex network whose noise model is accurately known.

CHAPTER 2

NOISE OF BULK MOSFET

2.1 Scaling Theory

For comparison of 3-D device noise characteristics with a planar device, it was necessary that the device sizes are same. Hence the planar MOSFET model was scaled down to 10nm regime and analyzed for noise. For scaling of MOSFET, various scaling theories were investigated. Some of the common scaling theories are:

1) Constant voltage scaling
2) Constant field scaling

The rules for scaling can be expressed in terms of the scaling constant K> 1. The device dimensions are scaled with a factor of K. But if the voltage and doping impurity concentrations are not scaled accordingly, the device will not withstand such a high current density and thus breakdown. Hence it is very important to scale down the supply and threshold voltage, and scale up the doping levels by the scaling constant.

The other parameters like rds, parasitic capacitance and the interconnect resistance are then scaled proportionately using the traditional formulae. Figures shown illustrate the scaling theory. Fig. 7-1 shows the non-scaled MOSFET and Fig. 7-2 scaled MOSFET which has the dimensions scaled down by factor of K>1.

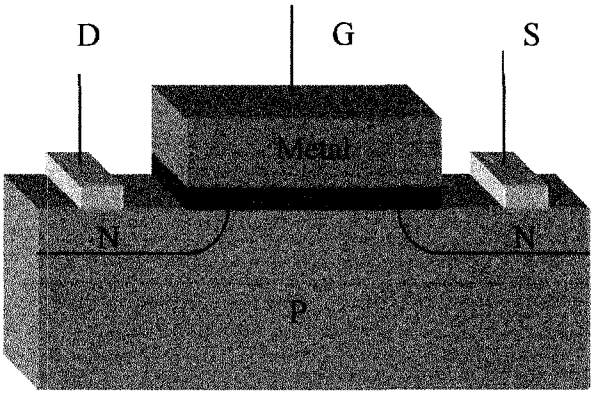

Fig. 2-1 Non-scaled MOSFET Device

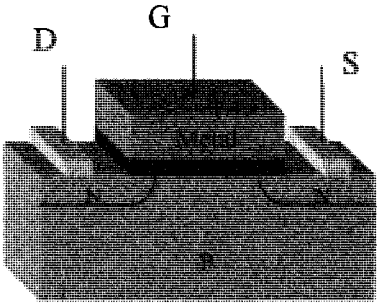

Fig. 2-2 Scaled MOSFET Device

2.2 Calculations for Scaling MOSFET

SGFET device has W=12.6 nm and L = 10nm. The MOSFET was thus scaled down according to this W/L ratio which gave different scaling factors for width and length scaling. The scaling factor for length has been denoted by K_L, while it is K_W for width scaling. The MOSFET device had W/L ratio of 60um/.18um which gives the following scaling factors:

$$K_L = 18$$

$$K_W = 14.356$$

Table 2-1 Scaling Factors used for MOSFET scaling to nanometer regime

Parameter	**Scaling Factor**
Vertical Dimensions	$1/K_w$
Horizontal Dimensions	$1/K_L$
Voltages	$1/K$
Substrate Doping concentration	K_L
Channel Resistance	$(K_W)/(K_L)^{(3/2)}$
Cgox	$1/K_L$
Cgs	$1/K_W$
Cgd	$1/K_W$
Cgb	$1/(K_L^2 * K_W)$
Cdb	$3*C_{gs}$
Csb	$3*C_{gs}$
Transconductance	$(K_L)^{(3/2)}/(K_W)$

For verification of these calculated results, the behavior of various parameters with gate channel length was analyzed after studying various papers. The values were used in MATLAB to extrapolate the values of the parameters at 10nm.

Table 2-2 Channel Resistance for various gate lengths for MOSFET scaling [2], [3],[4],[6],[10]

Gate Length [um]	Rds (Vgs-Vt =1)	Rds (Vgs-Vt =.5V) Rds*2	Rds (Vgs-Vt =.2) Rds*2.5	Rds (Vgs-Vt =.2) Rds*35
.08	380	760	1.9k	66.5
.35	400	800	2k	70
.4	480	960	2.4k	84k
.45	540	1080	2.7k	94.5k
.5	600	1200	3k	105k

Table 2-3 Transconductance for various gate lengths MOSFET scaling [2], [3], [8]

Gate Length [um]	Gm(uA/V)
0.1	610
0.2	390
0.3	350
0.4	300
0.5	210

Table 2-4 Effective Mobility for various gate lengths for MOSFET Scaling [2], [12], [13]

Gate Length [nm]	Effective Mobility (cm^2/V-s)
30	1800
50	2480
100	3632
300	4680
350	4000

Table 2-5 Junction Capacitance for various gate lengths for MOSFET Scaling [5], [6], [7], [8]

Gate Length [um]	Junction Capacitance (aF)
0.089	150aF
0.18	313aF
0.35	200aF
0.8	1096aF

2.3 Extrapolated Results for MOSFET

Fig. 2-3 shows the extrapolation of channel resistance for MOSFET to get the value of rds at 10nm. This curve fitting was done using MATLAB. The value of rds comes to 27kOhm.

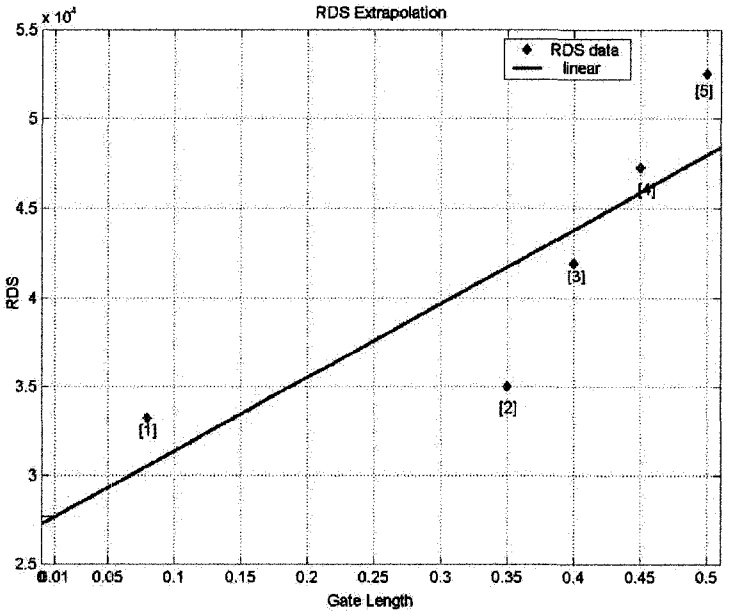

Fig. 2-3 Extrapolated value of channel resistance of MOSFET at 10nm [2], [3], [4], [6], [10]

Fig. 2-4 shows the extrapolated value of junction capacitance for MOSFET at 10nm. The points which are seen in the plot were values taken from various papers and then the data was extrapolated.

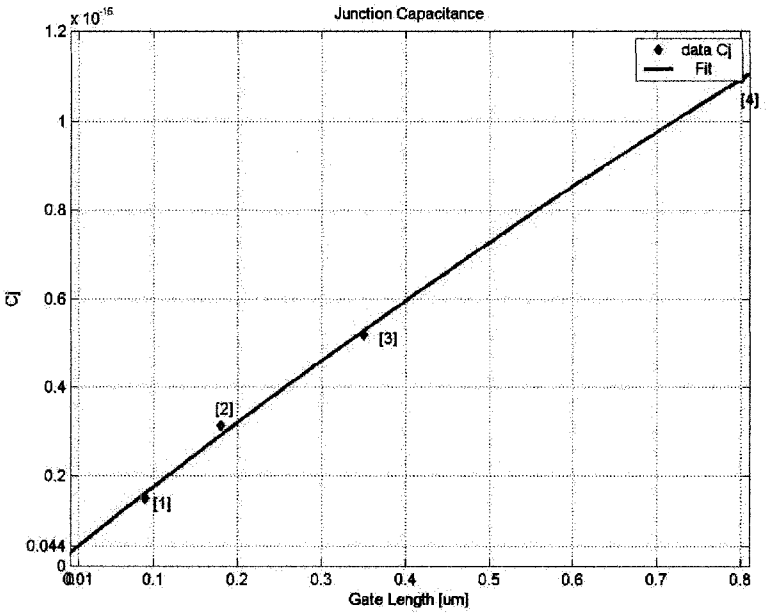

Fig. 2-4 Extrapolated value of junction capacitance
Of MOSFET at 10nm [5], [6], [7], [8]

Fig. 2-5 shows the extrapolation of transconductance for MOSFET at 10nm. Procedure similar to channel resistance and junction capacitance was used for getting g_m at 10nm. The value obtained was very close to the calculated values.

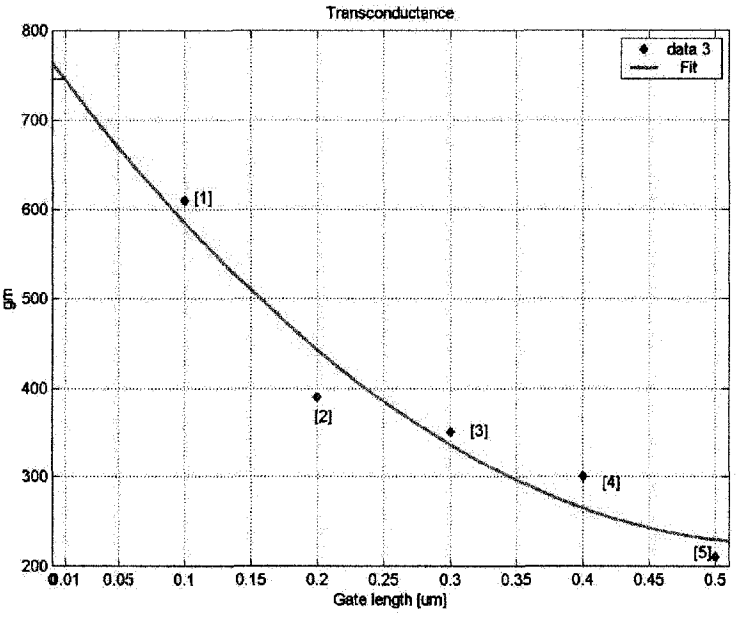

Fig. 2-5 Extrapolated value of transconductance for MOSFET at 10nm [2], [3], [8]

Fig. 2-6 shows the extrapolation of effective mobility for MOSFET as a function of gate length. It can be seen that as gate length decreases, mobility degradation occurs. Curve fitting was done using MATLAB.

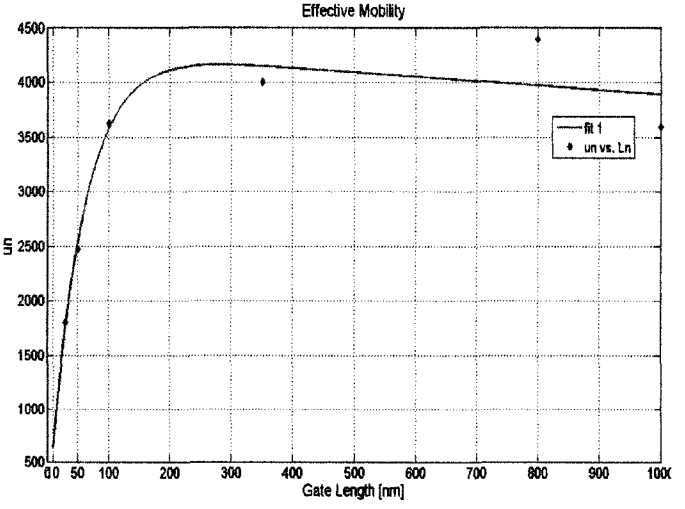

Fig. 2-6 Extrapolated value of Mobility in MOSFET at 10nm [2], [12], [13]

Table 2-6 shows the model parameter values for SGFET, MOSFET which was used for scaling and the scaled MOSFET. These values of scaled MOSFET were used in the noise model to get the noise characteristic. The same method of Direct Matrix Analysis was used and implemented using MATLAB.

Table 2-6 Table showing the elements of small signal model for SGFET, Non-scaled MOSFET and scaled MOSFET

PARAMETER	SGFET	MOSFET(Non-Scaled)	MOSFET SCALED
Wmin	12.54nm	.18um	12.54nm
Lmin	10nm	.18um	10nm
Gm	14uA/V	28.4mA/V	745uA/V
Rds	600k	486	27k
rds	3k	-----	-----
Rg	10	5.75	15.17
Rs	200	1.75	1500
Rd	70	1.75	1500
rg	.11	------	----
Rdb	-----	134	600k
Cgs	4aF	68.5e-15F	10.87aF
Cds	1.3aF	68.5e-15	10.87aF
Cgd	1.3aF	30.6e-15F	12.16aF
Cgox/Cox	3aF	1.25e-3	2.24e-2
Cgb	----	1e-21F	.4aF
Cdb	----	76.9e-15F	30.87aF
Csb	----	496e-15F	30.87aF

2.4 Scaled MOSFET Models and Nodal Analysis

Small Signal Model of scaled MOSFET's and the plots showing their noise behavior. It can be seen that Common Source configuration and Common Gate Configuration have the same gain, whereas Common Drain Configuration has unity gain.

The elements in the small signal model were defined as follows:

$$Y_1 = g_g \tag{2.1}$$

$$Y_2 = i*w*C_{gd} \tag{2.2}$$

$$Y_3 = g_d \tag{2.3}$$

$$Y_4 = i*w*C_{gs} \tag{2.4}$$

$$Y_5 = g_{ds} \tag{2.5}$$

$$Y_6 = i*w*C_{gb} \tag{2.6}$$

$$Y_7 = i*w*C_{sb} \tag{2.7}$$

$$Y_8 = i*w*C_{db} \tag{2.8}$$

$$Y_9 = g_{db} \tag{2.9}$$

$$Y_{10} = g_s \tag{2.10}$$

2.4.1 Common Source Configuration

The noise model of MOSFET was derived from its small signal model. This model was derived for all three configurations. Fig. 2-7 shown below shows the noise model for the scaled MOSFET in Common Source Configuration. In this configuration, the bulk and source terminals are assumed to be connected together and then to ground. MOSFET has an additional bulk resistance which is absent in case of SGFET. Also the source to bulk, drain to bulk capacitors are included in the model of MOSFET. It can be seen from the figure shown below there are six noise sources contributing to the overall noise in MOSFET. Similar to SGFET the gate thermal noise is at the input and source thermal noise is at the output.

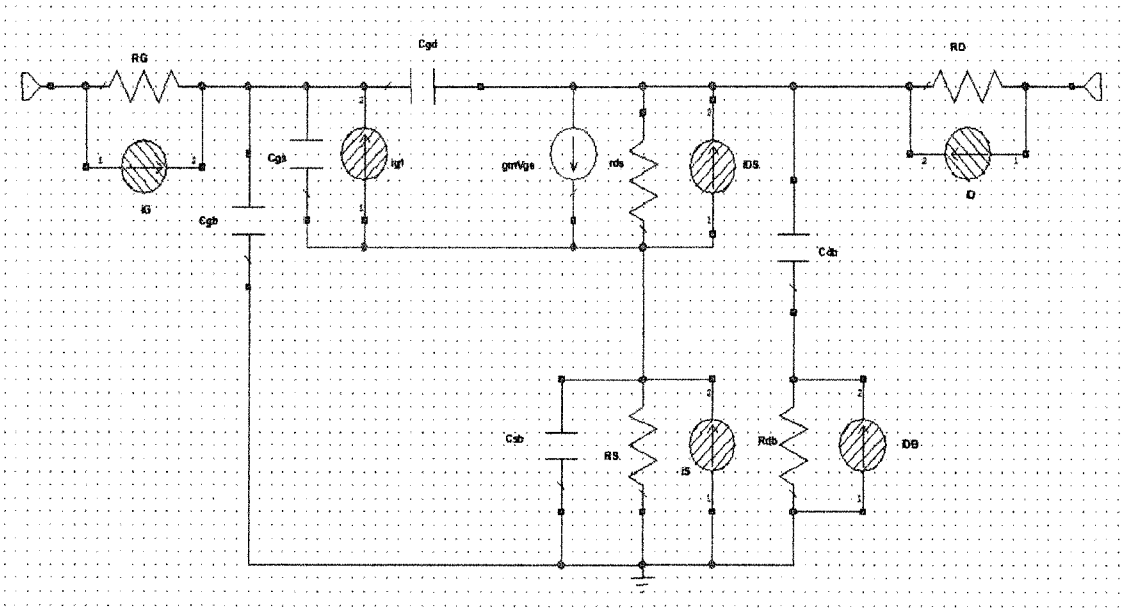

Fig. 2-7 Model of MOSFET in Common Source Configuration

Fig. 2-8 shows the network graph of MOSFET in CS configuration which is derived from Fig. 2-7. This model simplifies the analysis of circuit considerably and is useful in writing nodal equations for the circuit. As the complexity increases, representation in this form is better so as to minimize any chances of errors.

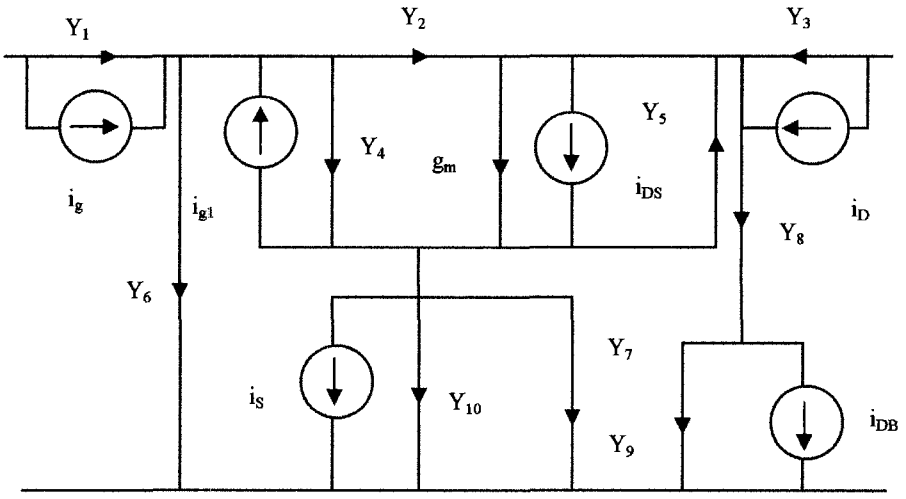

Fig. 2-8 Network Graph for Common Source Configuration

The equation below shows the admittance matrix for MOSFET in CS configuration. This matrix is determined from the nodal analysis equations written for Fig. 2-8. Matrix representation makes the data concise and easier for calculations. The MATLAB program which has been written for noise parameter calculations needs just the admittance and noise matrix as input and it characterizes the complete device.

[Y] =

$$\begin{vmatrix} Y_1 & 0 & -Y_1 & 0 & 0 & 0 \\ 0 & Y_3 & -Y_3 & 0 & 0 & 0 \\ -Y_1 & 0 & Y_1+Y_6+Y_9+Y_2 & -Y_2 & -Y_5 & 0 \\ 0 & -Y_3 & -Y_2+g_m & Y_2+Y_3+Y_8+Y_5 & -Y_5-g_m & -Y_8 \\ 0 & 0 & -g_m-Y_4 & -Y_5 & Y_7+g_m+Y_5+Y_4 & \\ 0 & 0 & -Y_6 & -Y_8 & -Y_7 & Y_8+Y_9 \end{vmatrix} \quad (2.11)$$

The equation shown below is the noise matrix for the MOSFET in CS configuration. This matrix includes the contribution of all noise sources. For an accurate noise analysis, it is very critical to get [A] and [Y] matrices accurate or the model may not predict the true characteristics of the device. Some of the noise sources may be ignored, but only if their contribution is not affecting the analysis considerably. Hence it is always better to consider all noise sources first and then determine which are dominant.

$$[A] = \begin{vmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ -1 & 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{vmatrix} \tag{2.12}$$

2.4.2 Common Drain Configuration

Fig. 2-9 shows the noise model of MOSFET in Common drain configuration. This topology acts as a source follower and has a voltage gain of one. In this case, gate thermal noise is at the input and source thermal noise is at the output. The analysis method presented in Chapter 1 is useful in transferring all the noise sources wither on the input side or on the output side. All the noise sources are included in the model shown below.

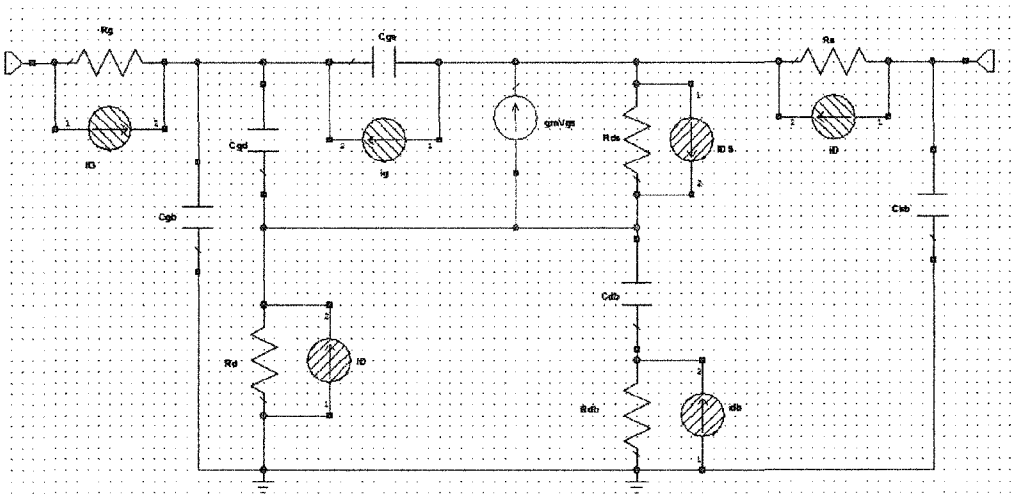

Fig. 2-9 Model of MOSFET in Common Drain Configuration

Fig. 2-10 which shows the network graph for MOSFET in CD configuration is derived from Fig. 2-9. This representation is used for writing nodal equations at each node. In this case, since there are 6 nodes, there will be six equations relating the currents, voltages and admittance of the circuit. They also include the noise current sources.

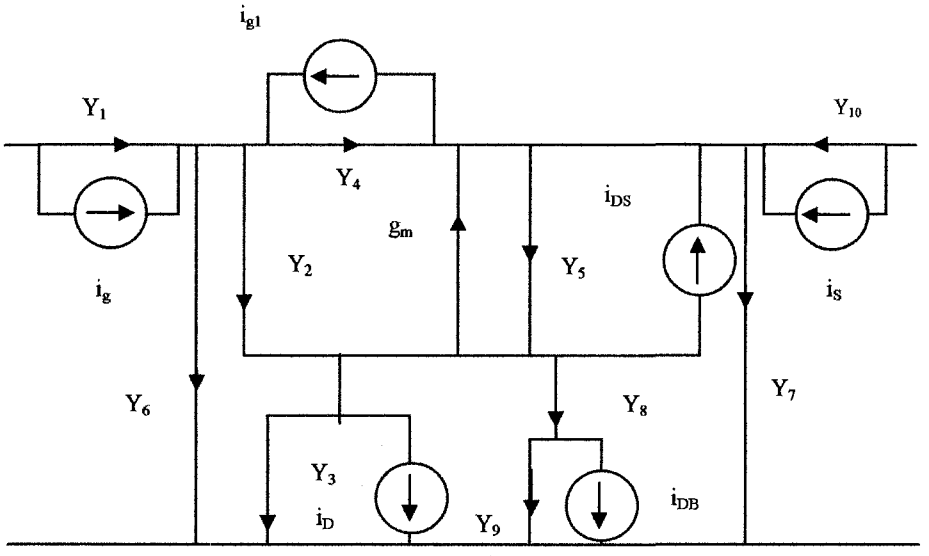

Fig. 2-10 Network Graph for Common Drain Configuration

The equation below shows the admittance matrix for CD configuration of MOSFET. [Y] Matrix represents all the admittance in the circuit. In this case, it is a 6X6 matrix since there are six equations, one for each node. This matrix is reduced to 2X2 to get the overall 2-port Y-parameters for the complete circuit. The direct matrix analysis method was implemented in MATLAB for the same. It has been discussed already in Chapter1.

[Y]=

$$\begin{vmatrix} Y_1 & 0 & -Y_1 & 0 & 0 & 0 \\ 0 & Y_{10} & 0 & -Y_{10} & 0 & 0 \\ -Y_1 & 0 & Y_1+Y_6+Y_4+Y_2 & -Y_4 & -Y_2 & 0 \\ 0 & -Y_{10} & -Y_4+g_m & Y_{10}+Y_7+Y_5+Y_4+g_m & -Y_5 & 0 \\ 0 & 0 & -g_m-Y2 & -Y_5+g_m & Y_5+Y_2+Y_3+Y_8 & -Y_8 \\ 0 & 0 & 0 & 0 & -Y_8 & Y_8+Y_9 \end{vmatrix} \quad (2.13)$$

[A] matrix shown below is the noise matrix of MOSFET in CD configuration. It shows the contribution of each noise at various nodes. [Y] and [A] matrices need to be precise for accurate characterization of noise for a device. This matrix is reduced to an order of 2X6 and not 2X2 since all the noise sources need to be considered and none of them can be eliminated from the calculations.

$$[A]= \begin{vmatrix} 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{vmatrix} \quad (2.14)$$

2.4.3 Common Gate Configuration

The noise model of MOSFET in common gate configuration in shown in figure below. In this case, bulk and source are not connected together and hence the circuit is slightly complicated. Since gate terminal is grounded, source thermal noise is at the input and drain thermal noise is at the output. Similar to CS and CD configuration, this circuit has six noise current sources and none of them can be ignored, unless their contribution is known.

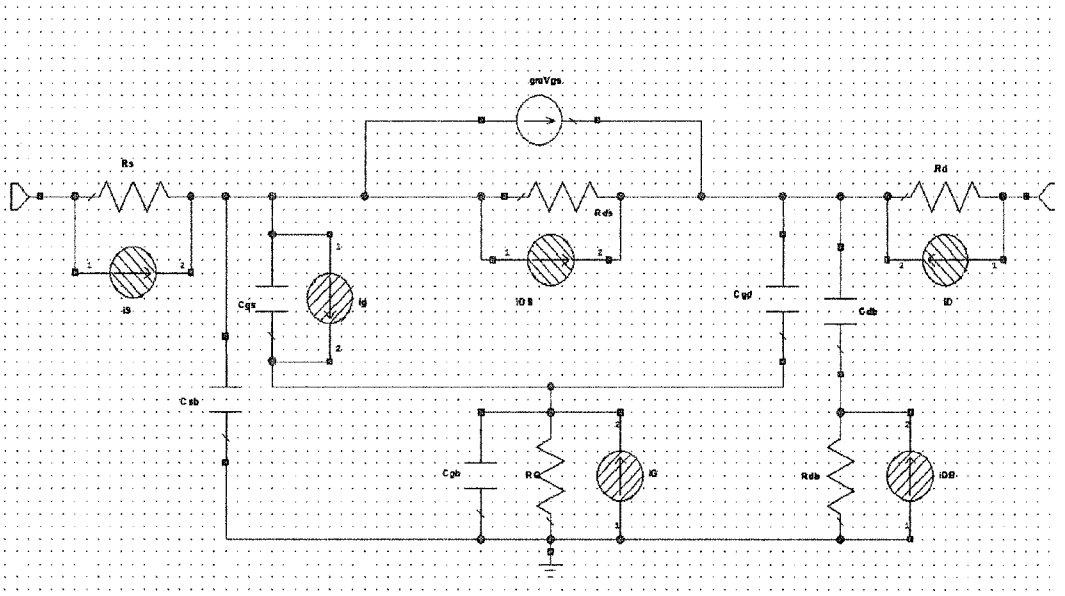

Fig. 2-11 Model of MOSFET in Common Gate Configuration

Fig. 2-12 shows the network graph for CG configuration of MOSFET. Nodal analysis is done for each of the nodes encountered in the model. This network has six nodes; hence six equations are generated using KCL. The representation of a circuit in the form shown is simple and makes the calculations and matrix formation easier.

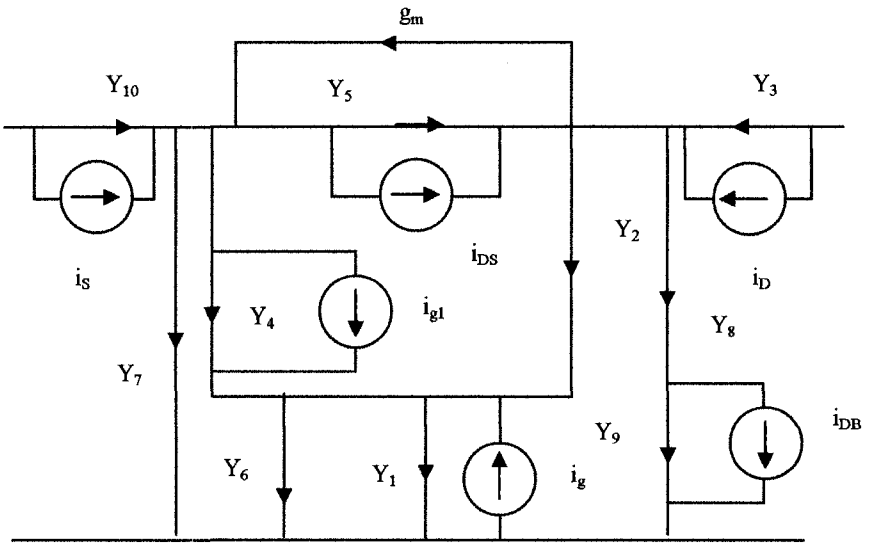

Fig. 2-12 Network Graph for Common Gate Configuration

The [Y] matrix shown below is the admittance matrix for CG configuration of MOSFET. This matrix is entirely different from the CS and CD configurations. Thus it can be predicted that the noise characteristics of each topology will vary which is shown in Chapter 4. This matrix is also 6X6 and is then reduced to 2X2 using direct matrix analysis. Thus the overall Y-parameters for the complete circuit are obtained.

[Y]=

$$\begin{vmatrix} Y_1 & 0 & -Y_1 & 0 & 0 & 0 \\ 0 & Y_3 & -Y_3 & 0 & 0 & 0 \\ -Y_1 & 0 & Y_1+Y_6+Y_4+Y_2 & -Y_2 & -Y_4 & 0 \\ 0 & -Y_3 & -Y_2+g_m & Y_2+Y_3+Y_8+Y_5 & -Y_5-g_m & -Y_8 \\ 0 & 0 & -g_m-Y_4 & -Y_5 & Y_7+g_m+Y_5+Y_4 & \\ 0 & 0 & 0 & -Y_8 & 0 & Y_8+Y_9 \end{vmatrix} \quad (2.15)$$

[A] matrix shown below is the noise matrix of MOSFET in CG configuration. This matrix also varies from one configuration to another and is unique for each circuit. Similar to CS and CD configurations, the order of this matrix is also reduced to 2X6. [B] and [D] matrices are derived from this matrix and they are then used for calculation of noise parameters. [B] and [D] matrices have been discussed in Chapter 1.

$$[A] = \begin{vmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ -1 & 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \end{vmatrix} \qquad (2.16)$$

2.5 Summary

The scaling theory best suited for MOSFET scaling was presented in this chapter. The simulation results of extrapolation of various parameters like channel resistance, mobility, transconductance and junction capacitance were very close to the calculated values.

The nodal analysis of MOSFET was also discussed and the impedance and noise matrix were derived to study the noise characteristics of scaled MOSFET. Simulation results are presented in Chapter 4. Chapter 3 deals with the nodal analysis of SGFET.

CHAPTER 3

NOISE OF SGFET

3.1 SGFET Device

The device structure of the vertical SGFET is shown in Fig. 1. The transistor is built on top of an n-well (p-well) which has a depth of 30nm and a diameter of 40nm. The intrinsic transistor has a channel length of 10nm, a radius of 2nm, a gate oxide of 1.5nm and 12nm source and drain junctions extended from both ends of the channel. NMOS and PMOS transistors are constructed as enhanced-type with undoped silicon bodies while source and drain junctions have Gaussian profiles with a peak doping concentration of 1020 cm^{-3} [11].

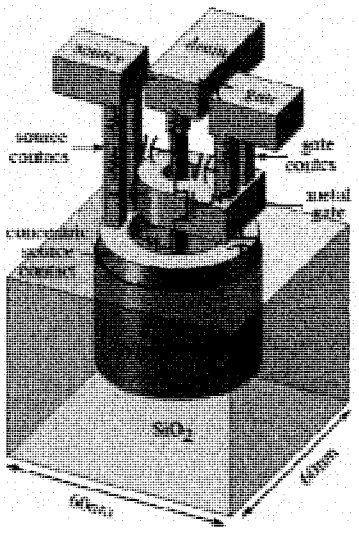

Fig. 3-1 3D view of Surrounding Gate Field Effect Transistor

3.2 Parasitic Model of SGFET

In the figure shown below, Cgsx is the parasitic capacitance between metal gate and the concentric source and Cgsy is the parasitic capacitance between metal gate and the source contact. The resistor rg accounts for the effective gate resistance at high frequencies caused by the distributed gate-oxide-channel. The resistance Rg accounts for two parallel gate contacts. Cdsx is the parasitic capacitance between intrinsic drain and source contacts and Cdsy is the parasitic capacitance between drain and source interconnects [11].

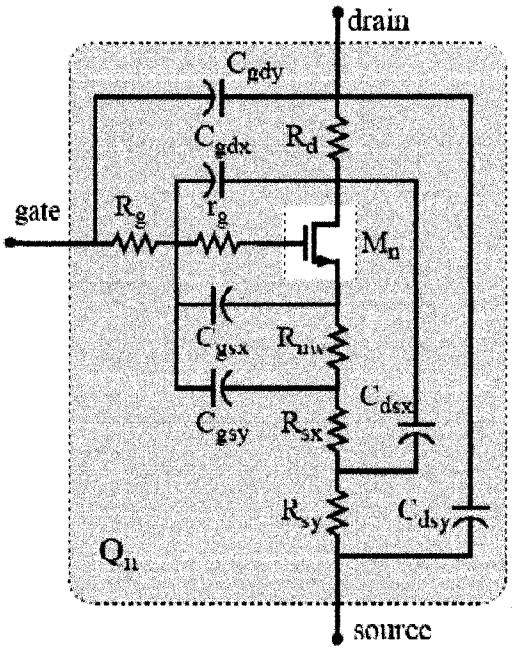

Fig. 3-2 Intrinsic Model of SGFET with Parasitics

Resistors Rsx and Rsy represent source contacts and resistors Rnw and Rpw represent overall concentric n-well and p-well resistances from intrinsic source to extrinsic source contacts of NMOS and PMOS SGFETs, respectively. Cgdx is the

parasitic capacitance between gate contact and the intrinsic drain and Cgdy is the parasitic capacitance between gate and drain interconnects. The resistor Rd represents the drain contact of the transistor [11].

3.3 Noise Model of SGFET

A noise model for any device can be derived if there is knowledge of an accurate small signal model that gives the values of capacitors and resistors. The location of noise sources in the model simplifies the derivation of noise model. Since the small signal model was already known, the noise model was derived for SGFET in all three configurations [1].

In this novel structure, there is an intrinsic transistor formed. The model also includes external parasitic, which consist of contact drain, gate, and source resistances. The parasitics encountered in this structure are the gate resistance (R_g), drain resistance (R_d), source resistance (R_s), and the resistance of intrinsic source (r_s); C_{gd} is the gate-drain capacitance which is given by

$$C_{gd} = C_{gd1} + C_{gd2} \tag{3.1}$$

Similarly C_{gs} is the gate to source capacitance and C_{ds} is the drain to source capacitance and is the sum of intrinsic gate/drain to source and extrinsic drain to source. Since the capacitors come in series for this device, the overall parasitics are reduced.

The gate, drain, and source resistances contribute to the thermal noise and can be given as follows:

$$i^2_g = 4kT/R_g \tag{3.2}$$

$$i^2_d = 4kT/R_d \tag{3.3}$$

$$i^2_s = 4kT/r_s \tag{3.4}$$

$$i^2_{Rs} = 4kT/R_s \tag{3.5}$$

The channel noise is i^2_{ds} which comes due to the channel resistance r_{ds}. The distributed gate resistance has also been considered and is represented by r_g. This contributes to the induced gate noise and is correlated with the channel noise at high frequencies. This correlation can be ignored at very low frequencies.

The noise correlation matrix for this noise model can be given as:

$C_Y =$

$$\begin{vmatrix} i_f i_f^* & i_f i_{ds}^* & 0 & 0 & 0 & 0 \\ i_{ds} i_f^* & i_d i_{ds}^* & 0 & 0 & 0 & 0 \\ 0 & 0 & i_g i_g^* & 0 & 0 & 0 \\ 0 & 0 & 0 & i_s i_s^* & 0 & 0 \\ 0 & 0 & 0 & 0 & i_d i_d^* & 0 \\ 0 & 0 & 0 & 0 & 0 & i_{Rs} i_{Rs}^* \end{vmatrix} \tag{3.6}$$

3.4 Nodal Analysis for SGFET

The noise model was derived for each configuration and then the network graphs were drawn. The network graphs simplified the process of writing nodal equations and then creating an admittance and noise matrix.

Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8, Y_9, and Y_{10} represent the various admittance elements of the small signal model. They are defined as follows:

$$Y_1 = G_g \tag{3.7}$$

$$Y_2 = i*w*C_{gd} \tag{3.8}$$

$$Y_3 = G_d \tag{3.9}$$

$$Y_4 = i*w*C_{gox} \tag{3.10}$$

$$Y_5 = g_{ds} \tag{3.11}$$

$$Y_6 = i*w*C_{gs} \tag{3.12}$$

$$Y_7 = g_s \tag{3.13}$$

$$Y_8 = G_s \tag{3.14}$$

$$Y_9 = g_g \tag{3.15}$$

$$Y_{10} = j*w*C_{ds} \tag{3.16}$$

3.4.1 Common Source Configuration for SGFET

The small signal model and network graph for Common Source Configuration of SGFET is as shown in Fig. 3-4 and Fig. 3-5.In common source configuration, gate thermal noise is at the input and drain thermal noise is at the output. Noise extraction method transfers all the noise sources in the circuit either on the input side or on the output side of the circuit. This is helpful in analyzing the overall noise contribution of all noise sources in the circuit.

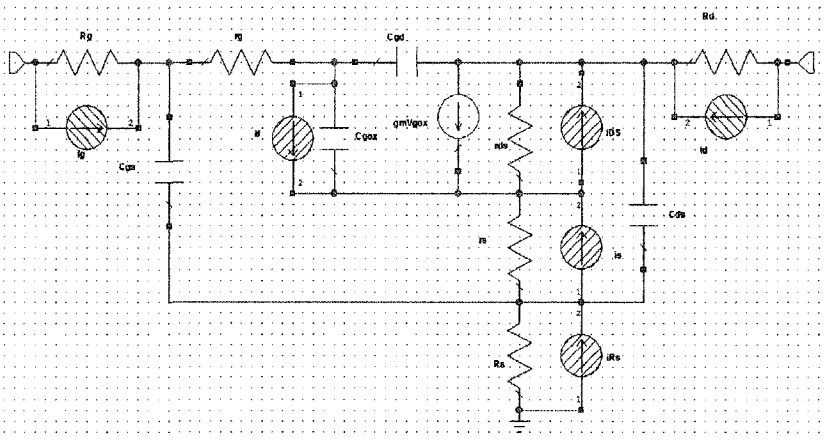

Fig. 3-3 Noise Model in Common Source Configuration of SGFET

Fig. 2-4 shows the network graph which is derived from the small signal model of SGFET in Common Source Configuration. There are seven nodes in this circuit where KCL can be applied to get the equations for each node. These equations are then used to form an admittance matrix and a noise matrix.

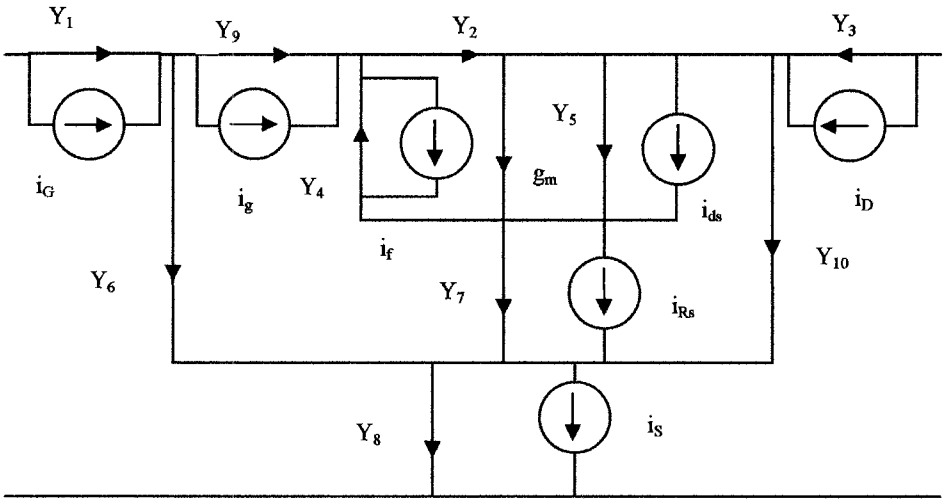

Fig. 3-4 Network Graph in Common Source Configuration for SGFET

For CS configuration, the [Y], [A] matrices are given by the following equations. [Y] matrix shows the admittance at each node of the circuit. This matrix is formed after writing nodal equations for the small signal model. This representation in matrix form is easier to implement in MATLAB and thus apply matrix reduction techniques. This matrix is 7X7 which is reduced to the order of 2X2 which thus gives overall Y-parameters for the circuit. This method is simple compared to the method of shorting the input and output to calculate the Y-parameters.

[Y]=

$$\begin{vmatrix} Y_1 & 0 & -Y_1 & 0 & 0 & 0 & 0 \\ 0 & Y_3 & 0 & -Y_3 & 0 & 0 & 0 \\ -Y_1 & 0 & Y_1+Y_6+Y_9 & 0 & 0 & -Y_6 & -Y_9 \\ 0 & -Y_3 & & Y_2+Y_3+Y_{10}+Y_5 & -Y_5-g_m & -Y_{10} & -Y_2+g_m \\ 0 & 0 & 0 & -Y_5 & Y_7+g_m+Y_5+Y_4 & -Y_7 & 0 \\ 0 & 0 & -Y_6 & -Y_{10} & -Y_7 & Y_6+Y_7+Y_{10}+Y_8 & 0 \\ 0 & 0 & -Y_9 & -Y_2 & -Y_4 & 0 & Y_9+Y_4+Y_2 \end{vmatrix}$$

(3.17)

[A] matrix shown below is the noise matrix for SGFET in Common Source Configuration. Depending on the noise contribution at each node in the circuit, the noise matrix for each of the circuits will be different. Thus for CS, CD and CG configurations, noise matrices are differ thus giving different noise characteristics. Noise matrix is also used for forming [B] and [D] matrices which are then used in formulation of noise parameters.

$$[A] = \begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & -1 \end{vmatrix} \quad (3.18)$$

3.4.2 Common Drain Configuration in SGFET

The small signal model and network graph for Common Drain Configuration of SGFET is as shown in Fig.3-5 and Fig.3-6.In common drain configuration, gate thermal noise is at the input and source thermal noise is at the output. This configuration acts as a source follower, thus given a voltage gain of one.

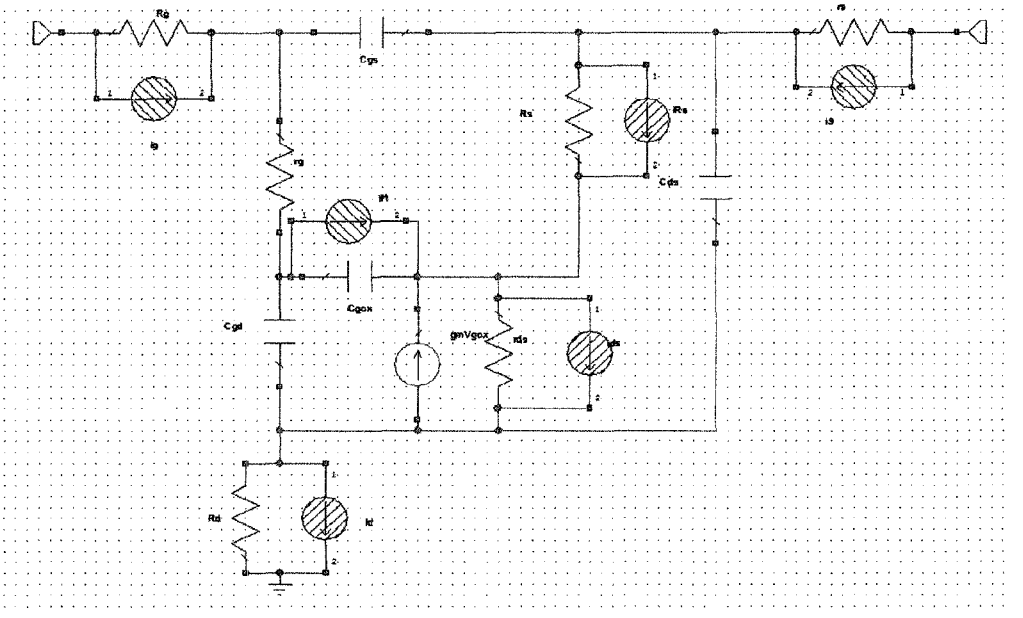

Fig. 3-5 Noise Model in Common Drain Configuration for SGFET

Fig. 3-6 shows the network graph for common drain configuration. This graph is derived from Fig. 3-5. The nodal equations for each of the nodes are written using KCL and then the admittance and noise matrices are formed. This network has seven nodes and hence there are seven KCL equations. These equations include all the noise sources and the admittance in the circuit.

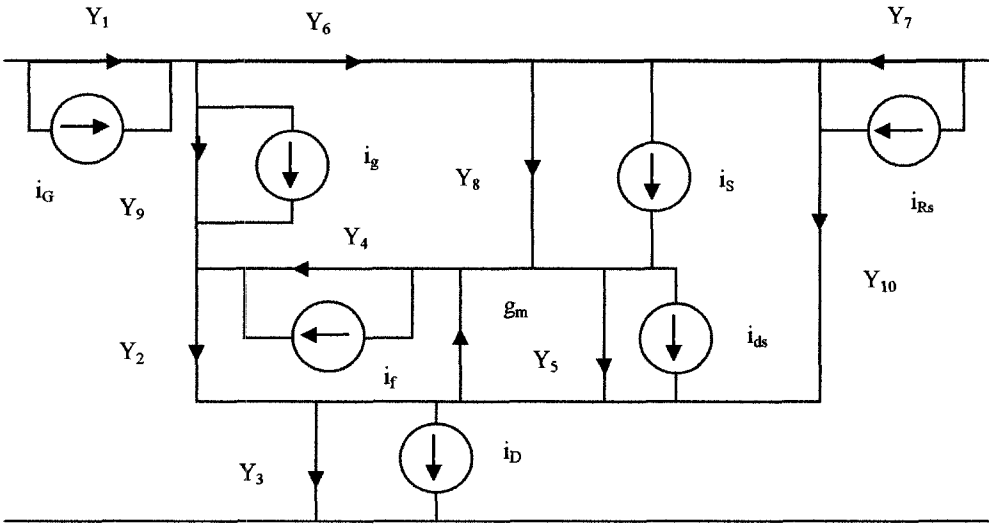

Fig. 3-6 Network Graph in Common Drain Configuration of SGFET

For CD configuration, the [Y], [A] matrices are given by the following equations. [Y] matrix is formed from the KCL equations written from the network graph in Fig. 3-6. Since the configuration has changed from CS to CD, the admittance matrix is different, giving different Y-parameters. This matrix is also reduced using direct matrix analysis method discussed in Chapter 1 to a 2X2 matrix. Thus the 2-port Y-parameters are obtained for the circuit.

[Y] =

$$\begin{vmatrix} Y_{10} & 0 & -Y_{10} & 0 & 0 & 0 & 0 \\ 0 & Y_3 & & -Y_3 & 0 & 0 & 0 \\ -Y_1 & 0 & Y_{10}+Y7+Y4+Y_5+g_m & -Y_5 & -Y_4-g_m & 0 & 0 \\ & -Y3 & -Y5-gm & Y8+Y3+Y2+Y5 & -Y2+gm & -Y8 & 0 \\ 0 & 0 & -Y4 & -Y_2 & Y_6+Y_2+Y_1+Y_4 & 0 & 0 \\ 0 & 0 & 0 & -Y_8 & & & Y_9+Y_8 \\ 0 & 0 & -Y_9 & -Y_2 & -Y_4 & 0 & Y_9+Y_4+Y_2 \end{vmatrix} \quad (3.19)$$

[A] matrix shown below is a 7X7 matrix and represents all the noise sources in the common drain configuration of SGFET. This matrix is reduced to 2X7 matrix and not 2X2 as is the case with [Y] matrix. This is because there are seven noise sources in the circuit and hence they should not be eliminated if the complete circuit needs to be characterized. Noise matrix being accurate is a critical part of noise parameter extraction of any device. If any of the noise sources is ignored, the model may predict a lower noise figure.

$$[A] = \begin{vmatrix} 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{vmatrix} \quad (3.20)$$

3.4.3 Common Gate Configuration

Fig. 3-7 shows the noise model for SGFET in common gate configuration. In this case, the input noise is source thermal noise, whereas the output noise is drain thermal noise. This configuration gives a gain similar to that of common source configuration and is usually used in combination with common source configuration to form a cascode topology.

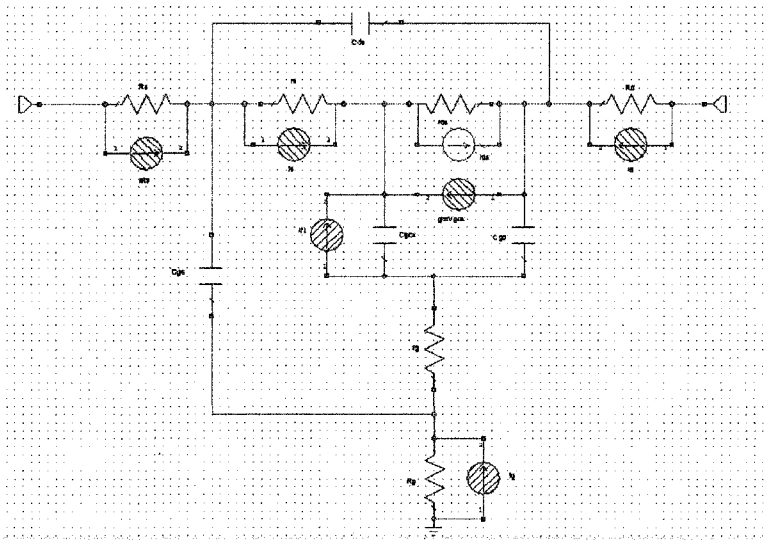

Fig. 3-7 Noise Model in Common Gate Configuration for SGFET

Fig. 3-8 shown below represents the network graph for common gate configuration. Similar to analysis done for common source and common drain configurations, nodal equations are written for this circuit and then admittance and noise matrices are formed. Network graph is drawn to make the nodal analysis simpler. This method is advantageous in case complex circuits like noise model of LNA with two or more stages and a Mixer. In such a case, if the network graph is derived and then nodal equations are written, there are fewer chances of errors.

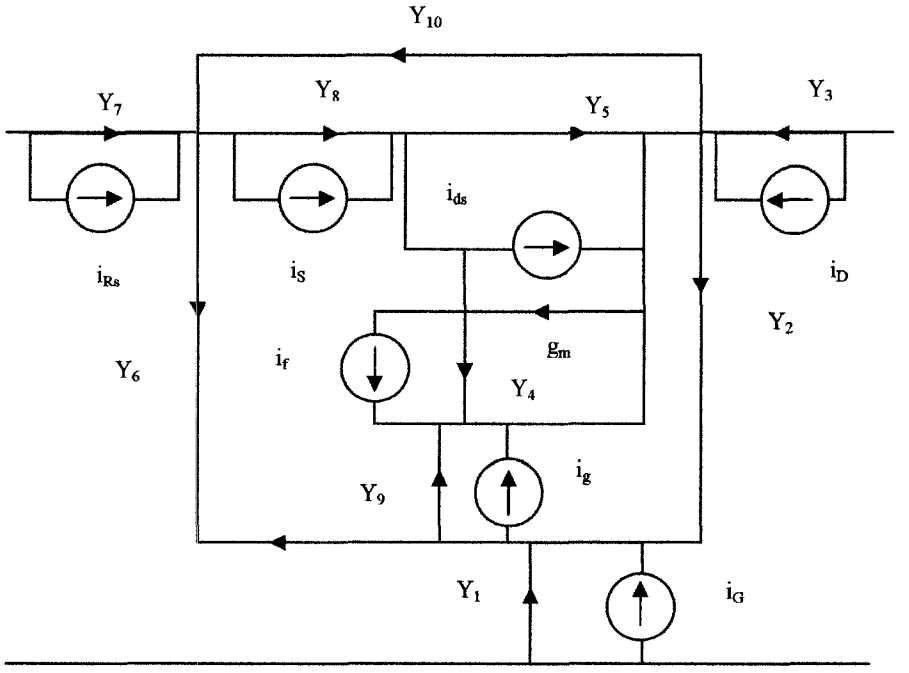

Fig. 3-8 Network graph for Common Gate Configuration

Equation below shows the admittance matrix for common gate configuration. As can be seen this is entirely different from CD and CS configurations. This thus shows that the noise characteristics in each of the configurations will be varying. Chapter 4 will discuss the noise parameters of all these configurations in detail.

[Y] =

$$\begin{vmatrix} Y_7 & 0 & -Y_7 & 0 & 0 & 0 & 0 \\ 0 & Y_3 & 0 & -Y_3 & 0 & 0 & 0 \\ -Y_7 & 0 & Y_{10}+Y_7+Y_6+Y_8 & -Y_{10} & 0 & -Y_6 & -Y_8 \\ 0 & -Y_3 & -Y_{10} & Y_3+Y_{10}+Y_5+Y_2 & -Y_2+g_m & 0 & -g_m-Y_5 \\ 0 & 0 & 0 & -Y_2 & Y_9+Y_2+Y_4 & -Y9 & -Y4 \\ 0 & 0 & -Y6 & 0 & -Y_9 & Y_9+Y_6+Y_1 & Y_9+Y_8 \\ 0 & 0 & -Y_8 & -Y_5 & -g_m-Y_4 & 0 & Y_8+Y_4+Y_5+g_m \end{vmatrix}$$

(3.21)

[A] matrix shown below is a 7X7 matrix and represents all the noise sources in the common drain configuration of SGFET. This matrix is reduced to 2X7 matrix and not 2X2 as is the case with [Y] matrix. Noise matrix is different for all three configurations and characterizes the noise performance of the device.

$$[A] = \begin{vmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & -1 & 0 & 0 & 0 \end{vmatrix} \quad (3.22)$$

3.4 Noise Sources in SGFET

The active and passive components in a circuit generate various types of noise during operations which are sometimes bias dependant. SGFET is modeled with resistive, capacitive and active components as shown in the figure. Thus different noise sources exist in SGFET with their power spectral densities. The noise sources include:

1) Terminal resistance producing thermal noise at the gate
2) Terminal resistance producing thermal noise at the drain
3) Terminal resistance producing thermal noise at the source
4) Thermal noise and flicker noise in the channel
5) Induced gate noise due to oxide capacitance Cgox

3.5 Summary

The parasitic model of SGFET was also discussed in this chapter. This chapter presented the nodal analysis of SGFET using Direct Matrix Analysis. The impedance and noise matrix were derived for all three configurations of SGFET.

Chapter 4 will show the simulated results for noise parameters of SGFET.

CHAPTER 4

SIMULATION RESULTS

4.1 Noise Characteristics for SGFET and MOSFET

The noise characteristics of SGFET and MOSFET were analyzed using the equations discussed in Chapter 1.As was shown in Chapter 3, the small signal model was fist formed and then a network graph was derived. Nodal equations were then written for each of the network graphs in all three different configurations.

Admittance and Noise matrices were formed based on these nodal equations. The equations (1.3)-(1.6) and (1.8) - (1.11) were used for calculating the noise parameters and then the noise figure.

Fig. 4-1 shows the gain of SGFET and scaled MOSFET in CS configuration. This represents a small signal gain over the frequency range 10Hz – 1THz. The gain of SGFET is 7.5dB till 100GHz and then it drops to 0dB at 1THz. MOSFET shows a higher gain of 13dB as compared to MOSFET which is due to large value of r_{ds} in MOSFET than SGFET. The gain characteristics are similar to SGFET and the gain drops at 1THz to 6dB.

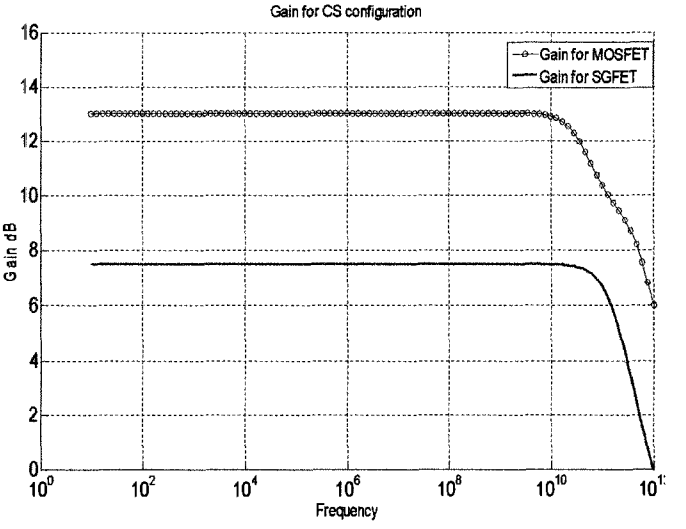

Fig. 4-1 Gain of SGFET and Scaled MOSFET in Common Source Configuration

Fig. 4-2 shows the equivalent noise resistance for SGFET and MOSFET in the band of 10Hz-1THz. The value of Rn is high at low frequencies and then decreases at high frequencies. It can be seen that the value of Rn in both cases are very close.

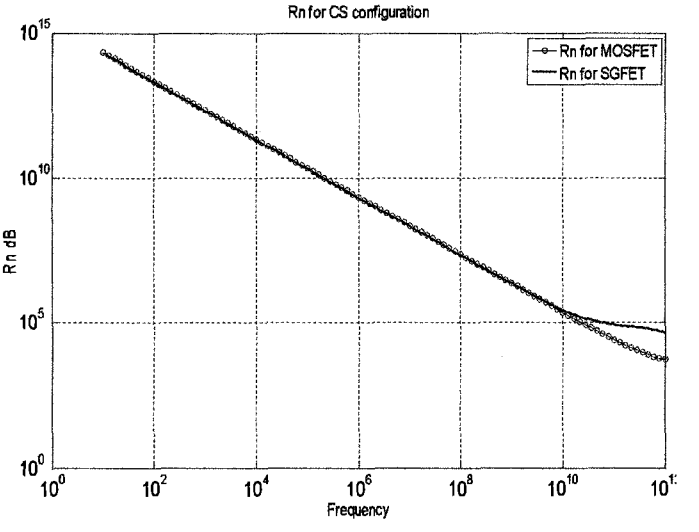

Fig. 4-2 Equivalent Noise Resistance of SGFET and scaled MOSFET in Common Source Configuration

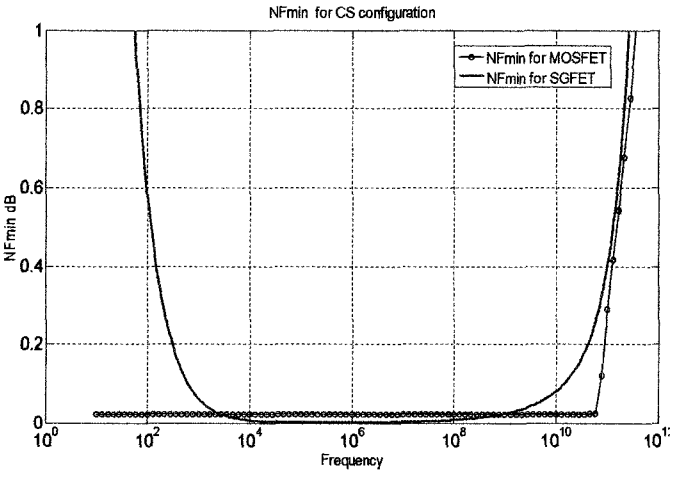

Fig. 4-3 Minimum Noise Figure of SGFET and Scaled MOSFET in Common Source Configuration

Fig. 4-3 shows the Minimum Noise Figure plot for SGFET and MOSFET. The calculation was done using equations discussed in Chapter1.It can be observed that the noise figure is high at low frequencies for SGFET and reaches a minimum value and again increases at high frequencies. This effect is due to the contribution of flicker noise at low frequencies and increase in gate induced noise at high frequencies. At the center frequencies, the flicker is very low and total noise is addition thermal noise and induced gate noise, giving a minimum noise figure. The devices can thus be used in the band where noise figure reaches a minimum value.

In case of MOSFET, the noise figure is constant over a certain band and then increases at high frequencies. This is because flicker noise is not very dominant as compared to other noise sources at low frequencies. At high frequencies, flicker noise is very low and induced gate noise is dominant, explaining the increase in noise figure.

Fig. 4-4 shows the gain of SGFET and MOSFET in CD configuration. This represents a small signal gain over the frequency range 10Hz – 1THz. Since this is a source follower topology, the voltage gain is around 1 which is expected. As the frequency increase the gain drops in both cases.

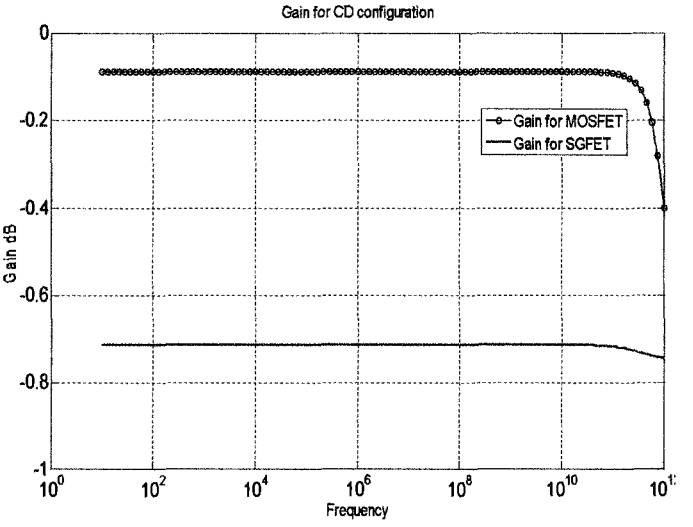

Fig. 4-4 Gain of SGFET and Scaled MOSFET in Common Drain Configuration

Figures 4-5 shows the equivalent noise resistance for SGFET and MOSFET in CD configuration. The values are very close to devices in CS configuration but the slope is different due to different impedance and noise matrices in both configurations.

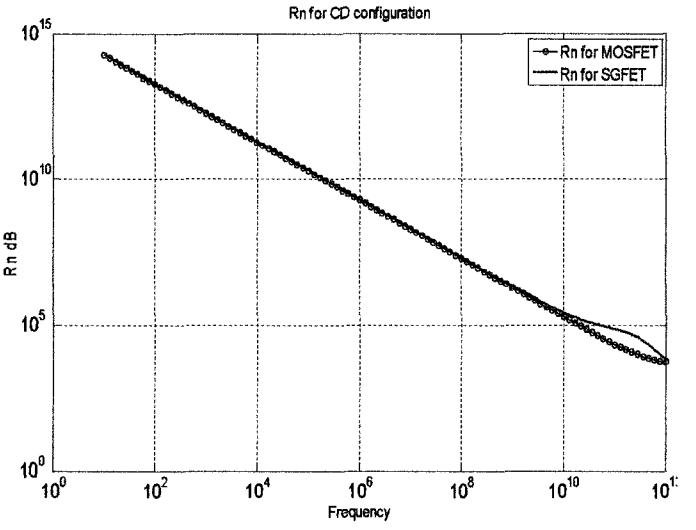

Fig. 4-5 Equivalent Noise Resistance of SGFET and Scaled MOSFET in Common Drain Configuration

It can be clearly seen from the above noise figure graphs that the behavior of two devices is opposite at low and high frequency ends. In case of SGFET since Flicker noise is dominant at low frequencies, the noise figure is high. For MOSFET, induced gate noise is dominant at high frequencies and hence noise figure is high. At the center of the frequency band, flicker noise is not that dominant and noise is summation of thermal and gate induced noise.

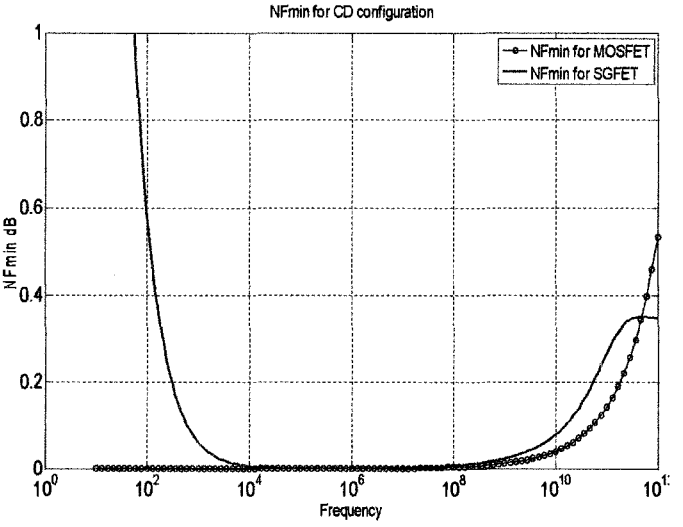

Fig. 4-6 Minimum Noise Figure of SGFET and Scaled MOSFET in Common Drain Configuration

In Fig. 4-7 the gain of SGFET and MOSFET in CG configuration is shown. The gain is little higher as compared to CS configuration, but the behaviour is similar and it and rolls off at high frequencies.

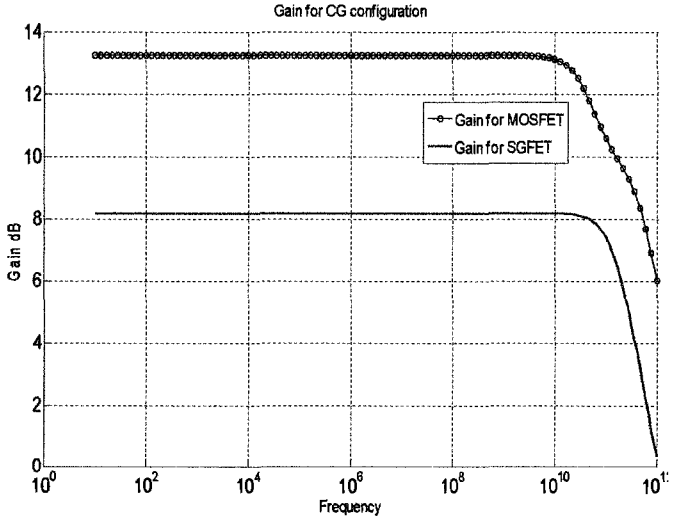

Fig. 4-7 Gain of SGFET and Scaled MOSFET in Common Gate Configuration

The above Figure 4-8 shows the equivalent noise resistance for SGFET and MOSFET in CG configurations. The noise resistance is slightly less compared to CD and CS configurations. The variation is due to the difference in impedance and noise matrices for all the three configurations.

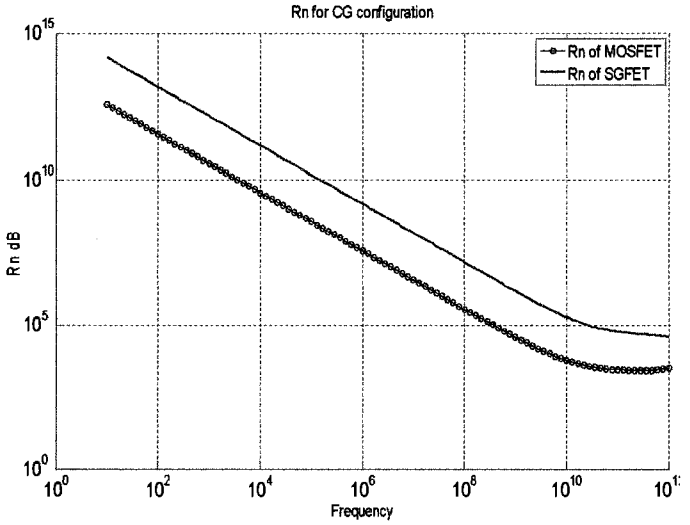

Fig. 4-8 Equivalent Noise Resistance of SGFET and Scaled MOSFET in Common Gate Configuration

Fig. 4-9 shows the noise figure plots for SGFET and MOSFET in CG configuration.In this case the bevaviour is same for both the devices. This is becasuse in CG configuration, though the noise sources values remain the same, they cancel each other at low frequenicies. Hence it does not show a high noise figure at low frequenicies. For CG configuration , noise figure is higher since induced gate noise is dominant.

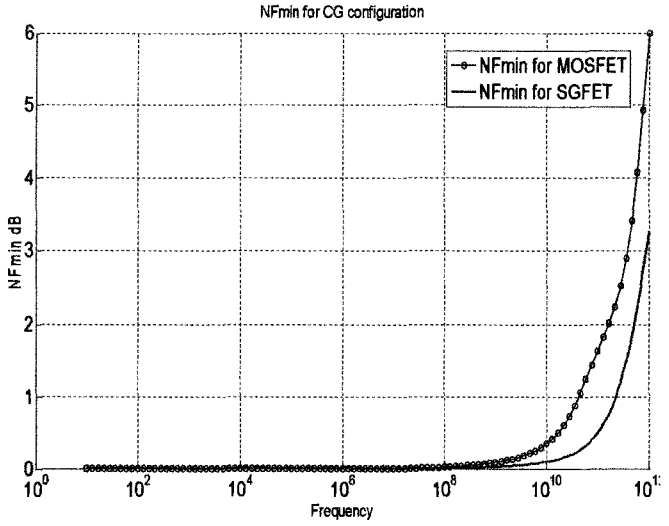

Fig. 4-9 Minimum Noise Figure of SGFET and Scaled MOSFET in Common Gate Configuration

4.2 Noise Current Sources in SGFET and MOSFET

The following current sources were investigated in SGFET:

1) Gate Induced Noise
2) Thermal Noise for Drain, Source and Gate
3) Channel Noise
4) Flicker Noise
5) Bulk Thermal noise in case of MOSFET
6) Intrinsic Source thermal noise in case of SGFET

Fig. 4-10 shows the induced gate noise for SGFET and MOSFET.Since this noise is directly proportional to frequency, it increases with increase in frquency which is expected.

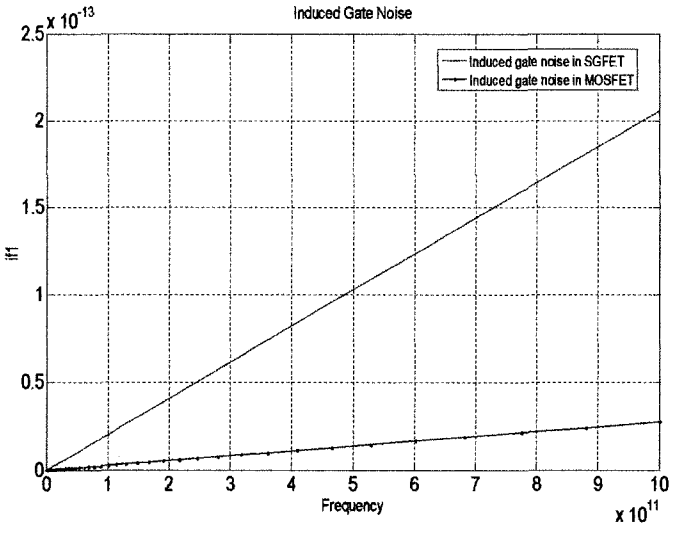

Fig. 4-10 Gate induced noise in SGFET and Scaled MOSFET

Fig. 4-11 shows the channel noise in SGFET. This noise is constant over the whole frequency band. Channel noise is due to fluctuations in the channel of the device and is correlated with induced gate noise at high frequencies. Since induced gate noise increases with increase in frequeny, the correlation also is greater at higher frequencies.

The above figure shows channel noise for MOSFET is higher as compared to SGFET. This noise is constant with frequency and correlated with induced gate noise due to the gate oxide capacitance.

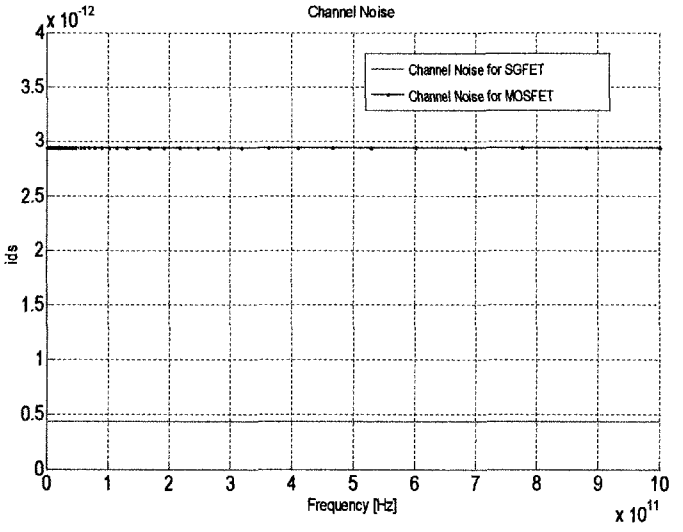

Fig. 4-11 Channel Noise in SGFET and Scaled MOSFET

This figure shows the flicker noise characteristics of SGFET.Flicker noise is inversely proportional to square of frequency and hence decrease with increase in frequency. This noise is dominant at low frequencies and reaches to a very low values at high frequency. The value at 10Hz for flicker noise is very high and then approaches zero at high frequency.

Fig. 4-12 shows the flicker noise in MOSFET which is higher as compared to SGFET. This is expected since the structures of SGFET and MOSFET are completely different and SGFET has an advantage of less electrons being trapped at Si-SiO_2 interface.

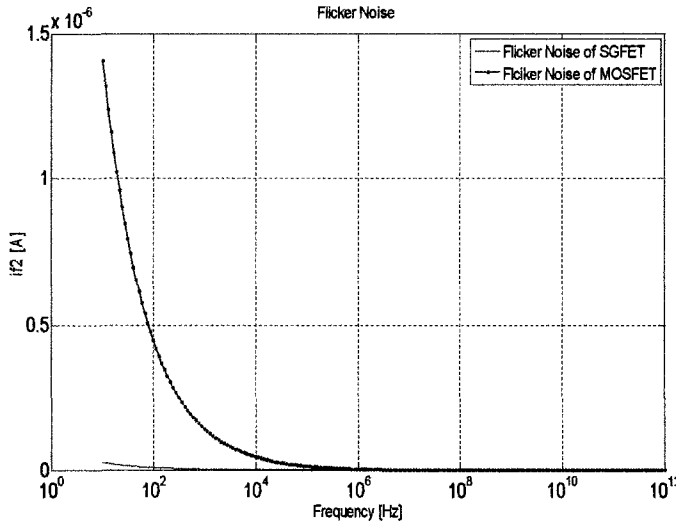

Fig. 4-12 Flicker Noise in SGFET and Scaled MOSFET

Figures 4-13 shows the gate thermal noise for SGFET and MOSFET, respectively. This noise is independent of frequency which explians the flat behaviour in the whole band. Gate thermal noise depends on the value of gate resistance and the temperature. In this case, the simulations were done at room temperature. As temperature increases the thermal noise increases. MOSFET exhibits lower gate thermal noise since it has a low value of gate resistance.

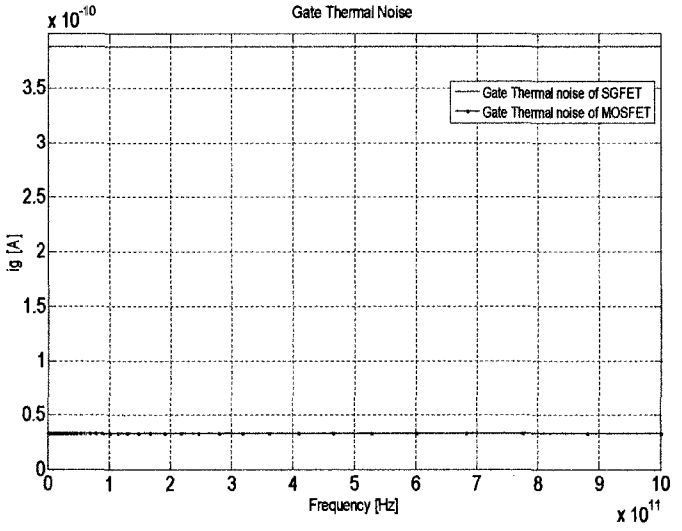

Fig. 4-13 Gate Thermal Noise in SGFET and Scaled MOSFET

Fig. 4-14 shows the simulated results for drain thermal noise of SGFET and MOSFET. This noise also depends on the drain resistance of the device and increases with increase in temperature. MOSFET shows a lower drain thermal noise due to its low value of drain resistance.

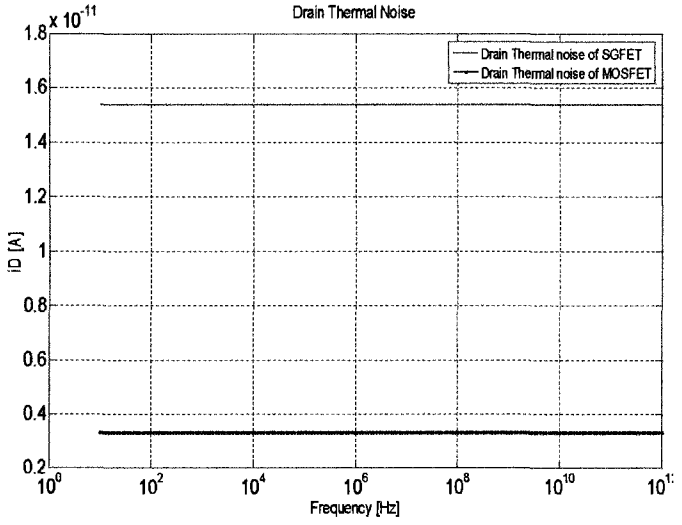

Fig. 4-14 Drain Thermal Noise in SGFET and Scaled MOSFET

The figure below shows the source thermal noise for SGFET and MOSFET caused due to the source resistance of both devices.MOSFET has lower source resistance compared to SGFET, explaining lower value of thermal noise than SGFET.

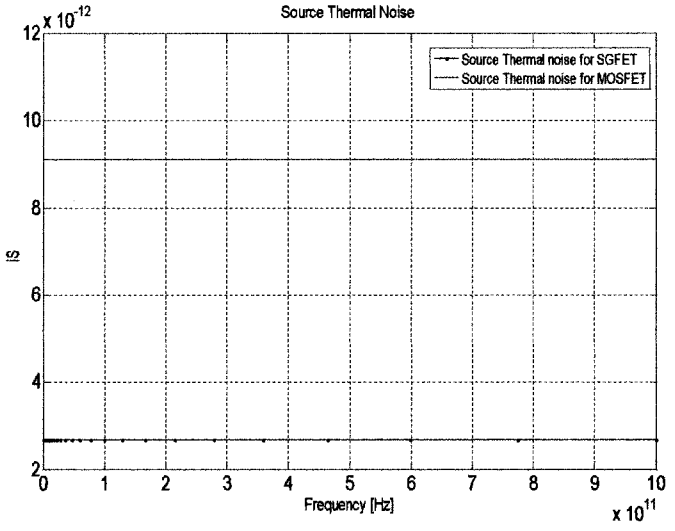

Fig. 4-15 Source Thermal Noise in SGFET and Scaled MOSFET

The Fig. 4-16 shows the thermal noise due to intrinsic source resistance of SGFET.This resistance is absent in case of MOSFET since an intrinsic transistor is not formed as is the case with SGFET.

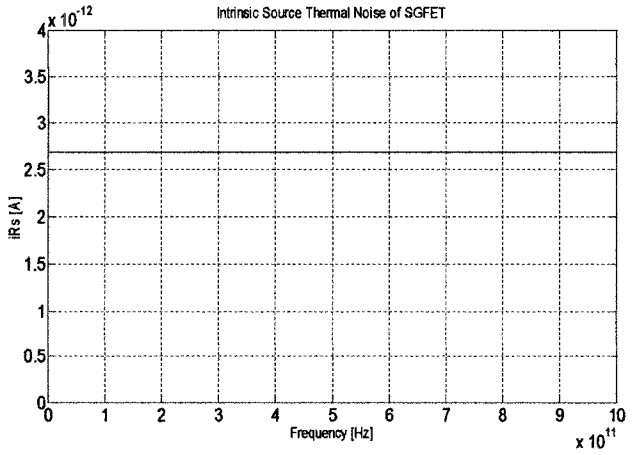

Fig. 4-16 Intrinsic source resistance Thermal Noise in SGFET and Scaled MOSFET

Fig. 4-17 shows the thermal noise contributed by the bulk resistance of MOSFET. This resistance is absent in SGFET since it has a different structure than MOSFET and does not have a bulk terminal. This noise also increases with increase in device temperature and bulk resistance.

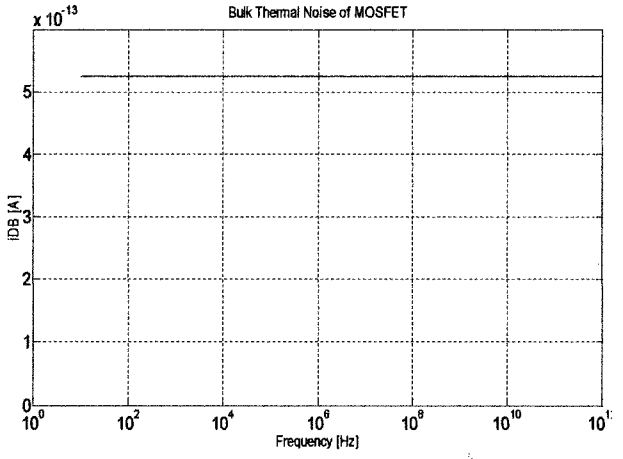

Fig. 4-17 Bulk Thermal Noise in MOSFET and Scaled MOSFET

4.3 Summary

The simulation results for noise parameters and noise sources of SGFET and MOSFET were shown in this chapter. It was observed that the noise characteristics of the device change considerably with changes in the configurations. SGFET shows less thermal noise compared to MOSFET while the flicker noise is higher compared to MOSFET. This can be attributed to the fact that the fitting factors are less in MOSFET than SGFET. In Chapter 5, the application of SGFET as a LNA has been presented.

CHAPTER 5

APPLICATIONS OF SGFET

5.1 LNA Design

Due to the low noise figure of this device over a broad frequency range, this is highly suitable for RF Applications to design a Low Noise Amplifier. Since the maximum operating frequency is 100GHz, it is well suited for WLAN, WiMAX as well as UWB, Microwave applications. This device can be used in Ka bands and other high frequency applications.

A design of cascode LNA has been presented in this paper. It can be seen from the graphs that SGFET can give a broadband performance with a very low Noise Figure over the whole band, making it ideal for Low Noise Applications. SGFET can be used in design of LNA's, Mixers and Local Oscillators since it has a very low noise figure over a very broadband. A LNA has been presented in this thesis.

5.2 Topology

The topology used for design of LNA was Cascode. Some advantages of cascode topology are [14]:

1) High reverse isolation compared to the conventional LNA
2) Higher power gain
3) Low Noise Figure

The simulations were done using Spectre RF CAD Tool in Cadence. A source degeneration inductor is used to get low noise figure. The input and output matching are such that they cancel the reactive part and then match impedance to 50 Ohms.

5.2.1 Frequency Specifications

The specifications were chosen for the LNA so as to show the performance of SGFET at very high frequencies. The frequency band used for design is used extensively in radio astronomy and point to multipoint communications. This LNA is a single stage cascode, but can be modified to two a stage LNA if the requirement is of higher gain.

The specifications of the LNA designed are as follows:

Table 5-1 Specifications for LNA Design

Parameters	Min	Typical	Max
Frequency	48GHz	50.2GHz	52GHz
Gain	19 dB	20dB	21.5dB
Noise Figure	.9dB	1.1dB	1.2dB
OIP 3	-10dBm	5dBm	8dBm
P1 dB out		-12dBm	

5.2.2 Electrical Characteristics

The table shows the DC characteristics of the LNA. Since the device is in nanometer range, the dc supply voltage need is also less compared to other devices. Hence the device was biased at 1V.

Table 5-2 Electrical Characteristics for LNA

Parameter	Values
DC Supply	1V
Quiescent Current	1.88mA
DC Power Dissipation	1.88 mW

5.3 Design Procedure

Since the noise analysis was already done for SGFET, the first step for LNA design was to see the noise figure characteristics over the gate voltage range. The bias point was chosen to have a trade off between gain and noise figure. Initially the input and output impedance of the SGFET were calculated without any matching elements. A source degeneration inductance of 500pH is added so as to satisfy the following equation.

$$R_{in} = \frac{L_s . g_m}{C_{gs}} \qquad (5.1)$$

Ls is thus selected for simultaneous matching of gain and noise.

The impedance obtained was reactive which was cancelled by the series capacitors at the input and output. Then a simple LC matching was used to transform the impedance to 50 ohms. Thus there was a real part which had to be matched to 50 Ohms. This thus acts as a down- converting impedance matching network at input and up - converting impedance matching at the output. Smith Chart was used extensively to optimize the calculated results.

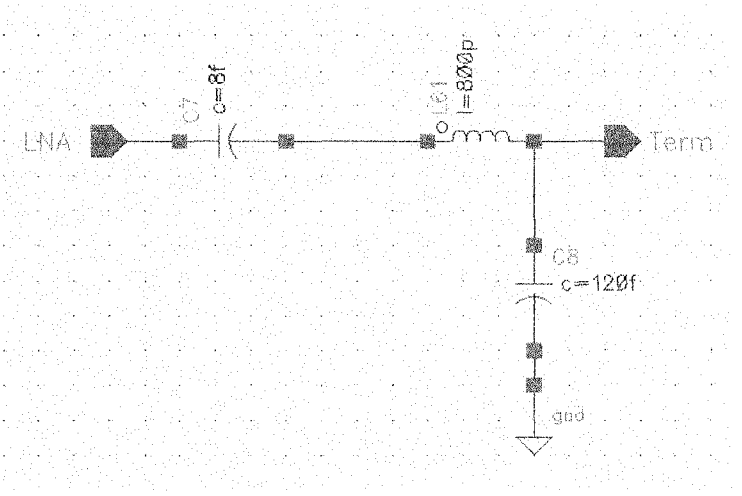

Fig. 5.1 Input Matching Network for LNA

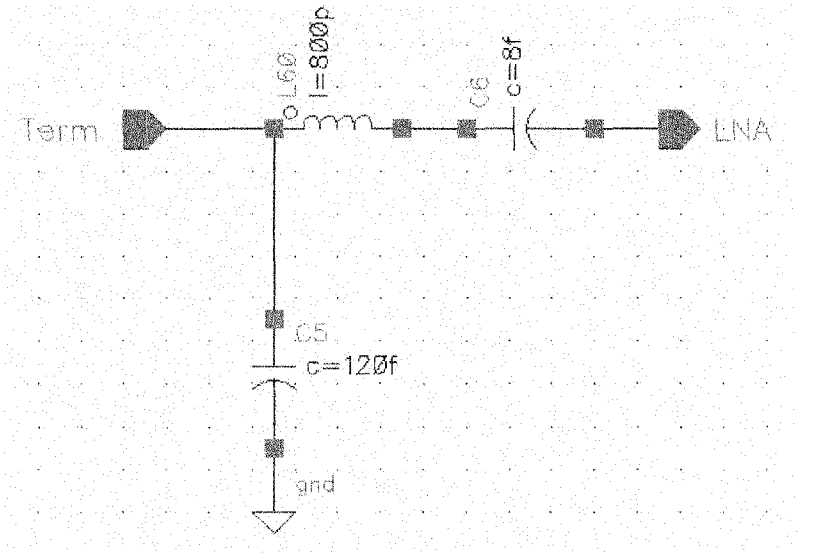

Fig. 5.2 Output Matching Network for LNA

The addition of source degeneration has the following advantages [14]:

1) It gives good input matching without adding thermal noise
2) Degeneration also improves the linearity by forming a negative series-series feedback
3) It improves the noise figure of LNA

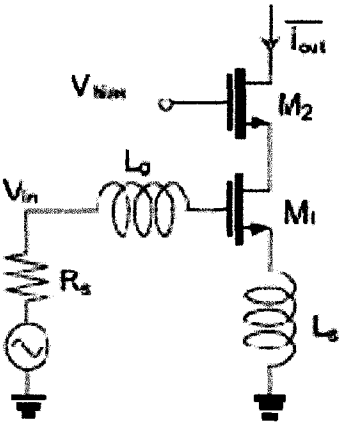

Fig. 5.3 Typical Cascode LNA with Source Degeneration

5.4 Stability Considerations in LNA

Stability is an important consideration for amplifier design, especially at higher frequencies. The most dominant node which is prone to oscillation at high frequencies is the gate of the cascode transistor. The input impedance of a capacitively degenerated device has a negative real part, and hence an inductance at the gate of cascode can form a Colpitts oscillator.

Thus to improve the stability of the cascode amplifier, a resistor was added to the gate of cascode to prevent the oscillations. A stabilizing resistor of value Rstab = 12Ω was added to the gate of the cascode transistor of LNA. The value of this resistor cannot be selected arbitrarily large, as it degrades the noise figure and reduces the efficiency of the bypass capacitor [14], [15].

Following Analysis were done on the LNA:

1) DC Analysis for dc current and dc power dissipation
2) S-Parameter Analysis for gain and noise figure

3) Harmonic Balance Analysis for output power

4) Two Tone Analysis for characterizing intermodulation distortion effects and linearity

Tables 5-3 and 5-4 show the components used for design of LNA. The list of all elements in the circuit along with their values is given. SGFET devices were cascaded to give a higher gain.

Table 5-3 Active Components in LNA circuit

Component	Multiplier	W	L	Description
M1	400	12.54nm	10nm	SGFET Device
M2	400	12.54nm	10nm	SGFET Device

Table 5-4 Passive Components in LNA circuit

Component	Value	Description
L1,L2	800pH	Input and Output series Matching elements
C1,C2	120fF	Input and Output shunt Matching elements
C3,C4	8fF	Input and Output blocking capacitors
Ls	500pH	Source Degeneration
R1,R2	12 Ohm	Stability resistors
Lb1,Lb2	500pH	Biasing Inductors for gate and drain

The cascode amplifier schematic is as shown below. A resistor was added at the gate of cascode to improve the stability. The stability considerations have been discussed in section 5.4.

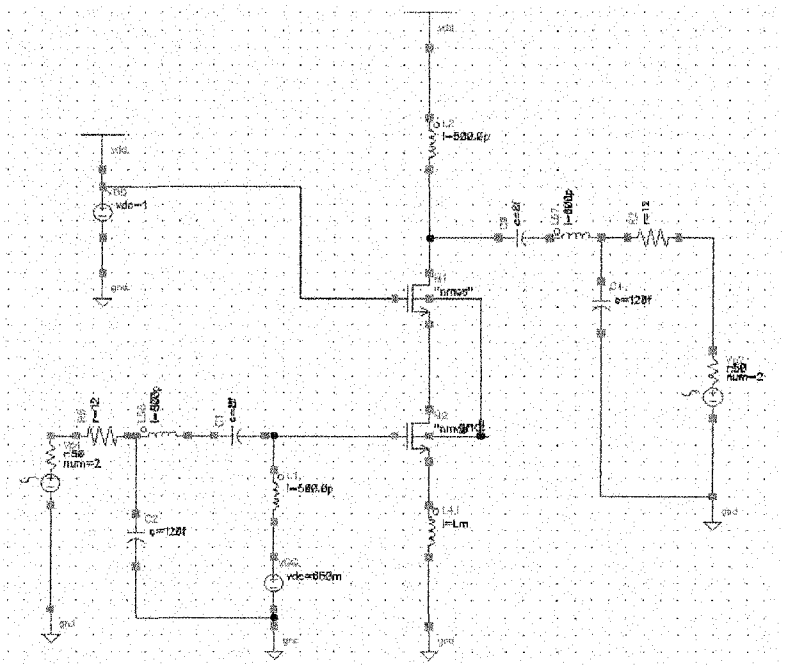

Fig. 5-4 Cascode Low Noise Amplifier Schematic

Fig. 5-5 shows the gain of amplifier. The maximum gain obtained is 20dB and then it rolls off to 19.2dB. The gain can be improved if one more stage is added to the existing design. Presently the LNA is a single stage cascode topology.

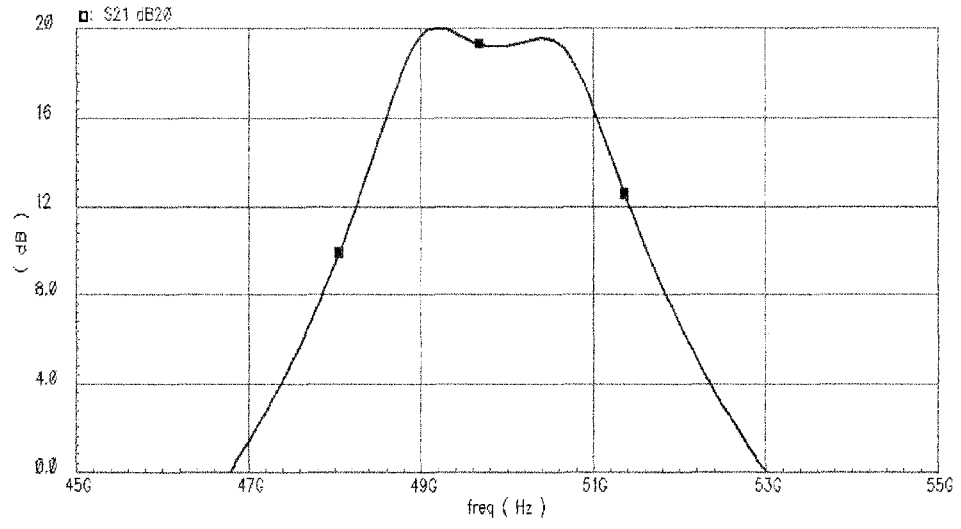

Fig. 5-5 Simulated Gain of LNA in Cadence

Fig. 5-6 shows the input and output return loss for LNA. It can be seen that in the band of operation S11 and S22 are both below 10dB which shows that the amplifier is matched well. S11 goes to a max (Jamal Deen)imum of -20dB while S22 goes to -25dB.

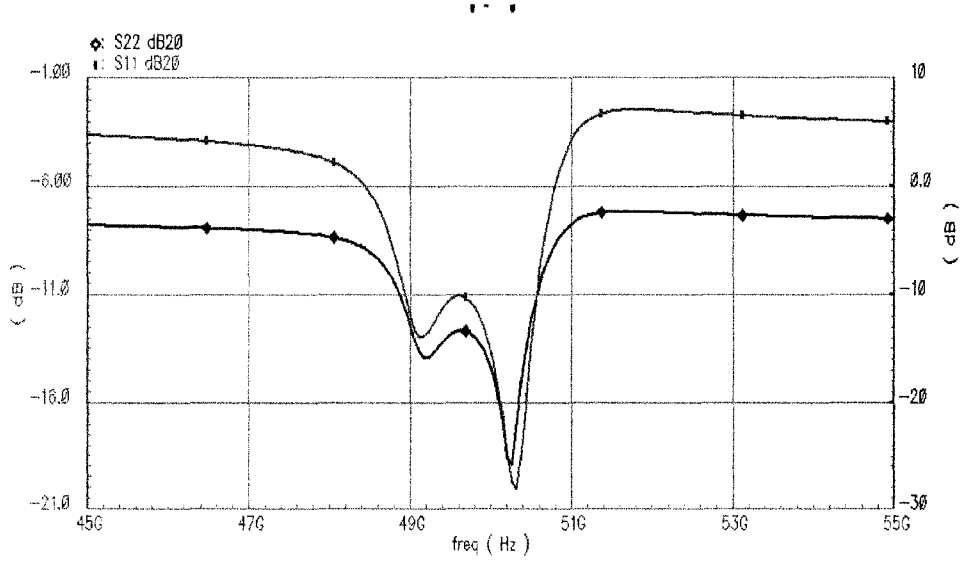

Fig. 5-6 Simulated Input and Output Return Loss of LNA

The figure below shows the reverse isolation of the amplifier. It is below 20dB in the band of interest.

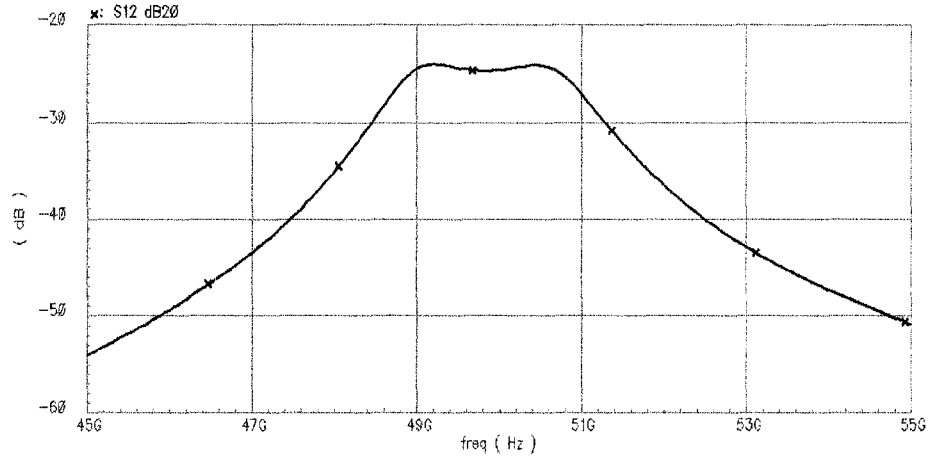

Fig. 5-7 Simulated Reverse isolation of LNA

Fig. 5-8 shows the noise figure of the amplifier. It is observed that noise figure is good in the band for which the amplifier has been matched, whereas it is high in the frequencies outside the band. The noise figure obtained is 1.1 dB and goes to maximum of 1.2dB.

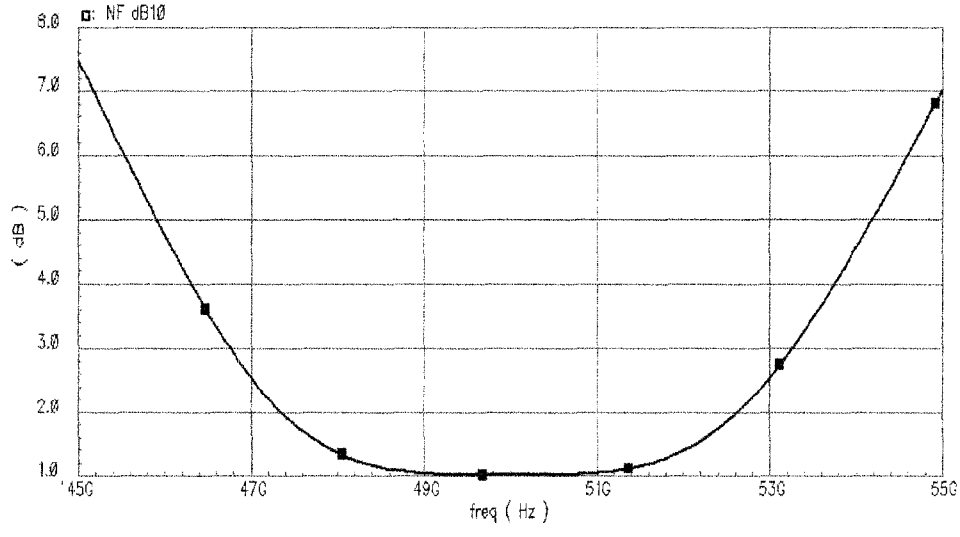

Fig. 5-8 Simulated Noise Figure of LNA

5.5 Applications of LNA

This LNA designed for 48-52 GHz can be used in applications like radio astronomy, Fixed Links both point to point and multipoint radio, Services Ancillary to Programming/Broadcasting, Fixed satellite service application and Satellite Feeder Links.

5.6 Summary

This chapter showed the application of SGFET as a Low Noise Amplifier. It is concluded from the results that SGFET can indeed be used in low noise applications over a broad range of frequencies. SGFET can thus be used as a device in circuits for WLAN, WiMAX to very high frequency circuits in military applications and radio astronomy. Due to low noise performance of SGFET, it can also be used to design mixers and oscillators.

CHAPTER 6

CONCLUSIONS

The noise parameter extraction was done for SGFET using a method called Direct Matrix Analysis. It was concluded that this method can be applied to any type of noise model or a small signal model and is very easy to implement even for very complex circuits. It can be implemented in MATLAB to make a generic program that can be used for any number of nodes and various circuit configurations. It is concluded that this method will prove very useful for noise characterization of a system such as LNA and Mixer if the small signal model is known and exact noise sources determined.

Various scaling theories were investigated and they showed that it is very important to consider all factors such as the supply voltage, threshold voltage, and doping levels while scaling or it may result in performance degradation. Thus constant field scaling was used, which scales down the voltages proportionately to the device dimensions. This scaling theory was applied to the bulk MOSFET, which gave similar results to the extrapolated values in MATLAB. The extrapolation was done after collecting data from various articles.

It was also observed that the flicker noise adds to the noise figure at very low frequencies and can be neglected at high frequency, which is consistent with the traditional flicker noise models. The noise figure for SGFET and MOSFET for all three configurations showed that flicker noise contributes to the noise at very low frequencies. It also cancels with the induced gate noise depending on the configuration used. The noise figure characteristic of the circuit is defined by the dominant noise source which is

usually flicker noise, channel noise and induced gate noises. But as temperature increases, thermal noise from all sources can become comparable to the flicker, channel, and induced gate noise, thus increasing the noise figure.

The comparison of SGFET with the scaled MOSFET demonstrated that SGFET exhibits lower flicker noise as compared to MOSFET. It also has lower channel noise but higher induced gate noise than MOSFET. In both cases, the noise figure reaches a minimum value in certain band which can be considered as an ideal band of operation.

The noise parameter extraction of SGFET shows that this device can be used as a low noise amplifier over a broad range of frequencies with very low noise over the whole band. The LNA application presented in the thesis shows that SGFET indeed can give a very low noise figure as compared to the planar MOSFET's. It is thus suitable for RF/microwave frequencies in implementation of mixers, oscillators, and amplifiers.

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