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Charge injection cancellation in analog-to-digital converters

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Charge injection cancellation in analog-to-digital converters

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San Jose State University, 1991

Charge Injection Cancellation

in

Analog-to-Digital Converters

A Thesis
Presented to
The Department of Electrical Engineering
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In Partial Fulfillment
of the Requirements for the Degree
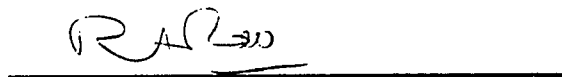**Master of Science**

By
Michael K. Mayes
May, 1991

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Abstract

Charge Injection Cancellation in Analog to Digital Converters

by Michael K. Mayes

Charge injection cancellation techniques using inverter delays to stagger the auto zero signals of multistage comparators exhibit varied offsets over supply, process, and temperature. Typically, these variations result from insufficient delay times between auto zero signals. By replacing the inverter delays with a programmable delay circuit, a better understanding of delay vs. offset is achieved. Further studies include the effect of forced voltage swing auto zero signals for reduction of offset sensitivity with respect to the supply voltage. Single ended and differential type comparators were designed using these techniques for charge injection cancellation. A working prototype was fabricated and tested for effectiveness.

The results find the offset of a comparator is a function of the delay time between auto zero signals and the output transient response of individual amplifier stages making up the comparator. The amplifier transient response is a function of charge injection induced step inputs. Further studies show charge injection errors are dominated by MOS mismatched channel charge in circuits using dummy device compensation.

An optimum delay between staggering auto zero signals is achieved by extending the delay beyond the worst case settling time of the amplifier. Constant voltage swings across MOS switches do not eliminate charge injection sensitivity to supply voltage due the effective threshold shift of the switches. However, as the swing is reduced, the transient response settles sooner due to reduced peak output voltages.

TABLE OF CONTENTS

1.0 Statement of Problem

Charge injection is a phenomena which effects the accuracy of analog integrated circuits. MOS analog circuits using transistor switching schemes to sample high precision voltage levels suffer degradations in performance due to charge injection [1].

In circuits using sample-data comparators, analog voltages are sampled and held on high impedance capacitive nodes using MOS switches. Once the input has been sampled, the MOS switch turns off in order to hold the signal. During switching, the MOS transistor couples charge into the high impedance storage node altering the acquired voltage. This voltage change causes an unwanted offset on the comparator input.

The sample-data comparator is used in analog integrated circuits requiring a sample-and-hold circuit and comparator. One such circuit is the analog-to-digital converter. Analog-to-digital converters use the sample-data comparator to acquire an input voltage and compare this voltage to an algorithmically generated reference voltages [2]. After acquisition, the analog voltage is converted to a digital code. Charge injection effects the offset of the analog-to-digital converter, leading to incorrect mapping between the analog and digital domains.

The comparator offset, due to charge injection, must be cancelled in order to eliminate excessive analog-to-digital converter offsets. This thesis examines charge injection cancellation techniques and how they fail to satisfactorily eliminate V_{os}. A new method of charge injection cancellation is proposed. The technique was confirmed by working silicon prototypes.

In prior experimentation culminating three years of work, two analog-to-digital converters were designed using known techniques of charge injection cancellation. The first, an 8-bit resolution ADC used a single ended, inverter type comparator design. The second used a differential type comparator for a 10-bit resolution ADC. In both cases, charge injection was the main contributor to offset problems delaying production of the parts. Three years of experimentations have led to several novel circuit techniques.

An analog test chip was designed containing single ended and differential comparators. The following circuit design techniques have been developed for charge injection cancellation:

> 1. Current controlled delays of staggered auto zero signals.
>
> 2. Forced voltage swing of auto zero signals.

1.1 Staggered Auto Zeroes

Since the gain of a single comparator is finite, typical ADC comparator designs use three stages of comparators to increase the overall gain (see figure 1.1). Each of the three stages requires a feedback switch to bias that individual stage. When T_1 is high, each
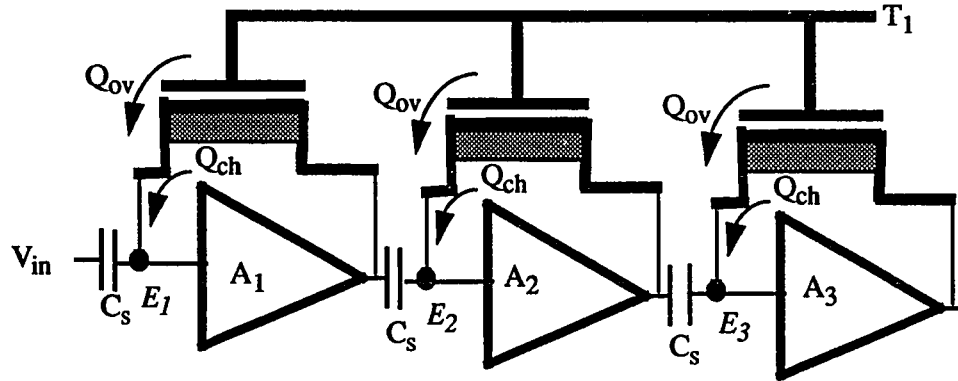
FIGURE 1.1   Three Stage Comparator

comparator is biased to its trip-point. Each stage is capacitively coupled with C_s in order to independently store the DC bias point of that stage while passing the AC signals. Once T_1 goes low, the comparator enters its high gain region of operation. For this comparator the overall gain is the product of the three individual gain stages

$$A_v = A_1 \times A_2 \times A_3 \qquad 1.1$$

A_v is typically 1000. On the falling edge of T_1, charge is injected into each of the three comparators high impedance input nodes. E_1, the first stage error voltage, contributes directly to the overall offset of the comparator. Since E_2 is isolated from the input by amplifier A_1, its contribution to the overall error is reduced by a factor of A_1. Similarly, the error voltage generated by the third feedback switch, E_3, is reduced by $A_1 \times A_2$. The overall error voltage as seen by the input to the comparator is

$$E_{in} = E_1 + \frac{E_2}{A_1} + \frac{E_3}{A_1 \times A_2} \qquad 1.2$$

For single stage gains greater than 1, the dominate error in E_{in} is E_1. Therefore, the charge injection of the first stage is the most significant contributor to offset voltage.

Since there are three stages of comparators, one known way to cancel the effect of the first stage error, E_1, is to delay turning off the feedback switch of the second stage until the first stage has settled to its charge injection altered trip point. If the second stage feedback switch is on while the first stage is settling, the error (E_1) generated by the first stage charge injection does not effect the output of the overall comparator.

One method of delaying or staggering the auto zero signals is to add several inverter delays between the gates of the feedback switches (see figure 1.2).
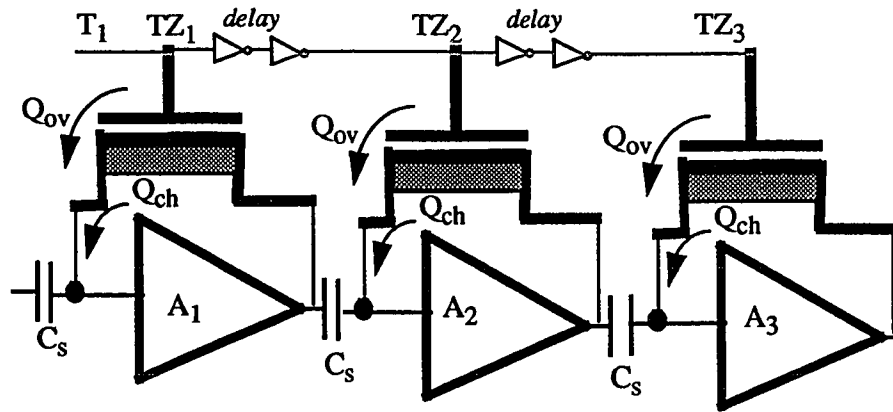
FIGURE 1.2 Staggered Auto Zero Signals

By adding two gate delays between TZ_1 and TZ_2 the second stage auto zero switch is on two gate delay times after charge injection has altered the first stage offset. Since the second stage is still forcing $V_{out}=V_{in}$, any error introduced by the first stage will not effect the bias point of the second stage.

When TZ_1 goes low, charge is injected into the input of amplifier A_1. This error voltage is amplified by A_1 and output to the input terminal of A_2. If TZ_2 is still "1" then the trip point of A_2 is not changed. If TZ_2 is "0" then the trip-point of A_2 is offset by the output of amplifier A_1. Too short a delay will not cancel the charge injection, while too long will reduce the maximum conversion time of the ADC. A typical design may use several mask sets to determine the optimum delay.

The problem with inverter delays is the limited control of their delay. To increase the delay, more inverters are required between auto zero signals. Rather than using inverters to delay the signals, a current programmable delay circuit can be used to externally control the delay. Delay vs. comparator offset can be determined with a precision delay circuit. The inverters would simply be replaced by delay blocks, see figure 1.3.
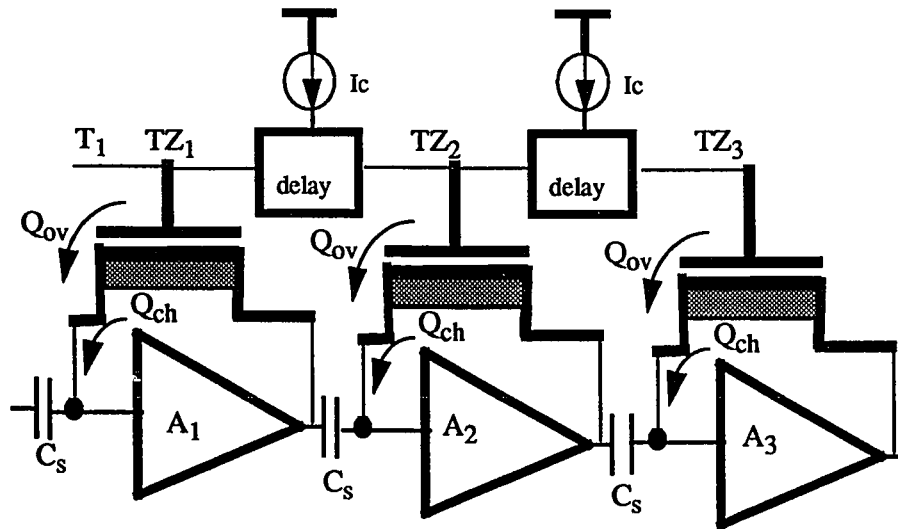
FIGURE 1.3 Programmable Delay Staggered Auto Zeroes

An external controllable current is used to adjust the delay between staggered auto ze-roes from 1ns to 100ns. In this case, the second stage feedback switch is turned off after the first stage switch. The time difference between successive auto zero switches turning off is externally controllable through I_c. An option also exists to short the auto zeroes to-gether for 0ns of delay.

1.2 Forced Voltage Swing of Auto Zero Signals

Not only does the offset change as a result of charge injection, but it also varies over supply voltage (V_{dd}). Most ADC's have a power supply rejection ratio (PSRR) specification. PSRR is defined as the offset variation as V_{dd} varies $\mp10\%$

$$4.5v \le V_{dd} \le 5.5v \qquad\qquad 1.3$$

The offset varies with V_{dd} because the signals driving the MOS feedback switches are swinging from V_{dd} to ground (figure 1.4), leading to variations in charge injection

$$Q_{inj} = Q_{ch} + V_{dd} \times C_{ov} \qquad\qquad 1.4$$

where Q_{ch} is channel charge injection and C_{ov} is the gate to source overlap capacitance of the MOS switch. These variations in charge injection lead to variations in comparator offset voltage

$$V_{os} = \frac{Q_{inj}}{C_s} \qquad\qquad 1.5$$

Since the trip point of comparators is typically designed to half supply

$$V_{trip} \approx \frac{V_{dd}}{2} \qquad\qquad 1.6$$

the minimum signal required to turn on the feedback switch is

$$V_{az} = V_{tn} + \frac{V_{dd}}{2} \qquad\qquad 1.7$$

where V_{tn} is the N-channel threshold voltage.

Instead of driving the feedback switches with an inverter swinging from $V_{dd} \mp10\%$ to 0v, The feedback switches are driven with a V_{dd} independent bias voltage.

$$V_{bias} \ge V_{tn} + \frac{V_{dd(max)}}{2} \qquad\qquad 1.8$$

In this case, ΔV across C_{ov} is fixed with respect to supply. As V_{dd} varies, V_{bias} remains constant, reducing offset variations over supply.

$$Q_{ov} = V_{bias} \times C_{ov} \Rightarrow CONSTANT \qquad\qquad 1.9$$
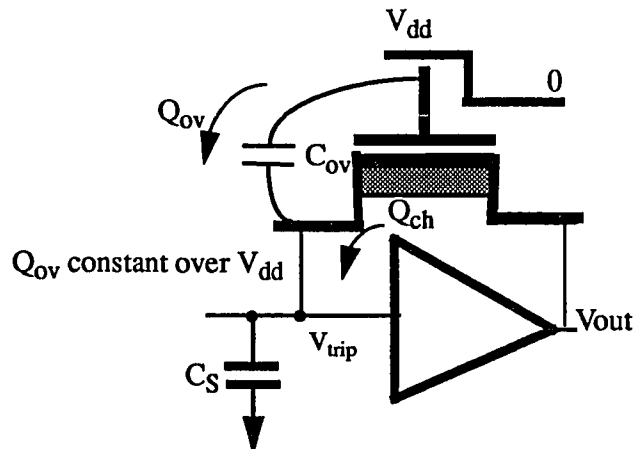
FIGURE 1.4 Constant Swing Auto Zero Signal

A typical specification for PSRR is 1/2 LSB. The first silicon from an 8-bit ADC with 2 inverter delays between each auto zero signal had a PSRR of 5 LSB. A fully differential 10-bit ADC had a PSRR of 10 LSB. These results were very discouraging; however, by changing the design several times the PSRR was significantly reduced. The proceeding circuits were developed to eliminate this problem without post adjustments of the mask set.

2.0 Background

2.1 Charge Injection

In precision analog circuits, such as analog-to-digital converters, MOS switches are used to sample voltage levels on capacitive storage nodes. The accuracy of this sampling is essential for proper analog processing of the acquired signal. Charge injection occurs when the MOS switch tied to the capacitive storage node is opened. As shown in figure 2.1, M_1 is on when $V_g=V_{dd}$. While M_1 is on, capacitor C_s is charged to V_{in}. At some time after C_s has charged to V_{in}, V_g is pulled low ($V_g=V_L$) forcing M_1 to turn off. Since M_1 is off, V_{in} can change without effecting the voltage stored on C_s. While V_g is changing from V_{dd} to V_L, charge injection causes the stored voltage across capacitor C_s to change. The charge injection is a combination of clock feed through and mobile charges in the channel [3].
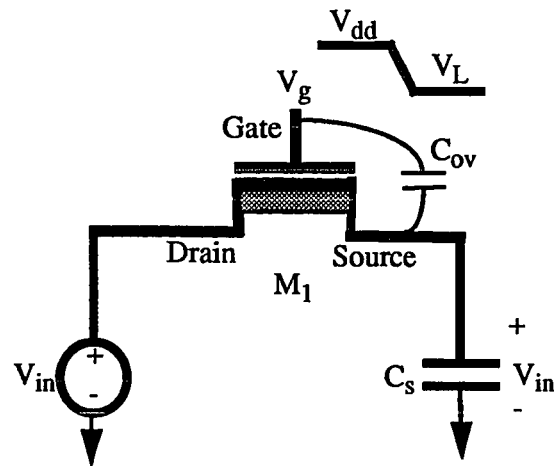
FIGURE 2.1 Simple Data Acquisition Circuit

Clock feed through is due to the overlap capacitance (C_{ov}) of the MOS switch. The overlap capacitance is due to the lateral diffusion (L_D) of the MOS transistor, see figure 2.2.
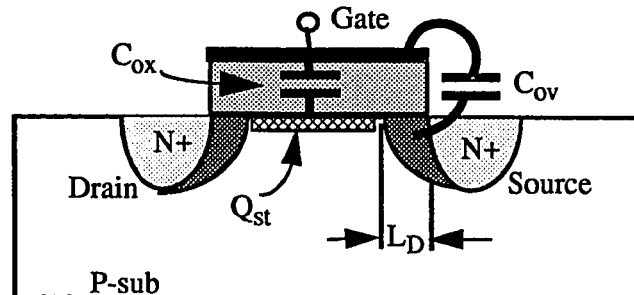
FIGURE 2.2 Overlap Capacitance of a MOS Switch

The overlap capacitance of an MOS device is

$$C_{ov} = C_{ox} \times W \times L_D \qquad\qquad 2.1$$

Where C_{ox} is the gate oxide capacitance per unit area, W is the transistor width and L_D is the lateral diffusion. Since the gate voltage is changing from V_{dd} to V_L during turn off, charge is coupled from the gate to the source through C_{ov} altering the voltage stored on C_s.

In order for an MOS switch to be conductive, an inversion layer of charge (Q_{st}) exists in the channel between the source and drain. When the MOS switch is turned off, this inversion layer collapses forcing the charge to exit into the source and drain [4]. A fractional part of this charge is injected into the source node adding to the clock feed through induced error on capacitor C_s.

When V_g is falling from V_{dd} to V_L, the MOS transistor goes through two regions of operation. These regions are shown in figure 2.3, and are defined by the following:

$$Region\ I\ V_{TE} < V_g < V_{dd} \qquad\qquad 2.2$$

$$Region\ II\ 0 < V_g < V_{TE} \qquad\qquad 2.3$$

where V_{TE} is the effective threshold of the MOS device including the source voltage (V_s).
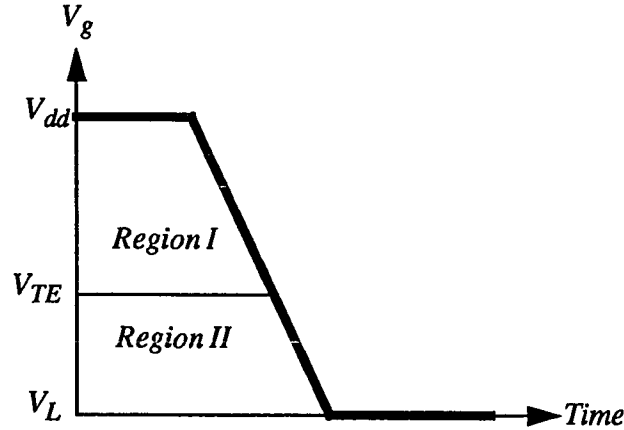
FIGURE 2.3 MOS Switching Regions of Operation

During the first region of switching, the transistor is turning off. Hence, all the channel charge is leaving the MOS switch in this region. C_{ov} is also coupling V_g to C_s. Once V_g falls below V_{TE} the transistor is off; hence, the channel charge (Q_{st}) no longer exists. However, C_{ov} continues to couple voltage to the storage capacitor C_s.

While in region I, the MOS switch (M_1 of figure 2.1) can be replaced by a combination of capacitors and a resistor [5], see figure 2.4. The Resistor (R_{ch}) is the on channel resistance of the MOS switch. C_1 is the combination of the overlap capacitance (C_{ov}) and
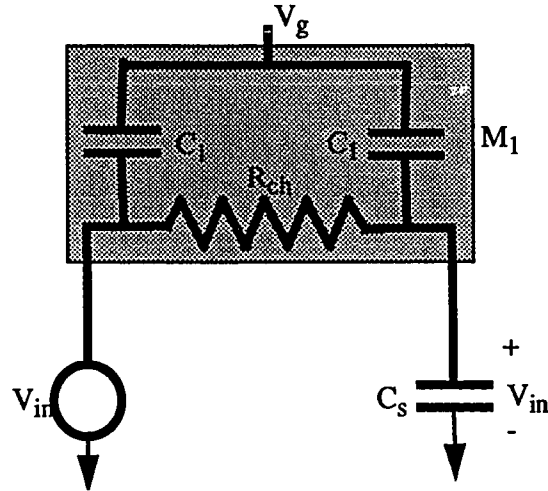
FIGURE 2.4 Charge Injection Model of a MOS Switch in *Region I*

the effective capacitance due to charge stored in the channel (C_{ox}).

$$C_1 = C_{ov} + \frac{C_{ox}}{2}$$ 2.4

where it is assumed half the channel charge exits through the drain and half through the source. The total charge stored in the channel is given by

$$Q_{st} = (V_{dd} - V_{TE}) \times C_{ox} \bullet W \bullet L$$ 2.5

where L is the channel length. The channel charge is the accumulation of electrons (absence of holes) on the gate capacitor's bottom plate, the channel.

Using the fundamental equation for charge coupling,

$$dQ = C \times dV$$ 2.6

The total charge injected into the capacitor C_s in *region I* is

$$Qtot_I = Q_{ch} + Q_{ov}$$ 2.7

The charge injection due to channel charge is

$$Q_{ch} = \frac{C_{ox}}{2} \times (V_{dd} - V_{TE})$$ 2.8

where Q_{ch} is assumed to be half the charge in the conductive channel (Q_{st}). This assumption is only valid for a gate voltage (V_g) with a long fall time. The magnitude of the charge injection due to mobile channel charges (Q_{ch}) depends on V_{TE}, V_{dd}, and C_{ox}. C_{ox} is process dependent, changing as the oxide thickness (T_{ox}) varies.

$$C_{ox} = \frac{\varepsilon \cdot \varepsilon_{si} \cdot W \cdot L}{T_{ox}}$$

2.9

where $\varepsilon = 1.04 \times 10^{-12}$, the permittivity of free space and $\varepsilon_{si} = 2.9$, the relative permittivity of silicon dioxide.

As the device gets larger (W and L increase), the charge injection due to Q_{ch} also increases. By reducing the width of the MOS switch, Q_{ch} is reduced; however, the on channel resistance of the MOS switch (R_{ch}) is increased.

$$R_{ch} = \frac{L}{k'_n \cdot W \cdot (V_{gs} - V_{TE})}$$

2.10

where k'_n is a process parameter of the transistor, and V_{gs} is the gate to source voltage. This increase in R_{ch} slows down the acquisition of V_{in}, since V_{in} charges C_s through R_{ch}, refer to figure 2.4. Therefore, there is a system limit as to how small W can be. Reduction in channel length (L) is limited by process technology currently at 1μ.

The channel charge injection (Q_{ch}) is also dependent on V_{TE}, the effective threshold voltage of the MOS switch. The MOS switch has a process controlled zero bias threshold voltage (V_{TO}). The effective threshold voltage (V_{TE}) alters the zero bias threshold voltage as a function of V_{in} and effect coefficient (γ). The effective threshold of the MOS device is given by[6].

$$V_{TE} = V_{TO} + V_{in} + \gamma(\sqrt{|-2\phi_f + V_{in}|} - \sqrt{|-2\phi_f|})$$

2.11

where $2\phi_f$ is the substrate fermi level. ϕ_f, γ, and V_{TO} are process dependent. The zero bias threshold (V_{TO}) typically ranges from 0.5 to 1 volt.

Since the body effect coefficient is positive for N-channel enhancement devices, V_{TE} increases as V_{in} increases. Therefore, the charge injection due to channel charge decreases as V_{in} increases. Combining 2.6, 2.8, 2.10, and 2.12, the net voltage change on the storage node as a result of channel charge is

$$V_{ch} = \frac{W \cdot L \cdot \varepsilon \cdot \varepsilon_{si}}{2 \cdot C_{ox} \cdot C_s} ((V_{dd} - V_{in} - V_{in}) - \gamma(\sqrt{|-2\phi_f + V_{in}|} - \sqrt{|-2\phi_f|}))$$

2.12

Typically, V_{dd} is equal to the supply voltage (V_{dd}); therefore, the channel charge injection is dependent on the value of V_{dd}. Charge injection is also a function of temperature, because V_{TO} is dependent on temperature.

$$V_{TO}(T) = V_{TO} - \alpha(T - T_o)$$

2.13

where V_{TO} is the zero bias threshold at room temperature $(T_o = 300°K)$ and T is the actual temperature. α is typically 2.3mv/°C [7]. V_{TO} decreases 2.3mv for every 1°C increase in temperature.

Clock feed through also contributes to charge injection in *region I*. The voltage change on the gate causes a charge of

$$Q_{ov_I} = C_{ov} \cdot (V_{dd} - V_{TE}) \qquad\qquad 2.14$$

to be injected into the storage node. This is also dependent on V_{dd}. However, the contribution of Q_{ov} in *region II* will make the overall contribution of clock feed through independent of V_{TE}.

Once the MOS switch has turned off, the transistor enters into *region II* of operation, see equation 2.3. Since the transistor is off, the charge injection due to channel charges is zero.

$$Q_{ch} = 0 \qquad\qquad 2.15$$

However, C_{ov} still exists as shown in the model of the MOS switch of figure 2.5.
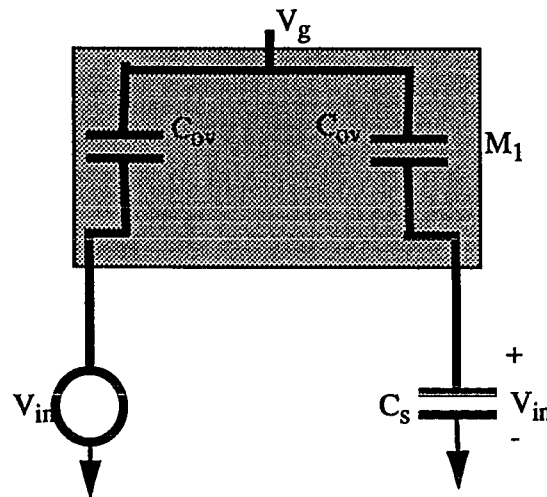
FIGURE 2.5 Charge Injection Model of MOS Switch in *Region II*

The net charge injected into the storage node for region II is

$$Qtot_{II} = C_{ov} \cdot (V_{TE} - V_L) \qquad\qquad 2.16$$

Combining 2.7, 2.8, and 2.16, the total charge injection is

$$Q_{inj} = C_{ov} \cdot (V_{dd} - V_L) + \frac{C_{ox}}{2} \cdot (V_{dd} - V_{TE}) \qquad 2.17$$

From equations 2.14 and 2.16, the total charge injection due only to clock feed through is

$$Q_{ov} = C_{ov} \cdot (V_{dd} - V_L) \qquad 2.18$$

Consequently, the overall charge injection due to clock feed through is independent of V_{TE}.

The effect of the combination of clock feed through and channel charge is to change the voltage stored on capacitor C_S from its original value V_S to V_S'.

$$V'_s = V_s + \frac{Q_{ov} + Q_{ch}}{C_s} = V_s + \frac{Qtot_I + Qtot_{II}}{C_s} \qquad 2.19$$

This error can be reduced by increasing C_S, but this effects the acquisition time of V_{in}. The time constant limiting the acquisition time of the input signal is

$$T_c = R_{ch} \times C_s \qquad 2.20$$

where R_{ch} is the on resistance of the MOS device given by 2.10 and C_S is the total capacitance tied to the storage node.

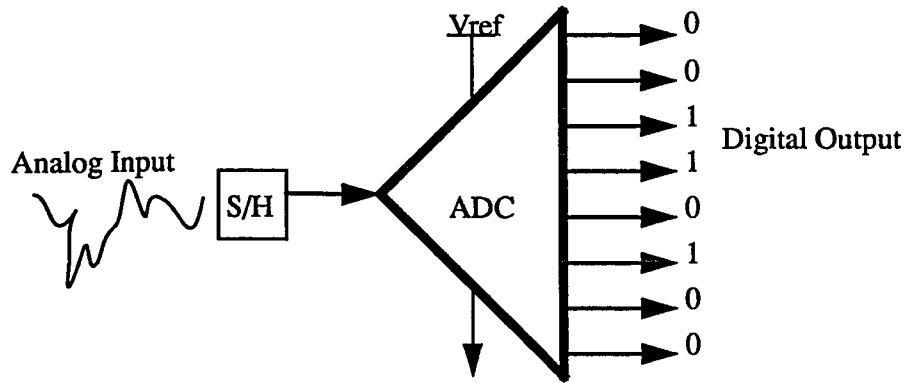## 2.2 Analog-to-Digital Converter Basics

An analog-to-digital converter (ADC) is a type of electronic circuit which functionally digitizes a continuous analog input voltage into a discrete digital word. The block diagram of a typical system consisting of an ADC is shown in figure 2.6.

FIGURE 2.6 Analog-to-Digital Converter System Block Diagram

A typical ADC uses a Sample-and-hold circuit to acquire an analog voltage level at some instance in time. The acquired discrete voltage is then fed to the algorithmic circuitry responsible for converting this voltage level to its digital equivalent. The sample-and-hold circuit is necessary because the ADC algorithmic block requires some non-zero amount of time to determine the digital equivalent of the applied input. Fundamentally, this non-zero time corresponds to the maximum conversion rate of the ADC.

Once the continuous input is held, the corresponding analog voltage is applied to the input of the ADC. For a resolution of N-bits, 2^N possible output codes exist. For example, an 8-bit ADC (N=8) has 2^8 =256 possible output codes. Digitally, this corresponds to binary outputs 00000000, 00000001, 00000010,..., 11111111. The analog input range is determined by a reference voltage (Vref). If the analog input $V_{in} \geq Vref$ the ADC will output 11111111. The lower end of the input range occurs at $V_{in} \leq 0v$, yielding the output 00000000. As the input changes linearly from 0v to Vref, the digital output changes discretely from 00000000 to 11111111. At an input voltage of Vin=Vref/2, the equivalent digital output is 10000000. The analog resolution (V_R) is the magnitude of each voltage quantization step required to change the output by one bit. This is related to the ADC's resolution (N) by the following

$$V_R = \frac{Vref}{2^N}$$

2.21

Ideally, the value of V_R is the same for each output code transition.

As shown in figure 2.7, the transfer curve of an 8-bit ADC is a plot of the digital output code vs. analog input voltage. V_R corresponds to the width of the staircase; the smaller the width, the higher the resolution.
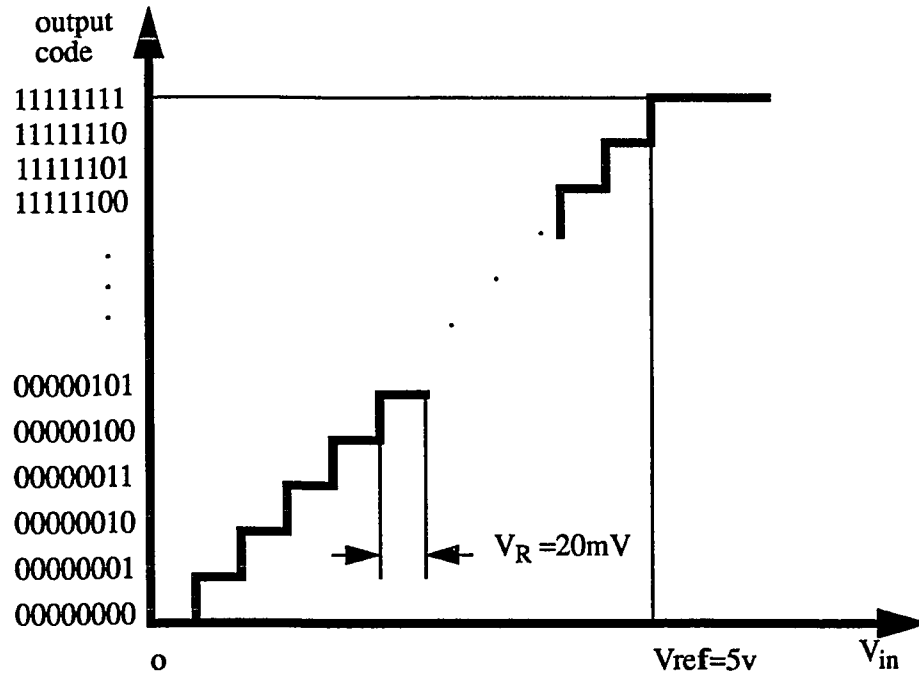
FIGURE 2.7   ADC Transfer curve

In a typical application, the reference voltage (Vref) is 5 volts. For an 8-bit resolution ADC, Vref is divided into 2^8 equal quantization steps. This corresponds to 20 mv of quantization voltage between each step. Referring to figure 2.7, as the input voltage increases from 0v to 5v, the digital output increases from 00000000 to 11111111. With each 20mv increase in Vin, the output increases by +1 binary code. There are many circuit design techniques and architectures for implementing the ADC transfer function of figure 2.7, but for now the ADC will be treated as a black box. Within that black box are analog decision blocks made of comparators and voltage dividing networks made of resistors and/or capacitors.

2.3 Sample-Data Comparator

2.3.1 Comparator building block in Analog-to-Digital Converters

One main element contained within the ADC is the sample-data comparator. In complementary metal oxide semiconductor (CMOS) integrated circuits, the comparator serves two functions. First, it is used to sample-and-hold the analog input voltage. ADC's using CMOS processes and sample-data comparators do not require an external sample and hold circuit. The second, and most important function of the sample-data comparator, is analog comparison. The analog comparator bridges the gap between real analog voltages and the mathematical digital words.

The analog comparator (figure 2.8) simply determines if the voltage potential at the positive input is larger than the voltage applied to the negative input.
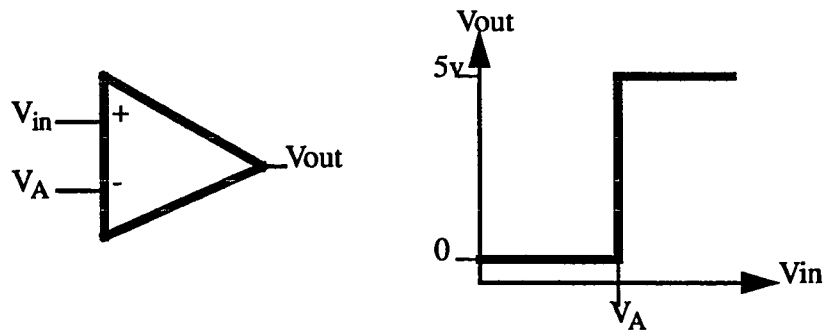
FIGURE 2.8 Ideal Analog Comparator and Transfer Function

The output of the comparator is determined by the following relationship.

$$\text{if } V_A > V_{in} \text{ then } V_{out} = 0v \qquad\qquad 2.22$$

$$\text{if } V_A < V_{in} \text{ then } V_{out} = 5v \qquad\qquad 2.23$$

The comparator is used as an analog decision block interfacing analog inputs to digital outputs. CMOS comparators can be designed with nearly zero input current. This allows the comparator to function as both a sample-and-hold and an analog decision block.
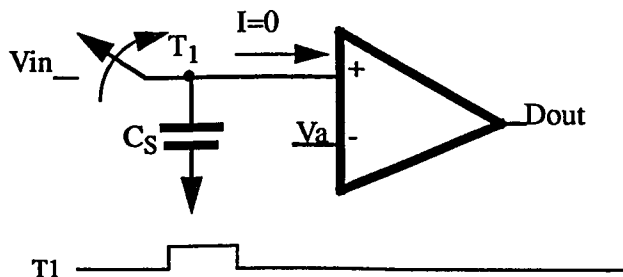
FIGURE 2.9   Comparator used as Sample-and-Hold

As shown in figure 2.9, the analog input voltage (Vin) is sampled on the capacitor C_S while signal T_1 is high. Once T_1 goes low and as long as T_1 remains low, the instantaneous input voltage remains stored on C_S. This type of built in sample-and-hold is possible in CMOS and NMOS integrated circuits because the MOS gate current is negligible. For bipolar type comparators the base current (I_B) would discharge the stored voltage; hence, CMOS is a common process used for ADC's with on board sample-and-holds.

A complete analog-to-digital converter may consist of resistors, comparators, and logic devices. Figure 2.10 shows the usefulness of a comparator in a 1-bit analog-to-digital converter. In this example, a resistor ladder is used to divide the reference voltage into a quantized decision voltage level used as an input to the comparator. This reference level is compared to the sampled input voltage.
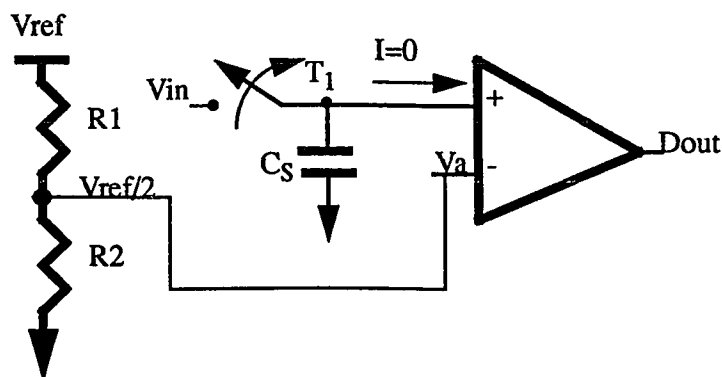
FIGURE 2.10   A 1-Bit Analog-to-Digital Converter

The output of the 1-bit ADC is either a digital "1" or a digital "0". If the sampled voltage, Vin>Vref/2 then the comparator output is a "1". If the input voltage is smaller then Vref/2, then the ADC output is a "0". For a 1-bit ADC (N=1), corresponding to an analog quantization step of V_R=Vref/2. Figure 2.11 shows the transfer curve of the 1-bit ADC. Notice how this resembles the transfer curve of the ideal comparator of figure 2.8.
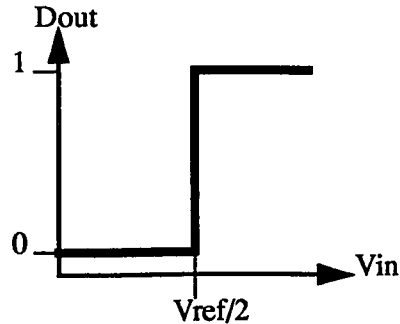
FIGURE 2.11   Transfer Curve of a 1-Bit ADC

In an N-bit ADC, resistors or capacitors must divide the reference voltage into 2^N equal quantization points. This leads to more complex circuits than that of figure 2.10. Regardless of the resolution, the comparator is a key element in most ADC architectures. The non-ideal behavior of the comparator is a major limiting factor in the resolution and conversion speed of the analog-to-digital converter.

2.3.2 Single Ended Comparators

The simplest CMOS comparator is an inverter. By biasing the inverter to its trip point, the inverter acts as a high gain amplifier. The trip point of a CMOS inverter is given by

$$Vtrip=Vout=Vin \qquad 2.24$$

The inverter trip point occurs when the inverter's output equals its input, this point serves as the bias point of the comparator. Figure 2.12 shows the transfer characteristics of a typ-

ical inverter. Except for finite gain, this curve is identical to that of an ideal comparator (figure 2.8) with V_A=Vtrip.
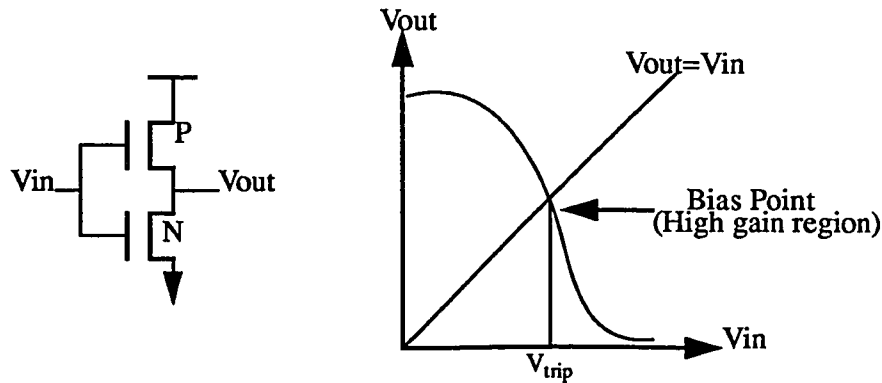
FIGURE 2.12 Transfer function of a CMOS Inverter

In order to use an inverter as a comparator, several additional circuit elements are required, as shown in figure 2.13.
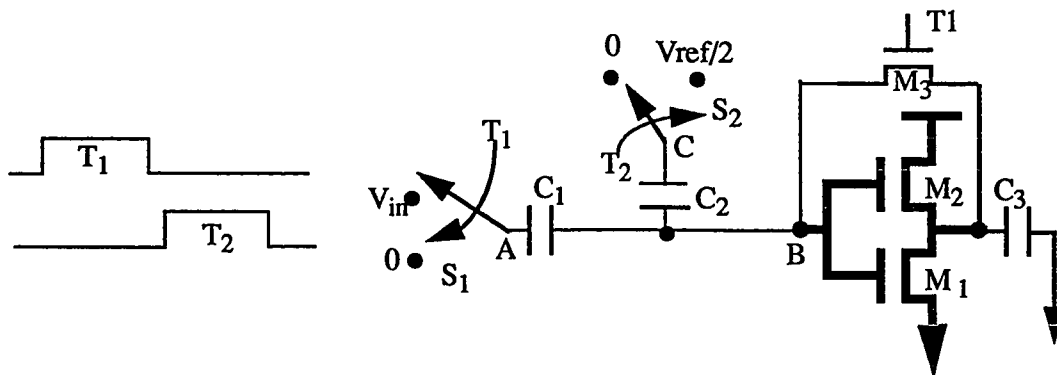
FIGURE 2.13 Detailed CMOS Comparator and Timing

The inverter, or gain element of figure 2.13, is comprised of M_1 and M_2. M_3 is known as the feedback or auto zero switch. When signal T_1 is high, Transistor M_3 is on, forcing the inverter into its high gain region: Vout=Vin=Vtrip. When T_1 goes low, M_3 turns off, but Vtrip is stored on capacitors C_1 and C_2. The inverter trip point remains stored on these capacitors throughout the conversion; thus, keeping the comparator in its high gain region. During the auto zeroing time (T_1=1) the analog input voltage (Vin) is sampled on capacitor C_1 through switch S_1. After T_1 goes low, T_2 goes high switching S_1 to ground and S_2 from ground to Vref/2. The fundamental equation for charge injection is

$$dQ = C \times dV \qquad\qquad 2.25$$

By switching node A from Vin to 0v a net charge of value

$$dQ_1 = C_1 \times (Vin - 0)$$ 2.26

is injected into node B. Simultaneously, node C is switched from 0v to Vref/2. This injects a net charge of

$$dQ_2 = C_2 \times \left(0 - \frac{Vref}{2}\right)$$ 2.27

into node B. Applying superposition, the total charge displacement at node B is given by:

$$dQ_{total} = dQ_2 + dQ_1$$ 2.28

This yields a net charge injected into node B of:

$$dQ_{net} = C_1 \times V_{in} - C_2 \times \frac{Vref}{2}$$ 2.29

Any net positive change in charge, $dQ_{net} > o$, on node B will raise the voltage at that point by

$$dV = \frac{dQ_{net}}{C_{nodeB}}$$ 2.30

driving the inverter output low. Any net loss of charge, $dQ_{net} < 0$, will lower the voltage at node B forcing the output of the inverter to its high state. If $C_1 = C_2$ then Vin will be compared to Vref/2. If Vin>Vref/2 then the net charge (dQ_{net} from equation 2.30) is positive and the inverter will output a "0". On the other hand, if Vin<Vref/2 the net charge is negative forcing the inverter output to "1". By logically inverting the comparator output, a transfer function similar to that of a 1-bit ADC has been achieved (see figure 2.11).

This inverter comparator behaves like the ideal comparator of figure 2.8 except it has finite gain limited by the output impedance of transistors M_1 and M_2 of figure 2.13. Along with finite gain, the comparator circuit also has an offset voltage. Conceptually, the offset voltage of a single ended comparator is the variation in trip point over supply, temperature, and process. During the auto zeroing phase ($T_1 = 1$) the feedback transistor accounts for these variations automatically and stores the exact trip point on the coupling capacitors C_1 and C_2. Since the inverter is always forced to the point Vin=Vout=Vtrip regardless of process and operating conditions, the inherent offset is 0. However, charge injection resulting from turning off feedback transistor M_3 effects the initial voltage at node B such that $V_{in} \neq V_{out}$, leading to an input offset voltage.

2.3.3 Charge injection in a Single Ended Comparator

Ideally, for a single ended comparator, the trip point will always be $V_{out} = V_{in}$. The only way an offset can exist is if some disturbance forces V_{in} to increase or decrease from its quiescent value. In this case,

$$v_{out} = V_{in} + V_{os} \times A_v \qquad\qquad 2.31$$

where V_{os} is the offset voltage or voltage change from quiescence as a result of some external disturbance and A_v is the comparator gain. In MOS inverters using feedback switches for auto zeroing, charge injection changes the comparator trip point from V_{trip} to $V_{trip} + V_{os}$. The result of this change in trip point leads to an initial offset on the comparator. Figure 2.14 shows how this effects the ideal comparator transfer curve.
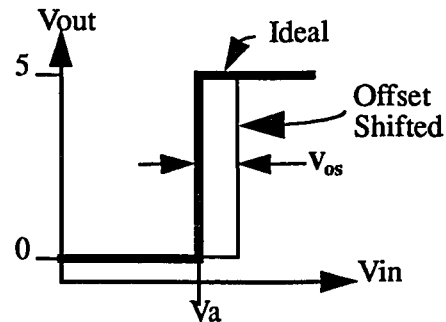
FIGURE 2.14 Transfer Curve of Ideal Comparator with Offset

This offset voltage (V_{os}) can be modeled as a voltage source tied to the input of the ideal comparator (see figure 2.15). In this case, a larger input voltage than V_A is required to overcome the offset voltage before the output can go high. The polarity of V_{os} can also be negative depending on the disturbance. For negative V_{os}, a smaller input voltage than V_a will force the comparator output high.

$$V_{in} = Va - Vb \mp V_{os}$$
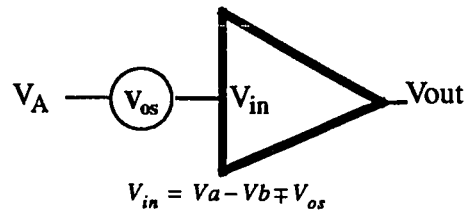
FIGURE 2.15 Ideal Comparator with Offset

The comparator offset causes an inherent offset in the ADC. Figure 2.16 shows how the ideal ADC transfer curve is effected by a comparator offset.
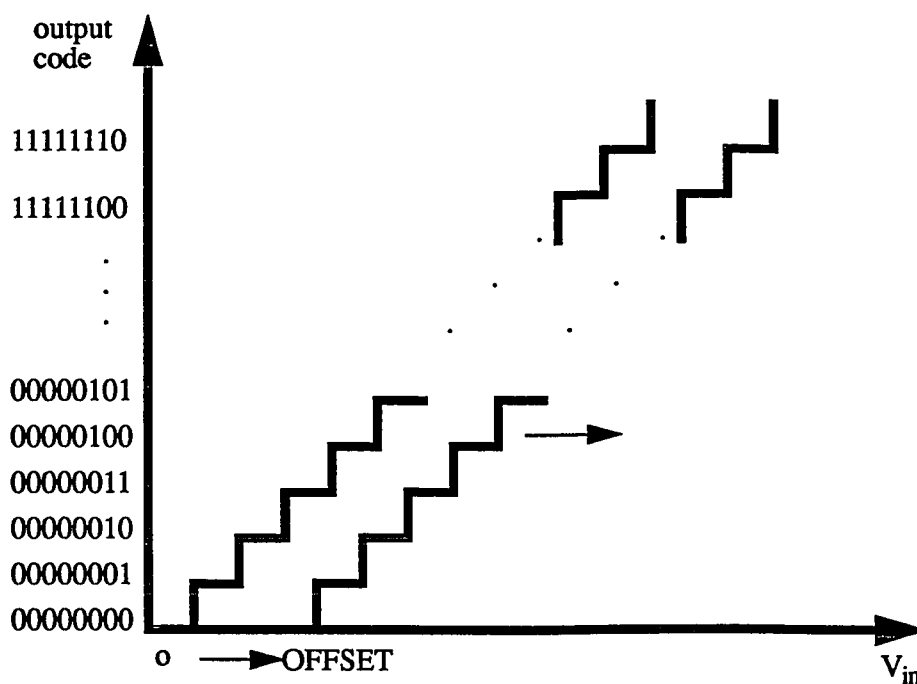
FIGURE 2.16 Ideal ADC Transfer Curve with Offset

The quantization between each step is unaffected by comparator offset in some ADC architectures; however, the zero point of the ADC has changed. A larger (or smaller) input voltage is required for the output of the ADC to change from 00000000 to 00000001. For many system designs using ADC's, a large offset error is undesirable; thus, circuit design techniques must be utilized to eliminate comparator offset.

As shown in figure 2.17, charge injection is due to the overlap capacitance (C_{ov}) and charge forming the conductive channel (Q_{st}) in the MOS feedback switch.
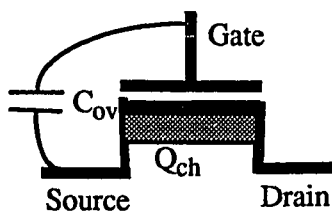
FIGURE 2.17 C_{ov} and Q_{ch} in an MOS Switch

The input node of a comparator is a high impedance capacitive node. Therefore, any charge injected into that node will change the voltage at that node (figure 2.18).
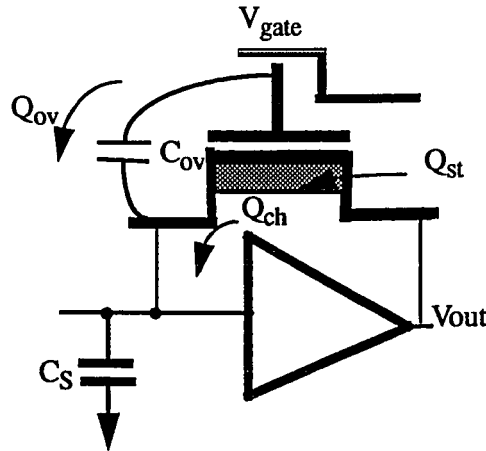
FIGURE 2.18   Charge Injection in a Single Ended Comparator

Charge is coupled to this node through C_{ov} of the MOS feedback switch. When the feedback switch is turned off, the gate voltage changes from supply (V_{dd}) to 0v. The total charge coupled through C_{ov} is

$$Q_{ov} = V_{dd} \times C_{ov} \qquad 2.32$$

When the MOS switch is on, there is some charge stored in the channel. When the switch is turned off, a fraction of that charge is injected into the input node of the comparator. This charge is Q_{ch}. The total charge injected into the input of the comparator is the sum of the fractional channel charge and charge coupled through C_{ov}:

$$Q_{inj} = Q_{ch} + Q_{gs} \qquad 2.33$$

From 2.25, the total change in voltage at the input is given by

$$dV_{in} = \frac{Q_{inj}}{C_s} \qquad 2.34$$

Substituting 2.32 and 2.33 into 2.34, the comparator offset is

$$V_{os} = \frac{(V_{dd} \times C_{ov} + Q_{ch})}{C_s} \qquad 2.35$$

2.3.4 Differential Comparators

In addition to the single ended comparator, a fully differential comparator structure can also be used in analog-to-digital converters. For differential type comparators, an initial offset exists due to mismatches between the two inputs. These mismatches are due to

input transistors, coupling capacitors, and load differences in the symmetrical circuit. When auto zeroing a differential comparator both outputs are shorted to the inputs of the comparator (see figure 2.19). This forces all inherent mismatches to be stored on the input capacitors, C_1 and C_2. Once auto zeroed, the comparator offset, due to input mismatches, becomes zero.
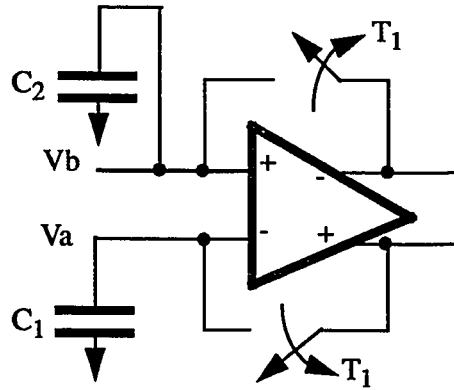
FIGURE 2.19 Differential Comparator

Once the feedback switches are opened, charge injection forces the high impedance input nodes to change voltage (see figure 2.20). If $Q_1=Q_2$, the overall effect of charge injection is a common mode change. The offset will not change since the comparator is fully differential. In a real circuit, $Q_1 \neq Q_2$ due to mismatches in the two feedback transistors, and mismatches in the coupling capacitors, C_1 and C_2. Therefore, $\Delta V_1 \neq \Delta V_2$ leading to an offset voltage V_{os} given by:

$$V_{os} = \Delta V_1 - \Delta V_2$$

2.36

The fully differential structure is less sensitive to charge injection than the single ended type comparator. But for high resolution ADC's, N>8-bits, charge injection can still lead to significant offset variations.
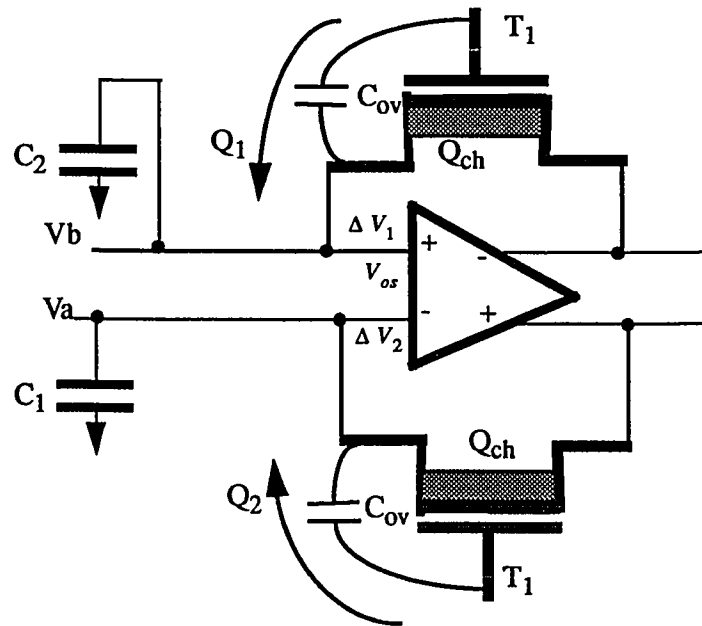
FIGURE 2.20   Differential Comparator with Charge Injection

2.4 Characterization of Analog-to-Digital Converters

2.4.1 Linearity Plot

The transfer curve of an analog-to-digital converter represents an ideal plot of the output code vs. input voltage. By plotting the transfer curve of a real ADC, linearity, offset, fullscale, and gain errors can be determined for characterization of its performance.

The linearity error of an ADC at an arbitrary code is the difference between the ideal input voltage required to give that code and the actual voltage. The actual voltage is determined by slowly ramping the input voltage from 0v to Vref. The digital output of the ADC is monitored and the input voltage is measured when the output of the ADC is making a transition. This voltage is subtracted from the ideal transition voltage for that code. The error voltage is

$$V_\xi = V_{measured} - V_{ideal} \qquad 2.37$$

V_ξ is determined for every code transition and converted from a voltage error to an LSB error

$$LSB_\xi = V_\xi \times \frac{2^N}{Vref} \qquad 2.38$$

where N is the resolution in bits. One LSB unit corresponds to the width of the ideal ADC transfer function's staircase. Ideally, one LSB change in the input voltage will change the output code by one bit.

A linearity plot is used to show the accuracy of an ADC. Rather than plotting the transfer curve to characterize the ADC, a plot of linearity error in LSB's, is plotted for each input code. Figure 2.21 shows a typical linearity plot of a 10-bit ADC.
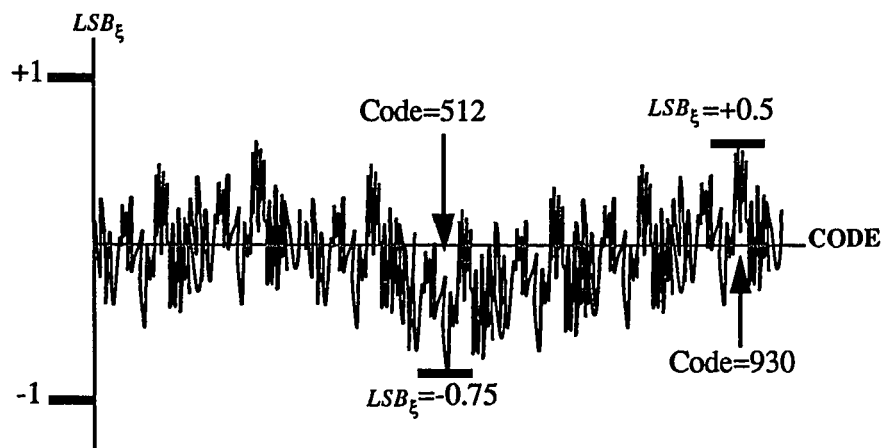
FIGURE 2.21   Linearity Plot of a 10-Bit ADC

In this plot, the horizontal axis corresponds to the codes 0 to 1023. The vertical axis corresponds to the linearity error at each code in LSB's. For this particular ADC, the worst error occurred at code 512. For this code, an error of -0.75 LSBs occurred.

For a 10-Bit ADC, the width of each step on its transition curve is

$$1LSB = V_R = \frac{Vref}{2^N} \qquad\qquad 2.39$$

For Vref=5v,

$$1LSB = \frac{5V}{1024} \cong 5mV \qquad\qquad 2.40$$

At each possible output code, the ideal input voltage is

$$V(Code)_{ideal} = \frac{Vref}{2^N} \times Code \qquad\qquad 2.41$$

The ideal input voltage required to give an output of 512 is

$$V(512)_{ideal} = \frac{5V}{1024} \times 512 = 2.5V \qquad\qquad 2.42$$

The error voltage at any given code is

$$V_\xi = LSB_\xi \times \frac{Vref}{2^N} \qquad\qquad 2.43$$

From figure 2.22, the error at code 512 is -0.75 LSB. This corresponds to an input error voltage of

$$V_\xi = \frac{5V}{1024} \times (-0.75) = -3.66mV \qquad\qquad 2.44$$

The actual input voltage required for the ADC to output a given code is the sum of the ideal voltage at that code and the error voltage at the same code. The input required for this ADC to change from code 511 to 512 is

$$V_{measure} = 2.5V - 3.66mV \qquad\qquad 2.45$$

A linearity plot is more useful than a transfer plot for determining the linearity of an ADC. Figure 2.22 shows the transfer curve of a 3-bit ADC and its corresponding linearity plot.
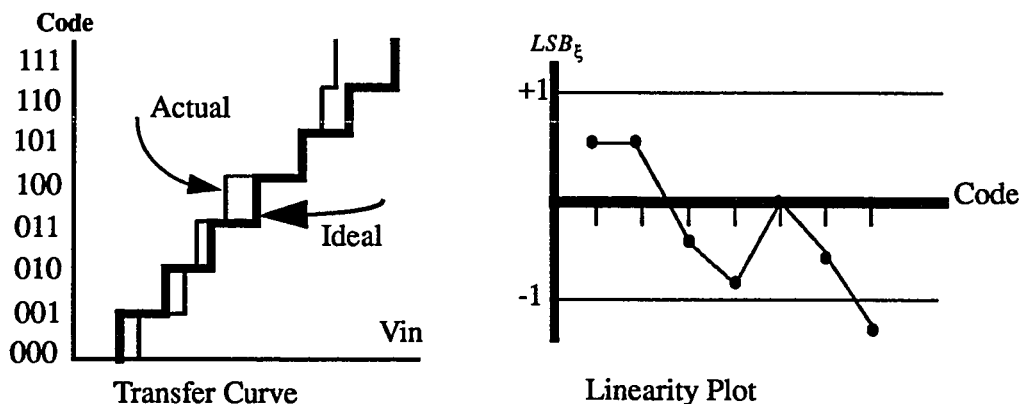
FIGURE 2.22 3-Bit Linearity Plot and Transfer Curve.

As resolution increases, the transfer curve of an ADC becomes difficult to interpret. The linearity plot is the conventional method of examining the linearity of the ADC. For large resolutions, the linearity plot is simpler to extract data for characterization of the ADC.

Along with linearity, the offset of the ADC can be determined from the linearity plot. Figure 2.23 shows the linearity plot of an ADC with a +1/2 LSB offset.
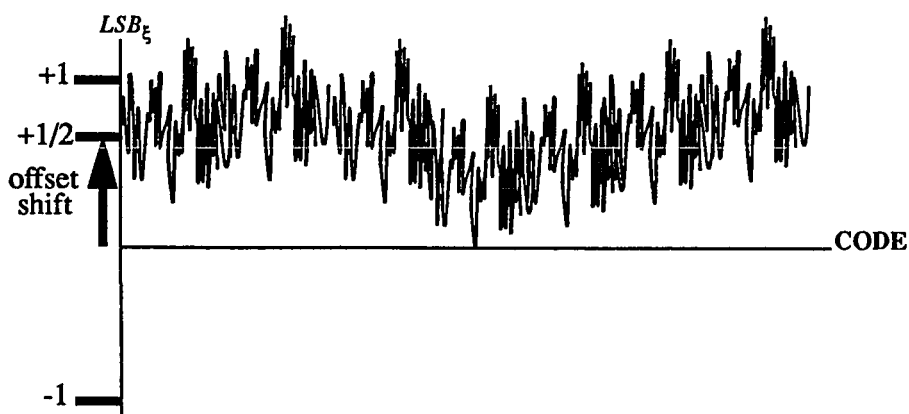
FIGURE 2.23 Linearity Plot of ADC with Offset

The offset error is the linearity error calculated at code 1. The ideal offset voltage from 2.41 is

$$V_{offset} = \frac{Vref}{2^N} \times 1 \qquad\qquad 2.46$$

The actual offset is the difference between V_{offset} and the measured input voltage at code 1 converted to an LSB error.

$$OFFSET = [V_{offset} - V_{code = 1}] \times \frac{Vref}{2^N}$$
2.47

The result of an offset in some ADC architectures is to shift the entire linearity curve by that offset. Typically, this offset is due to *charge injection*. An ADC with no offset error would have a linearity error of zero at code 1.

In addition to offset and linearity, the fullscale and gain error of an ADC can be determined from the linearity plot. The fullscale error of an ADC is defined as the linearity error at Code 2^N-1. In LSB's the fullscale error is

$$FS = \frac{Vref}{2^N} \times (2^N - 1) - V_{measure}(code=2^N - 1)$$
2.48

The gain error of an ADC is

$$GAINERROR = FS - OFFSET$$
2.49

Figure 2.24 shows an ADC with gain error.
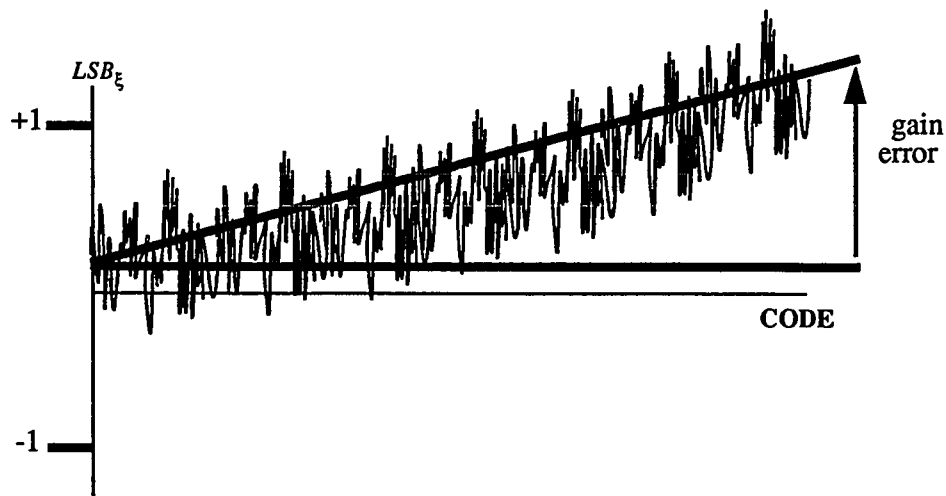
FIGURE 2.24   ADC Linearity Plot with Gain Error

The gain error shows up as a slope in the linearity curve. The larger the slope, the larger the gain error. An ADC with an equal offset error and fullscale error will not have a slope. Unlike offset, gain errors are not due to charge injection, they are a phenomena due to problems with the reference voltage.

2.4.2 Power Supply Rejection Ratio

With a linearity plot, many ADC errors can be easily extracted from the shape of the plot and the scales. Among them are offset, fullscale, gain, and linearity errors. An important piece of information that can be extracted from several linearity plots is the power supply rejection ratio (PSRR). For a typical CMOS ADC, the supply voltage (V_{dd}) is defined to be $5V \mp 10\%$. PSRR is defined as the difference in offset errors measured when V_{dd}=4.5V and V_{dd}=5.5V. Figure 2.25 shows two overlaid linearity plots of an ADC operating at two supply voltages.

FIGURE 2.25 Overlaid Linearity Plots of an ADC Operating at Two Different Supply Voltages

From these linearity plots, it can be seen that the offset has shifted the entire curve when the supply is varied from 4.5V to 5.5V. The power supply rejection ratio is defined as

$$PSRR = |offset\,(V_{dd}{=}4.5V) - offset\,(V_{dd}{=}5.5V)|$$ 2.50

For a typical ADC, the PSRR limit is 1/4 LSB. This means the offset in LSB's can shift by 1/4 LSB when the supply is changed from 4.5V to 5.5V. From 2.43, 1/4 LSB is approximately 1.25mv for a 10-Bit ADC
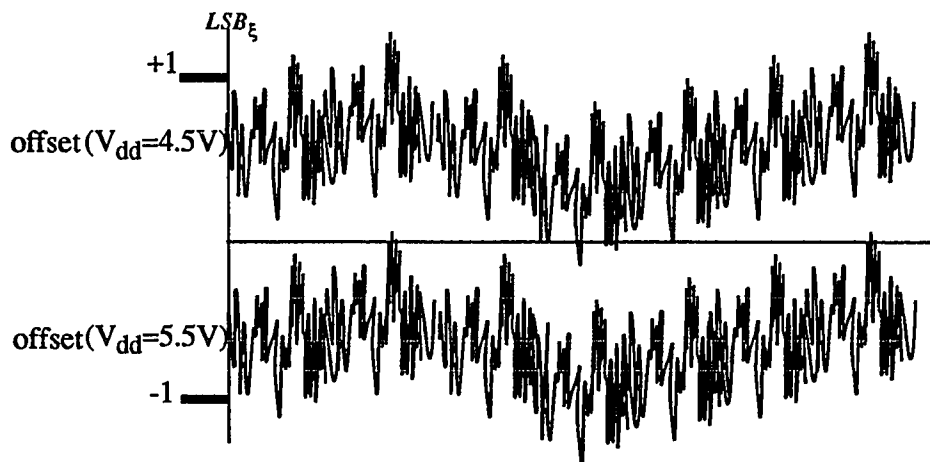
The main contributor to the PSRR error is charge injection. Charge injection leads to a comparator offset voltage, which leads to ADC offset errors. Charge injection is due to the feedback switch in the comparator coupling charge through its gate to source overlap capacitance and channel charges leaving the collapsing depletion region during shut off. The signal driving the gate of the feedback switch is swinging from V_{dd} to ground. Referring to equations 2.8 and 2.32, the charge injection is proportional to V_{dd}.

$$Q_{inj} \propto V_{dd}$$ 2.51

As V_{dd} increases, the charge injection increases forcing the comparator offset to increase in magnitude. Since charge injection is proportional to the supply voltage, the overall

ADC offset is also a function of supply. Therefore, the problems with the PSRR are due to charge injection. By eliminating charge injection or making charge injection independent of supply, the PSRR can be reduced.

2.5 Analog-to-Digital Converter Architectures

In order to fully understand the errors associated with analog-to-digital converters, the *black box* function for converting analog voltages to digital codes will be examined.

2.5.1 Successive Approximation Analog-to-Digital Converters

One method of converting analog voltages to digital codes is by the successive approximation algorithm [8], [9]. For an N-bit successive approximation (SAR) type analog-to-digital converter, N algorithmic steps (one for each bit of resolution) are required for conversion. The SAR algorithm determines the output code one bit at a time from the most significant bit (MSB) to the least significant bit (LSB). The detailed output takes the form

$$D_{out} = [b_N, b_{N-1}, b_{N-2}, ..., b_2, b_1]$$
2.52

where b_N is the MSB and b_1 is the LSB. The successive approximation algorithm requires one comparator, a voltage dividing array of resistors or capacitors, and a digital register.

The first step of the successive approximation algorithm is to compare the input voltage (V_{in}) to Vref/2. This is done by generating a residual voltage

$$Vres_1 = V_{in} - \frac{Vref}{2}$$
2.53

$Vres_1$ is applied to the input of an analog comparator. The comparator will output a "1" if $Vres_1$ is positive and a "0" if $Vres_1$ is negative. The comparator output is defined by

$$Comp=1 \text{ if } V_{in} > Vref/2$$
2.54

$$Comp=0 \text{ if } V_{in} < Vref/2$$
2.55

The MSB output of the ADC is determined by the comparator output.

$$b_N = Comp$$
2.56

This result (b_N) is stored in a successive approximation register (SAR) to be used for subsequent successive approximation steps.

Once b_N has been stored, the next bit can be determined. A new residual voltage is generated.

$$Vres_2 = V_{in} - \frac{Vref}{2} \bullet b_N - \frac{Vref}{4}$$
2.57

This second step compares Vref/4 to the input voltage minus the result of the first comparison. For $b_N=0$, the voltage (Vref/2) subtracted for the first comparison is added back to the residual cancelling the subtraction. For $b_N=1$, Vref/2 remains subtracted from the residual voltage. The comparator will now output Comp. Comp will be stored as bit b_{N-1} in the SAR. These comparisons continue until the LSB is determined. In the last comparison, a residual voltage is generated based on all previous steps.

$$Vres_N = V_{in} - \frac{Vref}{2} \bullet b_N - \frac{Vref}{4} \bullet b_{N-2} - ... - \frac{Vref}{2^{N-1}} b_2 - \frac{Vref}{2^N}$$ 2.58

Each successive step brings the value of Vres closer to the zero. The quantization error of the ADC is defined as

$$V_{quant} = V_{in} - \frac{Vref}{2} \bullet b_N - \frac{Vref}{4} \bullet b_{N-1} - ... - \frac{Vref}{2^{N-1}} \bullet b_2 - \frac{Vref}{2^N} \bullet b_1$$ 2.59

The quantization error is limited by the resolution of the ADC

$$V_{quant} \le \frac{Vref}{2^{N+1}}$$ 2.60

In terms of LSB's, the quantization error of an ADC is

$$LSB_{quant} \le \frac{1}{2} LSB$$ 2.61

The successive approximation algorithm is similar to the mathematical algorithm for determining the binary equivalent of a decimal number. If a decimal number can take on the values 0 to 255, the binary equivalent range would be 00000000 to 11111111. Letting Vref=256 and the binary output of the form [b_8, b_7, b_6, b_5, b_4, b_3, b_2, b_1], the successive approximation algorithm can mathematically determine b[8:1] for any decimal number from 0 to Vref=256.

For example, let Vin=123. The first step of the successive approximation algorithm is to compute

$$Vres_1 = V_{in} - \frac{Vref}{2} \rightarrow 123 - 128$$ 2.62

Since $Vres_1 < 0$, $b_8 = 0$. This result is stored in a register and passed on to the second step

$$Vres_2 = V_{in} - \frac{Vref}{2} \bullet 0 - \frac{Vref}{4} = (123 - 0 - 64) \ge 1 \therefore b_7 = 1$$ 2.63

$$Vres_3 = V_{in} - \frac{Vref}{2} \bullet 0 - \frac{Vref}{4} \bullet 1 - \frac{Vref}{8} = (123 - 0 - 64 - 32) \ge 1 \therefore b_6 = 1$$ 2.64

...

$$Vres_8 = V_{in} - \frac{Vref}{2} \bullet 0 - \frac{Vref}{4} \bullet 1 - \frac{Vref}{8} \bullet 1 - \frac{Vref}{16} \bullet 1 - \frac{Vref}{32} \bullet 1 - \frac{Vref}{64} \bullet 0 - \frac{Vref}{128} \bullet 1 - \frac{Vref}{256}$$ 2.65

The final residual voltage is an approximation of the input voltage. The quantization error of the algorithm is ±1/2. Another step would be required to determine if 01111011 represented 123 or 123.5. For an 8-bit ADC, the quantization is ∓1/2 LSB. For Vref=5v, this corresponds to a quantization error of 10mv.

The actual ADC consists of a binary weighted array of capacitors used to generate Vref/2, Vref/4,... (see figure 2.26).
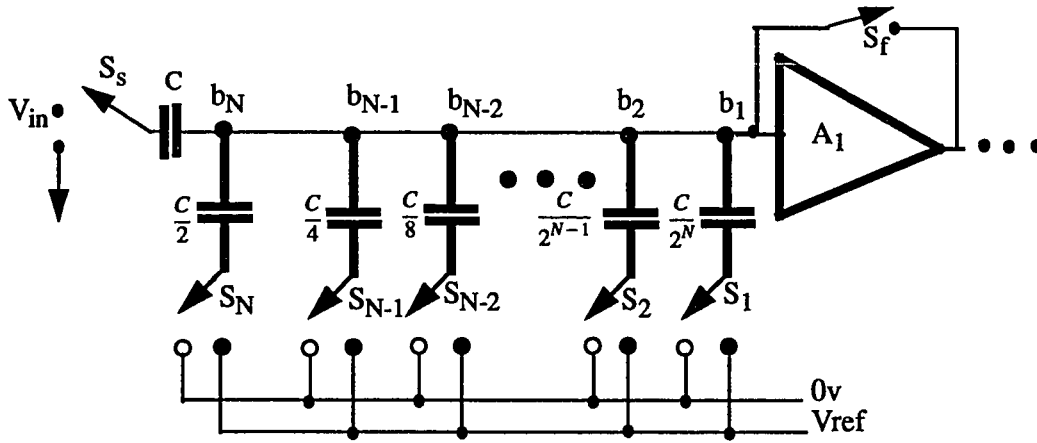
FIGURE 2.26 Successive Approximation ADC

The binary weighted capacitors are used to subtract Vref/2, Vref/4,..., $Vref/2^n$ from V_{in}, while the comparator is used to determine if the result (V_{res}) is positive or negative. A_1 is the first stage of a three stage sample-data comparator.

The first step of the conversion algorithm is to auto zero the comparator and sample the input voltage. The comparator is auto zeroed when the feedback switch (S_f) is closed. During sampling, switches S_1 through S_N are tied to 0v and S_s is tied to V_{in}. After acquisition, S_f and S_s are opened. A total charge of

$$Q_{in} = C \times V_{in} + Q_{inj}$$

2.66

is stored in the capacitor array, where Q_{inj} is the error due to charge injection.

Once V_{in} has been stored in the capacitor array, the MSB of data (bit b_N) is determined. This is done by switching S_N from 0v to Vref. This forces a charge of

$$Q_N = -Vref \times \frac{C}{2}$$

2.67

to be injected into the input node of the comparator. This is added to the previous charge giving a residual charge stored in the capacitor array of

$$Q_{res_n} = C \times \left(Vin - \frac{Vref}{2} \right) + Q_{inj}$$

2.68

The resulting voltage change on the input of the comparator is

$$\Delta V_n = \frac{C \times \left(V_{in} - \frac{Vref}{2} \right)}{C_{total}} + E_1$$

2.69

where the error voltage on the input to the first stage due to charge injection is

$$E_1 = \frac{Q_{inj}}{C_{total}}$$ 2.70

and C_{total} is the total capacitance on the comparator input node.

If ΔV_n is positive, the comparator output is "1" and if ΔV_n is negative, the comparator output is "0". Therefore,

$$\text{Comp}=1 \text{ if } V_{in}>Vref/2$$ 2.71

$$\text{Comp}=0 \text{ if } V_{in}<Vref/2$$ 2.72

The result of the first comparison (Comp) is stored in a digital register as b_N. If b_N is "1", then S_N remains at Vref for the extent of the conversion. On the other hand, if b_N is "0", then S_N is switched back to ground. By switching S_N back to ground, the charge removed from the capacitor array (Q_N) is injected back into the array. This leads to a residual charge, dependent on the result of the first comparison.

Switch s_{n-1} is now switched to Vref for the determination of the second bit of data. the net charge on the input node is

$$Q_{res_{N-1}} = C \times \left(V_{in} - \frac{Vref}{2} \cdot b_N - \frac{Vref}{4} \right) + Q_{inj}$$ 2.73

The resulting voltage change is

$$\Delta V_{N-1} = \frac{C \times \left(V_{in} - \frac{Vref}{2} \bullet b_N - \frac{Vref}{4} \right)}{C_{total}} + E_1$$ 2.74

The comparator will now output Comp based on the sign of ΔV_{n-1}. The value of Comp is stored as b_{N-1} in the SAR to be used for all *successive* steps that follow. b_{n-1} controls switch S_{N-1}.

This algorithm continues until the LSB of data (b_1) is determined. Switches S_N through S_2 are driven by the previous results b_N through b_2. Switch S_1 is tied to Vref. This results in a residual voltage of

$$\Delta V_1 = \frac{C \times \left(V_{in} - \frac{Vref}{2} \bullet b_n - \frac{Vref}{4} \bullet b_{n-1} - \dots - \frac{Vref}{2^{n-1}} \bullet b_2 - \frac{Vref}{2^n} \right)}{C_{total}} + E_1$$ 2.75

The result of this comparison is stored as b_1.

2.5.2 Charge Injection in Successive Approximation Analog-to-Digital Converters

Since the successive approximation type ADC uses only one comparator, it is the simplest architecture to study the effects of charge injection.

Once auto zeroing has completed, the feedback transistor must turn off. A net charge of Q_{inj} is injected into the high impedance storage node of the comparator, see figure 2.27.
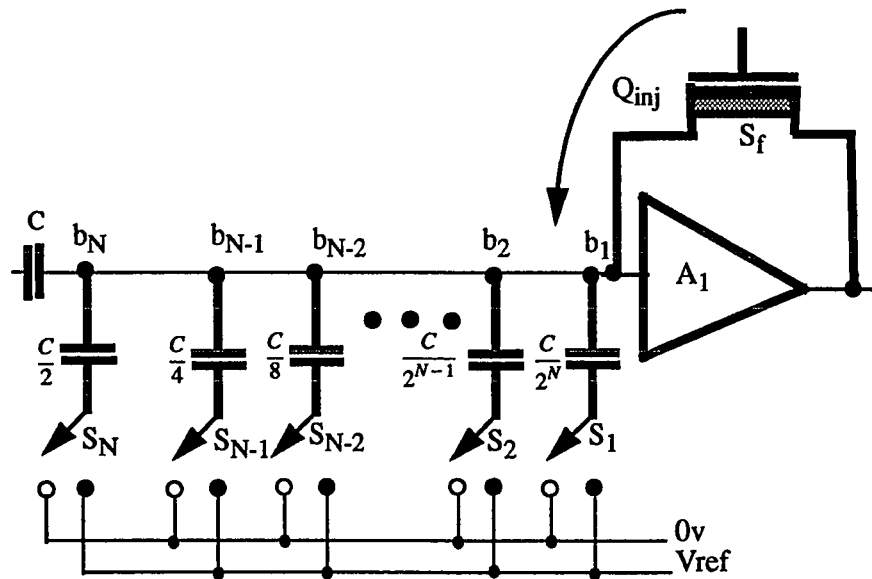
FIGURE 2.27 Charge Injection in Successive Approximation ADC's

The input voltage stored on this node is altered by the error voltage (E_1), from equation 2.70. This error voltage is independent of V_{in} because it equally effects all successive steps of the conversion (2.73-2.75). However, it is dependent on the trip point of A_1. Looking at the ADC as a black box, charge injection alters the input by

$$V_{in}' = V_{in} + E_1 \qquad \qquad 2.76$$

For a given input voltage, the error voltage (E_1) is added then the conversion is started. For all output codes, the expected voltage required to give those codes is shifted by E_1. The offset of the overall ADC is shifted from its ideal value by

$$Offset = E_1 \times \frac{2^N}{Vref} \qquad \qquad 2.77$$

As the resolution (N) increases, or the reference voltage (Vref) decreases, the offset change due to charge injection increases. For large resolution ADC's (N>10), charge injection significantly degrades the successive approximation analog-to-digital converter by altering the offset.

2.5.3 Flash Analog-to-Digital Converters

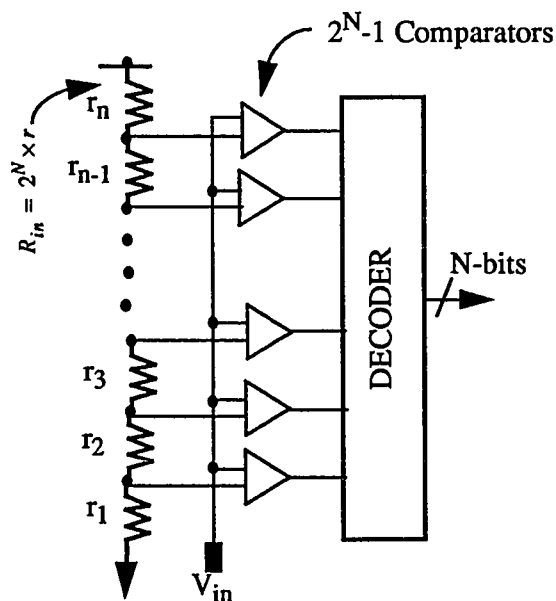Conceptually, the flash type ADC is the most straight forward architecture, see figure 2.28. An N-bit flash ADC uses 2^N-1 comparators and 2^N resistors to determine which of 2^N possible output codes V_{in} corresponds to [10], [11].

FIGURE 2.28 N-bit Flash Analog-to-Digital Converter

An N-bit Flash ADC consists of 2^N equal valued resistors spanning from ground to Vref. The voltage drop across each resistor is

$$V_{drop} = \frac{Vref}{2^N}$$

2.78

This voltage drop is equal to the quantization voltage of an N-bit ADC, see equation 2.21. The Resistor ladder represents the quantized analog voltage steps of the ADC transfer function. If the discrete voltage points at the top of each resistor were measured, they would increase from 0v to Vref in V_R sized steps. These discrete tap point voltages are compared to the input voltage. This comparison requires 2^N-1 comparators. Somewhere

along the resistor ladder, one of the tap voltages will be larger than the input voltage (see figure 2.29). All comparators tied to resistor tap points with voltage levels greater than V_{in} will output a "0", while all comparators tied to tap points with voltage levels less than V_{in} will output "1".
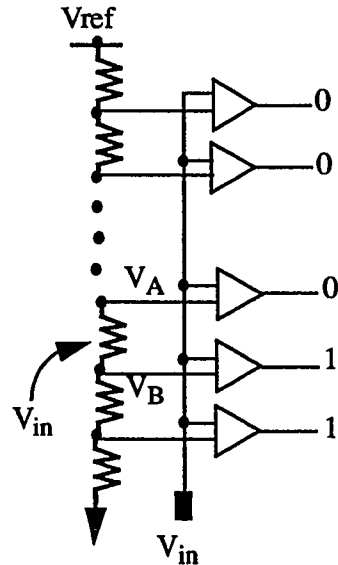
FIGURE 2.29   Comparator Outputs for $V_B < V_{in} < V_A$

V_{in} is a continuous analog voltage in the range defined by Vref. The comparators determined $V_B < V_{in} < V_A$ by changing their outputs from "1's" to "0's" for all comparators tied above V_A on the resistor ladder. The comparator outputs drive a decoder which maps the position along the ladder where the comparators *flip* from "1's" to "0's" to the digital output code. This mapping is similar to an ADC transfer curve with the horizontal axis replaced by resistor tap points, see figure 2.30.
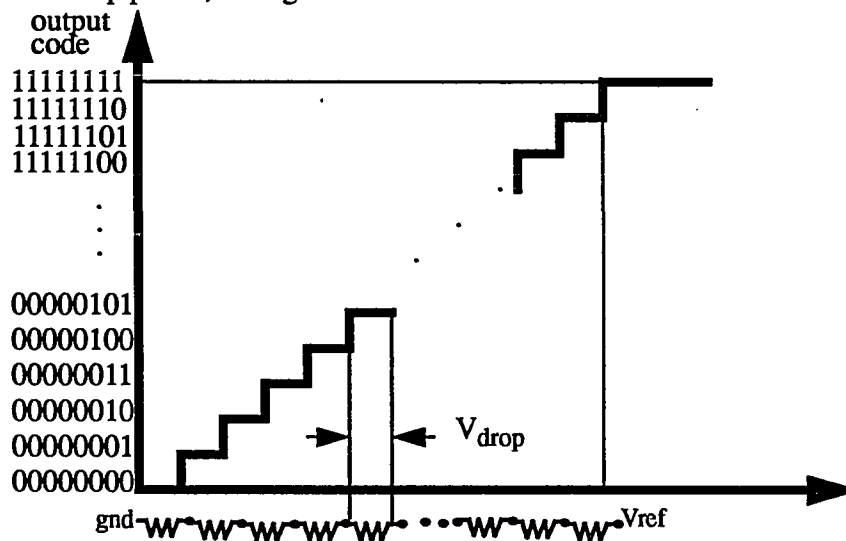
FIGURE 2.30   Resistor Ladder Mapping to ADC Output

For a flash ADC, the resistor ladder divides the reference voltage into the discrete voltages on the V_{in} axis of the ADC transfer curve. Analog comparators determine which tap-points are larger than V_{in} and which are smaller. A digital decoder network looks at the comparator outputs, $C_{out} = C_1, C_2, C_3, \ldots, C_{2^N-1}$, and determines the point where two adjacent comparator outputs are not equal. This flip point is decoded to generate the output code.

This type of ADC architecture is known as a *flash* type because its conversion takes place in one analog comparison step, unlike the successive approximation type ADC requiring N-steps. The advantage of a flash ADC is fast conversion rate, but the disadvantage is large numbers of comparators leading to high power consumption and increased die size.

In order to reduce comparator count without significantly sacrificing speed, architectures using several sub-flash steps are used. An N-bit half-flash ADC consists of two N/2-bit flash ADC's [12]. This type of converter significantly reduces the comparator, but increases the conversion time by slightly more than 2. By adding more flash steps, multistep ADC architectures further reduce comparator count in order to save on die area and power consumption [13].

2.5.4 Charge injection in Flash Analog-to-Digital Converters

Unlike the single comparator structure of the successive approximation ADC, the flash analog-to-digital converter uses 2^N-1 comparators. Each of these comparators is used to determine the transistion of one digital output code. Since each output code changes state when one comparator changes state, charge injecion effects each code independently.

The charge injection of each comparator makes the resistor tap-point voltage it is tied to look larger or smaller, see figure 2.31.
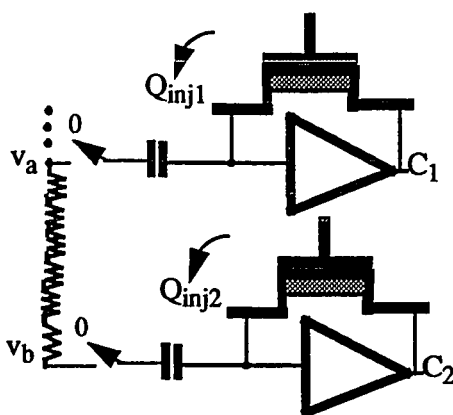
FIGURE 2.31 Charge Injection in a Flash ADC

Assuming the charge injection is different for each comparator. This leads to offsets in each comparator such that the response becomes

$$C_1 = 1 \text{ if } V_a < V_{in} + \frac{Qinj_1}{C_{total}}$$ 2.79

$$C2 = 1 \text{ if } V_b < V_{in} + \frac{Qinj_2}{C_{total}}$$ 2.80

where $Qinj_1$ and $Qinj_2$ are charge injection of two adjacent comparators. These $Qinj_x$ terms will change the linearity error at each code independently. Not only does charge injection effect the offset of a flash ADC, it also effects the linearity by forcing unpredictable changes on each step of the transfer curve. The offset is determined by the first comparator error, while the linearity is effected by each individual comparator.

2.6 Charge Injection Cancellation Techniques

Several methods for charge injection cancellation exist. These include the addition of dummy devices and staggered auto zeroes. Typically, these may not be enough for effective cancellation. Two alternative methods of cancellation are presented. The first is programmable delay auto zeroes, and the second is V_{dd} independent auto zero signals.

2.6.1 Dummy Device Cancellation

One method of cancelling the effects of charge injection is by adding a dummy switch to the high impedance input node of the comparator [14], see figure 2.32.
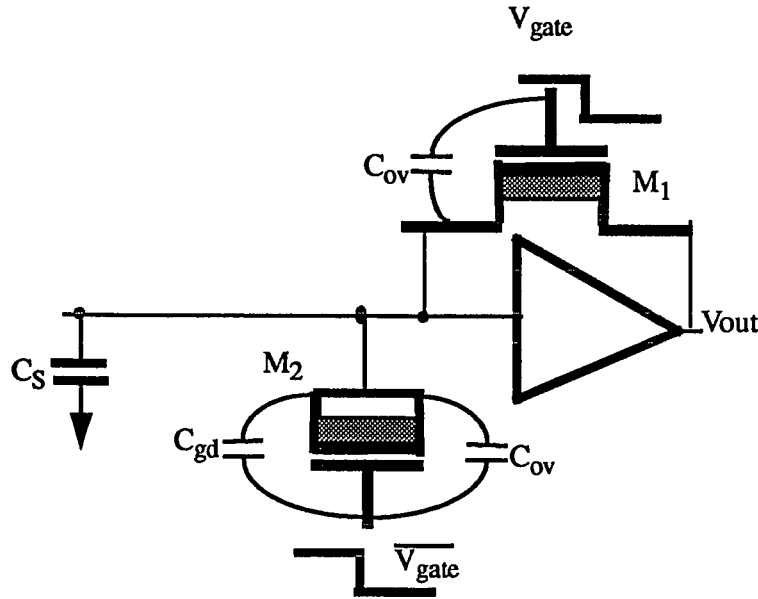
FIGURE 2.32 Dummy Device cancellation

The charge injection, due to clock feed through, can be cancelled by matching the overlap capacitance of M_1's source with the total overlap capacitance of M_2. If the lateral diffusion is the same for the source and drain, then

$$C_{gd} = C_{gs} = C_{ov}$$ 2.81

where the gate to source overlap capacitance is defined as

$$C_{ov} = W \cdot L_D \cdot C_{ox}$$ 2.82

Matching is achieved geometrically by setting the ratio between M_1 and M_2 as follows:

$$W_1 = 2 \times W_2$$ 2.83

$$L_1 = L_2$$ 2.84

Driving the gate of M_2 by the inverse signal driving M_1, the total charge injection due to clock feed through in figure 2.32 becomes

$$Q_{ov} = (C_{gd2} + C_{gs2}) (V_L - V_H) + C_{gs1} (V_H - V_L) \qquad 2.85$$

Assuming M_1 and M_2 have matching C_{ox} and L_D, substituting equations 2.81-2.84 into 2.85 yields

$$Q_{ov} = \left[\frac{2 \cdot W \cdot L_D \cdot C_{ox}}{2} - W \bullet L_D \bullet C_{ox} \right] (V_H - V_L) = 0 \qquad 2.86$$

Therefore, the total charge injection due to clock feed through is cancelled by the dummy device if M_1 perfectly matches M_2.

The problem with this technique is the channel charge injection (Q_{ch}). M_1 and M_2 must be driven by signals 180° out of phase with each other in order to cancel the clock feed through. This is typically done with an inverter whose input is the signal V_{gate} and output drives the gate of M_2. Since an inverter has finite delay, M_1 is turned off an instant sooner then M_2 is turned on. For small delays, M_1 may still be on when M_2 is turning on. This results in M_2 acquiring its channel charge from the comparator output node rather than the charge leaving M_1.

For large delays, the entire charge required to turn M_2 on is pulled out of the high impedance node. This charge is equal to the charge leaving M_1 during turn off if Q_{st} is split symmetrically between the source and drain. Typically, the charge is not split equally between the source and drain. The fractional part (χ) leaving the drain is dependent on the slew rate of the signal driving the gate (α) [15].

$$\chi = \sqrt{\frac{\mu_n \bullet C_{ox} \bullet W \bullet L}{\alpha \bullet C_s}} (V_H - V_{TE}) \qquad 2.87$$

where μ_n is the electron mobility. The net charge injection due only to channel charges becomes

$$Q_{inj} = \chi Q_{ch} - \frac{1}{2} Q_{ch} = Q_{ch} \left(\chi - \frac{1}{2} \right) \qquad 2.88$$

Complete cancellation only occurs when $\chi = 1/2$, the case where half the charge stored in M_1 leaves the source and half leaves the drain. χ is dependent on V_{trip} since V_{TE} increases as V_{trip} increases (see equation 2.11). It is also dependent on temperature, since the mobility of electrons (μ_n) decreases with temperature.

$$\mu_n \propto T^{-1.5} \qquad 2.89$$

χ is also dependent on process parameters. Therefore, χ varies over the normal operating conditions of the device. Consequently, dummy devices will not completely cancel charge injection. For circuits requiring <5mv of accuracy over supply and temperature, the dummy device fails.

2.6.2 Staggered auto zero signals

Another method of charge injection cancellation is possible in circuits using sample-data comparators. This cancellation technique involves breaking the gain elements of the comparator into stages and delaying the falling edge of the auto-zero signals driving the feedback switches of each stage [16]. Figure 2.33 shows a typical 3-stage sample-data comparator and its staggered auto zero timing.
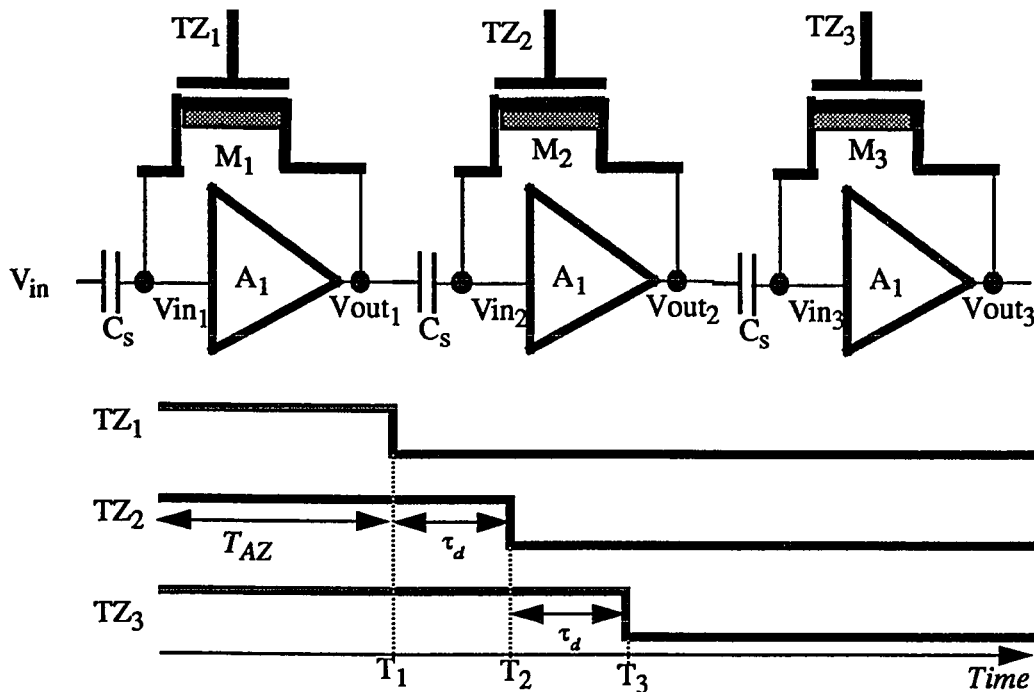
FIGURE 2.33 3-Stage Sample-Data Comparator with Staggered Auto Zero Signals

The first stage feedback switch is driven by TZ_1 which goes low before the signal (TZ_2) driving the feedback switch of the second stage. Similarly, TZ_2 goes low before the signal driving the third stage feedback switch. In other words, M_1 is turned off while M_2 is still on and M_2 is turned off while M_3 is still on.

During time T_{AZ}, all three feedback transistors are on, this is known as the auto zero time. While the transistors are on, each of the individual stages A_1, A_2, and A_3 are biased to their trip points $Vtrip_1$, $Vtrip_2$, and $Vtrip_3$, respectively. These trip points are stored on the amplifier input nodes Vin_1, Vin_2, and Vin_3, and output nodes $Vout_1$, $Vout_2$, and $Vout_3$.

At time T_1, TZ_1 goes low turning off transistor M_1. On the falling edge of TZ_1, charge $Qinj_1$ is injected into the input of stage A_1. This alters the stored trip point voltage on node Vin_1 by

$$E_1 = \frac{Qinj_1}{C_s}$$ 2.90

This error voltage is amplified by A_1, altering the output of the first stage

$$Vout_1 = Vtrip_1 - E_1 \cdot A_1$$ 2.91

This change in voltage is coupled through the capacitor C_s to the input of the second stage. If M_2 is still on, the error voltage $(-E_1 \cdot A_1)$ will not effect the bias point of A_2. While M_2 is on, any change at the input of A_2 will go to ground through the switch tied to the amplifier's output node. M_2 will continue to force Vin_2 to its trip point $Vtrip_2$.

Some time later (τ_d), TZ_2 will go low. τ_d is defined as the delay time between auto zero signals. The falling edge of TZ_2 injects a charge of $Qinj_2$ into the input of A_2. Since the input of each amplifier stage is high impedance, this leads to a stored error voltage of

$$E_2 = \frac{Qinj_2}{C_s}$$ 2.92

This error is amplified by A_2 and coupled to the input of amplifier A_3. The bias point of A_3 ($Vtrip_3$) is not effected if TZ_3 is still high.

Once TZ_3 goes low, a charge of $Qinj_3$ is injected into the input of amplifier A_3. This error is

$$E_3 = \frac{Qinj_3}{C_s}$$ 2.93

Amplifier A_3 amplifies this error voltage and the output of the last stage becomes

$$Vout_3 = Vtrip_3 - A_3 \cdot E_3$$ 2.94

The output of the last stage is not altered by the charge injection induced errors E_1 and E_2 of the first and second stages, respectively. Referring the error at the output of sample data comparator back to the input gives the output error in terms of input voltage levels. This input error is the offset of the sample-data comparator.

$$V_{offset} = \frac{Vout_3}{-A_1 \cdot A_2 \cdot A_3} = \frac{E_3}{A_1 \cdot A_2} - \frac{Vtrip_3}{A_1 \cdot A_2}$$ 2.95

The total error due to charge injection is reduced by the gain factor $A_1 \cdot A_2$. This is typically 100. The net result of staggered auto zero signals is to remove the effects of the charge injection induced errors of the first and second stages, while attenuating the offset of the third stage.

If the switches are opened at the same time,

$$TZ_1 = TZ_2 = TZ_3$$ 2.96

then the error generated by the first stage $(-E_1 \bullet A_1)$ is amplified by the second and third stages. Similarly, the error voltage generated by the second stage $(-E_2 \bullet A_2)$ is amplified by the third stage. The error voltage generated at the output of the third stage is

$$Vout_3 = Vtrip_3 - A_1 \bullet A_2 \bullet A_3 \bullet E_1 + A_2 \bullet A_3 \bullet E_2 - A_3 \bullet E_3 \qquad 2.97$$

Relative to the input, the overall offset of the sample-data comparator with no staggering is

$$V_{offset} = E_1 - \frac{E_2}{A_1} + \frac{E_3 + Vtrip_3}{A_1 \bullet A_2} \qquad 2.98$$

Not only is the charge injection of the first stage not cancelled, but it is also not attenuated. The effect of charge injection on the offset increases significantly when the auto zero switches are not staggered.

2.6.3 Programmable Delay Staggered Auto Zero Signals

Once charge is injected into the input node of an amplifier, the amplifier responds by generating an output error voltage. This output voltage is a replica of the input error voltage scaled by the gain of the amplifier. The amplifier stage requires a settling time τ_s, in order to generate the stable output error voltage. During this time, the output of the comparator is changing from its DC bias point to the final error induced bias point. This error voltage is coupled to the input of the second amplifier stage. If the second stage auto zero signal (TZ_2) goes low before the first stage amplifier has settled, then complete charge injection cancellation will not occur. The extent of offset cancellation is a function of the delay between auto zero signals relative to amplifier response times.

The delay between auto zero signals must be larger than the settling time of the amplifier.

$$\tau_d > \tau_s \qquad 2.99$$

If the delay time is not sufficient, then V_{offset} will be some value between those predicted in equations 2.95 and 2.98.

The delay between auto zero signals is typically generated with several inverters. The signal delay induced by inverter stages does not track the small signal response time of the amplifier stages. The inverter delay varies over temperature, process, and supply voltage independently of the amplifier response time. Unless the inverter delay is made excessively large, cases exist where the delay is too short to completely cancel the charge injection effects of the first and second stages. This results in offset variations as the temperature, supply, or process is altered.

One alternative is to use many inverter stages to guarantee worst case delays are much larger than amplifier response times. The problem with this approach is the excessive delays lead to reduced speed performance of the comparator. In circuits requiring high speed

sampling, this excessive delay will become the limiting factor in the overall speed of the circuit. The acquisition time is increased by $2 \bullet \tau_d$.

A second alternative is to design a bias controlled delay circuit with constant delay over temperature, supply voltage, and process. By externally trimming the bias circuit, various delays from excessive to minimum can be tested in order to determine the delay vs. offset variation. From this data, an optimum bias point can be established such that maximum speed can be achieved with minimum offset variations.

2.6.4 Supply Independent Swing

If the signals driving the auto zero switches are swinging from rail to rail, the overall charge injection is a function of the supply voltage (see equation 2.17). Many times a constant offset of a system can be cancelled if enough data is analyzed, but offset variations over supply voltage cannot easily be cancelled. Instead of driving the auto zero switches with signals swinging rail to rail, a supply independent swing from V_{bias} to 0v can eliminate offset drifts with respect to supply voltage. The only constraint on V_{bias} is that it be sufficiently large enough to insure the N-channel feedback switches are on. When driven with a signal swinging from V_{bias} to ground, the MOS switches induced charge injection becomes

$$Q_{inj} = C_{gs} \cdot V_{vias} + \frac{Cox}{2} \cdot (V_{bias} - V_{TE})$$

2.100

thus eliminating all first order effects of supply voltage.

3.0 Methodology

3.1 process

A 1μ, N-well, double metal CMOS process was used in the characterization of charge injection.

The MOS gates are self aligned poly (poly before diffusion) with a minimum channel length (L) of 1μ. This process is described in more detail by cacharelis [17]. Table 3.1 lists typical key process parameters of the MOS devices, capacitors, and parasitic elements.

In addition to the P-channel and N-channel MOS devices, This process also contains a poly diffusion capacitor. The capacitor area is defined by poly which is the top plate. The capacitor dielectric is a process controlled silicon dioxide growth between the N+ diffusion bottom plate and the poly top plate. The terminals of the device are defined by contacts made to the poly and N+ implant. Aluminum is then used as the interconnect layers.

The poly-N+ capacitors are commonly used in MOS analog-to-digital converters as storage and ratiometric capacitors. The matching between capacitors is more important than their absolute value. It is this matching which limits the resolution in capacitive redistribution ADC's.
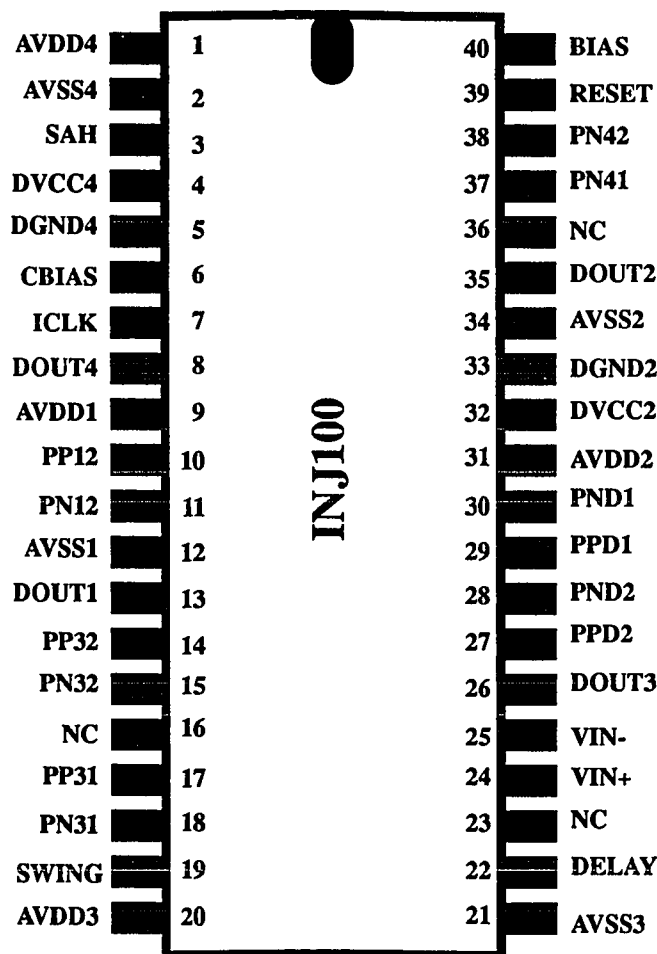
TABLE 3. 1 Typical Device Process Parameters

PARAMETER	Typical Value	Description
V_{TP}	-1.113 V	P-channel threshold voltage
γ_p	-0.0456 $V^{1/2}$	P-channel body effect coefficient
C_{ox}	1.73E-15 F/μ^2	P-channel gate oxide capacitance
β_p	2.15E-5 A/V^2	$\mu_p \cdot C_{ox}$
λ_p	0.371	Early voltage (SPICE Level 3)
L_D	0.07	P-channel Lateral Diffusion
V_{TN}	0.808 V	N-channel threshold voltage
γ_n	0.126 $V^{1/2}$	N-channel body effect coefficient
C_{ox}	1.73E-15 F/μ^2	N-channel gate oxide capacitance
β_n	7.3E-5 A/V^2	$\mu_n \cdot C_{ox}$
λ_n	0.0463	Early voltage (SPICE Level 3)
L_D	0.10	N-channel Lateral Diffusion
$C_{1,2}$	0.049E-15 F/μ^2	Metal1 to Metal 2 inter layer capacitance
C_c	0.822E-15 F/μ^2	Poly-Diffusion Capacitor

3.1.1 Test Chip Overview

In order to analyze the effects of charge injection relative to analog-to-digital converters, single ended and differential 3-stage sample-data comparators have been designed, simulated for functionality, and fabricated. Figure 3.1 shows the pin out of the complete test chip. The test chip contains two single-ended comparators (comp1 and comp2) and two differential comparators (comp3 and comp4).

	INJ100	
AVDD4	1	40 BIAS
AVSS4	2	39 RESET
SAH	3	38 PN42
DVCC4	4	37 PN41
DGND4	5	36 NC
CBIAS	6	35 DOUT2
ICLK	7	34 AVSS2
DOUT4	8	33 DGND2
AVDD1	9	32 DVCC2
PP12	10	31 AVDD2
PN12	11	30 PND1
AVSS1	12	29 PPD1
DOUT1	13	28 PND2
PP32	14	27 PPD2
PN32	15	26 DOUT3
NC	16	25 VIN-
PP31	17	24 VIN+
PN31	18	23 NC
SWING	19	22 DELAY
AVDD3	20	21 AVSS3

FIGURE 3.1 Pin Out of the INJ100 Test Chip

Analog power and ground are isolated for each comparator. AVDD1 and AVSS1 tie to analog V_{dd} and ground of comparator1. Similarly, AVDD2, AVDD3, and AVDD4 tie to power of comparators 2,3, and 4. AVSS2, AVSS3, and AVSS4 are the analog ground connections of the comparators. DVCC4, DVCC2, DGND4, and DGND2 are the digital power and ground pins driving the digital control logic.

The signal SAH is an external clocking signal controlling the duration of the acquisition of the input voltage. ICLK is an externally applied signal used to strobe the internal

sense amplifiers. **RESET** is an external signal required by the internal control circuitry used to reset the chip. These signals are common to all four comparators.

The **CBIAS** pin is used to set the bias current in the differential comparator. This pin is driven by an external voltage source. The **DELAY** pin controls the bias current of the programmable delay circuit; hence, it controls the delay time between auto zero signals. **Vin+** and **Vin-** are the analog input voltages shared by all four comparators. **Vin+** is sampled when **SAH** is a "1", and **Vin-** is sampled once **SAH** goes low.

Each comparator has its own digital output corresponding to the magnitude of the input voltage. **DOUT1, DOUT2, DOUT3,** and **DOUT4** are these outputs. PN_{xy} and PP_{xy} are probe circuits tied to internal comparator nodes, where x corresponds to the comparator number and y is the stage (1, 2, or 3) it is tied to. PPD_x and PND_x are internal probes tied to the output of delay circuits. These probes are used to monitor the delay time between auto zero signals. The **SWING** pin controls the swing of the auto zero signals, the external voltage applied to this pin is the value of the gate voltage when the feedback switch is on.

3.2 Circuits

3.2.1 Single Ended Comparator

As shown in figure 3.2, the single ended comparator consists of 3 gain stages capacitively coupled together. Each of these stages are inverter type comparators with feedback switches for biasing to the trip-point. These feedback switches have a channel width and length of 20μ and 3μ, respectively. The size of the feedback switch is larger than typically required to increase the charge injection, thus dominating the offset errors. The coupling capacitors are 0.5 pF.

The output of the last stage is fed into a sense amplifier whose purpose is to latch the output of the comparator. A reference input to the sense amplifier is generated by forcing an inverter identical to that of the third stage to always output Vtrip. Ideally, for V_{in}=0v, the comparator output (Vinp) will be equal to the generated reference voltage (Vtrip). If the input to the comparator (V_{in}) is slightly increased, then the three stage comparator will push Vinp lower than Vtrip (Vinn). Once strobed, the sense amplifier will output a "1" if Vin is positive. For a decrease in the input (V_{in}), the comparator will force Vinp to increase above Vtrip resulting in Dout="0".

For V_{in}=0v, the sense amp will flip to either a "0" or a "1". Although there is no input, charge injection will generate error voltages on the internal storage nodes. This will drive the output of the comparator high or low depending on the sign of the charge injection.

Programmable delay circuits are used between the auto zero signals. By adjusting the externally controlled bias voltage (the DELAY pin) then measuring the time delay between the signals at the PND1 and PND2 pins, a known delay is forced between auto zero signals (see figure 3.3). The overall comparator offset can be determined by ramping V_{in} up until the output of the sense amp begins to toggle from "0" to "1". The exact comparator offset is determined by monitoring the sense amplifiers output (Dout). The offset is equal to the input voltage required to change the output (Dout) to a "1" 50% of the time and a "0" 50% of the time. By observing the output signal (Dout) on the scope the offset is determined. When the intensity of a "1" is equal to the intensity of a "0", $V_{in}+ = E_{in}$ where E_{in} is the charge injection induced offset. This point is determined by setting $V_{in}- = 0$v. The input voltage required to achieve toggling in the sense amplifier is the charge injection induced offset voltage.

The delay is varied from 0ns to 100ns in order to determine the offset vs. delay of the comparator. At 0ns staggering does not exist, while 100ns is an excessive delay much larger then the comparator settling time. This data is gathered at various temperatures and supply voltages. Temperature sensitivity of the offset and PSRR can be determined at various delays.

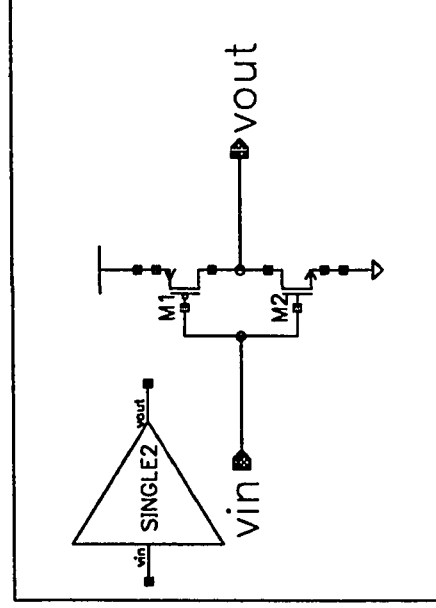Figure 3.2 Single Ended Comparator Schematic
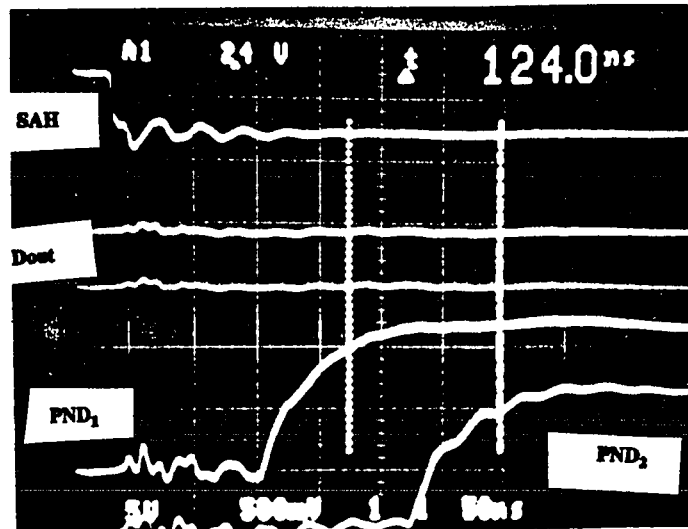
FIGURE 3.3 Oscilloscope Photo of Toggling Sense Amplifier output

The input of each stage also has a dummy device for clock feed through cancellation. These devices can be removed by a laser trim link. When the device is attached, clock feed through is compensated (see equation 2.86). Complete cancellation does not occur because channel charge is not completely cancelled (equation 2.88). Measuring the offset with and without the dummy device, the staggering cancellation effects are analyzed relative to channel charge injection and clock feed through.

The delay circuit's output drives the feedback switch. Typically, this signal swings from V_{dd} to 0v. In this case, the signals driving the feedback switches and dummy devices swing from SWING to 0v. The SWING signal can either be V_{dd} or Vbias; where Vbias is a constant with respect to V_{dd}. By externally controlling the SWING pin and varying V_{dd} from 4.5v to 5.5v, the PSRR can be monitored with and without constant auto zero swing. The forced voltage swing on the feedback switches, SWING=Vbias, should significantly decrease the PSRR for all auto zero delays.

There are two different 3-stage single-ended comparator structures on the test chip. The first (figure 3.2) uses a single1 inverter on the first stage and single2 inverters on the second and third. Single1 and single2 are identical circuits except their device sizes differ (see figure 3.4). The second 3-stage single-ended comparator consists of single1 inverter in all three stages.
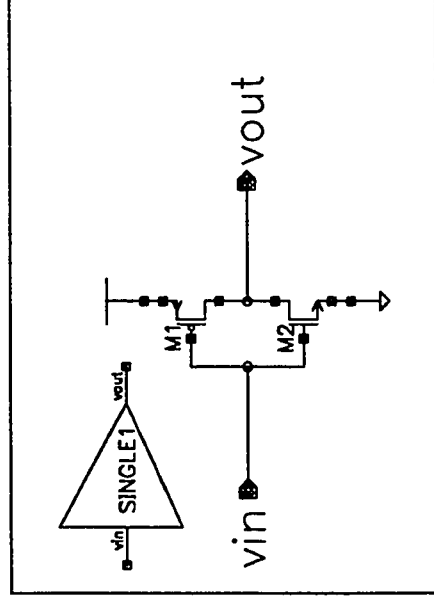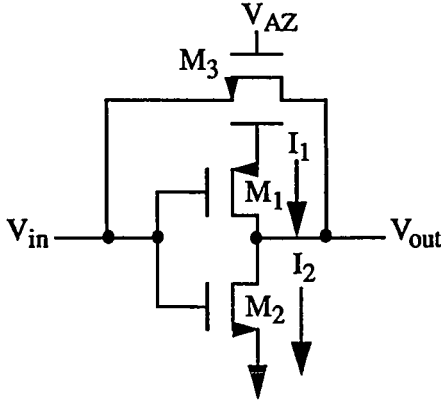
SINGLE2

SINGLE1

Figure 3.4 Single Ended Comparator Stages

Single1 and single2 are CMOS inverter structures. As shown in figure 3.5, the CMOS inverter is a push-pull type structure consisting of a P-channel device (M_1) used to pull Vout to V_{dd} and an N-channel device (M_2) used to push Vout to ground. M_3 is the feedback switch used to auto zero the amplifier.

FIGURE 3.5 CMOS Inverter Amplifier Stage (Single1 and Single2)

When the auto zero switch (M_3) is on (V_{AZ}=SWING), the output of the inverter is forced equal to the input of the inverter. At the bias point Vout=Vin, both transistors M_1 and M_2 are in the saturation region of operation

$$|V_{ds}| \geq |V_{gs}| - |V_T|$$

3.1

where V_{ds} is the drain to source voltage, V_{gs} is the gate to source voltage and V_T is the threshold voltage. The saturation current of an MOS device is

$$I_{sat} = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} (V_{gs} - V_T)^2$$

3.2

where μ is the mobility, C_{ox} is the gate to channel capacitance per unit area, and W/L is the device geometric dimensions. When Vout=Vin, M_1 has a saturation current of

$$I_1 = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} (V_{dd} - V_{in} - V_{TP})^2$$

3.3

and M_2 has a saturation current of

$$I_2 = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} (V_{in} - V_{TN})^2$$

3.4

Assuming no current flows out of the inverter and applying KCL to node Vout,

$$I_1 = I_2 \tag{3.5}$$

Substituting 3.3 and 3.4 into 3.5 and solving for V_{in}, the trip-point becomes

$$V_{in} = \frac{\sqrt{\mu_p \cdot \frac{W_1}{L_1} / \mu_n \cdot \frac{W_2}{L_2}} \cdot V_{dd} - V_{TP} - V_{TN}}{1 + \sqrt{\mu_p \cdot \frac{W_1}{L_1} / \mu_n \cdot \frac{W_2}{L_2}}} = V_{trip} \tag{3.6}$$

As W_1/L_1 is increased, V_{trip} increases; conversely, as W_2/L_2 increases V_{trip} decreases. By ratioing the device dimensions of M_1 and M_2, infinite trip points are possible, limited to the constraint that both transistors remain in the saturation region of operation for maximum gain (equation 3.1). The trip-point (V_{trip}) is also dependent on the supply voltage (V_{dd}). Since V_{trip} is the potential voltage at both the source and drain of the feedback switch (M_3), the effective threshold of M_3 changes as the trip point changes due to body effect. Therefore, the channel charge injection given by equation 2.12 page 10 changes as V_{trip} changes. This results in a PSRR error even if the voltage swing driving M_3 is independent of V_{dd}.

At this point, it is unknown wether the V_{dd} sensitivity (PSRR) is dominated by supply dependence of the auto zero swing or effective threshold shift of the feedback switch due to supply dependent trip points. Using the forced voltage swing of auto zero signals, the two cases can be isolated for individual analysis.

Once the CMOS inverter has been biased to V_{trip}, the voltage is stored on the coupling capacitor at the input of the comparator stage. The inverter is now in its high gain region of operation. For small signal changes in the input voltage, the output will respond with an inverted amplified version corresponding to that input.

Figure 3.6 shows the small signal equivalent circuit of the CMOS inverter amplifier.
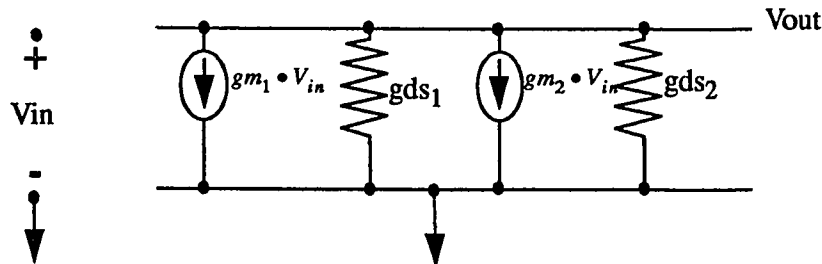
FIGURE 3.6 Small Signal Equivalent of CMOS Inverter

The gain of this circuit (V_{out}/V_{in}) is

$$gain = \frac{V_{out}}{V_{in}} = \frac{gm_1 + gm_2}{gds_1 + gds_2}$$

3.7

where the transconductance (gm) of a saturated MOS device is

$$gm = \sqrt{2 \cdot \mu \cdot \frac{W}{L} \cdot I_D}$$

3.8

The output transconductance (gds) is a function of the *early voltage* (λ) and the bias point (I_D)

$$gds = \lambda \cdot I_D$$

3.9

Empirically, λ increases as the channel length increases. Substituting 3.8 and 3.9 into 3.7, the small signal gain of a CMOS inverter becomes

$$gain = \frac{\sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \frac{W_2}{L_2} \cdot I_D} + \sqrt{2 \cdot \mu_p \cdot C_{ox} \cdot \frac{W_1}{L_1} \cdot I_D}}{(\lambda_1 + \lambda_2) \cdot I_D}$$

3.10

For single1, the channel lengths are 2μ while single2 has channel lengths of 4μ. Since Single2 has a longer channel length, its early voltage will be larger than that of single1. Single1 is a scaled down version of single2. Its W/L ratios are larger then the W/L ratios of single2; hence, its bias current (I_D) is larger for a given trip point. Furthermore, all parasitic capacitances related to single1 are smaller due to overall geometric reductions. Since single1 has a larger bias current and smaller early voltage levels, its gain is less than that of single2, but the combination of increased bias current and reduced parasitic capacitance decreases its response time.

By reducing the gain, the error cancellation given by equation 2.98 is less thereby increasing the charge injection induced offsets relative to the input voltage levels. Since stage2 has a larger gain than stage1, the error cancellation of stage2 will be larger. However, the settling time of stage1 is faster than stage2 resulting in less required delay time between staggered auto zero signals.

The comparator structure of figure 3.2 consists of a first stage high speed amplifier (stage1) followed by two high gain amplifiers (stage2). Since the dominate charge injection occurs on the first stage input node (see equation 2.98), the high speed first stage reduces the required auto zero delay while the high gain second stage reduces the charge injection.

The second single-ended comparator structure consists of three high speed stages (stage1). While the overall gain is lower, the response time is faster; therefore, this circuit requires less staggering delay. This type of high speed comparator is typically used in flash type analog-to-digital converters.
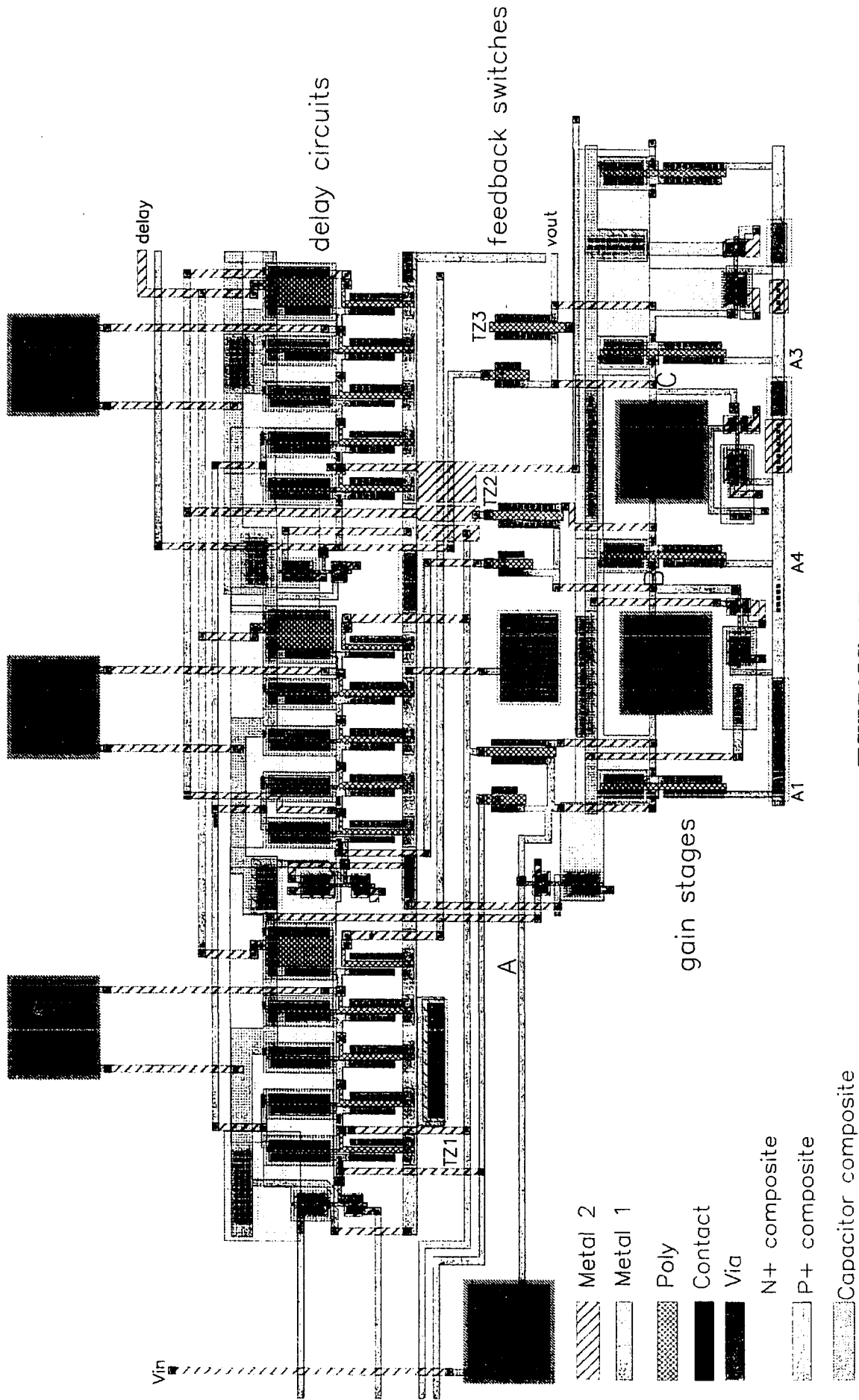
FIGURE 3.7 Single Ended Comparator Layout

Vin

delay

delay circuits

feedback switches

vout

TZ3

TZ2

TZ1

A

C

A3

A4

A1

gain stages

Metal 2
Metal 1
Poly
Contact
Via
N+ composite
P+ composite
Capacitor composite

As shown in figure 3.7 the layout of the single ended amplifier consists of three gain stages capacitively coupled together with delay stages between their auto zero switches. In order to avoid excessive offset errors, metal lines A, B, and C must not be crossed by any clock lines. Observing the layout, the only lines crossing these are static power and ground. Charge injections originates from the source of the feedback switches and the dummy devices driving nodes A, B, and C.

3.2.2 Differential Comparators

Figure 3.8 shows the differential 3-stage comparator structure. This is identical to the single ended architecture except the single ended amplifier stages have been replaced with differential structures. A differential structure requires two feedback switches, one from Voutp to Vinn and one from Voutn to Vinp. Both are driven with the same auto zero signal independently biasing both sides of the symmetrical comparator. The trip points, $Vtrip_p$ and $Vtrip_n$ are stored on the 0.5pF coupling capacitors. The first stage comparator's positive input is tied to an analog multiplexer selecting the positive input voltage pin ($V_{in}+$) or the negative input voltage pin ($V_{in}-$), typically tied to ground.

The auto zero signals are staggered with the same delay circuits used in the single ended comparator. The differential output of the third stage ties directly to the sense amplifier inputs. Since the signal is differential, the reference comparator used in the single-ended structure is not required here.

The differential comparator consists of three identical gain stages. The gain stage (see figure 3.9) consists of a differential input pair (M_1 & M_2), a current source (M_7), two diode connected loads (M_3 & M_4), and positive feedback transistors (M_5 & M_6) for increased speed and gain. This circuit is auto zeroed by turning on feedback transistors M_8 and M_9. Once auto zeroing is complete, the switches are simultaneously turned off. Ideally, equal amounts of charge are injected into the gate nodes of M_1 and M_2. Yet due mismatches in the feedback transistors M_8 and M_9, input pair M_1 and M_2, and coupling capacitors C_1 and C_2, an offset is induced.
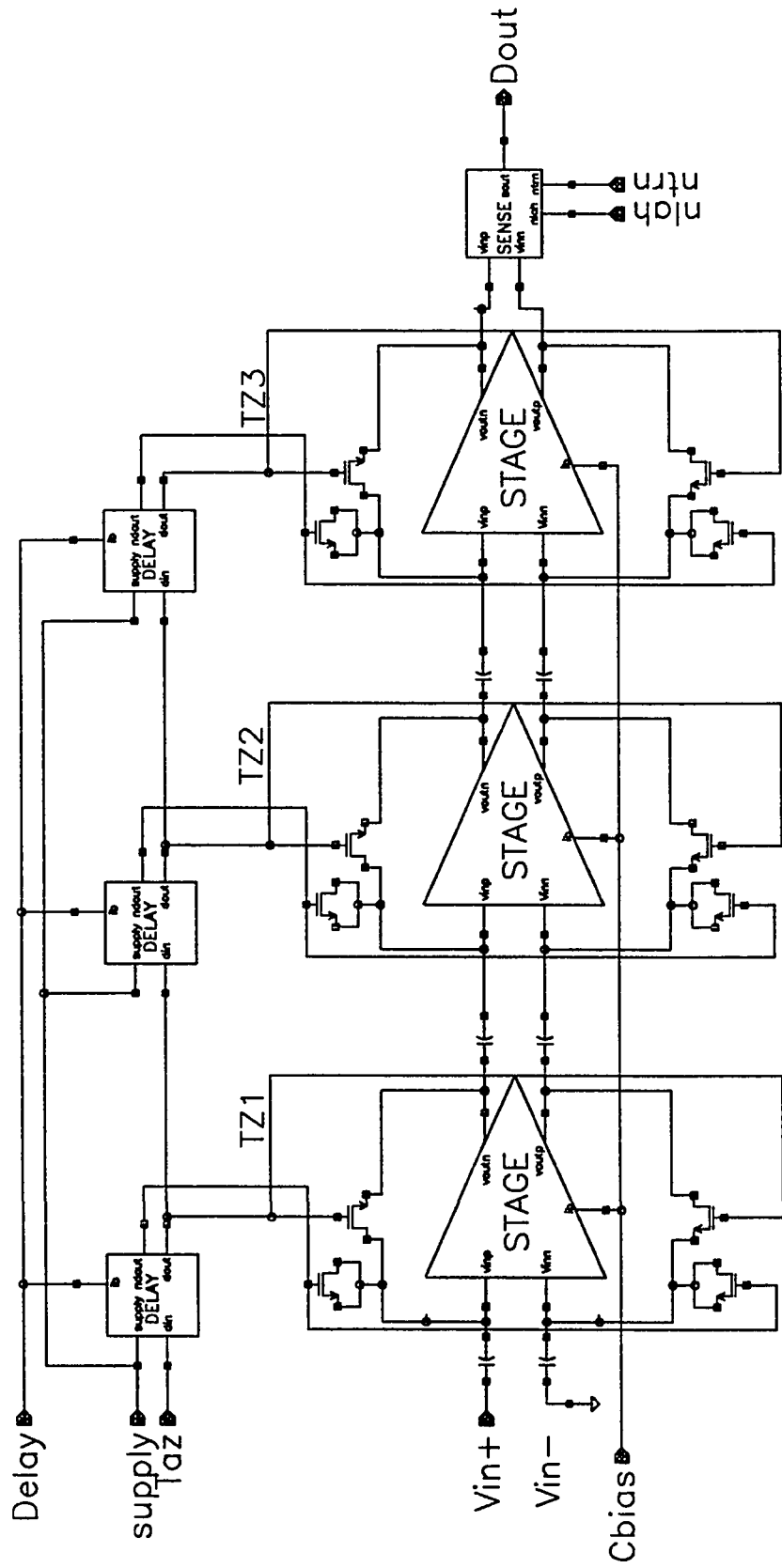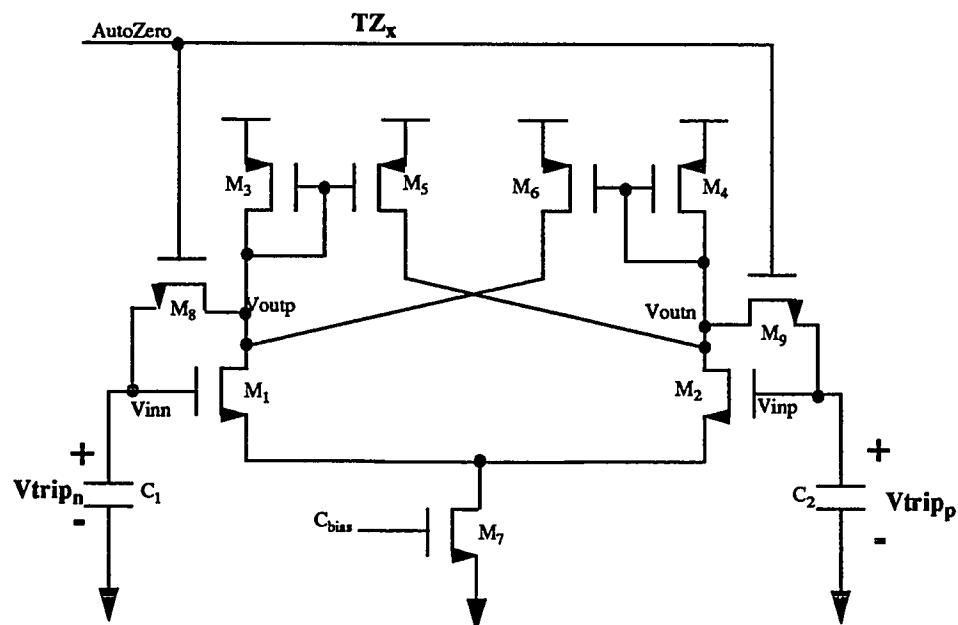
Figure 3.8 Differential Ended Comparator

FIGURE 3.9 Differential Comparator Gain Stage

The DC bias point (V_{trip}) of the comparator gain stage can is found by analyzing the half circuit of figure 3.10, where the drain of M_6 has been tied to voutp. This assumption is valid if $Vtrip_p=Vtrip_n$. Furthermore, the feedback switch is replaced by shorting Voutp to Vinn. The bias current (I_D) is externally controlled by the CBIAS pin.
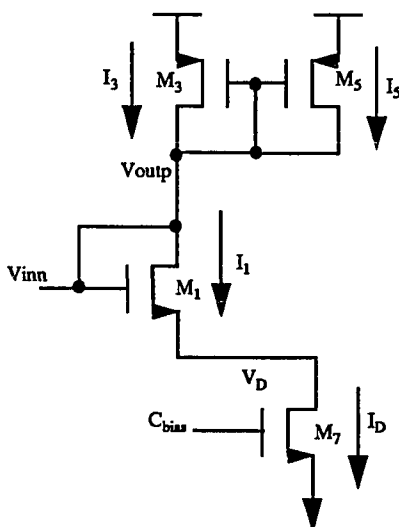
FIGURE 3.10 Half-Circuit Bias Point Model

Assuming all transistors are in the saturation region of operation, and

$$I_D = I_1 = I_3 + I_5 \qquad\qquad 3.11$$

where

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_7}{L_7} (C_{bias} - V_{Tn})^2 \qquad\qquad 3.12$$

$$I_1 = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_1}{L_1} (Vinn - V_D - V_{T1})^2 \qquad\qquad 3.13$$

$$I_3 + I_5 = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W_3 + W_5}{L_3 + L_5} (V_{DD} - Voutp + V_{Tp})^2 \qquad\qquad 3.14$$

Substitution Vtrip for Vinn and Vinp, and equating the currents of 3.12, 3.13, and 3.14, the trip point becomes

$$Vtrip = V_{DD} - V_{Tp} - \beta \cdot (V_{T1} + \alpha \cdot C_{bias} - \alpha \cdot V_{Tn}) \qquad\qquad 3.15$$

where α and β are related to the geometric ratios of the transistors.

$$\alpha = \sqrt{\frac{W_7}{L_7} / \frac{W_1}{L_1}} \qquad\qquad 3.16$$

$$\beta = \sqrt{\frac{\mu_n}{\mu_p} \cdot \frac{W_1}{L_1} / \frac{W_3 + W_5}{L_3 + L_5}} \qquad\qquad 3.17$$

Therefore, the trip-point is dependent on supply (V_{dd}), the externally controlled bias point (C_{bias}), and the device ratios. As **CBIAS** increases, the bias current (I_D) must increase resulting in a reduced trip point.

The half-circuit small signal equivalent circuit of the differential gain stage is shown in figure 3.11.
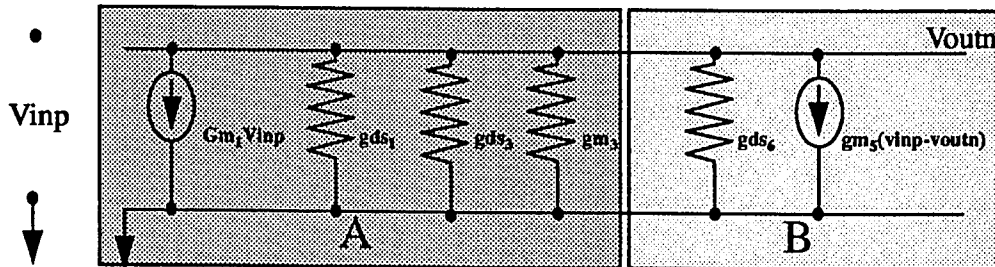
FIGURE 3.11 Small Signal Half-Circuit of Differential Comparator

The *A* section of the above circuit is the open loop gain of the amplifier, while the *B* section represents the positive feedback. The open loop gain (*A*) is determined by transistors M_1 and M_3, and the loading on the output node (Voutn). The open loop gain is

$$A = \frac{Voutn}{Vinp} = \frac{gm_1}{gds_1 + gds_3 + gm_3 + gds_6}$$ 3.18

Assuming gds<<gm, the open loop gain becomes

$$A = \frac{gm_1}{gm_3}$$ 3.19

Therefore, the open loop gain is proportional to the ratio of M_1 to M_3. The actual gain (3.18) decreases as I_D is increased due to an increase in the output transconductance (gds), see equation 3.9.

This amplifier also has a feedback path (*B*). The feedback is due to transistor M_5 of figure 3.9. The gain of the feedback neglecting the output transconductance terms is

$$\beta = \frac{gm_5}{gm_1}$$ 3.20

The separate components of this amplifier can be replaced by a feedback system as shown in figure 3.12.
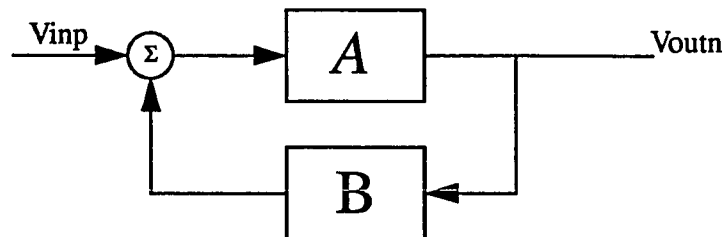
FIGURE 3.12 Feedback system of Differential Half-Circuit

The gain of figure 3.12 is

$$gain \equiv \frac{A}{1 - AB}$$ 3.21

Therefore, the gain of the differential amplifier is

$$gain = \frac{\dfrac{gm_1}{gm_3}}{1 - \dfrac{gm_5}{gm_3}} \qquad\qquad 3.22$$

where the transconductance (gm) is proportional to the device size (see equation 3.8). Since the feedback is positive, stability is achieved by making M_5 geometrically smaller than M_3. For this design, M_5 is 60% smaller then M_3. As the W/L ratio of M_5 is increased towards that of M_3, the loop gain (1-AB) approaches zero (gm_5=gm_3), increasing the overall gain to ∞.

While the offset of the comparator is virtually removed during auto zeroing, the charge injection induced offset results once the auto zero signal is pulled low (see figure 3.13). Mismatches in M_1 and M_2 geometric ratios lead to different trip points for nodes Vinp and Vinn (see equations 3.15-3.17). From equation 2.12 page 10, the charge injection is a function of body effect (γ) and effective threshold voltage, therefore

$$Qinj_1 \propto Vtrip_n \qquad\qquad 3.23$$

$$qinj_2 \propto Vtrip_p \qquad\qquad 3.24$$

Mismatches in the trip point of the positive and negative comparator inputs lead to unbalanced charge injection, and induced offset voltages.
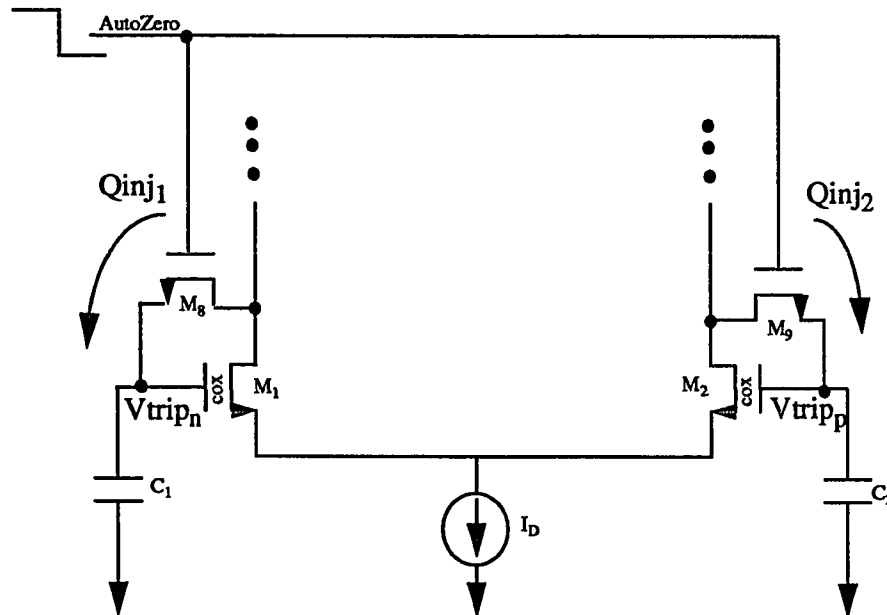
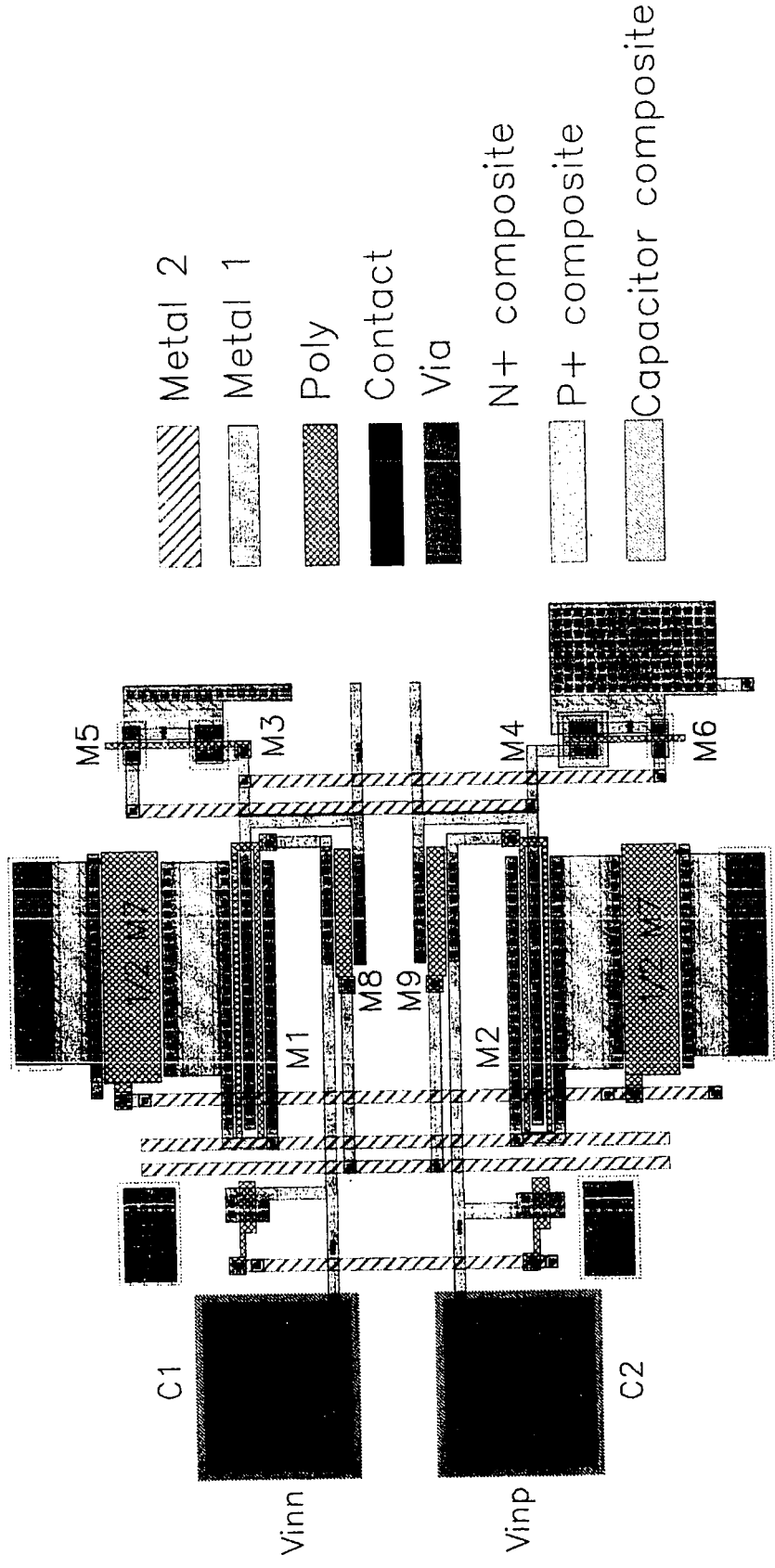**FIGURE 3.13 Charge Injection Induced Offsets in a Differential Comparator**

Figure 3.14 Differential Ended Gain Stage

Legend:
- Metal 2
- Metal 1
- Poly
- Contact
- Via
- N+ composite
- P+ composite
- Capacitor composite

Labels: M5, M3, M4, M6, M1, M8, M9, M2, C1, C2, Vinn, Vinp

The charge injection is also a function of the auto zero transistors (M_8 and M_9) device sizes and gate oxides.

$$Qinj_1 \propto W_8 \bullet L_8 \bullet C_{ox_8} \qquad\qquad 3.25$$

$$Qinj_2 \propto W_9 \bullet L_9 \bullet C_{ox_9} \qquad\qquad 3.26$$

Therefore, mismatches in oxide thickness and device sizes in the feedback transistors lead to charge injection induced offsets.

Mismatches between effective thresholds of M_8 and M_9 lead to an unbalanced channel charge injection contribution to $Qinj_1$ and $Qinj_2$.

A fourth factor contributing to charge injection induced offset voltages is mismatches between the input capacitors C_1 and C_2 and the gate capacitances of M_1 and M_2. The voltage offset generated is proportional to the inverse of the capacitance absorbing the charge (see equation 2.19 page 12). Therefore, the offset of a the differential comparator of figure 3.13 is

$$V_{os} = \frac{Qinj_1}{C_1 + W_1 \bullet L_1 \bullet Cox_1} - \frac{Qinj_2}{C_2 + W_2 \bullet L_2 \bullet Cox_2} \qquad\qquad 3.27$$

Variations in feedback transistor matching, threshold matching, trip-point matching, and input capacitor matching are un correlated; therefore, the offset of a differential comparator is unpredictable. Furthermore, the layout of the comparator is critical in achieving optimum matching. Figure 3.14 shows the layout of the differential ended comparator stage. Symmetry is important in improving matching between the two sides of the comparator. All signal lines crossing the high impedance input nodes have been drawn over both Vinp and Vinn. Parasitic capacitors exist between metal 1 and metal 2 wherever they cross (see table 1). For a symmetrical layout it is necessary to run the auto zero signal lines over the input nodes. If an auto zero line runs over one input, then charge is injected through the metal 2 to metal 1 capacitor to the input node inducing an offset. By running clock lines over Vinp and Vinn, the resulting charge injection is a common mode signal cancelled by the differential pair. However, mismatches in metal 2 to metal 1 capacitors tied to Vinp and Vinn and common mode errors lead to second order errors in the offset.

A complete layout of the 3-stage differential comparator is shown in figure 3.15. Critical to the layout are metal lines A,B,C,D,E, and F. For an optimum layout, these lines must be crossed by auto zero clock lines. In order to cancel the first order effects of coupling between metal 1 and metal 2 parasitic capacitors (see table 3.1), the clock lines where drawn over both positive and negative high impedance input nodes to each gain stage. This reduces the effects of clock coupling by making it a common mode signal.

Dummy devices have been added to both input nodes of the comparator and are driven with the inverse of the auto zero signal. These are used to check the effects of dummy device cancellation of clock feed through. They can be removed by laser trimming in order to determine their effectiveness.
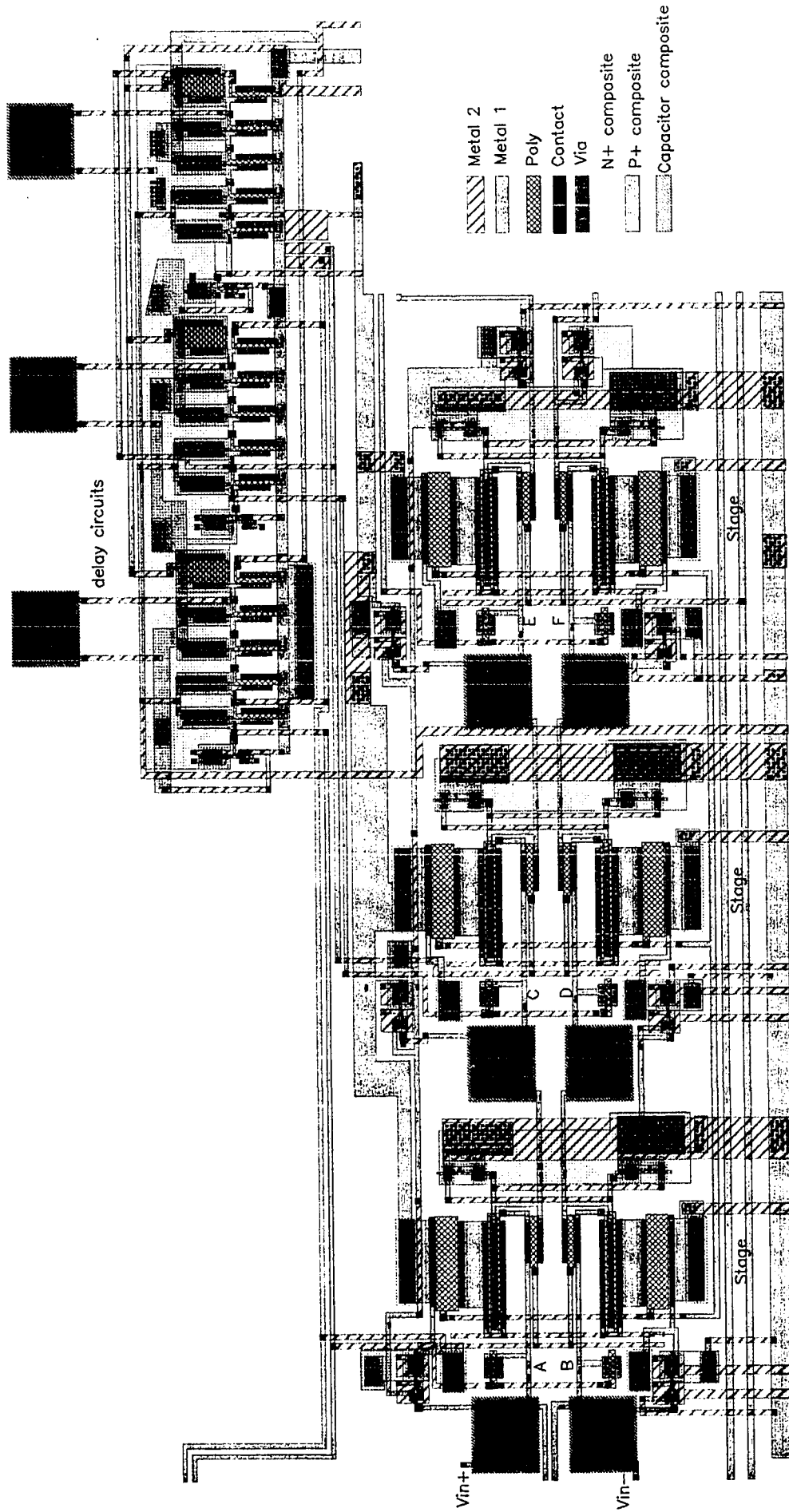
Figure 3.15 Complete Differential Comparator

3.2.3 Forced Charge Injection Circuits

In order to determine the extent that a certain delay is cancelling the charge injection, a separate circuit has been designed to inject a programmable amount of charge into the input of the first stage amplifier, A_1. For the single ended comparator, this metal option serves several purposes (see figure 3.16).
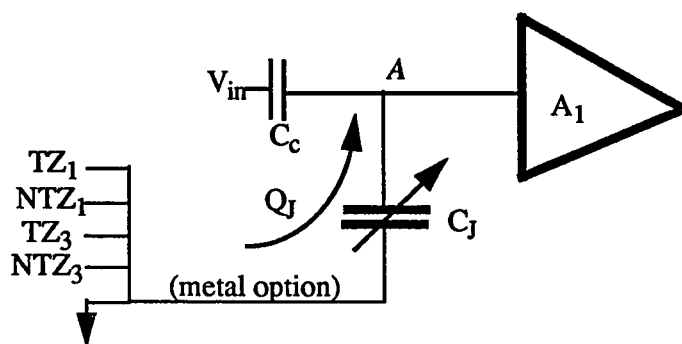
FIGURE 3.16 Forced Charge Injection Single Ended Comparator

The metal option, see layout figure 3.17, ties a laser trim programmable capacitor (C_J) to the input of the first gain stage. This capacitor is then tied to either TZ_1, NTZ_1(the inverse of TZ_1), TZ_3, NTZ_3, or ground. By tying TZ_1 to the capacitor, excess charge is injected into the input of A_1 while the second stage is still auto zeroing. The delay between TZ_1 and TZ_2 can be varied and offset determined. Similarly, NTZ_1 can be tied to the injection capacitor, C_J. Since this signal is out of phase with TZ_1, it will pull charge out of node A. Dependence on the polarity of charge injection will be examined here.

By connecting TZ_3 to C_J, an excess charge will be injected into node A after all the comparators have completed auto zeroing. This will serve as a reference point to determine how much charge injection in terms of offset was cancelled using TZ_1 instead of TZ_3. The difference of these two cases is a measure of the effectiveness of staggered auto zero signals.

By tying C_J to ground, the input capacitance of node A is increased by C_J. The voltage change or offset variation due to a fixed Q_{inj} will reduce as C_J increases. From this data, the magnitude of ΔQ can be determined by varying C_J and measuring the offset.

$$\Delta V = \frac{\Delta Q_{inj}}{C_c + C_J}$$

3.28

To A terminal

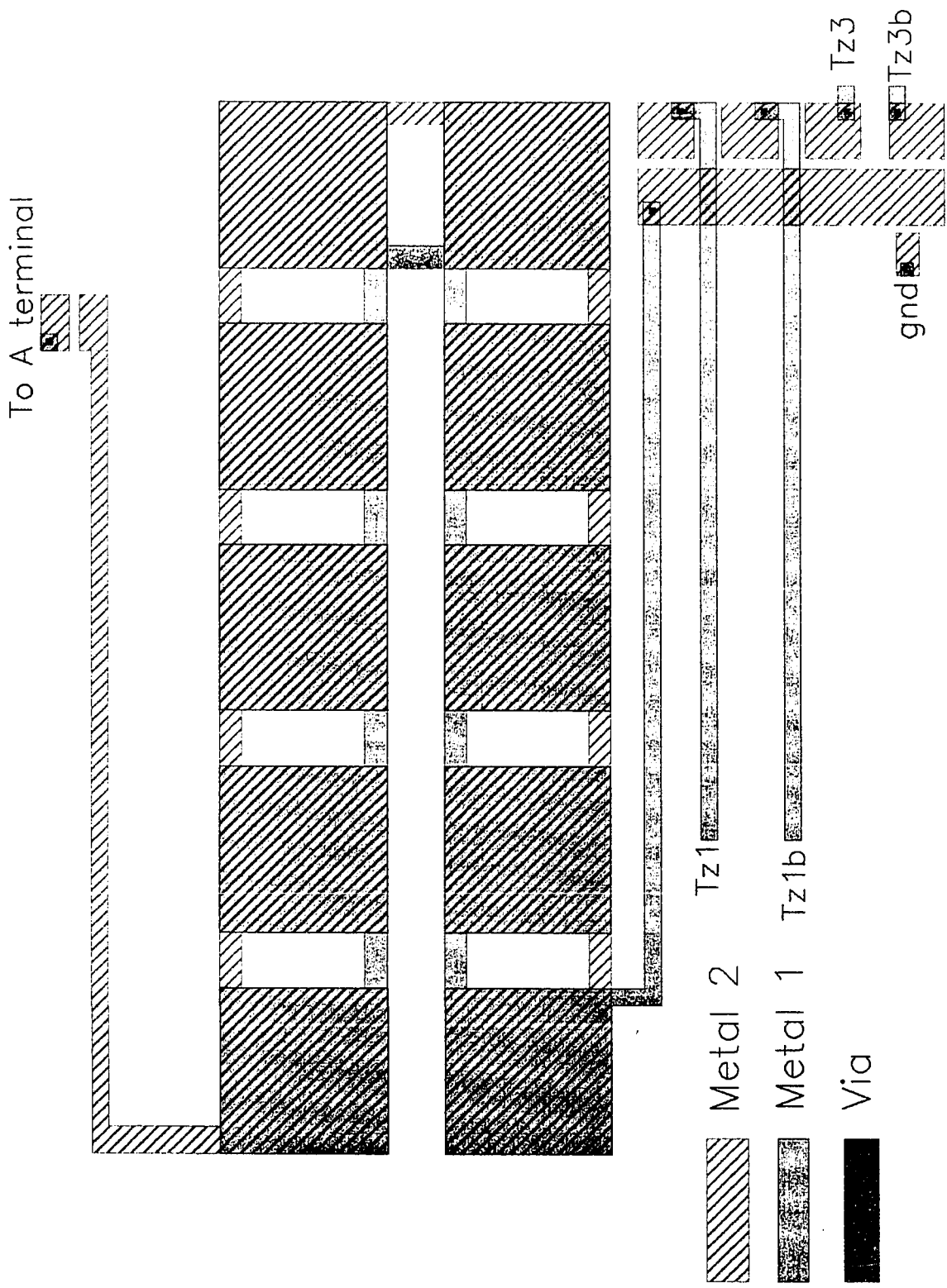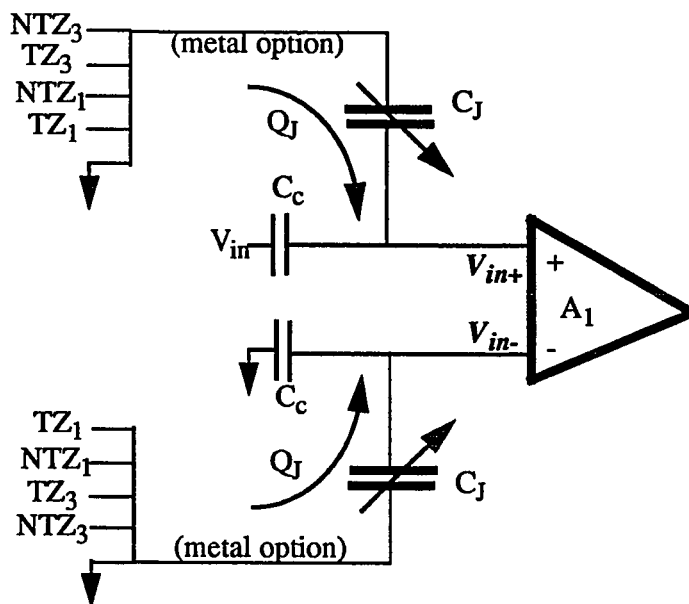Metal 2

Metal 1

Via

Tz1

Tz1b

Tz3

Tz3b

gnd

Figure 3.17 Forced Charge Injection Capacitor

The test chip also includes a differential comparator with two charge injection capacitors (see figure 3.18).


FIGURE 3.18   Forced Charge Injection Differential Comparator

TZ_1 can force charge into either (or both) + and - inputs of the comparator (node $Vin+$ and node V_{in-}, respectively). This charge injection occurs before TZ_2 turns off the second stage auto zero switch, allowing A_2 to cancel the excess charge injection. The magnitude of Q_Z can be controlled by laser trimming the value of C_J. As a reference, the same charge can be injected into either node using TZ_3 thereby eliminating charge cancellation by staggered auto zero signals.

A final experiment is performed by tying one injection capacitor to ground and eliminating the other, see figure 3.19. By doing this, the input capacitance of the first stage becomes unbalanced. If Q_{inj} is the same for both feedback switches, a ΔV_{inj} will exist due to the mismatched capacitor inputs. Measuring the offset as a function of C_J, the magnitude of ΔQ is determined. The information gained by analyzing the effects of mismatched ca-

pacitance is applied to the layout extraction in order to determine how capacitive parasitics effect the comparator offset.
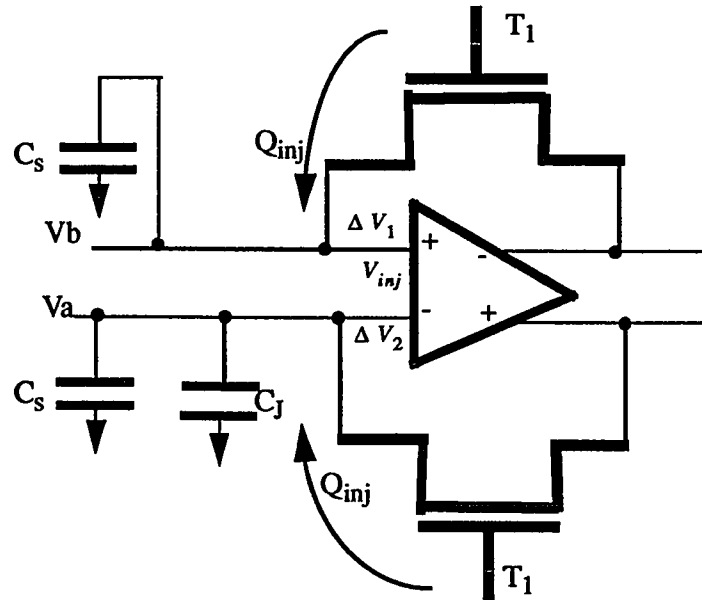
FIGURE 3.19 Charge Injection with Capacitive Mismatch

Each of the charge injection capacitors can be varied from 10% to 50% of the coupling capacitor (C_s) in 10% increments. Variations are done on the bench by laser trimming metal links.

3.2.4 Programmable Delay Circuit

In order to stagger the auto zero signals with a variable delay time, the current controlled delay circuit of figure 3.20 is placed between the auto zero signals driving the first, second and third stages. In this method of eliminating charge injection induced offsets, cascaded inverters have been replaced by the programmable delay stages.

This circuit is designed to have relatively constant delay over V_{dd}, temperature, and process. The magnitude of the delay is proportional to the bias current (I_{delay}) controlled by the external voltage applied to the **DELAY** pin. The delay stage is driven by the auto zero signal of the previous stage. The circuit is non-inverting with nearly zero delay from the rising edge of the input to the rising edge of the output, and a relatively long programmable delay between the falling edge of the input and the falling edge of the output. Therefore, the feedback switches are turned off at different times.
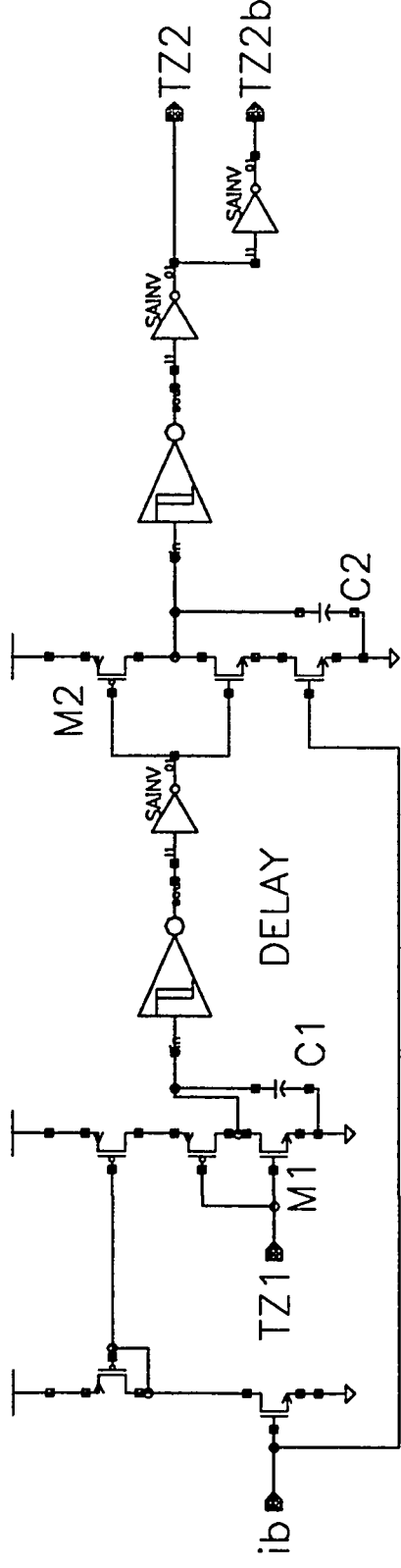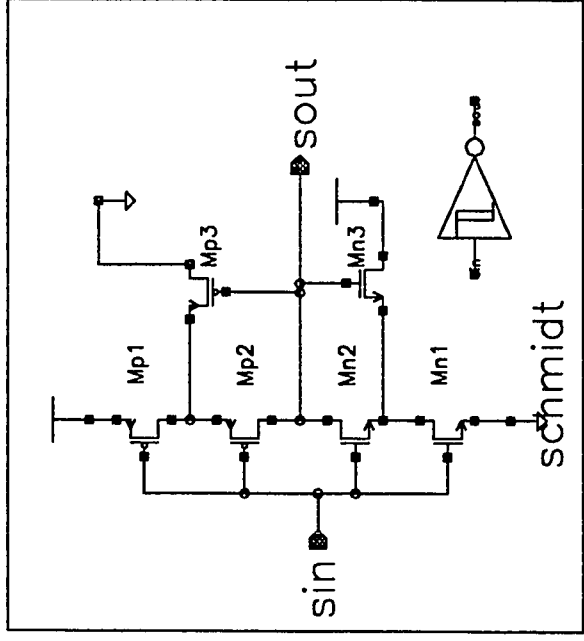
Figure 3.20 Delay Circuit

When the input TZ_1 goes high, Capacitor C_1 is pulled quickly to ground. This signal passes through a schmidt trigger and quickly pulls C_2 to V_{dd}. This signal drives the feedback switch TZ_2. The delay is relatively short compared to the auto zero time; hence, it can be assumed all three stages begin their auto zero time simultaneously. The relative delays between the rising edges of the auto zero signals has no effect on charge injection since all three stages are in the auto zero mode and set to Vtrip after the rising edges of these signals.

The falling edge of the auto zero signals is the critical timing in eliminating charge injection. Since the delay between auto zero signals can reduce charge injection, the falling edge has a wide range of possible delay times from the previous stage falling edge.

Once TZ_1 goes low, the N-channel input device (M_1) turns off. C_1 is charged to V_{dd} by the externally controllable current source. Since the increase in voltage across C_1 is relatively slow, a schmidt trigger is used to sense a threshold level of the voltage across C_1. The schmidt trigger has a hysteresis transfer function (see figure 3.21) with the loop set to 1V. Once the input to the schmidt trigger reaches V_H, the output changes from a "1" to a "0".
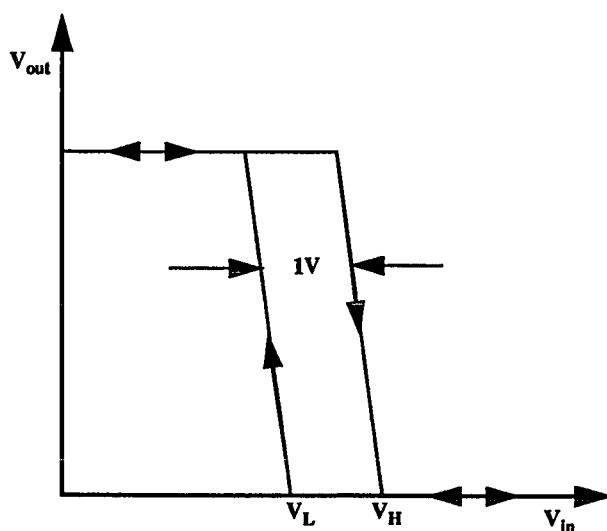
FIGURE 3.21 Transfer Function of a Schmidt Trigger

From the fundamental equation

$$i = C \cdot \frac{dV}{dt}$$ 3.29

The time required to charge the capacitor (C_1) from 0v to V_H is

$$dt = \frac{C_1 \cdot V_H}{I_{delay}}$$ 3.30

Once the voltage level reaches V_H, the schmidt trigger output goes low. This signal is inverted and drives a P-channel device (M_2). The P-channel device turns off allowing the second current source to discharge C_2 from V_{dd} to V_L. Once V_L is reached, the schmidt trigger output goes high. This signal is inverted and becomes a delayed auto zero (TZ_2) with respect to the input auto zero signal (TZ_1). The time required to discharge C_2 from V_{dd} to the trigger level of the schmidt trigger is

$$dt = \frac{C_2 \cdot (V_{dd} - V_L)}{I_{delay}}$$

3.31

If C_1 and C_2 are equal and both stages have the same bias current, then the total delay time from the falling edge of the input signal (TZ_1) to the falling edge of the output signal (TZ_2) is

$$dt = \frac{C}{I_{delay}} \cdot (V_{dd} + V_H - V_L)$$

3.32

The absolute values of V_H and V_L change over process and temperature, but the hysteresis loop (V_H-V_L) is relatively constant. Figure 3.20 shows the schematic of the schmidt trigger circuit. The low and high trip points are

$$V_H = \frac{V_{dd} + \sqrt{\beta_{n1}/\beta_{n3}} \cdot V_{tn}}{1 + \sqrt{\beta_{n1}/\beta_{n3}}}$$

3.33

$$V_L = \frac{(V_{dd} + V_{tp}) \cdot \sqrt{\beta_{p1}/\beta_{p3}}}{1 + \sqrt{\beta_{p1}/\beta_{p3}}}$$

3.34

where V_{tn} and V_{tp} are the threshold voltages of the P and N-channel devices, and β is the W/L geometric ratio of the device. The trigger levels of schmidt trigger are proportional to the geometric sizes and voltage thresholds of the transistors.

In order to reduce the delay times without excessive current (I_{delay}), capacitors C_1 and C_2 are laser trimmable (see layout figure 3.22). By removing C_1 and C_2, the over all delay given by 3.32 is reduced significantly, since the capacitance (C) is reduced to the input capacitance of the schmidt trigger rather then C_1 or C_2.

In order to reduce the auto zero delay times to 0ns, an option exists in the layout to short the auto zero signals together. TZ_1, TZ_2, and TZ_3 are hooked to metal 2 pads separated by minimum spacing. By removing the output of the delay circuit from TZ_2 and TZ_3, then shorting TZ_1 to TZ_2 and TZ_3, all three stages falling edges occur simultaneously. These signals are shorted together using a microscope and microprobe to smear the butter like top layer metal between the oversized TZ_1, TZ_2 and TZ_3 pads. This technique was discovered accidentally in previous work where a V_{dd} bus was smeared into a ground
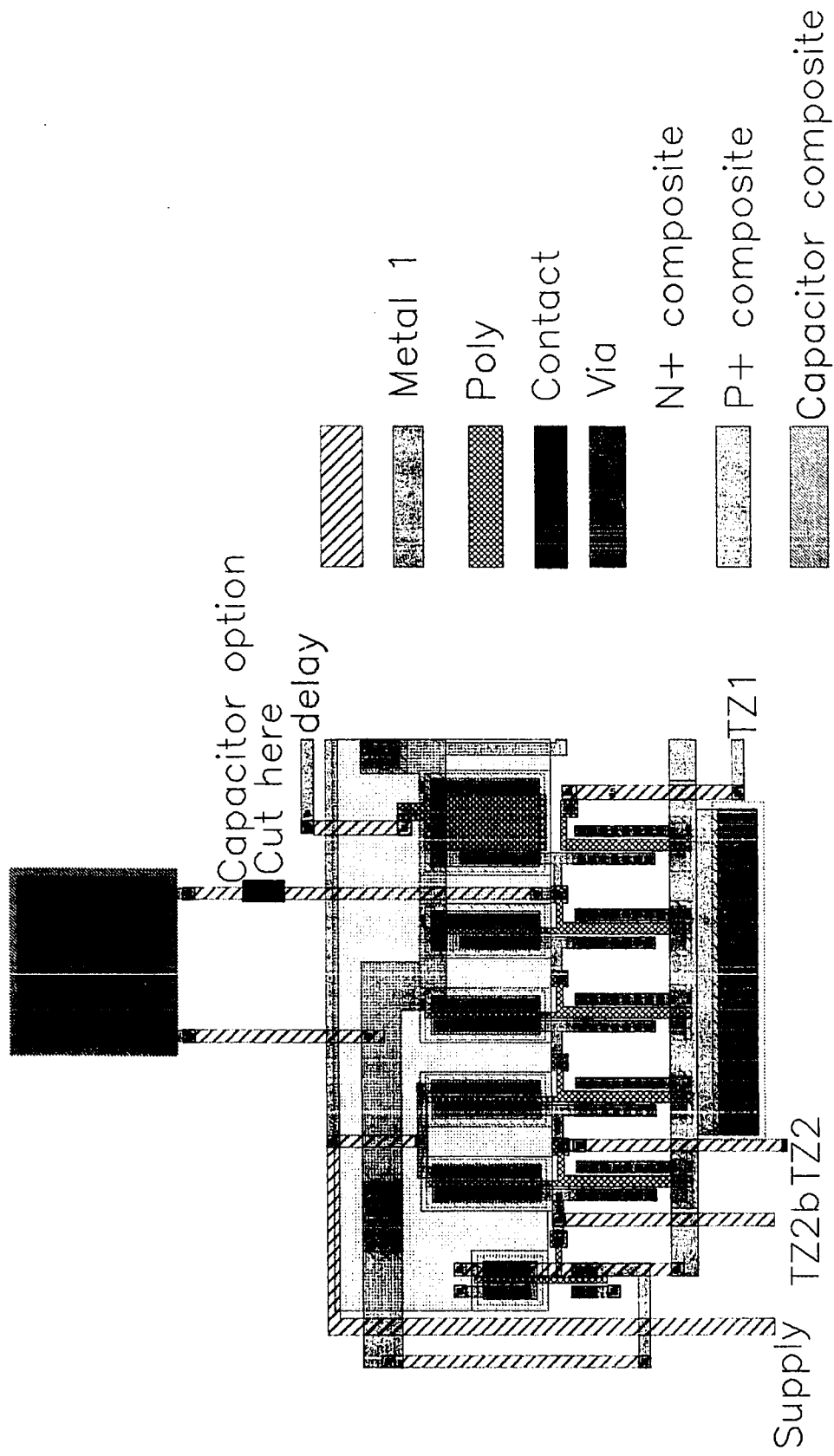
Figure 3.22 Delay Layout

bus. Once power was applied, the lines blew up like a fuse. Since then, this technique has been used purposefully in order to artificially hook two signals together.

3.2.5 Source Follower Probe Circuits

In order to determine experimentally the exact delay time programmed, a source follower probe circuit has been added between auto zero signals and bonded out to external pins. This probe circuit (see figure 3.23) isolates the internal circuits from high capacitance output pins and oscilloscope probes. Separate N and P-channel source follower circuits buffer the high impedance low drive internal nodes from the high capacitance outside nodes without loading effects. External 10KΩ resistors are required as loads for the follower circuits.
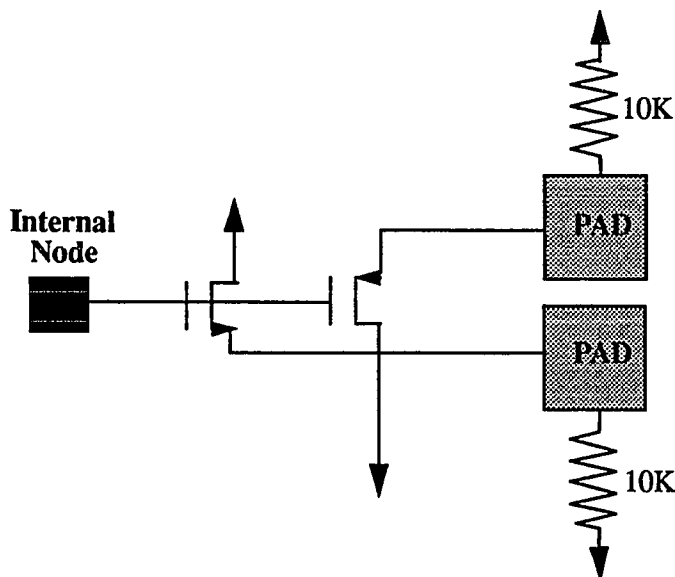
FIGURE 3.23 Source Follower Internal Probe Circuits

Probe circuits have also been added to various internal nodes in the single-ended and differential comparators. Using these probes along with external 10kΩ resistors, charge injection induced voltage changes, inter-stage gain, and trip points can be determined without loading down the internal nodes. If internal nodes were probed directly by microprobes, the capacitance associated would virtually eliminate the ability to measure charge injection since $C_{external\ probe} >> C_{internal\ node}$.

See figure 3.24 for layout of the probe circuit. The entire circuit is covered with a metal 2 probe pad. These follower circuits are added to many internal nodes for debugging the circuit in the event it does not work.
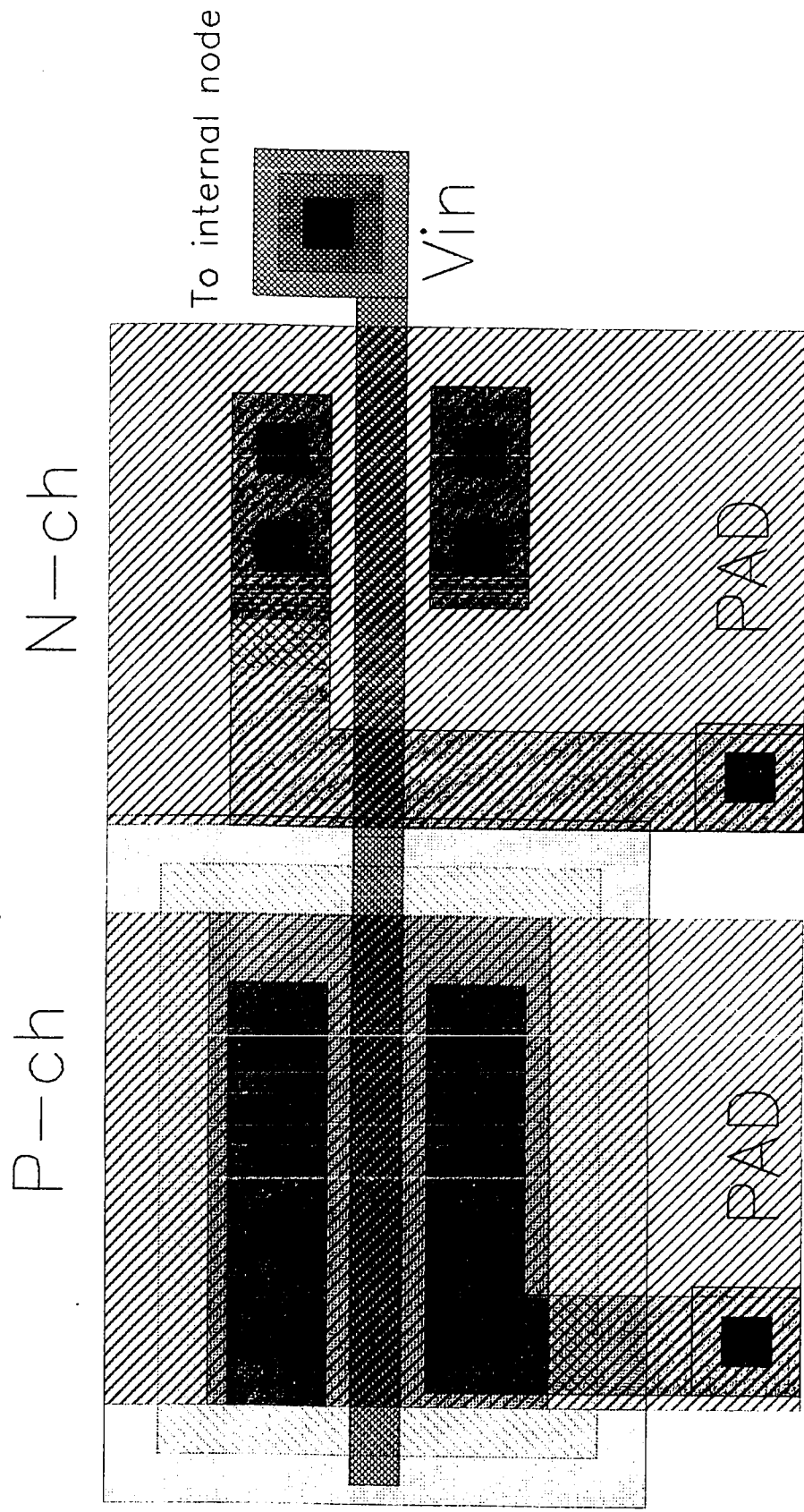
To internal node

Vin
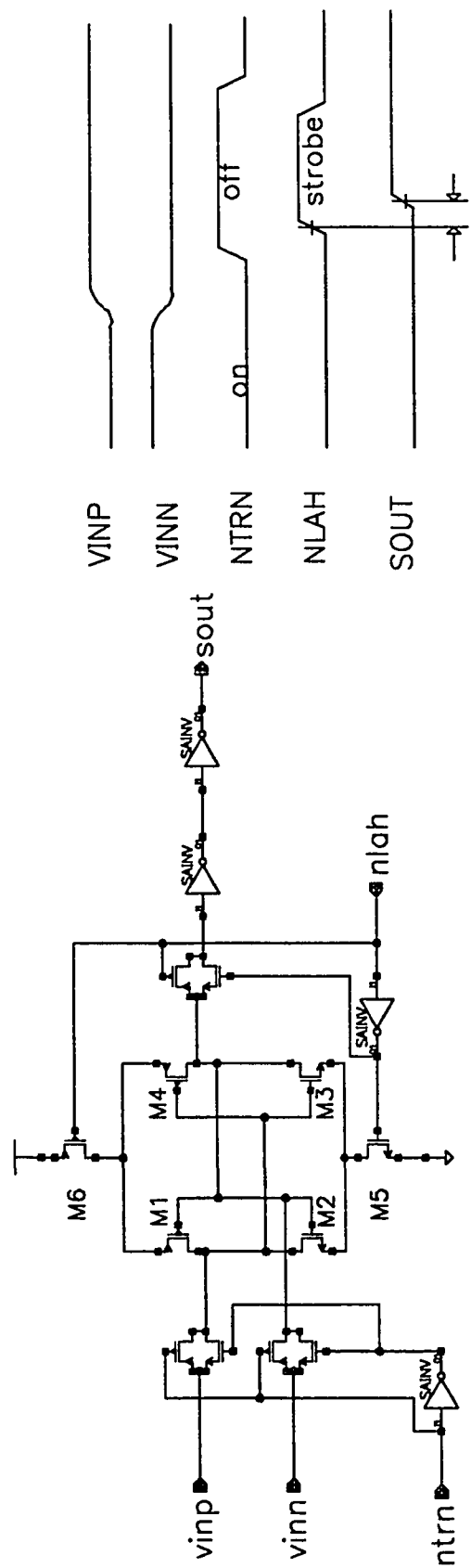
N-ch

P-ch

PAD

PAD

Figure 3.24 Probe Layout

Figure 3.25 sense Amplifier

3.2.6 Sense Amplifier

The comparator outputs drive a sense amplifier. The purpose of the sense amplifier is to determine if the comparator output is a digital "1" or "0". The sense amplifier is required for cases where the input voltages are small. The finite gain of the 3-stage comparator cannot directly drive digital components. The sense amplifier simply senses small differences in comparator output voltage and regeneratively generates a rail to rail signal.

As shown in figure 3.25, the sense amplifier is simply a cross coupled latch. M_1, M_2, M_3, and M_4 make up the latch. Transistors M_5 and M_6 are switches used to enable the regenerative action of the cross coupled latch by allowing current to flow through the inverters from V_{dd} to ground.

The output of the comparator drives the Vinp and Vinn inputs to the sense amplifier. Once the comparator output has settled in response to Vin, the **LAH** signal goes low isolating the sense amp input nodes from the comparator output nodes. At this instance in time, the comparator output is stored on the parasitic input capacitance. After the latch has been isolated from the comparator output, the *stb* signal is enabled allowing the difference in voltage levels across the latch (Vp and Vn) to be regeneratively amplified to V_{dd} or ground.

Regeneration occurs rapidly due to the positive feedback of this circuit. Figure 3.26 shows a detailed block diagram of the sense amplifier, where $M_1 \sim M_4$ have been replaced by inverters I_1 and I_2. M_5 and M_6 have been replaced by switches driven by stb. If the voltage across the parasitic capacitor Cp is slightly larger than that across Cn, Vp will force the output of the inverter I_1 to decrease. As Vn decreases inverter I_2 forces Vp to increase. The increasing Vp forces Vn lower, and so on. This regenerative action continues until Vp and Vn have reached the limits of the supply (V_{dd} and ground). This circuit takes the small signal outputs of the comparator and generates a signal capable of driving logic gates in <5ns. The output of the sense amp is buffered by several inverters gradually increasing in size to drive the external pin of the chip. Externally, the comparator output is seen as a"1"if $Vin > V_{offset}$ or a "0" if $Vin < V_{offset}$.
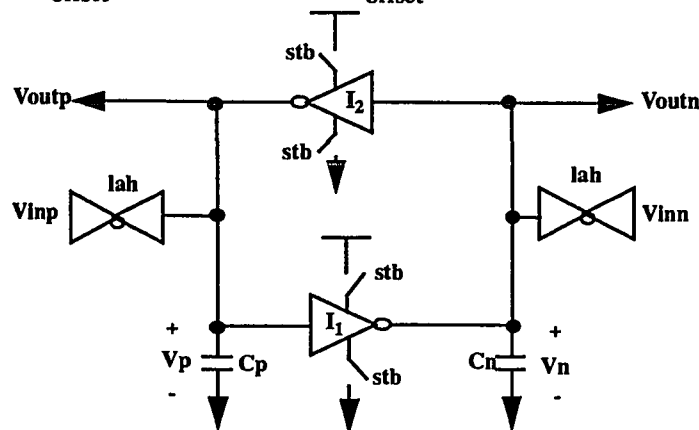

FIGURE 3.26 Simplified Cross-Coupled Sense Amplifier

Figure 3.27 Sense Amplifier Layout

Vinp

Vinn

Metal 2

Metal 1

Poly

Contact

Via

N+ composite

P+ composite

Capacitor composite
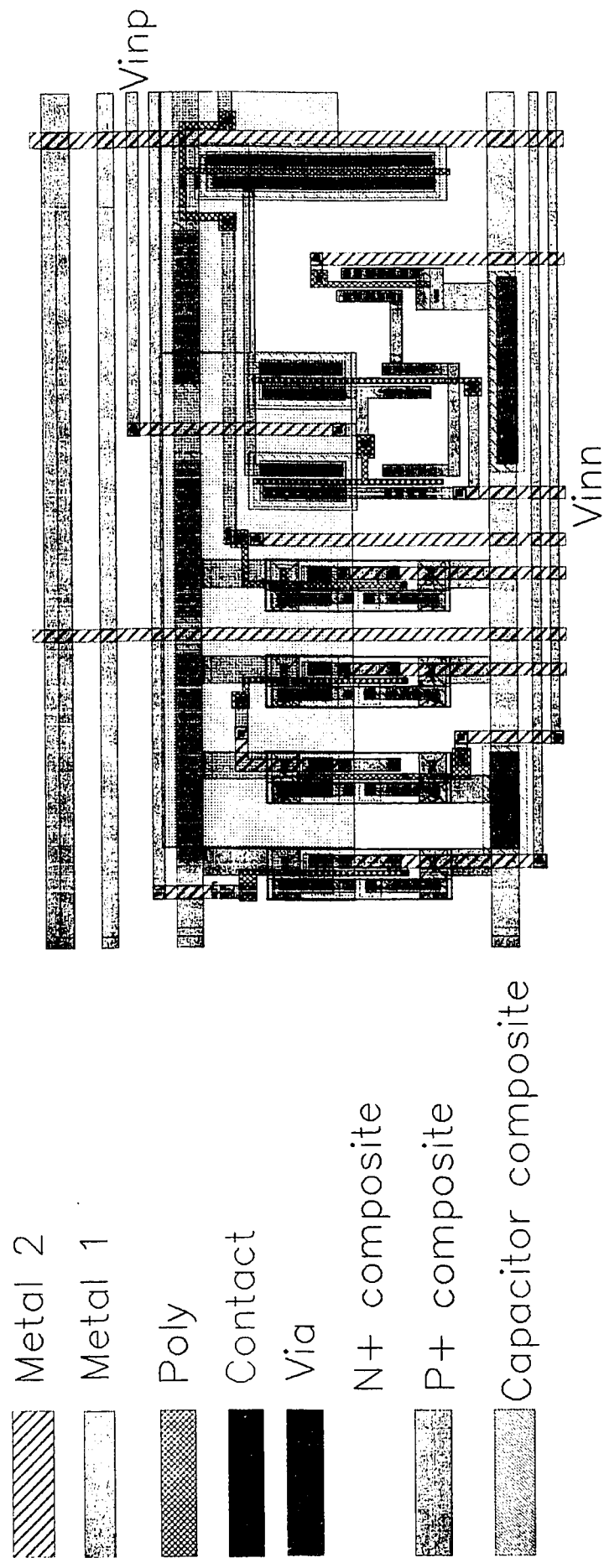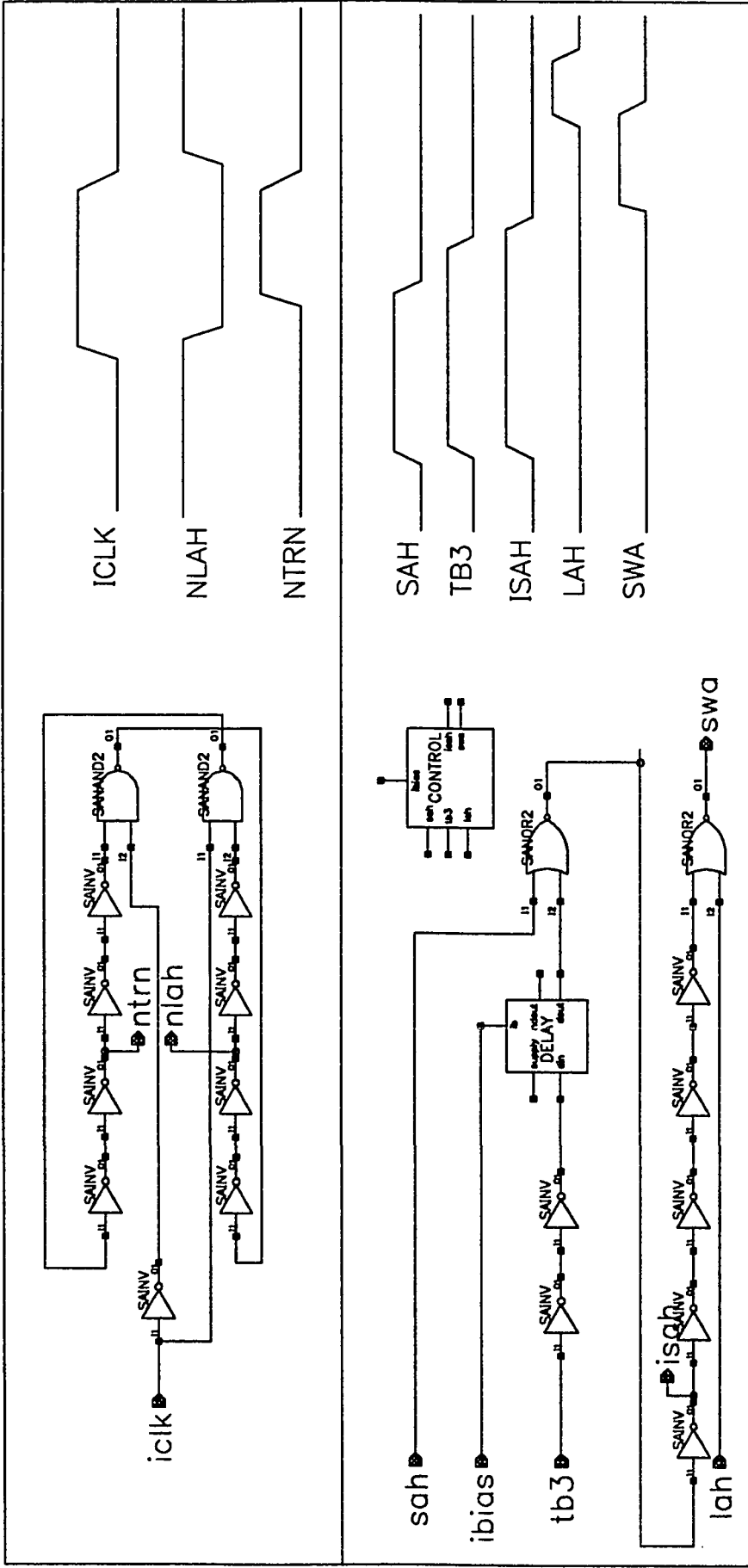
Figure 3.28 Control Logic and Timing

Any offset in the sense amplifier is reduced by the gain of the 3-stage comparator when referred to the input. Since these stages typically have a gain of 1000, the sense amplifier's offset is reduced by 3 orders of magnitude with respect to the input voltage level. The offset of the sense amplifier is due to MOS device mismatches in the symmetrical circuit. These mismatches are not cancelled since the sense amp is not auto zeroed. Figure 3.27 shows the layout of the sense amplifier. This cell was drawn in a modular form to attach easily to the comparator output.

3.2.7 Control

The comparator timing is generated by a digital control circuit (see figure 3.28). Part of the control circuit is responsible for enabling the acquisition of V_{in+}. As shown in figure 3.29, the signals used to sample the positive and negative input voltages are ISAH and SWA, respectively. The input analog signal consists of V_{in+} and V_{in-} (gnd).
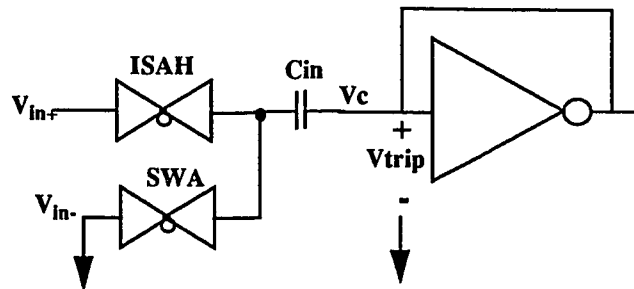
FIGURE 3.29 Input Analog Multiplexer

While *ISAH* is high, V_{in+} is sampled through the transmission gate on the bottom plate of the input capacitor. During this acquisition time, the comparator is biased to its trip point by the auto zero signal. The duration of the acquisition time is externally controlled by a programmable data generator's pulse width and clock frequency. After the acquisition of the positive input signal, the auto zero signal goes low allowing the comparator to enter into its high gain region of operation. The internal delay between auto zero signals begins at the falling edge of this clock. Once all three stages are in the high gain mode, the input is switched from V_{in} to ground. The ISAH signal goes low after the last stage comparator auto zero signal is disabled. Once ISAH goes low, SWA goes high turning on the transmission gate between V_{in-} (ground) and the top plate of the capacitor (Cin). ISAH and SWA must not overlap (both cannot be a logic "1" at the same time) or V_{in+} shorts to V_{in-}.

The input multiplexer switching action results in a net voltage change on the input capacitor (Cin) of

$$dV_c = V_{in} - 0 \qquad\qquad 3.35$$

This voltage change leads to a charge of

$$dQ = V_{in} \cdot C_{in}$$ 3.36

stored in the high impedance input node of the comparator. For an ADC, this charge represents the acquired input signal to be added to or subtracted from based on the algorithm used in the conversion of the input voltage to a digital code. The comparator offset is altered by the charge injected into the input nodes while the MOS feedback switches are turned off.

The net charge stored in the total capacitance at the input to the comparator is altered by the charge injection. This charge raises or lowers the effective trip point of the comparator. For $c_{in} \cdot V_{in} > Q_{inj}$, the comparator output becomes a "1"; furthermore, for $c_{in} \cdot V_{in} < Q_{inj}$, the comparator output becomes a "0". When V_{in} is equal to the comparator offset, its output toggles randomly between "0" and "1" due to zero mean noise. For an ideal comparator, this occurs at $V_{in}=0v$; however, the charge injection altered trip point requires a larger or smaller value of V_{in} to overcome the internal offset.

The timing between the falling edge of ISAH and the falling edge of TZ_3 is critical. If ISAH goes low before TZ_3 goes low, the stored voltage on the input of the comparator is altered by the feedback switch. This results in extreme errors dependent on the time relationship between ISAH and TZ_3. The control circuit uses a delay element between the auto zero signal of the last stage and the falling edge of ISAH (see figure 3.30). Externally, the SAH signal is applied which goes low before TZ_3 goes low. The SAH signal drives the auto zero switch of the first stage. Its falling edge is delayed under external control. This delayed signal drives the second stage. The ISAH signal is the combination of SAH and TZ_3.
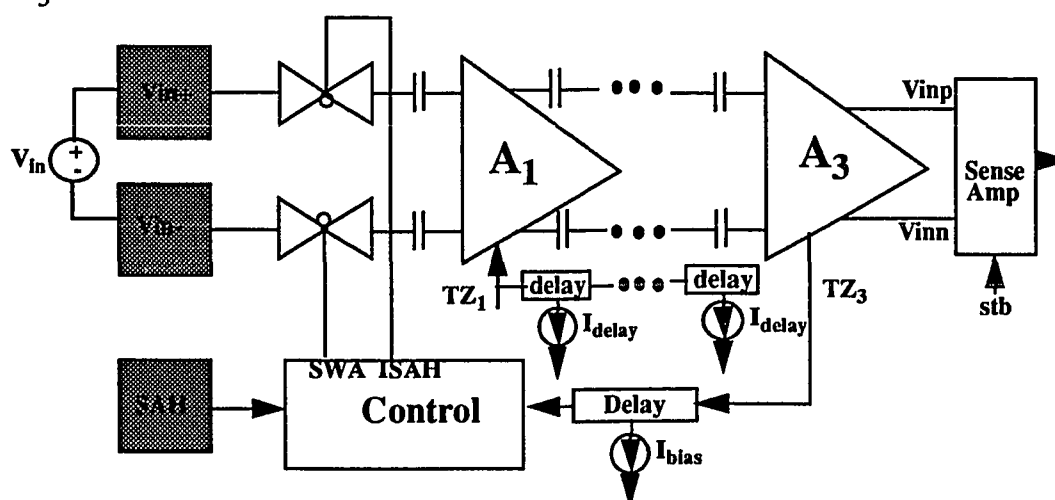

FIGURE 3.30 Sample-and-Hold Timing Control

The SWA signal remains high during the comparison phase. The comparator's output is allowed to settle until an externally controlled **LAH** signal is pulled high.**LAH** enables the sense amplifier to respond to the small signal comparator output. On the rising edge of **LAH**, the sense amp is strobed and the comparator output (**DOUT**) is ready to be read externally. **DOUT** will depend on the difference between V_{in} and the charge injection induced offset error E_{in}.

$$if\ E_{in} < V_{in}\ then\ Dout=1 \qquad\qquad 3.37$$

$$if\ E_{in} > V_{in}\ then\ Dout=0 \qquad\qquad 3.38$$

Once the data is read at the output pin, a reset signal goes high disabling the internal SWA signal. One half clock cycle later, the LAH signal is pulled low allowing the comparator to begin another cycle. The complete timing is shown in figure 3.31, where **SAH**, **ICLK**, and **RESET** are applied externally by a data generator.
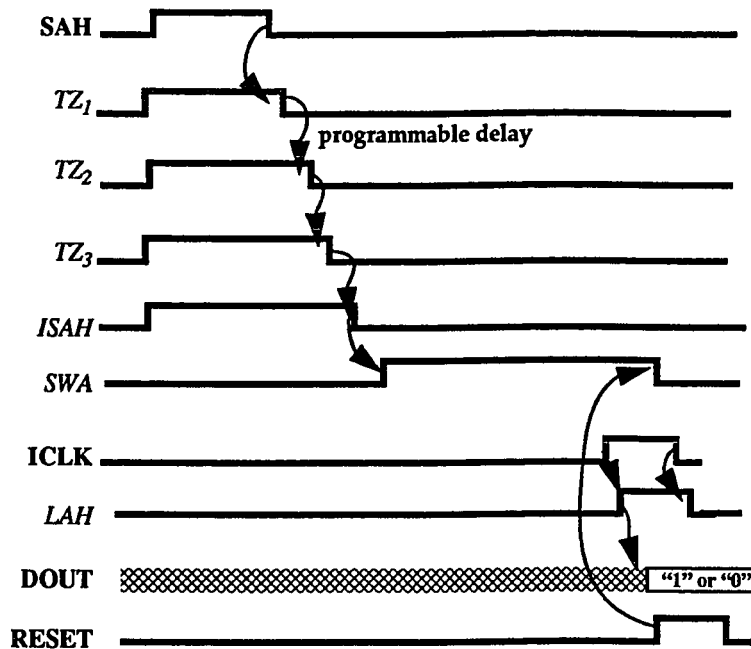
FIGURE 3.31 External Timing Control

By continuously running this timing and observing the value of Dout, the comparator offset is determined. As shown in figure 3.32, the input (Vin) and output (Dout) are tied together in an integrator feedback loop for automatic determination of the offset voltage.
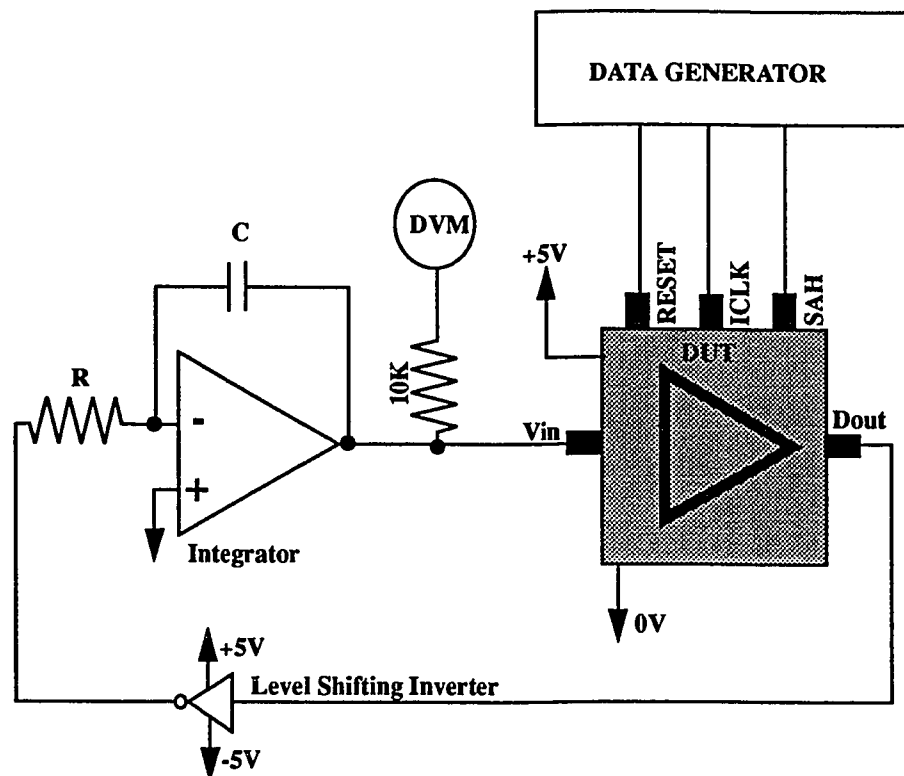
FIGURE 3.32 Closed Loop Method of Determining Comparator Offset

The comparator input voltage is generated by an operational amplifier wired in an integrating configuration. The input of the integrator is driven by the inverse of the comparator output signal. When the comparator output is a "0" The integrator input is driven by +5V. This forces the output of the integrator (V_{in} of the comparator) to linearly increase. Once V_{in} exceeds the offset of the comparator, Dout goes low. The input of the integrator is driven with -5V forcing the integrator output to ramp down. Once the voltage falls below the offset of the comparator, the output (Dout) goes high. Initially, the integrator output is oscillating; however, a steady state is reached eventually (see figure 3.33). By placing a digital volt meter (DVM) on the input to the comparator, the steady state input voltage is measured; hence, the comparator offset is known.
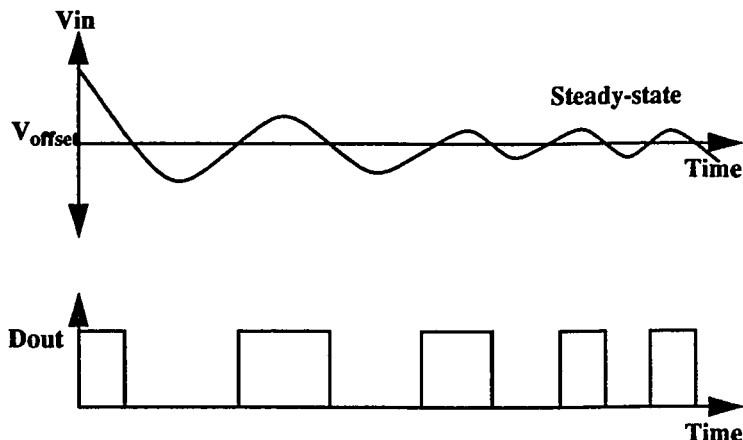
FIGURE 3.33 Vin Vs. Dout for a Comparator in a Integrator Feedback Loop

The DVM is isolated from the input node of the comparator by a 10k resistor. This reduces noise from the DVM. The device under test (DUT) is bypassed at all power, ground, and bias input lines by a $10\mu f$ and $0.1\mu f$ capacitor. The DUT is wired in a copper clad test board (see figure 3.34). This board serves as the ground plane, all bypass capacitor terminate here. Figure 3.35 shows the lab setup used in this thesis.

While running in a continuous comparison loop, the delay between auto zero signals is adjusted by the external input **DELAY**. **DELAY** controls the current flowing in the delay circuit. By sweeping the voltage (duration of delay), the various offsets are determined vs. delay time.

The power supply rejection ratio (PSRR) is determined for a given delay time by measuring the offset at supply voltages of 4.5 and 5.5 volts. The difference between these offsets is the PSRR.

By externally controlling the **SWING** pin, the swing of the auto zero signals can be altered. If **SWING** is tied to V_{dd}, the swing of the auto zero signal is dependent on the value of V_{dd}. Therefore, the charge injection is a function of V_{dd}, leading to offset variations. In order to have supply independent swings of the auto zero signals, **SWING** can be tied to a bias voltage (typically 3 to 4 volts). This is the constant voltage (V_{bias}) resulting in TZ signals swinging independent of V_{dd}.

Temperature sensitivity is determined using an external temperature forcing system. At various temperatures, the offset is measured vs. delay time. Typical temperatures range from $-55^{\circ}C$ to $125^{\circ}C$.

A complete layout and schematic of the test chip are shown in the appendix. The layout was generated on a SUN 4/110 workstation using Cadence software. The schematic was generated using Cadence Analog Artist software.
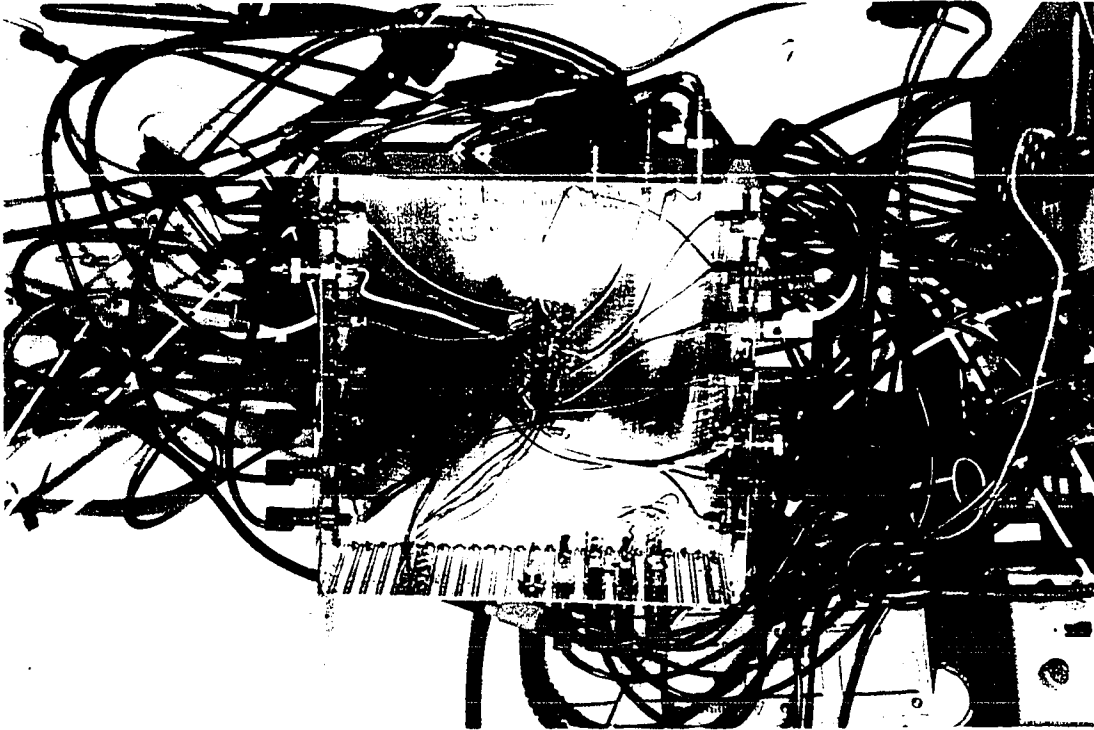
FIGURE 3.34 Test Board
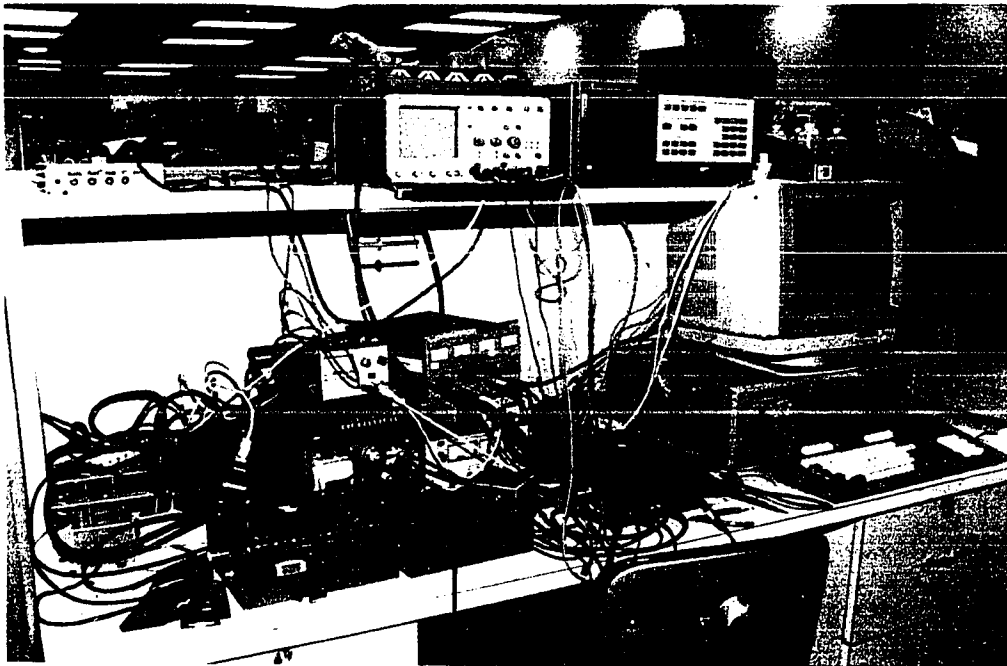
FIGURE 3.35 Test Setup

4.0 Results

Fabrication of the wafers containing the test chip for characterization of charge injection in analog to digital converters took 2 months. A photo of the resulting part is shown in figure 4.1. the parts were assembled in 40 pin ceramic packages. The equipment consists of a data generator, an oscilloscope, many power supplies and DVMs, an integrator box, and the device under test box custom made for this project. Nine experiments and many intermediate experiments were conducted on the parts in order to determine the effects of charge injection and related issues as the delay is varied between auto zero signals.

4.1 Experiment 1: Direction of Offset Shift

The first experiment performed determines the direction of offset shift due to charge injection induced error voltages with respect to the feedback switches and dummy devices. Furthermore, the relative magnitudes for the first, second, and third stage dummy devices are used to determine the comparator gain and dominate sources of charge injection.

Initially, the offset of the overall comparator was measured at $V_{dd}=5V$ for the single ended comparator (Comp1). For non-staggered auto zero signals ($T_d<3ns$) the overall offset was -7mv. One at a time, the dummy devices were removed and the offset measured. The first stage dummy device was removed leading to a new offset of -277mv. Next the second, and finally the third stage dummy devices were removed using a laser trimming microscope. The resulting offsets and the change from the previous step are shown in table 4.1.

TABLE 4. 1 Comparator Offsets with Dummy Devices Removed

	OFFSET	△
Initially	**-7mv**	▬▬
Remove #1	**-277mv**	**-270mv**
Remove #2	**-266mv**	**+11mv**
Remove #3	**-269mv**	**-3mv**
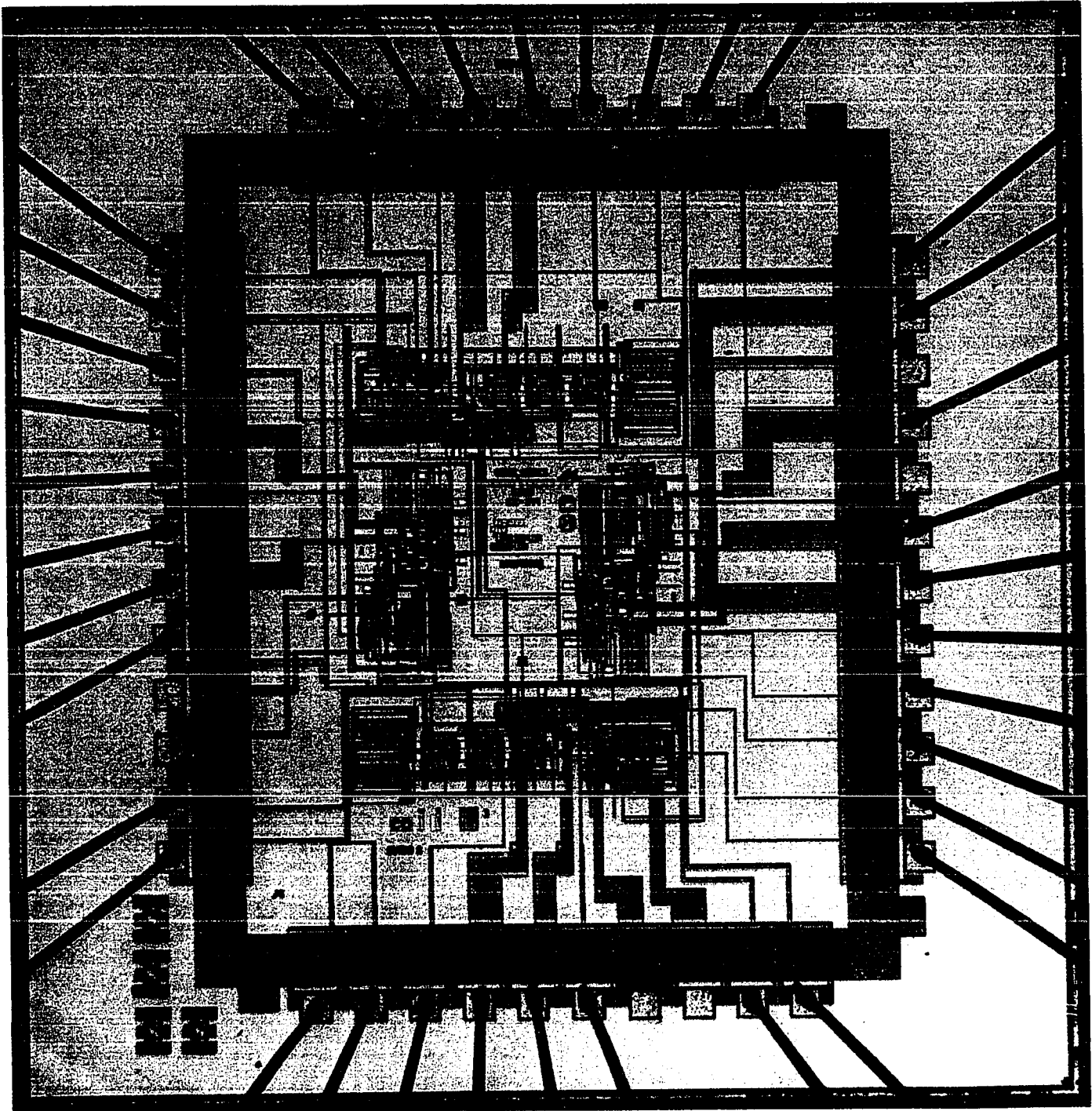
FIGURE 4.1 Die Photo

The input to the first stage of the comparator is tied to several sources of charge injection (see figure 4.2).

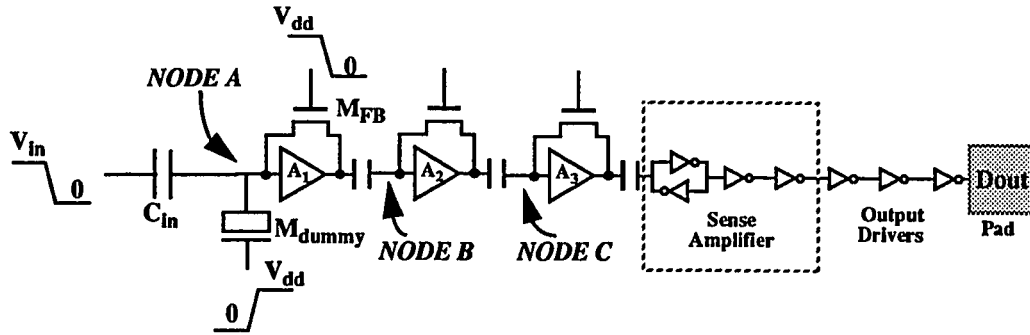**FIGURE 4.2 Sources of Charge Injection for First Stage Input Node**

Relative to Dout, the voltage at *NODE A* (V_A) is inverted. If $V_a<V\text{trip}$, Dout is a logic "1", while $V_a>V\text{trip}$ Dout is a "0". Neglecting charge injection, a positive input voltage ($V_{in}>0v$) the initial voltage at *NODE A* is reduced. Inversely, a negative input voltage increases the voltage at *NODE A*. By defining the total capacitance on *NODE A* as unity, the net change in voltage at *NODE A* with respect to the changing input signal (V_{in}) is

$$V_{A_{input}} = V_{trip} - V_{in} \bullet C_{in}$$
<div align="right">4.1</div>

Therefore, a positive input voltage forces *NODE A* below V_{trip} leading to a digital "1" at Dout. Conversely, a negative input voltage leads to a "0" output.

Since the signal driving the feedback switch (M_{FB}) is in phase with the input signal driving C_{in}, the effect of the feedback switch charge injection is to lower the voltage at *NODE A*.

$$V_{A_{feedback}} = - [V_{dd} \bullet C_{ov}] - \chi_{FB} \bullet C_{ch} \bullet [V_{dd} - V_{trip} - V_{TE}]$$
<div align="right">4.2</div>

where χ_{FB} is the fractional channel charge leaving the source of M_{FB}. In order to balance the negative voltage change due to the feedback switch charge injection (equation 4.2), the applied input voltage must be negative (equation 4.1). Therefore, the offset resulting from the first stage feedback switch is negative.

The signal driving the dummy device (M_{dummy}) is the opposite phase of the signals driving C_{in} and M_{FB}. The change in voltage due to M_{dummy} charge injection at *NODE A* is

$$V_{A_{dummy}} = 2 \cdot V_{dd} \cdot \frac{C_{ov}}{2} + \chi_{dummy} \cdot [V_{dd} - V_{trip} - V_{TE}] \cdot \frac{C_{ch}}{2} \qquad 4.3$$

M_{dummy} is geometrically half the size of M_{FB}, but both the source an drain tie to NODE A. Consequently, χ_{dummy} is 1. Complete cancelation between the dummy device and feedback device charge injection only occurs when $\chi_{FB}=1/2$ and the devices match.

Charge injection due to the dummy device increases the voltage at NODE A, leading to a "0" output for small positive input voltages. In order to reach the threshold of the comparator, a positive input voltage is required. This voltage is the positive offset of the comparator; therefore, dummy device charge injection on the first stage input node leads to a positive offset.

Since the voltage changes at NODE A are not attenuated by an amplifier stage with respect to V_{in}, they are dominate compared to the charge injection effects at NODE B and NODE C. Furthermore, since each amplifier stage is inverting, the offset due to the second stage dummy device is negative with respect to Vin. Figure 4.3 shows the direction and magnitude of the offset relative to V_{in} induced by the feedback switches and dummy devices of each stage.
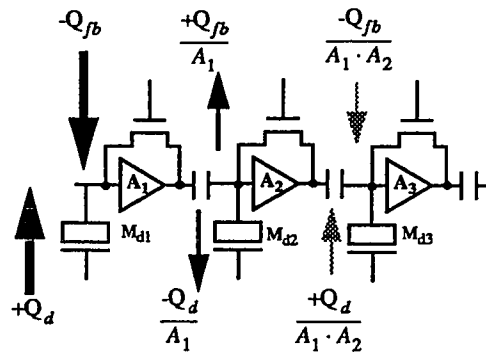

FIGURE 4.3 Offset Shift Direction and Magnitude

From table 4.1, the initial comparator offset is -7mv. Neglecting the second and third stages, this offset results from the feedback switch injecting more charge than the dummy device. By removing M_{d1}, the initial offset shifts -270mv. Therefore, the dummy device M_{d1} contributes +270mv of offset to the comparator balancing the -277mv offset resulting from the feedback switch. Once M_{d2} is removed, -270 mv is injected into the input of A_2, but this is attenuated and inverted by A_1. The net result is a +11mv offset shift. Therefore the gain of A_1 is approximately 25. The data in table 4.1 cannot be used to calculate the second and third stage gains because these stages are driven into the linear, low gain region of operation by the large charge injection signal applied to the first stage. Since the first stage gain is so large, and the charge injection of M_{d1} is larger than that of M_{d2} with respect to V_{in}, the charge injection induced offset voltages of the second and third stages can typically be neglected. Therefore, negative offsets result from dominate feedback switch charge injection and positive offsets are the result of dominate dummy devices.

4.2 Experiment 2: Swing Vs. Offset

In the second experiment, V_{dd} is fixed at 5.5V, the temperature is 27°c, and the output of the single ended comparator (Dout1) is monitored. The offset was determined for a range of voltages applied to the SWING pin. This pin controls the voltage swing on the feedback switches and dummy devices (see figure 4.4). Staggering is reduced to <3ns so the effects of the dominate first stage are not cancelled by the second stage.
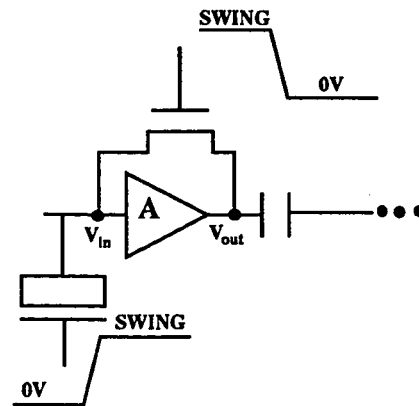
FIGURE 4.4 SWING Pin Driving Dummy Devices and Feedback Switches

The SWING pin was varied from 3V to 5.5V, the resulting comparator offset voltages are plotted in figure 4.5. For variations in SWING voltage, the comparator offset behaves differently in two regions. In the first region (I), the offset linearly increases as SWING increases from 3V to 3.5V. Once the swing exceeds 3.5V, the offset decreases linearly with increasing SWING voltage, eventually becoming negative at values larger than 4.65V.

From experiment 1, it may be assuming the first stage charge injection is dominate in the overall comparator offset. Therefore, for a dominate dummy device

$$Qinj_{dummy} > Qinj_{feedback} \qquad\qquad 4.4$$

the net offset is positive. Conversely, a dominate feedback device

$$Qinj_{dummy} < Qinj_{feedback} \qquad\qquad 4.5$$

leads to a negative offset.
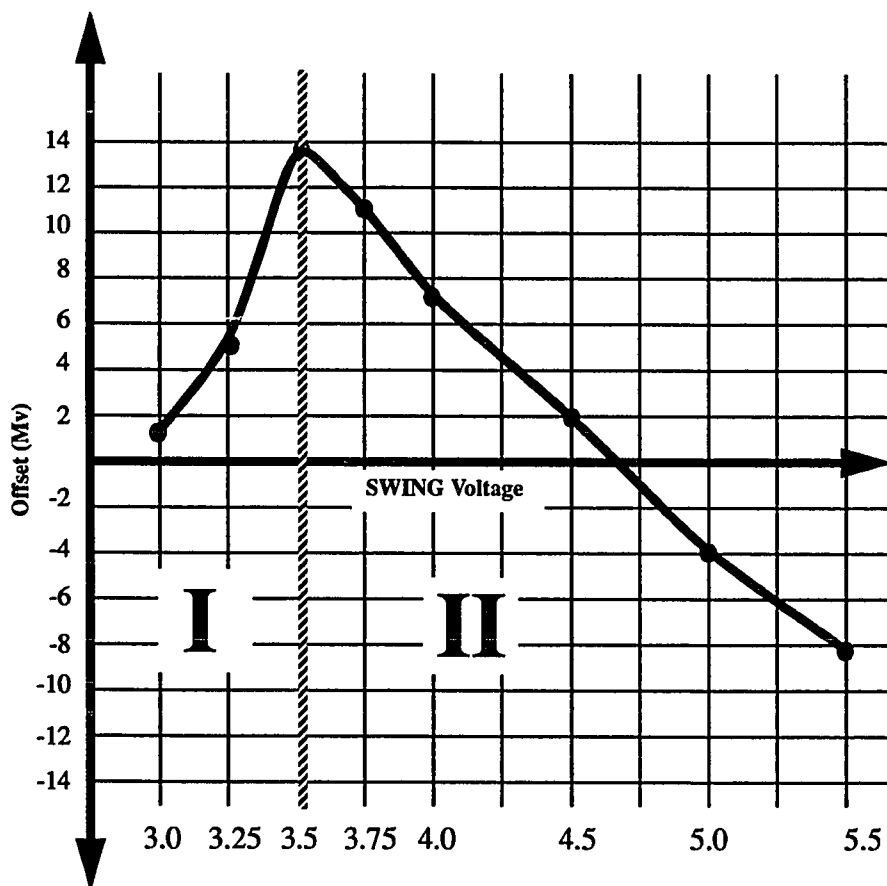
FIGURE 4.5 Offset Vs. Swing

For region I of figure 4.5, the offset is increasing as the voltage swing on the feedback switch and dummy device is increased. From equation 4.4, a dominate dummy device leads to a positive offset; therefore, the dummy device is contributing more charge injection then the feedback switch. As the *SWING* voltage increases, the offset increases because the swing is larger (replace V_{dd} with *SWING*) in equations 4.2 and 4.3).

In this region of operation the signal driving the feedback switch is small (<3.5V). The feedback switch is not operating in its normal region; either it is off, or in the saturation region of operation.

The feedback switch turns off once the bias point of the inverter reaches the point

$$V_{supply} < V_{TE} + V_{bias} \qquad\qquad 4.6$$

For this case, the comparator will not be biased at $V_{in}=V_{out}$. Furthermore, charge will not exist in the channel of the feedback and dummy transistors. Charge injection results only from the overlap capacitance. Variations of overlap capacitance leading to 14mv of offset

at a 3.5v swing are excessive for the process; therefore, the devices cannot be assumed off, channel charge must contribute to this error.

The feedback switch is in the saturation region of operation if

$$V_{out} - V_{in} > V_{supply} - V_{TE} - V_{in}$$ 4.7

For a transistor in saturation, the channel charge is on the source side of the transistor. Once the transistor is turned off, all this charge exits through the source. Since the drain side of the feedback switch is not inverted, the channel charge is less for a transistor in the saturation region of operation in comparison to a transistor in the linear region of operation. The magnitude of the charge depends on how deep the transistor is in the saturation region of operation. In region I the dummy charge injection is larger then the feedback charge injection; therefore, there is less channel charge injected by the saturated feedback switch then the linear dummy device.

As the swing increases beyond 3.5v, the feedback switch enters the linear region of operation.

$$V_{ds} = V_{in} + -V_{out} \cong 0V$$ 4.8

Since the feedback switch is geometrically twice the size of the dummy device, the total offset induced is a function of the fractional part of charge leaving the source of the feedback switch (χ_{FB}). From equations 4.2 and 4.3, the net offset resulting from channel charge injection is

$$V_{os} = \left(\chi_{FB} - \frac{1}{2} \right) (V_{dd} - V_{TE} - V_{trip})$$ 4.9

In this region of operation (region II), as the swing is increased, the offset decreases. Negative offsets result when the feedback switch charge injection is greater then the dummy device charge injection. This occurs if $\chi_{FB} > \frac{1}{2}$. Therefore, more channel charge exits the source than the drain of the feedback device.

4.3 Experiment 3: Offset Vs. Delay

In the third experiment, the offset was determined for various delays between auto zero signals. In this experiment, the single ended comparator was monitored for its offset voltage. The *DELAY* pin voltage was swept, and the resulting auto zero delay was measured using the internal source follower probe circuits and an oscilloscope. For this experiment, the temperature was fixed at $27^\circ C$. Furthermore, the capacitor was removed from the delay circuits (see figure 3.2, the delay layout) to allow shorter delay times. By sweeping *DELAY* from 1.3V to 5V, the auto zero delay time varied from 3ns to 100ns. Figure 4.6 shows the offset as a function of delay.
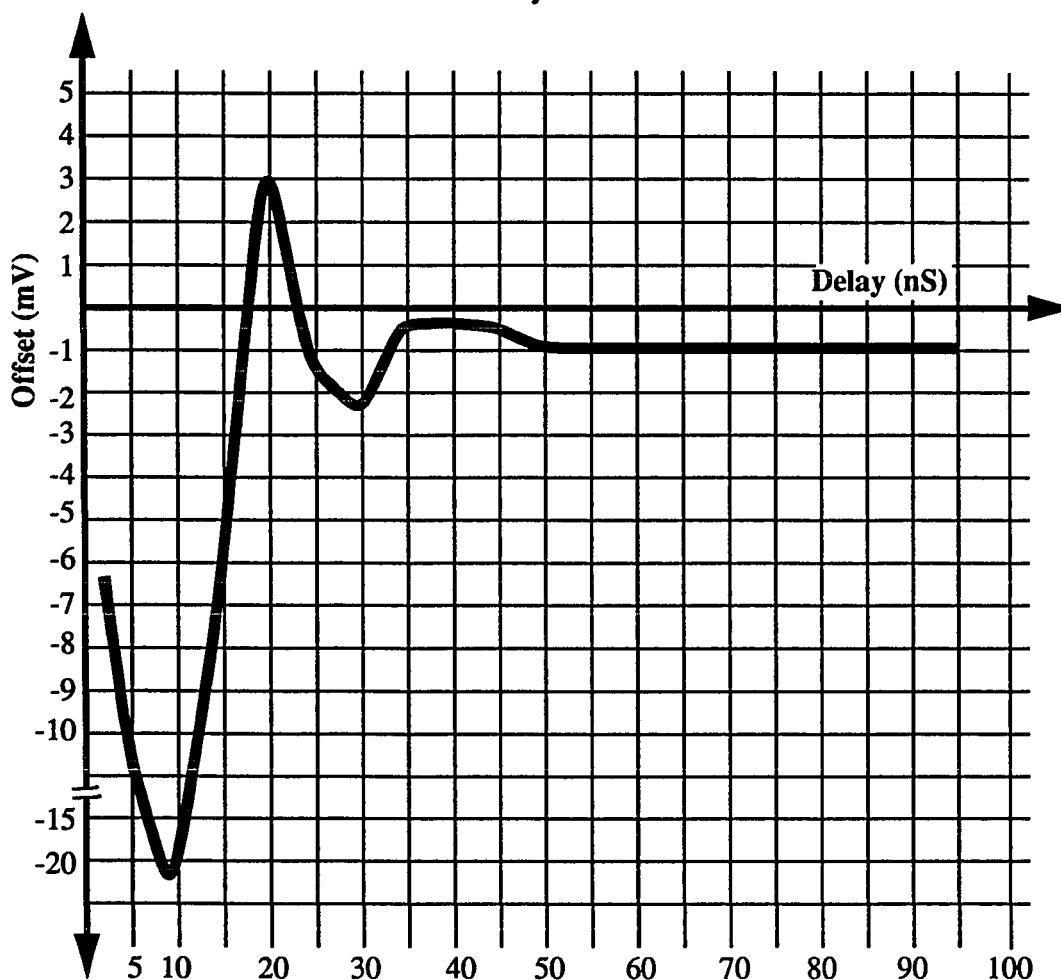
FIGURE 4.6 Offset Vs. Delay for Single Ended Comparator

For small delays between staggered auto zero signals (3nS-25nS), the offset is large and a strong function of delay time. As the delay increases, the offset stabilizes at -1mv. This offset is non-zero because the third stage charge injection is not cancelled and noise contributions both off and on chip. As shown in figure 4.6, as the delay is increased from 3ns, the offset goes negative. This trend continues until the delay reaches 10nS. At this

point, the offset increases. For delays in excess of 25nS, this damped sinusoidal response dies out and the offset settles to -1mv.

Assuming the first stage is dominate, the offset at a given delay is the voltage seen at the input of the second stage amplifier attenuated by the gain of the first stage amplifier. The offset vs. delay curve represents the transient response of the amplifier A_1 with a step input. The step input is due to the charge injection at the high impedance input of A_1. Figure 4.7 shows the input and output transient response of amplifier A_1.
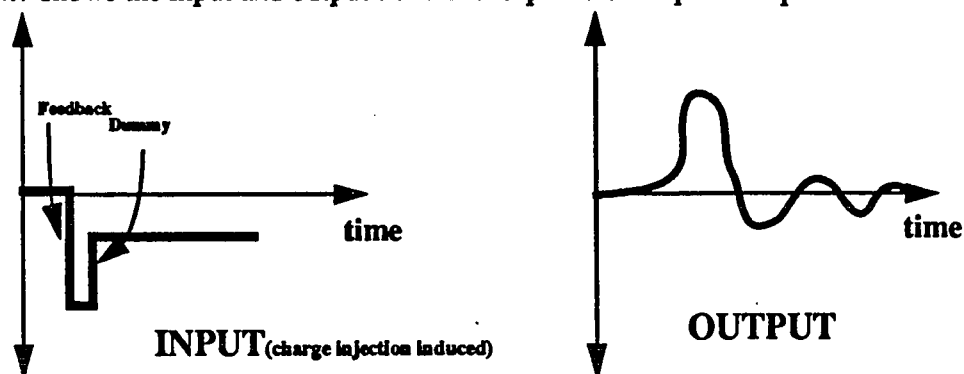
FIGURE 4.7 Transient Response of Amplifier A_1

As long as the second stage auto zero switch is closed, the output of A_1 is cancelled by the second stage. Once TAZ_2 is opened, the input to stage A_2 is held resulting in an offset. Using a probe circuit (see figure 3.25), the output of the first stage amplifier was observed using an oscilloscope. A step function similar to that of figure 4.7 was applied to the input node. The resulting transient response is shown in figure 4.8.
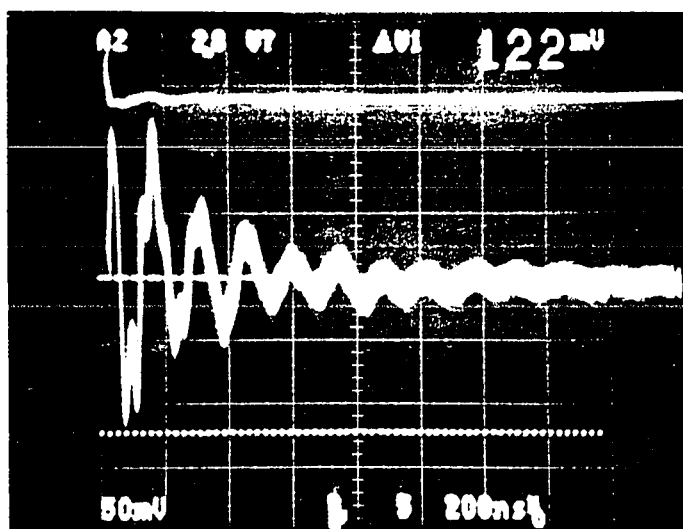
FIGURE 4.8 Output Transient Response of Single Amplifier Stage

The data obtained in figure 4.6 was expanded by measuring the offset vs. delay from 3ns to 20ns using small time increments between measurements. The result is a damped sinusoidal response similar to the observed comparator output response of figure 4.8.
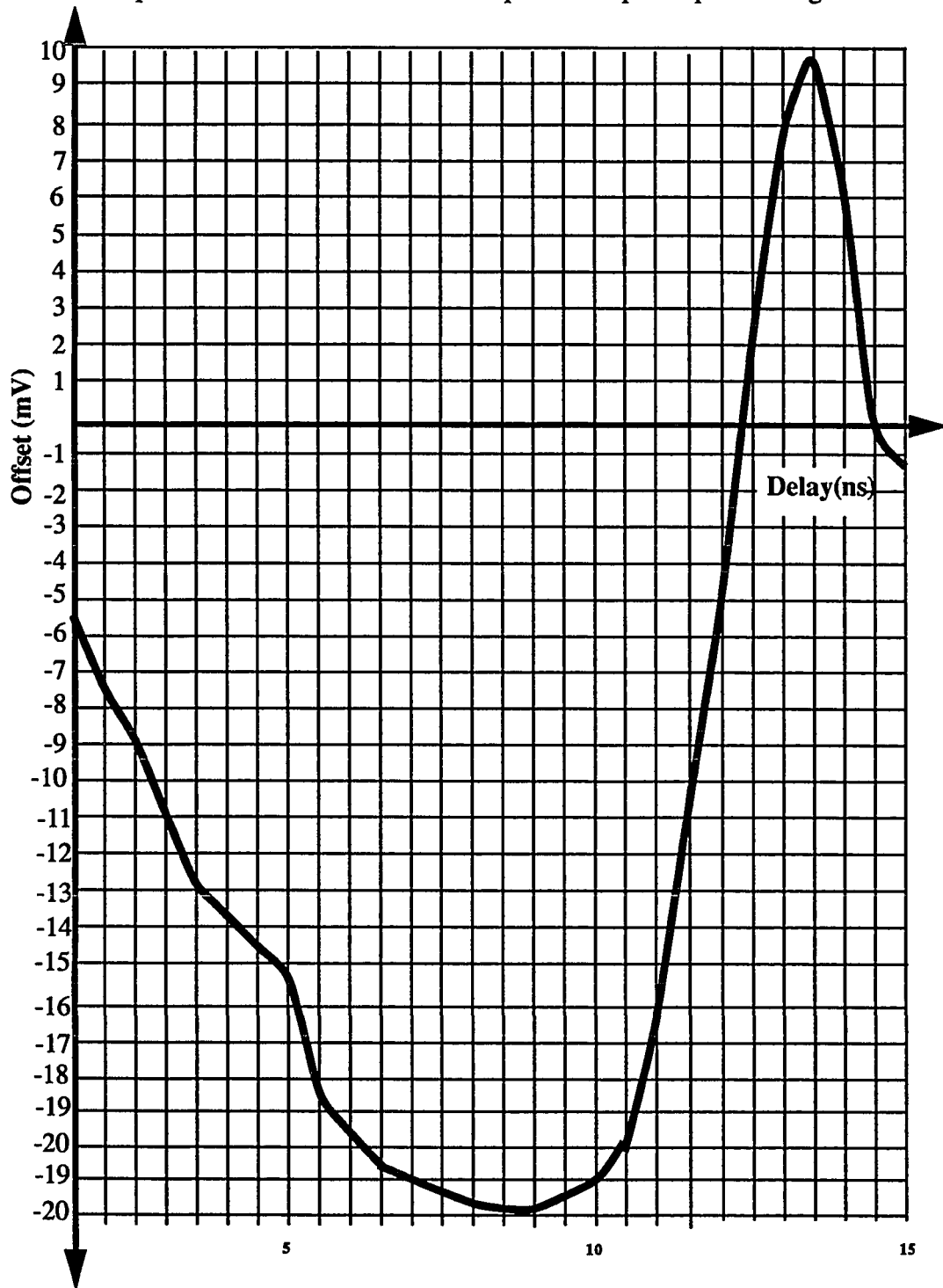
FIGURE 4.9 Detailed Short Delay Vs. Offset

As the delay increases beyond 20-30nS, the comparator output begins to settle. Observing figure 4.6, the offset for delay times greater than 30ns is less than 1mv. In this region, staggered auto zero signals are cancelling the dominate effects of charge injection for the first and second stages. However, the third stage charge injection is not compensated by staggered auto zero signals. Attenuated by the first and second stage gains, the third stage charge injection induced error (E_3) leads to an overall comparator offset of

$$V_{offset} = \frac{E_3}{A_1 \bullet A_2}$$
4.10

where A_1 and A_2 are the first and second stage gains, respectively.

The -1mv offset at long delay times is due to a third stage dominate feedback switch charge injection, see figure 4.3. An offset of -1mv in the third stage due to device mismatches alone is unlikely, since completely removing the third stage dummy device leads to a -3mv change in offset (see experiment 1). Therefore, the -1mv offset must be due to other factors besides device mismatch.

These factors can be attributed to noise contributions from the test system and internal chip noise sources. On-chip substrate noise leads to an overall DC offset shift in the comparator. Once the first stage auto zero switch has opened, internal noise sources are integrated and applied to the high impedance storage nodes resulting in DC offset shifts.

External to the chip, board level ground loops lead to offset voltages. The solution to these set-up problems is non-trivial and can lead to hundreds of hours of debugging. conventionally, the test board needs a good ground plane with bypass capacitors at every analog pin. The test board used for the offset measurements uses a copper clad box with all analog nodes bypassed to the ground plane by $10\mu F$ and.$1\mu F$ capacitors.

For the single ended comparator, the delay necessary for cancelation of charge injection induced offsets is in excess of 25ns. For delay times less than 25ns, the amplifier transient response is captured by the stage it is driving. For designs using 2 to 4 inverter delays between auto zero signals, the offset becomes excessively large due to the amplifier transient response. The offset error is lower for a delays less than 3ns when compared to delays in the range 5ns-15ns.

In a previously developed analog-to-digital converter, the auto zero signals were delayed by two inverter delays. For the process used, this lead to delays in the 5ns range. The offset error was very large for these devices. Experimentally, the inverters were replaced with a short circuit preventing staggered auto zero signals (0ns of delay). This resulted in a significantly reduced offset errors. The final design used 0ns delay between auto zero signals; however, if the auto zero signal delays were initially designed at 20nS, the offset would have been optimum.

4.4 Power Supply Rejection Ratio Vs. Delay

In the fourth experiment, the single ended comparator was tested under the same conditions of experiment 3, except the offset was determined for V_{dd}= 4.5, 5.0, and 5.5 volts. The power supply rejection ratio (PSRR) was determined vs. delay by subtracting the offset at V_{dd}=5.5V from the offset at V_{dd}=4.5V at a fixed delay. The PSRR directly reflects charge injection cancellation, since charge injection is proportional to supply voltage (V_{dd}). Figure 4.10 shows a plot of the PSRR vs. delay.
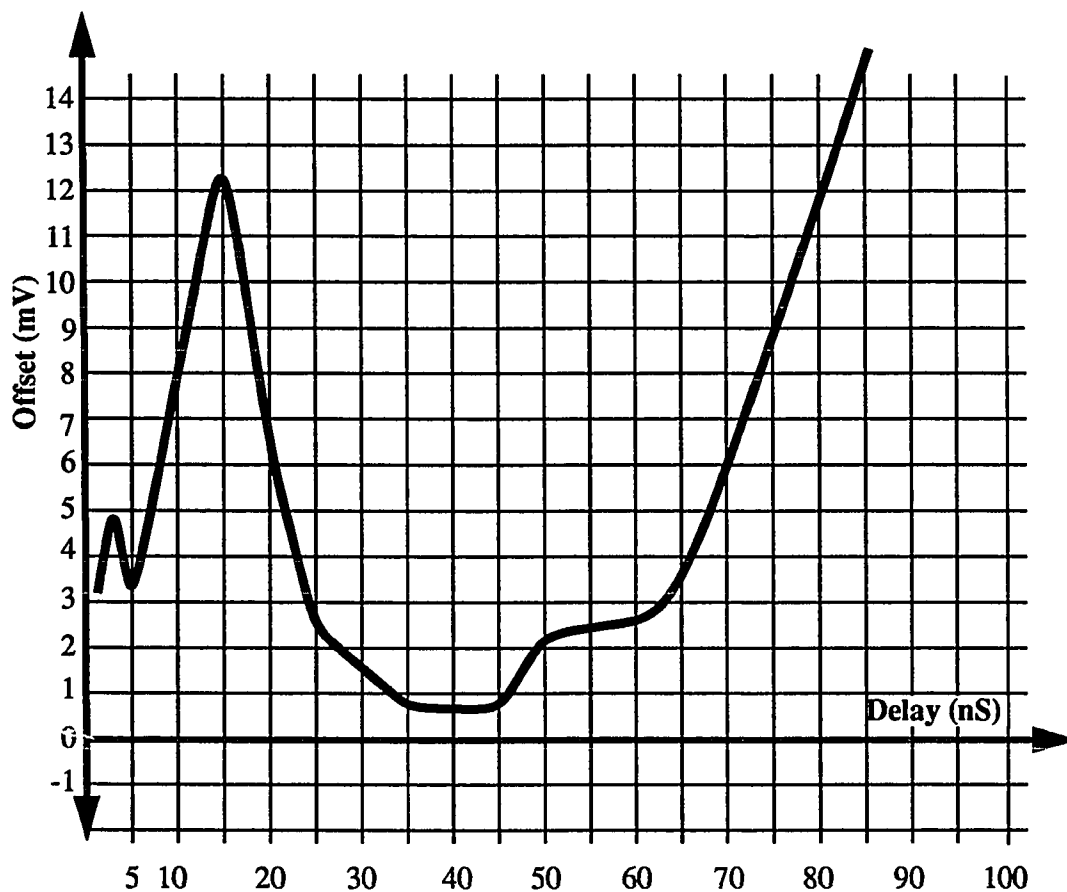
FIGURE 4.10 Power Supply Rejection Ratio Vs. Delay

For small delays between auto zero signals (<3nS), the PSRR was small enough for an 8-bit ADC with a +/- 1/4 LSB PSRR. However, as the delay is increased, the PSRR becomes extremely large. At 15ns delay, the PSRR peaks at 13mv. As the delay is further increased, the PSRR is reduced until it finally settles at <1mv. The PSRR remains small for delays in the range 35ns to 65nS. At 65ns, the PSRR rapidly increases with delay.

At the minimum delay the PSRR is small, yet non-optimum compared to longer delay times. For delays <3ns, the amplifier response has not peaked in its damped sinusoidal response. For minimum delay, the offset decreases as V_{dd} is increased, see figure 4.11. As shown in experiment 2, a decrease in offset is due to a dominate feedback device channel charge injection. The slope of this line is the PSRR at 3ns delay.
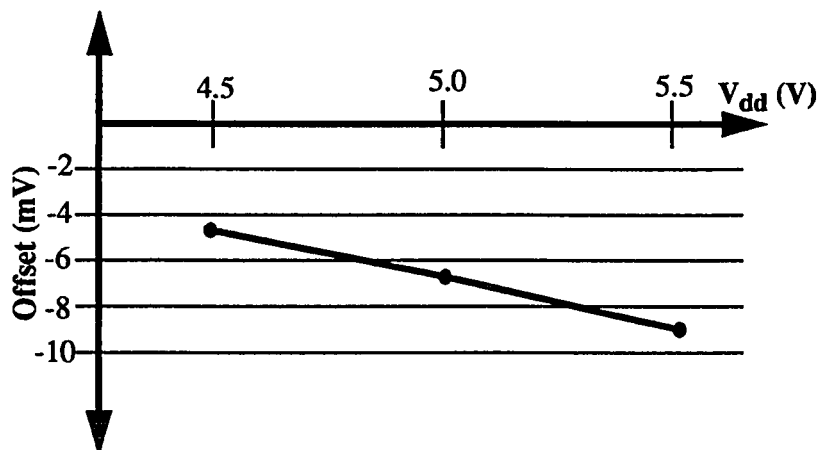
FIGURE 4.11 Offset Vs. V_{dd} for Minimum Delay

For minimum delay, the comparator offsets are not a strong function of the transient response of the amplifier. But, as the delay is increased, the peak values of the first stage amplifiers damped sinusoidal response are captured on the input capacitive node to the second stage amplifier. From equation 2.17 page 12, as the supply voltage is increased, the charge injection is increased resulting in an increased step function applied to the input of each amplifier. Furthermore, the amplifiers step response magnitude and phase change as V_{dd} changes (see figure 4.12).
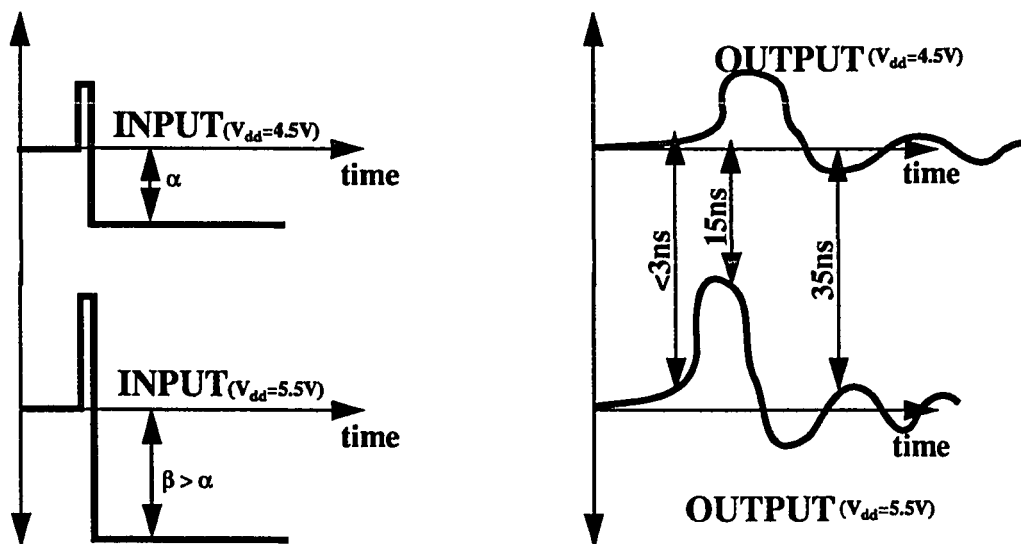
FIGURE 4.12 Amplifier Transient Response Vs. V_{dd}

As the delay times are increased from 3ns to 30ns, the first stage amplifier transient response is held at the second stage amplifier input the instant its feedback switch is turned off. At V_{dd}=5.5v, the amplifier response time is faster than V_{dd}=4.5v because the overdrive voltages and DC bias currents are larger. Also, the input step is larger at V_{dd}=5.5v due to the relationship between charge injection and power supply voltage.

At 15ns, the PSRR is at its peak. At V_{dd}=5.5v, the transient response is has hit its peak value at 15ns while the comparator transient response at V_{dd}=4.5v has not peaked. Furthermore, for V_{dd}=4.5v, the input step is smaller leading to smaller peak transient response. The experiment to follow, experiment 5, examines the comparator transient response as a function of swing in more detail.

As the delay is increased beyond 30ns, the comparator output has settled for both values of V_{dd}. Since the transient response has settled, the offset is small for both cases leading to a small PSRR (<1mv). Beyond 65ns of delay, an interesting phenomena occurs; the PSRR grows extremely large. This is due to the offset beyond 65ns at V_{dd}=5.5v (see figure 4.13), compared to the offset vs. delay at V_{dd}=4.5v (recall figure 4.6).
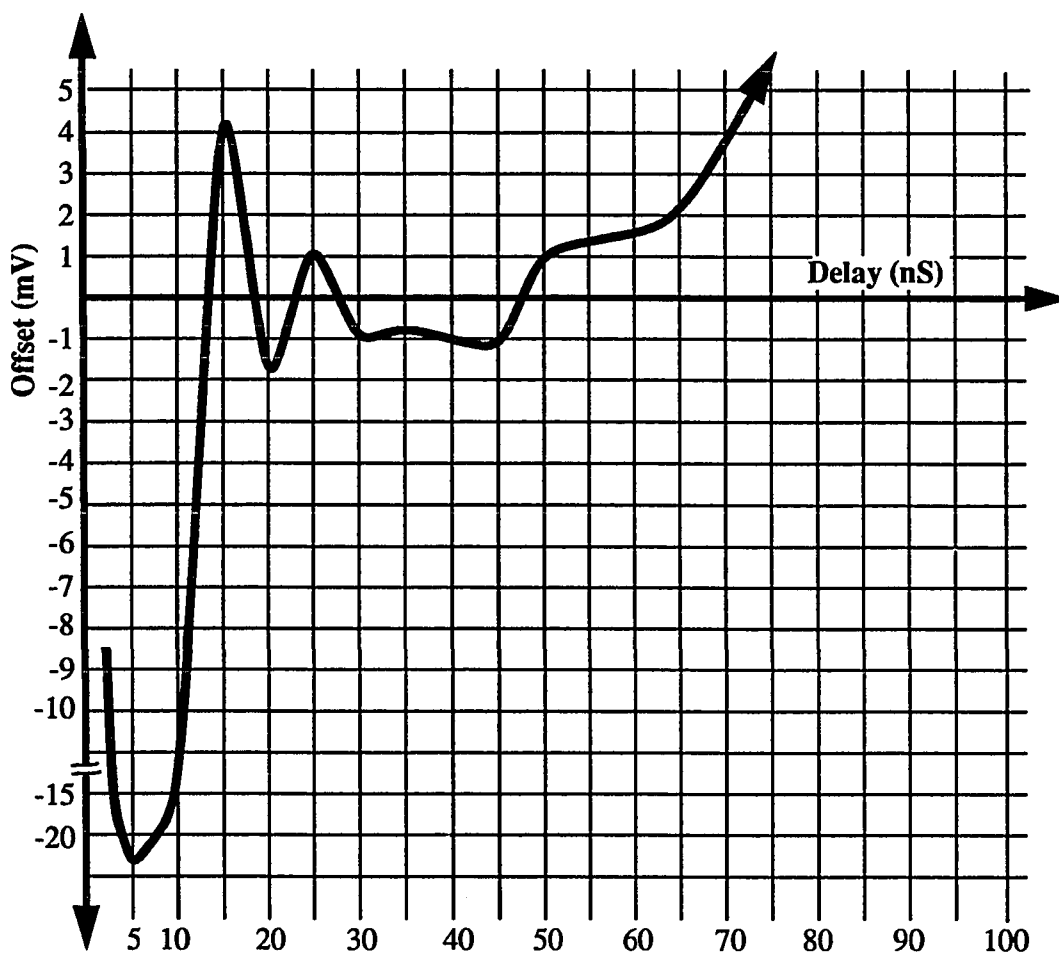
FIGURE 4.13 Offset Vs. Delay for V_{dd}=5.5v

This increase in offset also occurs at V_{dd}=4.5v; however, delays in excess of 100ns are required. In order to have a positive offset, the first stage dummy device must be contributing excessive charge injection compared to the feedback switch. Experimentally the dummy devices where removed and the offset measured vs. delay.

By removing the dummy devices, the offset does not increase for delays in excess of 500ns. Therefore, the dummy devices are the cause of the increase in offset and PSRR for delays in excess of 100ns. However, by removing the dummy devices, the offset is very large for small delays, and the comparator transient response time is increased. Figure 4.14 shows the offset vs. delay curve for a single ended comparator with no dummy devices at V_{dd}=4.5 and 5.5 volts.
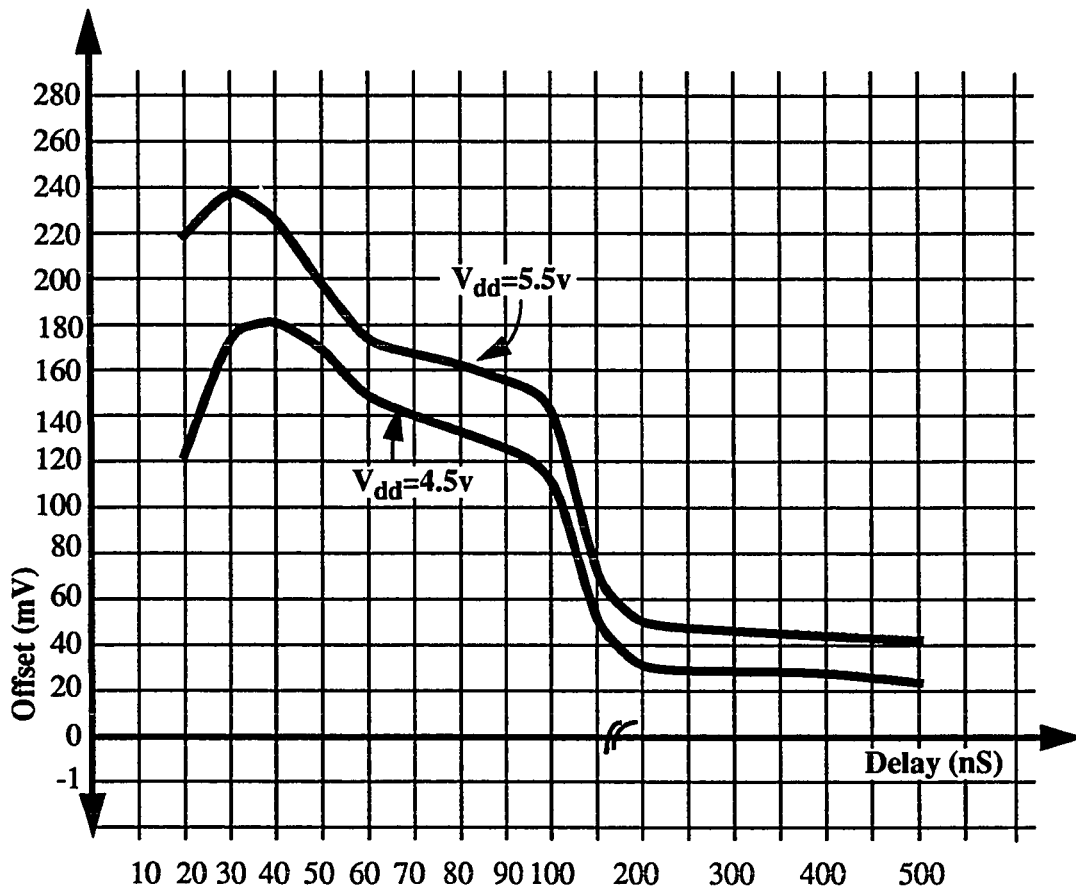
FIGURE 4.14 Offset Vs. Delay with Dummy Devices Removed

Delays in excess of 100ns are unreasonable in conventional comparator designs. In actual practice, either zero delay or 30ns leads to acceptable PSRR and offset errors, with optimum offset and PSRR at 30-50ns delay. Using 2 or 4 inverter delays between auto zero signals leads to poor PSRR and large offset voltages due to the transient response of the amplifier as V_{dd}, delay, or the process parameters change.

4.5 Experiment 5: Transient Response Variations as Charge Injection Step Size Changes

In this experiment the supply voltage is held at V_{dd}=5.5v and the *SWING* pin is varied. This pin controls the swing on the dummy devices and feedback switches. As *SWING* is varied, the offset vs. delay is monitored for the single ended comparator. Figure 4.15 shows the results of this experiment for swings of 3,4, and 5.5v.
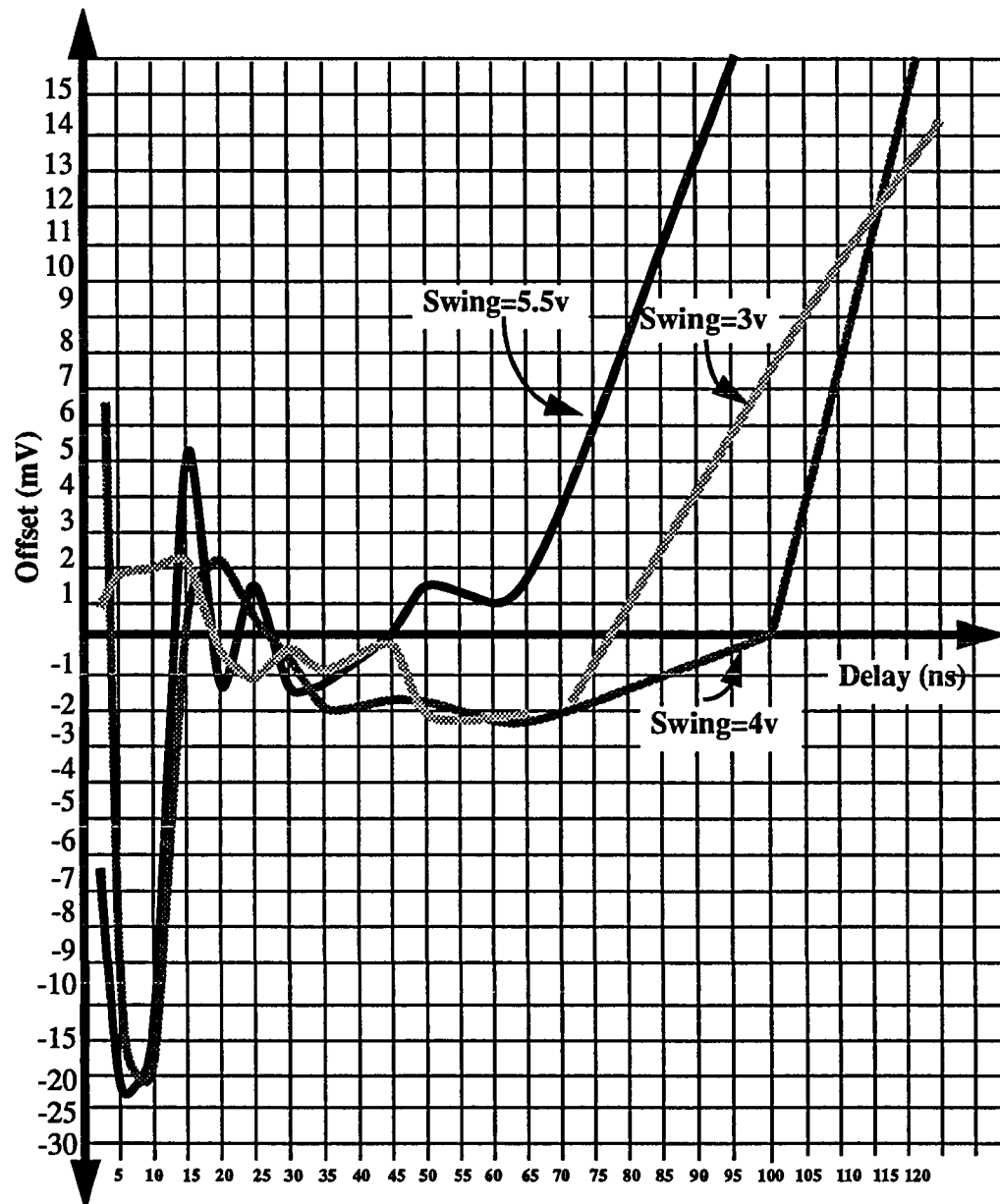
FIGURE 4.15 Offset Vs. Delay as SWING is Varied

Two conclusions can be drawn from the data presented in figure 4.15. The first observation is the peak transient offset is a function of the swing. As the swing increases, the peak value of the transient response increases, see figure 4.16.
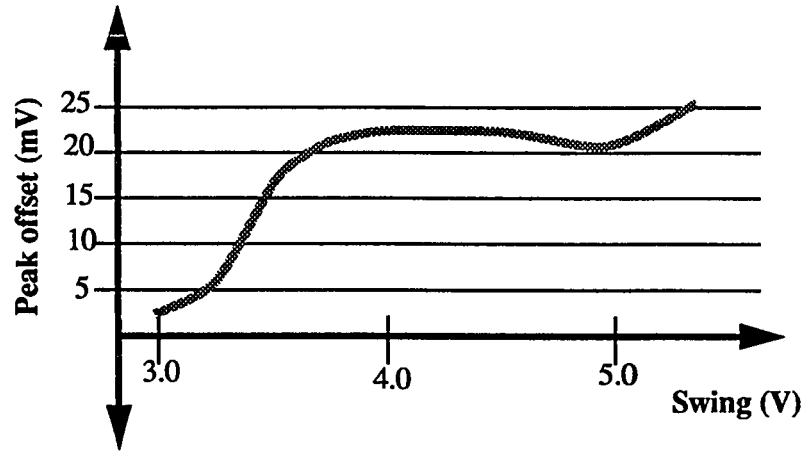
FIGURE 4.16 Peak Offset Vs. Swing

The second observation is the frequency of the damped sinusoidal transient response increases as *SWING* increases. Figure 4.17 shows the delay required for the offset to reach its peak value.
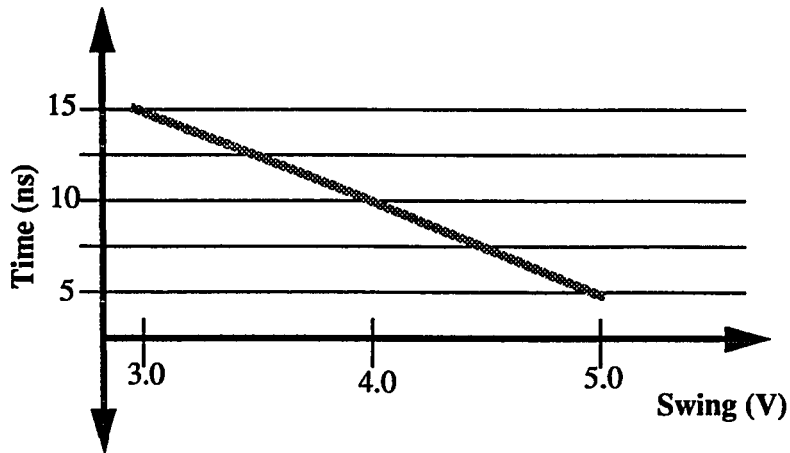
FIGURE 4.17 Peak Offset Vs. Swing

The offset is a strong function of V_{dd} for delay times falling within the amplifier transient response. These dependencies of offset on swing lead to PSRR errors.

4.6 Experiment 6: Temperature Sensitivity

In experiment 6, the single ended comparator offset vs. delay was determined at a fixed V_{dd}=5v, over variations in temperature, T=-55°C, 25°C, and 125°C. Figure 4.18 shows the results of this experiment.
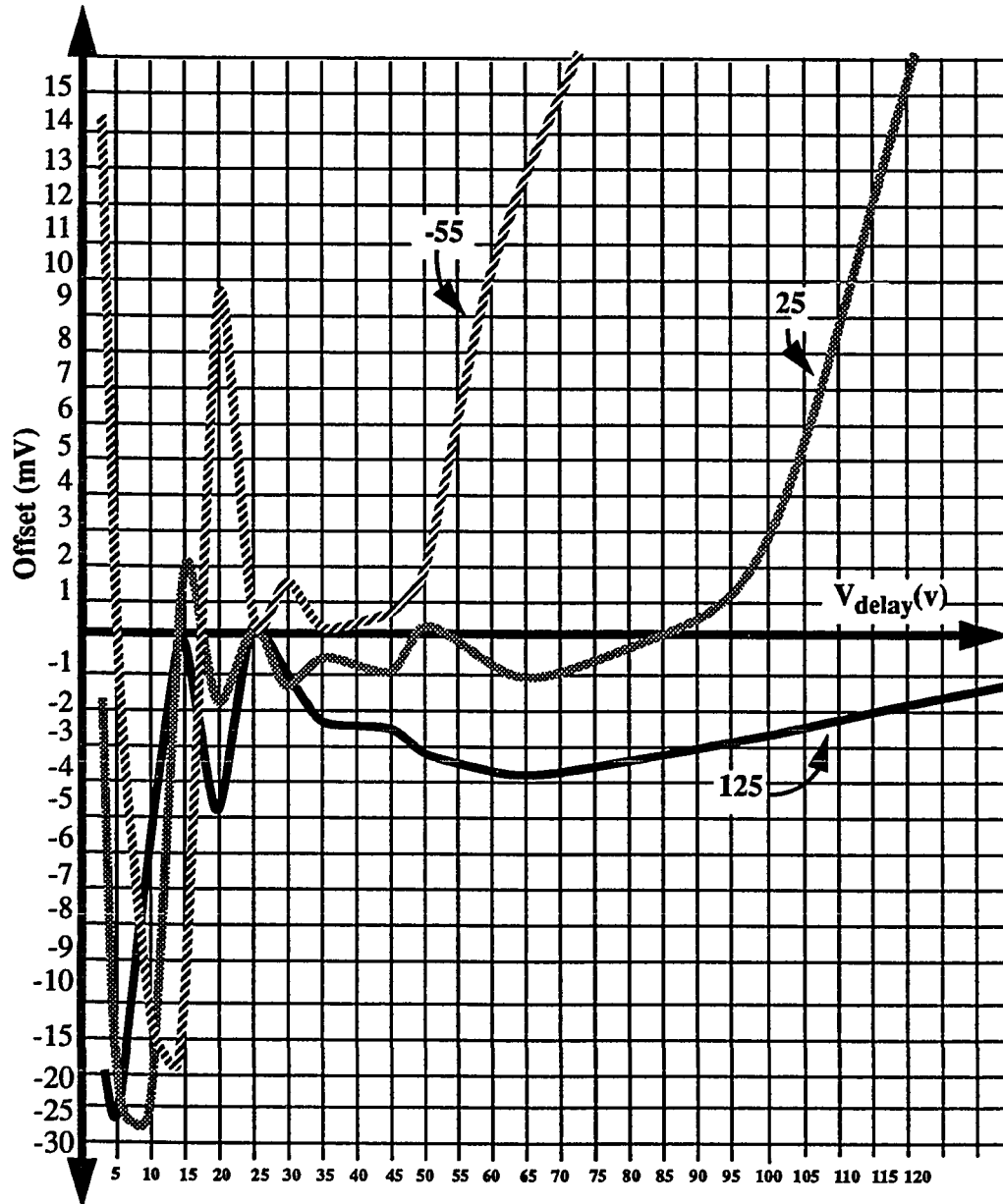
FIGURE 4.18 Offset Vs. Delay over Temperature

For small delays (<3ns) the offset is a strong function of temperature. As shown in figure 4.19, the offset increases as the temperature is decreased.
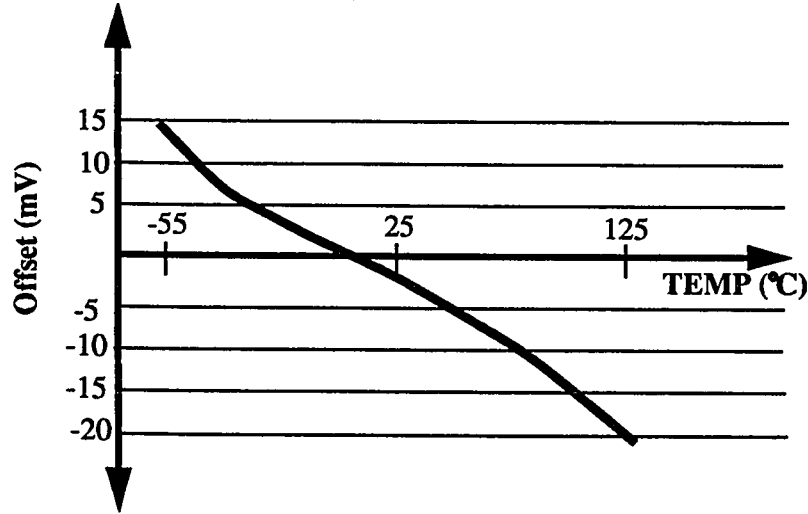
FIGURE 4.19 Offset Vs. Temperature at 3ns Auto Zero Delay

As shown in experiment 1, the offset becomes negative for dominate feedback switch charge injection and positive for excessive dummy device charge injection. In the current experiment, as the temperature is increased, the feedback switch of the first stage contributes increasing quantities of channel charge injection.

The slew rate of the signal driving the feedback switch increases for decreasing temperature. From section 2.6 equation 2.87, the fractional percentage of channel charge injection (χ) leaving the source is a function of the signal slew rate driving the gate of the switch. At colder temperatures $(-55°C)$, the slew rate is fastest due to increased mobility (current); therefore, χ falls below 1/2 leading to a decrease in channel charge exiting the source. Since the channel charge of the dummy device is not effected by slew rate (both source and drain tie to the high impedance input node), the offset increases due to decreased feedback switch channel charge injection as the temperature is decreased.

Conversely, as the temperature increases, the slew rate of the signal driving the feedback switch is reduced. This leads to increased χ; hence, the feedback transistor channel charge injection is increased. From figure 4.3, an increase in feedback transistor charge injection leads to a decrease in offset for a dominate first stage. At temperatures in excess of $25°C$, the offset is negative and decreasing with increasing temperature. As the delay is increased beyond 3ns, the offset is a function of a temperature dependent first stage amplifier transient response.

The threshold of an MOS device decreases as the temperature increases.

$$V_T = V_{T(25°C)} - 2.3 \cdot \frac{mV}{°C}(T - 25°C)$$

4.11

where T is the applied temperature. From equation 2.5 page 19, the channel charge increases as the threshold is decreased. Therefore, as the temperature increases from -55 to 125, the channel charge injection increases. This leads to increased step inputs to the amplifier stage, resulting in larger output peak swings.

Although the charge injection is smaller at cold temperatures, the variations with delay are larger at these temperatures. At cold temperatures, the larger electron and hole mobilities lead to increased currents. These increased currents lead to faster response times in the comparator, yet increased ringing results. This increased ringing is seen in the offset variation with delay.

As the delay increases to 25ns the amplifier response has settled, resulting in small offset variations as the temperature is changed. Beyond 50ns, the offsets become excessively large. This occurs at smaller delays for $-55°C$, while $125°C$, the offset remains flat. Recalling the results of experiment 4, where this phenomena occurred for smaller delays at V_{dd}=5.5 then V_{dd}=4.5, the amplifier response time is faster at V_{dd}=5.5v and cold temperatures, the extreme offset voltages at long delays are a function of comparator response time. The faster the comparator, the less delay required for the dummy devices to force the offset excessively positive.

For variations in power supply voltage and temperature, a window 25ns to 50ns exists where the offset is small. Outside this window, excessive offset voltages result from the sampled first stage transient response at short delays. Large delays lead to response time sensitive positive offsets.

4.7 Experiment 7: Offset Vs. Bias Current for Differential Comparator

In experiment 7, the output of the differential ended comparator is monitored for the offset voltage. The pin *CBIAS* is varied for a fixed V_{dd}=5.0v and the offset measured. As *CBIAS* is varied, the bias current and trip point of the comparator change (see figure 3.10 page 60). As shown in figure 4.20, the zero delay offset falls in two distinct regions of operation.
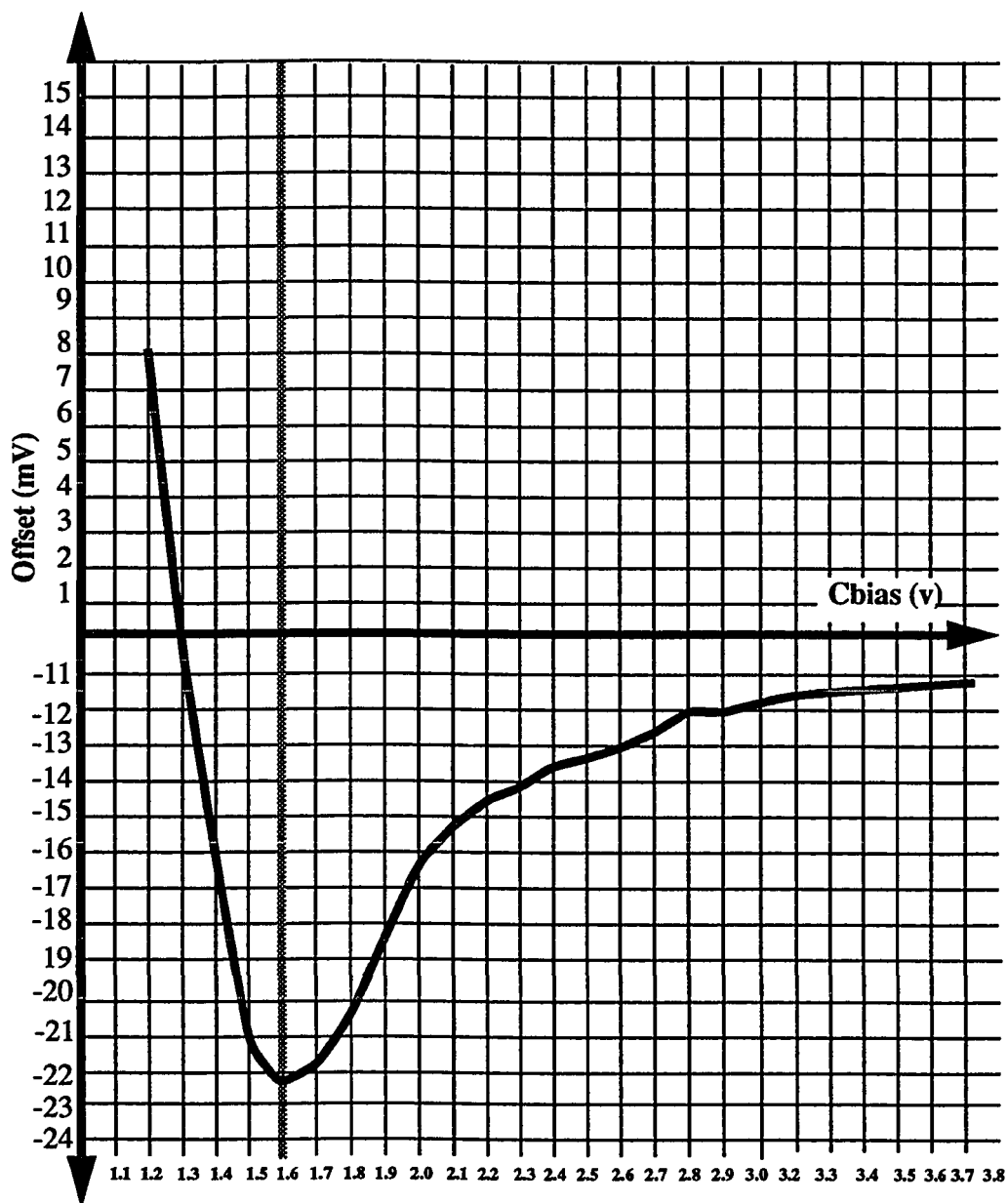

FIGURE 4.20 Offset Vs. Bias Current

As *CBIAS* is increased, the internal bias current is increased; furthermore, the trip point is decreased with increasing current. This decrease in trip point results in larger channel charge injection due to more overdrive on the feedback switch and dummy devices. Small bias currents result in less channel charge injection. For CBIAS less than 1.6v, the offset decreases with increasing bias current.

Once *CBIAS* reaches 1.6v, the offset increases with increasing current. The reduced trip point resulting from the increased current leads to more channel charge injection. Along with trip point, an increase in bias current leads to reduced gain (λI_D is increasing). Gain reduction results in larger second and third stage error contributions to the overall offset.

All first order effects resulting from mismatched charge injection between the dummy device and feedback switch are cancelled by the differential structure of the comparator. The offset variation is due to common mode errors. From previous experiments under normal conditions (T=25°C and V_{dd}=5v), it was determined the feedback device contributes more to charge injection than the dummy devices. Therefore, an increase in channel charge injection leads to an increase in input step size. As Vtrip decreases, the channel charge injection increases leading to increased common mode input signals and offset errors.

4.8 Experiment 8: Offset and PSRR Vs. Delay for Differential Comparator

In experiment 8, the differential comparator is biased at CBIAS=2.5v and the delay between auto zero signals swept. The offset was measured at V_{dd}=5.5v and V_{dd}=4.5v for each delay time. The results are plotted in figure 4.21.
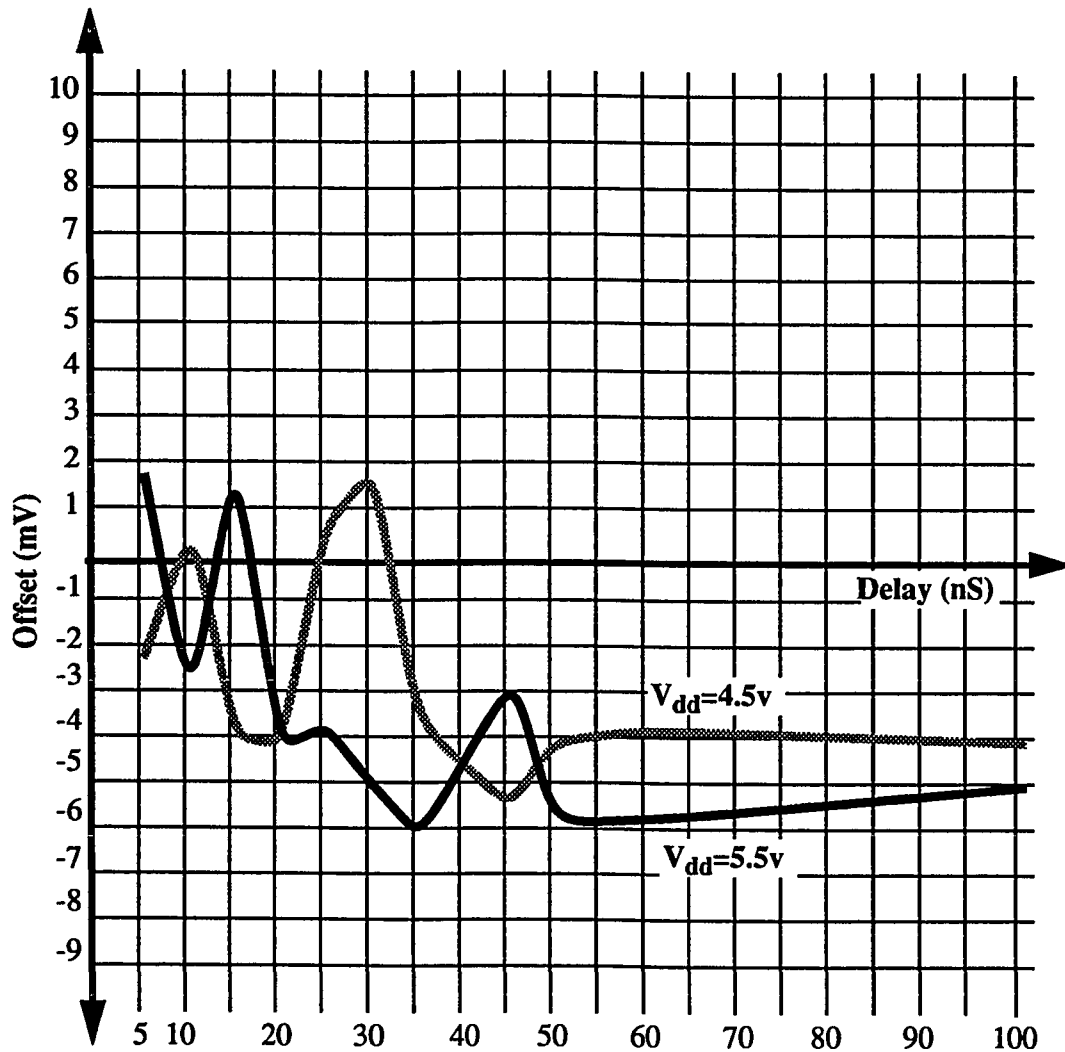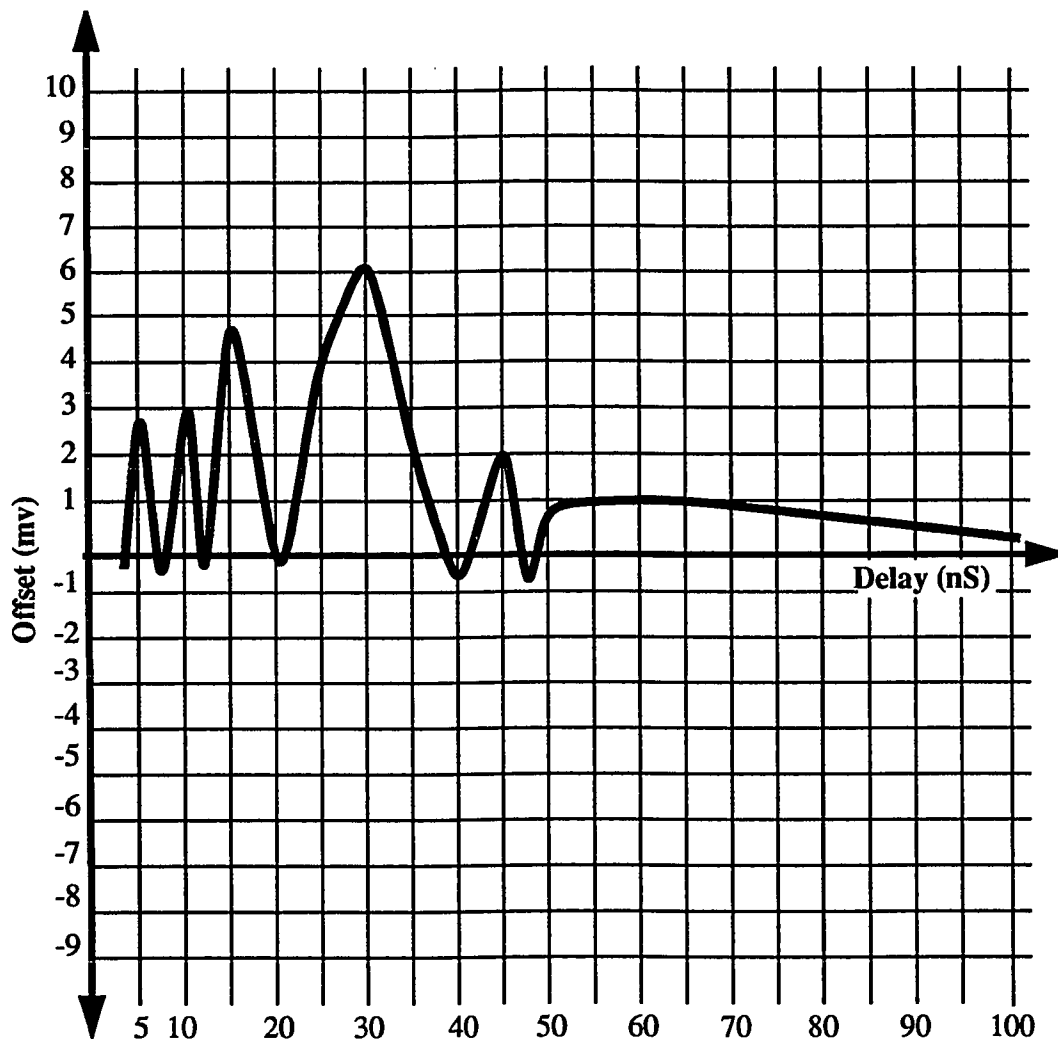

FIGURE 4.21 Offset Vs. Delay for Differential Ended Comparator

Along with the offset vs. delay, the PSRR vs. delay was determined as the difference in offset voltages for V_{dd}=5.5v and V_{dd}=4.5v. Figure 4.22 shows the results of this calculation.

FIGURE 4.22 PSRR Vs. Delay for Differential Ended Comparator

For small delays (5ns), the offset is small. In this region of operation the comparator output response has not peaked. Furthermore, the PSRR is small (0.4mv). As the delay is increased, the offset vs. delay begins ringing in a damped sinusoidal function. The ringing period is longer for the differential ended comparator relative to the single ended comparator (see figure 4.6). The offset ringing does not settle until the delay reaches 50ns.

At V_{dd}=5.5v, the peak value of the offset is -6mv. Under the same conditions, the single ended comparator has a peak offset of -23mv. The offset is significantly lower for the differential ended comparator. The differential ended comparator has both inverting and non-inverting inputs. For an ideally symmetrical differential comparator, equal step inputs to the positive and negative input terminals result in no transient output signal. The inputs are common mode, cancelled by the circuit's symmetry. In the real differential ended com-

parator, second order effects such as device mismatch and unbalanced charge injection (see figure 3.13 page 63) lead to common mode errors. These common mode errors are amplified by the first stage and result in a ringing function similar to figure 4.21. The single ended comparator has only a positive input terminal; hence, all the charge injection is seen by the input terminal. This leads to a larger error step input and larger peak transient response.

The power supply rejection ratio reaches a peak value of 6mv. This occurs at a delay time of 30ns. At 30ns, the offset has settled for V_{dd}=5.5v due to the faster response time at higher supply voltages. For V_{dd}=4.5v, the offset voltage is peaking out at 30ns. This phase difference results in the large PSRR error.

For delays in the range 5ns~30ns, the PSRR is ringing. This results from the ringing offsets vs. delay and the phase shift in offset vs. delay between V_{dd}=4.5v and V_{dd}=5.5v. Several instances in time, the transient offset at V_{dd}=4.5v is equal to the transient offset at V_{dd}=5.5v. For delay times coinciding with these transient time points, the PSRR is zero. Although the PSRR is zero at these instances in time, designs using fixed delays corresponding to these cancelation points exhibit strong sensitivities to the amplifier transient response. These cancellation points are dependant upon temperature, process, and supply voltage.

Increasing the delay beyond 35ns results in optimum offset variations and PSRR errors. The offset settles to -5mv. This offset results from the excessively large feedback devices used to allow charge injection to dominate the offset. In this region of operation, the delays have exceeded the response of the differential amplifiers.

Unlike the single ended amplifier, for excessive delays (>100ns), the offset remains flat for the differential amplifier. The offset of the single ended amplifier became excessively large for delay times greater then 65ns (see figure 4.13). Any error generated by the dummy devices (or other sources) when applied to differential amplifier is only a common mode signal; thus, any offset errors are reduced to second order common mode errors.

4.9 Experiment 9: Power Supply Rejection Ratio at a Forced Swing.

In this experiment, the voltage swing driving the dummy devices and feedback switches is held constant while the supply voltage was varied from 4.5 to 5.5 volts. The offset was determined at various delay times between auto zero signals for the differential ended comparator. The swing of the signal driving the charge injection devices is held at 4v for all cases. The results of the experiment are shown in figure 4.23.
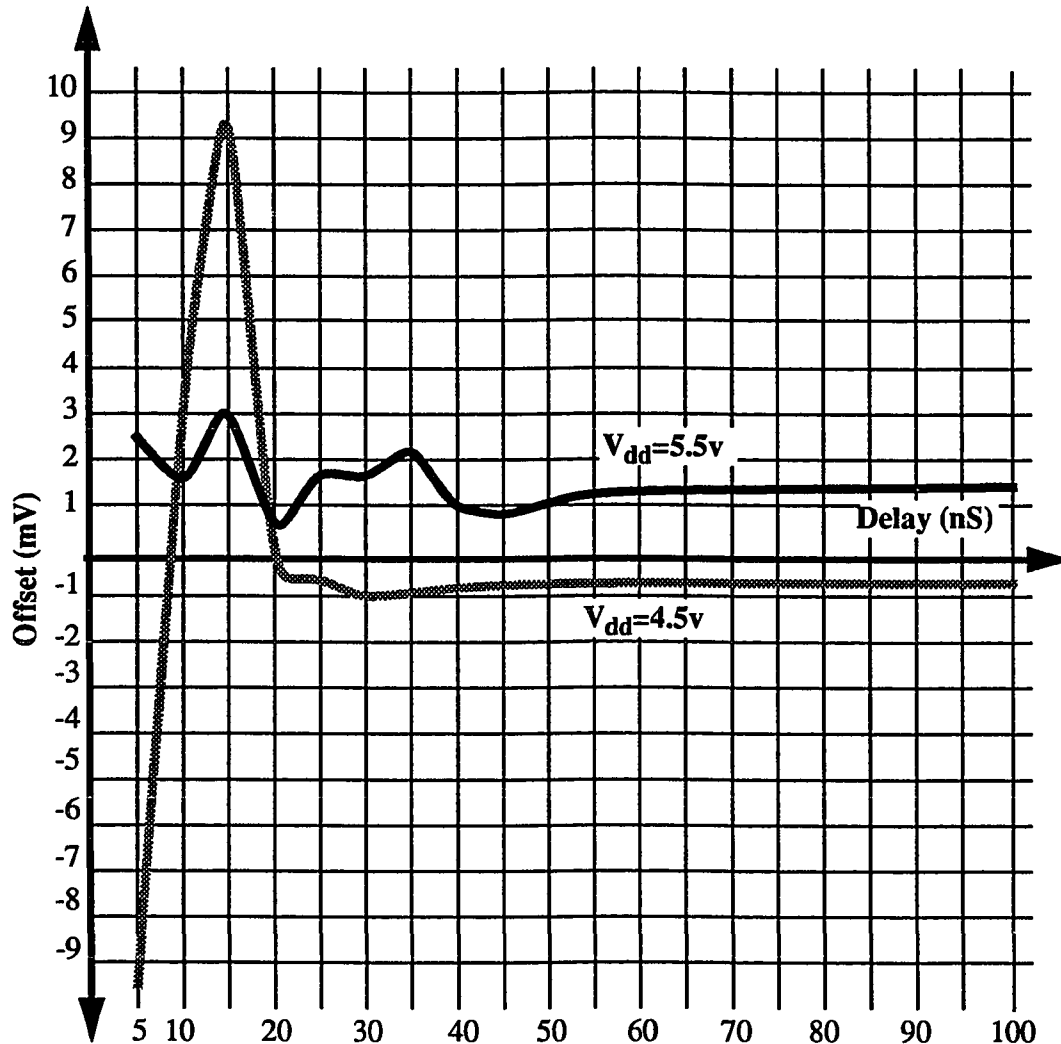

FIGURE 4.23 Offset Vs. Delay for Fixed Swing

For V_{dd}=4.5v, the offset variations are large for delay times less than 20ns. At V_{dd}=5.5v, the offset is relatively flat for all delay times. For V_{dd}=4.5v, the trip point of the comparator is lower than the trip point at V_{dd}=5.5v. For a constant swing of 4v, the channel charge injection is larger at V_{dd}=4.5v due to the lower trip point. This leads to a larger

charge injection step input; consequently, the peak output transient swings are larger for a supply voltage of 4.5v in comparison to 5.5v. These peak transient spikes are captured at the input of the second stage when its auto zero signal is turned off. This results in large offset voltages for the entire comparator at V_{dd}=4.5v.

Along with increased charge injection at V_{dd}=4.5v, the response time of the comparator is slower. This leads to longer settling times required for the first stage amplifier to respond to the charge injection step input voltage. This leads to poor PSRR for fixed swings resulting from the dependence of channel charge injection on trip point voltages.

The ringing at V_{dd}=5.5v is five times smaller in magnitude; consequently, the net charge injection due to the overlap capacitance of dummy device and feedback switch is nearly cancelled by the inverse clocking signals. PSRR is not due to the overlap capacitance of the switches, it is due to the mismatches in channel charge injection.

5.0 Conclusion

The offset of a comparator as the delay is varied between auto zero signals is a function of the output transient response of the first stage amplifier. The charge injection at the input of the first stage amplifier is dominate in comparison to the second and third stages. The error voltage input to the first stage is a step function due to unbalanced charge injection between the feedback switch and dummy devices. The amplifiers step response is a damped sinusoidal function. This charge injection induced output of the amplifier drives the input of the second stage amplifier. Once the feedback switch is opened on the second stage amplifier, the instantaneous output of the first stage is held on the second stage high impedance input node. This voltage level attenuated by the gain of the first stage amplifier is the comparator offset.

The power supply rejection ratio of the offset voltage is a function of the amplifier transient response variation over supply voltage. The transient response is a function of amplifier settling time and input step level. As the supply voltage is increased or the temperature is decreased, the amplifier settling time is reduced. The difference between offset voltages at V_{dd}=4.5v and V_{dd}=5.5v is large for delays less than the amplifier settling time due to phase differences in the response times. For a given delay, the response at one supply voltage is at its maximum, while the response at another is at its minimum. The PSRR is optimized for delay times between auto zero signals in excess of the worst case amplifier settling time. A window of min/max delays exists where the offset error is small as the supply voltage and temperature are varied.

Dummy devices cancel the effects of overlap capacitance charge injection (Q_{ov}) significantly. The offsets resulting from charge injection are primarily the result of mismatches between the channel charge injection of the feedback switches and dummy devices. Both the source and drain of the dummy device tie to the high impedance storage node; hence, all its channel charge contributes to the variation in voltage on the storage node. Conversely, only the source of the feedback switch ties to the high impedance storage node. The fractional percentage of charge leaving the source (χ) is a function of temperature and supply voltage. In cases where χ is too large compared to the fixed dummy devices, increased channel charge results in negative offsets due to excessive charge exiting the source of the feedback switch.

The PSRR was not reduced by applying a supply independent swing on the feedback switches and dummy devices. The effect of trip point dependent charge injection leads to large PSRR errors as a result of channel charge mismatch. As the supply is increased for a fixed swing, the trip point increases resulting in less channel charge injection and smaller step inputs. As the supply is decreased, larger step inputs lead to increased peak transient response. Coupled with longer amplifier response time, the variation in offset at 4.5v leads to large PSRR errors. Once the delay exceeds the amplifier response time, the PSRR and offset errors are significantly reduced. The required delay to achieve optimum PSRR and offset errors is reduced as the feedback switch swing is reduced.

The experiments in forced charge injection by smearing excessive capacitance into the input nodes of the comparator were unable to be performed due to a fabrication error. The

parts contained a thin oxide layer blocking the top layer metal from the microscopic probes. Fortunately, the devices were designed larger than necessary resulting in excessive charge injection.

In a practical application, the circuit used on this test chip will be placed in a 12-bit analog to digital converter. The delay between staggered auto zero signals can be varied through an externally programmable RAM. The results of this thesis are very promising in the improvement of offset and PSRR errors associated with conventional ADC architectures. This work serves as a guide line in the design of such comparators in complex analog systems.

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Appendix

The appendix consists of oversized plots of the layout and schematic.

delay

delay

supply

supply

chias

sah

reset

chias

sah

reset

vinn

vinp

vinn

vinp

iclk

iclk

delay

supply

delay

supply

chias

sah

reset

chias

sah

reset

vinn

vinp

STAGE

STAGE

STAG

STAGE4

STAGE4

STAG

DELAY

DELAY

DELAY

DELAY

DELAY

DELAY

CONTROL

CONTROL

CONTROL

CONTROL

delay
delay
supply
supply

cbias
sqh
reset
vinn
vinp
cbias
sqh
reset

STAGE
STAGE
STA

vinn
vinp
iclk
iclk

delay
supply

delay
supply

STAGE4
STAGE4
STAG

cbias
sqh
reset
vinn
vinp

cbias
sqh
reset
vinn
vinp

iclk

iclk
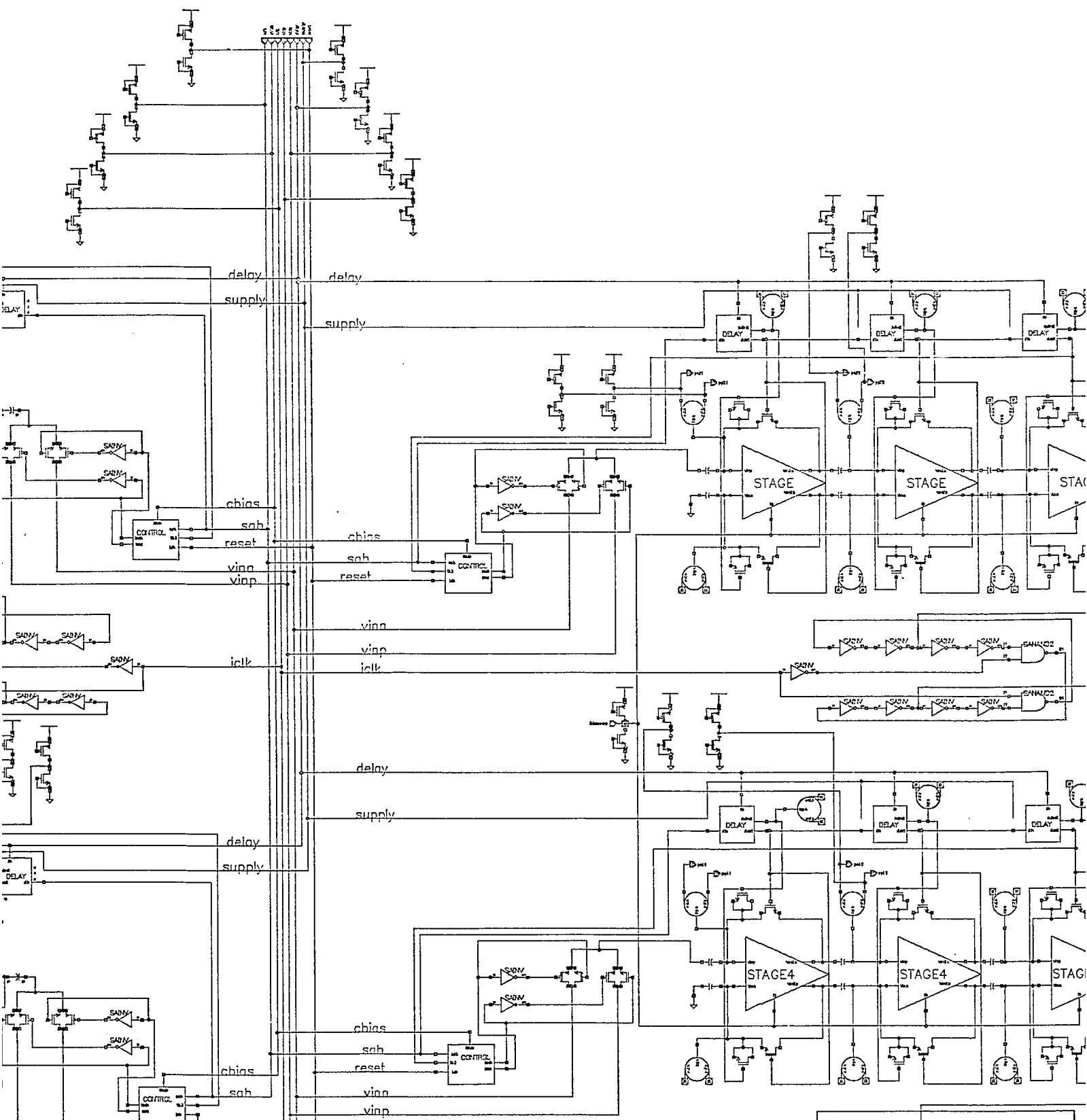
DRAWN
CHECKED
CHECKED
CHECKED
ISSUED

5   4   3   2

STAGE STAGE STAGE

3

STAGE4 STAGE4 STAGE4

4

cbias

iclk

dout4

avdd

pp12

pn12

avss

dout1

avss

sah

avdd

DAKP100GA

avdd

pp12

pn12

avss

dout1

pp32

pn32

pp31   pn31   supply   avdd   avss   delay

DAKP100GA

CM
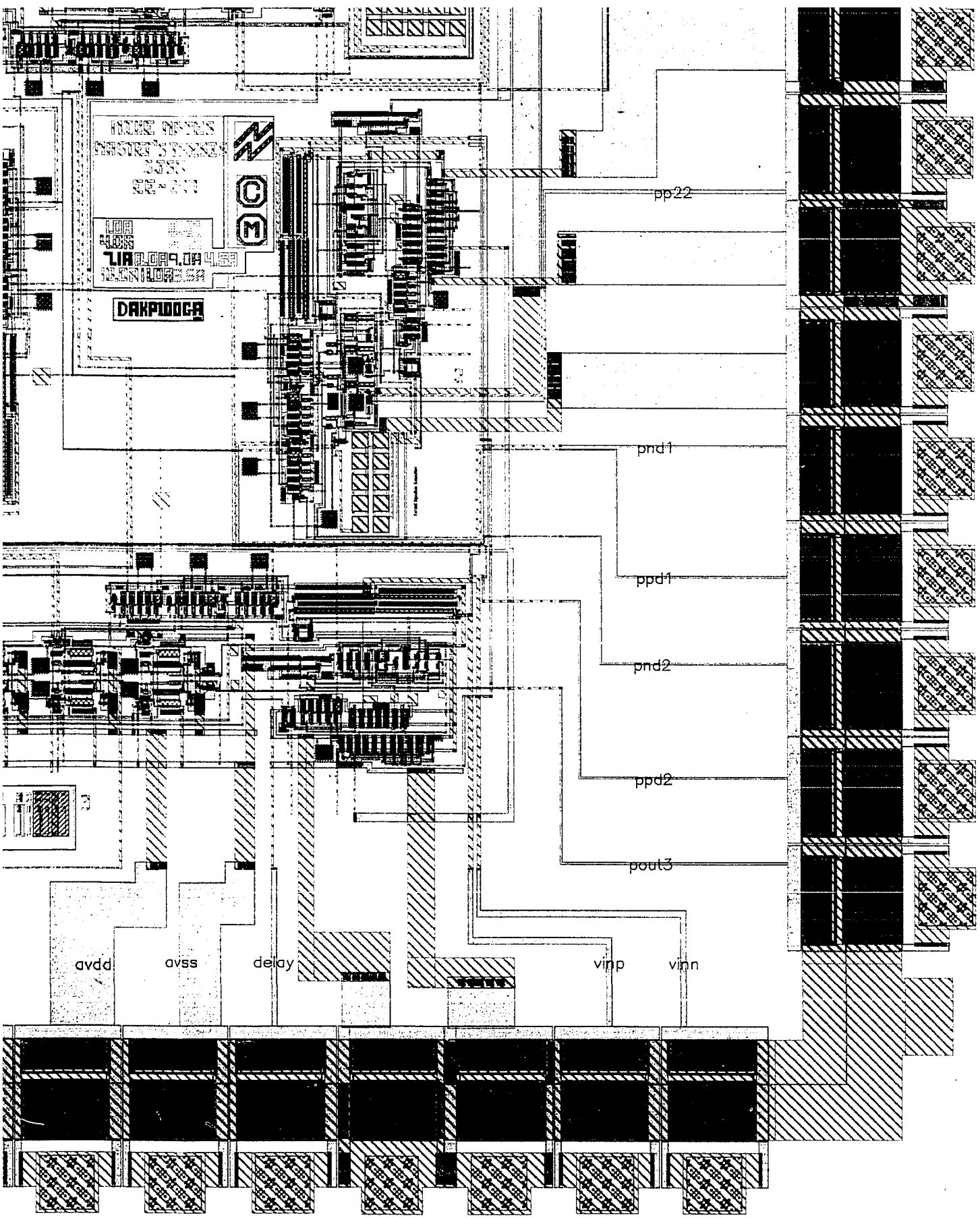
pp22

pnd1

ppd1

pnd2

ppd2

pout3

avdd   avss   delay   vinp   vinn

DAKP100GA

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