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A low-noise, low-power circuit for impedance measurement of biological processes

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A LOW-NOISE, LOW-POWER CIRCUIT FOR IMPEDANCE MEASUREMENT OF BIOLOGICAL PROCESSES

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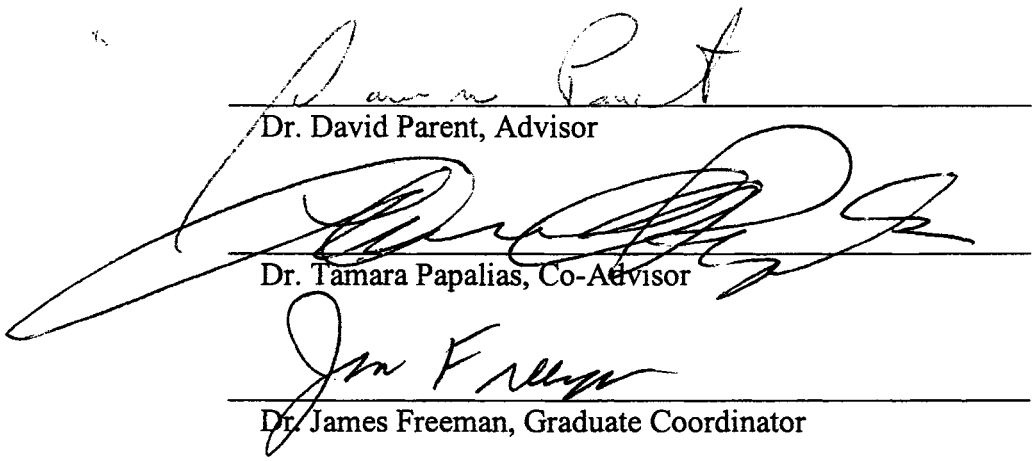

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ABSTRACT

A LOW-NOISE, LOW-POWER CIRCUIT FOR IMPEDANCE MEASUREMENT OF BIOLOGICAL PROCESSES

by Daniella Schefer

Electrochemical impedance spectroscopy has been a commonly-used technique in biomedical applications. With the advent of implantable impedance sensors, the requirements of these devices have become ever-more demanding. Small-scale ICs and low power use are necessary, and speed of measurement in non-stationary biological environments is also a concern.

To address these issues, a microscale, low-power integrated circuit has been developed in MOSIS using AMI 0.6um technology. The circuit is capable of receiving a dc and an ac signal (a frequency sweep from ~1kHz – 1MHz). In contrast to traditional electrochemical impedance spectroscopy, this novel circuit design, composed of a low-noise, low-power VLSI potentiostat with an injected ac signal, allows the simultaneous measurement of dc and ac impedance with very low power dissipation.

Equivalent electrode circuit components can be accurately measured and the frequency response of the device under test verified.

Acknowledgements

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1. Introduction

Electrochemical impedance spectroscopy (EIS) has long been the leading tool for characterization of electrode-electrolyte impedance [1]. Its usefulness has been demonstrated not only in the study of metal corrosion processes, but in biological systems and medical applications as well [2, 3]. Especially in the medical realm, exact characterization of the impedance of a neural medium is critical to gain information about, for instance, the occurrence of inflammation or tissue necrosis.

Demanding requirements of speed and accuracy for electrochemical systems have necessitated the development of faster and more sensitive circuits. Various circuits may be found in the literature [4, 5]; most, however, use large-area components (e.g., DACs, ADCs, commercial potentiostats) and are not sensitive enough for biological measurements. Along with low area and sensitivity, such a circuit would have to be capable of operating at high frequencies and be low-power enough to not damage the biological system under investigation.

Such a circuit has been developed using CMOS technology [6]. It has heretofore only been used with a DC bias voltage. This circuit is capable of measuring currents as low as 1pA, requires very little die area and power, and is very low-noise. Moreover, since it collects the data at the output prior to amplification, signal integrity is retained and quantization error reduced. These properties make it a good candidate for biological applications. The circuit consists of a potentiostat, followed by a comparator for recording the data.

In the course of this thesis work a realization was reached: there had been ample progress in the area of developing new techniques and algorithms for applying a signal to an electrode circuit and analyzing the impedance data. In terms of development of new circuit design, however, very little headway had yet been made. In the traditional application of EIS to corrosion analysis, advancements in design of measurement equipment was unnecessary. In biological measurement, however, circuit design is arguably of greater importance. There was a dearth of novel circuit design coupled with innovative measurement techniques.

The goals for this work were as follows:

(1) To develop a novel circuit design which could potentially be implemented in a biological environment – among other specifications it should be low-power, low-noise, have good accuracy and be of small enough size so as to be potentially implantable.

(2) To apply a known, validated method of analysis to the circuit, to verify that it would perform under conditions of simultaneous dc and ac excitation and to compare the generated results with those of other researchers doing identical analyses.

2. Electrochemical Impedance Spectroscopy

An electrochemical cell is normally composed of two or three electrodes (reference and working, and perhaps counter electrodes) immersed in an ionic solution (see Figure 1). The potential of the reference electrode is held constant, so that any electrical changes in the cell may be ascribed to the working electrode [1]. If the potential at the working electrode is raised with respect to the reference electrode, there is a flow of electrons from solution to electrode, representing an oxidation current. If the potential at the working electrode is lowered with respect to the reference electrode, there is a flow of electrons from electrode to solution, representing a reduction current.

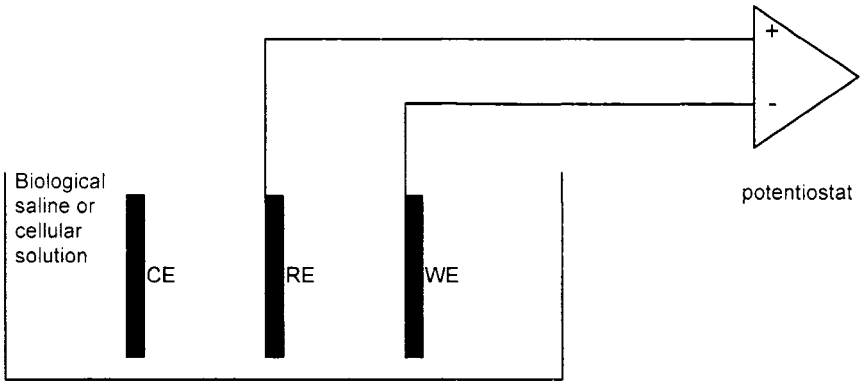

Figure 1—Electrochemical impedance spectroscopy measurement system

In order to measure the impedance, then, of an electrochemical cell, a voltage is applied at the working electrode and the current between the electrodes in solution is measured. The impedance of the cell is composed of resistive and capacitive elements (the inclusion and architecture of elements being based on the composition of the electrochemical cell, as well as the electrical characteristics under which the impedance is measured) [1]. These faradaic (mass transport effects) and non-faradaic (arising from the

solution resistance and the interface capacitance) elements come into play at various frequencies, and may therefore be included or excluded based on the measurement parameters.

3. EIS for Biological Applications

Electrodes for biological applications are normally fabricated from an inert metal like platinum or gold and are immersed in a saline solution in vitro or in physiological tissue in vivo [2]. The reference electrode is normally fixed by choosing a material with a known impedance such as the Saturated Calomel Electrode.

In biological measurements, there are three distinct ranges of frequency exhibiting various characteristics (see Figure 2). From dc to 100Hz, the surface area and material of the electrode as well as the dc potential on the electrode exhibit a primary role in determination of the impedance. At low frequencies, from dc to 100Hz, because of the primary role of surface area and electrode potential, kinetic reactions of the electrode-solution milieu determine the impedance. Diffusion or adsorption, charge transfer and interface polarization dominate the impedance characteristics. In the high-frequency range, from 1kHz to 100kHz or higher, impedance is determined by the geometric area of the electrode and the properties of the biological solution in which the electrodes are immersed. In the middle frequency range, from 100Hz to 1kHz, determining factors are a mixture of the low and high frequency characteristics.

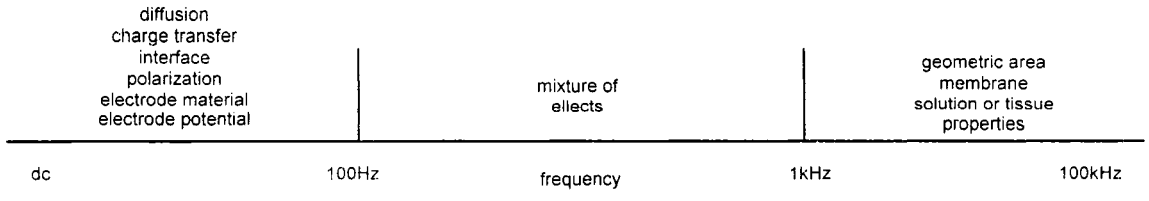

Figure 2—Frequency-controlled electrode/electrolyte properties[3]

Various authors have proposed equivalent circuits to measure the electrical characteristics of the electrode/electrolyte interface, the first of which was developed in 1899 and known as the Warburg model of impedance [7]. It can be thought of as a diffusion or mass-transfer impedance in series with a charge-transfer resistance, important under low frequency or dc conditions, though less so at high frequencies. Its impedance can be modeled as in (1) [8].

$$Z_W(\omega) = R_W + W_0 / \sqrt{j\omega} \tag{1}$$

where

ω is the frequency

R_W is the charge-transfer resistance

W_0 is the diffusion impedance

A second equivalent model of impedance, known as the Randles' circuit [9], is shown in Figure 3, where W is the Warburg impedance, C_i is the interface capacitance, due to charge separation close to or at the surface, and R_s the solution resistance.

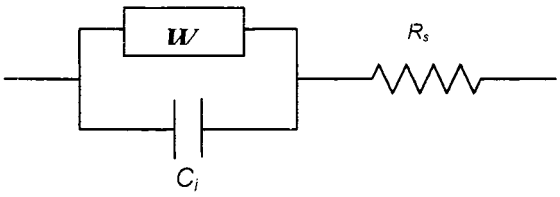

Figure 3—Randles' equivalent circuit

This equivalent circuit model takes into account the resistance of the solution (physiological saline or living tissue in biological systems) and the interface or membrane

capacitance as well as the lower-frequency diffusion characteristics. If the diffusion- or Warburg impedance is neglected (which can be assumed above approximately 1kHz [2]), then the equivalent electrode circuit may be viewed as in Figure 4.

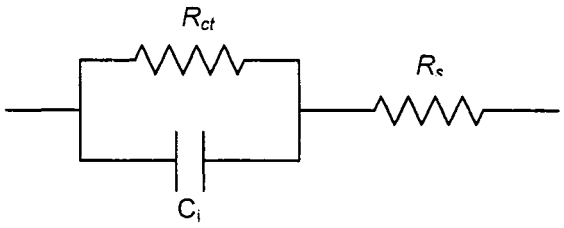

Figure 4—Randles' equivalent electrode circuit for higher frequencies

There are three main components in this model, the impedance of which may be described by the equation in (2):

$$Z = R_1 + \frac{R_2 - j\omega C R_2^2}{1 + \omega^2 C^2 R_2^2} \tag{2}$$

From this equation, the real and imaginary parts of the impedance can be derived as in (3) and (4):

$$Z' = R_1 + \frac{R_2}{1 + \omega^2 C^2 R_2^2} \tag{3}$$

$$Z'' = -\frac{\omega C R_2^2}{1 + \omega^2 C^2 R_2^2} \tag{4}$$

Other authors [3, 8, 10] have proposed more complex equivalent circuit models, based on the composition of the electrode/electrolyte milieu and the specific frequencies under investigation.

The behavior of the circuit is also different based on the different dc potential applied to the reference electrode [11] (see Figure 5). For instance, in region A, at low potential, diffusion resistance R_d >> charge-transfer resistance R_{ct}. Therefore the diffusion impedance can be much greater than the charge-transfer resistance, even at high frequencies. In region B, R_d and R_{ct} are approximately equal, and thus the diffusion impedance can be neglected at high frequency, though important at low frequency. In region C, R_{ct} >> R_d, and diffusion impedance has little or no effect on circuit behavior.

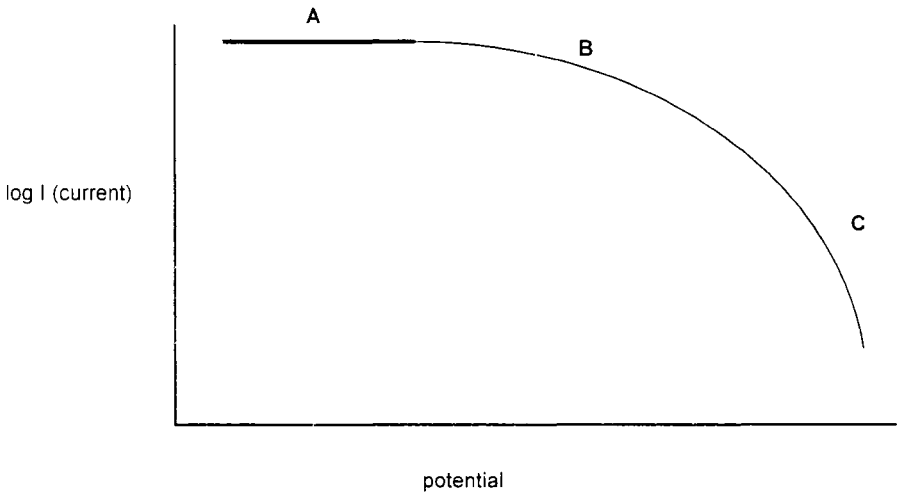

Figure 5—Potential – current diagram illustrating regions of differing impedance characteristics [1]

4. Methods of EIS Applied to Biological Systems

In the simplest measurement setup, a dc potential is connected to the working electrode of an electrochemical cell and the dc current measured [5]. This is known as the dc ohmtest method. Since the voltage sources and current sensor are external equipment, accuracy is reduced, in addition to the fact that in many cases, too much power is generated for use in a biological system.

A second method applies a potential step, so that the instantaneous response of the circuit can be measured. This process is known as chronocoulometry. A diffusion-based current is forced and the impedance of the circuit measured. This method is useful for finding the dc or low-frequency components of the impedance.

A linear dc sweep, composed of many small frequency steps, is the logical next step, providing additional information about the impedance at various potentials. In this way, the electrode impedance during either an oxidation or reduction reaction can be found.

Implementation of both a positive and negative sweep is known as cyclic voltammetry. This method, a bi-directional sweep, in which a voltage may be swept from –2V to 2V and back to -2V in 0.01V increments, can yield the impedance of oxidation (cathodic) and reduction (anodic) reactions, how the impedance behavior in these reactions differs and whether the reactions are reversible or not [1].

Yet a more complex method is termed potentiodynamic electrochemical impedance spectroscopy (PTEIS), where an ac signal is applied on top of the linear dc sweep. This method, of course, yields the higher-frequency components of impedance, while maintaining the lower-frequency diffusion-controlled reaction components. For example,

in [12], a staircase potential scan was applied to reversible and non-reversible systems. A signal amplitude from 5 to 10mV was applied to the electrodes, with the staircase potential step being much smaller than this. Bode plots (low frequency in this case) were then generated for each potential step. Based on preliminary spectral data, the authors constructed various possible equivalent electrode circuit models. Then, using curve fitting methods, the authors chose the most likely equivalent circuit based on the various components of impedance.

In [5], various other methods for testing the impedance of an electrochemical system are discussed, including the single frequency method, which can measure changes in impedance over time. It can also provide increased accuracy of measurement, since the measurement system and parameters are optimized for that one particular frequency. Problems, of course, include the lack of data at other frequencies as well as choosing the best equivalent circuit model for that frequency.

Expanding this tactic to include a swept ac frequency is the method known as ac voltammetry, which provides the response of the circuit along the entire swept frequency spectrum. The uncertainty as to the correct circuit model is increased greatly, and whether the data along an entire frequency spectrum is valid for that particular circuit model is called into question.

If the ac frequency sweep is superimposed on top of a dc staircase sweep, there are even more factors in question—recall the potential/current impedance dependency curve mentioned previously. Also, this method can be time-consuming since a Bode (or

Nyquist) plot is generated for each step of the dc potential sweep (e.g., an ac voltammetry sweep from –2V to 2V along 0.01V increments would yield 400 Bode plots).

Measurement time may not pose a problem for characterization of corrosion processes, but for biological environments, if the biological environment is transient (i.e., changes its composition or behavior over time), correct characterization may prove more difficult. Some researchers [13] have implemented techniques known using a Fourier transform to analyze the response of the circuit. In Fourier Transform Electrochemical Impedance Spectroscopy (FT-EIS), a collection of various frequency sine waves (or a noise signal) is applied to the circuit, and the resulting Fourier spectrum measured.

In [14], a short-time Fourier transform is applied to a cyclic voltammetry analysis. The authors explain that the application of this short-time Fourier transform (STFT) can yield simultaneous information about time and frequency data. Since this technique allows simultaneous measurement of many frequencies, it is much faster than previous methods.

As the implementation of impedance-measuring devices in biological systems became more widespread, the requirements for such devices became more stringent. Portability, low-power (so as not to damage the cellular milieu under investigation), and the aforementioned speed of measurement are critical specifications in the area of medical diagnosis. The interface [3] between the device and the environment, as well as the size, especially in implanatable devices [15], are notable concerns. Traditionally, the electrochemical cell was connected to a power supply and the received signals were directly routed to a large impedance meter. In biological solutions, however, levels of

current and voltage are by nature very small (e.g., action potentials in a neural solution [16]). Cellular signals must be amplified in order to be measured, and the signal must be digitized for signal processing to occur. Noisy measurements are therefore always an issue.

Various circuits have been developed to meet the raised requirements of impedance measurement in biological systems. Some of these measurement systems have employed enhanced techniques [10, 12, 13], while maintaining more-or-less traditional architecture. Others have implemented novel circuit design, which may or may not be coupled with novel measurement techniques. Depending on the application, various parameters (e.g., low-noise, low-power, accuracy, measurement speed, among others) may be optimized to meet various requirements [5].

5. Measurement Techniques

Among the various ways to measure impedance described above, the technique known as Fourier Transform Electrochemical Impedance Spectroscopy (FT-EIS) requisites further mention. In [13], such a measurement setup is implemented. An arbitrary waveform composed of 190 frequencies is superimposed on a dc sweep from –2 to 2V. A high slew rate amplifier supplies the collection of signals to the reference electrode. The signal from the working electrode is amplified, digitized, and stored on a computer for later FFT analysis.

Biological systems are by nature non-stationary. And gathering data with EIS, that is, applying an AC voltage signal over a number of frequencies to generate a Nyquist or Bode plot, normally requiring a few minutes time, can lead to error if the composition of the neural medium changes over the duration of the measurement. In EIS, it is also difficult to tell the difference between anodic and cathodic processes [1]. Time-resolved FT-EIS was developed to expand the capabilities of traditional EIS [13]. FT-EIS allows the simultaneous collection of kinetic (ac) parameters with potentiodynamic (dc) data. In FT-EIS, a white-noise (or multi-frequency) signal is generated concurrent with a swept DC voltage. This simultaneous application of sine waves of many different frequencies allows characterization of the impedance of the equivalent circuit within a very short time. This speed allows fast measurement of changing biological systems. With FT-EIS, it is also possible to deduce information about the various kinetic and diffusion mechanisms taking place within the circuit; for instance, by noting the behavior with frequency of the resistance and capacitance of the electrode in the equivalent circuit

(whether they vary together or in opposite directions), one can deduce which processes are coupled or uncoupled.

The method is viable for biological impedance characterization because of its quick measurement time and frequency range measured. Response of the circuit under conditions of oxidation and reduction can be differentiated. FT-EIS can also distinguish between kinetic reactions and electrochemical data based on the frequencies at which these processes occur. A large amount of data can be generated simultaneously, and then averaged, increasing the accuracy of the measurement. Drawbacks of this implementation are, however, the presence of the digital to analog and analog to digital converters, which, for low-noise applications, would have to be built on-chip, making the chip prohibitively large for biological applications.

6. Circuit Design Techniques

In [17], Angrisani *et al.* describe a digital signal processing instrument for impedance measurement. With this device, tracking of a time-varying impedance can be accomplished. The authors claim to reach a high level of accuracy in short measurement times. With a first technique, called the amplitude-phase technique, a sinusoidal signal and a voltage potential are applied to an electrode circuit and the output voltage sampled. Looking at the unknown impedance $Z_x = R_x + jX_x$, the real and imaginary parts of the impedance can be given by $R_x = |Z_x| \cos\varphi$ and $X_x = |Z_x| \sin\varphi$, where $|Z_x|$ and φ are the magnitude and phase of Z_x, respectively. Then, defining U and V_x as the rms values of the applied signals, $u(t)$ and $v_x(t)$, we obtain $|Z_x| = \frac{V_x}{U - V_x} R_r$. The phase φ is the displacement between the voltage drop $v_x(t)$ and the current $i(t)$ flowing into the impedance Z_x given by $i(t) = \frac{u(t) - v_x(t)}{R_r}$.

In a second technique, called the virtual bridge method, the measurement setup is identical to the approach used in ac bridge methods, except that the bridge reference arm is virtual. The instantaneous out-of-balance voltage on the bridge is defined as the difference between the measured voltage and the simulated voltage, given by $v_x(i\tau_c)$ and $v(i\tau_c)$, respectively, where τ_c is the sampling period. In an iterative process, the difference between the measured and simulated voltage drops is minimized until a desired accuracy

is reached. The voltage drop of the virtual arm of the bridge is given as

$$\frac{v(i\tau_c) - v[(i-1)\tau]}{\tau_c} = -av(i\tau_c) + bu(i\tau_c)$$

where

$v(i\tau_c)$ is the i^{th} element of the virtual voltage drop

$u(i\tau_c)$ is the i^{th} element of the initial sinewave applied to the bridge circuit

a, b are constants depending on the virtual bridge configuration

Then, a particular impedance is considered. The derivative of the voltage drop on the virtual arm is given as $v(i\tau_c) = A\sqrt{2}(U\sin(\omega i\tau_c)) + B\sqrt{2}(U\cos(\omega i\tau_c)) + De^{-\omega i\tau_c}$, where $De^{-\omega i\tau_c}$ has to do with the initial conditions imposed on the circuit and can be neglected for steady-state conditons. The constants in the equation are: $A = ba\frac{1}{a^2 + \omega^2}$ and $B = b\omega\frac{1}{a^2 + \omega^2}$. The normalized value of the out-of-balance voltage is given as

$$V_{out} = \frac{1}{V_x}\sqrt{\frac{\sum_i [v(i) - v_x(i)]^2}{N}}, (i = 1, \ldots N)$$

where

N is the number of samples/period

The measurement setup uses two ADCs and two DACs (which sample at a maximum frequency of 96 kHz). The goal of the measurement is determined by the user: If instantaneous impedance information is required, R_x and C_x can be provided immediately. If greater accuracy is desired, several measurements can be taken and the results averaged.

The first technique provides a relatively short processing time and is intended for tracking of time-varying impedance. Its low level of noise rejection, however, could prove to be an issue. The second technique, which minimizes the out-of-balance voltage, V_{out}, is iterative, and thus more time-consuming. The last optimized values of R_x and C_x (or L_x) are supplied. Since the sampled signals are averaged in this technique, noise rejection is higher. Because of the large die area of the analog-to-digital and digital-to-analog converters, this impedance-measuring tool may not be the best candidate for biological applications. In addition, the sensitivity is probably not high enough for ion current measurements (pA level). While the total measurement time of the virtual bridge technique (5 to 10ms) is promising, no mention is made of the power consumption or the levels of current generated. Noise could also be an issue.

6.1 VLSI Potentiostat

In [6], a novel circuit is proposed which takes into consideration the low-power and low-noise requirements necessary for measurement in a biological medium. It can also measure ionic currents as low as 1pA (up to 200nA), with a maximum non-linearity of +/- 0.1% over the range. The circuit presented in this thesis is based on the circuit in [6]. It is shown in Figure 6. A high-gain (86dB), wide-range, cascaded operational transconductance amplifier (OTA) with high output resistance is used in a second-generation current conveyor (CCII) configuration. Based on the measurement, V_{pot} is either a constant voltage or a triangular waveform for cyclic voltammetry.

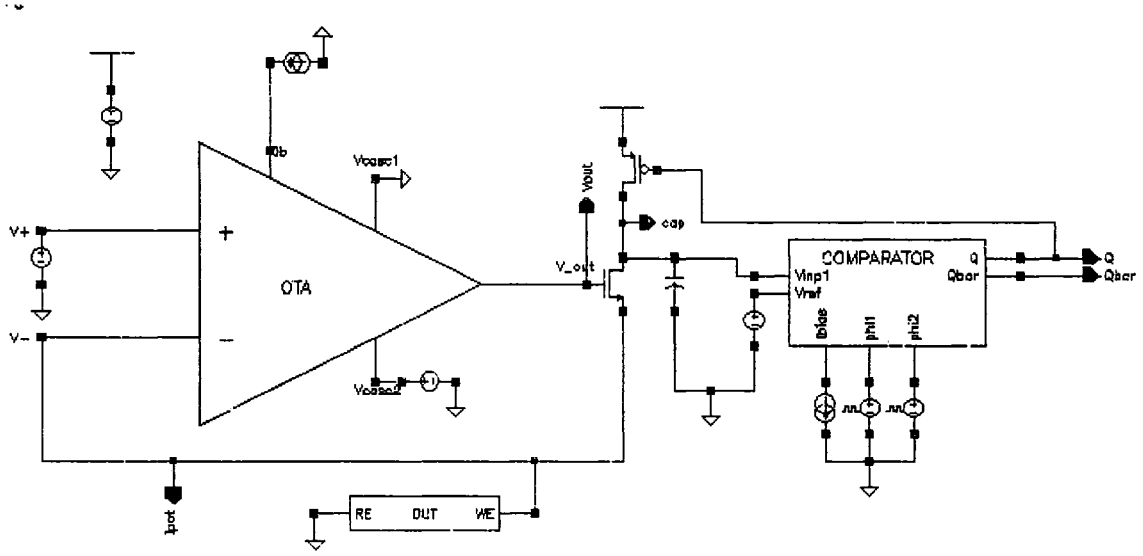

Figure 6—VLSI potentiostat used in ion current measurements

6.1.1 Circuit Operation

The load capacitor (C_d) is first charged to the supply voltage through the pmos transistor. Then, when the negative terminal has matched the voltage on the positive terminal of the amplifier (through a process of negative feedback), the capacitor discharges through the nmos transistor. When the capacitor has discharged to the level of the reference voltage at the input of the comparator, V_{ref}, a pulse is generated at the output of the comparator. The capacitor is then pulled high again by the pmos transistor. The current flowing through the electrode circuit (DUT) attached to the negative feedback loop of the amplifier can be computed by measuring the delay between the output pulses of the comparator, as shown in (5).

$$I = C\frac{dV}{dt} \tag{5}$$

where

C is the load capacitor

dV is the voltage on the capacitor

dt is the time between the comparator output pulses

The capacitor (C_d) value was found by simulation to be optimal at 1pF, thus reducing noise, but not slowing the system operation too much. Owing to the comparator and its "digitized" output, the circuit avoids having an A/D converter on-chip, giving it a small layout area.

6.1.2 Operational Transconductance Amplifier

The schematic of the operational transconductance amplifier is shown in Figure 7.

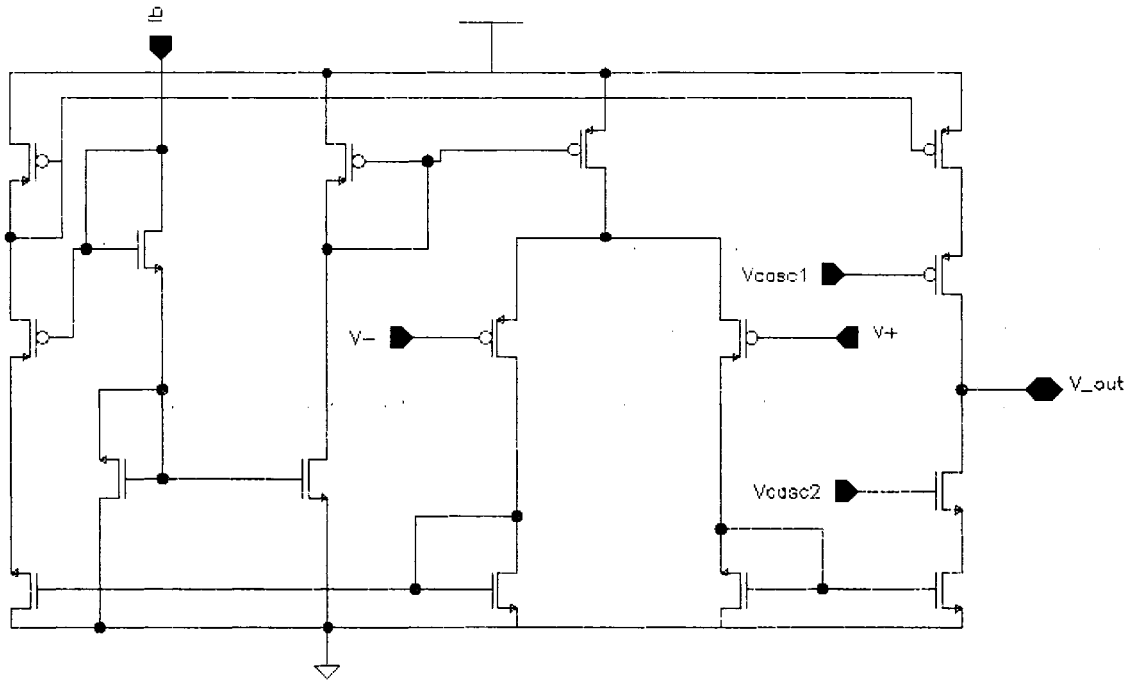

Figure 7—Schematic of OTA

The output of the OTA is designed for high gain, A_v, given in (6):

$$A_v = -g_{m1}(r_{01} // r_{02}) \tag{6}$$

where

g_{m1} is the transconductance of the nmos transistor

r_{01}, r_{02} are the output resistances of the nmos and pmos transistors

The gain due to the nmos is shown in (7),

$$g_{m1}r_{01} = \frac{1}{\lambda I_D}\sqrt{2\frac{W}{L}\mu_n C_{ox} I_D} \tag{7}$$

where

λ is the channel-length modulation coefficient and is proportional to $1/L$

To increase the gain of the nmos, its width was chosen to be $120\mu m$ (at minimum gate length). Since the gain of the nmos ($g_{m1}r_{01}$) increases as the drain current decreases, a lower current detection limit is possible. The parasistic capacitance of this large transistor is compensated by the load capacitor (C_d).

6.1.3 Noise of Output Transistor

There are two types of noise in MOS transistors – white noise and flicker noise. The noise at the capacitor during charging or discharging is caused by the input current. Thermal noise power spectral density for a MOS transistor in weak inversion is given in (8),

$$I_{DN}^2 = 2qI_D \tag{8}$$

where

q is the electron charge

I_D is the drain current

Integrating this current to obtain voltage noise on the capacitor gives (9),

$$U_N^2 = \frac{I_{DN}}{2\pi f C} \tag{9}$$

where

C is the load capacitor, C_d or C_c

f is the frequency of charging or discharging of the capacitor

Therefore, if the noise is thermal noise, there should be voltage noise present at $1/f^2$, or -20 dB/dec. At lower operating frequencies, flicker noise should become more noticeable. By setting thermal noise and flicker noise to be equal, the combination of the two noise sources can be minimized. For this process, flicker noise and thermal noise are equal when

$$\frac{f_c}{I} = 10^{11} A^{-1} s^{-1} \tag{10}$$

where

f_c is the corner frequency

For 1pA then, f_c = 0.1 Hz. Since the operating frequency of the design is 0.4 Hz, the frequency at which the thermal and flicker noise are equal is below this value and the noise of the output transistor is always low.

6.1.4 Noise at OTA

The noise of the OTA is lowered by properly sizing the transistors in the design. The input-referred thermal noise power is given by (11):

$$v_{ni;thermal}^2 = \frac{8kt\gamma}{g_{m1}}\left[1+\frac{2g_{m3}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right] \tag{11}$$

To minimize the thermal noise of devices M3-M8, sizing of the transistors is such that $g_{m3}, g_{m7} << g_{m1}$. The devices are then pushed into strong inversion where their transconductance decreases with $1/\sqrt{I_D}$.

6.1.5 Comparator

The comparator used in this circuit is a high-speed cmos comparator with 8-bit resolution [18] (see Figure 8). It is composed of a differential input stage, two flip flops and an S-R latch. The sampling rate of this comparator is up to 65 MHz. Moreover, power consumption is only 0.85 mW at 65 MHz clock rate with 32.5 MHz input signal. Resolution of the circuit is +/- 4.9 mV. It was fabricated in a double-poly, double-metal 1.5 μm n-well process with a very small die area ($140\mu m^2 \times 100\mu m^2$). The clocks, φ1 and φ2 are non-overlapping (see Figure 9). There are two time intervals required for the operation of this circuit, the reset interval and the regeneration interval. During the reset-time interval, while φ2 is high and φ1 is low, current is flowing through M12 which forces nodes *a* and *b* to be initially equal. When the input stage settles on an input difference, the voltage is reflected on nodes *a* and *b*. While φ1 is low, the n-channel flip flop is isolated from the p-channel flip flop by transistors M8 and M9. The pre-charge

transistors, M10, M6, M7, and M11 pull nodes *c* and *d* to the positive supply voltage. At this time the latch is in the astable, high-gain mode.

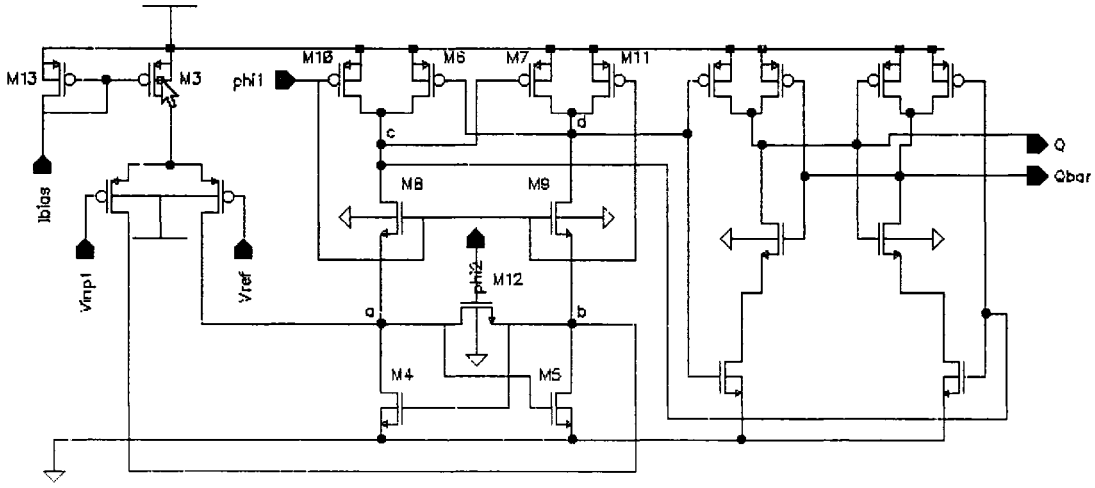

Figure 8—Schematic of Comparator

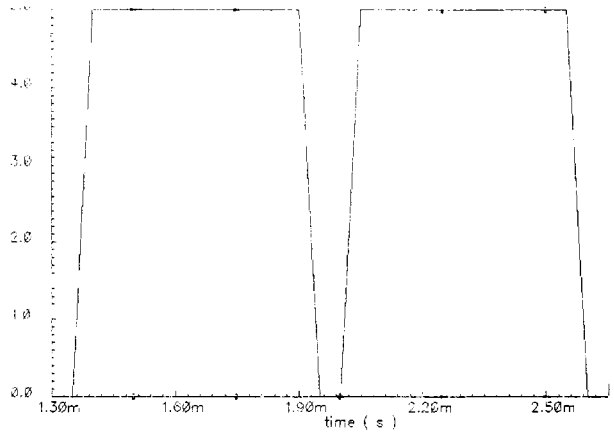

Figure 9—Reset and regeneration time intervals of φ1 and φ2

During the first step of the regeneration time interval, both clocks are low. Since φ2 is off, nodes *a* and *b* are floating. During the second regeneration step, when φ1 goes high and φ2 is low, transistors M8 and M9 are off. The two flip flops, the n-channel and the

p-channel, regenerate the two voltage differences—that between nodes *a* and *b* and between *c* and *d*. The voltage between nodes *c* and *d* is soon amplified nearly to the level of the power supply voltage. The S-R latch is then driven to its full complimentary digital output levels at the end of the regeneration period.

The input voltage difference is critical for the final voltage decision. Incorrect resetting will call hysteresis. Through optimization of the time constants for the resetting process and for the regeneration step, the transistor widths were chosen as follows: With W_4 chosen to be 12μm, $W_{12} = 1/3\ W_4$, $W_1 = 2\ W_4$, $W_8 = W_{12}$, $W_{10} = 2.5\ W_{12}$, and $W_6 = 2.5\ W_1$. For the implementation in the circuit used in the research herein, based on the smaller minimum size transistor available in AMI 0.6nm technology, W_4 was chosen to be 8λ, or 4.8μm.

The optimal bias voltage for the comparator was found to be 20 μA. The current can be raised to increase the comparison speed, but a larger offset voltage will result. Input capacitance for the comparator was found to be 30 fF.

6.1.6 Propagation Delay of Comparator

The propagation delay of the comparator is given by the comparator offset as shown in (12),

$$\pm t_{off} = t_{final} - t_{ideal} = \frac{CV_{off}}{I_{inp}} \tag{12}$$

where

$V_{off} = V_{final} - V_{ref}$

Since a high-speed comparator was used in the design, with a maximum offset voltage of 5mV, the total delay is less than 0.2% of total time.

6.1.7 Resolution

The smallest detectable change in current was found to be 100fF, as shown in (13),

$$\delta t = C\left(V(t) - V_0\right)\left(\frac{\delta i}{i(i+\delta i)}\right) \tag{13}$$

where

$V(t)$ is the voltage at time t

V_0 is the initial voltage of the capacitor

δt is the change in charging/discharging time of the capacitor

δi is the minimum change in current that can be resolved

The advantages of the VLSI potentiostat include its small size, portability, accuracy and ability to measure very small levels of ionic current. If, however, more information is needed regarding the impedance (small-signal as well as dc) of the DUT, an ac signal is necessary. With the aforementioned circuit it is possible to find the real part of the impedance, that is, the current flowing through the resistive part of the equivalent circuit. Finding the imaginary part or the reactive elements of the equivalent circuit is, however, unrealizable.

7. Novel Circuit Design

In this thesis work, therefore, a circuit was developed (see Figure 10) which extended the function of the VLSI potentiostat to include an ac component which could, in conjunction with the time-resolved measurement of dc current, also measure the frequency response of the DUT and thus the imaginary (capacitive) part of the impedance.

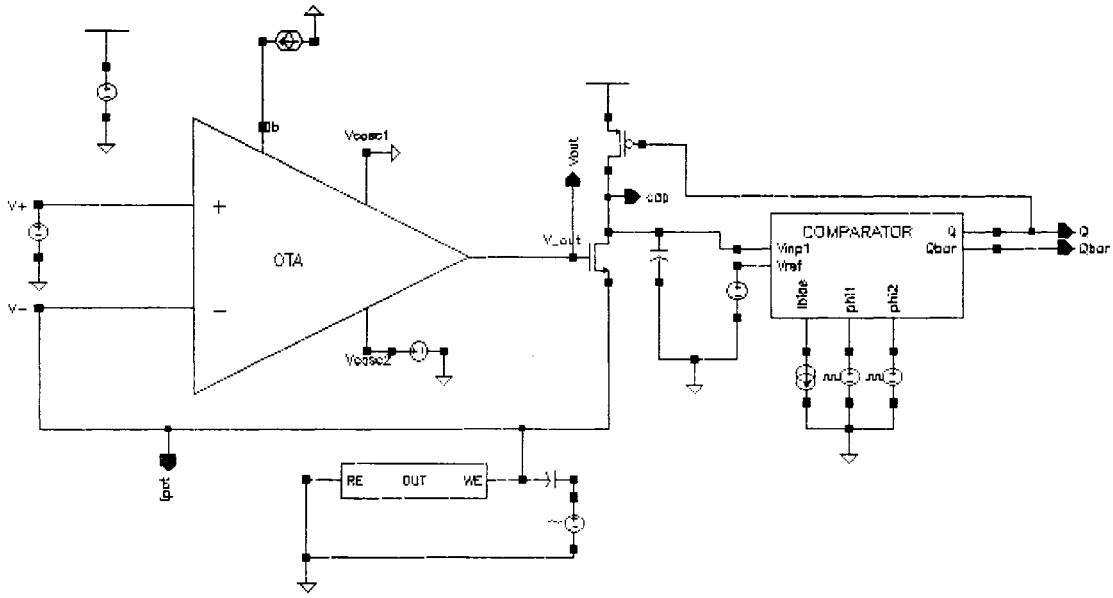

Figure 10—Novel circuit implementation

The time-resolved measurement of current through the DUT is a slow process requiring 30ms for a 1pA current. The injection of an ac signal across a large (10nF) capacitor causes the high-frequency signal to be superimposed on top of the slow discharge of the load capacitor (see Figure 11). Since charging of the capacitor is done

very quickly, the frequency response of the capacitor can only be measured during its period of discharge.

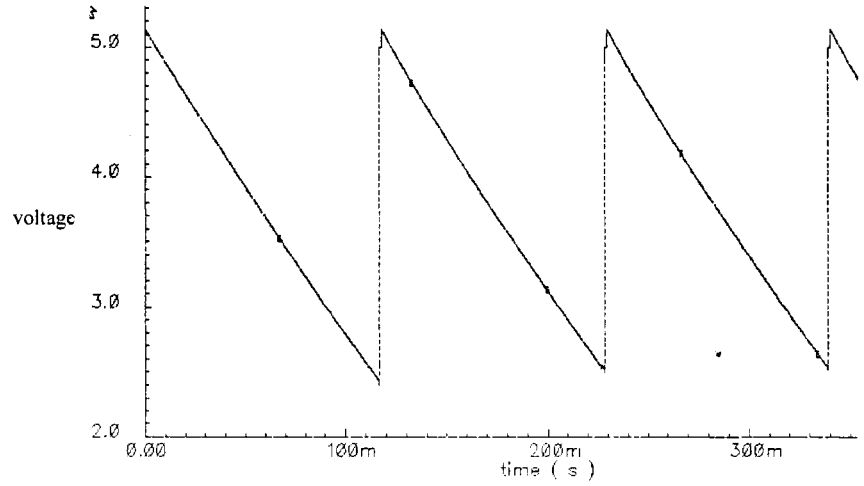

Figure 11—Discharging of capacitor under dc conditions

The equivalent impedance circuit of the ac portion of the potentiostat is composed of the capacitor following the ac input signal (C_{signal}) followed by the equivalent electrode circuit (DUT). The load capacitance and the capacitance of the nmos transistor at the output of the OTA can be neglected because they are so much smaller than C_{signal}. The equivalent impedance seen by the ac source can thus be calculated based on the values of C_{signal} and the impedance of the DUT, and its real and imaginary components are given in (14-16):

$$Z = R_1 + \frac{R_2 - j\omega C R_2^2}{1 + \omega^2 C^2 R_2^2} \tag{14}$$

$$Z' = R_1 + \frac{R_2}{1 + \omega^2 C^2 R_2^2} \tag{15}$$

$$Z'' = -\frac{\omega C R_2^2}{1+\omega^2 C^2 R_2^2} \tag{16}$$

From these equations and the value of R_s measured through the time-resolved dc analysis, C_i can be found using the complex non-linear least squares (CNLS) method.

Figure 12 illustrates the time-resolved functions of the VLSI potentiostat. The capacitor discharges at a rate proportional to the current through the DUT. Pulses are generated at the output of the comparator (Q), synchronizing with the discharge of the capacitor. The time between output pulses as a function of current through the DUT vary markably. It requires a relatively long time for the capacitor to discharge when the current through the DUT is very low (2.5s for 1pA current). This time can be shortened by reducing the value of the load capacitor; but if it is too small, it will be overcome by noise. The accuracy of the measurement is very high.

An ac signal is applied through a large (probably off-chip) capacitor to the working electrode of the DUT. All other circuit parameters remain the same (except the load capacitor for optimization purposes). The initial impedance values of the components in the DUT and equivalent electrode circuit were implemented based on [5]. The process is as follows: An equivalent circuit with initial impedance component values (realistic as having been garnered from the experiments) is inserted into the design. Simulation takes place and optimization is performed on the circuit elements. Then, when the component values of a new DUT are unknown, the circuit has been pre-optimized to find them. The optimization DUT used in this circuit is as in Figure 13, where R_s, R_{ct} and C_i are set to 500Ω, 100GΩ, and 10nF, respectively. The exact initial values are not critical. In fact,

changing the values provides the information necessary to calculate the measurement accuracy of the circuit.

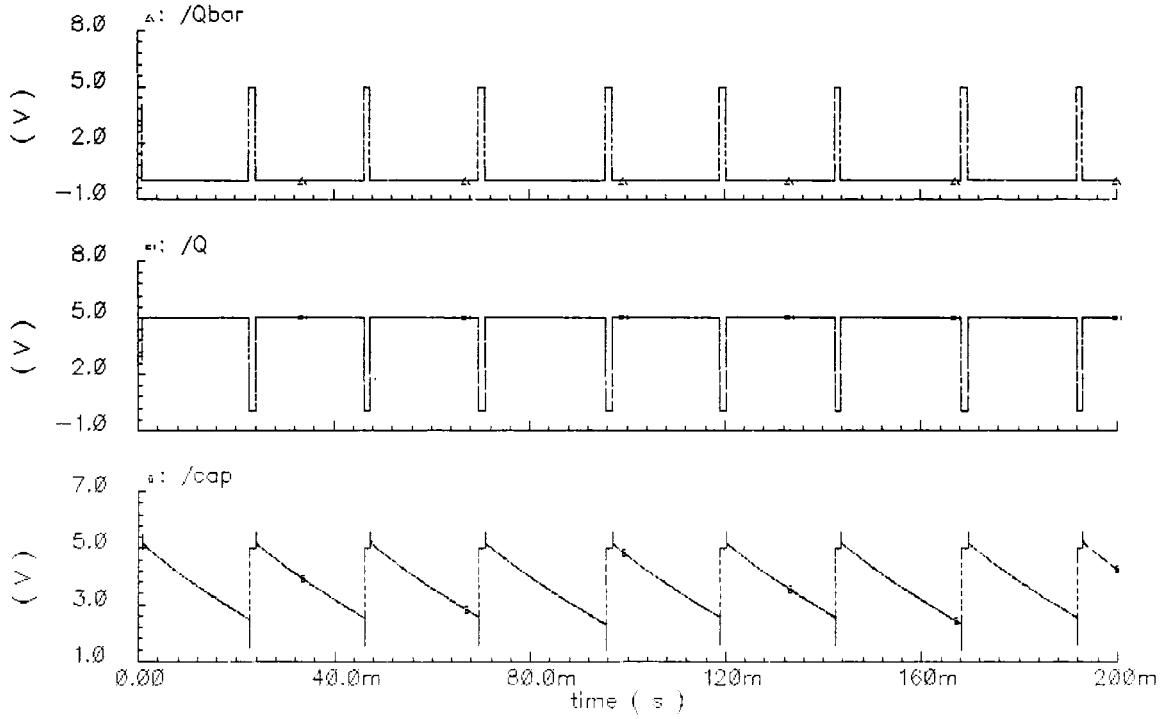

Figure 12—Time-resolved function of potentiostat

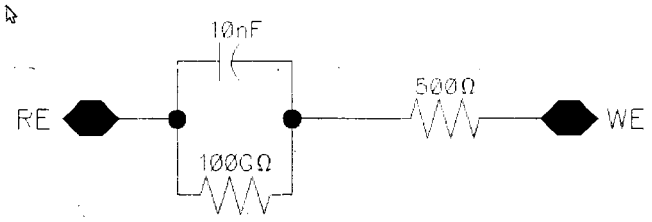

Figure 13—Equivalent electrode circuit used for initial simulation of DUT[8]

The equivalent impedance circuit is shown with its real and imaginary components as follows. Note the presence of the capacitor (C_{signal}) following the ac signal. This capacitor must be made much larger (10x in this case) than the expected value of the

measured capacitance, C_i, which for simulation purposes was set at 10nF. Therefore C_{signal} was set at 100nF. The resistance (r_{ds}) of the nmos transistor and the load capacitor (much smaller than the capacitance to be measured, C_i) can also be neglected.
The simultaneous operation of the dc and ac functions of this circuit is shown in Figure 14 (in this case v_{ac} = 1V and swept from 1kHz to 1 MHz with dc offset of 1.5V). The delay between the pulses at the output of the comparator may still be used to calculate very low levels of current through the electrode circuit. The amount of error in the measurement, however, has increased to ~10%. This is a result of the application of the ac signal. Since the discharging of the capacitor triggers a pulse at the comparator whenever it drops to V_{ref}, 2.5V, any perturbation at this time can cause the trigger to come earlier or later.

Decreasing the amplitude of the ac signal serves to decrease the error in the measurement times. The amplitude of v_{ac} may thus be decreased, though may not be set too low because of noise interference.

Also, one can see that the capacitance voltage oscillates temporarily before settling to its final discharge rate. This is also due to the injection of the ac signal because of the slow speed of the OTA and because the negative terminal takes longer to reach the value of the positive terminal when the ac signal is applied. To avoid these sources of error, dc and ac measurements may be completed separately if desired. In biological systems, however, there are distinct advantages to being able to take such measurements simultaneously.

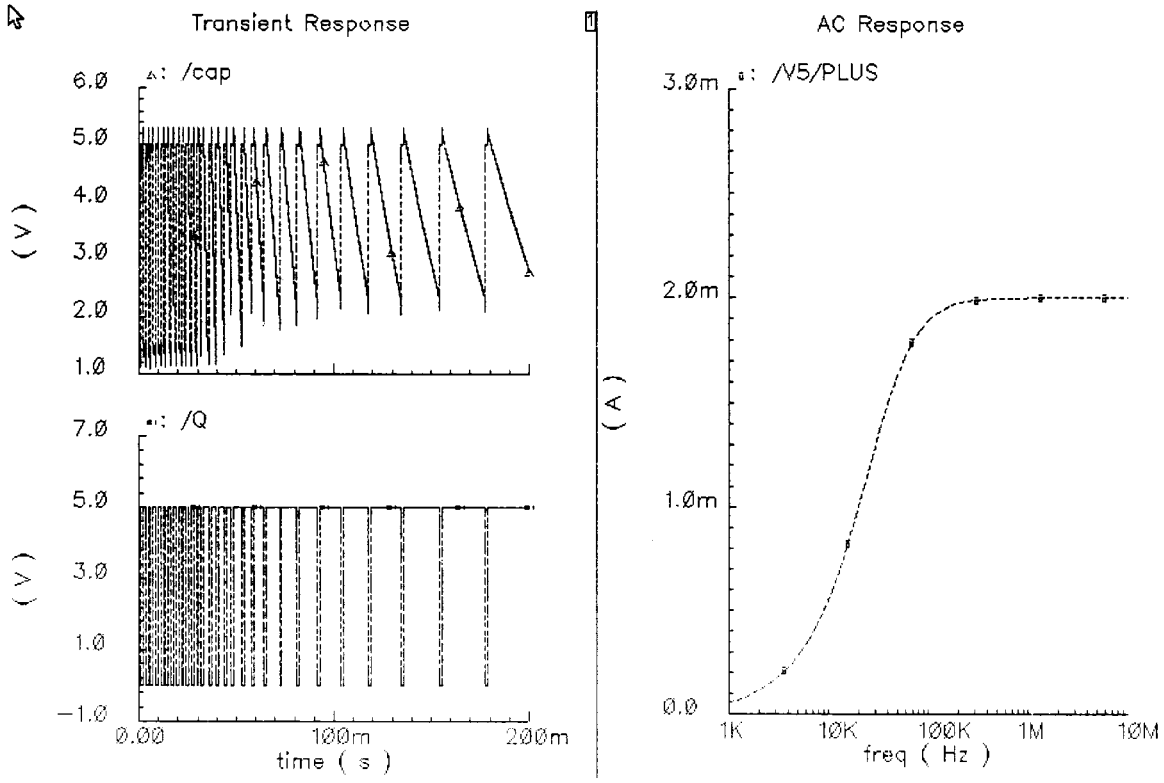

Figure 14—Simultaneous operation of dc and ac measurement

Using this tandem dc and ac measurement system, the complete impedance circuit may be found. At dc, C_i acts as an open circuit; so the components contributing to impedance include only R_s and R_{ct}. At ac, since C_i passes some current, R_{ct} may be neglected. The imaginary component of the impedance can thus be calculated.

NOTE—*The suggested electrode architecture may be altered in such a way that the current flows through the counter electrode to the working electrode. In [18], authors claim that current flow through the reference electrode is unwanted because of its high resistance as well as its tendency to make the reference electrode potential unreliable.*

7.1 Computation of Impedance Parameters

The real part of the impedance was computed by dividing the voltage at the ac voltage source by the current through the voltage source and taking the opposite sign since the current is flowing in the opposite direction. The imaginary part was computed by the same method, only taking the complex part of the impedance.

When looking at high frequencies (say above about 350kHz), one can see that the imaginary part of the impedance is low (50Ω), which is less than a tenth of the real part of the impedance. At this point, the real part of the impedance is relatively constant at 500Ω. Therefore, at this frequency, the impedance can be considered as simply a pure resistance. To compute this resistance, one can take the potential of the voltage source (in this case 1V) and divide it by the series resistor, R_S, since the external capacitor, C_{signal}, and the electrode capacitance are, in effect, shorted at this frequency. The ac amplitude, 1V, divided by R_S, 500Ω, gives 2mA, or the current flowing through the DUT, which is verified by simulation, as shown in Figure 15. As shown, the current through the voltage source arrives asymptotically at its final value, which is limited by the ratio of the ac voltage at the voltage source and the series resistance of the DUT. One may also note that, as the frequency of the input signal is increased, the current through the DUT is also increased. This suggests a practical frequency limit at a certain ac voltage input for biological systems, such that damage to the system under investigation is not incurred. For example, the power dispersion in this example would be $P = CV^2f$, so that the power increases linearly with frequency and with the square of the voltage. If the system under investigation is especially sensitive, the ac voltage amplitude would have to be held low.

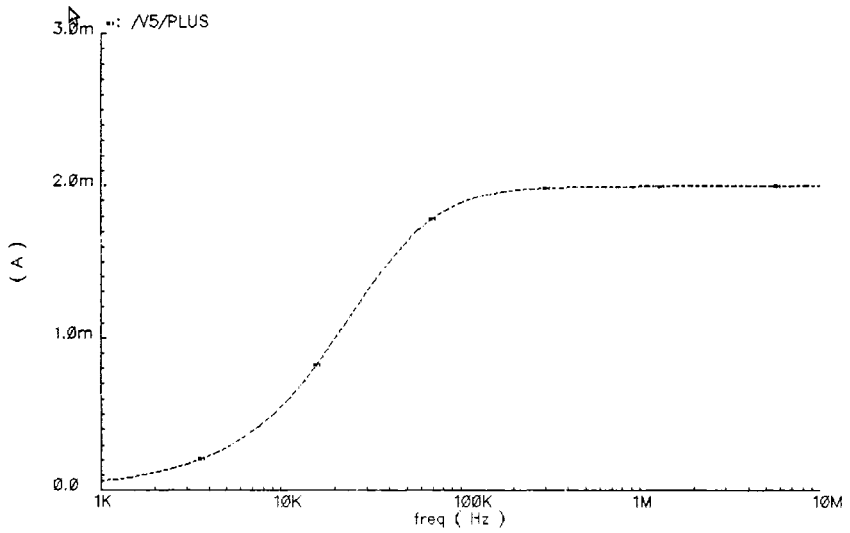

Figure 15—Current through DUT during ac excitation

Looking at the voltage across the load capacitor leads to questions about the equivalent impedance of the nmos transistor, the pmos transistor, and the load capacitor. Looking at the voltage across the capacitor (see Figure 16), one can see that it is approximately equal to the ratio of the sizes of the pmos and nmos transistors, though other factors may be at play as well. The capacitance of the nmos transistor is very small, and even smaller when in parallel with the load capacitor (50Ω). The resistance of the nmos is also extremely large, $r_{ds} = (r_d - r_s)/I_{dut}$. In this simulation, since $r_d = 2.5V$, $r_s = 1.5V$, and $I_{dut} = 15pA$, $r_{ds} = 66.7G\Omega$. One may also notice the ~ 10% drop in I_{dut} at low frequency, due to the voltage divider effect of the two capacitances, C_{signal} and C_{dut}. Making C_{signal} larger would reduce this effect of voltage division.

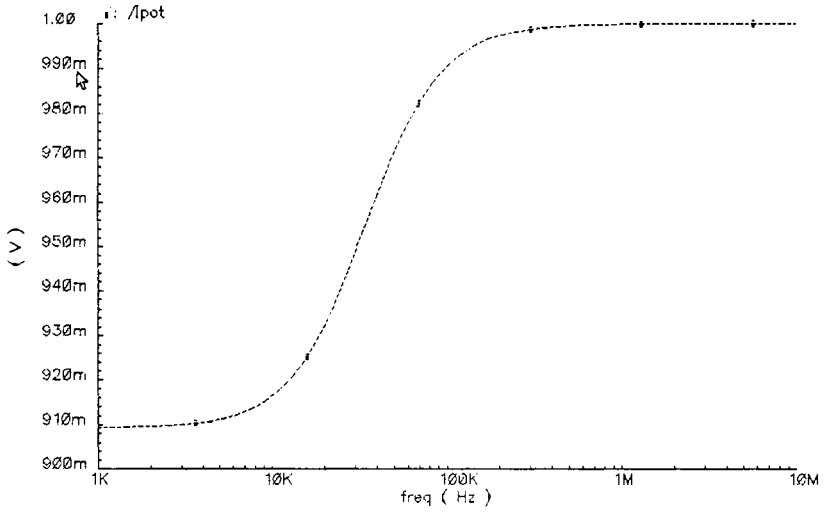

Figure 16—Potential at working electrode of DUT

At lower frequencies, the reactive components are seen to be dominant (see Figure 17), such that the imaginary part of the impedance is much greater than the real part (e.g., the reactive impedance is 5.34kΩ at 3.3kHz, more than ten times greater than the real part).

NOTE---*Both capacitors, the external and that contained in the DUT, must be taken into consideration. In order to be able to neglect the external capacitance, it would have to be made much larger than the capacitor contained in the DUT. Too large of an external capacitance, however, can slow the system speed markably.*

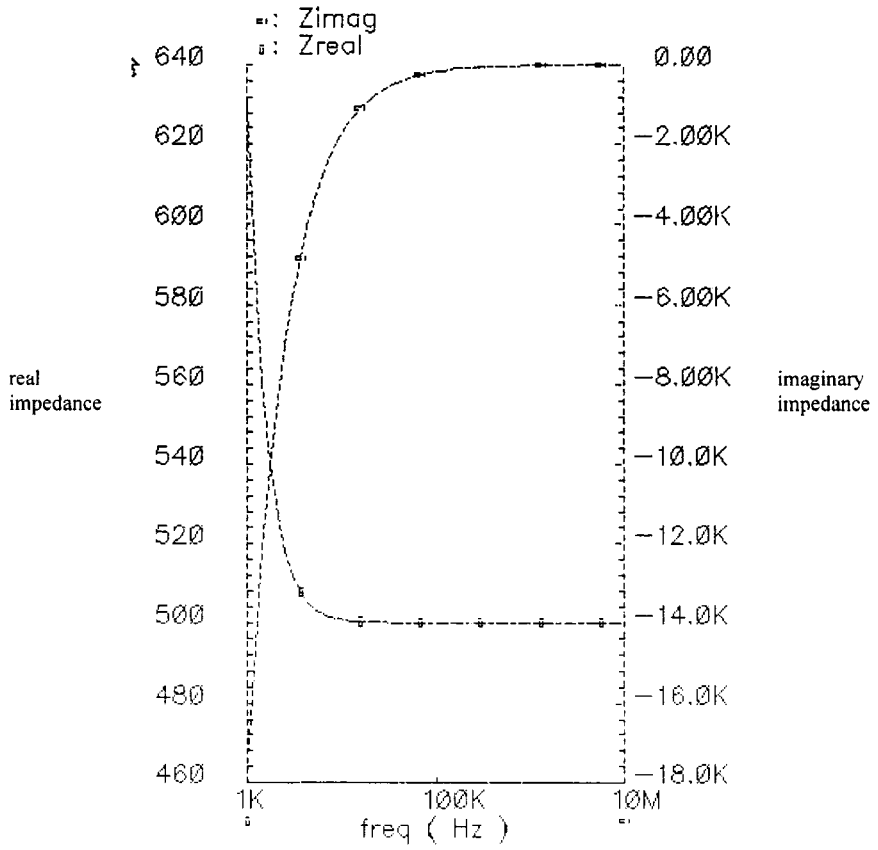

Figure 17—Real and imaginary parts of the impedance

7.1.1 Example Calculation of Impedance Parameters

An example of the calculation of the reactive part of the impedance and thus the capacitance of the DUT is as follows: $1/j\omega C$ is the impedance, which equals $-j/\omega C$. Taking the imaginary part of this, you get $-1/\omega C$. In Figure 17, one can see that at 1kHz frequency, the imaginary part of the impedance is equal to -17.5kΩ. Therefore the total value of reactive impedance seen by the voltage source is $-1/(2\pi fC) = Z$, where f = 1kHz and Z = -17.5kΩ. The equivalent capacitance is thus 9.09nF. The series combination of the two capacitors is shown in (14):

$$\frac{1}{C_{total}} = \frac{1}{C_{signal}} + \frac{1}{C_{dut}} \tag{14}$$

Since C_{total} was computed as 9.09nF and C_{signal} is known (100nF), C_{dut} can be found as 9.9989nF ~ 10nF, which is the initial value set to C_i to simulate the impedance measurement. Therefore, it has been shown that this measurement technique can find the reactive component of impedance at this frequency. Further frequency sweep measurements must, however, be done to examine the reliability and validity of this technique over a larger frequency range. To increase accuracy of the measurement, samples would need to be taken along the impedance curve and the complex nonlinear least squares (CNLS) method performed.

From the diagrams of the magnitude and phase of the impedance (see Figure 18), one can see the identical response. At low frequency, the magnitude of the impedance rises to 18kΩ with a phase of -90°, which means that the impedance is wholly reactive. At higher frequencies, the magnitude of the impedance falls to 500Ω, and the phase rises to 0°, which means that only the resistive component of the impedance is seen.

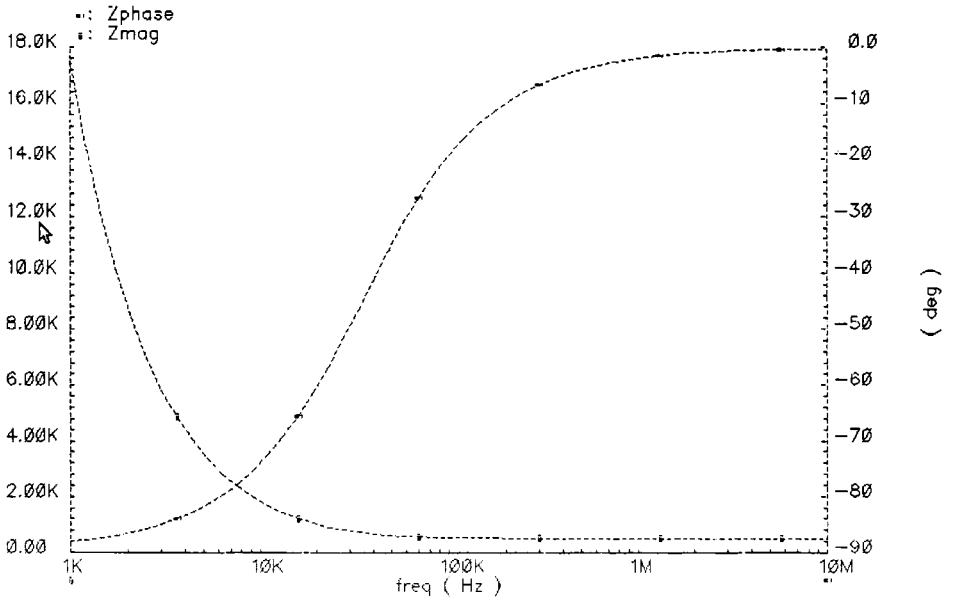

Figure 18—Magnitude and phase of impedance

One can see then that a simultaneous dc and ac measurement is possible which can be especially important for biological systems. However, a few problems exist with this measurement setup. Firstly because of the injected ac signal, the amplifier takes longer to settle to its final value. Because of the ac perturbation on the inverting node of the OTA, the output of the OTA is temporarily oscillating and causes the capacitor to discharge and be reset repeatedly during this settling process. This behavior is shown in Figure 19. A second problem is that the ac signal may change arbitrarily the discharge rate of the capacitor and thus the rate of pulses at the output of the comparator, up to a maximum of 10% error. Reducing the voltage swing on the ac signal reduces this error in discharge time variability, but must be maintained at a minimum voltage to be distinguishable from noise.

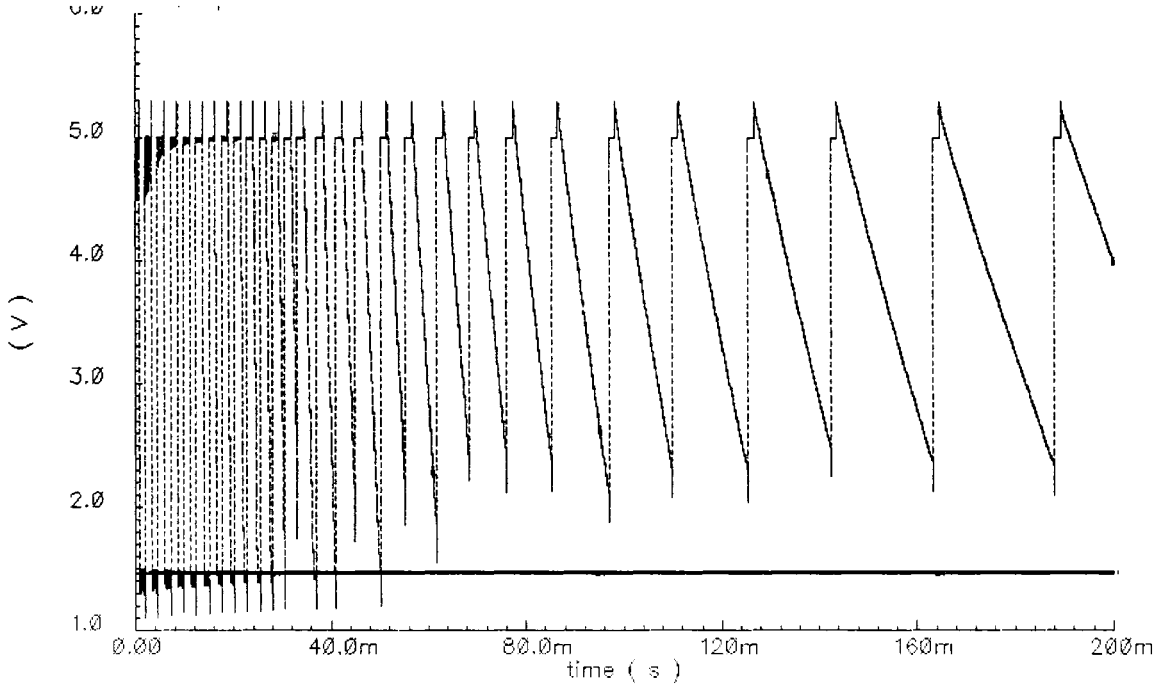

Figure 19—Oscillation of capacitor during OTA settling time

8. Further Research

In terms of an initial investigation, this research has shown promise that a novel circuit design, tailored to the requirements of biological measurements, can be integrated with current analysis techniques. The potential uses of this system, however, have not yet been realized.

Firstly, further investigation of the frequency spectrum needs to be accomplished with testing at various ac magnitudes. In addition, application of a collection of sine waves (as in ac voltammetry) or a noise signal at the ac input with subsequent Fourier devolution at the output could lead to the recognition of further implementation possibilities for this circuit.

An automated test and measurement technique could also help to decrease the variability of measurement as well as collect data digitally for averaging and error analysis. Just such a system (the original idea of which came from [13]) has been conceived as in Figure 20 and will be implemented in the future course of this research. In particular, this LabVIEW™-controlled system will collect the dc potential offset, the (optional) dc sweep and the superimposed single frequency, collection of sine waves at various frequencies, or noise signal. It will apply the dc signal and potential sweep to the non-inverting node of the current conveyor and the ac portion to the inverting node. After completion of measurement, it will collect the ac data from the load capacitor and then digitize it, using a computer-installed ADC card. Delay between pulses at the output (Q) will be averaged and the dc current of the DUT and thus the total dc resistance of the DUT can be extracted. Using the measurement of the digitized voltage data at the load

capacitor, the real and imaginary parts of the impedance can be found. Then, using the complex non-linear least squares (CNLS) method, the values of the respective resistors and capacitor can be calculated.

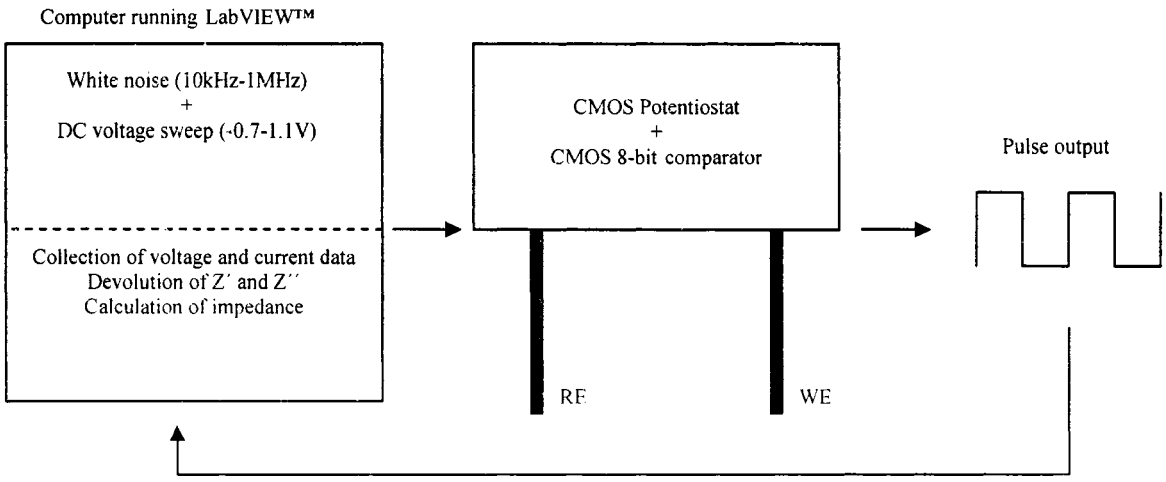

Figure 20—LabVIEW™ measurement setup

Furthermore, this method could be used to derive various candidates for the best architecture of the equivalent electrode circuit. In this vein, and especially if measurements are to be made at lower frequencies, the Warburg impedance could be re-added to the equivalent circuit to see if its addition provides a better equivalent circuit fit. Such a measurement system using LabVIEW™ (though with a different measurement circuit, of course) was implemented in [19]. The authors claim that their measurement setup is much more flexible than traditional systems. Their "electrochemical detection system" is capable of generating a modulation signal, obtaining the dc potential of the working electrode as well as the ionic current between the electrodes and displaying the

output in terms of a voltammogram. In addition, the authors were able to demonstrate their system using electrochemical biosensors.

With the use of micron-sized electrodes, currents are in the pico- to nano-ampere range, and thus two electrodes are often used (that is, the counter and the reference are tied together).

An interesting aspect of this process is that it can be set to perform any of the usual electrochemical measurements as well as a new measurement type defined by the user. Data can be collected and analyzed to track differences in measurement, differences in the impedance of various biosensors (that is, biosensor characterization) as well as the aforementioned derivation of the equivalent electrode circuit.

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