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Investigation of deposition and annealing temperatures on stiction in MEMS

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INVESTIGATION OF DEPOSITION AND ANNEALING TEMPERATURES ON
STICTION IN MEMS

A Thesis

Presented to

The Faculty of the Department of Chemical and Materials Engineering

San Jose State University

In Partial Fulfillment

Of the Requirements for the Degree of

Master of Science

By

Gilbert K. Hermosillo

August 2004

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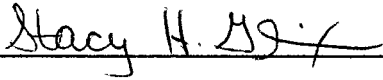
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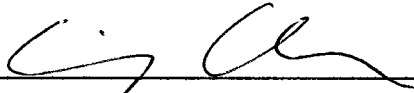
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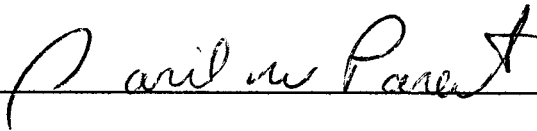
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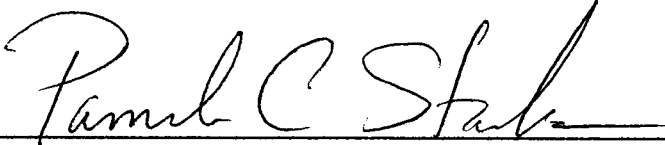
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ABSTRACT

INVESTIGATION OF DEPOSITION AND ANNEALING TEMPERATURES ON STICTION IN MEMS

By Gilbert K. Hermosillo

The purpose of this research was to investigate the effect that polysilicon thin film properties had on stiction of microelectromechanical systems (MEMS). The different polysilicon thin film properties were achieved by varying the deposition and annealing temperatures. The deposition temperatures used were 585°C, 600°C, and 620°C and the annealing temperatures used were 550°C and 1000°C. Micromachined cantilever beams were used to assess stiction. The overall stiction observed was minimal compared to the number of beams examined, but the difference in stiction between the individual wafers was significant. The polysilicon properties that were of interest were roughness, film stress, grain size, and crystallographic texture. These film properties along with the variations in polysilicon film thickness contributed to the observed stiction variation by altering the polysilicon surface energy and the mechanical stiffness of the beams.

ACKNOWLEDGEMENTS AND DEDICATION

I dedicate this thesis to my wife Guillermina and my daughter Rebecca. They supported me through all of the long hours work at home, at school, and in the lab. I also dedicate this thesis to my father, Gilbert, my mother, Shirley, and my grandmother Amalia who helped me to keep up with maintaining my home while I worked on this research.

I owe a special debt of gratitude to my thesis advisor, Dr. Stacy Gleixner, for allowing me to work with her on this research and for arranging for me to work in the Stanford Nanofabrication Facility. It was a valuable learning experience for me that helped me to tie all of the concepts that I learned during my graduate studies in the Material Science department at San Jose State University together.

I want to thank my reading committee, Dr. Emily Allen and Dr. David Parent, for taking the time to read my thesis and provide insightful comments that helped to make the thesis better.

I want to thank Dan Vroom for working with me in the lab. We spent long hours there processing our test specimens. Working with Dan was a learning experience since I had never worked in a clean room environment and Dan had a lot of industry experience. I also want to thank Walt Prater whom I have enjoyed collaborating with on a number of projects at San Jose State University.

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CHAPTER 1

INTRODUCTION

1.1 Background

Microelectromechanical Systems (MEMS) combine mechanical elements with signal processing elements. Although there are no rigidly defined scale requirements for MEMS devices, they are generally on the order of 1 μm to 1mm[1]. The signal processing side of MEMS devices consists of integrated circuits (ICs) that either drive the mechanical elements or process the interactions between the mechanical elements and the environment in which the MEMS device operates. The types of mechanical elements used in MEMS devices (gears, diaphragms, beams, etc.) are basically the same as those used in macro scale machinery. These mechanical elements can be combined to produce MEMS devices such as micromotors, actuators, and microvalves.

1.2 Manufacturing Technology

Since the development of solid-state electronic devices, the semiconductor industry has been focused on increasing both the functionality and speed of IC devices while reducing manufacturing costs. These objectives have been achieved through improvements in IC manufacturing technologies, which have allowed the size of the IC components to be reduced.

The manufacturing technologies used for the IC industry made the production of MEMS devices possible. The basic IC manufacturing processes of thin film deposition,

lithography, and etching are being used to produce MEMS devices. The advantages of using the IC manufacturing technologies are that the processes are well understood, the equipment already exists to perform many of the process steps, and batches of MEMS devices can be produced on wafers at relatively low costs. However, there are several differences between IC fabrication technology and MEMS fabrication technologies. The fabrication techniques used for ICs produce primarily non-structural, 2-dimensional circuits. The requirements for the thickness of the films used to build IC components are based on electrical requirements. Also, the IC fabrication technologies are applied primarily to semiconductor materials and interconnect metals. MEMS fabrication technologies are required to produce structural and mechanical elements that must withstand static and dynamic stress environments. The 3-dimensional structural components often require intricate mask patterns and thick films to create mechanical systems with movable components. This is illustrated in the MEMS micromirror shown in Figure 1[2]. The fabrication techniques currently used in MEMS are referred to as micromachining or microfabrication[1]. Another difference between MEMS fabrication technologies and IC fabrication technologies is that MEMS device components are often made from materials that are not normally used in IC designs.

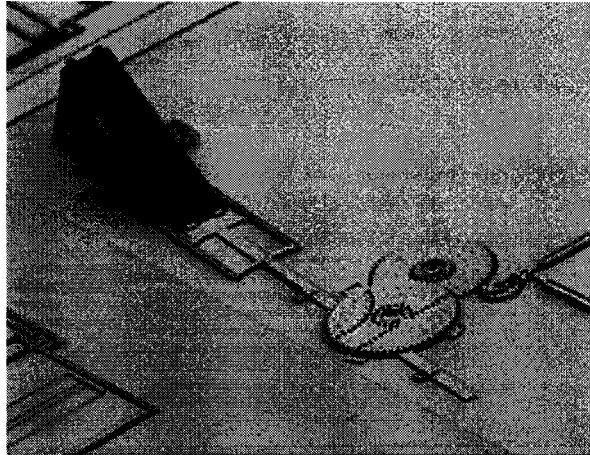


Figure 1. The microengine pinion gear powers a torque converter that moves a mirror by pushing a linear rack. [2]

1.3 Materials Used in MEMS

Since the fabrication techniques used in MEMS are closely related to IC fabrication techniques, common semiconductor materials such as silicon and gallium arsenide are commonly used in MEMS devices. The behavior of these materials during manufacturing is well understood and the existing manufacturing tools can be used to produce silicon or gallium arsenide MEMS devices[1]. Silicon and gallium arsenide are used extensively in actuating and sensing devices where the MEMS substrate is required to be active. Other materials such as polymers, quartz and metals are also used in MEMS devices[1].

Silicon is the most widely used material for manufacturing MEMS devices. This is due not only to the wealth of knowledge and experience available for processing silicon developed in the IC manufacturing industry, but also the structural and electrical

properties of silicon[1]. Silicon has physical properties that are similar to other common structural materials used in mechanical devices. The Young's Modulus for silicon is roughly the same as that for steel at 2×10^5 MPa, but silicon has a lower density[1]. This makes it possible to produce mechanical components that are both stiff and light. The melting point of silicon is higher than that of aluminum[1]. The high melting point makes it possible for the silicon to withstand the high temperatures often used in MEMS manufacturing processes. The coefficient of thermal expansion is 8 times smaller than steel and 10 times smaller than aluminum[1] so it is dimensionally stable over a wider range of temperatures. Since silicon is a semiconductor material, both the electronic and mechanical portions of MEMS can be fabricated on the same chip using the same manufacturing processes.

1.4 MEMS Applications

In the late 1980's, MEMS devices were mainly produced in laboratory settings for experimentation purposes. They were not commercially viable due to low power and short operational lifetimes, which limited their practical use[1]. Advancements through research made commercially viable devices possible.

There are several industries currently making use of MEMS devices. The automotive industry is already using MEMS inertia sensors for controlling the deployment of airbags[1]. MEMS devices are also being used in ink jet print heads to control the flow and placement of ink[2]. MEMS devices are being used in the fiber optics industry as optical switches[1]. MEMS have been applied to digital micromirror

displays (DMD) where the display consists of thousands of chips that control micromirrors[3].

1.5 MEMS Industry Growth

The MEMS market has continued to grow since the early 1990's. The MEMS Industry Group (MIG), which was founded in 2001 for MEMS manufacturers in the United States, estimated that there are currently 1.6 MEMS devices for each person in the United States. This number was expected to reach 8 MEMS devices per person by 2004[4]. MIG valued the MEMS industry at between 2 – 5 billion dollars in 2000 and forecasted growth to 8 – 15 billion dollars by 2004[4]. The MIG estimates were based on the chip device value. NEXUS, the European equivalent of MIG, valued the industry at 14 billion dollars in 1996 and forecasted growth to 38 billion dollars by 2002[4]. The European estimates were based on the total market value of the devices containing the MEMS components. The number of companies manufacturing MEMS devices has increased dramatically recently with 70% being founded since 1995[4]. The steady growth of the silicon-based microsensor market from 1989 to 1999 is shown in Figure 2[1]. Microsensors are only one family of MEMS devices. The industry will continue to grow as advancements are made in MEMS design and fabrication to improve the reliability and performance of MEMS devices. The biomedical industry is projected to be an area where MEMS sensors will have a significant number of applications[1].

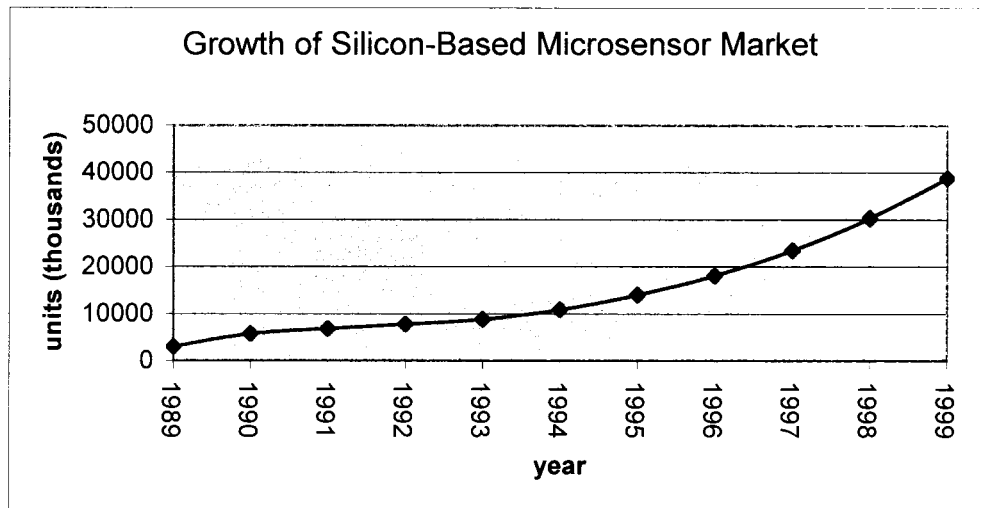


Figure 2. Worldwide Silicon-Based Microsensor Market. [1]

1.6 Technical Challenges

There are several technical challenges associated with silicon MEMS devices that need to be overcome to increase the usefulness of MEMS technology. Two of the most prevalent failure modes that occur in silicon MEMS are[2]:

1. Friction between sliding surfaces
2. Adhesion of contacting surfaces or stiction

Both of these failure modes are associated with the surface properties of the silicon[2].

The problem of friction between sliding surfaces is caused by operational parameters.

Friction problems can be mitigated through careful design of the mechanical system to

preclude excessive forces between the mechanical elements[2]. There are other solutions

to this problem that involve the application of protective and/or lubricating films. These

films are designed to reduce the frictional forces between the sliding surfaces and protect the surfaces from wear[2].

Stiction is a problem that can occur due to a variety of reasons including manufacturing processing, external environments, and operational environments. Stiction refers to the phenomena where MEMS mechanical elements come in contact with other surfaces within the device and become stuck. This can occur during fabrication, operation, or storage. Stiction is a major problem in the MEMS industry since MEMS devices are built to very tight tolerances and some applications require mechanical elements to touch as shown in Figure 1, where the gears of the micromirror are in contact with each other.

1.7 Thesis Objective

There have been several studies performed to attempt to understand and alleviate the stiction problem. The proposed solutions have revolved around manufacturing process modifications, the addition of surface coatings and mechanical design changes to provide enough force to release stuck elements. There have not been many studies that have been focused on understanding the impact that the silicon film properties (grain size, texture, etc.) have on stiction. The objective of this research was to investigate the impact that silicon deposition and annealing parameters had on the post release stiction of micromachined cantilever beams.

CHAPTER 2

LITERATURE REVIEW

2.1 Stiction Mechanisms in MEMS Devices

Komvopoulos and Yan[5] published a paper that analyzed the relationship between surface roughness and stiction. The analysis involved simulation tools that were used to model both the thin film surface geometries and the effect that the surface roughness had on stiction and the force required to pull a stuck component free. The surface roughness was modeled using fractal geometry, which has been used to study irregular surfaces. The basic equation used was:

$$z(x) = L_x \left(\frac{G}{L_x} \right)^{(D-1)} \sum_{n=0}^M \frac{\cos\left(\frac{2\pi\gamma^n x}{L_x} \right)}{\gamma^{(2-D)n}} \quad \text{Equation 1}$$

$z(x)$ – Surface height

L_x – Fractal sample length

G – Fractal roughness parameter

D – Fractal dimension of a surface profile

γ – Scaling Parameter

There were no actual experiments conducted, but the data was compared to previous experiments. The simulation considered four primary stiction mechanisms, which were:

- 1) Van der Waals Forces
- 2) Electrostatic Forces
- 3) Capillary Forces
- 4) Elastic Deformation Forces

Van der Waals, Electrostatic, and Capillary forces were all described as contributors to stiction, while the elastic deformation forces were considered to oppose stiction. The materials interfaces examined in the study were silicon dioxide/silicon dioxide, diamond like carbon (DLC)/DLC, and silicon dioxide/platinum. Each of these interfaces represented a different surface chemistry with some being hydrophilic and some being hydrophobic. The interface between two silicon surfaces was not included since Komvopoulos and Yan stated that bare silicon reacts readily with the environment and the surfaces are no longer pure silicon.

Van der Waals forces are created by the electron motion from lower to higher energy levels within the silicon atoms on the surface. Both the normal and retarded Van der Waals forces were found to decrease with increases in separation between the two surfaces, as indicated in the results for Van der Waals pressure versus separation distance presented in Figures 3 and 4[5]. The difference between normal and retarded is the separation distance between the surfaces. The equations for normal and retarded Van der

Waals forces are different so the curves are different. Komvopoulos and Yan plotted both curves for the entire range of separations. From the data presented in Figure 4, the affect of surface separation had a greater affect than the material surface chemistry. The data in Figure 5[5] indicated that the Van der Waals forces were affected more by the surface roughness than by the material properties. The absence of a knee on the smooth plot had to do with the smooth films not having asperities to come into close proximity enhancing the Van der Waals forces. The Van der Waals force was the dominant stiction contributing mechanism for rough surfaces in close proximity on the order 5-10nm. Figure 5 also shows the electrostatic, capillary, and deformation forces.

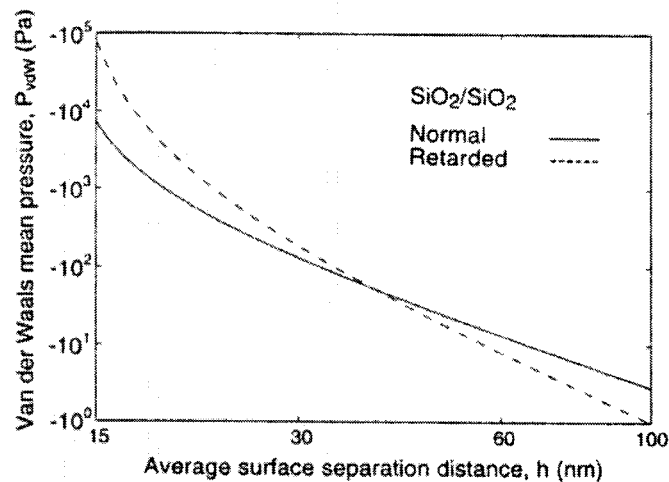


Figure 3. Retarded and normal Van der Waals mean pressure versus average surface separation for rough silica surfaces. [5]

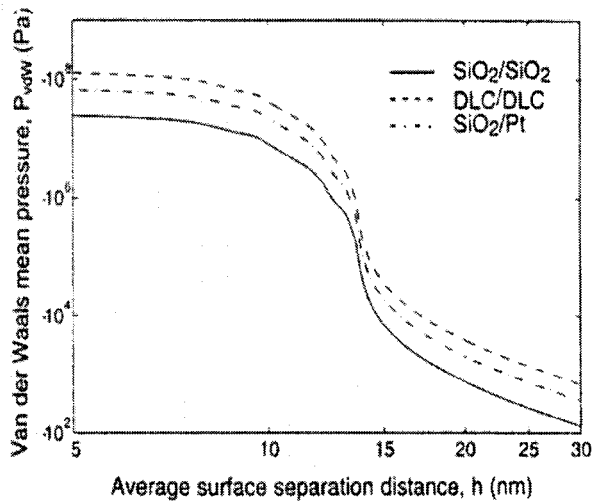


Figure 4. Van der Waals mean pressure versus average surface separation distance for three different material systems. [5]

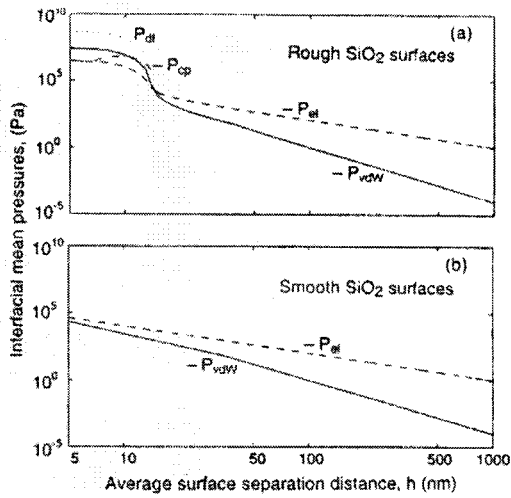


Figure 5. Interfacial mean pressures versus average surface separation distance for silica (a) rough surfaces and (b) smooth surfaces. [5]

The electrostatic forces were due to Coulombic attraction from trapped electrical charges, material work function differences, and external voltages. Komvopoulos and Yan stated that an electrostatic charge buildup could occur during fabrication. The electrostatic forces were considered to be more substantial than the other mechanisms for

smooth surfaces and for rougher surfaces at separation distances greater than 15nm, as shown in Figure 5.

The capillary forces occurred during the fabrication process. A typical MEMS fabrication process often includes a step to remove the sacrificial layer by wet etching and then a water rinse operation to remove the etchant. The water is often trapped underneath the moving structures and this trapped water creates forces that pull the released structure to the substrate. This could also occur in operating devices that are exposed to humid environments. Komvopoulos and Yan stated that the capillary force is primarily due to the Laplace pressure difference. The contribution of the surface tension of the water was not considered to be significant. The capillary force was estimated to be zero when the surfaces were in contact since all of the liquid was squeezed out of the interface. The capillary force was also found to be zero for surface separation distances greater than 15nm. The results for capillary pressure versus separation distance are shown in Figure 6[5]. The capillary force remained for greater separation distances when subjected to 90 percent humidity. The data presented in Figure 6 also shows that the surface condition, hydrophilic vs. hydrophobic, has a significant impact on the capillary forces. DLC has a hydrophobic surface that affects the contact angle of the water on the surface. Komvopoulos and Yan determined that the capillary forces are not present when the surfaces were smooth.

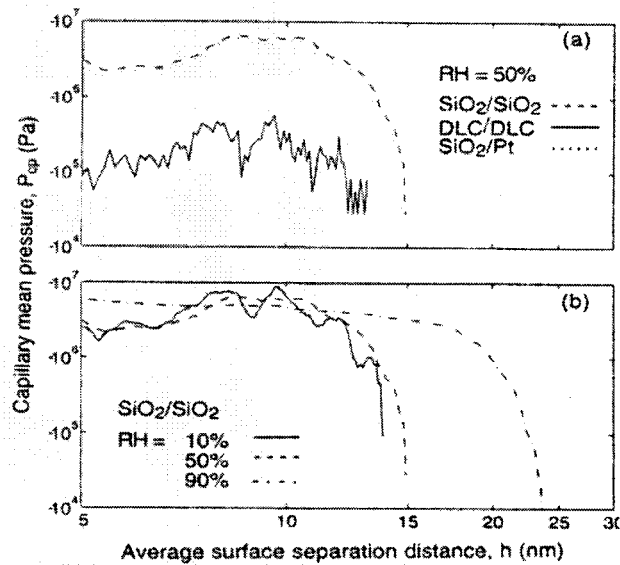


Figure 6. Effects of contact angle (a) and relative humidity (b) on the variation of the capillary mean pressure with average surface separation distance. [5]

The last type of force considered was the elastic deformation force. The elastic deformation forces result from the contact of high points on the opposing surfaces. Under contacting forces, these high spots deform and create repulsive forces. The elastic deformation forces were only significant when the surface separation was close enough for the high points to contact each other as presented in Figure 5. The distance considered close enough by the simulation was approximately 10nm.

Komvopoulos and Yan also studied the effects of surface roughness on the critical pull-off stiffness. The critical pull-off stiffness is the stiffness required for a stuck component to break free. They concluded that the critical pull-off stiffness increased with decreasing surface roughness as was shown in Figure 7[5]. The fractal dimension, D , used to characterize the surface was 1.4 and the surface energy, U , used was 0.5V.

The relative humidity, RH, used was 50 percent. The range of surface roughness values, 0.7 to 7nm, was chosen since the roughness of silicon is usually 1 to 20nm. The data presented in Figure 7 is in agreement with experimental observations.

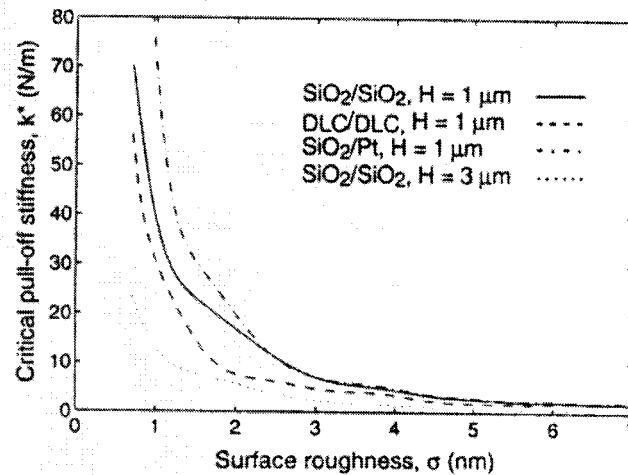


Figure 7. Critical pull-off stiffness versus equivalent surface roughness for different material systems with $D=1.4$ at $U = 0.5$ V, $RH=50$ percent, and $T=20$ C. [5]

In the study performed by Legtenberg *et al.* [6] on post-release stiction, they discussed Van der Waals forces, capillary forces, hydrogen bridging, and electrostatic forces. Hydrogen bridging occurs for hydrophilic surfaces since they have a large number of hydroxyl groups that can form hydrogen bonds between the beam and substrate surfaces. The density of bonding sites was reported to be 5.0 ± 0.5 per nm^2 . The Legtenberg *et al.* study was different from the Komvopoulos and Yan study because they conducted experiments on post release stiction. The experimental approach involved the

use of beams that were clamped at both ends as shown in Figure 8[6]. After the post release etch, the shortest stuck beam lengths were used to calculate the surface energies. The assumption was that all of the beams were pulled down by capillary attraction. The beams that remained stuck after complete drying were held down by one of the other stiction mechanisms. The surface energies were calculated using the following equation:

$$\gamma_s = \left(\frac{\pi^4 E h^3 d^2}{4L_{det}^4} \right) + \left(\frac{\pi \epsilon E h d^2}{4L_{det}^2} \right) \quad \text{Equation 2[6]}$$

γ_s -bond strength
 L_{det} -detached length of beam
 E -plate modulus
 h -beam thickness
 d -zero displacement gap spacing
 ϵ -strain

The calculated surface energies were compared to the bonding energies for the different stiction mechanisms. When the energies were equivalent, the matching stiction mechanism was estimated to be the primary stiction contributor.



Figure 8. Doubly clamped beam.

The beams were made from a two-film stack with plasma enhanced chemical vapor deposition (PECVD) oxide grown at 650mTorr and 300°C, and low pressure chemical vapor deposition (LPCVD) polysilicon deposited at 250mTorr and 590°C. The wafers were annealed at 1100°C in nitrogen for 1 hour to reduce residual stresses. The film thicknesses and beam dimensions were chosen to provide beam stiffness variations. All of the wafers were etched in 50% hydrofluoric acid for 25 minutes. After the release-etch, the wafers were subjected to different treatments to make them either hydrophobic or hydrophilic. The wafers were hydrophobic after the hydrofluoric acid etch and remained hydrophobic after the post etch deionized water rinsing operation. Another treatment that was used for hydrophobic wafers was to add isopropyl alcohol (IPA) to the rinse water and then rinsing them in pure IPA. The treatment for the hydrophilic wafers involved immersion in 70% nitric acid heated to 100°C for 1 hour followed by rinsing in deionized water.

The stiction data from the beams that were hydrophobic indicated that the primary stiction mechanism at work was Van der Waals forces. The stiction data from the beams that were hydrophilic indicated that the primary stiction mechanism at work was hydrogen bridging. The hydrophobic samples did not always have a clean transition from free standing to stuck down. This was believed to be partially due to surface contamination that could cause a solid bridging between the two surfaces. The shortest stuck beams were used for the energy calculations when this occurred.

The discussions in both studies provided insight on the various stiction mechanisms. This information was useful in designing and carrying out the experimental

work described in this thesis and analyzing the results. There were some issues with the Komvopoulos and Yan study and the Legtenberg *et al.* study. In the Komvopoulos and Yan study, they attempted to correlate all of the stiction mechanisms to surface roughness. The roughness was not correlated to processing parameters so it was not clear what typical roughness parameters were normally encountered in MEMS fabrication. The Legtenberg *et al.* study included a detailed discussion of the different stiction mechanisms; however, the contributions of film thickness variations and surface roughness were not mentioned in great detail. The thickness variations would have impacted beam stiffness and the surface roughness would have affected the capillary attraction force.

2.2 Polysilicon Film Properties

Background information on polysilicon film properties was needed to correlate the impact of these properties on stiction. T.I. Kamins[7] discussed the importance of surface diffusion on thin film properties. The term surface diffusion refers to the movement of the adsorbed atoms on the substrate or growing film surface prior to incorporation into the film. The degree of surface diffusion impacts the grain size and texture of the growing film. The factors that have the greatest influence on surface diffusion are deposition temperature, deposition rate, and deposition pressure. Surface diffusion increases with substrate temperature, but if the temperature is too high, the adsorbed silicon atoms can desorb. The deposition rate is important because the atoms need time to diffuse to the growing nuclei. If the deposition rate is too high, the atoms

will be buried under the growing film before they can diffuse to a growing nucleus. The amorphous films are deposited at low temperatures and the atoms do not have the energy to desorb or diffuse so the nuclei do not fully form. Kamins reported that in LPCVD deposition at pressures on the order of 0.2 Torr, the transition from crystalline to amorphous occurred at 580°C. The dominant thin film texture is also affected by the deposition temperature and pressure since both of these parameters impact atomic arrangement during thin film growth.

Kamins addressed the effects of post deposition processing. The properties of films deposited as amorphous and then crystallized by annealing were different from those deposited as polycrystalline and then annealed. The initially amorphous films have fewer crystallites prior to annealing than the initially polycrystalline films. During annealing, a crystallite in the amorphous films can grow larger due to less infringement from other crystallites. The grain growth for the polycrystalline films tends to be columnar starting at the film/substrate interface and extending to the surface of the film. The amorphous films tend to begin crystallization in the bulk of the film. The final post-annealed grain size depends on the number of crystallites in the amorphous film prior to annealing. The number of crystallites increases with increasing deposition temperatures. For this reason, Kamins stated that amorphous films deposited at lower temperatures have larger grain sizes after annealing than amorphous and polycrystalline films deposited at higher temperatures. The affect of annealing on the dominant film texture is shown in Figure 9[7]. The annealing data presented in Figure 9 was for initially amorphous films deposited at 580°C and initially polycrystalline film deposited at 620°C.

The annealing temperatures ranged from 800°C to 1200°C. The amorphous films showed an increase in the (311) texture with higher annealing temperatures. The polycrystalline films did not show a texture change until 1100°C.

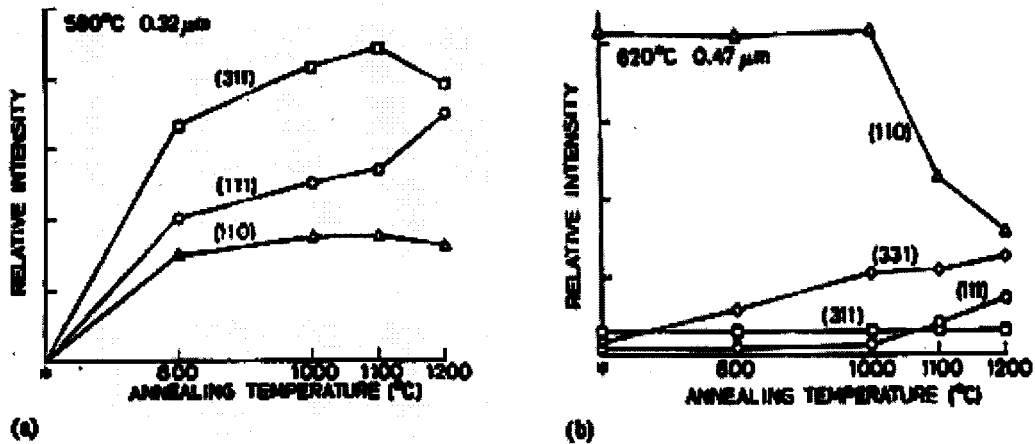


Figure 9. Relative intensity of grain orientations vs. annealing temperature for silicon films deposited in an LPCVD reactor in (a) an initially amorphous form at 580°C and (b) an initially polycrystalline form at 620°C. *As deposited.[7]

Kamins discussed the stress of the films after deposition and after subsequent heat treatments. Films deposited by LPCVD are deposited at temperatures that don't provide enough energy for atomic rearrangement. This can lead to compressive stresses after deposition. Although Kamins does not state the deposition temperature, the data for LPCVD films deposited at 620°C from the present research agreed with his observation. Kamins also stated that the compressive stress decreases with increasing film thickness. It was also stated that stress changes should occur for amorphous after annealing due to crystallization, but that the stress for films deposited as polycrystalline would not change after annealing.

Kamin's study provided useful information on the influence of processing variables on the final polysilicon film properties. The annealing times were not specified so it was not clear whether longer annealing may have had an effect on the film grain size and texture. The statement that annealing had little affect on stress for polycrystalline films did not correlate with the observations from the present research or other studies that showed that annealing changed film stress.

Xiang-Zheng Bo *et al.*[8] studied grain growth during the annealing of amorphous silicon thin films. The Bo *et al.* study examined the grain growth of the amorphous silicon both with and without the underlying silicon dioxide layer. The grain growth was found to be greater without the underlying oxide. The final grain size was determined by the nucleation rate and the grain growth rate as described in the following relationship:

$$d \propto \left[\frac{v_g}{N} \right]^{\frac{1}{3}} \quad \text{Equation 3[8]}$$

d – grain size

v_g – grain growth rate

N – Nucleation Rate

The solid phase crystallization (SPC) usually occurred at the interface between the silicon and oxide where there were a greater number of nucleation sites. After annealing at 600°C for 24 hours, the average grain size for the polysilicon with the underlying oxide was 0.3µm and 0.6µm without an underlying oxide. This was determined by examining samples with transition electron microscopy (TEM). This showed that the oxide had an impact on the silicon film crystallization process.

Bo *et al.* also examined film stress and stated that the stress would increase during SPC due to the volume contraction associated with the transition from amorphous to crystalline form and the resistance of motion of the silicon atoms at the interface between the silicon and oxide.

Hasegawa *et al.*[9] studied the grain structure and texture of polysilicon thin films formed by annealing amorphous silicon films to attain polycrystalline films. Amorphous silicon thin films are normally deposited using silane (SiH₄) gas, however, disilane gas was used in the investigation since it allowed the use of lower deposition temperatures down to 450°C. Silane requires deposition temperatures in excess of 550°C. The lower temperatures were desirable for growing larger grains during annealing.

The amorphous silicon films for the Hasegawa *et al.* experiment were deposited between 450°C and 580°C on fused quartz substrates. The deposition was conducted using the LPCVD process with 100% disilane gas at a flow rate of 2.5 sccm and 1 Torr. The film thicknesses achieved were on the order of 0.7 +/- 0.2µm. All of the amorphous films were annealed at 600°C.

The post annealing grain sizes were estimated using both TEM and x-ray diffraction (XRD). The grain size values perpendicular to the film surface were obtained using the XRD technique where the half-width value of the various diffraction peaks for the crystallographic planes were used to estimate the grain size. The Scherrer equation was applied:

$$\delta = \frac{0.9\lambda}{B \cos \theta} \text{ . Equation 4[9]}$$

δ – grain size

λ - wavelength

B - half-width value diffraction peak

θ - Bragg angle

The grain sizes in the parallel plane of the thin film were estimated using TEM. The grain size results are presented in Figure 10[9] where it can be seen that the largest grain size determined by XRD was on the order of 0.15 μm and the largest grain size determined by TEM was on the order of 2.5 μm . The results suggested that the perpendicular grain sizes were unaffected by the deposition temperature while the parallel grain sizes increased with decreasing deposition temperature. The data also suggests that the largest grains perpendicular to the film surface had <111> texture.

The stresses of the films were examined and it was concluded that the polysilicon films had stresses that were due to thermal expansion coefficient mismatches between the polysilicon film and the substrate. These stresses were the extrinsic components of the overall stresses on the test wafers. The overall film stress is composed of extrinsic and intrinsic stresses. The intrinsic stresses are due to the internal composition of the polysilicon film. The stresses observed in the amorphous films were considered to be primarily intrinsic.

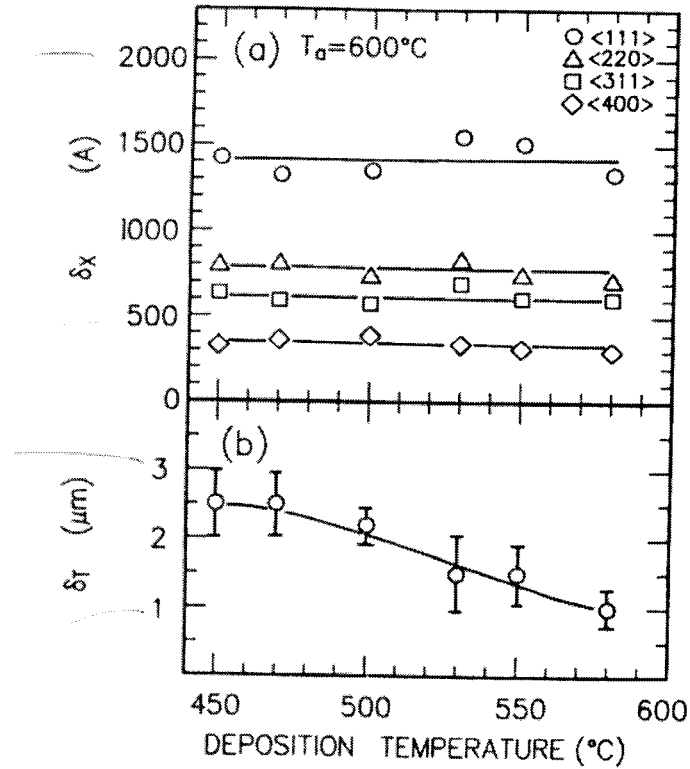


Figure 10. XRD(δ_x) and TEM(δ_T) grain size as a function of deposition temperature.[9]

The film textures were determined using the same XRD technique used to determine the perpendicular grain sizes. The relative intensities of the crystallographic planes of the films were compared to determine the predominant film structures. The XRD technique provided data for the entire film thickness. The data had to be corrected for film thickness variations and variations in sensitivity between the various crystallographic planes. The texture data was correlated with the Raman spectra data, which indicated the degree of crystallization in the thin films. The Raman spectra only

provided crystallinity data for the top 0.3 μm of the 0.7 μm film thickness. Since the annealing time for the onset of crystallization was virtually the same as for the first XRD peak formation, it was concluded that the crystallization was bulk-induced as opposed to surface-induced. The degree of crystallinity for deposition temperatures of 470 $^{\circ}\text{C}$ and 550 $^{\circ}\text{C}$ increased the longer that they were annealed at 600 $^{\circ}\text{C}$. From the data presented in Figure 11[9], the predominant post-annealed structure for amorphous silicon films deposited at 470 $^{\circ}\text{C}$ was $\langle 100 \rangle$ and the predominant structure for amorphous silicon films deposited at 550 $^{\circ}\text{C}$ was $\langle 111 \rangle$. Hasegawa *et al.* stated that the texture differences between the different deposition temperatures were due to the differences in the intrinsic stresses of the films.

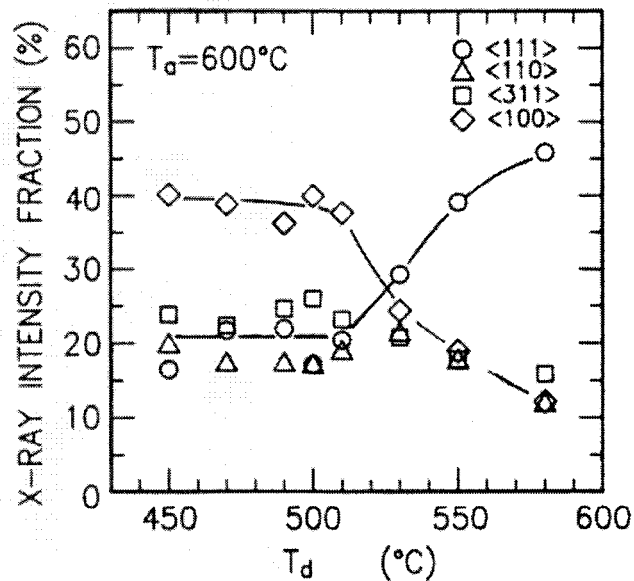


Figure 11. Texture vs. film deposition temperatures, all annealed at 600 $^{\circ}\text{C}$. [9]

The Hasegawa *et al.* study was useful for understanding the effect that deposition and annealing temperatures had on the final crystal structure of initially amorphous silicon thin films. It also provided a brief explanation of the components of the film stress and how stress impacted film properties. There were several areas in the study that raised questions. The number of samples used in the study for the various deposition and annealing conditions was not specified. This data would have been useful since the film thicknesses can vary within a furnace run and between furnace runs. The film thickness could affect the final annealed film properties.

The grain size data that was reported was confusing since the results for the XRD and TEM methods did not follow the same trends. The grain sizes determined by TEM showed a trend with the deposition temperature while the grain sizes determined by XRD did not. This was most likely due to imperfections in the film and the fact that the films were too thin for the XRD technique.

The determination of the dominant texture was also questionable. The data presented in Figure 11 for amorphous films deposited at 500°C showed that the predominant texture of <100> comprised 40% of the film, and the texture of <311> comprised 25% of the film. It was hard to tell if this difference was significant since the amount of error associated with the texture determination was not reported.

2.3 Methods for Assessing Stiction

Mastrangelo and Hsu[10] conducted a study on the surface energy of polysilicon using micromachined cantilever beams. Their investigation was based on the phenomena

where the capillary forces from water trapped under the beams after the post etch release rinse process pulled the beams down onto the substrate surface. The beams remained stuck to the substrate if the elastic restoring forces of the beams are not significant enough to break the bonds between the beams and substrate. It was concluded that this adhesion force was equivalent to the surface energy of the two surfaces in contact. The basic beam configuration is shown in Figure 12[10]. The elastic energy (U_E) of the beam was calculated using the following equation:

$$U = \left(\frac{6EIh^2}{s^3} \right) \left(1 - m - \frac{m}{3} \right) \quad \text{Equation 5[10]}$$

s-Unbonded Beam Length (μm)
 E-Modulus of Silicon ($\text{N}/\mu\text{m}^2$)
 h-Beam height above substrate (μm)
 m-Non-dimensional number related to beam tip slope at contact point
 I-Moment of Inertia of Beam (μm^4)

Where equation for I is:

$$I = \frac{wt^3}{12} \quad \text{Equation 6[10]}$$

w-Beam Width (μm)
 t-Beam Thickness (μm)

The adhesion energy (U_S) of the beam was calculated using the following equation:

$$U_S = -\gamma_s w(L-s) \quad \text{Equation 7[10]}$$

γ_s -Interfacial Surface Energy (mJ/m^2)
 L-Overall Beam Length (μm)

In the literature γ_s is referred to as interfacial energy, surface energy and stiction energy. The term stiction energy is the most correct since there are other factors that contribute to stiction besides surface energy. The overall energy of the beam/substrate system was determined by combining the two energy equations above to get the total energy as shown in the following equation:

$$U_T = (6EIh^2/s^3)(1-m-m/3) - \gamma_s w(L-s) \quad \text{Equation 8 [10]}$$

The equilibrium value for the unbonded length, s^* , was found by differentiating U_T with respect to s and setting this equal to zero. The resulting expression for γ_s was found by evaluating the point where s^* just equals the beam length, which is the point where the beam remains barely attached to the substrate. At this point, the elastic and adhesion energies were balanced. The resulting equation for γ_s was:

$$\gamma_s = \frac{3}{8} \left(\frac{Et^3 h^2}{L_d^4} \right) \quad \text{Equation 9 [10]}$$

L_d -portion of stuck beam that remains unstuck

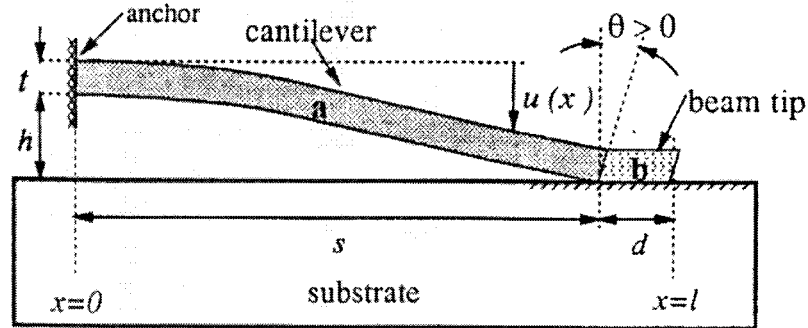


Figure 12. Cross-section of a polysilicon cantilever beam adhering to its substrate. [10]

The beams used were deposited on (100) n-type substrates using LPCVD. The silicon dioxide (SiO₂) layer was deposited using SiH₄ and oxygen (O₂) gases at 300mT and 450°C. The polysilicon layer was deposited using SiH₄ at 320mT and 590°C. The polysilicon films were then annealed at 1050°C for 3 hours to alleviate residual stresses. The SiO₂ was used for both the beam support and the release layer. The release layer was etched away using 49% Hydrofluoric Acid (HF). The beam lengths, L , were varied from 14μm to 300μm in 1μm increments. The beam thicknesses, t , were varied from 0.5μm to 2μm. The support height, h , was varied from 0.5μm to 3μm. The beams were made in two groups with one being hydrophobic and the other being hydrophilic. The hydrophobic beams were rinsed after the HF etch and then air-dried. The hydrophilic samples were immersed in a sulfuric acid (H₂SO₄)/peroxide (H₂O₂) bath and then air-dried.

The results of the Mastrangelo and Hsu investigation for the hydrophilic and hydrophobic beams are shown in Figure 13[10] and Figure 14[10]. These are plots of the detachment length, L_d , versus a function related to the beam dimensions, $(h^2t^3)^{1/4}$, derived from Equation 8. The surface energies were determined by calculating the slope of the line drawn through the data points. The value of γ_s for the hydrophilic samples was 140 ± 70 mJ/m² and the value of γ_s for the hydrophobic samples was 145 ± 70 mJ/m². These values were essentially the same so the experimental method and data reduction techniques used were not able to differentiate between the hydrophobic and hydrophilic surfaces. The surface energy values were approximately twice that of the surface tension

of water, which was stated to be 72mJ/m^2 . From this it was implied that thin films of adsorbed water on each surface might have held the beam and substrate together.

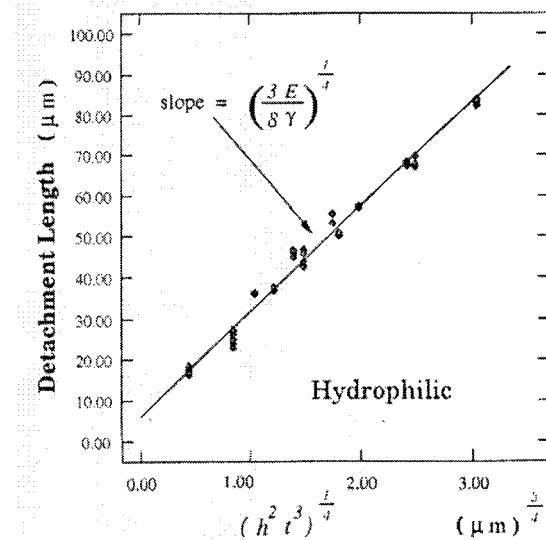


Figure 13. Plot of the detachment length as a function of the parameter $(h^2 t^3)^{1/4}$ for hydrophilic samples. [10]

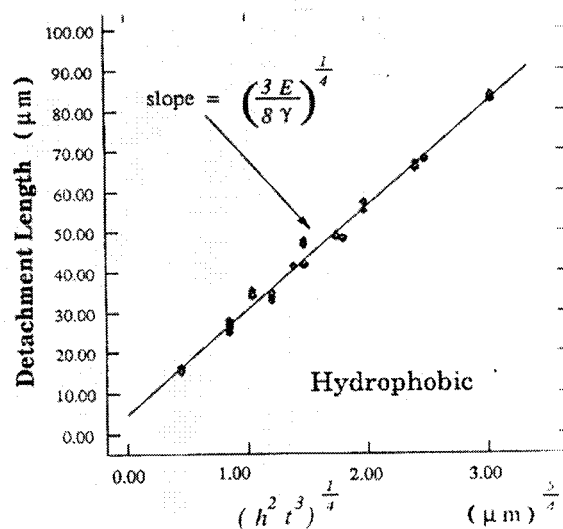


Figure 14. Plot of the detachment length as a function of the parameter $(h^2 t^3)^{1/4}$ for hydrophobic samples. [10]

Michalske and deBoer[11] used a modified version of the Mastrangelo and Hsu technique for measuring the surface energy in their investigation. They applied the same basic principles of balancing the elastic energy of the beam, U_E , and the adhesion energy, U_S , but added fracture mechanics principles as well. By adding the fracture mechanics approach, they were able to calculate surface energies for beams that were attached to the substrate. The stuck beam configurations used by Michalske and deBoer are shown in Figure 15[11]. The two different shapes possible for the beams after sticking were arc-shaped and *s*-shaped.

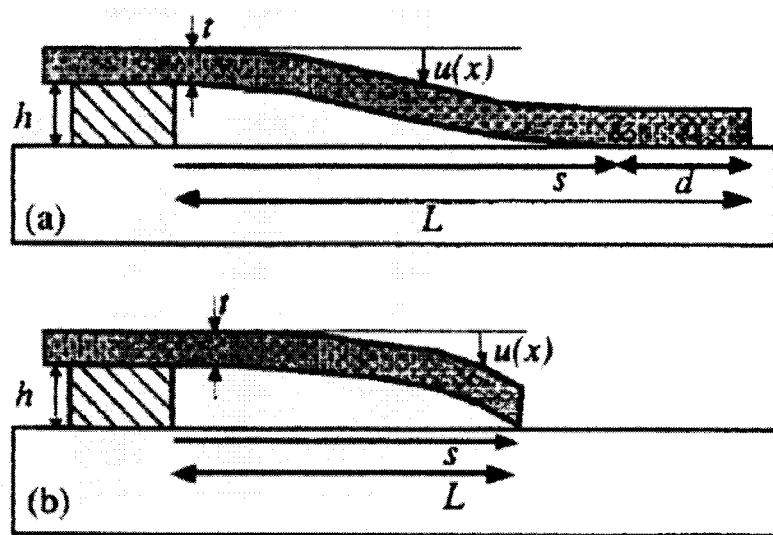


Figure 15. (a) S-shaped beams ($m=0$) are attached over a long length d . (b) Arc-shaped beams ($m=3/2$) are attached only very near their tips. [11]

The Mastrangelo and Hsu study focused on the arc shaped beam since this is the beam configuration just before the beam breaks free from the surface. Using the arc-shaped configuration introduced inherent error since the contact dimension, d , was very

small and difficult to measure. Michalske and deBoer focused more on the *s*-shaped configuration. The *m* value for *s*-shaped beams was 0 and the *m* value for arc-shaped beams was 1.5.

The fracture mechanics concept of the crack driving force, *G*, was employed in this study. The crack driving force was defined by the equation:

$$G = -\left(\frac{1}{w}\right)\frac{dU_T}{ds} \quad \text{Equation 10[11]}$$

The *s* was considered to be the crack length and *w* was the beam width. When the crack driving force was equal to the interfacial surface energy, Γ , then the interfacial surface energy could be determined. The equations for the interfacial surface energy for both mode shapes were:

$$G = \Gamma = \frac{3}{2}\left(\frac{Et^3h^2}{s^4}\right) \quad \text{Equation 11[11]}$$

$$G = \Gamma = \frac{3}{8}\left(\frac{Et^3h^2}{s^4}\right) \quad \text{Equation 12[11]}$$

Where Γ was equal to $2\gamma_s$, since both the beam and substrate were made of the same material.

The experimental approach used was similar to the one used by Mastrangelo and Hsu except that the beam widths, thicknesses, and heights above the substrate were all the same. The polysilicon was deposited at 600°C and annealed at 1100°C. The annealing

step was performed to alleviate stress in the film. The hydrophilic beams were immersed in H₂O₂ after the post-etch rinse and then air-dried after final rinse. The hydrophobic beams were immersed in octadecyltrichlorosilane (ODTS) after the post-etch rinse. This left a thin layer of ODTS on the beams prior to final rinse. The hydrophobic beams were also air-dried.

The results demonstrated that the actual beam deflection behavior followed the theoretical predictions. The shortest hydrophilic beam that remained adhered to the substrate was 58 μ m. An adhesion shape transfer from arc to *s*-shape occurred at a beam length of approximately 145 μ m. The shortest hydrophobic beam that remained adhered to the substrate was 120 μ m. The transition from arc to *s*-shape occurred at 250 μ m. The resulting average stiction energy values are shown in Table 1[11]. The data in this table is for both hydrophilic and hydrophobic beams adhered in both the *s*-shaped and arc-shaped configurations. The corrected data took into account the compliance of the beam support structure. The average stiction energies, γ_s , for the polysilicon thin films, which were equal to one-half of the interfacial surface energies, are also included in Table 1.

Table 1. Corrected Values of Γ . [11]

Treatment	Beam Shape	s_{min} (μ m)	Uncorrected Γ (mJ/m^2)	Corrected Γ (mJ/m^2)	γ_s (mJ/m^2)
Hydrophilic	Arc	58	222	91	45.5
	S	172	11.3	9.4	4.7
Hydrophobic	Arc	120	12.1	9.5	4.75
	S	225	3.9	3.6	1.8

The difference between the s-shaped and arc shaped stuck beams was the amount of surface area available for bonding. For rougher films, there would be less possible area for capillary forces to pull the beams into contact with the substrate. The s-shaped beams are less affected by surface roughness due to the greater contact area. Michalske and deBoer also mentioned that for the arc shaped beams, impurities could collect at the tip during drying and could create a solid bridge between the beam and the substrate.

The hydrophobic and hydrophilic forces were different as predicted by equation 13[11], which showed the relationship between the critical wetting angle and the adhesion strength due to capillary attraction.

$$\Gamma_{\text{cap}} = \gamma_s \cos \theta_c \quad \text{Equation 13[11]}$$

Γ_{cap} – Capillary Force

γ_s – Surface Tension of Water

θ_c - Critical Wetting Angle

The Mastrangelo and Hsu and Michalske and deBoer studies provided a wealth of information on conducting beam experiments and interpreting the data. Unfortunately, information on the number of samples analyzed was not included in either study. This information would have been useful to assess whether their results were statistically significant.

Neither study mentioned the amount of drying time after the various post etch treatments and rinsing operations. Capillary forces are the primary cause for beams being pulled down to the substrate and the capillary forces are caused by the rinsing water trapped under the released beams. The drying time is significant since the capillary

forces decrease as the water evaporates. Ultimately, many of the beams will become unstuck due to their restoring forces unless other stiction mechanisms are at work. The experimental results can be misleading if stiction measurements are made prior to complete drying.

There was also no mention of the effect that film stress could have had on stiction. Both experiments had annealing steps to reduce the film stresses from deposition. In the present experiment, film stress affected beam curvature. Beams curving down could appear stuck even though they are not. Beams curved up may not be susceptible to meniscus formation during the rinsing operation and therefore would not be drawn to the substrate.

2.4 Literature Review Summary

The studies reviewed in the literature review provided information that was useful in planning and executing the present research as well as providing insight on interpreting the experimental results. The summary of results of the reviewed studies were:

1. Komvopoulos and Yan found that surface roughness impacted stiction.
2. Legtenberg *et al.* determined that the stiction mechanism for hydrophobic surfaces was Van der Waals forces and for hydrophilic surfaces it was hydrogen bonding.
3. Kamins found that the polysilicon thin film structural properties were affected by the deposition and annealing temperatures.

4. Xiang Bo *et al.* found that the underlying oxide influenced polysilicon grain growth.
5. Xiang Bo *et al.* found that polysilicon film stress changed during annealing.
6. Hasegawa *et al.* found that polysilicon grain size and texture were impacted by the deposition temperature.
7. Hasegawa *et al.* determined that the stresses observed in polysilicon films were extrinsic and the stresses observed in amorphous films were intrinsic.
8. Mastrangelo and Hsu determined that the adhesion energy holding stuck beams down was roughly twice the surface energy of water.
9. Mastrangelo and Hsu did not find adhesion energy differences between hydrophobic and hydrophilic surfaces.
10. Michalske and deBoer found that the shortest hydrophilic stuck beam was 58 μm and the shortest hydrophobic stuck beam was 120 μm .

The knowledge from not only the results of these studies, but also the experimental methodology used was valuable in the design, execution, and analyses phases of the present experiment. The Komvopoulos and Yan study and the Legtenberg study provided information on the different stiction mechanisms as well as the affect that the polysilicon surface properties had on stiction. The Legtenberg study pointed out that post-release stiction occurred in two parts with the first being the initial pull down of the beams due to capillary forces followed by one of the other stiction mechanisms, such as

Van der Waals forces, holding the beams in place after the water evaporated. The impact that deposition and annealing temperature had on polysilicon film structure mentioned in the Kamins, Xiang Bo *et al.*, and Hasegawa *et al.* provided the information necessary to establish the deposition and annealing temperatures. The experimental approach employed by Mastrangelo and Hsu and Michalske and deBoer was used in the present research. The discussion of beam theory was particularly useful for calculating the minimum stuck beam lengths and adhesion energies.

CHAPTER 3

EXPERIMENTAL METHODS

3.1 Experimental Objective

The experimental objective was to produce micromachined cantilever beams from polysilicon thin films having different grain sizes, textures, and surface properties and then use these beams to investigate the impact that these properties have on stiction.

3.2 Hypothesis

The grain boundary regions on polysilicon thin films are characterized by disorder with high concentrations of defects. This means that the greater the area of grain boundaries on the film surface, the higher the surface energy. The surface properties of polysilicon thin films with larger grain sizes are therefore different from polysilicon thin films with smaller grain sizes. Surfaces with higher surface energies are more reactive since the tendency for the substrate/beam system is to reduce the overall energy. Adhesion or stiction is one of the means to reduce surface energy. Considering that surface energy is an important factor in stiction, MEMS devices made from polysilicon thin films with larger grain structures should be less susceptible to stiction than those made from polysilicon thin films from smaller grain structures from a surface energy perspective.

The predominant texture of the polysilicon thin films also plays an important role in stiction since the surface roughness and atomic packing are impacted by the texture. The term “texture” refers to the preferred crystallographic orientation of the grains in the thin film. The close-packed planes for silicon, which has a diamond cubic crystal structure, are the {110} family of planes. When the texture of the polysilicon thin film is {110}, the density of surface atoms should be higher than for other planes. The surface energy of the {110} plane should be the lowest since there are fewer broken bonds on the surface. Surfaces with the {110} texture should be less susceptible to stiction.

The impact of polysilicon thin film surface roughness on stiction was discussed in the literature. Komvopoulos and Yan found that rougher films were less susceptible to stiction due to the fact that there is less surface area coming into contact. This is true not only for capillary forces, but for Van der Waals forces, hydrogen bridging, and solid bridging.

3.3 Experimental Methodology

The experimental approach that was used involved varying the silicon deposition and annealing temperatures. Previous studies had shown that the deposition and annealing temperatures affected both the grain size and texture of polysilicon thin films[8,11,12]. For silicon thin films that were initially polycrystalline, the annealing conditions have been found to have little effect on texture. The annealing conditions did affect the texture of the initially amorphous films since they developed crystalline

structure during annealing. The deposition and annealing conditions used are presented in Table 2.

Table 2. Deposition and Annealing Conditions.

Deposition Temperature	Anneal	# Beam Wafers
585 °C	550 °C-18hr 1000 °C-1.75hr	AT
	550 °C-12hr 1000 °C-2hr	A1
	1000 °C-3hr	B1, B2
600 °C	550 °C-18hr 1000 °C-1.75hr	CT
	550 °C-12hr 1000 °C-2hr	C1
	1000 °C-3hr	D1, D2
620 °C	550 °C-18hr 1000 °C-1.75hr	ET
	550 °C-12hr 1000 °C-2hr	E1
	1000 °C-3hr	H1, H2
Total		12

The deposition temperatures were selected to get amorphous, semi-amorphous and polycrystalline silicon films. The annealing conditions were selected to vary the grain sizes and textures between the wafers and to reduce film stress. Reducing the film stress was important for producing straight beams. The annealing temperatures selected

were 550°C and 1000°C. The 550°C anneal required an additional 1000°C step to bring the film stress down to below 100MPa, which was important for assuring that the beams were straight.

Since the crystallization of the amorphous and semi-amorphous films involves nucleation and grain growth, the degree that each of these occurs impacts grain size. If nucleation dominates, then the final grain sizes won't be as large since the greater number of growing grains will impinge on one another more rapidly. If grain growth dominates, then there will be fewer growing grains and grains can grow larger without impinging on one another. It was hypothesized that the 550°C annealing temperature is less conducive to nucleation than the 1000°C annealing temperature so the silicon films annealed at 550°C would have larger grains.

Cantilever beam sets were then made on each wafer. The beam lengths were varied from 60 to 400µm in 20µm increments. These lengths were based on the results of the de Boer and Michalske study[11]. The beam configuration that was used is shown in Figure 16. The beam thickness, width, and height above the substrate were not varied although the processing has inherent variations so there were some differences. This was primarily true for the amorphous and polycrystalline silicon films. After the post release etch rinsing step, the wafers were examined using an interferometer and the degree of stiction observed was then compared between the wafers.

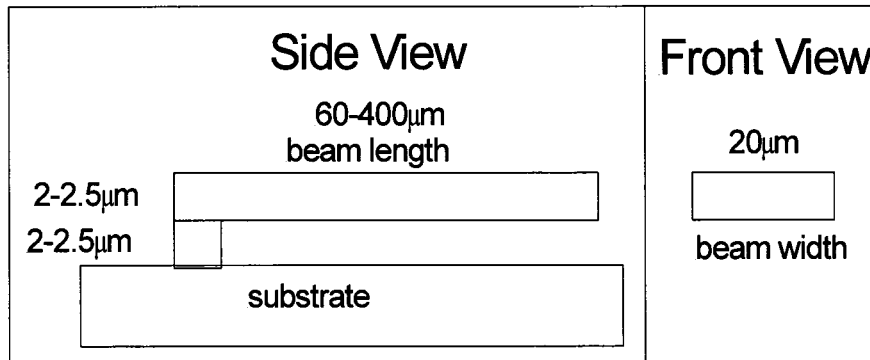


Figure 16. Cantilever beam configuration.

This approach was similar to those used in previous studies[9,10] to measure interfacial adhesion energy. In these studies, the calculations of the interfacial adhesion energy were based on either the shortest unstuck length for arc shaped stuck beams or on the length of an s-shaped stuck beam that remained unstuck. Both approaches involved the use of a microscope combined with a Michelson Interferometer, but the measurement of the s-shaped unstuck beam length involved the addition of software to interpret the interferometer image and provide data on the beam height along the entire beam length. The interferometer used for this experiment did not have this capability so the focus was on whether the beams were stuck in the arc or s-shaped configuration and not on the unstuck length of the s-shaped stuck beams.

3.4 Beam Fabrication

The primary processes used to manufacture the beams are presented in the process flow diagram shown in Figure 17. Basic processes such as pre-diffusion cleaning and

visual inspections are not included in the process flow diagram. The stress measurements were not performed for every wafer. Stress measurements were used to establish the annealing times. Silicon thickness measurements were also not taken for every wafer, but were taken on a sample of wafers for process characterization. The primary processes are discussed in the following sections.

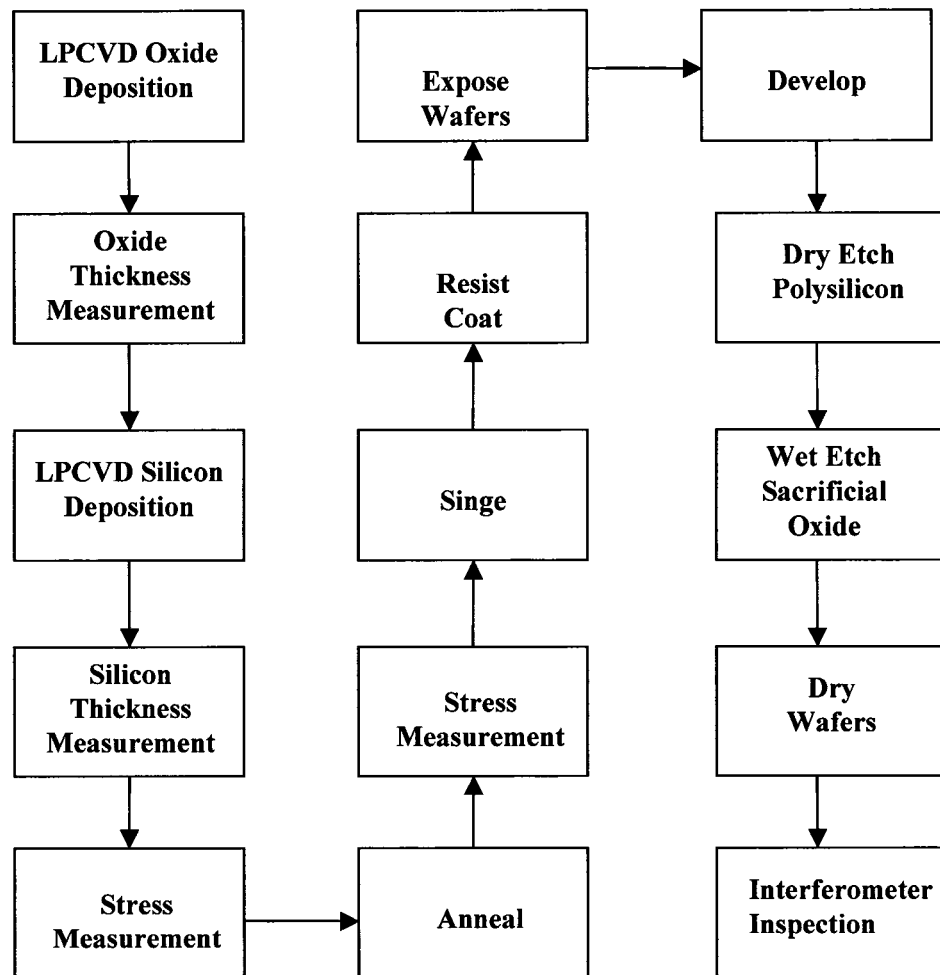


Figure 17. Process flow chart.

3.4.1 Deposition Processes

The experimental beams were fabricated on 4-inch p-type <100> substrates with either 2-2.5 μm polycrystalline or amorphous silicon thin films on top of 2-2.2 μm SiO_2 thin films. The matrix of test wafer polysilicon deposition temperatures and annealing times is shown in Table 2. Silicon and SiO_2 thin films were deposited at the Stanford Nanofabrication Facility using the Tylan LPCVD furnaces. The SiO_2 films were deposited by pyrolysis of silane (SiH_4) and oxygen at 400°C and 350mTorr. The amorphous silicon was deposited by pyrolysis of SiH_4 at 585°C and 400mTorr. The semi-amorphous silicon was deposited at 600°C and 400mTorr. The polycrystalline silicon was deposited at 620°C and 400mtorr.

3.4.2 Annealing

The two different annealing temperatures were used since the annealing temperature has been linked to the final grain size of polysilicon thin films[8,9]. The wafers were annealed in a quartz tube furnace in a nitrogen atmosphere at atmospheric pressure. The annealing was done for three reasons;

1. To crystallize the amorphous films
2. To modify grain size
3. To relieve film stress

The studies referenced in the literature review chapter stated that amorphous silicon films crystallized during annealing. The link between the annealing temperature and grain size

was also mentioned. The studies on cantilever beam fabrication all included an annealing step to reduce the film stress so that the released beams would not curve down or up. The experimental annealing process was characterized by annealing the wafers in intervals with stress measurements after each interval. Stress measurements were taken using the Frontier Semiconductor Measurement Systems SMSi 3800® stress tester at Stanford. The data was used to determine the appropriate times for both the 550°C and 1000°C annealing processes for each of the deposition temperatures (585°C, 600°C and 620°C). The target was to attain stresses below 100MPa.

The 1000°C annealing process was easier to characterize since the same process had been used in the Mastrangelo and Hsu study[10]. All of the wafers were sufficiently stress relieved for beam production after 3 hours, which was consistent with the Mastrangelo and Hsu study. The 1000°C annealing process characterization run for a wafer with polysilicon deposited at 620°C is shown in Figure 18. The wafer used for this test started at a high compressive stress of -197 MPa and after 100 minutes of annealing at 1000°C, the stress transitioned from compressive to tensile. After 2 hours and 45 minutes, the stress returned to the compressive side with the final stress being -3.5 MPa. From the 1000°C annealing process characterization runs for the 585°C amorphous silicon and 600°C semi-amorphous silicon, it was found that a 3 hour annealing time was also sufficient. Both of these films started out highly tensile at 220 MPa and 394 MPa and were reduced to -9 MPa and 7 MPa, respectively. The 1000°C anneal time for all of the wafers was set at 3 hours.

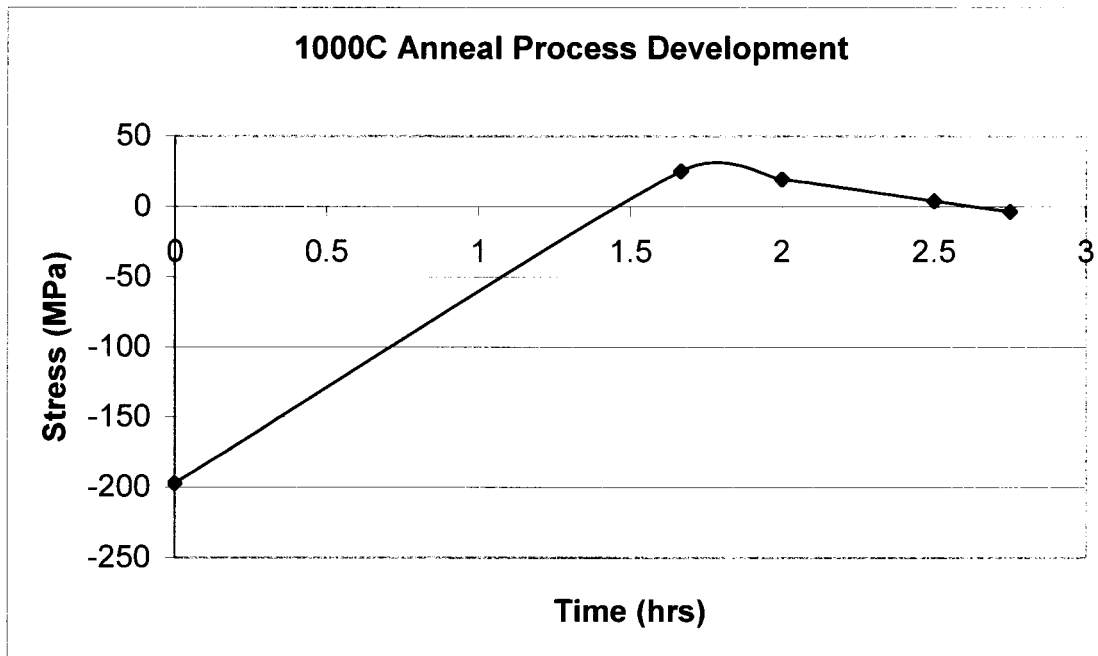


Figure 18. 1000°C annealing stress history.

The 550°C annealing process was more difficult to characterize since the annealing times were much longer. Annealing was performed in 3 hour increments of up to 12 hours and then an additional 6 hour step to bring the total annealing time to 18 hours. Ultimately, the wafers required a final anneal at 1000°C to bring the stresses down to acceptable levels for producing straight beams. The annealing processing for the three deposition temperatures is shown in Figure 19. The data presented in Figure 19 indicates that the 585°C and 600°C silicon thin films are changing dramatically during the 550°C annealing step. The pre-anneal and post anneal stress values for the 550°C/1000°C annealing process are shown in Table 3. The differences in the initial stresses for the 585°C and 600°C films are due to the differences in the amount of atomic arrangement of

silicon that occurs on the wafer surfaces. Both are compressive which agrees with the literature. The polysilicon film deposited at 620°C was under tensile stress due to a thermal coefficient of expansion mismatch between the polysilicon and the underlying oxide layer. Previous studies [7,8,9] had shown that the amorphous and semi-amorphous films experienced crystallization and grain growth during annealing. This is most likely what caused the stress changes witnessed after annealing.

Table 3. 550°C/1000°C anneal stress values.

Wafer	Pre-Anneal Stress	Post-Anneal Stress
600°C dep, 550°C/1000°C anneal	357.44MPa	-34.11MPa
620°C dep, 550°C/1000°C anneal	-159.66MPa	-13.24MPa
585°C dep, 550°C/1000°C anneal	213.94MPa	72.57MPa

(-) compressive, (+) tensile

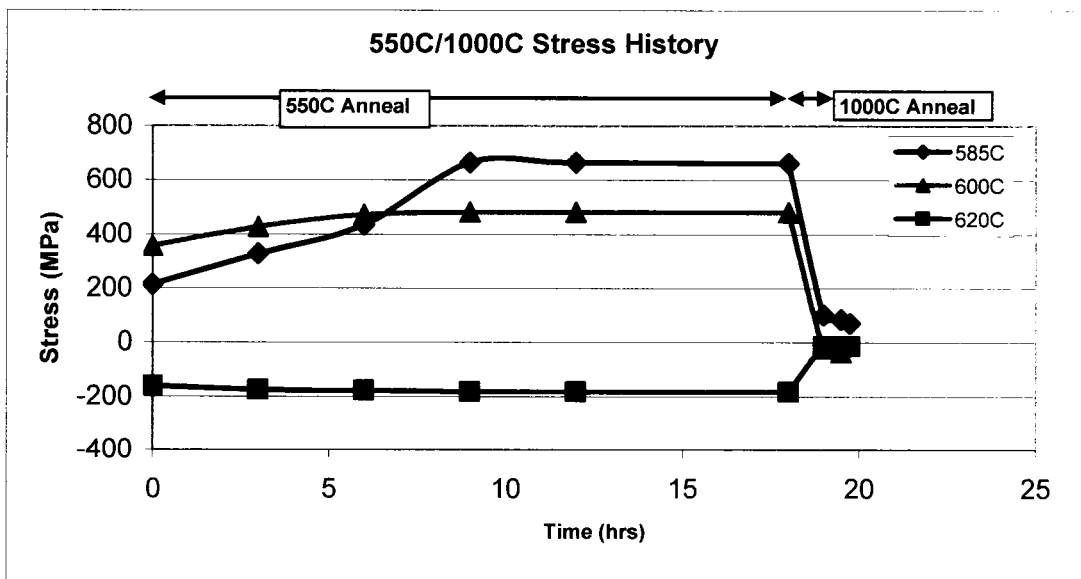


Figure 19. 550°C/1000°C anneal stress history.

Based on the examination of the data shown in Figure 19, it was decided that annealing past 12 hours at 550°C had no real effect on the stress, so the remaining wafers were annealed for 12 hours at 550°C followed by a 1000°C annealing step for 2 hours.

3.4.3 Photolithography

The photolithography process was conducted after annealing. One of the standard processes commonly used for similar applications in the Stanford lab was selected for this experiment. The process consisted of the following steps:

1. 150°C singe for 30 minutes
2. Prime with Hexamethyldisilazane (HMDS)
3. Spin on 1.6µm of Shipley 3612 positive resist on Silicon Valley Group (SVG) coater track at 2000 rpm for 30 seconds
4. Pre-bake at 90°C for 2 minutes
5. Expose on Karl Suss Contact Aligner for 1.7 seconds
6. Post Exposure bake at 115°C for 90 seconds
7. Develop on SVG developer track for 120 seconds in Shipley LDD-26W
8. Post Bake at 110°C for 2 minutes

In step 2, the Hexamethyldisilazane (HMDS) priming process was used to improve the adhesion between the photoresist and substrate surface oxides. The HMDS

reacts with the oxide surface in a process known as silylation, forming a strong bond to the surface. At the same time free bonds are left, which readily react with the photoresist to enhance adhesion[15].

Several test runs were performed to establish the exposure time on the Karl Suss Contact Aligner®. Based on optical observations, a 1.7 second exposure time provided the best pattern transfer. The wafer mask used to pattern the beams onto the wafers is shown in Figure 20, and one of the beam clusters on the mask is shown in Figure 21. The mask consisted of 43 beam clusters with 54 beams per cluster.

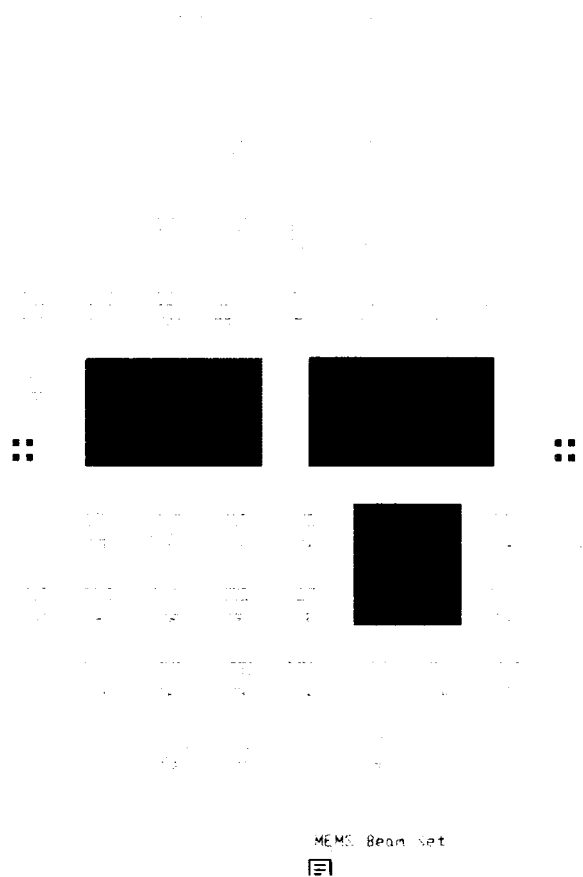


Figure 20. Beam mask with 43 beam clusters.

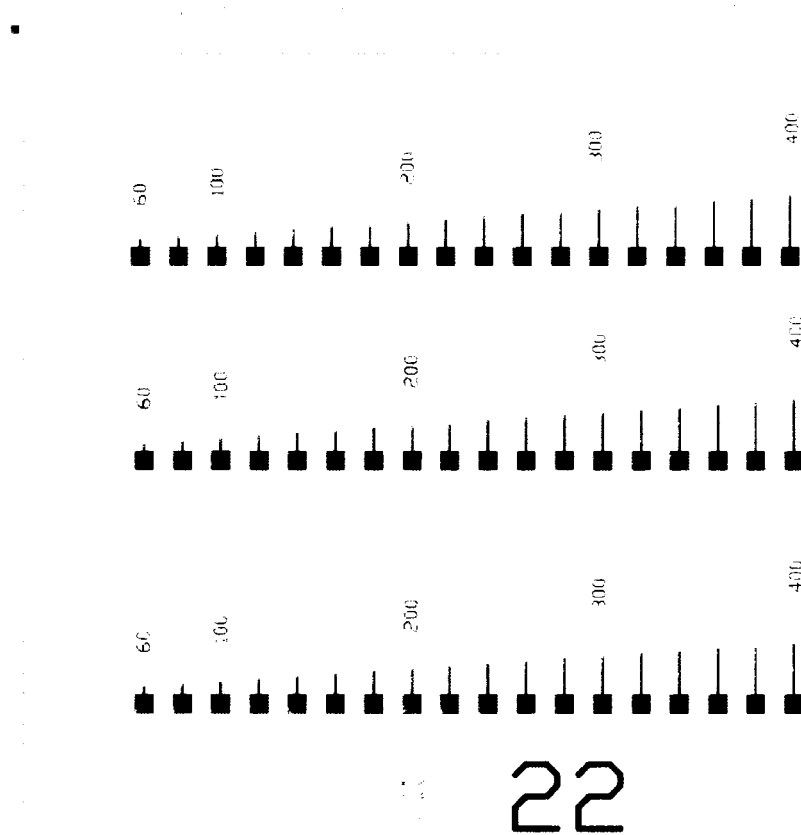


Figure 21. Beam cluster with 3 groups with 18 beams per group.

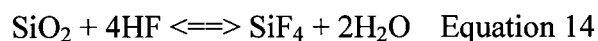
3.4.4 Dry Etching

The process used for etching the polysilicon not protected by the photoresist was reactive ion etching. This was done on the Drytek® 2 plasma etcher at Stanford. The gases used for etching polysilicon were Sulfur Hexafluoride (SF_6) and Freon22 (CHClF_2). The flow settings were 117sccm of SF_6 and 51sccm of CHClF_2 . The RF

power for the plasma was 400Watts with the reflected power not being greater than 20Watts. The chamber pressure was 150mTorr. The Drytek2 could accommodate 6 wafers at one time. The approximate etch rate for polysilicon determined from trial runs was about 1600Å/min. The estimated etch rate for LPCVD oxide was much less and was approximated to be 200Å/min. The etching process took a total of 15-20 minutes per wafer. The process was performed incrementally with inspections between each increment. The etching was complete when the oxide under the polysilicon looked free from any polysilicon residue. The wafers were then immersed in a heated piranha etch (9:1 H₂SO₄:H₂O₂ at 120°C) for 20 minutes to strip the resist.

3.4.5 Release Etch

In order to release the beams, the oxide under the beams had to be etched away without etching away the polysilicon beams. Therefore, the etchant had to have a high selectivity towards the oxide while not etching the polysilicon. For this reason the buffered oxide etch (BOE) solutions was selected. BOE does not etch polysilicon and has a relatively high etch rate for oxide (400-1650Å/min for 20:1 BOE and 1400-6000Å/min for 6:1 BOE). BOE is composed of hydrofluoric acid (HF) and NH₄F. The etching is accomplished by the HF. The NH₄F is a buffer solution that maintains the PH of the BOE solution. The chemical reactions for HF etching and solution buffering are shown in equations 13 and 14.



The amount of etch time to release the beams was determined using the etch indicators below each beam cluster. These indicators are shown in Figure 19 under the beam cluster. They are small squares with 10 μ m, 15 μ m, 20 μ m, and 30 μ m side dimensions. The wafers were removed periodically from the BOE solution, rinsed, and then examined with a microscope. The etch indicators allowed the degree of etch to be estimated. Since the beams were 20 μ m wide, the removal of the 20 μ m etch indicator indicated that the oxide under the beams in the cluster corresponding to the etch indicator had been removed and the beams were released. However, the etch process was not uniform, so not all of the 20 μ m indicators were removed at the same time. Some over-etch was tolerable since the beam bases were 150 μ m squares. Etching beyond the 30 μ m etch indicator was not desirable because the stiffness of the beams could change due to excessive undercutting of the base. The release etch process took approximately 1.5 to 3.5hrs to complete. The wafers were not spun-dried after the post-release etch rinse to minimize the possibility of breaking the released beams. The excess water on each wafer was gently blown away with nitrogen and then the wafers were placed in the storage cassettes. The wafers were left in the cassettes to dry at ambient temperature and humidity without any further treatment.

3.5 Data Collection

The oxide and silicon thin film thicknesses were measure using a Nanometrics Nanospec System®. The system uses non-contact spectro-reflectometry to measure the

thickness of semi-transparent thin films that are reflective in the visible range[17]. The measurement process involves comparing the intensity of reflected light from a bare silicon wafer and from a silicon wafer with a thin film on the surface. The Nanospec takes spot measurements so several places on the wafer have to be examined to fully assess the thin film thickness on the entire wafer. The film thicknesses were measured in five locations, which are shown in Figure 22.

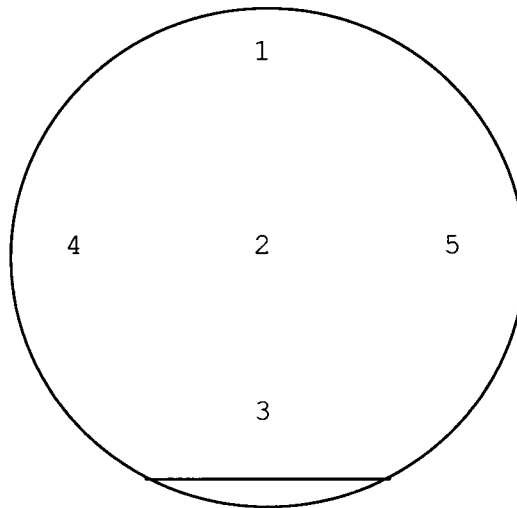


Figure 22. Thickness measurement locations.

The overall film stress was measured on a Frontier Semiconductor Measurement Systems SMSi 3800. The SMSi 3800 measures wafer curvature by deflection of a scanning laser beam. The curvature was converted to stress using the following equation:

$$\sigma = \frac{Eh^2}{(1-\nu) 6Rt} \quad \text{Equation 16}$$

- σ – Avg. Film Stress
- E – Young's Modulus
- ν – Poisson's Ratio
- R – Substrate Radius of Curvature
- T – Film Thickness
- h – Substrate Thickness

The overall film stress is defined as a combination of the extrinsic film stress and the intrinsic film stress. The extrinsic film stress is caused by external factors such as mismatches in thermal expansion properties between the polysilicon film and the underlying oxide and substrate. The intrinsic stresses are due to the internal thin film structure. Individual scans and maps, consisting of 6 scans at 30° intervals, were taken. An example of a stress map from the SMSi 3800 is shown in Figure 23.

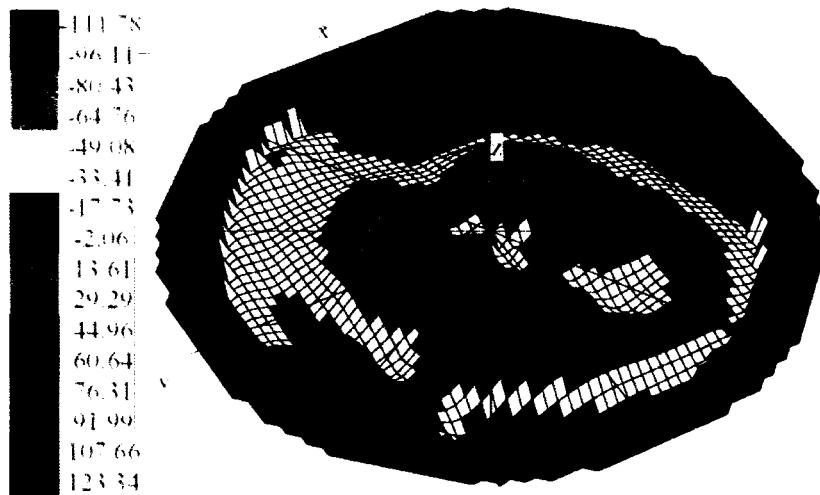


Figure 23. Wafer ET stress profile.

Beam stiction was assessed using a Zygo® white-light 3D surface profiler. The Zygo® assesses the topography of a surface through scanning white-light interferometry, which is a technique in which patterns of bright and dark lines (fringes) result from an optical path difference between a reference and a sample beam. The incoming light is split inside an interferometer with one beam going to an internal reference surface and the other to the sample. After reflection, the beams recombine inside the interferometer, undergoing constructive and destructive interference and producing a light and dark fringe pattern[16]. The data from the Zygo® showed whether beams were straight, curved up, or curved down. The Zygo® produced data in a variety of forms including observing fringe patterns on the visual screen and saving images of individual beams. Examples of the beam images are shown in Figures 24 and 25. The heights of the beam bases and tips were measured on the Zygo® for each wafer to provide an indication of the polysilicon film stress. The beams that curved up indicated tensile film stress while the beams that curved down indicated compressive film stress.

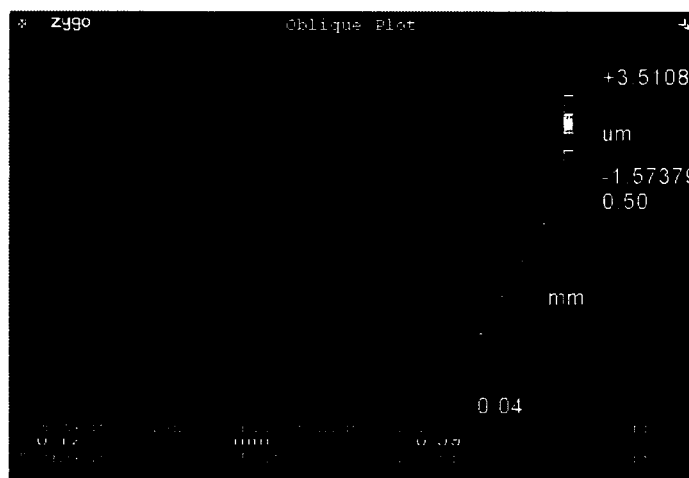


Figure 24. Image from Zygo® interferometer of beam with tip stuck to substrate.

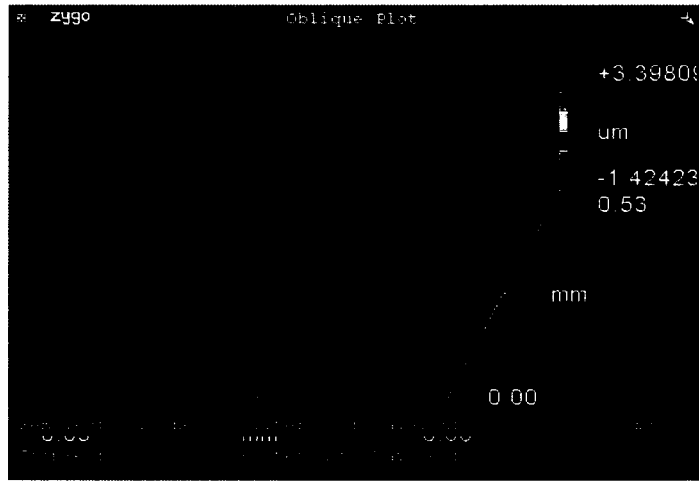
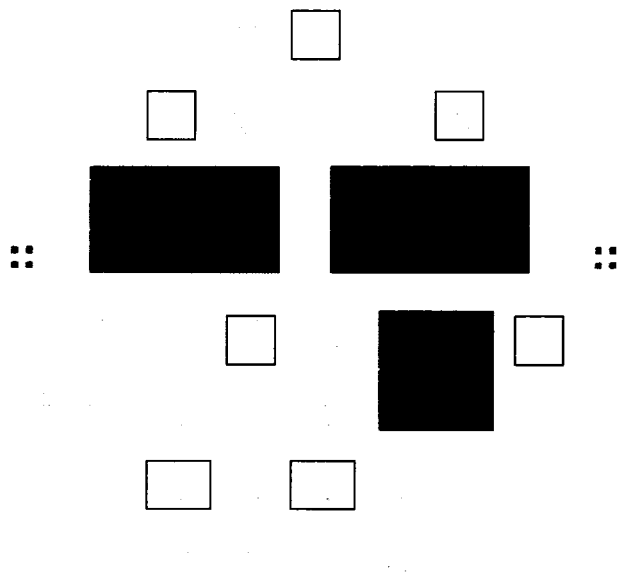


Figure 25. Zygo® image of beam stuck to substrate in s-shape.

There were 43 groups of beam clusters on each wafer with 54 beams per cluster. Due to the large number of beams on each wafer, data was taken for only 7 of the groups. The 7 groups were located in different areas of the wafers as shown in Figure 26. Since the release etching process was not uniform or certain beam clusters were observed to be damaged, other groups were often substituted for the target groups, although the replacement groups were in the same basic area. The Zygo® was configured with a 20x lens for the beam examination because it provided the best data. With the 20x lens, only 3 beams could be examined at one time so each wafer took a significant amount of time to inspect. For this reason, images could not be captured for all stuck beams. Most of the data taken was from visual inspections where the fringe patterns indicated whether beams were stuck. When there was doubt as to whether beams were stuck or whether the beam was stuck in an arc or s-shaped configuration, an image of the beam was captured and examined.



MEMO Beam Ser

Figure 26. Target beam cluster groups for interferometer inspection.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Overall Results

The stiction results from this investigation are presented in Table 4, which includes the deposition and annealing conditions, overall drying time, and the percentage of stuck beams per wafer. The greatest amount of stiction occurred on the wafer with semi-amorphous silicon deposited at 600°C and annealed for 18 hours at 550°C followed by 1.5 hours at 1000°C (CT), and the wafer with polysilicon deposited at 620°C and annealed for 18 hours at 550°C followed by 1.75 hours at 1000°C (ET). Wafer CT had 16 percent of the beams stuck and wafer ET had 9.8 percent of the beams stuck.

Table 4. Stiction Data Summary.

Wafer	Deposition Temperature	Annealing Condition	Drying Time (days)	% Beams Stuck
A1	585°C	550°C-12hrs 1000°C-2hrs	10	0.0
AT	585°C	550°C-18hrs 1000°C-1.75hrs	9	0.0
C1	600°C	550°C-12hrs 1000°C-2hrs	9	5.0
CT	600°C	550°C-18hrs 1000°C-1.5hrs	10	16.0
E1	620°C	550°C-12hrs 1000°C-2hrs	9	3.7
ET	620°C	550°C-18hrs 1000°C-1.75hrs	9	9.8
B1	585°C	1000°C-3hrs	9	2.4
B2	585°C	1000°C-3hrs	10	2.7
D1	600°C	1000°C-3hrs	10	2.7
D2	600°C	1000°C-3hrs	10	6.1
H1	620°C	1000°C-3hrs	9	3.0
H2	620°C	1000°C-3hrs	11	3.7

The number of the beams stuck relative to beam length is shown in Figure 27, which is a histogram for all of the stuck beams on all of the wafers. Based on previous studies[6,10,11], the expectation was for there to be a transition length from beams being stuck in an arc-shape to beams being stuck in an s-shape and for beams to not be stuck at all. The expectation was for the longer beams to be stuck in the s-shape. This was because the longer beams are not as stiff and require less capillary force to pull down to the substrate than the shorter beams. The lower stiffness also made the longer beams easier to hold down after the rinse water evaporated. As the beams decrease in length they become stiffer and require higher forces to pull them down and hold them down once the capillary forces disappear. The stiffer beams tend to stick at tips of beams creating an arc-shape. At the point where the stiffness of the shorter beams becomes higher than the capillary force, the beams were not expected to stick at all. The beam widths, thicknesses, and heights above the substrate used in this experiment were the same as those used in the study by de Boer and Michalske. The results for the de Boer and Michalske study were that the shortest stuck beam for the hydrophobic wafers was 120 μm . They observed a transition from the arc-shaped to s-shaped stuck beams at 245-250 μm .

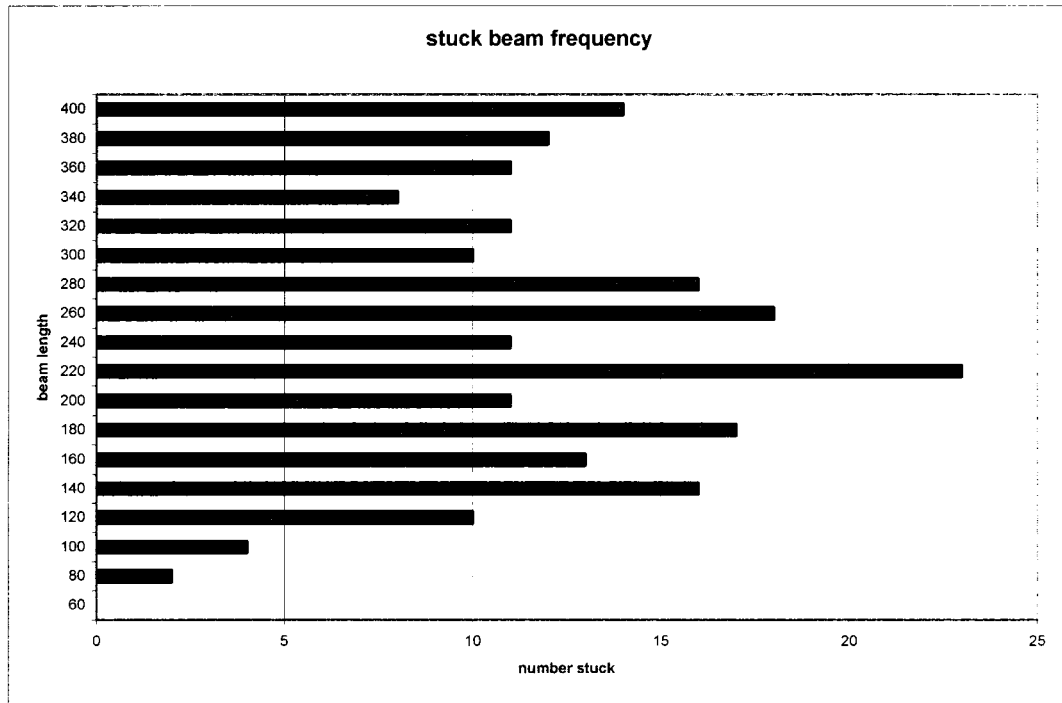


Figure 27. Histogram of beam length versus stiction.

The transitions mentioned were not observed in this investigation. The beam lengths used in this experiment ranged from 60μm to 400μm in 20μm increments. The data in Figure 27 shows that the beam length with the highest number of stuck beams was 220μm. On the wafer with the shortest stuck beam, which was 80μm, longer beams remained unstuck. Although the beam dimensions were basically the same as the de Boer and Michalske study, it was not clear from their study the number of beam groups that they examined and the statistical spread that they encountered. They also used different post etch processes to establish the polysilicon film surface properties. The hydrophobic samples in their experiment were treated with octadecyltrichlorosilane (ODTS), while the wafers in this experiment were hydrophobic due to the HF release

etch process. The ODTs coating may have provided a more uniform surface condition and a different surface energy.

The variability witnessed was most likely due to the substrate and beam surfaces being hydrophobic. The hydrophobic surfaces did not wet the wafer surfaces uniformly. In studies by Legtenberg et al.[6] and Mastrangelo and Hsu[10], similar variability for hydrophobic beams was encountered. The reason for this was estimated to be dynamic capillary effects, local surface asperities, dust particles, and other contamination.

4.2 Statistical Analysis

Since the number of beams that were stuck was small compared to the number of beams examined, analysis of variance (ANOVA) analyses were performed to determine whether the differences in stiction between the wafers were significant. In ANOVA, a calculated F value greater than the critical F value means the results are statistically significant. The ANOVA analyses were performed considering two factors, the differences in stiction between the deposition and annealing conditions and the differences in stiction between beam lengths. The ANOVA was performed both with replicates and without replicates. The replicates were the 6 pairs of wafers processed through similar deposition and annealing conditions. The results of the analyses are shown in Table 5. The results for the analyses done with and without replicates provided a similar result, which was that the differences in stiction between the annealing and deposition conditions were significant while the differences in stiction between the different beam lengths were not significant.

Table 5. ANOVA for All Wafers and Beam Lengths.

ANOVA Analyses	F	F _{crit}	P
All Wafers - 2 Factor without Replication	10.47	1.84	3.90E-15
All Beam Lengths - 2 Factor without Replication	1.25	1.67	0.23
All Wafers - 2 Factor with Replication	7.07	2.48	5.78E-05
All Beam Lengths - 2 Factor with Replication	0.84	1.76	6.40E-01

The stiction data was also analyzed using ANOVA by grouping the wafers by deposition temperature, annealing temperature, and surface roughness. The surface roughness differences were determined by visual observation and were not actually measured. Since they weren't measured, they were grouped into two categories, rough and smooth. The results of this analysis are presented in Table 6. The difference in the amount of stiction between wafers was found to be significant for all of the groups except for the wafers annealed for 3 hours at 1000°C. For this group, the calculated F value of 1.6 was less than the critical F value of 1.74. From this data it could be assumed that the variability was due to the annealing process and not the deposition process. The data in Table 6 also showed that the differences in stiction observed between the different beam lengths for the rough and smooth wafers were not significant.

Table 6. ANOVA for Different Groups of Conditions.

ANOVA Groups	F	Fcrit	P
585°C Deposition Wafers	5.83	2.79	0.00
600°C Deposition Wafers	12.87	2.79	2.231E-06
620°C Deposition Wafers	4.56	2.79	0.01
550°C Anneal Wafers	15.75	2.32	5.963E-11
1000°C Anneal Wafers	1.60	1.74	0.08
Stiction for all beams on smooth wafers	18.17	2.09	2.890E-16
Stiction between different beam lengths on smooth wafers	1.41	1.71	0.14
Stiction for all beams on rough wafers	4.56	2.79	0.01
Stiction between different beam lengths on rough wafers	1.61	1.83	0.10

The statistical analyses showed that there were differences in the observed stiction between all of the wafers, but that there was no difference in the observed stiction between the different beam lengths.

4.3 Capillary Forces

There are two basic mechanisms at work for post release stiction to occur. After the final rinsing process step, water trapped under the beams creates capillary forces which pull the beams to the substrate surface. Once the beams are in contact with the

substrate, one of the other stiction mechanisms such as Van der Waals or hydrogen bridging holds the beams down. One of the primary questions that must be answered in order to analyze the data is whether the capillary forces generated in this investigation were sufficient to pull the beams down to the substrate. This requires a comparison of the forces required to pull the beams down and the capillary forces generated after the final rinsing process.

The equation used for calculating the pull down force on the beams was:

$$p = \frac{v_{\max} 8EI}{L^4} \quad \text{Equation 17}$$

p=Force (N/m)
v=Beam vertical displacement (m)
E=Youngs modulus (N/m²)
I=Moment of inertia (m⁴)
L=Beam length (m)

Equation 17 applies to a uniform load along the entire beam length, which is conservative since the wetting was not uniform. It was conservative since it made the required pull down force higher. From Equation 17 it can be seen that the critical pull down force is dependent on the beam length and the beam moment of inertia. The moment of inertia is dependent on the beam cross-section and will be discussed in Chapter 5. The beam post was assumed to be rigid with no compliance. Since part of the post was etched during the release etch process, the post was not perfectly rigid. This would also add to the conservatism of the force calculation since the stiffness in Equation 17 was higher than the actual stiffness. The critical force vs. beam length is plotted in Figure 28 to show not

only that the force decreases as the beam length increases, but that the critical force is different for the different wafers due to variations in the moment of inertia from wafer to wafer.

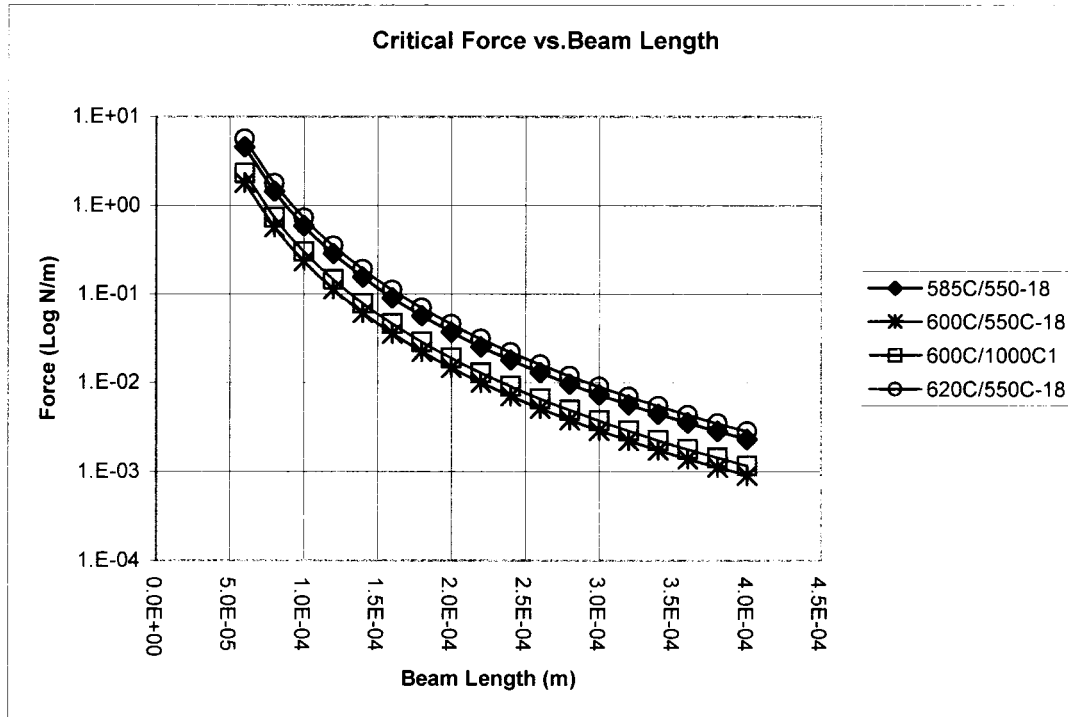


Figure 28. Log of pull down force versus beam length for select wafers calculated using equation 18 and polysilicon and oxide thickness data.

The magnitude of the capillary pressure is dependent on the critical wetting angle, which is determined by the affinity of the substrate and beam surfaces for water. The capillary pressure is also affected by the separation distance between the beam and the substrate. This distance is determined by the sacrificial oxide thickness and polysilicon film stress. Both of these factors will be discussed in Chapter 5. The equation for capillary pressure is:

$$P_c = \frac{2\gamma\cos\theta}{z} \quad \text{Equation 18}$$

P_c =Capillary pressure (N/m²)

γ =Surface tension (N/m)

θ =Critical wetting angle

z =Distance between beam and substrate (m)

The capillary force (N/m) is calculated by multiplying the capillary pressure by the beam width. The variation of the capillary pressure with the separation distance between the beam and substrate calculated from Equation 18 is shown in Figure 29 for a critical wetting angle of 82 degrees. The 82 degrees corresponded to critical wetting angle for hydrophobic surfaces in a previous study[11]. The surface tension of water used was 73mJ/m². The capillary force increases as the separation distance decreases.

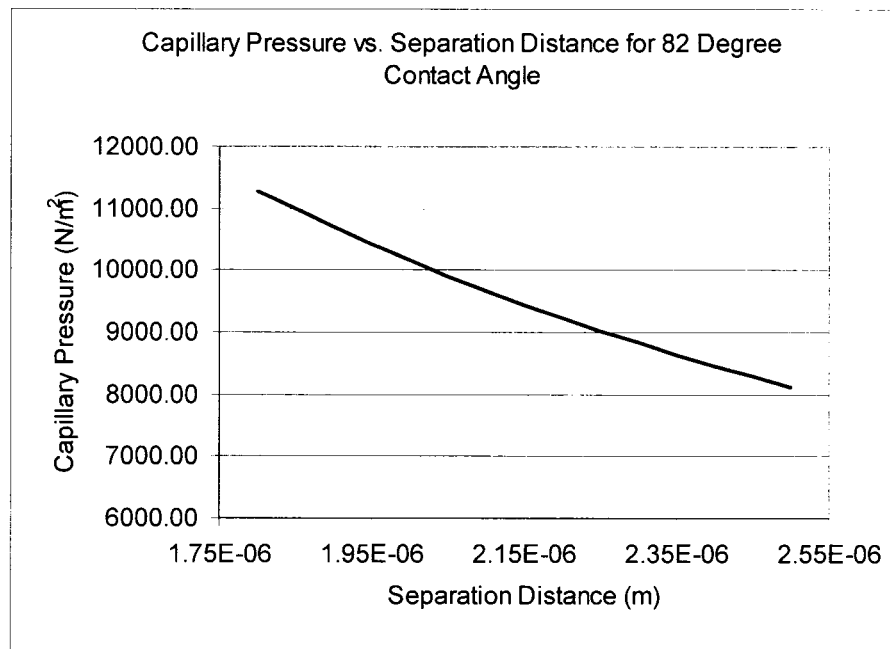


Figure 29. Capillary pressure vs. separation distance.

The results of the comparison of the critical pull down forces and the capillary forces are shown in Table 7. Since the critical pull down force is dependent on both the moment of inertia and the beam length, the results in Table 7 show the shortest beam that could have been pulled down by the capillary forces for each wafer. The calculated shortest stuck beam in the Michalske and de Boer study was 120 μm , which was in the same range as the calculated shortest stuck beam lengths for this investigation which were between 120 and 160 μm . The moment of inertia differences caused variation in the value of the shortest stuck beam length between the wafers.

Table 7. Beam Length and Stiction Energy Data.

Wafer	Calculated Shortest Stuck Beam due to Capillary Forces(μm)	Shortest Observed Stuck Beam (μm)	Polysilicon Thickness (m)	Height Above Substrate (m)	Stiction Energy $\gamma_s(\text{mJ}/\text{m}^2)$
585°C/550°C-12hr	140	none	2.26E-06	2.03E-06	0.00
585°C/550°C-18hr	140	none	2.37E-06	2.09E-06	0.00
585°C/1000°C1	140	180	2.23E-06	1.99E-06	2.60
585°C/1000°C2	140	160	2.22E-06	2.02E-06	4.24
600°C/550°C-12hr	120	100	1.87E-06	2.09E-06	17.78
600°C/550°C-18hr	120	120	1.74E-06	2.09E-06	6.91
600°C/1000°C1	120	240	1.89E-06	2.15E-06	0.59
600°C/1000°C2	120	80	1.88E-06	2.14E-06	46.25
620°C/550°C-18hr	140	160	2.54E-06	2.12E-06	7.00
620°C/550°C-12hr	140	140	2.54E-06	2.19E-06	12.74
620°C/1000°C1	140	220	2.50E-06	2.11E-06	1.85
620°C/1000°C2	160	140	2.60E-06	2.08E-06	12.32

Several of the wafers had beams that were stuck in a “roller coaster” shape with the middle of the beam stuck to the substrate and the tip curling upward as shown in Figure 30. This indicated a strong capillary attraction to pull the middle of the beam down. Beams that were under high enough tensile stresses had tips that were above the substrate enough to not allow meniscus formation and thus could not be pulled down by capillary attraction.

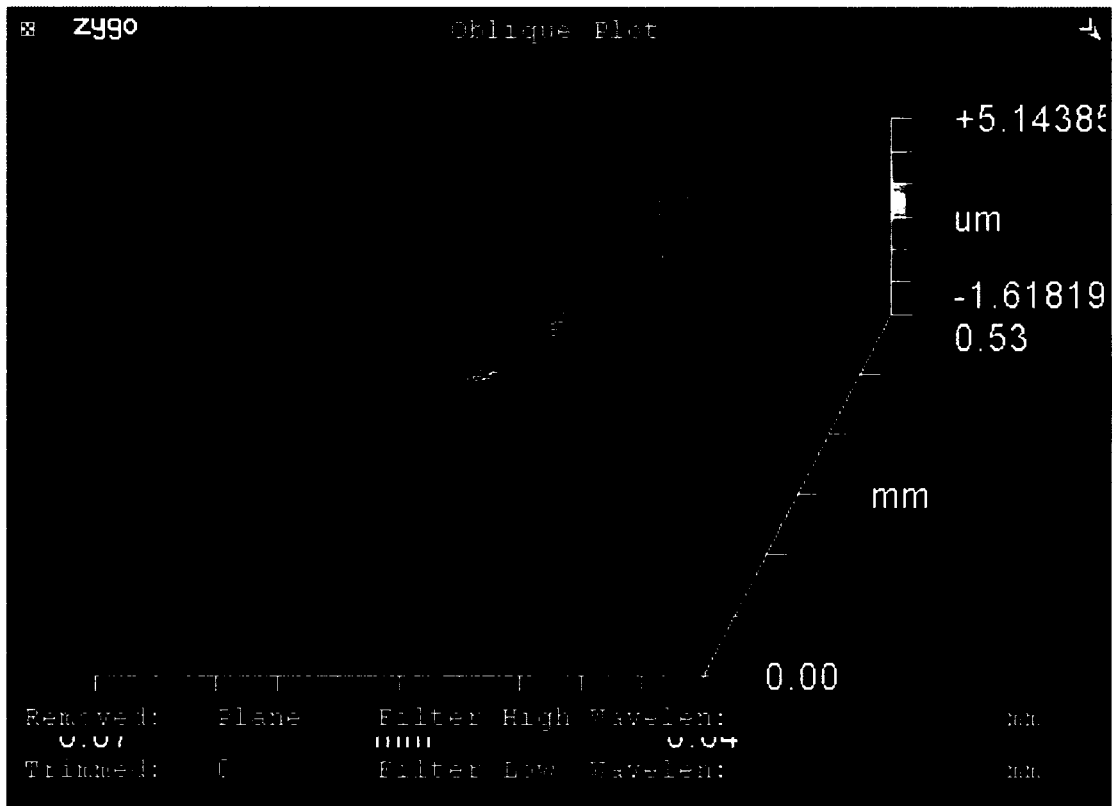


Figure 30. Roller coaster beam on 600°C wafer.

So in this section it was determined that the capillary forces generated by the water from the final rinsing process were large enough to pull beams to the substrate. The shortest beam lengths were not the same for all of the wafers due to variations in the oxide and polysilicon film thicknesses, which affected the moment of inertia and the separation between the beams and the substrate. The thickness variations will be discussed in Chapter 5.

4.4 Stiction Energy

As mentioned previously, the stiction process observed in this investigation consisted of two components. The first was the capillary forces from water left after the rinsing process, which initially pulled beams down to the substrate. The shortest beams that could be pulled down by the capillary forces generated during this investigation for each wafer are presented in Table 7. The second component was the stiction force present after the wafers had completely dried. Not all of the beams pulled down by the capillary forces would remain stuck after drying. All of the wafers were examined at least twice during the nine to eleven day drying time. Beams with a high enough restoring force could break free as was witnessed during the wafer inspections.

The study by Legtenberg *et al*[6] compared calculated stiction energy with estimated stiction energies for the different stiction mechanisms. The stiction energies for this investigation were calculated using the following equation:

$$\gamma_s = \frac{3}{8} \left(\frac{Et^3h^2}{L^4} \right) \quad \text{Equation 19}$$

γ_s =Stiction energy (J/m²)

L=Beam length (m)

t=Beam thickness (m)

h=Beam height above substrate (m)

This is the equation that was used in the de Boer and Michalske study. It applied to arc-shaped stuck beams and was used in this experiment because the experimental beams were primarily stuck in the arc-shape with a small number stuck in the s-shape or roller coaster shape. Since there was not a clear transition between unstuck and stuck beam lengths as previously mentioned, the shortest stuck beam for each wafer was used to calculate the stiction energies. The calculated stiction energies are presented in Table 8. The calculated stiction energies were smaller than the energies from the Legtenberg study for hydrophobic surfaces. The Legtenberg values for hydrophobic silicon were between 40 and 100 mJ/m². This range was consistent with the bonding energy associated with Van der Waals forces. The values for this investigation were between 1.85 and 46.25 mJ/m². The differences in the stiction energy values could have been due to the fact that Legtenberg study was based on beams fixed at both ends and that they used two different treatments to get hydrophobic surfaces.

Table 8. Summary Table of Different Factors vs. Percentage of Stuck Beams.

Dep Temp	Annealing Condition	Observed Roughness	Film Stress (Mpa)	Average Polysilicon Thickness (A)	Average Oxide Thickness (A)	Shortest Stuck Beam (μm)	Grain Size (nm)	Texture	% Stuck Beams
585C	550C-12hr 1000C-1.75hr	Smooth	72.57	23662	20953	na	300	{111}	0.0
585C	550C-18hr 1000C-2hr	Smooth		22598	20256	na	220	{111}	0.0
585C	1000C-3hr	Smooth	-9.18*	22268	19860	220	180	{311}	2.4
585C	1000C-3hr	Smooth	-9.18*	22194	20200	160	180	{311}	2.7
600C	550C-18hr 1000C-1.5hr	Smooth	-34.1	17367	20867	120	240	{111}	16.0
600C	550C-12hr 1000C-2hr	Smooth		18694	20865	100	200	{111}	5.0
600C	1000C-3hr	Smooth	6.8*	18874	21548	240	150	{110}	2.7
600C	1000C-3hr	Smooth	6.8*	18828	21394	80	150	{110}	6.1
620C	550C-18hr 1000C-1.75hr	Rough	-13.2	25350	21176	160	60	{110}	9.8
620C	550C-12hr 1000C-2hr	Rough		25400	21879	140	40	{110}	3.7
620C	1000C-3hr	Rough	-3.5*	24960	21117	220	30	{110}	3.0
620C	1000C-3hr	Rough	-3.5*	25900	20802	140	30	{110}	3.7

4.5 Summary

The low number of stuck beams observed in this investigation could be attributed to the fact that all of the wafers were hydrophobic after processing. The wetting was not uniform over the surface of the wafers so the capillary forces were also not uniform. The stiction and ANOVA data showed that there was a difference between the stiction observed for the different deposition and annealing conditions. The ANOVA analysis showed that the wafers with films deposited at 580°C, 600°C, and 620°C that were annealed at 1000°C for 3 hours were not significantly different.

The capillary force generated by water trapped under the beams was sufficient to pull beams down to the substrate. However, the degree of wetting was not uniform so the capillary forces were not uniform. For this reason there was not a clear transition between the unstuck and stuck beams or between the arc and s-shaped stuck beams.

The stiction energies calculated from the data were less than the values from the literature. The stiction energies indicate that Van der Waals forces could be holding the beams down.

There were several thin film properties that could explain the differences in stiction observed. These properties are:

1. Surface Roughness
2. Film Stress
3. Polysilicon and Oxide Film Thicknesses
4. Film Grain Size and Texture

With the exception of beam length, the deposition and annealing temperatures affected all of these factors. These factors are discussed in the following chapter along with their impact on stiction. A summary of each of these factors is presented in Table 8. Stress values were not taken for all of the wafers. The stress values marked with an asterisk were taken from a representative test sample.

CHAPTER 5

THIN FILM PROPERTIES

5.1 Surface Roughness

The surfaces of the amorphous and semi-amorphous silicon thin films deposited at 585°C and 600°C were different than the polysilicon thin films deposited at 620°C even after annealing, as observed visually. The 585°C and 600°C films were highly reflective while the 620°C film was opaque with a light purple color. When examined with an optical microscope, the surfaces of the 585°C and 600°C films appeared smooth, while the surfaces of the 620°C films appeared rougher. This was consistent with work done by Bisaro, Magarino and Proust where they found that amorphous and semi-amorphous LPCVD films were smoother than fully crystalline LPCVD films[18]. This can also be seen in Figure 31, which shows SEM images from this experiment of an annealed 620°C film and an annealed 600°C film.

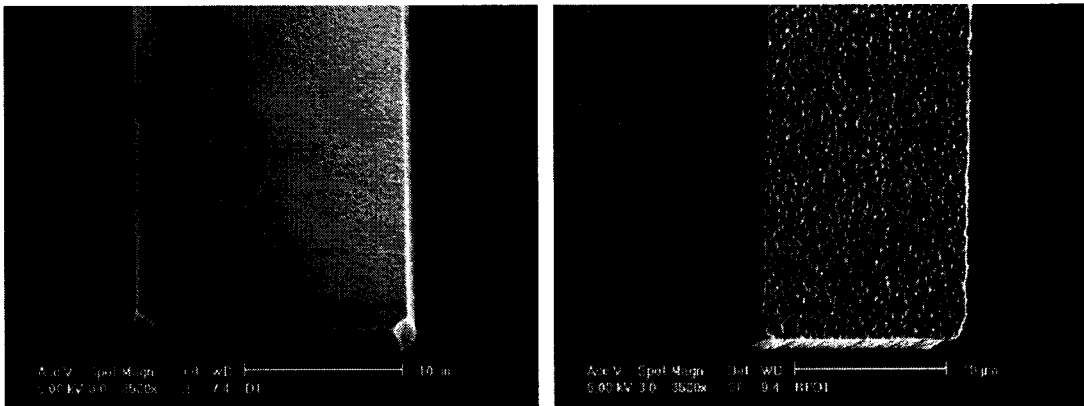


Figure 31. Comparison of surface for polysilicon surfaces from annealed amorphous, left, and annealed polysilicon, right.

In the study by Komvopoulos and Yan[5] it was concluded that the critical pull-off stiffness increased with decreasing surface roughness as was shown in Figure 7[5]. The critical pull-off stiffness was the amount of restoring force required to pull a stuck beam free. This was because the surface roughness affects the capillary force. As the surface roughness increases, the actual contact area between the beam and substrate decreases. The magnitude of the capillary force decreases with decreasing contact area. Therefore, the capillary force should be higher for the smoother surface due to the increased contact area, leading to more stiction. It is important to note that the affinity of the substrate and polysilicon for water also affects the capillary force since it determines the critical wetting angle of the water. The more hydrophilic that the surfaces are, the smaller the critical angle and the greater the capillary force, leading to more stiction.

The amounts of etch debris also was observed to be greater for the smoother surfaces. This is most likely due to the increased amount of contact area between the larger pieces of debris and the film surfaces. The increased contact area translates to higher capillary attraction forces, which hold the debris in place during the rinsing processes. The observations were made during the etch process where the wafers were removed at periodic time intervals to assess whether the beams were released. The debris was also observed during the interferometer inspections after the wafers were dry. The etch debris consisted of the silicon dioxide sacrificial layer and some of the smaller polysilicon features that were etched away during the release etch process. The etch debris can collect at the tips of beams that have been pulled down to the substrate and create a solid bridge that holds the beams down after drying. This stiction mechanism

was discussed in the Legtenberg *et al.* study[6], but was not observed during their experiment.

Even though the data in this experiment did not show a trend between visually observed surface roughness and stiction, it has been shown in the literature that surface roughness does affect stiction. The actual surface roughness was not measured so there may have been subtle differences that were not apparent from visual inspection. Also, since there are several different mechanisms at work besides surface roughness, the effect of roughness may have been masked by a more dominant mechanism. However, based on the findings in the literature, rougher surfaces are not as susceptible to stiction due to the lower amount of surface contact.

5.2 Polysilicon Film Stress

The polysilicon thin film stress played an important role in the presence of stiction. The wafers with amorphous films deposited at 585°C and annealed at 550°C/1000°C (A1 and AT) did not have any stuck beams after the nine to eleven day drying time. During intermediate inspections, the AT wafer did have some stuck beams. The stress data for the AT wafer showed that it had a tensile stress of 72.57MPa in the unpatterned film. If this stress remained in the patterned beams, it would have caused the beams to curl up slightly. However, during the interferometer examination, the beams were found to be basically straight as shown in Figure 32. The beam shown in Figure 32 is a 240µm beam that does not curve up or down. The beams on an unannealed test wafer with polysilicon deposited at 620°C are shown in Figure 33. The beams shown in Figure

33 were 220 μm and 240 μm . The 240 μm beam is slightly curved up and 220 μm beam is noticeably curved up which indicates that polysilicon was under tensile stress.

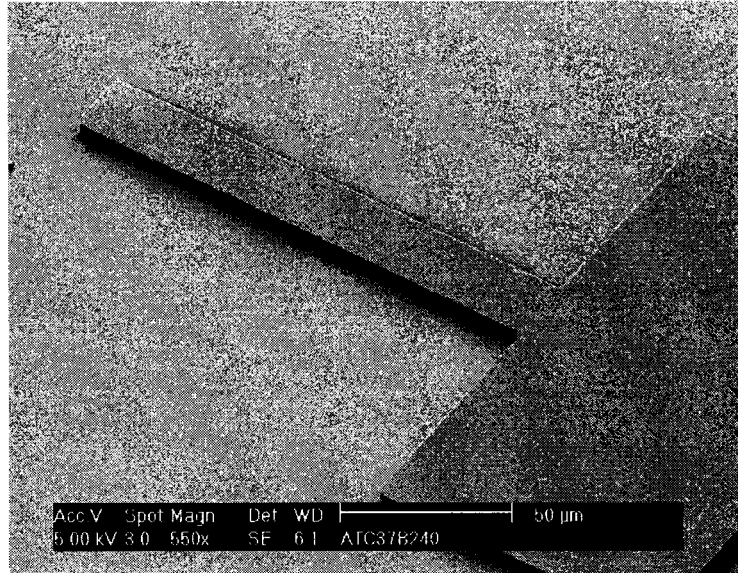


Figure 32. SEM image of 240 μm beam from wafer with amorphous silicon deposited at 585 $^{\circ}\text{C}$ and annealed for 18 hours at 550 $^{\circ}\text{C}$ followed by 1.75 hours at 1000 $^{\circ}\text{C}$.



Figure 33. SEM image of 220 μm and 240 μm beam from wafer with polysilicon deposited at 620 $^{\circ}\text{C}$ with no annealing.

The stress measurements that were taken after annealing and before patterning and etching the polysilicon did not cover the entire surface of the wafer. The laser mapped the wafer at 30 degree intervals and then estimated the stresses of the sections in between the scanned lines. Even though the stress varies across the wafer from tensile to compressive, the overall stress was tensile. The stress of the A1 wafer was not measured, but the beams across the entire wafer were curved up indicating high tensile stresses. The stress on the wafer with semi-amorphous silicon deposited at 600°C and annealed for 18 hours at 550°C and 1.75 hours at 1000°C (CT) had a compressive stress of -34.2 MPa. The stress on the wafer with the polysilicon deposited at 620°C and annealed for 18 hours at 550°C and 1.75 hours at 1000°C (ET) had a compressive stress of -13.2 MPa. The compressive stresses may have contributed to the higher number of stuck beams found on these two wafers.

Stress observation taken from the Zygo interferometer inspection of the patterned and released beams were compared to the SMSi3800 stress data for the unpatterned film as shown in Table 9. One of the beam groups on each wafer was examined to determine whether the beams were curved up or down. Beams that were curved up were considered to be under tensile stress and beams that curved down were considered to be under compressive stress. These observations were noted in Table 9. The stress observations in Table 9 were often not in agreement with the measured stresses. This was most likely due the fact that the SMSi3800 stress values were taken before the beams were patterned and etched. The Zygo interferometer observations were taken on released beams. The overall polysilicon film stress is composed of two components, intrinsic stress and

extrinsic stress. The extrinsic stresses are mostly caused by mismatches in the coefficient of thermal expansion between the substrate, oxide and polysilicon layers.

Table 9. Stress Observations from Zygo vs. Actual Stress Measurements.

Wafer	Base Height (μm)	Tip Height (μm)	Stress from Zygo Interferometer	Measured Stress (MPa) compressive (-)	%Stuck
585°C/550°C-12hr	3.75	3.94	Tensile		0.0
585°C/550°C-18hr	3.96	3.85	Compressive	72.57	0.0
585°C/1000°C-1	3.95	3.9	Compressive	-9.18	2.4
585°C/1000°C-2	3.89	4.17	Tensile	-9.18	2.7
600°C/550°C-12hr	3.56	4.07	Tensile		5.0
600°C/550°C-18hr	3.65	3.83	Tensile	-34.10	16.0
600°C/1000°C-1	3.61	3.63	Tensile	6.80	2.7
600°C/1000°C-2	3.69	3.86	Tensile	6.80	6.1
620°C/550°C-12hr	4.35	3.88	Compressive		3.7
620°C/550°C-18hr	4.28	3.86	Compressive	-13.20	9.8
620°C/1000°C-1	4.26	3.97	Compressive	-3.50	3.0
620°C/1000°C-2	4.31	4.07	Compressive	-3.50	3.7

The intrinsic stresses are due to the internal properties of the films. The SMSi3800 measured the wafer curvature, which was converted to overall stresses. Prior to the patterning and etching of the beams, the curvature of the substrate is due to both the extrinsic and intrinsic stresses. After the beam patterning and etching processes, the oxide and polysilicon films are no longer continuous across the substrate so the extrinsic

stresses should be reduced. The oxide under the beams is also removed so the stresses in the beams are no longer affected by coefficient of thermal expansion mismatches between the oxide and the polysilicon. Therefore, the stresses observed in the released beams were due to the intrinsic stresses of the polysilicon film. The intrinsic film stress was influenced by the oxide and substrate because these had a part in determining the lattice mismatches encountered during the silicon film growth. Annealing alleviated the mismatch by providing the silicon atoms with the energy to rearrange to better match the oxide.

There was no correlation between the stresses measured before and after beam patterning to the percentage of observed stiction. The stresses could impact stiction by causing the beams to curve up or down. Beams that curved down would appear to be stuck and beams that curved up would not allow the meniscus formation under the beams that is necessary for capillary attraction. With the exception of the beam annealed at 550°C for 12 hours followed by annealing at 1000°C for 2 hours, all of the beams examined with the Zygo appeared to be straight.

5.3 Polysilicon and Oxide Film Thicknesses

The thicknesses of the polysilicon and oxide thin films that defined the beam dimensions were not fixed. There were variations between runs and between the different deposition temperatures. The average thickness data is presented in Table 10. Thickness data was taken in 5 places on each wafer after the films were deposited and

prior to annealing. The thickness values in the Table 10 are averages of the 5 measurements except for the wafer with 600°C semi-amorphous silicon annealed for 18 hours at 550°C followed by 1.5 hours at 1000°C. The film thickness on this wafer was measured using a profilometer after the beams had been patterned, etched, and released. For this reason the thickness data from this wafer cannot be compared to the other wafers. The difference in thickness between this wafer and the other 600°C wafers was most likely due to contraction of the film during annealing when the silicon atoms rearranged from the partially amorphous structure to the fully crystalline structure.

Table 10. Oxide and Amorphous/Polysilicon Thickness.

Wafer	LTO _{AVE} (Å)	Amor/Poly _{AVE} (Å)
585C Amorphous-12hr 550C Anneal	20256	22598
585C Amorphous-18hr 550C Anneal	20953	23662
585C Amorphous-3 hr 1000C Anneal	19860	22268
585C Amorphous-3 hr 1000C Anneal	20200	22194
600C Semi-Amorphous- 12hr 550C Anneal	20865	18694
600C Semi-Amorphous- 18hr 550C Anneal	20867	17367*
600C Amorphous-3hr 1000C Anneal	21548	18874
600C Amorphous-3hr 1000C Anneal	21394	18828
620C Polysilicon-12hr 550C Anneal	21879	25400
620C Polysilicon-18hr 550C Anneal	21176	25350
620C Polysilicon-3hr 1000C Anneal	21117	24960
620C Polysilicon-3hr 1000C Anneal	20802	25900
*thickness measured after annealing,		

ANOVA analyses were performed on the polysilicon and oxide thickness measurements to determine whether the thickness variations were significant. The results for the oxide thickness measurement are presented in Table 11. The calculated F-value of 1.50 was below the critical value of 1.99, which indicates that there were not significant oxide thickness variations between the wafers.

Table 11. ANOVA Results for Oxide Thicknesses.

ANOVA for Oxide Thickness				
Source of Variation	Degrees of Freedom	F	P-value	F crit
Between Groups	11	1.496	0.164	1.995
Within Groups	48			
Total	59			

The amorphous and polysilicon thicknesses were also analyzed using ANOVA. The results are presented in Table 12. The analysis shows that there were significant variations in the amorphous and polysilicon thicknesses from wafer to wafer. This was expected since the three different deposition temperatures of 585°C, 600°C, and 620°C had different deposition rates. The measurements for the 600°C wafer annealed for 18 hours at 550°C were not included in the analysis since they were not taken at the same point in the manufacturing process as the other wafers. When the amorphous and polysilicon wafers were compared within their deposition temperature groups, the results were more uniform. The results of the ANOVA for the 620°C polysilicon wafers indicate that the variation of the thicknesses between the wafers was not significant. The results of the ANOVA for the 585°C amorphous and 600°C semi-amorphous silicon

wafers indicate that there were significant thickness variations between the wafers.

When the thickness data for wafers for both the 585°C and 600°C that were annealed for 18 hours at 550°C were removed, the thickness variation between the remaining wafers was not significant.

Table 12. ANOVA Results for Amorphous and Polysilicon Thicknesses.

Wafer Group	F	Fcrit
All Wafers	367.899	2.216
620°C Polysilicon	2.970	4.066
600°C Semi-Amorphous Silicon	67.461	4.066
600°C Semi-Amorphous Silicon without Wafer Annealed at 550°C for 18 Hours	3.155	3.885
585°C Amorphous Silicon	14.265	3.239
585°C Amorphous Silicon without Wafer Annealed at 550°C for 18 Hours	2.395	3.885

The polysilicon film thickness impacts the stiffness of the beams. The stiffness of the beam is determined by the moment of inertia, which is related to the shape of the cross section of the beam. The equation for the moment of inertia for a rectangular cross section of the beams used in this experiment is shown below:

$$I = \frac{bh^3}{12} \quad \text{Equation 20}$$

I=Moment of inertia (m⁴)

b=Beam width (m)

h=Beam thickness (m)

The moment of inertia versus the percentage of stuck beams for each wafer is shown in Table 13. The width of the beams was considered constant and the variations in the moment of inertia were caused by variations in the beam thickness. The thinner the polysilicon film, the lower the moment of inertia.

Table 13. Moment of Inertia vs. Percentage of Beams Stuck.

Wafer	Beam Width (m)	Polysilicon Thickness (m)	Moment of Inertia (m⁴)	%Beams Stuck
600C/550C-18hr	2.00E-05	1.74E-06	8.73E-24	15.9
600C/550C-12hr	2.00E-05	1.87E-06	1.09E-23	5.0
600C/1000C2	2.00E-05	1.88E-06	1.11E-23	6.1
600C/1000C1	2.00E-05	1.89E-06	1.12E-23	2.7
585C/1000C2	2.00E-05	2.22E-06	1.82E-23	2.7
585C/1000C1	2.00E-05	2.23E-06	1.84E-23	2.4
585C/550C-12hr	2.00E-05	2.26E-06	1.92E-23	0.0
585C/550C-18hr	2.00E-05	2.37E-06	2.21E-23	0.0
620C/1000C1	2.00E-05	2.50E-06	2.59E-23	2.9
620C/550C-18hr	2.00E-05	2.54E-06	2.72E-23	9.8
620C/550C-12hr	2.00E-05	2.54E-06	2.73E-23	3.7
620C/1000C2	2.00E-05	2.59E-06	2.90E-23	3.7

The moment of inertia was used to calculate the amount of force required to pull a beam down to the substrate. The lowest pull down force was for the beams on the wafer with polysilicon deposited at 600°C and annealed at 550°C for 18 hours. The data presented in Table 13 shows that this wafer had the lowest moment of inertia and the highest percentage of stuck beams. There does not appear to be a trend, however, since the wafer

with the polysilicon deposited at 620°C and annealed at 550°C for 18 hours had the second highest percentage of stuck beams and the third highest moment of inertia.

5.4 Grain Size and Texture

Even though the grain sizes and textures for the wafers were not directly measured, differences were predicted based on the literature. During the incremental annealing processes, the wafer stress changes indicated that the film morphologies had changed. This was particularly true for the 585°C and 600°C silicon films that were annealed at 550°C. The stress history for the wafer with amorphous silicon deposited at 585°C and annealed for 18 hours at 550°C followed by 1.75 hours at 1000°C, Figure 19, shows a dramatic increase in stress during the incremental annealing process. As previously mentioned, the amorphous films experience an increase in the tensile stress due to the ordering of the silicon atoms from amorphous to crystalline structure. The reduction of the tensile stress seen later was due to grain growth and continued atomic reordering. The order of largest to smallest grain size as estimated from the literature and the deposition and annealing conditions is shown in Table 14. The grain size and texture estimates were based on references [11,12]. The 550°C anneal was done to get larger grain sizes, especially in the 585°C and 600°C films, however, it is not clear how the 1000°C annealing step after the 18 and 12 hour annealing steps at 550°C affected the final grain size. The transformation from amorphous to polycrystalline films involves the nucleation of new grains and then the growth of those grains. In order to get larger grained films, the energy provided by the annealing process should favor grain growth. It

is not clear whether the 1000°C step promoted a high degree of nucleation that would have created a smaller grain structure. The 620°C films were estimated to have the smallest grain sizes due to the fact that those 620°C films were already polycrystalline so there would be more grains growing during annealing. Since more grains were growing, they would impinge upon one another limiting growth. The 620°C films with the 550°C annealing step were estimated to have slightly larger average grain sizes due to the lower amount of energy available for nucleation and the possibility that the larger grains in the as-deposited film experienced greater growth.

Table 14. Grain Size and Texture Estimates.

Wafer	Grain Size	Texture	% Beams Stuck
585°C Dep 550°C Ann 18hrs	300nm [11]	<111> [6]	0.0
600°C Dep 550°C Ann 18hrs	240nm [11]	<111> [6]	15.9
585°C Dep 550°C Ann 12hrs	220nm [11]	<111> [6]	0.0
600°C Dep 550°C Ann 12hrs	200nm [11]	<111> [6]	5.0
585°C Dep 1000°C Ann 3hrs	180nm [11]	<311> [12]	2.4
585°C Dep 1000°C Ann 3hrs	180nm [11]	<311> [12]	2.6
600°C Dep 1000°C Ann 3hrs	150nm [11]	<110> [12]	2.6
600°C Dep 1000°C Ann 3hrs	150nm [11]	<110> [12]	6.1
620°C Dep 550°C Ann 18hrs	60nm	<110> [12]	9.8
620°C Dep 550°C Ann 12hrs	40nm	<110> [12]	3.7
620°C Dep 1000°C Ann 3hrs	30nm [11]	<110> [12]	3.7
620°C Dep 1000°C Ann 3hrs	30nm [11]	<110> [12]	2.9

The experimental hypothesis was for the wafers with smaller grained polysilicon films to experience higher instances of stuck beams. This is because smaller grained films have more grain boundaries, which leads to higher surface energies. Polysilicon thin films with higher surface energies are more likely to stick, to lower the overall system surface energy. The films that were predominantly $\{110\}$ texture, the close packed plane for the diamond cubic crystal structure, should have had the lowest percentage of stuck beams due to the smallest number of broken bonds exposed on the film surface. The data presented in Table 15 did not show a definite relationship between the grain size and texture of the polysilicon beams and beam stiction. The wafer with the highest degree of stiction was estimated to have the $\{111\}$ texture and the second largest grain size.

The fact that the experimental results did not agree with the experimental hypothesis could have been due to the cumulative impact that the other factors had on stiction as well as the fact that the grain size and texture were not determined experimentally for any of the samples.

CHAPTER 6

CONCLUSION and RECOMMENDATIONS

6.1 Conclusion

The differences in the amount of stiction observed between wafers were statistically significant. The exact cause of the observed difference was difficult to determine since there were several factors that could have contributed to the differences observed. The surface roughness, film stress, film thickness variation, affinity for water, grain size, and preferred texture were all factors. The variation in beam length was not a factor in the observed degree of stiction.

6.2 Recommendations

In order to effectively compare stiction between wafers, the film thicknesses should be controlled as tightly as possible. A recommendation for future experiments of this type is to characterize the deposition process carefully and then run the deposition on more than 20 wafers during the same run. Hopefully the variability in thickness would be a minimum. If not, then there would be enough wafers to assemble subsets in the same thickness range. The film thickness should be measured on all wafers in a minimum of 5 places.

Several test wafers should be used to establish the low temperature (550-600°C) annealing process. Wafer stress measurements should be taken at three-hour increments to adequately observe the stress histories. It may also be helpful to include features on the mask that can be used to evaluate the intrinsic film stress.

The wafer surfaces should be treated to make them hydrophobic and hydrophilic. This would enhance the repeatability by providing more uniform surface properties.

In order to make the experiment manageable, only one polysilicon deposition temperature and two annealing temperatures should be evaluated. If the work is being done in the Stanford University lab, the 585°C deposition temperature is recommended since the process produces good repeatability with respect to the film thickness.

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