Growth of High Quality $Si_{0.75}Ge_{0.25}$ alloy layers using various types of buffer layers

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Despite of low cost, abundant in nature, process simplicity and prospect of bandgap engineering, SiGe is still away from its full-fledged usages. To realize the utilization of SiGe, strain relaxed and smooth alloy layers is required. In our previous research, we have shown that short-period $(Si_m/Ge_n)_N$ superlattices with various steps are effective to reduce the surface roughness and strain. For device fabrication, the thinner buffer layer will be better. So, we have concentrated our attention to get effective and thinner buffer layers, and care has been given to grow the buffer in easier way, which will lead lower cost and minimum time for fabrication.

We have used Si(001) wafer as a substrate for the growth of various epitaxial layers. The substrates were cleaned following standard chemical cleaning process before introducing them into the growth chambers. The samples were grown in ultra high vacuum environment by molecular beam epitaxy (MBE) process. Compositions of the samples were determined by XPS. The residual strain in the grown layers were estimated from the XRD data. Surface morphology and the nature of dislocations and interfaces were observed by AFM and cross-sectional transmission electron microscopy (XTEM), respectively.

From on going research, some results have been presented bellow:

[1]. Growth of $Si_{0.75}Ge_{0.25}$ alloy using H^+ exposed $(Si_{14}/Ge_1)_{20}$ superlattices

In this experiment, 2000-Å-thick $Si_{0.75}Ge_{0.25}$ alloy layers have been gown on Si(001) using short-period $(Si_{14}/Ge_1)_{20}$ superlattice (SSL) buffers with H^+ exposure. During the growth of buffer layers a constant flow of H^+ (K-cell temperature of H was 1200°C) was maintained. Buffer layers were grown at different temperatures from 300-400°C, and the $Si_{0.75}Ge_{0.25}$ alloy layers were grown at 500°C on each buffer layer. From XRD data, it has been seen that the residual strain of the alloy layers increases with decreasing of the growth temperature of the buffer layer and reaches to a lower value of about –0.02% at 350°C (Fig.1). At this temperature, the surface nobilities of the mono-layerly deposited Si and Ge atoms may become lower. Probably, they can form abrupt superlattice layers. Dislocations originated from the substrate/SSL interface can be deflected or filtered by the SSL layers. As a result, the top alloy layer becomes relaxed with less dislocation densities. AFM images also support this observation.

The AFM images of the samples showed island like patterns instead of cross-hatch pattern (Fig.2). The root-mean-square (rms) roughness estimated from the AFM images show a decreasing trend with decreasing of the growth temperature of SSL buffer layers (Fig. 3). This result matches with residual strain shown in Fig. 1.

The nature of dislocations and the interfaces of the grown layers were observed by cross sectional transmission electron microscopy (XTEM). The micrographs of the sample with 350°C grown buffer layer is shown in Fig. 4. Very dense nucleated dislocation sites are seen in the SSL buffer and substrate regions.

Works to be done: We could not precisely control the H^+ flux. H^+ flux will have some effect on the depositions. Changing the flow of H, the effect of the H^+ exposure during the growth of buffer layers on the top alloy layers can be observed. Furthermore, to understand the relaxation process more clearly, we need more TEM experiments.

[2]. Growth of $Si_{0.75}Ge_{0.25}$ alloy using $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ SSL buffers

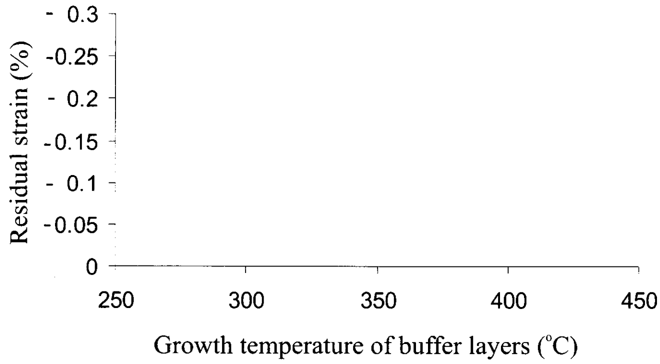
In this research, 2500-Å-thick $Si_{0.75}Ge_{0.25}$ alloy layers have been grown on the same type of substrates using short-period $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ superlattices (SSLs) as buffers. In the SSL layers, first a layer of 14 monolayers (MLs) of Si (thickness ~20Å) followed by a thin layer of $Si_{0.75}Ge_{0.25}$ (thickness 5-6Å) were grown. These Si and $Si_{0.75}Ge_{0.25}$ were repeated for 20 times. The alloy layer showed smooth surface (rms roughness ~12Å)(Fig. 6) and low residual strain (~-0.16%)(Fig. 7) for the 300°C-grown-SSL buffer. Low temperature growth of SSL layers can introduce point defects sites and low temperature growth of $Si_{0.75}Ge_{0.25}$ in SSL layer reduces the Ge segregation length, which lead to a strained SSL layer formation. Strained layers are capable to make barrier for the propagation of threading dislocations and point defect sites can trap the dislocations. This type of buffer is easier to grow and reveals high quality top alloy surface.

Works to be done: It will be needed to perform more research on this type of buffer layers. Changing the growth temperature range of the buffer layers and changing the thickness of the upper alloy layers from 2500 to 2000Å, the effect of the buffer on the alloy layers can be more clearly observed. Residual strain distribution can be understood by XRD rocking curve. Recently, VBL has received such advanced x-ray diffractometer. XTEM and plane view TEM images are necessary to comment on the internal dislocation distribution. To see the abruptness in in SSL layers, energy filtered high resolution XTEM can be used.

[3]. Growth of $Si_{0.75}Ge_{0.25}$ alloy using Sb mediated LT-Si buffer layers

In this experiment, 2000-Å-thick $Si_{0.75}Ge_{0.25}$ alloy layers have been grown using Sb mediated LT-Si buffer layers. In other experiments, we have deposited 1000-Å pre-Si compensating layer on the chemically cleaned and annealed Si substrate. But here, we have grown various layers with and without pre-Si layers and have compared the effects on surface roughness and residual strain. A very thin layer of Sb (~3/4 MLs) was grown at 200°C following a desorption for 10 min at 550°C. A very thin (~2/3 MLs) Ge layer was then grown at 300°C to provide a controlled rough surface, which may create extra point defect sites in the buffer layers. Then about 400-Å-Si buffer layers (LT-Si) were grown at different temperatures from 300-400°C. The upper alloy layers were grown at 500°C as like as other experiments. Residual strain of the samples has been estimated from the XDR data and is shown in Fig. 8 as a function of the growth temperature of the LT-Si buffer layers. Surface morphology has been observed by AFM and the rms roughness is shown in Fig. 9 as function of the growth temperature of the buffers.

Work to be done: There are many questions remain unsettled. Now, samples without Ge are being grown. TEM image of various samples will be taken to understand the relaxation process.



Fi g. 1. Residual strain of the $Si_{0.75}Ge_{0.25}$ alloy layers as a function of the growth temperature of the SSL buffer with H^+ exposure.

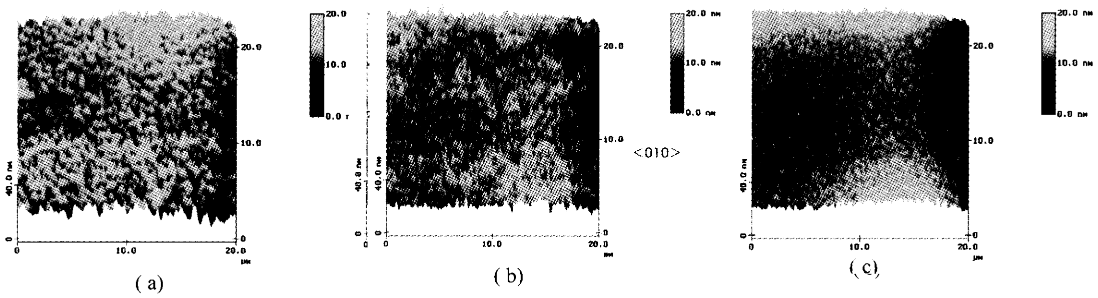
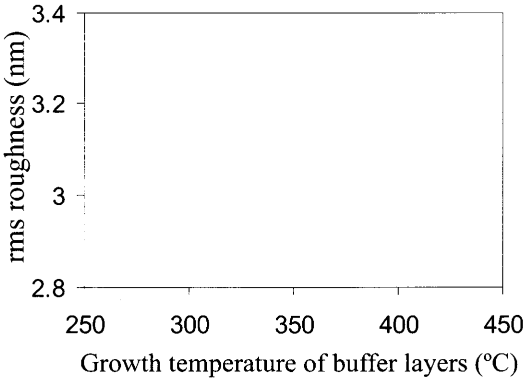


Fig. 2. AFM images (20 μm x 20 μ m) of the $Si_{0.75}Ge_{0.25}$ alloy layers, where buffer layers were grown at (a) 400°C, (b) 350°C and (c) 300°C.



Fi g. 3. The rms roughness of the $Si_{0.75}Ge_{0.25}$ alloy layers as a function of the growth temperature of the SSL buffer with H^+ exposure.

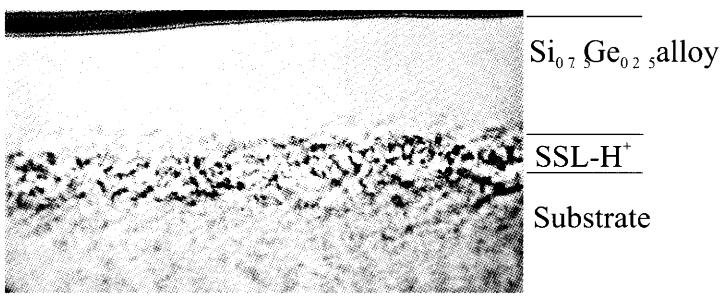
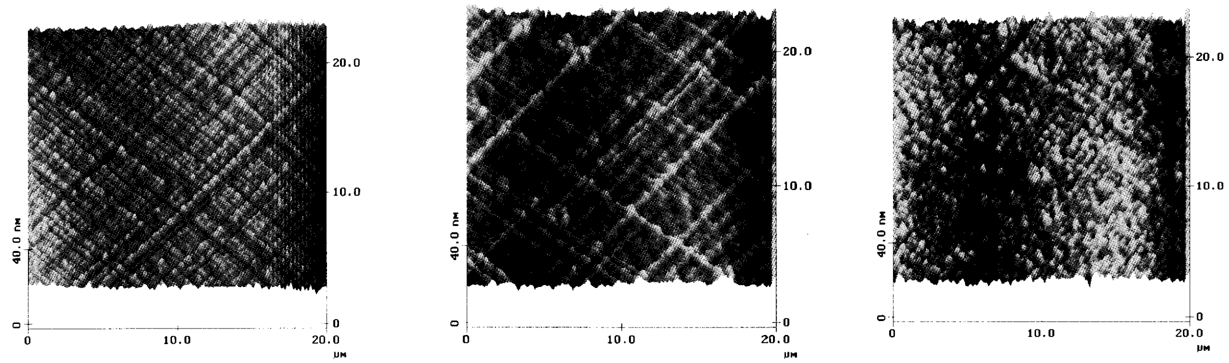


Fig. 4. Cross sectional transmission electron microscopy imageof the sample with SSL buffer layer grown at 350°C with H^+ exposure.



(a) T_B-400°C (b) T_B-350°C (c) T_B-300°C

Fig. 5. AFM images (20 µm x 20 µ m) of the samples with $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ SSL buffers, where buffer layers were grown at (a) 400°C, (b) 350°C and (c) 300°C.

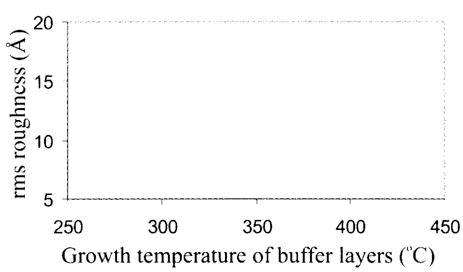


Fig.6. rms roughness of the samples with the $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ alloy layers as a function of the growth temperature of the buffer layers

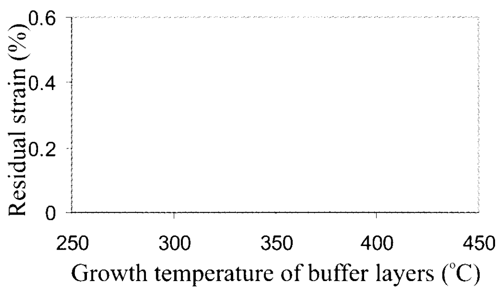


Fig.7. Residual strain of the samples with the $(Si_{14}/Si_{0.75}Ge_{0.25})_{20}$ alloy layers as a function of the growth temperature of the buffer layers

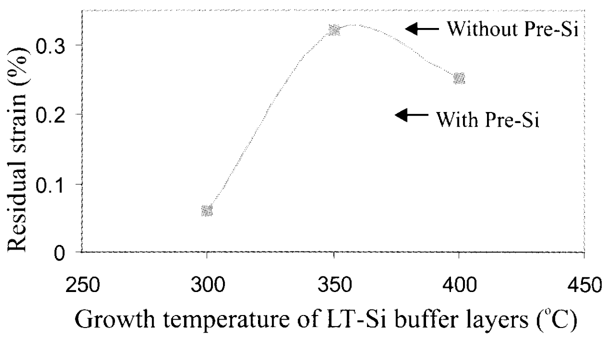


Fig. 8. Residual strain of the samples with and without pre-Sias a function of the growth temperature of the LT-Si buffer layers.

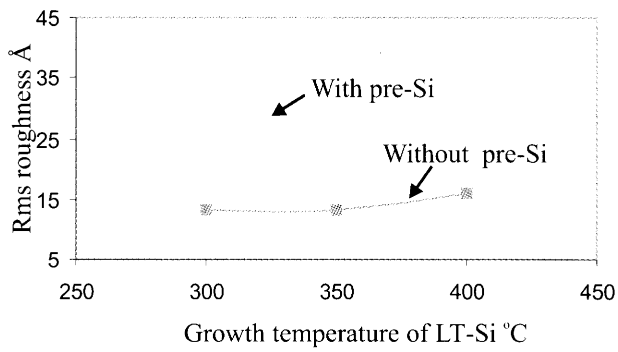


Fig. 9. rms roughness of the samples with and without pre-Si as a function of the growth temperature of the LT-Si buffer layers.