Nanogap Device: Fabrication and Applications

Jun Hyun Han
Marquette University

NANOGAP DEVICE : FABRICATION AND APPLICATIONS

by

Jun Hyun Han, B.A., M.A.

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A nanogap device as a platform for nanoscale electronic devices is presented. Integrated nanostructures on the platform have been used to functionalize the nanogap for biosensor and molecular electronics. Nanogap devices have great potential as a tool for investigating physical phenomena at the nanoscale in nanotechnology. In this dissertation, a laterally self-aligned nanogap device is presented and its feasibility is demonstrated with a nano ZnO dot light emitting diode (LED) and the growth of a metallic sharp tip forming a subnanometer gap suitable for single molecule attachment.

For realizing a nanoscale device, a resolution of patterning is critical, and many studies have been performed to overcome this limitation. The creation of a sub nanoscale device is still a challenge. To surmount the challenge, novel processes including double layer etch mask and crystallographic axis alignment have been developed. The processes provide an effective way for making a suspended nanogap device consisting of two self-aligned sharp tips with conventional lithography and 3-D micromachining using anisotropic wet chemical Si etching. As conventional lithography is employed, the nanogap device is fabricated in a wafer scale and the processes assure the productivity and the repeatability. The anisotropic Si etching determines a final size of the nanogap, which is independent of the critical dimension of the lithography used.

A nanoscale light emitting device is investigated. A nano ZnO dot is directly integrated on a silicon nanogap device by Zn thermal oxidation followed by Ni and Zn blanket evaporation instead of complex and time consuming processes for integrating nanostructure. The electrical properties of the fabricated LED device are analyzed for its current-voltage characteristic and metal-semiconductor-metal model. Furthermore, the electroluminescence spectrum of the emitted light is measured with a monochromator implemented with a CCD camera to understand the optical properties. The atomically sharp metallic tips are grown by metal ion migration induced by high electric field across a nanogap. To investigate the growth mechanism, in-situ TEM is conducted and the growing is monitored. The grown dendrite nanostructures show less than 1nm curvature of radius. These nanostructures may be compatible for studying the electrical properties of single molecule.

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Jun Hyun Han, B.A., M.A.

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TABLE OF CONTENTS

LIST OF FIGURES

1. INTRODUCTION

For many years, the interest in nanoscale materials and devices has been increasing. Much work has been performed to develop fabrication methods and to apply nanoscale devices in diverse fields. Work has been done to interpret physical phenomena such as the quantum effect (Mao, Li, Wu, & Xu, 2009; Romeike, Wegewijs, Hofstetter, & Schoeller, 2006; Shin et al., 2011), plasmon (Larsson, Alegret, Kall, & Sutherland, 2007; Quinn et al., 2000), and ballistic transport (Kong et al., 2001), which occur only at nanoscale level (10^{-9} m), which is equivalent to the size of an atom or a molecule. Also, the interpreted phenomena have been applied in various fields including electronics, material science, biology and chemistry. In this work, a novel fabrication method for the suspended nanogap device is presented, which could be used as a platform for nanoelectronics. Some of the applications based on the nanogap device are also investigated.

1.1 Nanoscale science and engineering

The nanotechnology recently applied in numerous science and engineering fields is not a new discipline. The origin is in a lecture given by Richard Feynman at the annual meeting of the American Physical Society in 1959 (Feynman, 1992). In this speech, he highlighted the possibility of manipulations and machining of materials in the atom or the molecular level and emphasized effectiveness and efficiency of this small world. In 1974, Norio Taniguchi was the first person to use the term "Nanotechnology" for explaining the preciseness and fineness on the order of 1nm, 10^{-9} meter in length (N. Taniguchi, 1974). After that, with the development of microelectromechanical systems (MEMS), the various fabrication methods for realizing a system or a device in micro or nanoscale have been developed and numerous devices have been designed and fabricated in various fields.

One interesting outcome in nanotechnology is a nanowire having a diameter of nanometer size, equivalent to about one thousandth the diameter of a human hair. Metal nanowires and semiconductor nanowires are applied in electronics, photonics, sensors, and energy applications. This is because the unique physical properties such as thermoelectric properties, quantum size effects and sensitivity arising from the large surface to volume ratio are exhibited, which are different from these of bulk material (Soci et al., 2010). As an example, X. Duan reported a nanoscale field-effect transistor with a single crystal indium phosphide nanowire (Duan, Huang, Cui, Wang, & Lieber, 2001) . Also, a single crystal silicon nanowire doped with boron or phosphorus could be used as building blocks for a passive diode and active bipolar transistor (Cui & Lieber, 2001). These results proved that the nanowires could apply to nanoscale electronics without the complex processes used in the semiconductor industry, since they can transfer electrons and holes. Since the nanowires have a large surface to volume ratio, promising high sensitivity, and the size of the nanowire is similar to the size of the species being sensed, nanowire sensors have also attracted much attention. For example, SnO_2 nanowires for detecting 10 ppm hydrogen gas have been developed (B. Wang, 2008). Similarly, a CuO nanowire was tested as a CO gas detector (Liao et al., 2009). In these experiments, the change of electrical conductance or resistance of the fabricated sensor was measured to detect a gas. The sensitivity of nanowire to light allows for the application to photo detectors. A report on a photodetector using ZnO nanowire was presented (Kind, Yan, Messer, Law, & Yang, 2002). According to this work, the conductivity of ZnO nanowires shows magnificent current change to incident of specific ultra violet light at 365nm, corresponding to the ZnO band gap.

To overcome the limitation of miniaturization in the semiconductor industry, many researchers have started to consider several conceptually new materials and structures from the molecular scale point of view. One of the progressive fields is molecular electronics, which uses electron and hole transport in single organic molecules connected to two electrodes (Tsutsui & Taniguchi, 2012). The first basic design of molecular electronics is a molecular rectifier,

mimicking a semiconductor p-n junction (Aviram & Ratner, 1974). Their work presented the feasibility of using a single molecule as a building block in electronics. Following these results, research for switches, diodes, and transistors using the single molecule has been performed by many scientists. This research has been made to understand a change in electrical properties of various single molecules by controlling metal molecule contact and stimuli such as electric field and light. Applying nanotechnology in electronics will lead to the creation of new components that operate faster, have higher sensitivity, consume less power, and can be packed to higher densities.

1.2 Nanogap device

Although various approaches for synthesizing nanomaterials such as nanowires, nanoparticles, and carbon nanotubes have been developed, there are still some challenges for understanding their electrical, optical and thermal properties, as well as employing nanoscale structures and materials in electronic devices. The existing challenges to use nanomaterials for developing new electric components are basically related to two questions. How do materials at the nanoscale integrate with macro or micro devices? How can researchers measure physical or electrical properties of single molecules and build physically stable devices with nanostructure and nanoscale materials? Since nanotechnology involves handling the materials at the nanometer scale, devices or instruments for investigating nanoscale material should allow for manipulating them at the nanoscale. Metal electrodes for integrating the target nanomaterials are especially required for understanding their optical and electrical properties. The method for integrating a nanostructure into a nanoscale device involves establishing a junction between metal electrodes and the materials. Before the development of nanogap devices, scanning tunneling microscopy (STM) and atomic force microscopy (AFM) were utilized for studying electrical and optical properties. Although these methods are useful for interpreting prototype devices in a laboratory, it

is very difficult to apply this approach to practical devices or chips due to the volume and cost of the instruments. Therefore, a device that is small enough to integrate a nanoscale material at the chip level is required. Research for a nanogap device which consists of an electrode with a nanometer gap separation has already begun. Nanogap devices integrating nanowires, conductive organics, or metals on metal electrodes have been employed for molecular electronics (Iqbal, Balasundaram, Ghosh, Bergstrom, & Bashir, 2005; Sapkov & Soldatov, 2013; Tang et al., 2009), optical plasmonics (Ward, Huser, Pauly, Cuevas, & Natelson, 2010), tunneling based sensors (Albrecht, 2012; Kubena, Vickers-Kirby, Joyce, Stratton, & Chang, 2000) and bio/chemical sensors (S. K. Kim et al., 2009; Lohndorf, Schlecht, Gronewold, Malave, & Tewes, 2005) .

1.3 Recent work on nanogap devices

For nearly 20 years, various approaches for fabricating nanogap devices with nanofabrication methods have been studied. The fabrication methods investigated are classified into five main types and include mechanical pulling, direct electron beam lithography (EBL), electrochemical deposition, focused ion beam machining nanowire, and electromigration. This work has been reported and promising results have been presented. In this chapter, major methods for fabricating nanogap device are introduced and investigated.

1.3.1 Mechanical pulling

The mechanical pulling method for fabricating two facing gold electrodes was reported by M. A. Reed et al. in 1997 (Reed, Zhou, Muller, Burgin, & Tour, 1997). To create the nanoscale gap with a gold wire, a notched gold wire was installed on a bending beam using glue contacts for fixing it in place as shown in Fig. 1. 1. The beam was supported with pizo elements and counter supports. All of the components were immersed in benzene-1, 4-dithol solution in tetrahydrofuran (THF) creating a nanogap and integrating a molecule simultaneously.

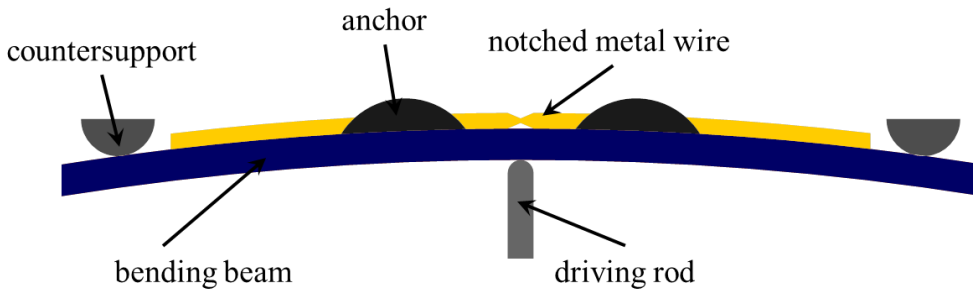

Fig. 1.1 Schematic illustration for nanogap formation by using the mechanical pulling method.

The gold wire was stretched by a pizo element until breakage to form a separated tip at room temperature. After the breakage, the monolayer was self-assembled for establishing a junction between the tips. The current-voltage characteristic and conductance of the molecule integrated to gold wire by self-assembly method was measured. Although the method was very useful for understanding of electronic transport at a molecular scale, the number of molecules forming a junction with the gold electrode was ambiguous due to uncontrolled curvature of the radius. Futhermore, the kinds of applied target materials were limited since the self-assembly method was employed for integrating materials such as atoms or molecules to the gold wire. Due to the existence of a driving unit for breaking gold wire, direct imaging for measuring physical size of fabricated nanogap was another challenge.

1.3.2 Electron beam lithography

Electron beam lithography (EBL), based on charged particle-beams, is a high resolution patterning technique. The focused electrons having high energy are used to expose electron sensitive resist like polymethyl methacrylate (PMMA). The patterning is started with coating the substrate with a layer of electron resist, PMMA, and then exposing the layer to an electron beam

in a targeted area with a software mask instead of a physical mask. The energetic electron beam breaks bonds with PMMA so that The PMMA can be dissolved in some chemicals.

The work applying direct EBL to nanogap fabrication was reported by M. D. Fischbein in 2006 (Fischbein & Drndic, 2006). Fischbein presented a strategy for controlling the electron back scattering, which affected the critical dimension of the printed pattern. In order to reduce the back scattering, a silicon nitride (SixNy) thin film was used as a substrate. The pattern defined by EBL was utilized for metal deposition, and lift off was performed to remove undesired metal by dissolving the patterned resist underneath the metal. The merit of this method is that a nanogap that is only a few nanometers in size is fabricated without additional processes. Although the EBL offers a high resolution pattern, it is a time consuming process which is not acceptable for wafer scale fabrication. Mass production and repeatability is another challenge.

1.3.3 Electrochemical deposition

The methods of electrochemical deposition combined with conventional optical lithographic technology provided a simple, reproducible and controllable nanogap (F. Chen, Qing, Ren, Wu, & Liu, 2005; Narang, Reddy, Saxena, Gupta, & Gupta, 2012; Umeno & Hirakawa, 2005). The large initial gaps between metal electrodes on a Si or glass substrate were fabricated through lithography and either a lift off process or metal etching as shown in fig 1.2 (a). The gaps were then narrowed down to a nanometer scale with electrochemical deposition on the fabricated electrodes as shown in Fig. 1.2 (b). In order to control the size of the gap, resistance or voltage change was monitored, and the process was stopped when the monitoring signal reached a predetermined value. The method provided a gap that was tens of nanometers wide. However, since deposited metal was added to the initial metal nanogap, it was difficult to fabricate an atomically sharp nanogap, which is required in molecular electronics. Also, the method fabricates electrodes having rough surfaces since the plating results in large grain size for the gold.

Furthermore, as the electroplating of gold requires cyanide material, which needs special care for handling and pH control, to prevent the generation of highly toxic hydrocyanic acid. These requirements result in an environmentally unfriendly process.

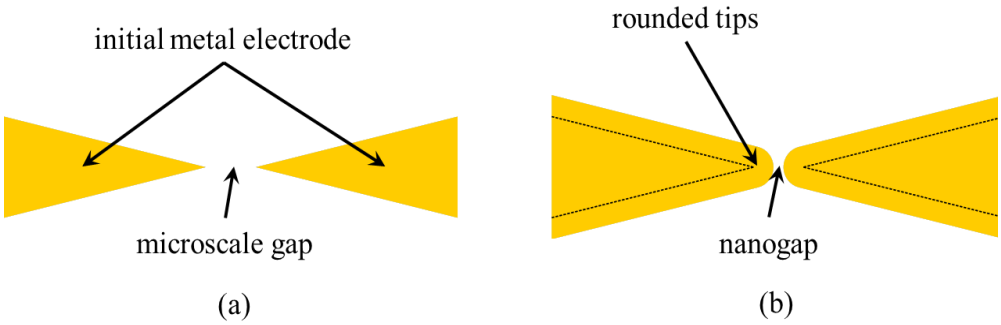

Fig. 1.2 Schematic illustration of nanogap forming by electrochemical deposition. (a) Initial metal electrode defined by lithography. (b) Metal tips forming nanogap by electrochemical deposition showing large radius of curvature.

1.3.4 Focused ion beam (FIB)

The focused ion beam (FIB) developed in the 1970s has been applied in diverse fields including localized milling, deposition of material, surface modification, and imaging of materials with high performance ion beams. Especially in the MEMS, the technique has demonstrated its capability for rapid prototyping of complex 3D structures at the micro or nanoscale (C. Kim, Ahn, & Jang, 2012). The principle of the method is that when the ion beam is directed onto a target solid surface, all surface atoms will receive energy. If the energy is bigger than the surface binding energy, the surface atoms will be sputtered.

The fabrication of a nanogap using FIB has been performed by T. Nagase in 2006 (Nagase, Gamo, Kubota, & Mashiko, 2006). Their process consisted of two steps. The first step was to form a nanowire that was 50nm wide and 200nm long on a patterned electrode using lithography as shown in Fig. 1. 3 (a). In the second step for fine machining, the wire is irradiated

using a 12nm diameter ion source and a line scan with real time monitoring. Finally, nanogaps of 3~6nm are fabricated as shown in Fig. 1. 3 (b) and the author claims that the yield is about 90%.

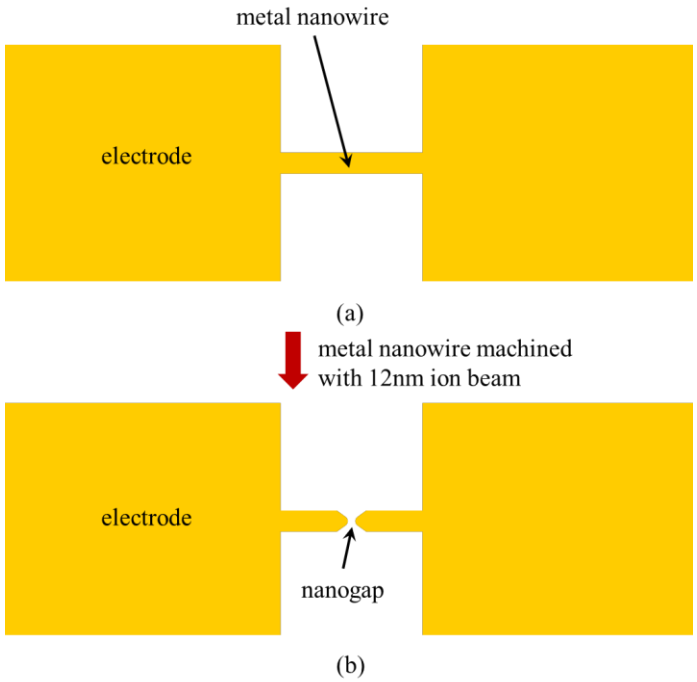

Fig. 1.3 Schematic illustration of a nanogap forming with FIB. (a) Initial metal nanowire defined by lithography. (b) Formed nanogap on nanowire after nanowire machining by 12nm ion beam.

Although the FIB allows for fabrication of the nanometer sized nanogaps and controlled position with the in situ monitoring milling step, the fabricated nanogap top surface is rough due to redeposition of milled material. Also, for fine nanogap creation, the number of parameters has to be precisely controlled. These interacting parameters which determine the gap size and geometrical properties include scan strategy, ion energy, ion current and dwell time.

1.3.5 Electromigration

The electromigration method for generating a nanogap at the nanometer scale uses electron wind force to break nanowires. Generally, electromigration has been studied in order to understand the failure mechanism of thin metal wires broken under a large current density over a long period of time in an integrated circuit. The phenomenon is a complex interaction that is affected by several variables, including the size and material of interconnection, current density, and temperature. At high current densities, the motion of electrons is equivalent to the electron wind, which involves the transfer of momentum. The motion forms an electron stream flowing through a metal to a scattering center embedded in the metal (Hesketh, 1979). The metal atom gains momentum from collisions with conducting electrons and starts its motion along the direction of the electron wind. As a result, the migrating atoms leave behind vacancies, and the combination of these vacancies gives rise to the formation of a void at the cathode. The migrating atoms accumulate toward of the anode, forming hillocks.

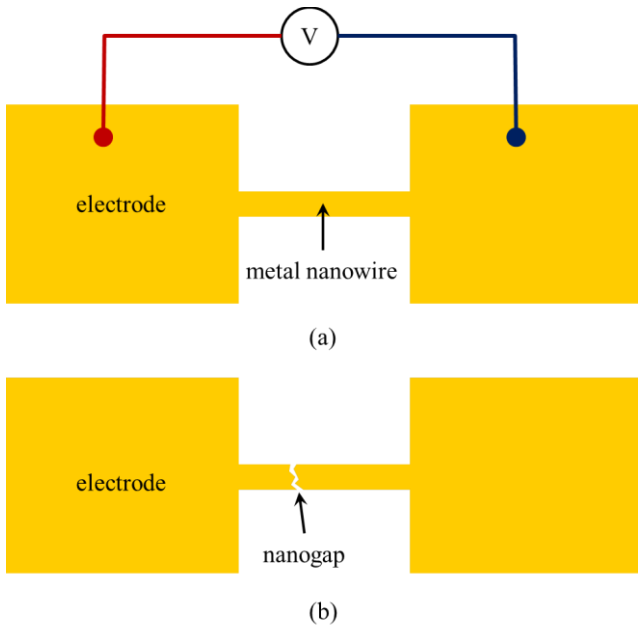

Fig. 1.4 Schematic illustration of nanogap formation with electromigration. (a) Initial nanowire defined by EBL. DC is biased on electrode for generation Joul heating. (b) Formed nanogap by electromigration.

This method is advantageous for fabricating nanogap based on existing nanoscale wires or nanostructures between metal electrodes as shown in Fig. 1. 4 (a). However, the fabrication of the nanowire or the nanoscale structure is another challenge. It is usually complex and time consuming, using processes such as electron beam lithography (Strachan et al., 2005). When the initial thickness of the lithographically defined electrode is not fine enough, the nanogap created using electromigration has an irregular shape, and controlling the size and position of the nanogap is tedious work (Hadeed & Durkan, 2007) .

1.4 Our method

As mentioned in previous sections, the nanogap device is an important component of a device for understanding electronic properties of nanoscale materials and for constructing a nanoscale device using nanoscale materials. However, previous devices have demonstrated some limitations when connecting single molecules or single nanowires to the fabricated devices, since the devices have large radius of curvature tips, although the size of the gap is proper for the single molecule size. The rounded electrode offers only a chance connection of a few materials since the width of the material is smaller than the curvature of radius of electrode. Also, the devices fabricated on silicon substrates which are insulated by silicon oxide or silicon nitride affect the measurement of electrical or optical properties, due to the interaction between target materials and substrates.

A new method to overcome drawbacks of other methods is required for realizing the integration of a single nanostructure. The method presented in this work employs conventional lithography and 3-D micromaching using anisotropic wet chemical etching of silicon for suspended nanogap devices. The processes developed and the fabricated nanogap device have following unique properties :

a. Photolithography, which allows fast pattern transfer, is used since the final nanogap size is not affected by the resolution of applied lithography, but rather determined by silicon etching for a specified time.
b. Since photolithography is the industrial standard, the process developed is compatible with the complementary metal-oxide-semiconductor (CMOS) fabrication process.
c. Since the size of the nanogap is determined by a self-terminated (111) plane etching and (100) plane etching, the critical dimension limitation of optical lithography is overcome to create nanoscale devices.
d. Since the fabricated electrode consists of 3 planes, one (111) plane and two (100) planes, a self-aligned zero dimensional sharp tip can be obtained.
e. The 3-D micromachining allows fabrication of the suspended nanogap device using a silicon-on-insulator (SOI) wafer.
f. The suspended nanogap device allows blanket metal evaporation instead of metal etching or lift-off resulting in complex processes, so various metal and organic materials can be deposited on the silicon nanogap device.
g. The suspended nanogap device minimizes the leakage current occurring between metal electrodes and a substrate or between a target material and a substrate.
h. Since the suspended nanogap device allows direct integration of a semiconductor material, ZnO, across the nanogap, time consuming and laborious work is not needed for integrating nanostructure into the fabricated nanogap device.
i. The fabricated device is acceptable for direct imaging with TEM since the machining of the handle wafer of SOI does not affect physical stability of the suspended nanogap device.

1.5 Chapter outline

In chapter 2, the fabrication methods, including lithography and etching, for nanoscale devices will be introduced. Although the methods came from MEMS technology, the techniques have been developed to realize nanoscale devices. The method for accurate alignment of lithographically defined patterns to the crystalline axes of the substrate will be investigated for achieving etching resolution and uniformity in fabrication of a nanoscale device.

In chapter 3, the suggested fabrication process for a suspended nanogap device will be presented. For realizing suspended nanogaps using 3D micromachining, the device design, process development, device fabrication, and tip sharpening with low temperature thermal oxidation will be described in detail. The anisotropic wet etching for silicon machining using the unique double layer etch mask is applied.

In chapter 4, the applications of a suspended nanogap device will be presented. The mechanism of forming a sub-nanometer scale, atomically sharp tip by induced electric field is defined, and an experimental set up for forming an atomically sharp tip based on suspended nanogap devices will be described. Also, a practical light emitting diode (LED) device using nano zinc oxide (ZnO) dot based on the suspended nanogap device will be presented. The nano ZnO dot is directly grown across a suspended nanogap and the light emission mechanism and electrical characteristics of the device will be explained with a metal-semiconductor-metal model.

Finally, in chapter 5, the results of the previous chapters will be summarized and future work presented.

2. NANOSCALE DEVICE FABRICATION

As the scale of a nanoscale device corresponds to the size of an atom or molecule, the fabrication method should consider how to integrate and locate the tiny materials at an exact position in the device. Also, many unconventional lithographic techniques have been developed and applied to realize the devices at nanoscale. In this chapter, the method developed for patterning nanoscale structure, categorized as a top-down and bottom-up approach, will be presented. The top-down approach includes conventional photolithography, deposition and etching to fabricate nanoscale devices based on a bulk substrate. The bottom-up approach uses non-conventional lithography techniques such as scanning probe lithography and soft lithography with self-assembly monolayer. This offers an effective way for building nanoscale structures. Also, an excellent method for crystallographic axis alignment is reported in this chapter. The optical alignment method developed is an important step in the fabricating of nanoscale devices with 3-D bulk machining using anisotropic wet chemical etching.

2.1 Top-down and bottom-up

The nanofabrication can be categorized into two main approaches, top-down and bottom-up. Fig. 2.1 shows shcematically the concept of both approaches for building nanostructures. The bottom-up approach, inspired by biological processes using chemical or physical forces to assemble basic units such as atoms, molecules, proteins, and DNA into larger structures, has been widely adapted to nanofabrication. The typical bottom-up approach uses chemical processes such as self-assembly, sol-gel, chemical vapor deposition (CVD), template synthesis, and spays pyrolysis (Ruiz-Hitzky, Aranda, Darder, & Ogawa, 2011). In sol-gel synthesis, solid particles (chemical precursors) in a liquid form a gel by dehydration and chemical reaction at low temperature, 200°C to 600°C. In the gel state, the materials are shaped or applied onto a substrate by spinning, dipping, or spraying.

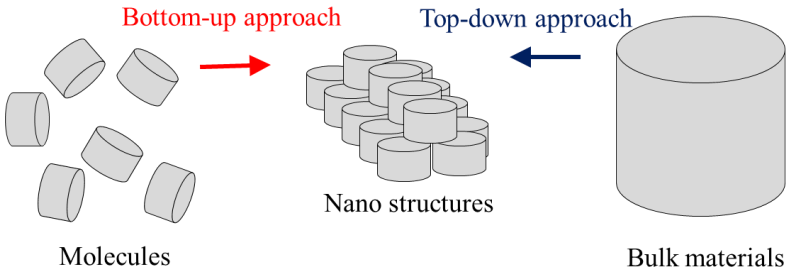

Fig. 2.1 Schematic illustration of top-down and bottom-up approach.

The top-down approach begins with bulk substrates such as Si and glass wafers and reduce them into smaller and smaller pieces by cutting, etching, and slicing as shown Fig. 2.1. The approach for fabrication of nanoscale devices is similar to conventional fabrication methods used by the semiconductor industry and for microelectromechanical systems (MEMS). The overall process is categorized by three steps as shown Fig. 2.2. The first step is film deposition using chemical vapor deposition (CVD) and physical vapor deposition (PVD). In this step, various films including silicon dioxide (SiO_2), silicon nitride (Si_xN_y), polysilicon, and metals are deposited for various purposes. The deposited film is utilized as an etch mask, an electrode, an insulator, or structure supporter, depending on the mechanical, electrical, and chemical propeties of the film. After deposition, in order to transfer patterns on the layer, lithography is performed. The resolution of the features is determined by the resolution of the lithography used. A resist is coated on the substrate and the required feature is created on the substrate through a development process in a suitable solution followed by alginment and exposure steps. The remaining resist layer acts as a etch mask for dry etching or wet etching. The etching makes 3 dimensional structures having a height, a length and a width in micro or nanoscale onto a subtrate. In this step, dry etching and wet etching technique can be applied to form designed shapes. These three steps are continuously repeated until a designed device is produced.

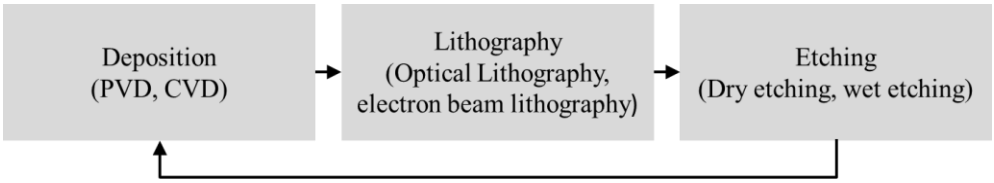

Fig. 2.2 Top-down approach for nanoscale device fabrication

Although nanofabrication is categorized by top-down and bottom-up approaches, hybrid nanofabrication, which combines both approaches, is required to integrate systhesized nanomaterials to functional devices such as sensors and electrical components in real appications like the ZnO nano dot LED in this work. In the following sub chapters, two steps, lithography and etching, which mainly determines the quality of nanoscale devcies in fabrication processes, are discussed.

2.2 Lithography

In nanoscale device fabrication, since most of the geomteric factors including size, accuracy, and resolution are decided by the resolution or critical dimension (CD) of the applied lithography, this process is the most important for realizing the designed features and topology. For microscale devices, the photolithography technique has enough resolution for the fabrication of devices, but for nanoscale devices, it does not. For more accurate features required for the nanoscale, many techinques have been developed to surmount the resolution limitation. The methods replacing photolithography include EBL and other approaches such as nano imprint, soft lithography, scanning probe lithography and nano ink have been developed.

2.2.1 Photolithography

The most widely used form of lithography for fabrication of structures for the integrated circuit (IC) and MEMS industry is photolithography. The major advantages of this method are a

high throughtput and a reproducibility assuring low cost. The overall process is divided into seven steps and is shown in Fig. 2.3. The most sensitive steps determining the accuracy and resolution of the fabricated devices are the alignment and the exposure.

Process	Purpose
Dehydration	Removing most of the absorbed water on the surface of substrate
↓	
Coating hexamethyldisilazane (HMDS)	Acting as a promoter between the surface of substrate and photoresist
↓	
Spin coat	Coating liquid photoresist material with 3,000rpm or higher
↓	
Soft bake	Driving off the solvent in resist on hotplate
↓	
Alignment and exposure	The resist coated wafer is aligned to the mask and the mask pattern is transferred on the photoresist
↓	
Develop	The soluble area of photoresist are dissolved by liquid developer chemical
↓	
Hard bake	Evaporating the remaining photoresist solvent and improving the adhesion of the resist to the wafer surface

Fig. 2.3 Overall process of photolithography

In photolithography, the resolution limit mainly depends on diffraction, and it can be represented as

$$R = k_1 \frac{\lambda}{NA} \qquad (2.1)$$

where, λ is the wavelength of the incident light, NA is the numerial aperture of the imaging lens system, and k_1 is an expreimental parameter depending on resist parameters, process conditions, and mask aligner optics (Madou, 2002). Therefore, an optical lithography system having a smaller wavelength, larger numerical aperture, and a smaller k1 is required to reduce the resolution. With the development of optics, G line (436 nm), I line (365nm), KrF (248.3nm), ArF (193.4nm), F2 (157.6nm), and extreme ultraviolet (EUV, 13.5nm) can be installed onto the exposure system, and the system using EUV can acheive 16nm resolution (Brunner, 2003). Also, in order to increase the NA, a lens with low aberration level is required. The process can be improved by controlling wafer flatness, thinner resist coating, and reducing topography. To realize low k1, a lot of research has been performed exploring various phase shift mask approaches (Gueder, Yang, Krueger, Stevens, & Zacharias, 2010; Kwak, Ok, Lee, & Guo, 2012), off-axis illumination (Y. Kim et al., 2009), subresolution assist feature (Kempsell et al., 2009), and an optical proximity correction method (Melville et al., 2011).

2.2.2 Nanoimprint

Although many efforts have been made to increase the resolution of phtolithography, the improvements are accompanied by increased cost, due to a complex photolithography system and strict management during the resist coating step. The nanoimprint lithography (NIL) is an exellent alternative for solving the increasing cost in device fabrication. The method applied to production of compact disks has been developed, and 25nm vias and trenches were fabricated with thermal nanoimprint lithography (Chou, Krauss, & Renstrom, 1995). The principle of nanoimprint lithography is simple, having two basic steps. Fig. 2.4 shows the process of the originally proposed NIL process (Chou, Krauss, & Renstrom, 1996). In the first step, the imprint step, the pattern of nanostructures on the surface of the mold is transferred to the resist by pressing, and then the mold is removed. During the imprint step, the resist is heated to a temperature above its

glass transition temperature to become a viscous liquid being able to flow, and the resist can be easily deformed into a replica shape to the mold. In the second step, anisotropic etching is performed for removing the residual resist. Since the method does not use any optics, the resolution is not limited by the effects of wave diffraction. Generally, PMMA is used as a primary resist since the material has a small thermal expansion coefficient and small pressure shrinkage coefficient to offer an exact replica of the mold. The advantages of NIL are high patterning resolution, high pattern transfer accuracy, 3-D patterning, simplicity in reducing other fabrication steps, high throughput, and low cost. However, NIL should be performed in a vacuum to reduce air bubble creation resulting from heating the PMMA. Also, the process needs a contact between an imprint mold and a wafer. As the mask could be damaged, it has to be changed periodically.

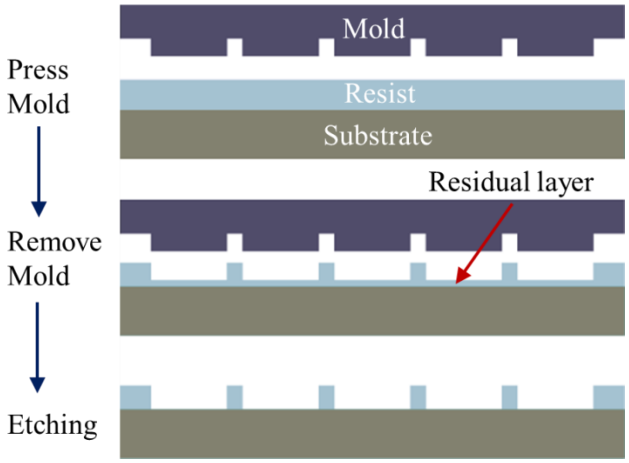

Fig. 2.4 Schematic illustration of nanoimprint lithography (NIL). The process consists of pressing the mold for transferring the mold pattern to the resist, removing the mold, and the anisotropic etching for removing residues on the surface of the substrate.

After the original method was invented, more improved methods have been applied in device fabrication including grating fabrciations (Chu et al., 2007; Z. Yu, Wu, Chen, & Chou, 2001), fabrication of metal line on plastic substrate (H. Lee, Hong, Yang, & Choi, 2006),

fabrication of organic light-emitting diodes (Ishihara et al., 2007), and fabrication of nanochannel for a bio chip (D. Xia, Yan, & Hou, 2012).

2.2.3 Scanning probe lithography

A technology which can directly manupulate a nanomaterial is scanning probe lithography using AFM. The AFM was originally invented to measure the topology of a surface with high spatial resolution, known as atomic resolution. The microscope measures a surface through the deflection of a micro cantilever having an atomically sharp tip on the end of it. The attractive or replusive force between the tip and the surface varying with the space between the tip and the surface induces deflection of the cantilever, and the deflection detected by reflecting a laser beam from the cantilever on to a photodiode is used to image the surface topography by raster scanning the tip over the surface. The Fig. 2.5 shows the typical AFM probe and operation process for imaging the surface.

The lithography based on the atomic force microscope uses a sharp probe to heat, scratch, oxidize or transfer nanomaterials to the surface of substrates for patterning nanoscale features. The method is an effective method compared to the photolithographic process due to its simplicity, high resolution, and low cost. One of the methods developed uses a localized electron source for exposing 200nm PMMA film with a gold coated tip (Majumdar et al., 1992). In this work, the energy for dissoling polymer chains is supplied by biased voltage between the AFM tip and the gold coated substrate. The resolution of the method depends on the radius of the tip. Exposing of the PMMA using AFM lithography results in no mechanical damage and no chemical modification of a polymer film.

The scratching method with an AFM tip that is fabriated with silicon nitride is another lithography method using AFM for patterning at the nanoscale on surfaces of III-V semiconductors (Magno & Bennett, 1997) and conducting polymers (L. Li et al., 2010). In these

methods, the AFM tip is used for physically scratching the semiconductor and polymer surface with AFM mechanical contacting force to the surfaces. For sucessful work, the parameters including the cantilever properties, tip material, substrate condition, and speed of tip have to be correctly controlled. For example, cantilevers having a large spring constant are useful for making deeper features, and a sharper tip allows a for narrow features.

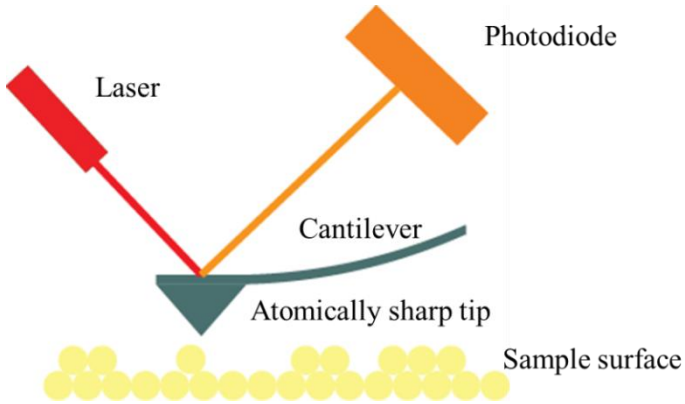

Fig. 2.5 Schematic illustration for measurement principle of AFM

Also, AFM lithography is employed for direct modification of thin polymer films on a substrate by a resisitive heating induced tip (Basu, McNamara, & Gianchandani, 2004; Mamin, 1996). For generating heat on the tip, a piezoresistive cantilever fabricated with silicon that was doped with boron was used as a substrate in Mamin's work. For producing nanoscale pits on the polycarbonate surface, the AFM tip is heated up to 170°C. The concept of the method is extended to read, write and erase data on a thin polymer film with an array of AFM-type probes, called Millipede (Vettiger et al., 2002).

The method for directly producing nanostructures on the substrate using AFM lithography is tip-induced local oxidation on a silicon or metal surface (Avouris, Martel, Hertel, & Sandstrom, 1998). AFM tip-induced local oxidation is an electrochemical anodiazation based on biasing between a tip and a surface under ambient conditions. When an AFM probe is brought

close to the metal or the semicondutor surface and a bias is applied to it, ambient humidity acts as source of OH- ions for oxidizing the surface. The major parameters for height and width of the oxide grown are level of biased voltage, AFM tip scanning rate, and concentration of humidity. Oxide dots, grating and pillars have been reported (Červenka et al., 2006; Mo, Wang, & Bai, 2008; Nemutudi, Curson, Appleyard, Ritchie, & Jones, 2001) for the tip-induced local oxidation with AFM.

A recently developed lithograhy for transferring molecules to metal surfaces using an AFM tip is dip pen nanolithography (DPN). In this method, capillary transport of molecules from the AFM tip to the solid substrate is used to directly write patterns consisting of a relatively small collection of molecules in submicrometer dimensions (Piner, Zhu, Xu, Hong, & Mirkin, 1999). When an ink coated AFM tip contacts the surface, a water meniscus natually forms between the tip and the surface and then the ink moves on the substrate by capillary transport through the meniscus. The important key for successful DPN patterning is choosing an ink and a substrate with an appropricate chemical affinity. For example, in the first report with this approach, 1-octadecanethiol and Au were used as the ink and substrate. Variables considered for successful molecular transport include chemical affinity as well as temperature, humidity, contact force of tip, and scanning speed. An accurate control of these variables allows dots to be obtained, as well as lines with nanoscale resolution. This method has been used for patterning a molecule (Ivanisevic & Mirkin, 2001), a protein (Noy et al., 2002), and DNA (Demers et al., 2002). Futhermore, parallel DPN has been developed for high throughput and increasing area accessibility (M. Zhang et al., 2002).

2.2.4 Soft lithography

Another alternative method developed for replacing opticallithography is soft lithography which is a non-photolithographic set of printing methods and uses patterned elastomers as a

stamp, mold, or mask for fabrication of micro or nano scale structures (Y. Xia & Whitesides, 1998). Soft lithogrpahy is the collective name for the set of techiniques including microcontact printing (μCP) for self assembly molecules, replica molding (REM), microtransfer molding (μTM), micromolding in capillaries (MIMIC), and solvent-assisted micromolding (SAMIM). Since elastomeric materals are used as a stamp, mold, or mask instead of a rigid photomask in these methods, they can be suited to nonplanar substrates as well as flat substrates. Also, they can be applied to the flexible substrate made by polymers.

To fabricate a master mold in softlithography, a conventional lithography technique, micromachining or e-beam lithography is performed with a silicon or a glass substrate. An elastomeric stamp is cast from the master mold functionalized with silane vapor to protect the polymer from adhering to the surface of the master. The elastomeric material poured over a master is cured and released for fabricating a stamp. The typical material for a stamp is polydimethylsiloxan (PDMS) because it provides a surface that has a low interfacial free energy allowing easy release from the substrate after stamping, does not react with other chemicals, does not swell with humidity, has good thermal stability, is isotropic and homogeneous, is optically transparent down to 300nm, and passes gas easily.

A method for forming patterns of self-assembled monolayers (SAM) on surfaces of substrates by contact between stamps wetted with an ink of the molecules (alkanethiol) and substrates is μCP. With this method, only the regions that come into contact with the stamp are covered with a monolayer of SAM on a gold coated substrate, and unstamped areas remain bare. Although SAM does not allow the durability to serve as resists for pattern transfer in reactive ion etching due to its thin thickness, some of the SAM techniques, which are hydrophobic, such as CH_3- and CF_3- terminated, one can withstand for wet ecthant since hydrophobic interations between patterned SAM and a sorrounding aqueous wet etch enhances the barrier properties of SAM. Therefore, it serves as a resist for wet etching the underlying substrate. Also, μCP is used to demonstrate a selective atomic layer depostion of TiO_2 thin film using chemical vapor

deposition on patterned alkylsiloxane self-assembled monolayers (M. H. Park, Jang, Sung-Suh, & Sung, 2004) .

Instead of a pattern of self-assembled monolayers, the approach for patterning organic materials such as polystyrene and SU-8 is replica modeling (REM). REM is an efficient method for duplication of the topography including shape, morphology and the structure of the mold. The fabrication process is similar to μCP in fabricating PDMS molds, but in order to pattern the inverse shape of the mold, a solidifying process for a liquid precursor poured on the mold is required. REM is applied in polymer microring resonators (J.K.S. Poon, Yanyi Huang, G.T. Paloczi, & A. Yariv, 2004), high-aspect ratio polymeric nanopillars (Y. Zhang, Lo, Taylor, & Yang, 2006) , and 3-D metal patterns with a metal sputtered PDMS mold (Zhao et al., 2009).

Microtransfer molding (μTM) is a form of softlithography and a useful method for fabricating simple patterns in the nanoscale. A typical μTM procedure has four steps. A liquid prepolymer is applied to the recessed regions on the mold and the mold is put in conformal contact with the substrate. The prepolymer is cured by exposure to ultraviolt light and the mold is peeled off. The residual polymer is removed by oxygen plasma treatment. The major advantages of μTM are simplicity, an ability for fabrication of multilayer structure, and an allowance of highly parallel processes for high throughput. The approach, μTM, has been used for fabricating glassy carbon microstructures (Schueller, Brittain, & Whitesides, 1999) , arrays of Schottky diode (Hu, Deng, Beck, Westervelt, & Whitesides, 1999) and microlens arrays (C. Chang, Yang, Huang, & Jeng, 2006) .

Micromolding in capillaries (MIMIC) uses capillary action to fill a hole or a channel which is a space between a PDMS stamp and a substrate with a liquid such as prepolymer or a mixture of the materials. The filled liquid has either cross-linked, crystallized, cured adhered, or deposited onto the surface of the substrate, and then the PDMS stamp is removed. After peeling off the PDMS, the free standing structure of organic or inorganic materials are left where they are filled in the capillaries. In this approach, the fluids with low surface tension and low viscosity are

most ideal. Although, MIMIC is limited to application involving the fabrication of innterconected structures by capillary action, it is applied to studying the biosynthesis of silver nanoparticles (R. R. Naik, Stringer, Agarwal, Jones, & Stone, 2002), fabrication of tin oxide gas sensors (Heule & Gauckler, 2003), and the patterning of bacterial cells (K. Suh, Khademhosseini, Yoo, & Langer, 2004) .

Solvent-assisted micromolding (SAMIM) uses a solvent to wet a PDMS stamp and soften or dissove the structure layer, typically an organic polymer. The applied solvent only dissolves the structure polymer, not PDMS. The PDMS stamp is pressed on a polymer film, which is dissolved in the solvant and fills the space between relief structures of the stamp. After dissipation and evaporation of the solvent, the solid polymers formed by the designed pattern remain on the substrate. The work conducted by SAMIN includes fabrication of polymer LEDs (Rogers, Bao, & Dhar, 1998), directly patterning semiconducting polymer films (Lawrence, Turnbull, & Samuel, 2003), and fabrication of an alignment layer and a wall structure for liquid crystal display (LCD) (Yun, Sung, & Cho, 2012).

2.3 Etching and bulk micromachining

After the lithography steps, materials are removed from a device, usually in a selective manner, transferring the lithography patterns onto devices for fabricating desired devices. In miniaturiztion science and engineering, there are a lot of material removing methods such as wet and dry etching, FIB milling, laser machining, ultrasomic drilling, electrical discharge machining (EDM), and traditional precision machining. Usually, a highly pure silicon wafer is used as a substrate in MEMS and NEMS (nanoelectromechanical systems). Since the silicon wafer is mechanically brittle, mechanical machining for tranferring mechanical force to the substrate is not acceptable to remove the material. Instead of mechanical machining, dry and wet chemical

etching have been widely applied to remove the film or bulk materials in processes based on wafers.

2.3.1 Dry etching

Dry etching is one of the methods for removing material from an unmasked pattern of substrate by physical ion bombardment, chemical reaction through a reactive species on the surface, or combined physical and chemical mechanisms using plasma systems. The physical etching based on ion bombardment uses plasma which provides energetic ion species that are accelerated toward the wafer surface by the electric field. When the energetic ions collide with the substrate or the thin film, their mometum is transferred to the surface of the surbstrate or thin film. If the tranferred energy exceeds the bonding energy of the target material, atoms in unprotected areas of the substrate are dislodged. Typically, an inert gas such as argon is used to generate plasma. The benefit of this physical etching approach is strong directionallity of the etch, achieving highly anisotropic etch profiles and allowing for a high etch rate. However, this approach has poor selectivity, definined as the etch rate of the material being etched relative to the etch rate of another material. Another problem is that the materials removed by the etching approach are not volatile, so the removed materials may redeposit back on the substrate, causing particulate and chemical contamination.

In the chemical etching approach, plasma creates neutral reactive species, free radicals and reactive atoms that chemically react with target materials on the substrate. The generated reactive species diffuse to the surface and are adsorbed on the surface for chemical reaction. This approach has an advantage in selectivity but produces poor critical dimension due to its uncontrolled isotropy profile. For remedying the disadvantages of physical and chemical plasma etching, a combined approach, for example, reactive-ion etching (RIE), has been presented.

The RIE process uses a physical method to assist chemical etching or create reactive ions participating in chemical etching. In this process, the wafers are placed on an RF-powered cathode inducing DC self-bias for acquiring a large voltage differemce with plasma. This condition creates directionality for the ion species moving toward the wafer, improving the anisotropic profile. With the correct selection of etching chemistry, hard mask, and process parameters (pressure, temperature, and bias), RIE provides more control in terms of the etching selectivity and final device profile (X. Peng, Matthews, & Xue, 2011) . Fluorine-based chemistry has been widely used for silicon-based materials (SiO_2, Si_xN_y, SiON SiC, etc.) etching, and chlorine-based chemistry is more effective for etching aluminum, AlN, Al_2O_3, InP, GaN, InN, etc.

In micro or nanomachining, deep reactive ion etching (DRIE) was used for building high aspect ratio vertical structures with dry etching in diverse fields including micromachined comb drives (Y. Sun, Nelson, Potasek, & Enikov, 2002) and X-ray diffraction grating (Barillaro, Diligenti, Benedetti, & Merlo, 2006). The process of DRIE involves of some steps to prevent lateral etching: (i) deposition of a fluorocarbon polymer passivation layer, (ii) etching of the fluorocarbon polymer at the bottom of the trench, and (iii) subsequent etching of the underlying silicon. The benefits of this approach are flexibility of geometric limit, high possibility of fabricating true vertical walls, and high etch rate as well as high aspect ratio. Also, the method provides high selectivity to the photomasking materials. However, because alternating etching and passivating cycles the etched side wall can not have an atomically smooth surface resulting. This issue makes DRIE unacceptable for fabricating nanoscle devices.

Dry etching differs from wet etching in materal selectivity. While wet etching allows precise control over the etched layer, dry etching also reaches the underlying layer. Precise control of the etch stopping layer is critical for nanoscale device fabrication with multilayer structure. Therefore, the plasma reactor used in nanosclae device fabrication should be equipped with a monitor that indicates when the etching process is to be terminated. An end-point can be defined by the falling signal from the layer component to be removed or by the rising signal of its

under-layer material component. Alternatively, the intensity of a reactant species or the etch byproducts can be used for end-point detection.

2.3.2 Bulk micromachining

Although anisotropic dry etching offers effective device fabrication in film and bulk machining, anisotropic wet chemical etching is widely used for shaping 3-D structures as it provides atomically smooth etched surfaces, high selectivity, excellent repeatability, high uniformity, and low production cost. Specifically, in silicon bulk machining, anisotropic wet chemical etching has been applied to fabricating membranes (Iosub, Moldovan, & Modreanu, 2002; Moser & Baltes, 1993), microfluidic devices (N. Naik et al., 2007), nanochannels (Haneveld, Jansen, Berenschot, Tas, & Elwenspoek, 2003), silicon nanowires (C. Lee et al., 2011), and AFM tips based on a cantilever (Resnik, Vrtacnik, Aljancic, Mozek, & Amon, 2003).

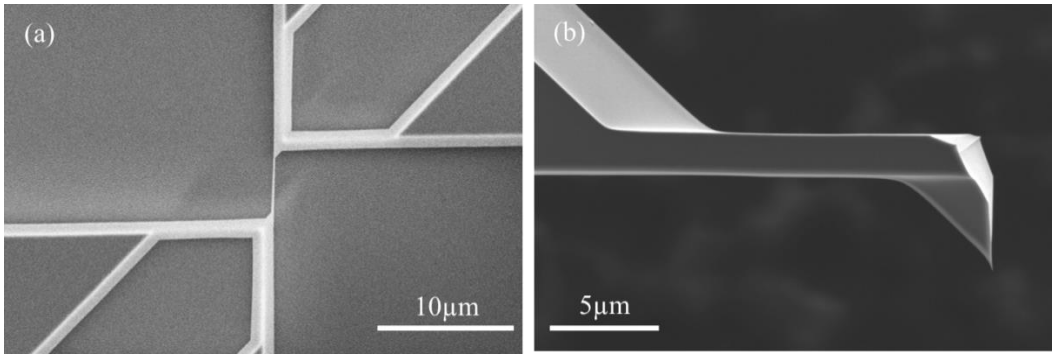

Fig. 2.6 Fabricated nanoscale device using anisotropic wet etching : (a) 80nm width and 50nm thickness silicon nanowire, (b) Silicon AFM probe showing atomically sharp tip.

In this work, the suspended nanogap device is mainly fabricated by anisotropic wet chemical etching. Fig. 2.6 shows the silicon nanowire and the silicon AFM probe fabricated on a silicon on insulator (SOI) wafer by anisotropic wet chemical etching in our lab, Nanoscale Device Lab, at Marquette University. The silicon wafer used is a (100) oriented wafer, and under etching

in [100] direction is applied to fabricate self-terminated nanowires and an AFM probe showing an atomically sharp tip. The fabricatied nanowire has 80nm in width and 50nm in thickness.

Silicon is a crystalline material with a diamond cubic lattice structure. Due to its crystalline structure, many alkaline wet etchants including potassium hydroxide (KOH), tetra methyl ammomium hydroxide (TMAH), and ethylene diamine-pyrocatechol (EDP) etch silicon anisotropically. The difference in etch rates for various crystallographic orientations in a single crystal of silicon with an alkaline solution etchant provides a large variety of silicon structures that can be fabricated in a highly controllable and reproducible manner. The etching mechanism and process for the anisotropic etching have been studied since the 1970s, and the process has been stabilized for use in diverse fileds. For example, in KOH, a representative anisotropic etchant, silicon atoms at the surface react with hydroxide anions. The silicon is oxidized and four electrons are injected from each silicon atom into the conduction band (G. T. A. Kovacs, Maluf, & Petersen, 1998) .

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^- \quad (2.2)$$

Simultaneously, water is reduced, leading to the evolution of hydrogen.

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2 \quad (2.3)$$

The complexed silicon, $Si(OH)_2^{2+}$, further reacts with hydroxide four anions to form a soluble silicon complex and water.

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2+} + 2H_2O \quad (2.4)$$

Thus, the overall reaction is

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2+} + 2H_2 \quad (2.5)$$

Due to the diffrent etch rates for the differrent crystal planes in anisotrpic wet etching, differently oriented wafers show differently etched structures. Fig. 2.7 shows the etched structures for (100)-oriented and (110)-oriented silicon wafers. In both cases, since the etch rate of {111} planes of silicon having a high bond density is much slower than other planes, {110} and {100}, the etched structure is bounded by {111} planes. The property allows 3-dimensional bulk machining of Si wafers. The anisotropic ething of the (100) oriented silicon wafer produces pyramidal pits with 54.74° {111} side wall angles relative to the (100) plane as shown in Fig. 2.7 (a). The (110) oriented silicon wafer having [111] flat shown in Fig. 2.7 (b) is used to fabrciate deep trench shapes since it is possible to fabricate an atomically smooth vertical wall.

The etch rate for a silicon wafer in a KOH solution depends on the temperature and concentration of the KOH solution as well as silicon orientation (K. Sato et al., 1998). Generally, the etch rate of KOH increases with increating temperature and the decreasing concentration of either H_2O or OH^-, use of both in the reaction results in a lower etch rate. The temperature and KOH concentration effects on the etch rate of (100) silicon are given by (Seidel, Csepregi, Heuberger, & Baumgartel, 1990) .

$$Etch\ rate = k_0[H_2O]^4[KOH]^{\frac{1}{4}} e^{-\frac{E_a}{kT}} \qquad (2.6)$$

where the etch rate is in μm/hour, the concentrations are in mol/liter, k is Boltzmann's constant, T is temperature in Kelvin, activation energy E_a=0.595 eV ,and k_0 = 2480μm/h(mol/liter)$^{-4.25}$. Also, the roughness of silicon machined by anisotropic etching is an important factor in nanoscale device fabrication. The change in roughness strongly depends on the crystallographic orientation of the silicon, concentration of KOH solution and temperature (K. Sato, Shikida, Yamashiro, Tsunekawa, & Ito, 1999). According to the research worked by Sato et al., the etched (100) plane provides the smoothest surface. Also, etched (110) and (111) plane offer good surface roughness similar to (100) plane. However, high index planes such as {210} planes, {320} planes, and {221}

planes show a rough surface in the same etch conditions of temperature and concentration. The surface roughness properties for different crystallographic orientations of silicon is independent of etching time for {100} and {111} planes but the {110} planes have greater surface roughness, which increases etching time. The concentration of KOH in the etchant is one of the parameters, which determine the surface roughness. Increasing the concentration of KOH decreases the roughness of the etched surface. However, in general, concentrations of KOH below 20wt% are not used since the etch process produces high surface roughness and insoluble precipitates, which interfere with subsequent etching and degrade uniformity in etching. Also, in order to increase surface smoothness, isopropyl alcohol (IPA) is added to the KOH solution (Zubel & Kramkowska, 2001). Futhermore, smoothness of the etched surface is deeply related to the removal of small hydrogen bubbles from the silicon surface. When a hydrogen bubbles sticks to the surface, it retards the etching reaction for produces a rough surface. The high temperature KOH etching helps to reduce the creation of the hydrogen bubbles since decreased viscosity of the etchant at high temperature allows the bubbles to dislodge easily from the surface (Dutta et al., 2011).

For 3-dimensional bulk machining using anisotropic wet chemical etching, a mask is required to prevent unwanted etching in the mask area. A variety of thin film materials can be used to mask alkali hydroxide etches. Silicon nitride and silicon dioxide are commonly used since their etch rate in the etchant is very low when compared to the silicon. The etch rate of silicon nitride deposited with Low-pressured chemical vapor deposition (LPCVD) is nearly zero and the etch rate of thermally grown silicon dioxide is around 7.7nm/min in KOH solution (Williams, Gupta, & Wasilik, 2003). Since the etch rate of silicon nitride is almost zero in KOH wet etching, silicon nitride is used as an etch mask for long time silicon etching, as is used in making a through hole. The silicon wafer that silicon nitride is deposited on is used for fabrication of a silicon nitride membrane. Also, for bulk micromachining of silicon used in this work for fabricating a nanogap device, silicon nitride film deposited with LPCVD is used as a basic etch mask as well as thermally grown silicon dioxide.

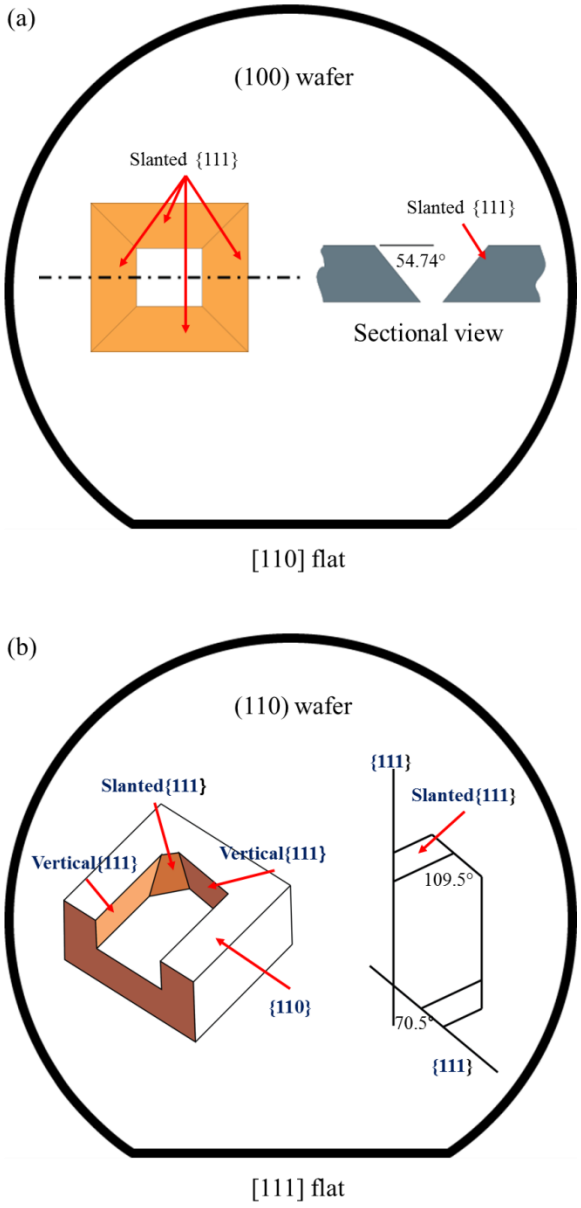

Fig. 2.7 Schamatic illustration of a silicon wafer etched by anisotropic wet chemical etchant : (a) Etched structure for (100) wafer bounded by {111} planes, and (b) Etched structure for (110) wafer having four vertical {111} planes and two slanted {111} planes.

2.4 A novel method for accurate crystallographic axis alignment

Due to the crystallographic dependence of an etched structure created using anisotropic wet chemical etching, the accuracy of mask alignment to the silicon crystallographic axis plays an important role in fabricating a device with designed patterns. A misalignment can change the etch rate of the crystal planes and cause significant facet undercuts, resulting in distorsion of the etched structures compared to the desired structures (Seidel, Csepregi, Heuberger, & Baumgartel, 1990). Generally, the major flats on substrates that specify the crystal orientation are used as a reference but the specified accuracy of a flat is ±0.5° (Ciarlo, 1992; F. Tseng & Chang, 2003). To avoid the anisotropic wet etching property, DRIE has been used for deep trench fabrication since dry etching is independent of the crystallographic axis of substrate. However, as mentioned in the previous chapter, in spite of its ability to produce structures with aspect ratios of 50:1 or better DRIE is not always attractive due to high levels of sidewall roughness and crystal damage generated by the process(B. Wu, Kumar, & Pamarthy, 2010). Therefore, we will present a novel method for accurate crystallographic axis alignment acceptable for anisotropic wet etching and report on the effectiveness of the suggested method with a deep trench, 90μm deep, 2μm wide, and with 4μm pitch fabrication on a (110)-oriented silicon wafer.

2.4.1 Optical method for grating pattern alignment

In this chapter, a new all-optical method is presented, in which gratings on a photomask are aligned to pre-etched gratings on the substrate. The suggested method uses the change of the intensity of a reflected microscope light since the reflected light intensity depends on the angular misalignment between two gratings. The change is measured with a photodetector at the end of the eyepiece lens of the mask-aligner and monitored through an oscilloscope. The accurate alignment to the substrate crystallographic axes is achieved without the need for individualized wafer marking or processing.

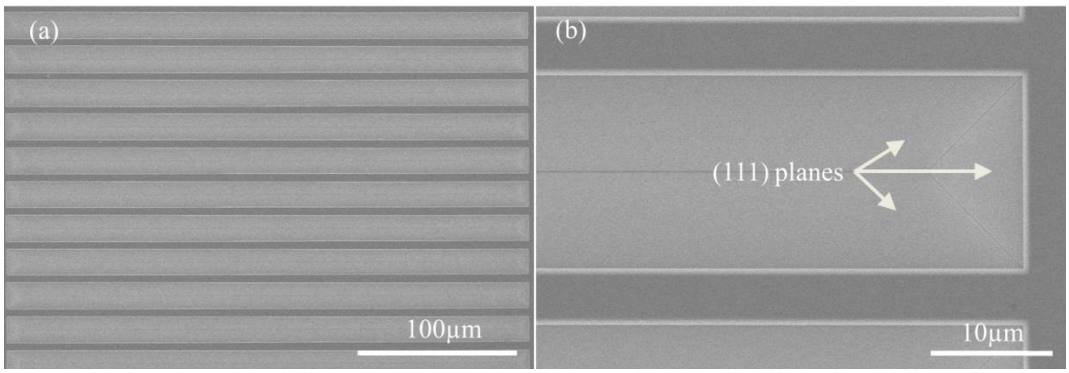

Fig. 2.8 Rectangular gratings on (100)-oriented wafer after anisotropic wet cheminal etch. (a) An overview of gratings bounded by (111) plane with 12-hour long etch using 30% KOH at 70°C. (b) Close-up view of a grating showing atomically smooth (111) planes.

For alignment of the substrates's crystallographic axes, two periodic grating patterns, one on the substrate and the other on the optical photomask, are used. The grating patterns on the substrate fabricated near the substrate periphery is defined with opticallithography. The orientation is coarsely aligned to the major flat of the substrate. After patterning, the grating is etched with an anisotropic etchant, KOH, and it is bounded by the (111) planes. The misalignment resulting from the inaccurate major flat can cause the (111) planes to show "steps" along the vertical grating sidewall (Seidel, Csepregi, Heuberger, & Baumgartel, 1990). Therefore, a long anisotropic etch is typically required to reduce the steps and to reveal the true crystal planes of the substrate used as reference for the device alignment. Since the higher Miller index planes {hkl} show high etch rates compared to (111) plane, a 12-hour long etch with 30%w.t KOH at 70°C is performed and it produces atomically smooth (111) planes shown in Fig. 2.8.

Next in the process is making sure that the grating on the optical photomask is aligned to the fabricated grating on the substrate. When the grating on the optical mask and fabricated grating on the wafer are overlapped, the grating on the optical photomask can be aligned to be parallel and alternated with respect to the fabricated patterns, as shown in Fig. 2.9. In this configuration, microscope light used in a mask-aligner is shone on the overlapped gratings and the intensity of the light which is relfected back is measured with a photodetector mounted on the

eyepiece of the mask aligner. The incident light to the overlapped gratings is reflected by the area between the (111) plane on the substrate and grating on the optical mask. The etched areas, (111) planes, on the substrate, scatter or reflect the incident light since they are non-parallel to the substrate. In case of misalignment between the gratings, the total reflected light at the photodetector is reduced due to overlapping of the normally-reflecting areas as shown in Fig. 2.9 (a). When the gratings on the optical photomask are perfectly aligned to the gratings on the substrate, the intensity of reflected light measured at the photodetector shows the maximum value, as shown in Fig. 2.9 (b). The suggested optical method for cystral alignment offers accuracy which is better than ±0.05°.

Fig. 2.9 (a) shows schematically the general case in which the gratings on the optical mask are slightly misaligned (θ < 0.5 degree) and rotated with respect to the center of the pre-etched gratings on the wafer. The relative vertical displacement of the schematic is such that the maximum amount of the normally reflecting portion of the gratings on the photomask overlap the etched gratings on the wafer, thus reflecting a maximum amount of light for this angular misalignment. One cell of the grating that is periodically repeated with pitch, P, is shown in Fig. 2.9 (c). The total area per cell that reflects light normally is $2Pl - 2W_s l + A_{overlap\_g}$, where $A_{overlap\_g}$ is the area of the etched groove that is covered by one grating in the mask. Here W_s and W_m are the width of each grating on the substrate and photomask respectively, and l is the half-length of the gratings (on the mask and the substrate). For small angles of misalignment (e.g. as θ < 0.5°), $A_{overlap}$ can be calculated as $W_m \cdot (W_s - W_m/2)/\theta$. Thus the light intensity at the photodetector is proportional to:

$$I(\theta) \propto 1 - \frac{W_s}{P} + \frac{W_m \cdot (W_s - \frac{W_m}{2})}{2P} \cdot \frac{1}{\theta} \qquad (2.7)$$

This expression is valid until the gratings on the mask can be entirely enclosed by the gratings on the wafer, i.e. for all $\theta > \theta_{min\text{-}coarse} = (W_s - W_m)/2l$. It can be shown that this $\theta_{min\text{-}coarse}$

represents the angular misalignment of the gratings on the wafer with respect to the crystallographic axes of the substrate. Hence the initial coarse alignment guarantees an angular alignment better than alignment schemes using only the wafer major flat ground by the manufacturer.

Once the photomask and the substrate are aligned with coarse alignment, the gratings on the optical mask are aligned to the substrate, as illustrated by the general case in Fig. 2.9 (d). The approximate area overlapped during coarse alignment can be calculated as a function of the angular misalignment, θ. If h is the height of the portion of optical mask outside of the pre-etched silicon groove, then, $h = l\tan\theta$. The overlapped area is $A_{overlap\_p} = (l/2)h \approx (1/2)l^2\theta$. From Fig. 2.9 (b), the maximum reflected light will be registered on the photodetector when the gratings on the optical mask and the wafer align, because the gratings on the optical mask are aligned inside the pre-etched gratings on the wafer. Therefore, the normalized light intensity can be obtained by total reflecting areas on the optical mask and wafer by subtracting the overlapping area, $A_{overlap\_p}$,

$$I(\theta) \propto 1 - \frac{l}{2m} \cdot \theta \qquad (2.8)$$

where m is the distance between gratings on the optical mask and those on the wafer.

The overlapped area is proportional to the misalignment angle and the length of the gratings. To maximize the signal for the photodetector, the grating length should be close to the field of view of the microscope and the large number of gratings. The accuracy of angular alignment during fine alignment would typically be limited by the signal-to-noise ratio at the photodetector.

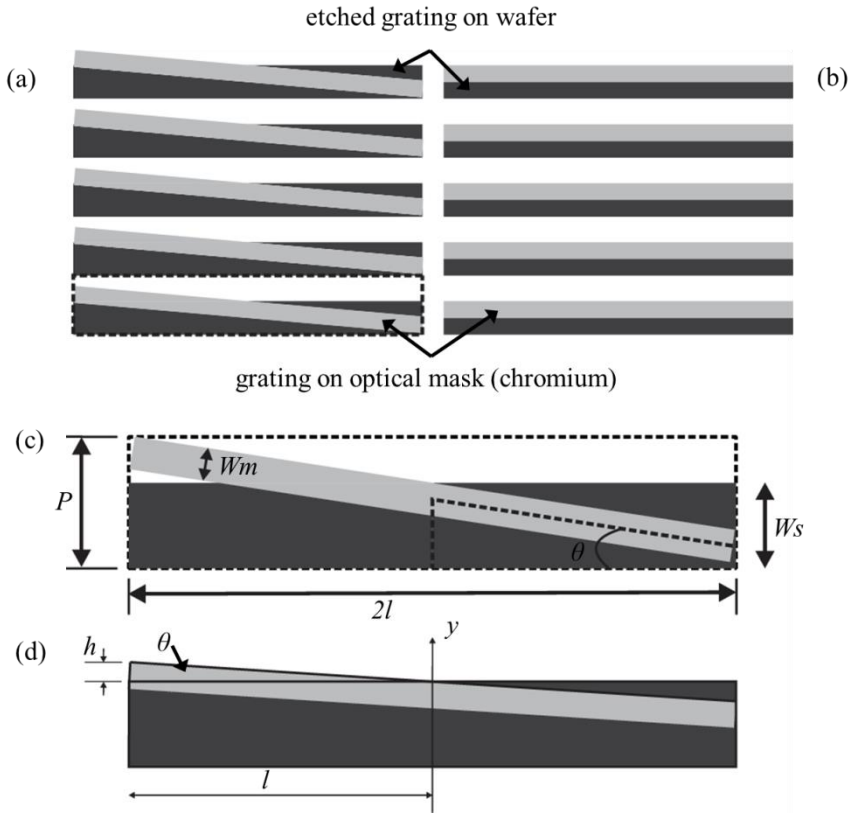

Fig. 2.9 Schmatic illustration of alignment of grating on wafer and optical mask. (a) Misaligned mask to the etched grating. (b) Aligned mask to the crystallographic axes. (c) Single grating cell describing the parameters of the grating. (d) Close-up view of the overlapped area for calculation for fine alignment.

2.4.2 Fabrication of high aspect ratio trenches

High aspect ratio trenches are fabricated to illustrate the accuracy of the suggested alignment method with a (110)-oriented silicon wafer. To investigate the relationship between misalignment and trench depth, a series of gratings are designed as shown in Fig. 2.10.

The fabrication process starts with depostion of silicon nitride film which serves as the etch mask to define the set of gratings on the 300mm thickness silicon substrate. The silicon nitride film is deposited using low-pressure chemical vapor deposition. The gratings, 300μm length, 10μm width with a 20μm pitch, are patterned on the (110)-oriented substrate by a photolithographic method and the major flat is used as a reference for coarse alignment. The

patterns developed are transferred onto the 300nm silicon nitride thin film using reactive ion etching. The trasnferred grating patterns were etched using 30% KOH at 70°C for 12 hours. Typically, the etched grating had a wider width than the design width since the coarse alignment results in misalignment. After the KOH etch, the silicon nitride film used as an etch mask for producing the gratings was selectively removed by hot phosphoric acid etch.

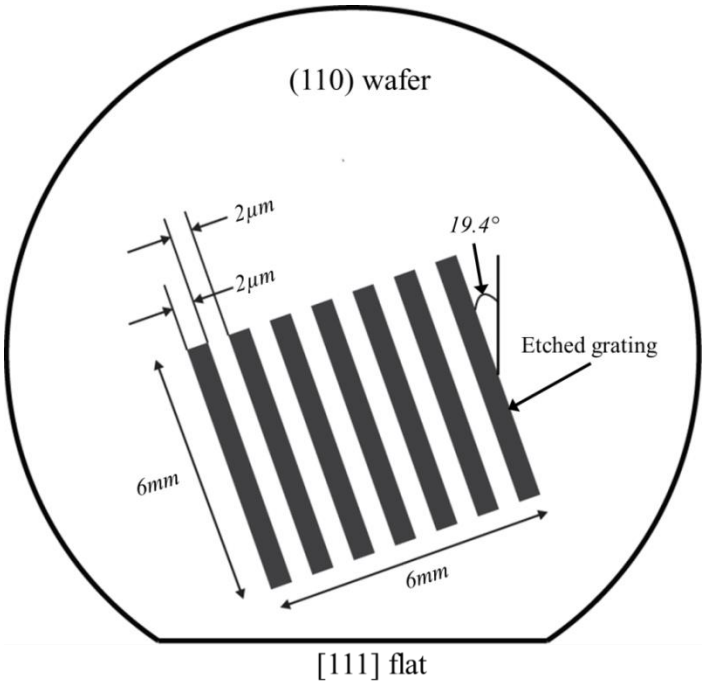

Fig. 2.10 Grating pattern for deep trenches on (110)-oriented wafer with [111] major flat

The alignment method mentioned in the previous chapter is applied. The same photomask used to define the substrate grating is aligned with respect to the pre-etched grating on the substrate. At this stage, the mask is accurately aligned to the crystallographical axes of the substrate, measuring maximum intensity of reflected light. Two alignment marks on the photomask are lithographically transferred to the substrate. In our case, we transferred alignment keys for a GCA i-line optical stepper to the left and right of the substrate. After the alignment, a 300 nm low-stress silicon nitride film is deposited on the (110)-oriented substrate to serve as the

etch mask during deep trench etching using anisotropic wet chemical etching. For fabricating the high aspect ratio trenches, periodic arrays of a rectangular trench structure with a width of 2μm, a length of 6mm, and a pitch of 4μm are patterned. The patterned trenches are aligned to a set of (111) planes that are vertical to the (110) wafers. The pattern is transferred to silicon nitride film using RIE, and the trenches are etched using 30% KOH at 70°C. The trenches fabricated are shown in Fig. 2.11. The Fig. 2.11 (a) is top view of the total number of 1500 deep trenches, 6mm long, 2μm wide and 50μm deep. The sectional view of fabricated trenches as shown in Fig. 2.11(c) shows the exellent uniformity of the etch depth.

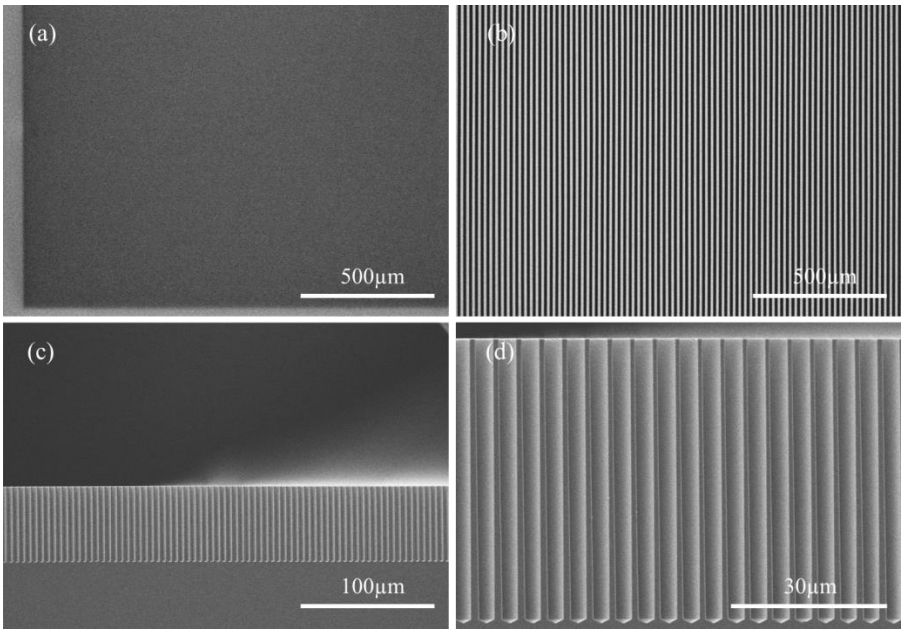

Fig. 2.11 Fabricated array of deep trenches on (110)-oriented wafer. (a) Top view of the 1500 trenches. (b) Close-up view of (a). (c) Cross-sectional overview of the trenches. (d) Close-up view of (c).

2.4.3 Analysis of undercut effect in deep trench fabrication

For high aspect ratio structures, the etch rate of high Miller index plane {hkl} with respect to the (111) plane and the crystal alignment are critical parameters for an accurate

nanoscale device. In this chapter, we will analyze the relationship between the depth of trench and misalignment with a series of gratings designed as shown in Fig. 2.12. Each grating is 0.05° rotated successively with respect to the central grating set, up to ±1° in both the clockwise and conuter-clockwise direction. The grating in the center is designed to be aligned with [111] crystal direction. The designed pattern is used to analyze the function explaining the relationship between possible etch depth and misaligned angle. The grating misalignment to the [111] crystal direction results in severe undercut. Since the patterned trenches have the long length, even infinitesimal misalignment is observed by gemometrical analysis of etched grating. With the suggested method, we have achieved the least undercut of the grating in the middle, indicating that the alignment accuracy is better than 0.05°.

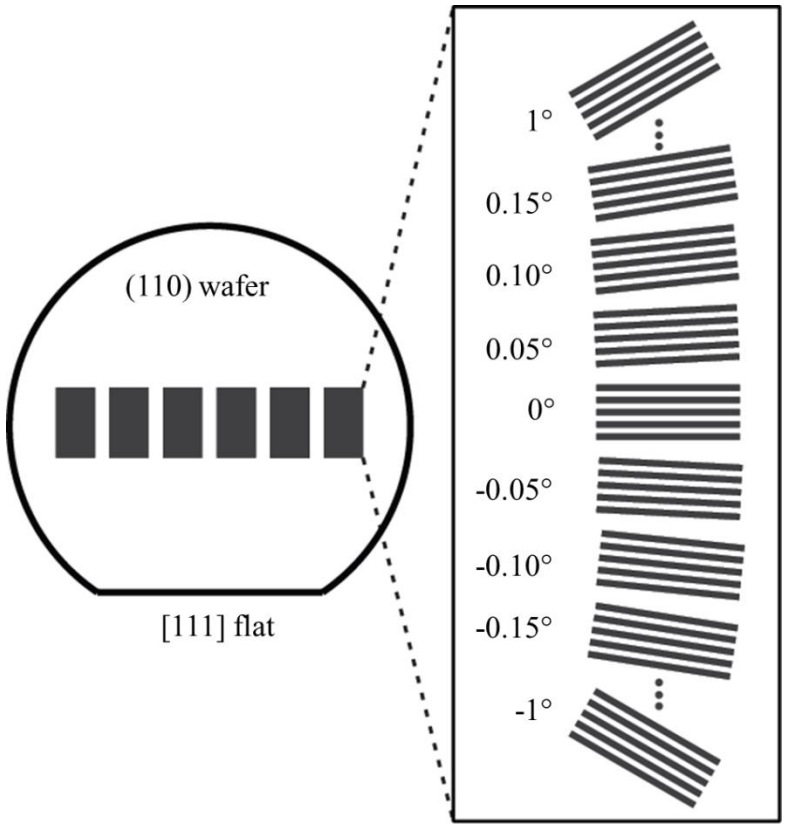

Fig. 2.12 Printed series of grating aligned along the pre-etched [111] direction on (110) - oriented wafer. Each grating is 0.05° rotated successively up to ±1°.

The relationship between alignment accuracy and the achievable aspect ratio of deep trenches created by anisotropic chemical wet etching is calculated. The upper bound of the allowable misalignment for fabrication of the deep trenches is presented in Fig. 2.13 (a). The distance between underetch fronts, "*b*", is determined by the misalignment angle (θ) to the [111] direction and original interval of gratings, "*a*". Therefore, the distance of undercut fronts resulting from misalignment is defined by

$$b = a/\sin\theta \qquad (2.9)$$

The etch rate of the high Miller index plane that is defined undercut front in Fig. 2.13(a) depends on the misalignment (Ciarlo, 1992; Seidel, Csepregi, Heuberger, & Baumgartel, 1990). For calculating the allowable depth of trenches, let α be the etch rate of the (110) plane and β be etch rate of the high Miller index planes {hkl} for a given KOH concentration and temperature. Then the relation between the etch rate can be written as

$$\beta = c \times \alpha \qquad (2.10)$$

where the *c* is a proportional constant determined experimentally by fitting the measured etch depth of trenches. In this study, the constant "*c*" is measured to be 1.6 for 30% KOH at 80°C as shown in Fig. 2.13 (b), which is close to the reported value (Zubel & Kramkowska, 2004). The etch rate determined for high Miller index planes, "*β*", and the distance of undercut fronts, *b*, are used to determind the etch time. Then we can calculate the etch depth, d using.

$$d = \frac{t_{hkl} \times \alpha}{2} \qquad (2.11)$$

where t_{hkl} is the etch time of high Miller index planes.

Fig. 2.13 (b) shows the relation between maximum trench depth and misalignment angle to the crystal axes. The reason that trench depth is determinded by etch time of the {hkl} plane is

that the etch rate of {hkl} planes is faster than the typical etch rates of (110) and (111) planes. For an initial spacing of 2μm between the trench walls, "*a*", a misalignment angle of the trench wall to the actual silicon (111) planes must be less than 0.05° for etching the 90μm deep trench. Also, the etching of the (111) plane in KOH solution determines the limitation of the trench depth. The green line in Fig. 2. 13 (b) describes the effect.

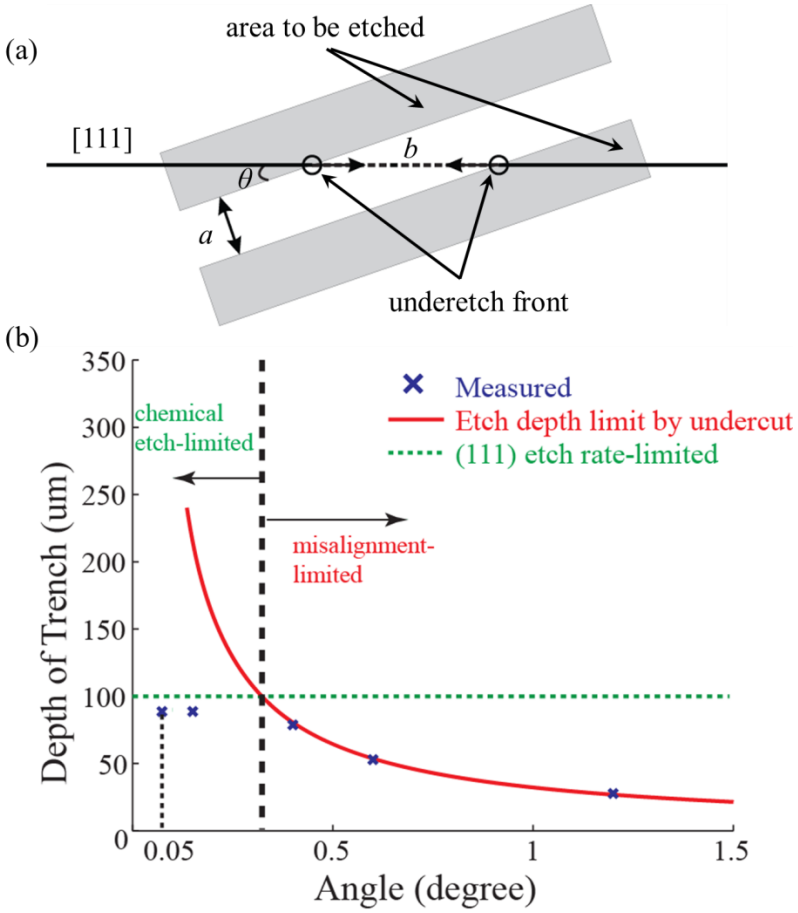

Fig. 2.13 The achievable maximum trench depth for a 2μm trench width and a 4μm pitch gratings by misalignment and (111) etch rate. (a) Schamatic illustration of {hkl} plane underetch front along the [110] direction with misaligned gratings. (b) Etched depth as function of misalignment angle and non-zero (111) planes etch rate.

From Fig. 2.14 (a) showing the top of etched trench, we see the approxiamtely 600nm undercut over a 80μm trench depth etch using 30% KOH at 70°C. Also, Fig. 2.14 (b) showing the

bottom of the fabricated trench indicates the (111) plane step that is visible in the SEM image. The existence of (111) plane step describes the misalignment of trench patterns to the crystal direction (Seidel, Csepregi, Heuberger, & Baumgartel, 1990). Since the step height is too small to measure with the SEM, the misalignment would be very small. The thickness of wall of etched trench is 600nm at the top (Fig. 2.14 (a)) and 1.4μm at the bottom (Fig. 2.14 (b)).

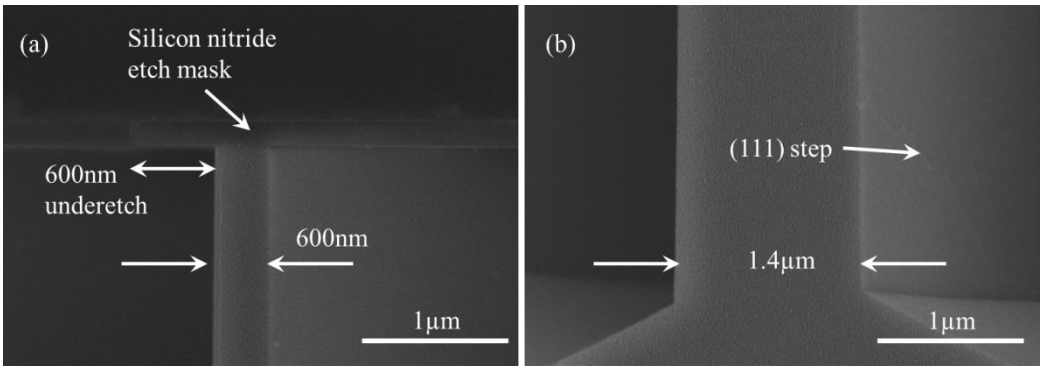

Fig. 2.14 SEM images of 80μm depth trench for analyzing misalignment. (a) Top of the wall. (b) Bottom of the wall.

3. NANOGAP DEVICE FABRICATION

As mentioned in Chapter 1, diverse types of nanogap devices act as platforms for integrating nanoscale materials in a system and manipulating these materials. For example, the semiconductor nanowire that is integrated into the metallic electrodes of nanogap devices has been used in various applications including sensors (Cui, Wei, Park, & Lieber, 2001; Favier, Walter, Zach, Benter, & Penner, 2001; J. S. Wright et al., 2010), LEDs (Duan, Huang, Cui, Wang, & Lieber, 2001; Gudiksen, Lauhon, Wang, Smith, & Lieber, 2002), and photodetectors (Kind, Yan, Messer, Law, & Yang, 2002). Nanogap devices that consist of two metallic electrodes facing each other have been fabricated with various methods as presented in Chapter 1. Some methods used metal wires and nanowires. The metal wires are broken by mechanical pulling, and the nanowires are machined with FIB or are broken by electromigration to form a nanogap. Other methods have used electrochemical deposition to reduce lithographically defined metallic gap sizes to the nanoscale.

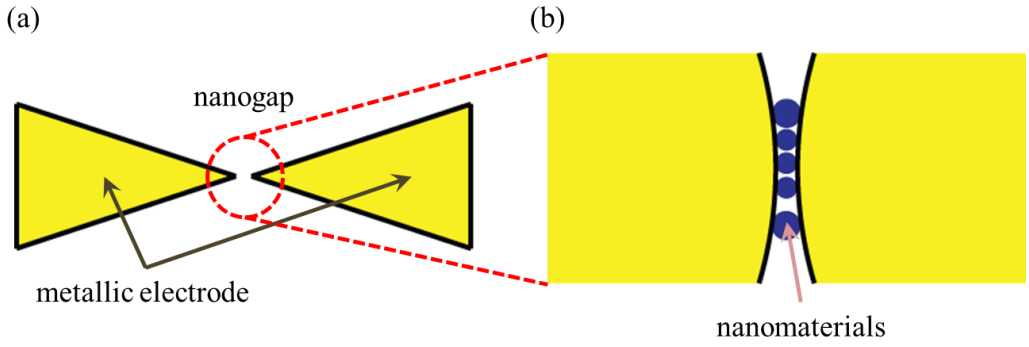

Fig. 3.1 Schematic illustration of nanogap formed by two sharp vertexes. (a) Nanogap device consisted of two planar metallic electrodes. (b) Close-up view of (a) showing rounded tips on which a few of nanomaterials are attached.

The parameters that should be considered for developing and fabricating a nanogap device in order to realize an effective platform are size of the gap, sharpness of the electrode tip, and electrical and physical isolation of the electrodes. However, the research performed has

focused on reducing the gap size between the metallic electrodes. The nanogap size is an important parameter for understanding electrical properties of a single molecule or nanoscale materials, but other parameters such as radius of curvature of the tip and electrical isolation have to be considered for effective integration of nanomaterials into the nanogap device. When a new design and fabrication process of a device are developed, the radius of curvature of the nanogap device and electrical isolation of the electrodes from the surface of a substrate, as well as the gap size, have to be considered. If the radius of curvature of the nanogap device is not atomically sharp, the device might not guarantee integration of a single molecule. In this situation, the nanogap device offers enough space to attach a few or several single molecules as shown Fig. 3.1 (b). Since the self-assembly method has been widely used to integrate nanoscale materials to the metallic nanogap in an uncontrolled manner, the radius of curvature of the nanogap device is the unique controlling parameter for integration of the single molecule or single nanomaterial between two metallic electrodes. Generally, a nanogap device has two vertices facing each other in order to offer a sharp tip, minimizing the radius of curvature as shown Fig. 3.1 (a). However, in the nanoscale, it is hard to say that the tip of the nanogap device is atomically sharp. The geometric characteristics of the device depend on the fabrication process developed and the resolution of the applied lithography approach. For example, the method using electrochemical deposition for reducing initial nanogap size may not allow zero dimensional sharp tips.

Another parameter to be considered is the electrical and physical isolation of the metallic electrode from a substrate. Most fabricated nanogap devices are a planar type onto a substrate. With this configuration, it is difficult to achieve the physical and electrical isolation for minimizing the leakage current during measurements. Specially, when the nanogap device is used as a platform to measure electrical properties of a nanomaterial integrated into electrodes of the nanogap device, the leakage current cannot be ignored since typical nanomaterials exhibit high Mega or Tera ohm resistance (Y. F. Lin et al., 2008; Y. Lin et al., 2010).

In this chapter, a novel nanogap device that is suspended on the substrate and consists of two atomically sharp tips will be presented. The device is fabricated using a 3-dimensional bulk machining approach on a silicon on insulator (SOI) wafer. The SOI wafer is suitable for the fabrication of the suspended nanogap and a 3-dimesional bulk machining approach allows forming the very sharp vertex at the end of the electrode.

3.1 Device design

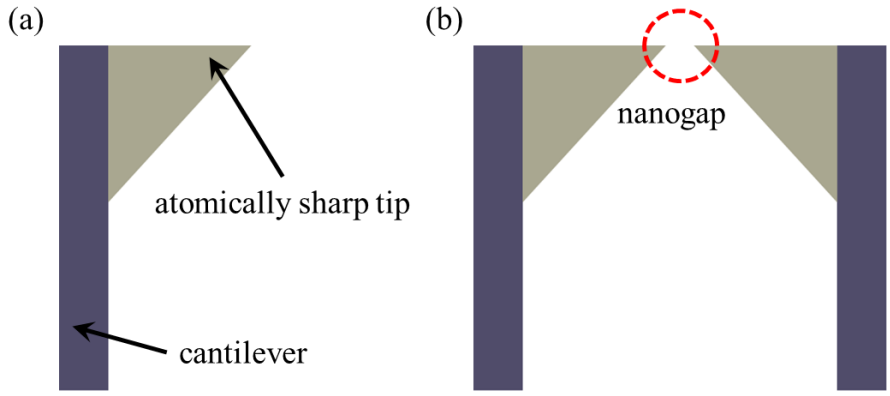

Fig. 3.2 The design concept of the nanogap device presented in this work. (a) Typical AFM probes consisted of a cantilever and an atomically sharp tip. (b) The arrayed AFM probes facing each other with a nanometer gap.

The design concept of the suspended nanogap device presented in this work starts from a cantilever with a sharp tip such as AFM tip. When the two cantilevers, having atomically sharp tips, are arrayed facing each other with a nanometer gap, the configuration allows for the nanogap device as shown in Fig. 3. 2. Since the tip for the AFM probe was developed by Binnig in 1986, much work has been done to achieve the atomically sharp tip measuring for atomic resolution with atomic force microscopy (Wolter, Bayer, & Greschner, 1991). The resolution, including the lateral resolution of the AFM, depends deeply on the radius of the tip integrated on the cantilever, and various fabrication methods for the tip have been developed based on the silicon substrate (Boisen, Hansen, & Bouwstra, 1996; J. Li, Xie, Xue, & Wu, 2012; X. Li, Han, Bao, & Yang,

2007). The fabrication methods have been very well established and have been stabilized with 3-dimensional bulk micromachining.

The suspended nanogap device in this work is designed to be compatible with 3-D bulk machining with anisotropic wet etching. As such, the SOI wafer used as a substrate shown in Fig. 3. 3 consisted of 5μm top silicon, 4μm buried silicon dioxide, and a 630μm handle wafer. The SOI wafer is useful for fabricating the suspended nanogap device because the buried oxide is easily removed by HF solution without damage to the silicon nanogap tip at room temperature. The 5μm top silicon ensures physical stability of the tip of nanogap after fabricating the suspended nanogap device. The top silicon is a (100)-oriented wafer and the wafer flat is in the <110> direction. The 4μm silicon dioxide offers enough space to minimize the leakage current when the device is used as a platform to measure electrical properties of integrated nanomaterial between the two sharp tips. Also, the silicon dioxide can be used as an electrical insulator between the top silicon and the handle wafer, and it acts as a mechanically strong base for holding the silicon nanogap device.

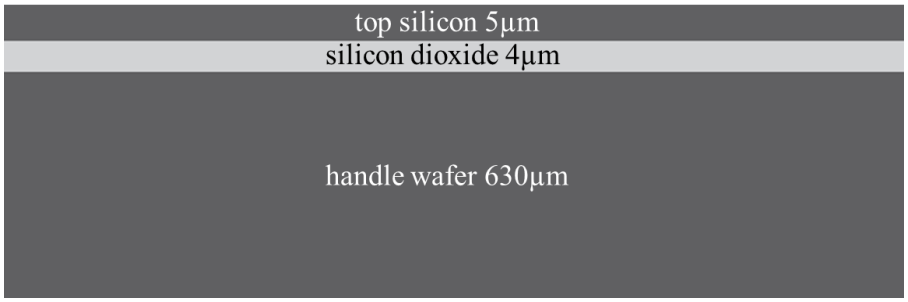

Fig. 3.3 Schematic illustration of SOI wafer for fabricating the suspended nanogap device

In order to use the anisotropic wet etching property, the devices designed are aligned to the (100) direction as shown in Fig. 3.4. When “edge 1” is simultaneously etched by anisotropic etchant, two {111} planes are exposed, and the planes bind the etched shape since the etch rate of the (111) is much slower than the (100) plane. The two {111} planes forming a vertex of a

triangle shape allows fabrication of atomically sharp tips. After performing etching of “edge 1”, “edge 2” is etched in the [100] direction, and the nanogap device is fabricated. In this work, the width of the electrodes is 120μm to 250μm, and the length is 150μm to 250μm for various configurations. The designed and fabricated size of the electrodes offers feasibility and stability for landing a tungsten probe onto the electrode surface. Furthermore, an in-situ experiment for understanding ion-migration mechanism for growth of a dendrite-like atomically sharp tip between metallic electrodes needs a large size of electrode since the wire connection on the electrodes is required instead of installation of the tungsten probe. Therefore, for the experiment work, a 500μm by 500μm electrode is designed and fabricated.

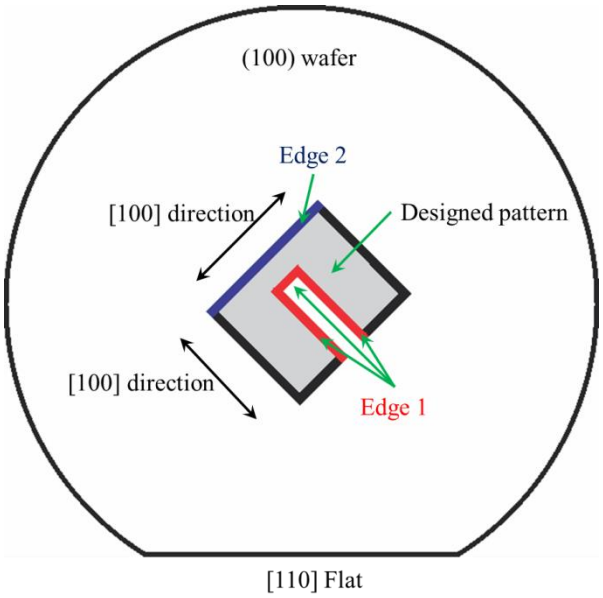

Fig. 3.4 Schematic illustration of aligning designed nanogap device

3.2 Process development

The device fabrication using 3-dimensional bulk machining approach needs various fabrication processes. Generally, the approach requires many steps of lithography, etching and

deposition for fabricating designed devices as mentioned in Chapter 2. In this work, conventional optical lithography, low-pressure chemical vapor deposition (LPCVD) to deposit the silicon nitride layer, thermal oxidation of silicon to form the silicon dioxide layer, and KOH anisotropic etching are applied for fabrication of the silicon nanogap device. These processes have been widely adapted to fabricate devices in MEMS and NEMS, and their usefulness, effectiveness, and efficiency have been proved through much research.

As mentioned in Chapter 2, although the optical lithography approach shows less resolution and critical dimension than electron beam lithography and other types of nonconventional lithography such as nanoimprint, soft lithography, and AFM probe lithography, the approach is compatible with high volume production and reproduction since the optical mask covers the entire wafer at one time. However, repeated lithography could accumulate misalignment errors and could affect the final the device dimension. To overcome the limitation of lithography resolution for fabrication of the nanogap device, a unique double-layer etch mask is suggested in this work. Although the process developed for the nanogap device requires lithography to be used 3 times, the main accuracy and uniformity of the device is determined in the first use of lithography when applying the suggested double-layer etch mask. The mask for the first lithography step has all patterns necessary to determine the final nanogap device. Since the entire pattern is printed with one mask, the misalignment error is not a considered factor in the fabrication. The accuracy of aligning a pattern with a different mask is no better than the accuracy of the pattern on the mask. The second and third lithography steps are performed to form an etch window for local etching of the silicon dioxide layer in order to expose silicon, and the silicon is etched with anisotropic etchant, KOH.

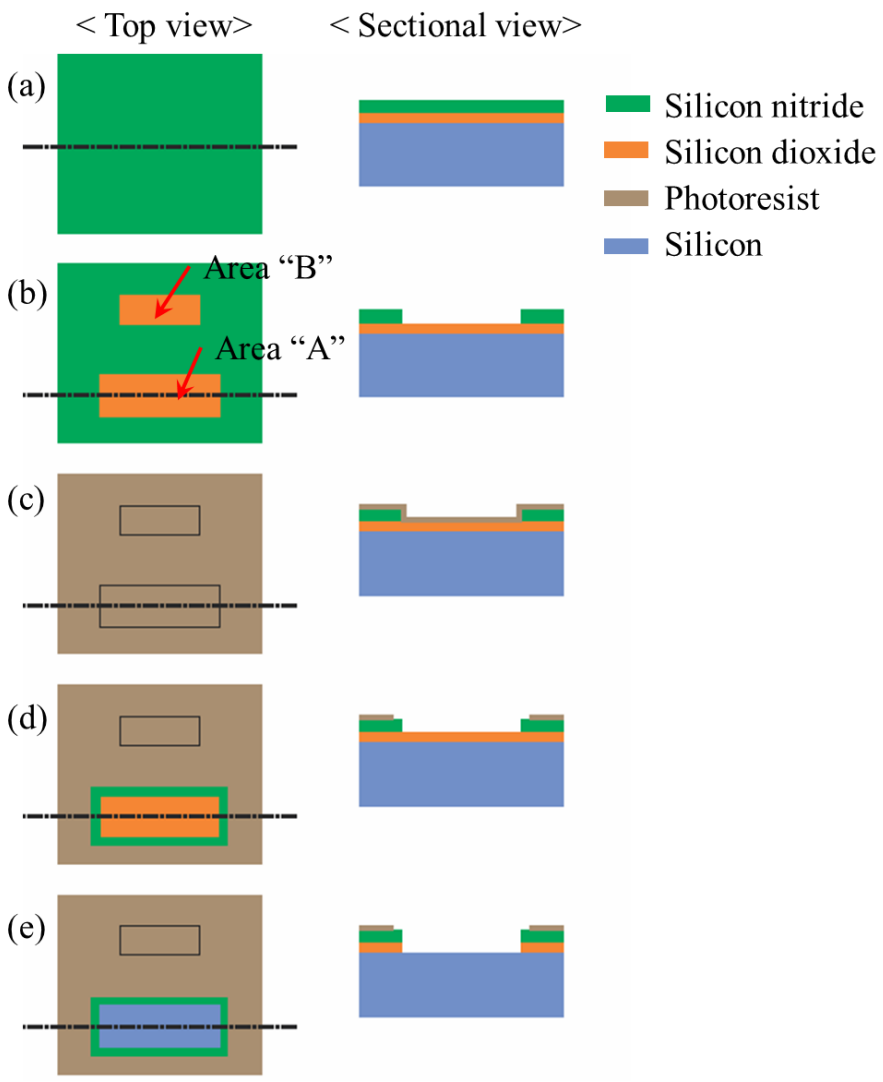

Fig. 3.5 Schematic illustration for applying unique double-layer etch mask in fabrication

Fig. 3.5 shows an example of using the double-layer etch mask for fabrication. First of all, as shown in Fig. 3.5 (a), the process starts with a silicon wafer on which silicon dioxide and silicon nitride are deposited. The silicon nitride is patterned by optical lithography with a mask and etched by reactive ion etching (RIE) to define two rectangular patterns, "area A" and "area B", as shown in Fig. 3.6 (b). After silicon nitride etching, silicon dioxide in the "area A" and "area B" is exposed. In this configuration, we can just expose silicon in "area A" without etching silicon oxide in "area B" by second lithography as shown Fig. 3.5 (c) and (d). The photoresist

pattern formed is used as the etch mask for etching silicon dioxide in buffered oxide etchant (BOE). Since the silicon nitride film is also used as the etch mask for the silicon dioxide etch with BOE, the accuracy of the second lithography alignment which forms onto the silicon nitride layer, is not critical as shown in Fig. 3.5 (d). The required accuracy of conventional optical lithography is sufficient. Finally, Fig. 3.5 (e) shows the exposed silicon layer, and the "area A" can be etched anisotropically with KOH or other anisotropic etchants after removing the remaining photoresist. As the silicon dioxide in "area B" also can be used as an etch mask for anisotropic etching using KOH etchant, the "area A" is the only area to be etched. Furthermore, when the etching of "area B" is required, the third lithography step and the same etching process is performed after oxidation of the whole wafer to form an etch mask in etched "area A". The advantages of using the double-layer etch mask is that the accuracy and the uniformity of the fabricated device are deeply dependent on the resolution of the first lithography and not on subsequent misalignments of the lithography.

The silicon nitride film is deposited onto the silicon dioxide layer for use as an etch mask for anisotropic KOH etching and to define etching area for fabricating a nanogap device in this work. Since the etch rate of the silicon nitride layer in KOH etchant is near zero, it can be utilized as an etch mask for long time silicon etching with thin film layers (Williams & Muller, 1996). The deposition of silicon nitride film is performed by the LPCVD approach. The LPCVD offers high-purity deposit, good process control and good economy over competing deposition techniques, such as atmospheric pressure CVD (APCVD), rapid thermal CVD (RTCVD), atomic layer deposition (ALD) and plasma enhanced CVD (PECVD) (Stoffel, Kovacs, Kronast, & Muller, 1996) . Also, silicon nitride film deposition with the LPCVD method shows the lowest etch rate in KOH etchant (Williams, Gupta, & Wasilik, 2003). In LPCVD, dichlorosilane (SiH_3Cl_2, DCS) or silane (SiH_4) are typically used as a source of silicon, and ammonia (NH_3) is utilized as the nitrogen source for silicon nitride deposition at a temperature between 700 and 900°C (Olson, 2002). Generally, after deposition of a silicon nitride layer on a silicon substrate,

mechanical stress remains in the layer due to the thermal mismatch between the deposited silicon nitride layer and the substrate (French, Sarro, Mallee, Fakkeldij, & Wolffenbuttel, 1997). In nanoscale device fabrication, since the residual stress of the deposited silicon nitride could result in deflection of the fabricated device, low stress silicon nitride deposition is required and the film is realized by controlling deposition parameters such as temperature, total gas flow, and gas flow ratio (Gardeniers, Tilmans, & Visser, 1996). Table 3.1 shows the parameters for deposition of the low stress silicon nitride film in this work.

Table 3.1 conditions for deposition of low stress silicon nitride

Parameters	Value
Pressure	135 ± 25 mTorr
Temperature	850±10°C
DCS flow rate	300±15 sccm
NH3 flow rate	60±3 sccm
Deposition rate	70±10 Å/min

The silicon dioxide layer also is used as an etch mask for KOH etchant in this work. Although the etch rate of the silicon dioxide is higher than silicon nitride, its use is feasibility for growth and etching. There are many methods for growing the silicon dioxide layer on the silicon substrate, but the thermal oxide wet approach is applied in this work, as the silicon dioxide grown by this approach is denser and etches more slowly than chemical-vapor-deposited oxides (Williams, Gupta, & Wasilik, 2003). Thermal oxidation of silicon is easily achieved by heating the wafer to high temperature, typically 900 to 1200°C, in water vapor. A bubbler containing DI water connects to a wafer furnace and it supplies vaporized water at 97°C. In this work, the furnace used is a 6 inch cylindrical quartz tube, which has three-zones to maintain temperature

uniformity. In the wet approach, the chemical reaction occurring at the silicon surface is as follows :

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \qquad (3.1)$$

In the oxidation process, silicon is consumed and the resulting oxide expands during growth. The ratio of silicon thickness converted to the final oxide thickness is 46 percent. For example, when 100nm of oxide has grown, 46nm of silicon will be consumed. The etch rate of the silicon dioxide in KOH is 7.7nm/min in 30% KOH at 80°C (Williams & Muller, 1996). In order to determine thickness of silicon dioxide used as the silicon etch mask, the oxidation is performed at 960°C for different times.

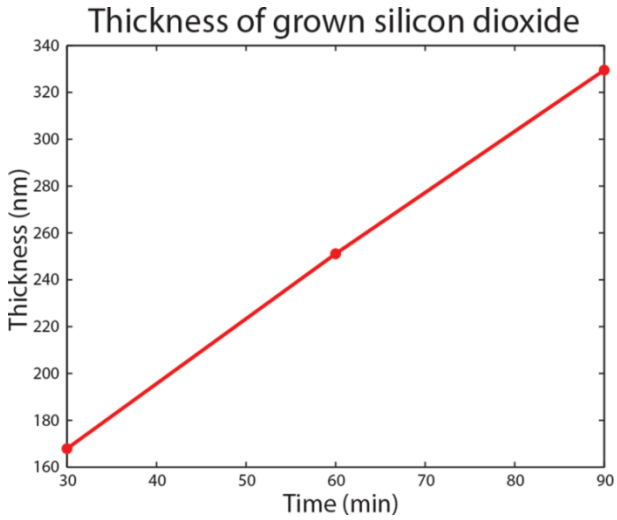

Fig. 3.6 Thickness of silicon dioxide grown at 960°C in a quartz furnace

The Fig. 3.6 shows the thickness of the silicon dioxide grown measured by an ellipsometer. The grown thickness is 167.9nm, 251.1nm and 329.5 nm for 30min, 60min, and 90min of oxidation respectively. In this work, KOH etching is performed twice for fabricating the nanogap device, and each etching time is 20min and 60min in 30% KOH at 60°C. For 20min etching, 30min of oxidation is performed, and for 60 min etching, 60min of oxidation is

performed to create an etch mask. After silicon anisotropic etching of silicon, the sacrificial silicon dioxide layer is removed by BOE or HF etching at room temperature. The one reason for using the silicon dioxide layer as an etch mask is that the sacrificial layer is easily etched in BOE or HF without any kind of complex process involving vacuum, heating and gas. Although it is possible to etch silicon nitride layer at atmosphere pressure, the etchant, 85% phosphoric acid, has to be heated at 170°C for a few hours.

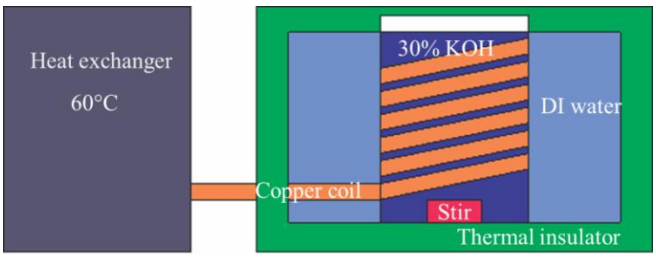

Fig. 3.7 Schematic illustration of KOH etching system for uniform temperature and concetration distribution of KOH solution. The system is composed of a heat exchanger, thermal insulator, DI water, quartz beaker, and copper coil.

As mentioned in the previous chapter, the nanogap device in this work is fabricated by three dimensional (3D) bulk micromachining using the anisotropic etching property of the single crystal silicon. When the silicon is etched by KOH etchant, the etch rate depends greatly on the weight ratio of the KOH solution and the operation temperature. Therefore, the deviation of the solution concentration and temperature of the KOH contained in a quartz beaker induces non-uniformed etch profile in the silicon etching. The non-uniformed etch rate results in different nanogap sizes in a same substrate since the etching of silicon for specified time determines the size. In order to reduce temperature and concentration distribution in the KOH solution during this work, the temperature of the KOH is controlled by a heat exchanger, and a stirrer that rotates with 300rpm is used in the etchant as shown Fig. 3.7. The heat exchanger helps to maintain the constant temperature of the KOH solution through a copper coil and the container containing DI water. Also, the KOH solution is thermally closed to the environment by a thermal insulator for

protecting against heat exchange. In this configuration, we achieve the uniform 0.31μm/min silicon etch rate with 30% KOH solution at 60°C.

3.3 Device fabrication

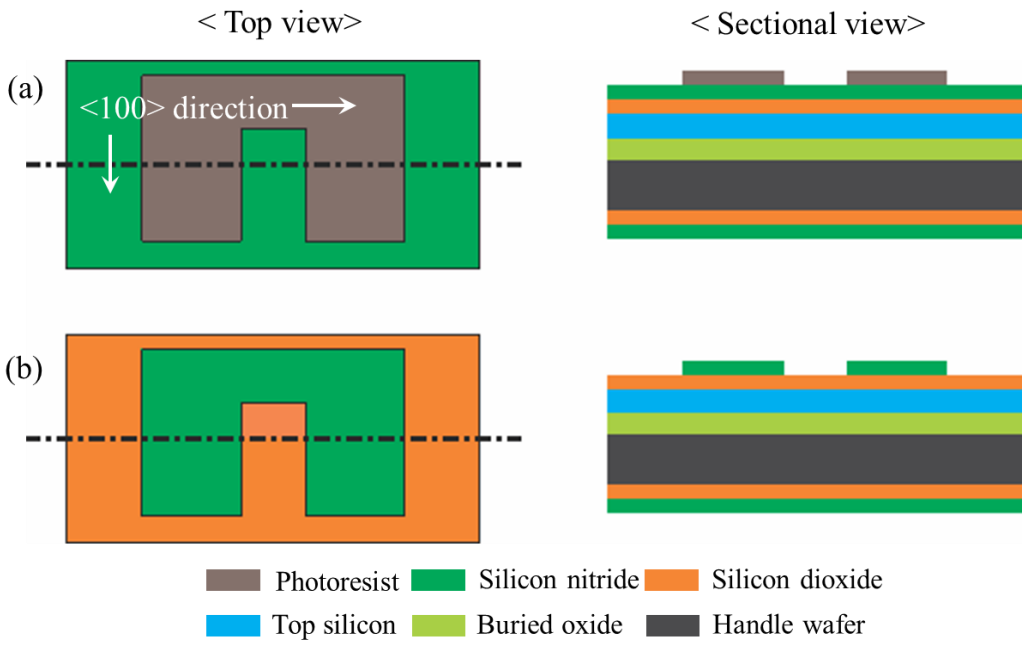

Fig. 3.8 Top view and sectional view of the first patterning of the nanogap device. (a) First lithography step for silicon nitride etching. (b) Etched silicon nitride for defining structure of the nanogap device fabricated by anisotropic wet chemical etching.

The suspended nanogap device fabricated on the SOI wafer with a (001) crystal orientation is mainly processed using three steps of conventional optical lithography and two sequential steps of anisotropic wet chemical etching. First of all, a substrate composed of a 5μm thick top silicon layer, a 4μm thick buried silicon dioxide layer and a 600μm thick handle wafer is thermally oxidized to form a 250nm thick silicon dioxide layer on both the top silicon and handle wafer. A 300nm thick low stress silicon nitride film is then deposited. The two layers, low stress silicon nitride and silicon dioxide film, serve as KOH etch masks in the subsequent fabrication process.

In the first step of fabrication, silicon nitride film is patterned by a stepper as shown in fig 3.8 (a). A GCA i-line optical stepper is used in this step. The lithography process follows standard process flow as mentioned in Chapter 2. Firstly, the wafer is cleaned with a solution of sulfuric acid and hydrogen peroxide to remove organic contaminants, and dehydration is performed at 300°C for 5min to remove moisture on the surface of the substrate. Hxamethyldisilzane (HMDS) for improving adhesion of the photoresist on the surface of the wafer is applied by vaporization in a heated vacuum chamber. The photoresist is applied by a manual spinner, and the thickness is decided to serve as an etch mask following 300nm silicon nitride etching. The photoresist coated wafer is baked at 100°C for 1min to drive off solvents in the photoresist. After exposure, the wafer is developed to dissolve the exposed part of the photoresist. The remaining photoresist acts as an etch mask following silicon nitride etching with RIE using the gas containing fluorine. In this work, tetrafluoromethane gas (CF_4) is introduced to the RIE system for etching the silicon nitride film. The silicon nitride pattern defines the overall device structure as shown in Fig. 3.8 (b) and the pattern is aligned in the <100> direction of the top silicon.

The second lithography step is performed to create an etch-window in area “A” as shown in Fig. 3.9 (a). Due to the use of the same mask in the second lithography and third lithography steps, image reverse lithography is performed. In this work, the photoresist used is AZ5214 E, and the photoresist allows positive and negative patterns. Although the lithography process is the same as positive pattern lithography, negative patterning requires extra baking for 2min at 120°C and extra UV exposure on the photoresist without a mask after first exposure. The patterned photoresist serves as an etch mask for etching the silicon dioxide layer of area “B” in BOE as shown in Fig. 3.9 (a). In this configuration, the silicon nitride film also serves as an etch mask for the silicon dioxide layer. So the accuracy of the alignment does not affect the etch profile like using the double-layer etch mask described in previous chapter. The etch rate of the thermally grown silicon dioxide is around 100nm/min in 1:5 BOE, and the etching is performed for 2min

40sec at room temperature. After silicon dioxide etching, the top silicon is exposed as shown in fig 3.9 (b).

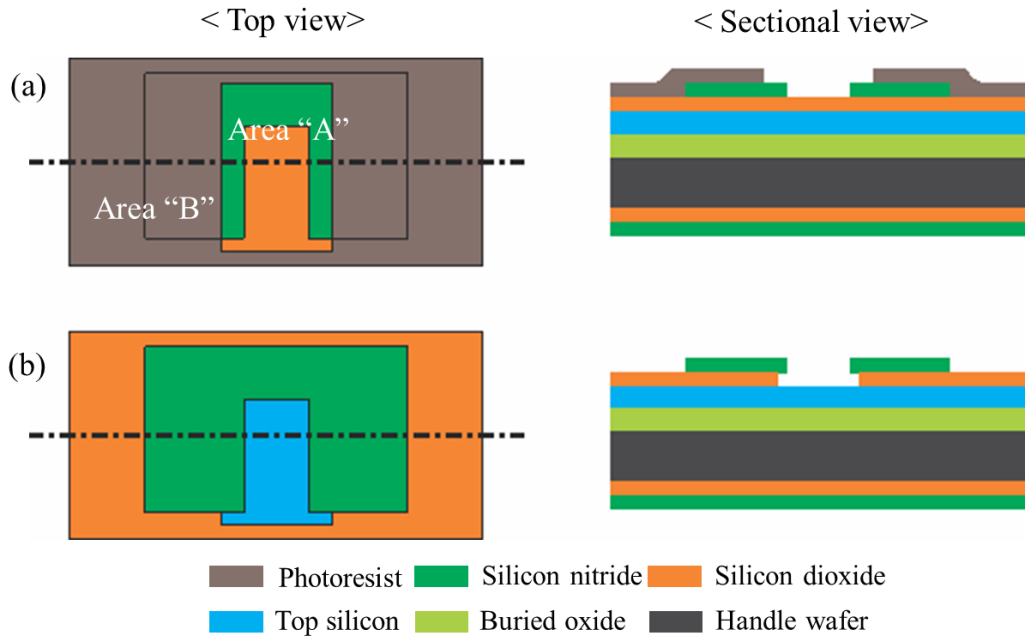

Fig. 3.9 Device fabrication process for first etch window. (a) Photoresist pattern defining silicon oxide etching area with BOE. (b) After etching of silicon dioxide in area "a", top silicon is exposed for first anisotropic etching.

The exposed top silicon is etched first by KOH etch, and the etched profile is shown in Fig. 3.10 (a). Due to the anisotropic characteristics of the KOH etching, the etched surfaces are {111} and {100} planes. The {111} planes are self-terminated at the angle of 54.74° with respect to the (001) plane, while the {100} planes are undercut underneath etch masks, silicon nitride and silicon dioxide, until the KOH etch is manually stopped. In order to etch all of 5μm thick top silicon in the height direction, the etching is performed for 20min at 60°C in 30% KOH. In this configuration, the etch rate of {100} planes is 0.31μm/min.

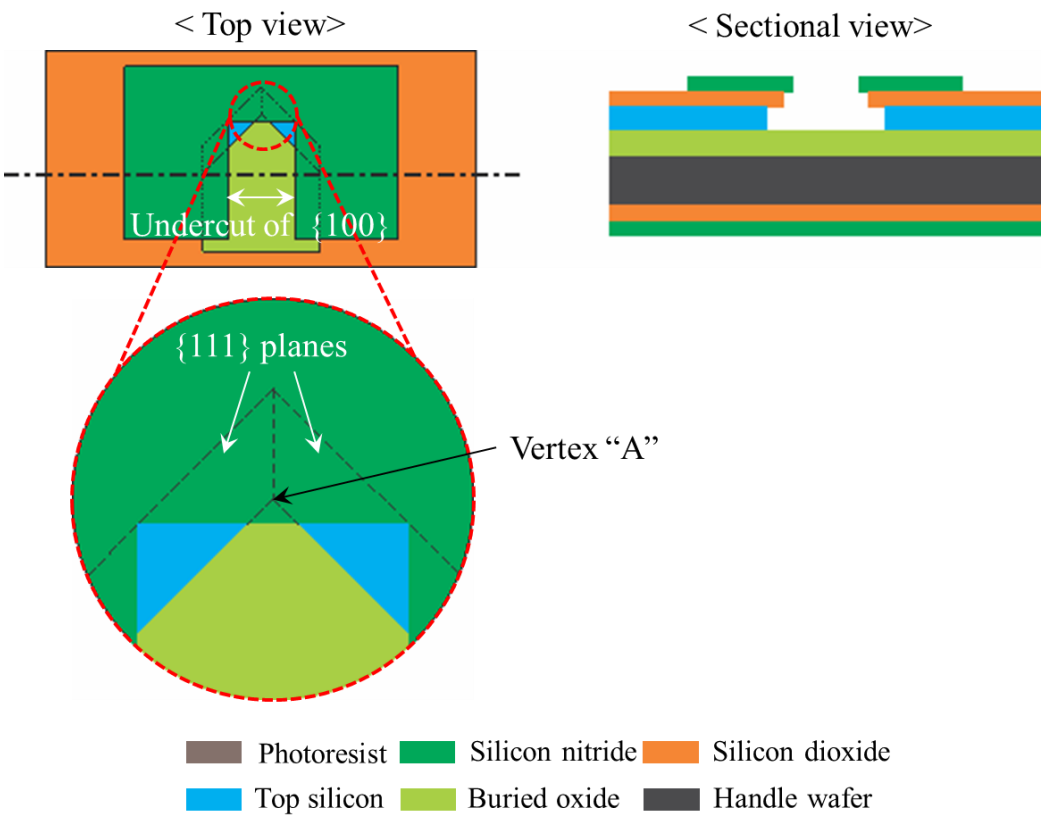

Fig. 3.10 Etched profile of first KOH etch. The silicon etching is stopped at the boundary which is formed by {111} planes and manually stopped in the <100> directions by removal of the etchant.

The next process is oxidation of the silicon surfaces, {111} planes and {100} planes, exposed first by KOH etching. The silicon dioxide grown is thermally oxidized and the layer serves as an etch mask for a second KOH etching. The silicon dioxide layer is grown in a furnace that has a three zone control system at 960°C for 60mim and has a 250nm thickness.

The third lithography step conducted after silicon oxidation is performed to form an etch-window for second silicon etching in the process of nanogap fabrication, as shown in Fig. 3.11 (a). The patterned photoresist and silicon nitride film are used as etch masks for silicon dioxide etching. The etch of the uncovered silicon dioxide layer by photoresist using BOE for 6min at room temperature allows exposing the top silicon for the second anisotropic chemical wet etching,

as shown Fig. 3.11 (b). The remaining silicon dioxide film under the photoresist protects the first etched silicon surface during the second KOH etch.

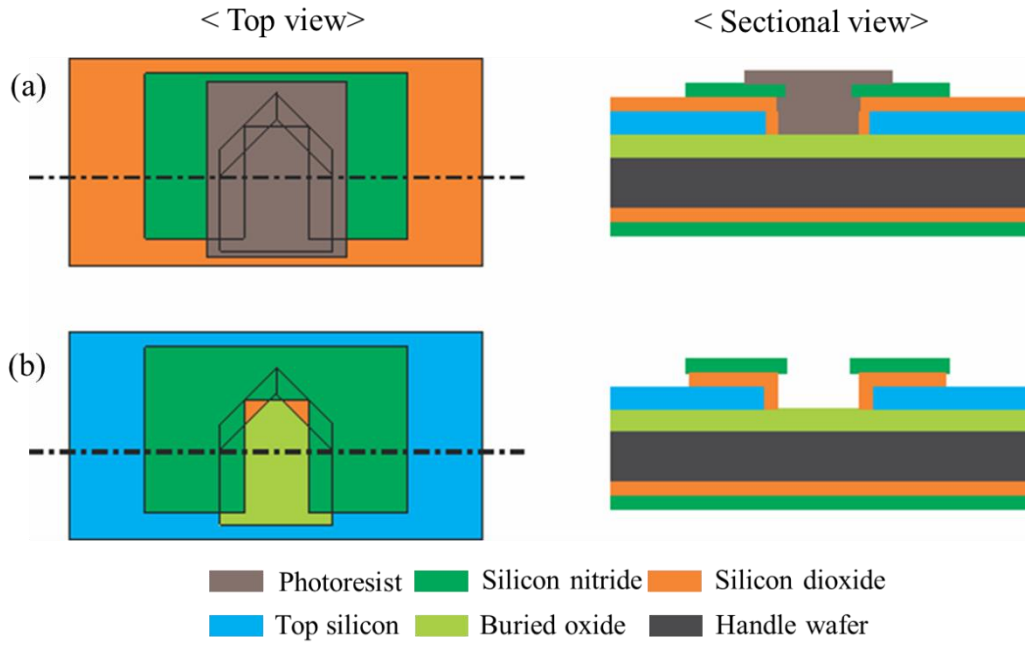

Fig. 3.11 The process of the third lithography step defining the etch-window for the second silicon etching. (a) Third pattern by an optical lithography (b) The exposed silicon after silicon nitride etching with BOE.

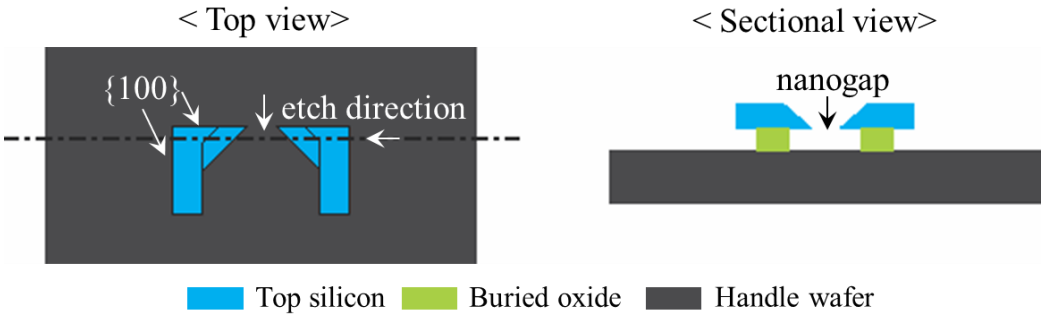

Fig. 3.12 The profile of the fabricated nanogap device. The device layer is perfectly suspended from the handle wafer, and the buried oxide physically supports the electrical pads.

The exposed silicon from the previous step, silicon dioxide etching, is etched in 30% KOH at 60°C for 60min. This process, which is the final silicon etch step, allows for formation of

a nanogap between two silicon cantilevers. Fig. 3.12 shows the etch direction and etched profile. In this step, the exposed silicon is not only etched but also undercut in the [100] direction. The undercut is terminated when the etching of the {100} plane meets the vertex "A" formed by two {111} planes. Fig. 3.10 shows the vertex. The nanogap size is determined by the amount of undercut etching in the <100> direction as shown in fig 3.14. Since the {111} planes are formed at 45° with respect to the [100] direction, the relationship between the amount of undercut, *k*, and nanogap size is given by Eq. 3.2.

$$nanogap\ size = 2 \times k \qquad (3.2)$$

where *k* is the amount of over etching and distance between a vertex on line "b" and line "c" on which etching is stopped.

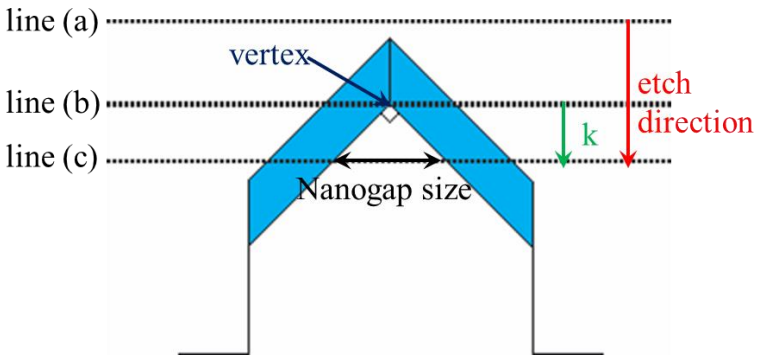

Fig. 3.13 The relationship between nanogap size and undercut in the [100] direction.

After fabricating the nanogap device based on the SOI wafer, the sacrificial silicon nitride film is removed with 85% phosphoric acid. Since the silicon is etched in the phosphoric acid, thermal oxidation is performed to protect the fabricated nanogap (van Gelder & Hauser, 1967; Williams, Gupta, & Wasilik, 2003). The silicon nitride etching using 85% phosphoric acid is performed for 5hr at 170°C. In the final step, the buried oxide is etched in 48% HF for 3min. The removal of buried oxide results in the suspended nanogap from the SOI handle wafer, while the

electrical pad is supported by buried oxide, which offers electrical insulation as shown in Fig. 3.12. The typical nanogap size formed with this fabrication method ranges between 10 nm and 80 nm as shown in Fig. 3.14.

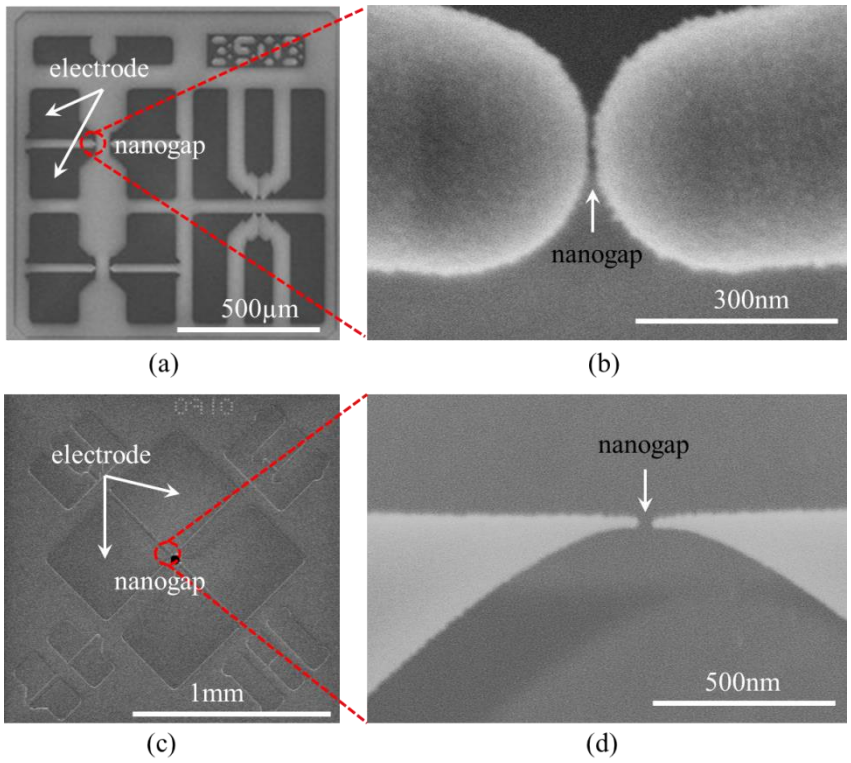

Fig. 3.14 Scanning electron microscope images of various fabricated nanogap devices. (a) and (c) overall device image. (b) and (d) close-up of tips of nanogap device

The gap is further reduced by depositing silicon nitride and evaporating metal layers over the tips forming the nanogap. The deposition of the silicon nitride film on the nanogap device ensures device insulation as well as reduces gap size. Metal deposition on the silicon nanogap device results in the electrodes for various applications of the nanogap device. The deposited metals are zinc, nickel, gold, and platinum for measuring tunneling current and for nanomaterial growth using ion migration between the two tips (details in following chapter). Specially, the deposited zinc is used to grow a zinc oxide quantum dot between two sharp tips (details in following chapter). Also, a gold deposited nanogap device could be used as a platform for

measuring single molecular electrical properties using the self-assembly method. Furthermore, organic conductive materials including pentancene and rubrene are thermally evaporated on the tips.

3.4 Tip sharpening of nanogap device

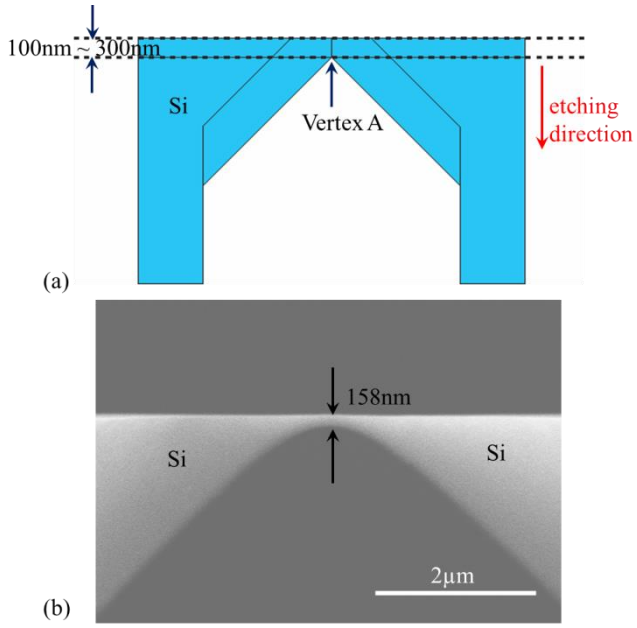

Fig. 3.15 Second silicon etching for tip sharpening with low temperature silicon oxidation. (a) The schematic illustration for etching stop and remaining silicon. (b) SEM image of the device resulting from intentionally stoppping the second KOH etch.

To reduce radii of curvature, two methods are applied in this work. The edge consisting of the two {111} planes allows ideally atomically sharp tips, but the radius of curvature of the fabricated device is 100nm to 300nm, due to the process including the second oxidation step for forming a silicon etch mask and the second silicon etching. The first method uses a low-temperature thermal oxidation process with the fabricated silicon nanogap device. The second method applies ion-migration for atomically sharp tips on a metal deposited nanogap device. The strong local electric field across metal tips facing each other causes the metal ion migration in the form of dendrite-like growth at the cathode (the details in following chapter).

The silicon tip sharpening using low-temperature oxidation suggested by Marcus in 1990 has been widely used in AFM tip fabrication (Folch, Wrighton, & Schmidt, 1997; Resnik, Vrtacnik, Aljancic, Mozek, & Amon, 2003b), silicon needle arrays (Gesemann, Wehrspohn, Hackner, & Mu?ller, 2011; Roxhed, Gasser, Griss, Holzapfel, & Stemme, 2007), and silicon field emitters (Kanemaru, Hirano, Tanoue, & Itoh, 1996). The mechanism mainly depends on the oxidation stress configuration at low temperatures, 900~1050°C and the silicon consumption in the silicon dioxide growth process. At low temperatures, the growth rate of silicon oxide is not uniform for the curvature since stresses are induced while at high temperatures above 1100°C. The stresses are released due to the decreasing of the viscosity of the oxide, which allows oxide flow. The stresses concentrate at the surface at the smallest radius of curvature, and the oxidation rate is decreased at this region locally for both dry (O_2) and wet (H_2O) oxidation. Therefore, the stress concentration results in a lower oxidation rate at the tip, and a very sharp tip is formed beneath the oxide layer. After etching away the silicon dioxide enclosing the silicon tip, atomically sharp silicon tips can be obtained.

In this work, in order to apply this approach, tip sharpening with low-temperature oxidation, the second silicon etching, which is the final etching for forming the nanogap, is stopped before the remaining bridge is totally etched. The remaining thickness of the silicon bridge in the etching direction shown in Fig. 3.15 is controlled by silicon etching time in the final step, and the thickness is between 100nm and 300nm. Since the smallest radius is formed at vertex A after the anisotropic etching, when low-temperature oxidation is applied to our device configuration, the nanogap with two atomically sharp tips is formed at the position of vertex A. This is the same as in Marcus' work. In the wet and dry oxidation processes, silicon is consumed to form the silicon oxide layer, and the ratio of the silicon thickness converted to resulting silicon oxide is 46 percent. Therefore, low temperature oxidation is performed in a quartz chamber at 950°C for 30min to 1hour in order to change the remaining silicon to silicon oxide for nanoscale gap. Since the silicon oxide is grown in three directions in our configuration, the process time of

oxidation is determined by considering geometry factors as well as silicon oxide growth rate and the ratio of silicon consumption. The silicon oxide grown is removed by etching using 49% HF, and then an atomically sharp silicon nanogap is formed as shown in Fig. 3. 16. The resulting radii of the tips fabricated using the approach are about 15nm, as shown in Fig. 3.16 (a) and (b).

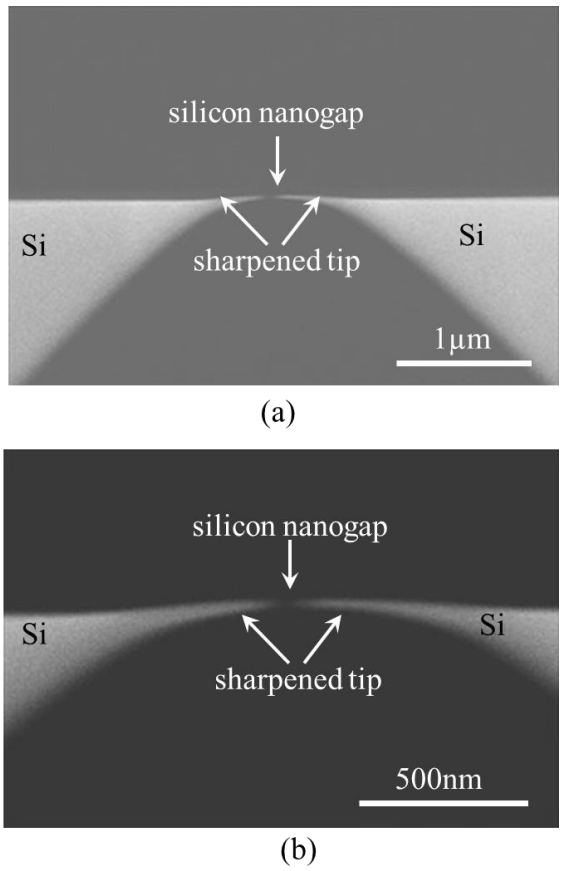

Fig. 3.16 SEM image of the fabricated silicon nanogap devices sharpened by low-temperature oxidation approach.

4. APPLICATIONS

In this chapter, the nano ZnO dot LED and the nanogap formed by field-induced atomically sharp tips will be presented as applications of fabricated silicon nanogap devices. The first application to be presented is a nano ZnO dot LED emitting visible light. The nanoscale ZnO dot is directly integrated on the metallic nanogap device through thermal Zn oxidation without any manipulations of the nanostructure. The detailed fabrication process and the study of the optical and electrical properties are presented in following section. Also, the growth of an atomically sharp tip by ion transport induced by an electric field will be discussed. The novel approach used shows tips of 1nm radius of curvature, and the tips are available for studying electrical and thermal properties of single molecules.

4.1 ZnO light-emitting diode (LED) based on nanogap device

The nanoscale light-emitting diode has received particular attention recently due to its energy saving property. Specifically, the single photon emitters have been extensively studied owing to their application in quantum computing using qubits instead of bits, networking and cryptographic key generation, and decoding. In order to create a single photon emitter, a device has to be fabricated in the nanoscale, where quantum dots and single molecules have been widely used. In this chapter, the synthesizing process of a ZnO nanostructure between a nanogap and the electroluminescence property of the fabricated device is presented.

4.1.1 The properties of ZnO for LED

In this chapter, the properties of ZnO including band gap, synthesizing methods, light emitting properties, and some native defects are presented. Since ZnO has a wide direct band gap for producing UV light, much work has been performed to apply the ZnO nanostructures in LED

devices. Various synthesizing and growth methods offer efficient ways to form wafer size with single crystal and nanoscale structures such as nanowires, nanorods, and nanodots. Furthermore, the methods for synthesizing ZnO nanostructures determine intrinsic defects such as O vacancies and Zn interstitials, which affect the optical and electrical properties.

The light emitting diode (LED) is basically a device which emits radiation by electrical energy, and it is usually fabricated with a semiconductor p-n junction. Under forward bias conditions, the diode emits light in the UV, visible, or infrared region of the electromagnetic spectrum depending on the electronic excitation. The amount of light output is directly proportional to the forward current. Therefore, when higher forward current is biased, the brightness of light is increased. The LED is used in wide applications including display backlight, communication, medical service, signage, and general illumination.

Although visible light LEDs have been in existence for some time, wide band gap semiconductors have been studied for the creation of blue and UV light. Also, semiconductor materials having a direct band gap have been studied, since these semiconductors show the radiated recombination in a first-order transition process, and their quantum efficiency is much higher than that for an indirect band gap semiconductors, where phonons are involved in the process of emitting light. The most common semiconductor of the direct band gap type is gallium arsenide (GaAs). The bandgap of this semiconductor is 1.42eV at room temperature (Krijn, 1991). Therefore, GaAs has been used for infrared radiation. However, it is well known that the GaAs LED is quite sensitive to radiation damage, so permanent degradation has to be considered in some applications such as space electronics (Khanna et al., 2000). Also, when the GaAs is grown on a Si substrate, a difference in thermal expansion coefficients between the substrate and the growing material leads to the formation of a large number of dislocations, and cracks are formed in the GaAs film during cooling. They act as a serious obstacle for epitaxial growth of high quality thin GaAs film (Bolkhovityanov & Pchelyakov, 2008) .

A semiconductor having a wide band gap compatible with the blue, white, and UV light is gallium nitride (GaN). The bandgap energy of GaN is 3.39eV at room temperature and single crystalline GaN is usually grown on sapphire substrates, since these substrates withstand elevated temperature and allow for an easy method of production (Akasaki & Amano, 1997). GaN based semiconductors have been widely used in diverse fields including piezoelectric sensors (Bykhovski, Kaminski, Shur, Chen, & Khan, 1996), gas sensors (Stutzmann et al., 2002), photodetectors in various light regions (Carrano et al., 1998; Doyennette et al., 2005; Monroy et al., 1998), field-effect transistors (Y. Ohno & Kuzuhara, 2001), as well as light emitting devices. In spite of the many merits of the GaN semiconductor, there are a few challenges to consider in practical applications. Firstly, it is difficult to grow large single crystals. GaN usually has a large lattice mismatch with the sapphire substrate, which leads to a high concentration of defects. Secondly, it is difficult to etch GaN with wet processes. Since the wet etching is widely used to realize the designed device, the applicable fabrication process is limited. Also, GaN exhibits unintentional n-type conductivity owing to nitrogen vacancies (Janotti & Walle, 2009).

In the nanotechnology field, electrical and optical properties of the ZnO nanowire, nanorod and nanodot have been widely researched. Zinc oxide (ZnO) is semiconductor showing outstanding properties of direct wide bandgap and low cost for production. In various applications, much research has been performed to replace semiconductor with ZnO (Reynolds, Look, & Jogai, 1996). Specifically, ZnO has been of interest in optoelectronics applications due to its direct band gap which is ~3.3eV at room temperature and its large excitation binding energy which is ~60meV (Ozgur et al., 2005). The large excitation binding energy assures efficient laser action at room temperature. The wide band gap allows for ZnO to substitute for GaN, and it is easier to grow high quality ZnO bulk single crystals with simple crystal-growth techniques (Look, 2001). Bulk ZnO single crystals are grown by the chemical vapor transport method, the flux method, the pressure melt growth method, and the hydrothermal method. Specifically, growth of 2 inch ZnO single crystal substrates with a hydrothermal method is reported in 2005 (Maeda, Sato, Niikura,

& Fukuda, 2005). Also, various methods for growing thin films or layers have been studied. ZnO thin films are formed by chemical spray pyrolysis (Studenikin, Golego, & Cocivera, 1998), screen printing (Hasan, Nur, & Willander, 2012), electrochemical deposition (Gu & Fahidy, 1999), sol-gel synthesis (J. Lee, Ko, & Park, 2003), solid-vapor process (Umar, Kim, Lee, Nahm, & Hahn, 2005), and oxidation of metallic zinc film (Y. G. Wang et al., 2003). The techniques have been used to fabricate LEDs, transparent conductive electrodes for solar cells, piezoelectric devices, and gas sensors. Furthermore, since the ZnO is etched in the solution of hydrochloric (HCl) acid and acetic (CH_3COOH) acid, micromachining is possible for forming patterns (Ohashi et al., 2007).

Although ZnO has many advantages including a large direct band gap, feasible growth methods, device fabrication methods, and wafer scale growth, the intrinsic defects have to be considered in nanotechnology applications. The most frequently reported defects in ZnO are oxygen vacancies and Zn interstitials. To understand the effect of the oxygen vacancies, theoretical and experimental studies have been performed (Janotti & Walle, 2005; X. J. Wang, Vlasenko, Pearton, Chen, & Buyanova, 2009). The oxygen vacancies lead to typically n-type ZnO, and it is a main factor of the broad deep-level emission. In other words, the photon energy depends on the concentration of the oxygen vacancies in ZnO. Zn interstitials are responsible for unintentional n-type conductivity, and it has been proved that they are present in very low concentrations of n-type ZnO. They are the predominant defects under Zn vapor rich environments. The Zn interstitials always donate electrons to the conduction band, thus acting as a shallow donor.

4.1.2 Synthesizing of nano ZnO dot across nanogap

A novel method for integrating a nano ZnO dot onto a silicon nanogap device to create a practical nanoscale light emitter is presented in this chapter. The suspended nanogap device is

effectively used as a platform for direct integration of the nano ZnO dot on the nanogap by Zn evaporation and thermal oxidation on the device on a wafer scale. The method does not require any additional processes for electrical connection between nanostructures and electrodes.

Generally, as mentioned in the previous chapter, diverse methods are used for synthesizing a nanostructure on a substrate. The methods provide high yield and controlled growth direction. However, the common problem with the methods is that complex and time consuming processes are required for integration of the nanostructure grown onto electrodes. Although it is possible to manipulate and position nanoscale materials using nanoscale tools such as a scanning probe microscope, this process is serial, slow, expensive, and not suitable for wafer scale fabrication. The previously studied methods for integration on the wafer scale employ electric fields (P. A. Smith et al., 2000), magnetic fields (M. Chen et al., 2003), laminar flow in microfluidic channels (Messer, Song, & Yang, 2000), and optical traps (Pauzauskie et al., 2006). Although these methods have resulted in promising results for integration of the nanomaterial on the wafer scale, it is difficult to make electrical contact between the nanostructure and electrodes. For good electrical connection, additional processes such as annealing are required. Also, the scratching process for individually separating nanostructures from a substrate would damage them.

In this work, a nano ZnO dot is synthesized by thermal oxidation followed by Zn evaporation across the tips on a nanogap device. Firstly, a 50nm thick nickel (Ni) film is thermally evaporated on the silicon tips, which are separated by less than 100nm. A 50nm thick Zn film then is evaporated without breaking the vacuum of 7×10^{-7} Torr to prevent oxidation of the deposited Ni film and to promote the adhesion of the Zn film on the Ni film. The Ni film underneath Zn serves as the electrical pad for the nanostructure formed. Fig. 4.1 shows the fabrication process for a laterally formed nano ZnO dot across the silicon nanogap device. The thickness of the evaporated film is chosen to cover the nanogap as shown in Fig. 4.2 (a) and (b). Fig. 4.1 (a) shows the SEM image of the initial nanogap device and Fig. 4. 2 (b) shows an SEM

image of the initial nanogap filled with ZnO thermally oxidized from evaporated Zn. In our experience, the total thickness of the evaporated material should be larger than the initial nanogap size to fill the nanogap with evaporated material.

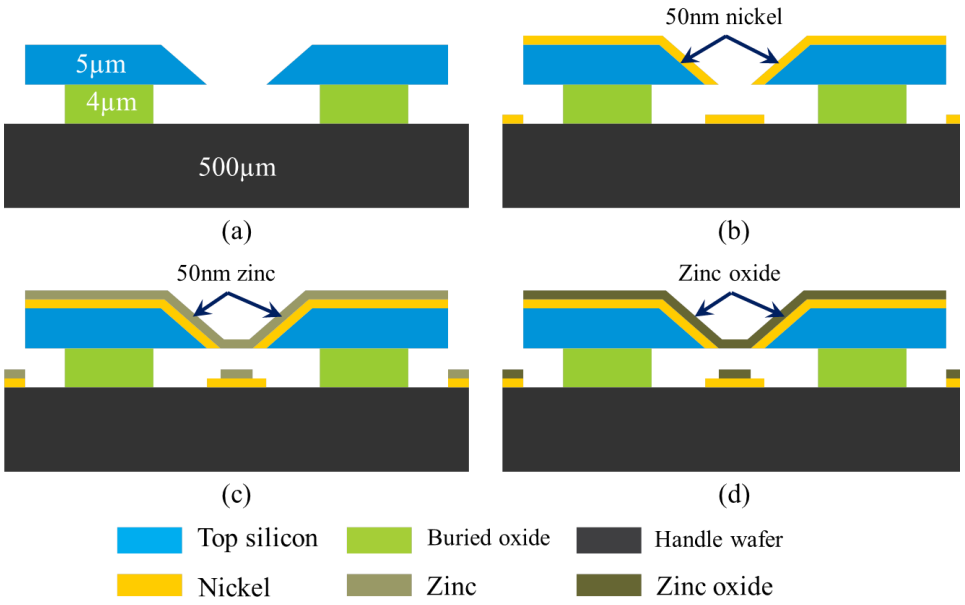

Fig. 4.1 Cross sectional views for ZnO nanodot forming process. (a) Initial silicon nanogap device. (b) Evaporated Ni on the device. (c) Evaporated Zn on Ni film. (d) ZnO formation by Zn oxidation.

After evaporation, thermal oxidation is performed at 500°C for 2 hours in a quartz tube furnace with 5 sccm oxygen gas. The quartz tube furnace is naturally cooled down to room temperature. The oxygen flow rate is controlled by a mass flow controller (MFC), and the furnace temperature is increased at 50°C/min. The oxidation process allows the entire 50nm thick Zn film to be converted to ZnO film as shown in Fig. 4. 3 (a) and (b). The ZnO film formed shows dense structures composed of very fine particles, exhibiting granular structure as shown in Fig. 4. 3 (a). The SEM image in Fig. 4.3 (b) shows the cross section of the uniform Ni layer and ZnO layer. Other researchers have reported similar oxidation methods to form ZnO with deposited metallic

Zn film (S. Cho et al., 1999; Z. W. Li, Gao, & Reeves, 2005; Nwoko & Uhlig, 1965; Rambu, Sirbu, & Rusu, 2010; Y. G. Wang et al., 2003).

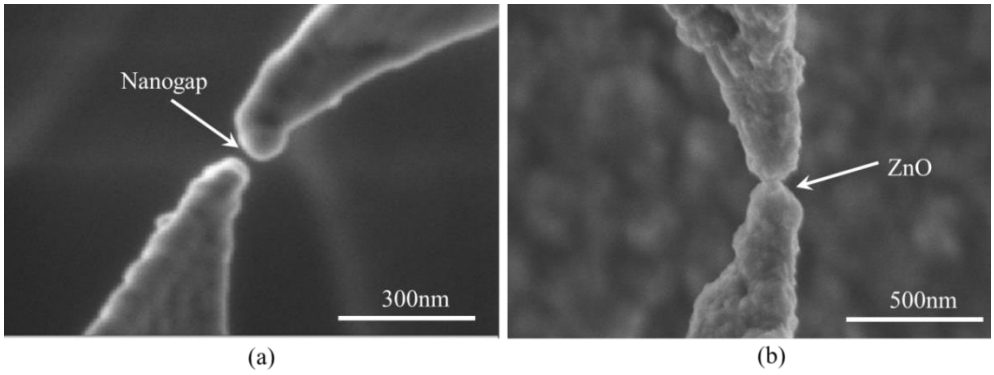

Fig. 4.2 SEM image of the fabricated nano ZnO dot. (a) Initial nanogap device. (b) The nanogap device thermally oxidized after Zn evaporation.

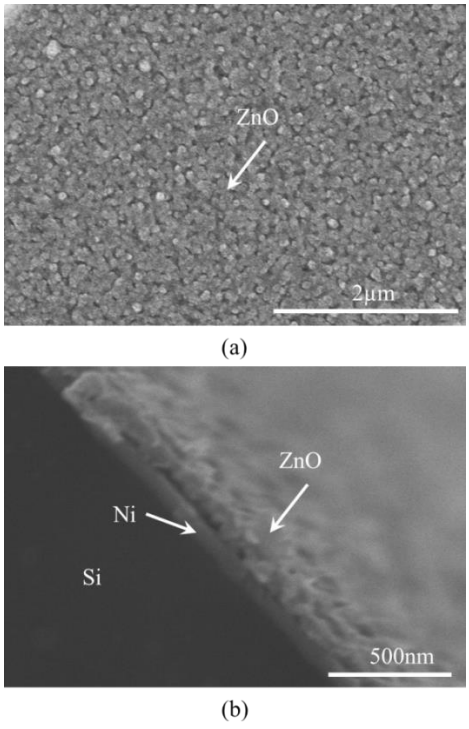

Fig. 4.3 SEM image of ZnO film. (a) Top view of dense ZnO film. (b) Cross-sectional view of Ni and ZnO layer after thermal oxidation.

To confirm conversion of Zn film to ZnO, X-ray diffraction (XRD) is performed as shown in Fig. 4. 4. The XRD pattern exhibits the peaks at 31.8°, 34.5° and 36.2°. The peaks are characteristic of the hexagonal ZnO crystalline structure (Rambu, Sirbu, & Rusu, 2010). The peak at 51.6° is the corresponding Ni under the ZnO film. The existence of the peak of Ni shows that the Ni layer is undamaged during Zn thermal oxidation together with visual SEM image shown in Fig. 4. 3 (b).

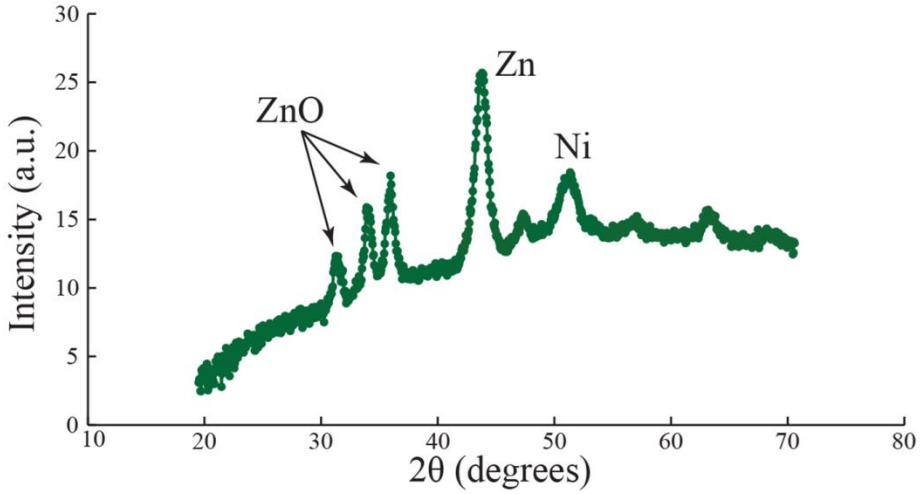

Fig. 4.4 XRD data of the ZnO formed by thermal oxidation of metallic Zn film. The data shows ZnO diffraction peaks confirming the conversion of Zn film to ZnO film, and a Ni peak underneath ZnO film.

4.1.3 Experimental methods and results for nano ZnO dot LED

The optical and electrical properties of the laterally suspended nano ZnO dot, which is directly integrated to the silicon nanogap, were studied. To understand the optical properties of the fabricated device, the spectrum of the light emitted from the nano ZnO dot with DC bias was measured and analyzed. The light intensity with respect to the applied DC bias was measured and photon rate was investigated based on the measured light intensity. Also, the I-V curve for the

fabricated nano ZnO dot LED was measured, and the property of the metal-semiconductor-metal (M-S-M) junction was investigated.

Before investigating the electrical and optical properties of the nano ZnO dot, the electrical conductivity of the metallic nanogap device and electrical leakage were analyzed. The electrical conductivity in a pad and electrical leakage between the electrical contact pad and the handle wafer were measured using an HP 4145A semiconductor analyzer right after the metal evaporation on the device in a shield chamber. The semiconductor analyzer, which has a source measure unit (SMU) is used to measure the current passing through electric pads and a handle wafer. In the test setup configuration, SMU1 and SMU2 in the semiconductor analyzer are connected to the nanogap electrode and handle wafer respectively. The output connector of each SMU establishes a triax interface in the semiconductor analyzer. In this test, the measured current level is less than 1nA, and it is recommended to use a guard conductor for low current measurements to protect losses and stray field distortion. For sensitive measurements, the guard is used to minimize the losses from signal to ground by applying the signal voltage to the guard. However in our measurements we did not use the ground, because we used two SMUs with a two port measurement configuration. In this setup, using a guard to protect the main signal is required. Fig. 4. 5 illustrates the recommended connections for low current measurement and high resistance measurement, respectively. The signal (core conductor) and guard (inner shell conductor) of the triax cable are used with a triax-to-BNC converter to connect the coaxial cable. Fig. 4. 5 shows the full setup connections with BNC interfaces and device under test (DUT) connections protected by metal guard connected configuration.

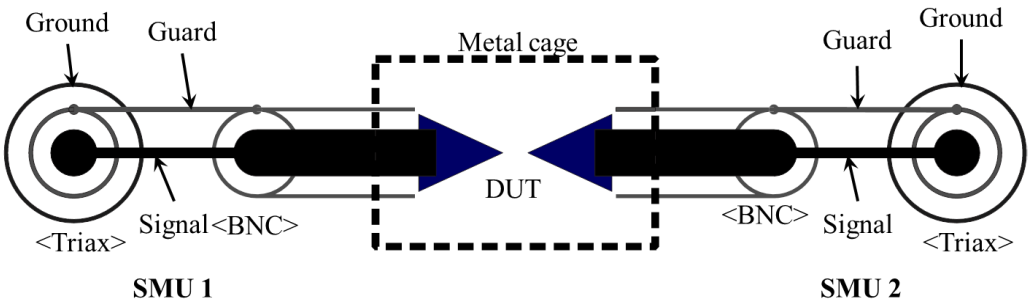

Fig. 4.5 Experimental set up for measuring low current with an HP4145 A semiconductor analyzer

A chamber consisting of a microscale 3 axes stage controlling the position of the device, four 3-axes manipulators positioning probes, and a probe establishing physical contact with the device was used for achieving an exact contact position between the probes and the electrical pad on the device, as shown in Fig. 4. 6. For measuring low current, the method using a guard shown in Fig. 4. 5 was adopted.

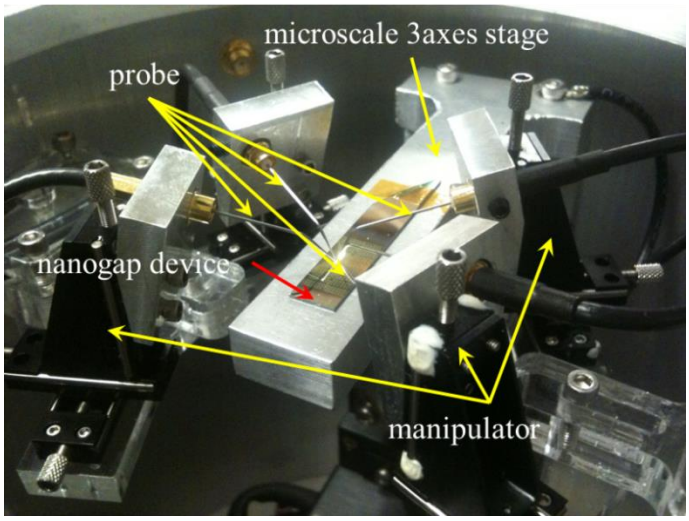

Fig. 4.6 The chamber for measuring electrical isolation and conductivity between the electrical pad and the handle wafer of the fabricated nanogap device.

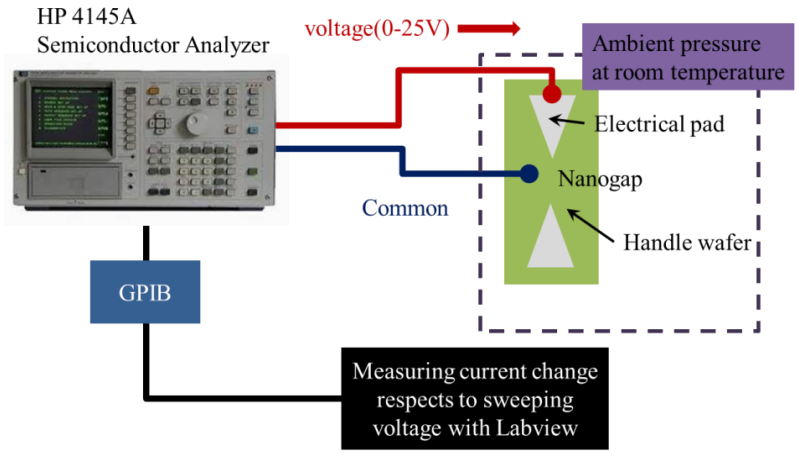

Fig. 4.7 Schematic illustration of the measurement set-up for measuring leakage current between electrical pads and handle wafer and for checking electrical isolation

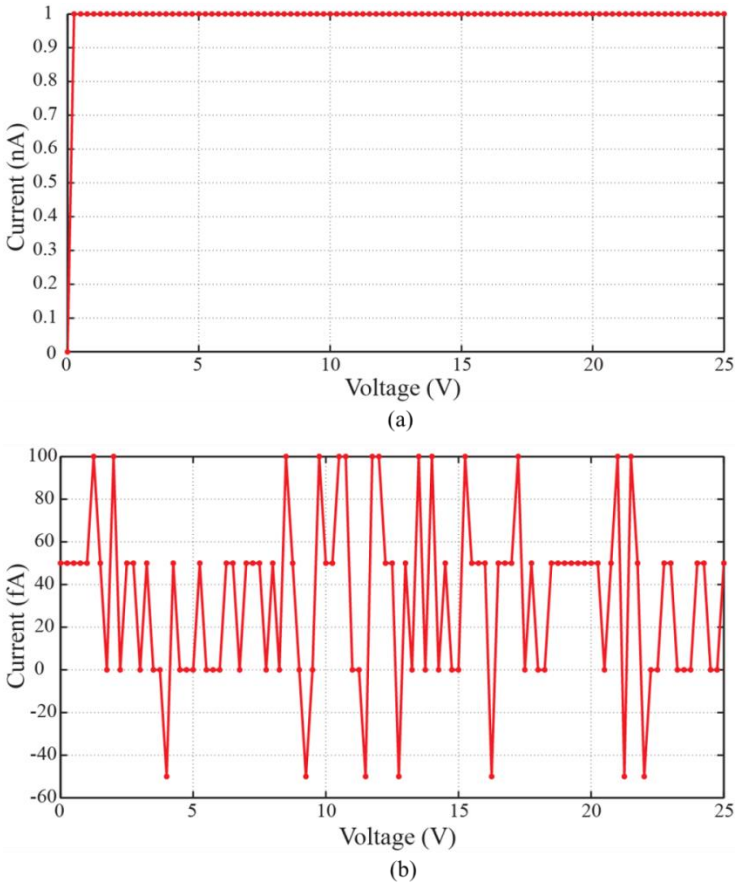

Fig. 4.8 Basic electrical properties of metallic nanogap (30nm Nickel deposited on the silicon nanogap). (a) Electrical conductivity at an electrical pad, (b) Electrical leakage between an electrical pad and a hadlewafer after blank evaporation.

In the measurement of electrical conductivity with the semiconductor analyzer, the instrument was controlled through Labview, and the measured data was saved in the computer, which was connected to the instrument as shown in Fig. 4. 7. In this measurement, voltage (0 ~ 25V) was swept as a source. The conductivity of thermally deposited 30nm Ni in an electrical pad and the leakage current between the electrical pad and the handle wafer was measured. The voltage source was increased in 0.25 V steps, and in total 101 points were measured. The current compliance was applied to protect the electrical pads from breaking owing to Joule heating. In order to measure the electrical conductivity of the deposited metal, the measurement was performed in an electrical pad. As a result, the measured current reached the compliance current as shown in Fig. 4. 8 (a) and the leakage current was 100 femto ampere (fA) as shown in Fig. 4. 8 (b). Fig. 4. 1 shows the electrodes are separated by more than a few μm of air resulting from undercut etching of the buried oxide, which ensures very good electrical isolation. Therefore, most of the current flows though the nanogap.

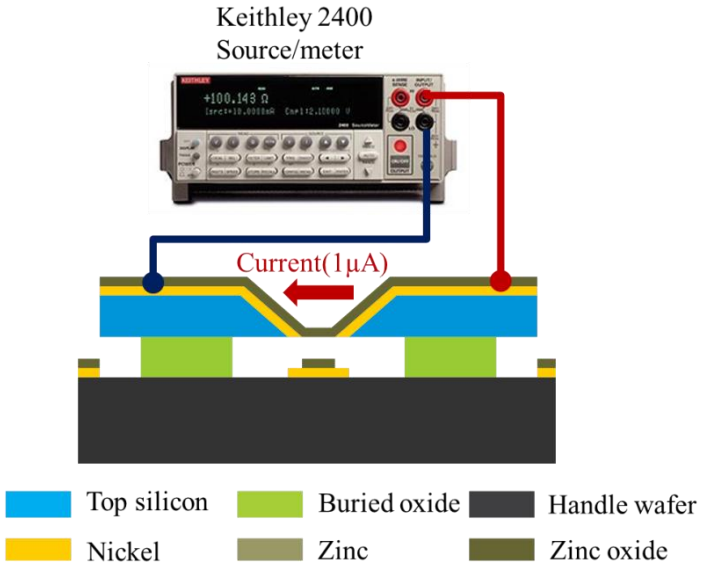

Fig. 4.9 Schematic illustration of the experimental setup for investigating electroluminescence of nano ZnO dot.

Using the device configuration, which allows ignoring the leakage current, electroluminescence (EL) of the nano ZnO dot was investigated to understand the optical properties of the device. To apply electric current to the device, a Keithley 2400 meter is connected to the Ni layers, which were used as electrodes on the device as shown in Fig. 4. 10 (a). For DC bias, two tungsten probes were wired to the source / meter with a BNC cable, and the probes made physical contact with the Ni layer. A tungsten probe was installed on the micro manipulator for controlling probe position for accessing the micro-size electrodes.

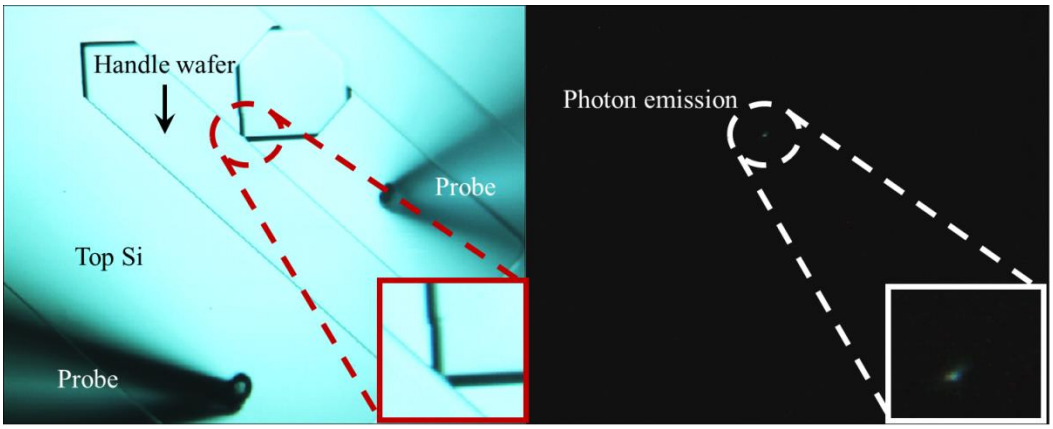

Fig. 4.10 Visible emitted light from the nano ZnO dot with DC bias in microscope. (a) Nanogap device on which ZnO is integrated before biased. (b) Nanogap device showing photon emission.

Fig. 4. 10 (b) shows a microscope image of a visible light emitted from the ZnO under 1μA DC bias. The position of the emission of light was observed at a position exactly corresponding to the location of the ZnO. It proves that the synthesized nano ZnO dot was a source of electroluminescence. Only the ZnO film between the nanogaps was electrically active and the light was emitted only from the synthesized film. Fig. 4. 10 (a) shows the device under an optical microscope before a bias is applied. Fig. 4. 10 (b) shows the device under 1μA bias in the dark. The light intensity from the ZnO nanostructure under the bias was bright enough to be seen

through an optical microscope at 200X magnification with the bare eye, and the location of light emitting exactly corresponded to the location of the synthesized nano ZnO dot.

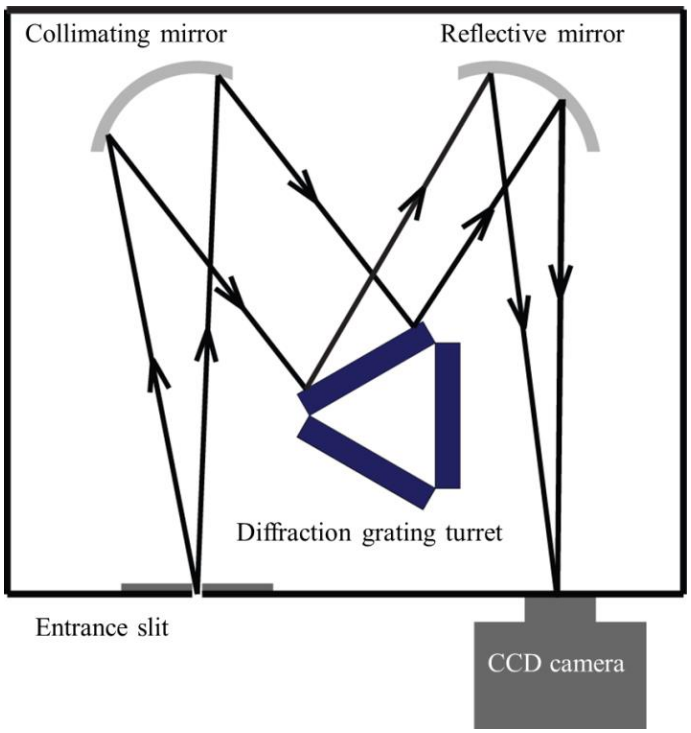

Fig. 4.11 Schematic illustration of typical monochromator having CCD camera for spectroscopy.

For a detailed investigation of the optical properties of the light emitted in the device, the spectrum was measured with monochromator installed with a charge-coupled device (CCD) camera. The monochromator used was an Acton SP-2356 of Princeton Instruments, and the CCD camera was Cascade 512B. The monochromator is composed of three main components, including a diffraction grating, slits, and spherical mirrors as shown in Fig. 4. 11. The entrance slit determines the amount of light entering into monochromator as its size is mechanically controllable. If the slit is opened widely, the resolution is decreased due to imaging effects. Otherwise, the narrow slit width results in a diffraction effect reducing resolution. The spherical mirror collimates the light entering through the silt to convert the light to parallel rays. The

collimated light is diffracted from the rotating diffraction grating, and then the light is collected on another reflective mirror, which refocuses it on the exit slit. Since each wavelength of light in the diffracted light beam focuses on a different position through the reflective mirror, monochromatic light with respect to the rotation angle of the diffraction grating is observed by CCD camera, and the intensity and wavelength of the light is calculated for a spectrum of incident lights.

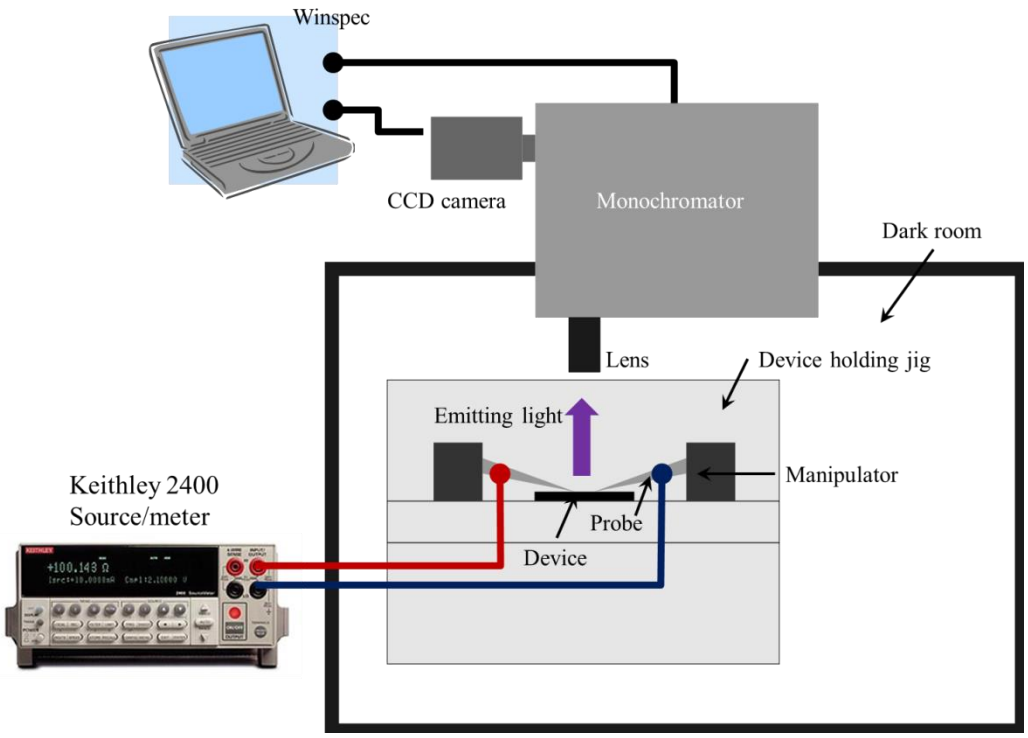

Fig. 4.12 Schematic illustration of the experimental setup for determining the spectrum of the light from the nano ZnO dot

For obtaining the spectrum of the light from spectroscopy of the nano ZnO dot, the monochromator and the device are located in a black box to block any incoming light as shown in Fig. 4. 12. The device is fixed on a device-holding jig adjusting the location of the device in 3 directions. The jig is used to focus the device on the lens which is installed on the entrance slit.

As in the previous light emission experiment, the device is connected to the Keithley 2400 for DC bias through tungsten probes. When the current is biased, the emitting light passes through the monochromator, and the CCD camera measures the light. The intensities with respect to the wavelengths are measured by the program "Winspec". Fig. 4. 13 shows the spectrum of the electroluminescence for the fabricated nano ZnO dot with the experimental setup.

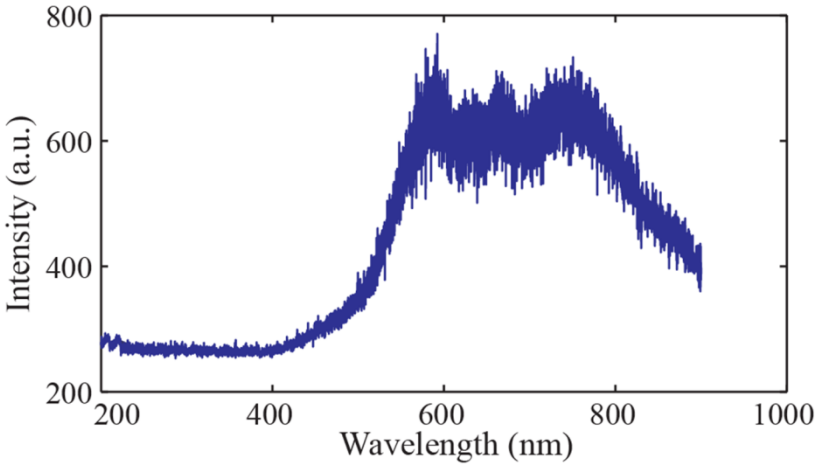

Fig. 4.13 Measured electroluminescence at 1μA bias from nano ZnO dot between metallic nanogap.

A typical spectrum obtained from the device in this work is shown in Fig. 4. 13. The measured spectra of electroluminescence from the ZnO nanostructure show a broadband of emission with major peaks between 600 and 700nm. The spectrum is very similar to that in the previously reported work, in which the electroluminescence shows a broad visual band but no noticeable UV wavelength. Although the bandgap of the ZnO corresponds to the UV wavelength (3.3eV), it shows green light emission due to the oxygen vacancy and also red emission at 700nm, which is attributed to the zinc vacancies or excess oxygen (C. H. Ahn, Kim, Kim, Mohanta, & Cho, 2009; Bano et al., 2010). Low UV intensity from the measured electroluminescence could be due to relatively lower carrier density than that for photoluminescence and recombination of the injected carriers at defects and surfaces, states more effectively than from band edge.

Furthermore, the cause of the visual spectrum without UV line from the ZnO structure might result from dislocations related to luminescent centers including surface states and Zn vacancies (Hsieh et al., 2009; Ohashi et al., 2005; Radoi, Fernandez, Piqueras, Wiggins, & Solis, 2003) .

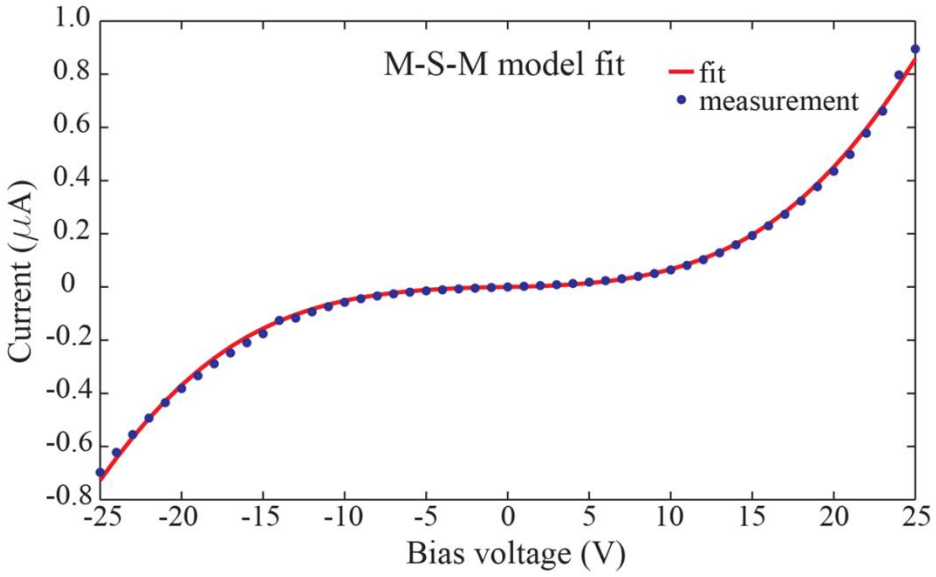

Fig. 4.14 A M-S-M model fit of a measured I-V charateristics from the nano ZnO dot across nanogap.

To further investigate the electroluminescence from a nano ZnO dot between the metal tips, the measurement of the current-voltage characteristic was performed. Basically, the I-V curve, determined by the transport of charge inside the device, has been used to study a device's fundamental parameters. The experimental setup used for I-V measurement is similar to the experimental setup for measuring leakage current as mentioned in the previous chapter, as shown in Fig. 4.3 and Fig. 4.4. The applied voltage for the measurement is scanned from -25V to 25V with a 1V increment. In each voltage, current is measured, and the result is shown in Fig. 4.14. The measured I-V characteristic shows a typical metal-semiconductor-metal junction characteristic which is essentially two metal-semiconductor contacts connected back to back. The PKUMSM program (Z. Zhang et al., 2007) was used to fit the measured I-V curve and to extract the semiconductor parameters such as the Schottky barriers of the device as shown in Fig. 4.14.

The extracted values of the barrier height are 0.525 eV and 0.565 eV respectively and the values are asymmetric. This asymmetry may result from Ni-Zn alloy formation at their boundary. Furthermore, resistance of the nano ZnO dot, doping concentration, and carrier mobility were extracted, and the values determined are 104 MΩ, 3.86×10^{17} cm^{-3} and 1.81×10^{-2} $cm^2/(V\ sec)$, respectively. From the extracted values of the barrier height, the energy band diagram at equilibrium shown in Fig. 4.15 was developed. The left junction (J_2) is reverse biased and the right junction (J_1) is forward biased. At junction J_2, two type of electron transports are possible : thermionic emission and thermionic field emission. In thermionic field emission, electron-hole pairs can be generated by impact ionization. At junction J_1, holes from metal are injected. In both cases, light emission occurs and electroluminescence form the hole injection is dominant until the space-charge-limited effect occurs.

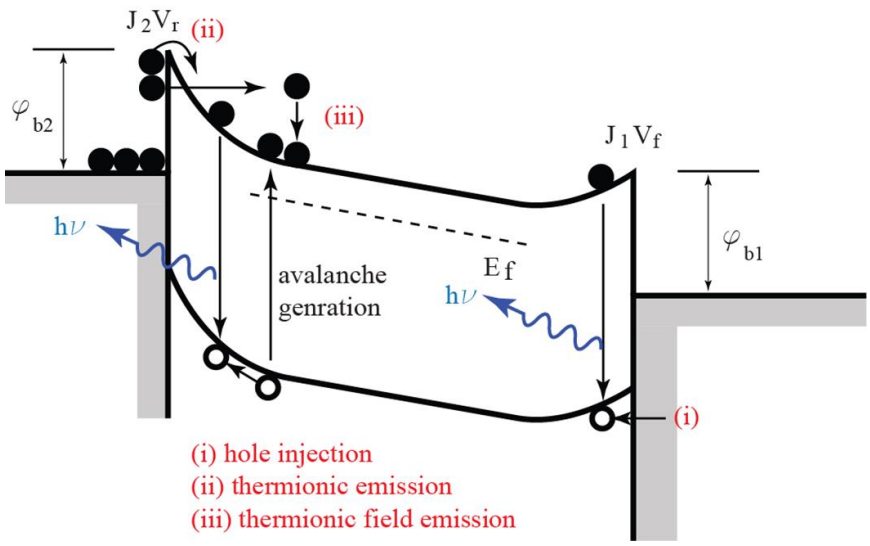

Fig. 4.15 A M-S-M model of the nano ZnO dot device. Energy band diagram of Ni-ZnO-Ni under a DC bias.

The work function ($q\Phi_s$) and electron affinity ($q\chi$) of synthesized ZnO have been reported to be 4.45 eV and 4.29 eV, respectively (Hossain et al., 2003), and the work function ($q\Phi_m$) of Ni is 5.15 eV. Therefore, the Schottky barrier heights at each junction are 0.86 eV.

However, the extracted value shows a difference from the calculated value. The difference may come from the completely depleted ZnO between the Ni covered tips. At equilibrium, the ZnO with the metal contacts are completely depleted assuming the typical concentration of doping of ZnO is $10^{17}/cm^3$.

$$W = \sqrt{\frac{2\varepsilon_s\varepsilon_0 V_0}{qN_d}} \quad (4.1)$$

where W is length of depletion region, V_0 is difference between the work function of Ni and work function of ZnO, ($V_0 = q\Phi_m - q\Phi_s = 5.15$ eV - 4.45 eV = 0.7 eV, $V_0 = 0.7$ V), ε_s is the relative dielectric constant of ZnO (ε_s =7.8), ε_0 is the permittivity of free space ($\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm), q is charge on an electron or hole ($q = 1.6\times10^{-19}$ C), and N_d is the concentration of the doping of ZnO ($N_d = 10^{17}/cm^3$). Therefore, the depletion width is calculated as follows,

$$W = \sqrt{\frac{2\varepsilon_s\varepsilon_0 V_0}{qN_d}} = \sqrt{\frac{2\times7.8\times8.85\times10^{-14}\times0.7}{1.6\times10^{-19}\times10^{17}}} = 77.7nm \quad (4.2)$$

Since the typical size of nanogap is less than 100nm, the nano ZnO dot and Ni junction is completely depleted. Due to this condition, any bias voltage is higher than a reach-thorough voltage (V_{RT}) at equilibrium. The electroluminescence from hole injection at J_1 is dominant in the suspended nano ZnO dot LED device. Electroluminescence from avalanche breakdown at J_2 is expected to occur at a much higher voltage, which is the voltage causing the space-charge-limited effect. In our case, the avalanche breakdown voltage has not been determined due to the device breakdown.

Fig. 4. 16 shows measured light intensity from the nano ZnO dot light emitter with respect to different levels of applied voltages. The measured turn-on voltage for light emission is 12.5 V. The photon-count is integrated for intervals ranging from 1 to 180 sec at each measurement point and is normalized to photon-count per second. The inset in Fig. 4. 16 shows a

close-up view of the photon rate converted from the measured intensity between the applied bias of 12.5V and 20V. The photon rate at 12.5 V is estimated to be ~9000/sec. The photon rate increased as high as 10^7/sec at 40V.

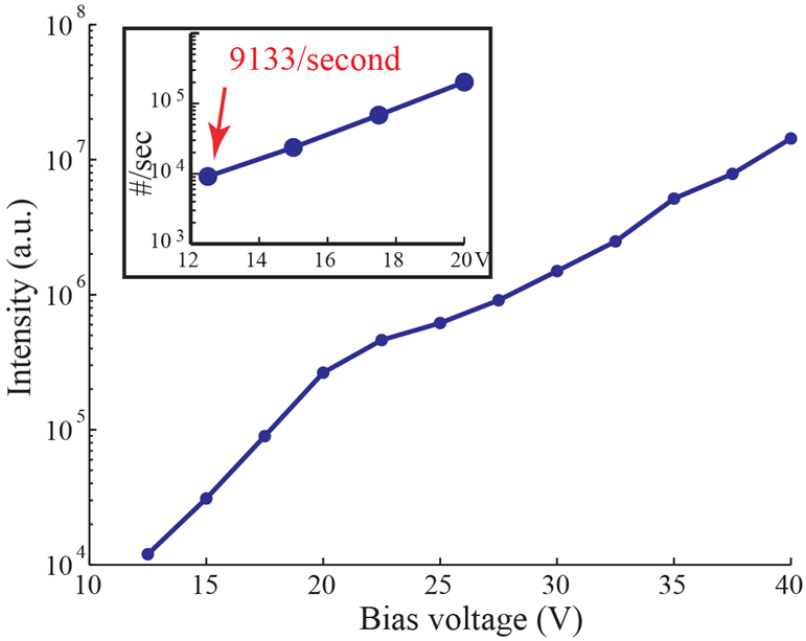

Fig. 4.16 Measured light intensity from a nano ZnO dot light emitter. The inset shows photon counts per second.

4.1.4 Conclusion

In this section, an effective method of direct integration of a nano ZnO dot across the fabricated nanogap tips of the nanogap device is presented. The novel method offers an effective way to build an electronic device with nanomaterial without time consuming and complex processes. The nano ZnO dots are integrated at exact positions, and wafer scale integration is performed by Zn thermal oxidation after Ni and Zn thermal evaporation. The Ni layer is not only used for electrodes consisting of an M-S-M junction, but also acts as an adhesion promoting layer for Zn evaporation. To investigate the conversion of Zn to ZnO through thermal oxidation, SEM

measurement and XRD were performed. The optical and electrical properties of the fabricated nano ZnO dot LED were investigated. For studying the optical properties, the electroluminescence of the device was measured with constant current bias. Although the bandgap of the ZnO corresponds to the UV wavelength, the fabricated devices show peaks between 600nm and 800nm in the electroluminescence spectrum due to intrinsic defects including O vacancies and Zn interstitials. The electrical properties were studied by I-V measurement with a semiconductor analyzer. The measured I-V curve was well fitted with a PKUMSM program, and the values of Schottky barrier's height were extracted and compared to calculated values.

4.2 Nanogap formed by field-induced atomically sharp tips

As mentioned in the previous chapter, a platform having a nanoscale gap defined by metallic tips has been extensively studied because of its ability to synthesize and/or characterize nanoscale electronic structure. For example, the conductance quantization which jumps on the order of the conductance quantum, $2e^2/h$, and the tunneling current for different sizes of nanogap created mechanically controllable metallic nanogap device was investigated at low temperature (Ruitenbeek et al., 1996). In order to generate coherent multiple electron beams, the apex of a sharp nano-object made by a multi-walled carbon nanotube (MWCNT) wase used (B. Cho, Ishikawa, & Oshima, 2007). The self-breakdown mechanism of the atom sized junction in the microfabricated mechanically controllable break junction (MCBJ) was exploited at room temperature under various displacement rate conditions (Tsutsui, Shoji, Taniguchi, & Kawai, 2008) . Electron transport through fulleropyrrolodine terminated molecule bridging, and a graphene nanogap was investigated. The graphene nanostructure was used as a platform for single-molecular electronics for the transistor effect (Bergvall, Berland, Hyldgaard, Kubatkin, & L\ofwander, 2011) . For detecting substances that are invisible to the human eye and tiny biomolecules, various types of nanogap devices have been employed (X. Chen et al., 2010).

Planar type nanogap devices have been used for gold nanoparticle-labeled biosensing and nanoparticle-enhanced biosensing. Vertical nanogap devices have also been applied in biosensing of DNA or RNA. The nanogap devices with three terminals have been used to detect the molecular binding events of very small quantities of biomolecules and to identify antibodies, enzymes or proteins by measuring voltage, resistance and capacitance. However, the work on nanogap platforms has focused on only reducing and controlling the size of the gap at the sub-nanometer scale without considering the control of the radii of curvature of the tips that make up nanogap devices. The large radius of curvature of the tips leads to growth of interesting nanomaterials and nanostructures across nanogap devices in uncontrolled orientations and material states. Additionally, since the nanogap device in most of these platforms are in physically direct contact with the substrate, it is difficult to decouple the electrical, magnetic, chemical or mechanical interaction between the nanostructure and the substrate (Anantram & Leonard, 2006; Y. Yang et al., 2012) .

In this chapter, the approach to define a precise nanogap size and atomically sharp tip radius of curvature, by directly controlling tip-to-tip interaction using an external electrical field, is presented. The approach presented allows nanogap devices having tips of less than 1nm radius of curvature. The applied external electric field leads to metal ion transport at the cathode tip and results in host metal dendrite growth, as well as the grown tips forming nanogaps being self-aligned to each other due to the applied local electric field. To investigate the growth of the dendrite between metallic nanogap, in-situ measurement were performed.

4.2.1 Suspended single nanostructure

A nanostructure growth method based on the ZnO nanogap devices is presented, which allows for direct growth of a suspended single nanostructure across the nanogap in air and at room temperature. The structure grown is also located at a specific location. This work provides

an effective way for integrating a nanoscale structure on existing electronic devices. Furthermore, the suspended single nanostructure has an ideal configuration for building electronic devices that minimize leakage currents.

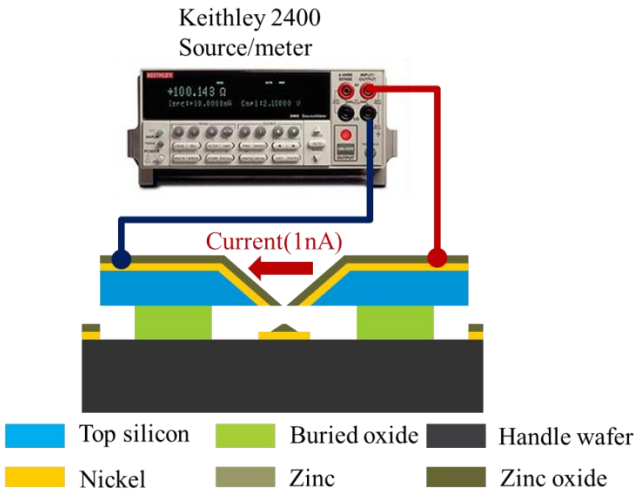

Fig. 4.17 Experimental setup for nanostructure growth in air and at room temperature by DC current bias

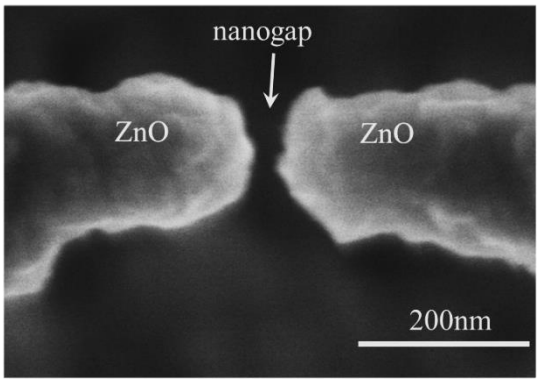

Fig. 4.18 Ni/ZnO coated nanogap tip fabricated by thermal Zn oxidation

The growth is initiated by high electric field caused by a current bias of 1 nA and the experimental set up is shown in Fig. 4. 17. In case of a ZnO nanogap, fabrication processes were similar to the processes which were performed for nano ZnO dot LED described in the previous

section. However, the initial nanogap was not filled with by the metal evaporation. In other words, the metal depositions and Zn thermal oxidation reduced the nanogap size and a ZnO nanogap device is formed as shown in fig 4. 18.

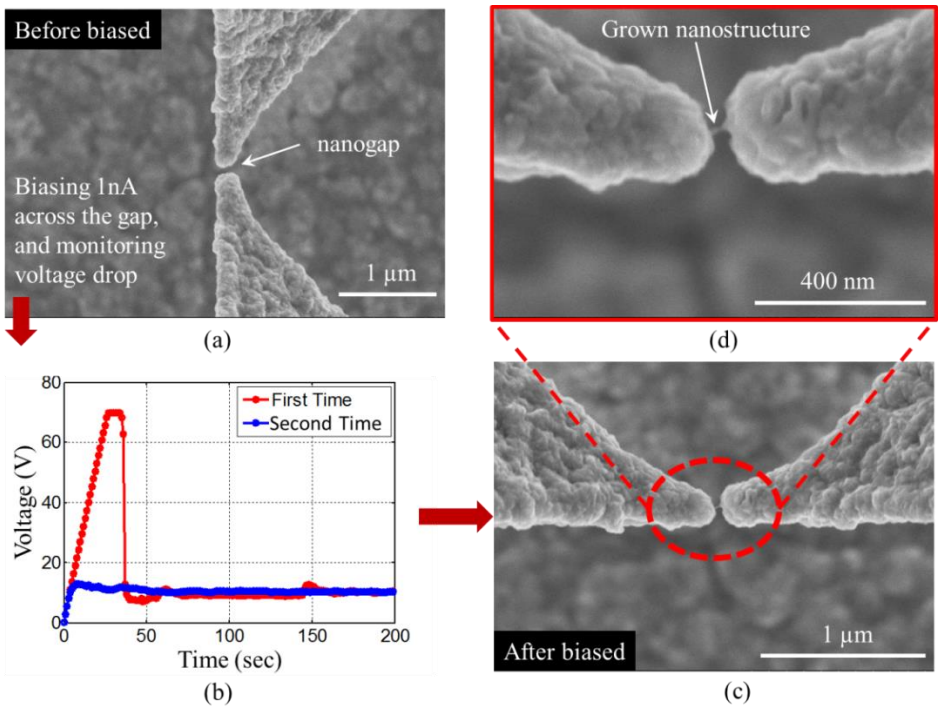

Fig. 4.19 Nanoscale structure growth between the nanogap under high electric field. (a) The tips forming the nanogap are covered with Ni/ZnO. Initially, a nanogap exists at this stage. (b) A DC bias of 1nA is applied across the nanogap while monitoring the voltage change. (c) SEM image of the device after the DC bias. (d) Magnified SEM view of the nanogap in (c). A visible single nanostructure is bridged across the initial tips.

Figs. 4. 19 and 4. 20 show nanostructures grown based on the ZnO nanogap devices. When the electrical source was applied to the devices, the potential difference across the device increases as a function of time until its maximum limiting value, compliance voltage, or until the value needed to establish a DC bias current of 1 nA through the device under test was reached. This voltage change across the nanogap is monitored during the biasing step, and the voltage versus time graph is shown in Fig. 4. 19 (b) for the devices. In this case, the initial size of the gap was 80nm, and the voltage across the nanogap increased until the compliance voltage, 70V, and

the value was held for 10 seconds. The voltage, termed the break-down voltage, abruptly dropped to 15V when the gap was bridged by a suspended nanostructure. Once the nanostructure bridge was formed across the nanogap, the voltage was maintained and the average electric field across the nanostructure was estimated to be on the order of 2×10^9 V/m. Also, the average current density was estimated to be approximately 5×10^6 A/m^2, assuming an average nanostructure radius of 8.5nm.

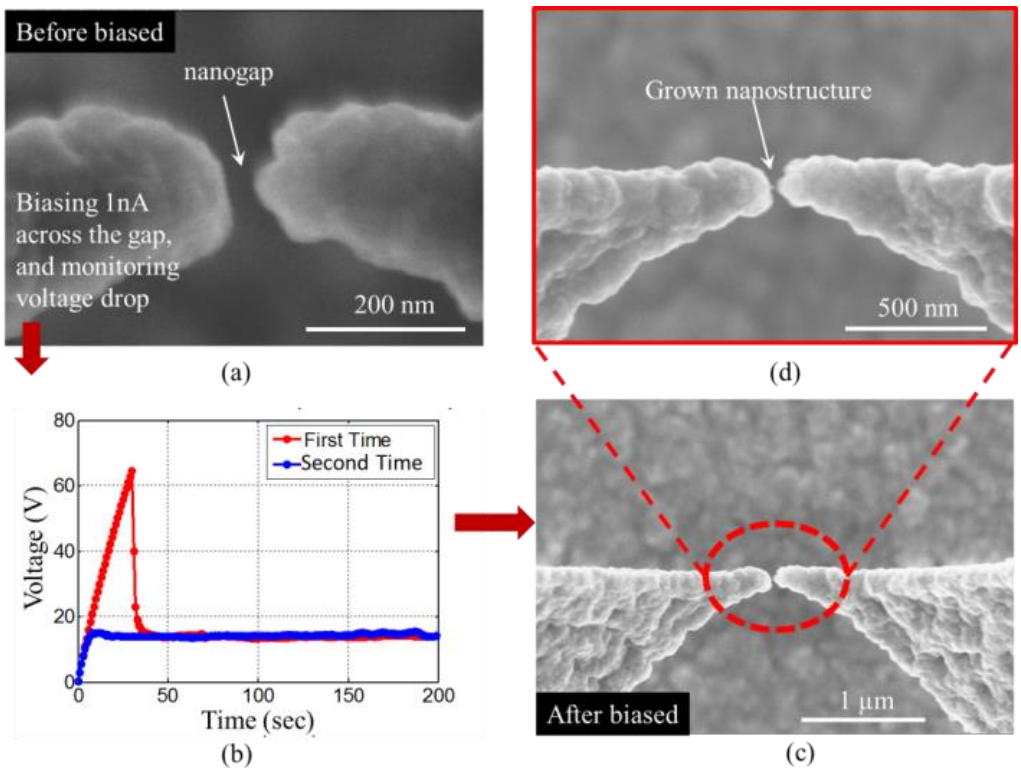

Fig. 4.20 Grown nanostructure across initial 50nm nanogap. (a) SEM image of 50nm initial gap device. (b) Monitored voltage respect to the time with 1nA DC bias. (c) Overview of grown nanostructure. (d) Magnified grown nanostructure induced by electric field.

Fig. 4. 20 shows another experimental result, which was conducted with an initial 50nm nanogap. In this case, the voltage reached 65V and then suddenly dropped. The variation of maximum voltage with respect to the initial gap size indicates that the electric field across the nanogap is an important factor for nanostructure growth. Also noticeable, the nanostructures

grown were asymmetric as shown in Fig. 4. 19 (d), Fig. 4. 20 (d) and Fig. 4.21. The nanostructure on the negative terminal tip was larger than that of the positive terminal. The formation and shape of the nanostructures was consistent for 20 of 25 devices used in this work. When the initial size of the nanogap of the other five samples was less than 10nm, multiple nanostructures were grown across the nanogap, and the shape was more symmetric as shown in Fig. 4. 21 (d).

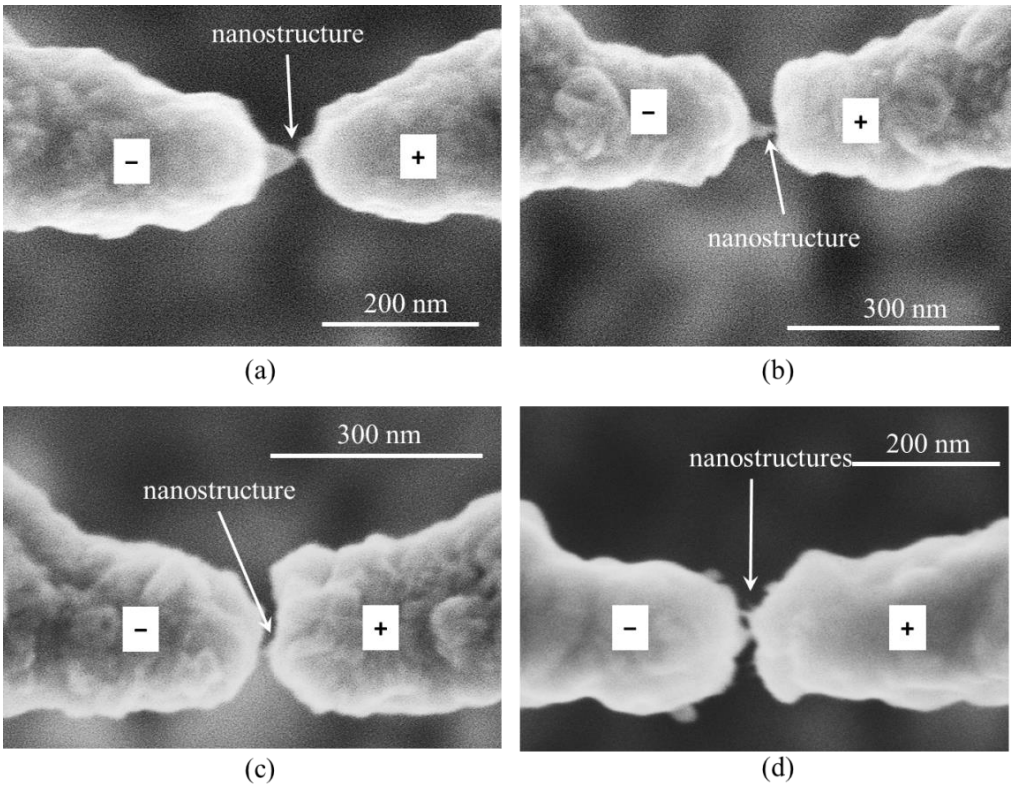

Fig. 4.21 SEM images of nanostructures grown between the nanogaps. Four different nanogaps show different asymmetric shaped of nanostructures. The initially narrow nanogap device in (d) shows growth of the multi nanostructures.

The physical and electrical properties of the nanostructure grown were monitored after another DC bias of 1nA was applied to the device for 24h in air and at room temperature. No further shape changes of the nanostructure are observed in SEM images, and the resistance change was less than ±5% with respect to the initial resistance value. To understand the electrical properties of the nanomaterials grown, I-V curves of the devices were measured using a HP4145

semiconductor analyzer. Fig. 4. 22 shows the measured I-V curve after the nanostructure was grown across the nanogap. The voltage is swept across the nanogap device and current is monitored. The voltage bias was limited ±15 V owing to a tendency to damage the nanostructure by burn-through with high voltage. The I-V data in Fig. 4. 22 show typical M-S-M junction characteristic like that in Fig. 4. 14 which shows the I-V characteristic of the nano ZnO dot light emitter. The Ni used as the electrode in this work should form a Schottky contact with ZnO.

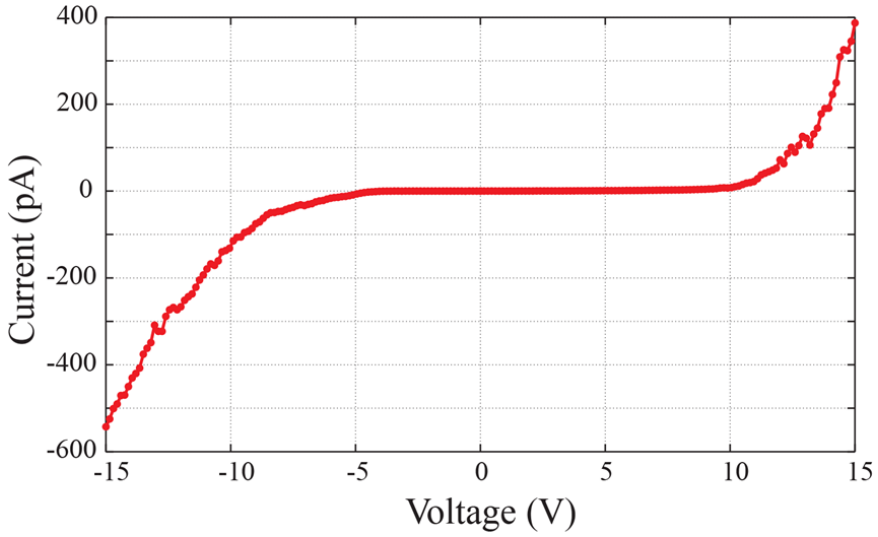

Fig. 4.22 I-V curve of the device shown in Fig. 4. 18. The I-V data show typical M-S-M junction characteristic, which is back-to-back Schottky diode.

4.2.2 Device fabrication for studying a growth mechanism with in-situ TEM

For a more detailed investigation of the growth mechanism of nanostructures induced across nanogap by an electric field, in-situ transmission electron microscopy (TEM) experimentation is required. To create a device adaptable to in-situ TEM, additional processes such as making thru-holes in a handle wafer of a SOI wafer and forming an individual die for installing the die onto a TEM holder were required with the fabricated nanogap device. The thru-

hole has to be located between the tips forming the nanogap for passing electron beams and the size had to be controlled to keep the mechanical strength of the tip and electrode.

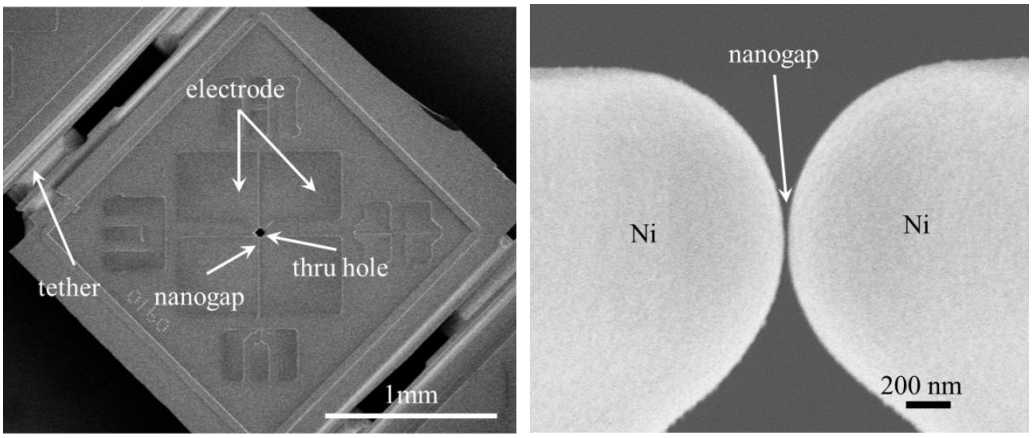

Fig. 4.23 SEM images for Ni deposited nanogap device. (a) Overview of fabricated suspended metallic nanogap device. (b) A close-up SEM view of the metallic nanogap.

First of all, for long-time etching of 600μm thick handle wafer, a 150nm thick, low-stress silicon nitride film was deposited by LPCVD on the fabricated silicon nanogap device. The pattern for etching silicon nitride was printed on the back side of the SOI wafer through a back side aligner. In this step, the patterned photoresist acted as an etch mask for etching silicon nitride film in RIE. The RIE for the silicon nitride film etching was performed in a vacuum system maintaining 300mTorr, and CF_4 gas was introduced as a reaction gas. After etching the silicon nitride film, the exposed silicon area was etched by a wet chemical anisotropic etchant, KOH, for 32 hours at 60°C with the KOH bath system described in the previous chapter. In this fabrication, the silicon etching that determines the size of thru-hole was self-terminated by four (111) planes and the size was 60μm x 60μm on the top of the handle wafer as shown in Fig. 4. 23 (a). In this etching step, the silicon etching for die separation was conducted simultaneously with the

creation of a thru hole. The tethers offered mechanical stability of each die after etching as shown in Fig. 4. 23 (a).

After thru-hole etching and die separation were performed, metal was evaporated on the nanogap device. Since the fabricated nanogap device was physically isolated from the substrate, a 2μm space between the device layer and handle wafer, any lift off process or shadow mask, which are time consuming and lead to complex processes, is not needed for forming metallic electrodes. The fabricated nanogap device configuration, suspended nanogap device, allowed blanket evaporation of various metals such as gold (Au), aluminum (Al), nickel (Ni), chromium (Cr), and copper (Cu) for electrodes. For thin film metal deposition, a high vacuum evaporator having mechanical and diffusion pumps capable of 5×10^{-8} Torr ultimate pressure was used. Also, the evaporator used Joule heating to melt the metal source in a tungsten basket, an alumina coated tungsten basket, and a crucible. In this work, a 60 nm thick Ni layer was thermally evaporated over the entire device under a vacuum of 7×10^{-7} Torr. During the process, the evaporation rate and thickness were monitored using a monitoring system including a quartz crystal located in the evaporation chamber. The deposited Ni served as a metal source for metal ion transport by an electric field as well as metal electrodes. Fig. 4.23 (b) shows an SEM image of the final Ni layer deposited nanogap device.

The silicon nitride film deposition process for forming a silicon etch mask for KOH etching had two other functions. The first role was preventing silicide formation, which changes electrical contact conductivity when contact metal is thermally evaporated on the silicon tips and electrodes. The SiN film between the top silicon layer and the metal film originally blocked the diffusion and interaction for forming silicide. Therefore, an electrical interaction between the metallic electrode and the silicon substrate was removed when the device was biased for generating a high electric field. The second effect was to reduce the initial size of silicon nanogap as shown in Fig. 4. 24. When the silicon nitride was deposited on the silicon device, the micromachined nanogap was reduced by approximately 70nm, with 150nm SiN film deposition.

Also, the metal evaporation further reduced the nanogap size in the same manner. Although the SiN and metal deposition resulted in increasing the radius of curvature of the tips, this effectively reduced the size of gaps.

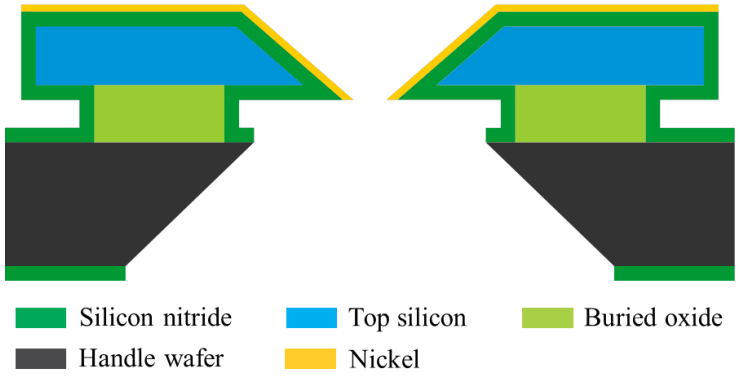

Fig. 4.24 Schematic illustration for sectional view of nanogap device on which silicon nitride is deposited and nickel is evaporated.

4.2.3 Experimental method and results for in situ TEM of nanostructure growth

To investigate the growth mechanism of nanostuructures between metallic tips by metal ion transport, the fabricated device was installed on a TEM holder, and in-situ TEM was performed. Since the grown nanostructure was too small to be observed in SEM, TEM was adopted and a real time image was acquired by camera, which was installed in the TEM.

A die separated from a wafer was 2.5mm x 2.5mm in length and width, respectively, as shown in Fig. 4.25 (a). The size is required to install the die in a TEM holder. For easy handling and stable installation of one small die in the TEM in-situ holder, a die holder which was fabricated with silicon substrate was used, as shown in Fig. 4. 25 (a). The holder had frames for holding the nanogap device, and thru holes for electron transmission for TEM were fabricated using a KOH anisotropic etching approach with a silicon wafer, on which silicon dioxide and silicon nitride were initially deposited. After the device was installed on the holder, a wire was

needed for electrical connection between the electrical pad of the nanogap device and the electrode of the TEM holder. One end of the wire was connected by silver epoxy on the nanogap electrodes as shown in Fig. 4. 25 (a), and the other end was soldered to the electrode of the TEM holder as shown in Fig. 4. 25 (b). The copper wire used was coated with an insulator, and the end points of the insulator were removed by a laser for firm electrical connections. The TEM holder was installed on the JEM 2100F, which is high resolution field-emission TEM, and the in-situ experiment is performed.

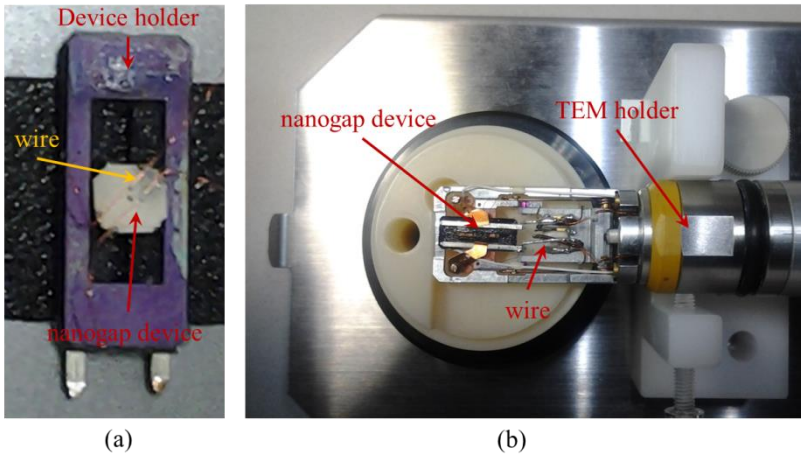

Fig. 4.25 Nanogap device for in-situ TEM. (a) Nanogap device and the device holder for stable installation to the TEM holder. (b) The installed nanogap device on the TEM holder.

To investigate the metal ion transport under an electric field, a 10nA DC current bias was applied across the nanogap. The maximum voltage drop was limited using the bias compliance of the Keithley 2400 source/meter, and the compliance was set up to 100V as shown in Fig. 4. 26. In this biasing configuration, the nanogap forms an open circuit initially, causing the initial current to be zero. By applying a high electric field (~10^9 V/m) at the tip, the dendrite-like nanostructure was grown from the cathode toward the anode tip, where the electric field is the highest across the nanogap.

Fig. 4. 27 shows in-situ TEM images of a nanostructure growth sequence over time for a constant current, 10nA. The electrical current between the electrodes forming the nanogap increased during the ion transfer progress as shown in Fig. 4. 28 (a). In spite of the current fluctuation in the process of nanostructure growth in Fig. 4. 28 (a), the trend of current change shows that the current increased until the set bias current 10nA. When the current was equal to the set bias, the nanostructure growing from the cathode bridged the gap to the anode. Also, the voltage dropped abruptly when the current reached the set value shown in Fig. 4. 28 (b). The cause of the current fluctuation could be the result of the growth of multiple nanostructures on the cathode tip, which would change the local electric field. The trend of voltage change during in-situ TEM was similar to the nanostructure growth in air and room temperature described in the previous chapter, although the growth time was longer than for the experiment in air. The cause of longer growth time could be due to interference of the electric field across the nanogap electrodes by the 200kV electron beam used in TEM for monitoring.

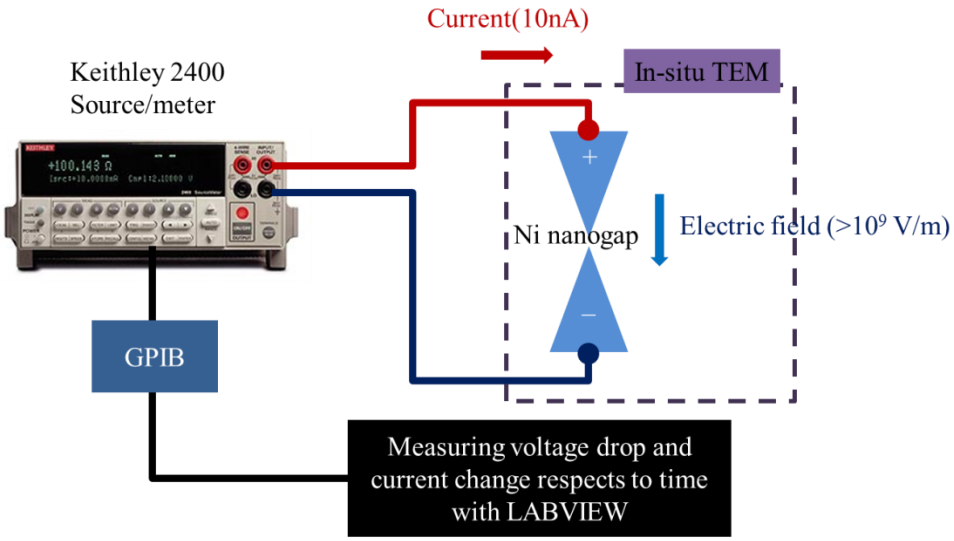

Fig. 4.26 Schamatic illustration of measurement set-up for metal ion transfer growing of the dendrite nanostructure across nanogap.

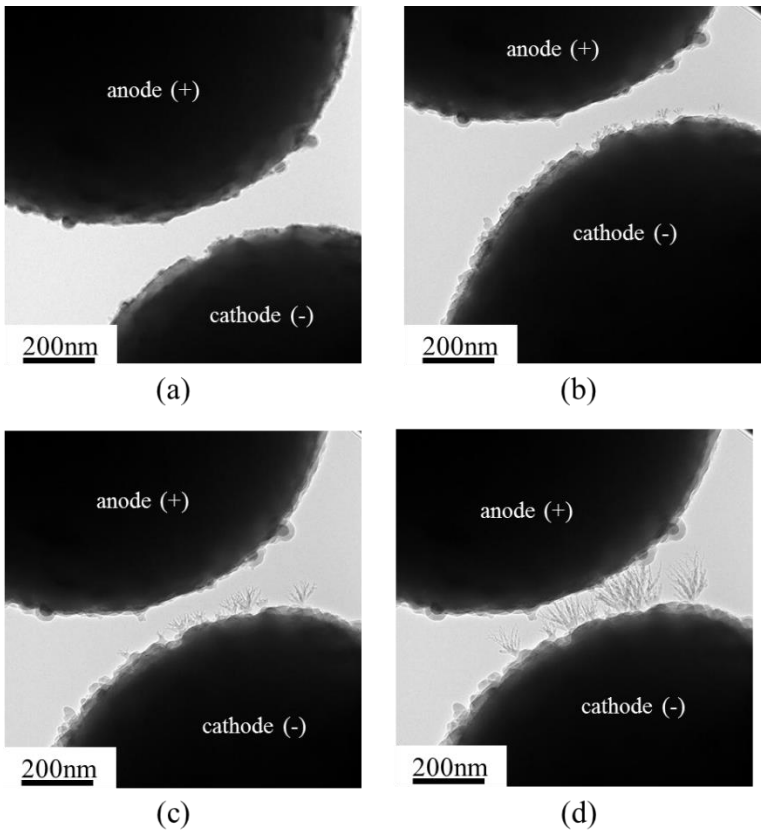

Fig. 4.27 In-situ TEM images of the growth of the nanostructure with 10nA bias across nanogap. The bias polarity is indicated on the tips. (a) Ni nanogap at the beginning of current bias, (b) Dendrite nanostructure starting to grow, (c) Further growth of the nanostructure, (d) Fully grown nanostructure between tips.

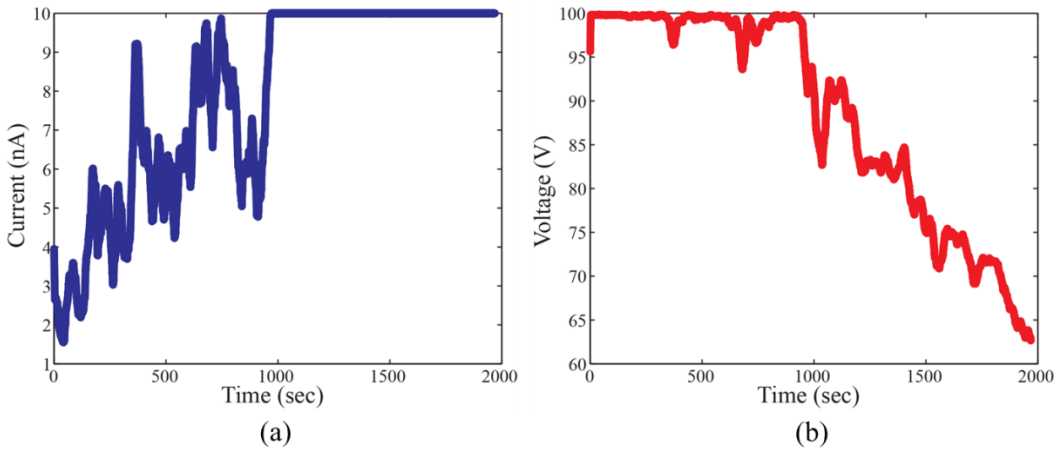

Fig. 4.28 Measured DC bias during in-situ experiments for growing the nanostructure. (a) Current profile across nanogap, (b) Voltage drop across the nanogap.

Fig. 4. 29 shows the length and the growth rate of the nanostructure across the nanogap with respect to biased time. The growth rate was ~ 0.034 nm/s during most of the growth duration. As the nanostructure was growing toward the anode tip, the growth rate increased due to the upward trend of the electric field. The cause of the increasing electric field was reduction of the distance between tips, although the biased current was constant.

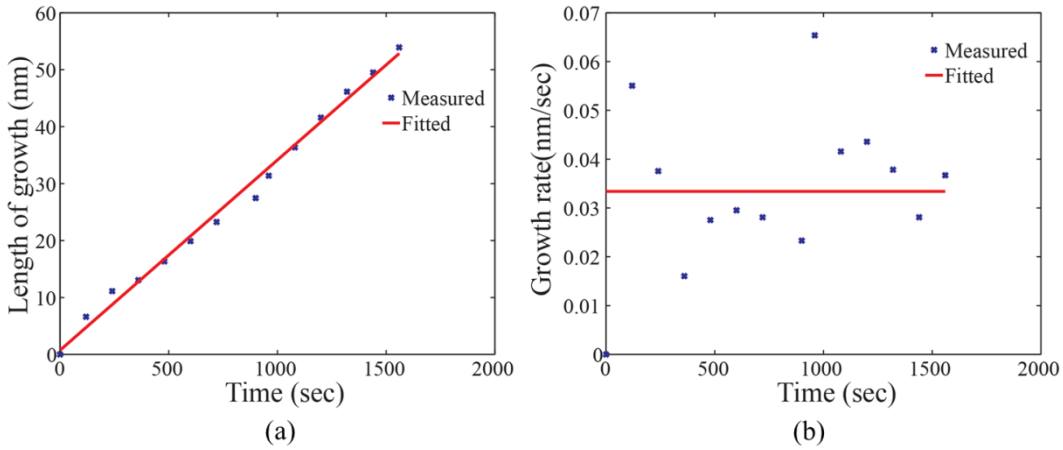

Fig. 4.29 The nanostructure length and growth rate with respect to the DC bias time. (a) Linearly increasing length of nanostructure between metallic tips. (b) Growth rate of nanostructure with respect to the time.

Fig. 4. 30 shows the result of energy-filtered TEM (EFTEM) for the nanostructure grown. The presence of C and Ni was detected using JEM 2200FS having an in-column energy filter. The result supports the growth mechanism by showing that nickel is one of the two predominant elements in the nanostructure grown, as shown in Fig. 4.30 (c). The presence of carbon in the nanostructure shown in Fig. 4. 30 (b) is likely an artifact resulting from electron-beam induced deposition during the in situ TEM experiments (Bachtold et al., 1998; Zaitsev, Shtempluck, & Buks, 2012). The resulting radius of curvature of the tip of the dendrite was typically less than 1nm as grown.

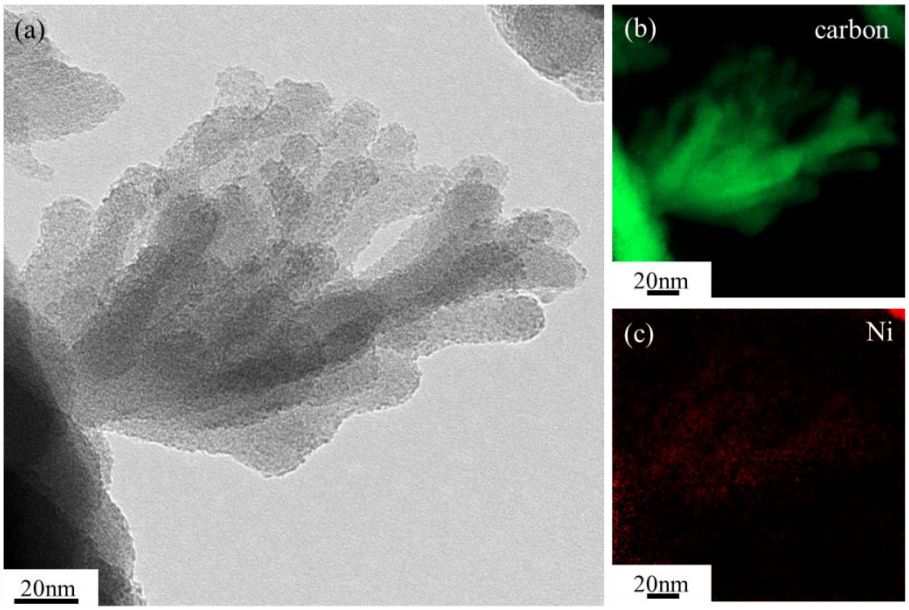

Fig. 4.30 EFTEM analysis image for the grown nanostructure in Fig. 4. 27. (a) TEM image focused on one of the nanostructure grown, (b) Carbon element in the nanostructure, (c) Ni element in the nanostructure.

4.2.4 Nanostructure growth mechanism

Research interpreting the nanostructure growth mechanism induced by an electrical field has been recently performed. Specifically, the filament growth and dissolution mechanism in metal-insulator-metal (MIM) has been actively studied with the various MIM configurations. The MIM configuration consists of electrical conductors with metals including silver (Ag), copper (Cu), nickel (Ni), and platinum (Pt), as well as insulators including silver sulfide (Ag_2S), silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), and porous silicon. The filament growth and dissolution mechanism results in bipolar switching characteristics, called a memristor which is a two terminal non-volatile memory device based on electron or ion migration induced switching effects. The understanding of the filament growth and rupture mechanism is crucial for application of a memristor as a memory cell, usually called a resistance switching random access memoriy.

Generally, four different mechanisms, electromigration (Yuk et al., 2010), field ion emission (Kume, Tomoda, Hanada, & Shirakashi, 2010), cation migration (Y. Yang et al., 2012) and anion migration (Waser & Aono, 2007), are deeply related to nanostructure growth by metal ion transport under a high electric field. In the four mechanisms, cation migration on a substrate is caused by the electrochemical metallization and dissolution of elemental metal-based filaments at the anode. Cation migration occurring through dielectric substrate materials such as silicon dioxide, aluminum oxide, and amorphous silicon is also closely related to the ion mobility in the substrate, and the mobility of the cation determines the growth direction as well as shape of filament. The field ion emission between metallic nanogaps on the silicon dioxide layer results in the atom migration from anode to cathode. On the other hand, anion migration is realized with transition metal oxide, which is used as an insulator. The mechanism has been described by migration of oxygen vacancies toward the cathode, which also depends on the interaction with the host material.

In our device configuration, any direct interactions between metal ions and the substrate can be ignored since the nanogaps are electrically and mechanically isolated from substrates. Therefore, the metal ion migration is the sole parameter due to the interaction with the electric field and/or electron tunneling current. Eliminating the other mechanisms based on the interaction with substrates, it is postulated that the ion migration occurs only at the cathode tips. The external electrons from the source are accumulated in the cathode, and the Ni metallic tips are ionized by the electrons. The ionized Ni transports toward the anode by a strong electric field between tips in air and in vacuum as shown in Fig. 4. 20 and Fig. 4. 27. The growth mechanism by ion migration is also supported by in-situ TEM showing dendrite nanostructure growth at the cathode tip, with no recognizable change at the anode tip. Also, the stem thickness near the cathode increases during constant current bias. This result is different from metal filament growth at the anode reported by Y. Yang et al. and W. Kume et al. Based on the in-situ TEM images of the growth, it is likely that the nanostructure growth results from the ionization of Ni and/or NiO by electron

tunneling and transport of the ion under the high electric field at the cathode (D. C. Kim et al., 2006).

4.2.5 Conclusion

Nanostructure growth across ZnO nanogaps and metallic nanogaps formed by an electric field between two tips was investigated. The method allows for fabricating a few nanometers of a nanogap with atomically sharp metallic tips in air and in vacuum. The in-situ TEM to image in real time is used to interpret the growth mechanism of metallic nanostructure and the image allows identifying the ion migration mechanism under the strong electric field applied by a DC current source. The composition of the grown dendrite nanostructure is demonstrated to be the same as the host material using EFTEM analysis, although carbon is present due to the electron beam enhanced deposition in TEM. Also, when different materials such as metals, polymers, and oxide-based materials are deposited on the fabricated suspended nanogap, it is possible to use the nanogap device as a platform for nanoscale synthesis and characterization.

The reason for growth of dendrite nanostructure can be explained by a localized high electric field accompanying the nanostructure growth. The nanogap size is reduced to a level which is compatible with single molecular electronic, since the length of dendrite nanostructures grown between tips can be determined by controlling the bias termination at the atomic scale. Therefore, the suspended atomically sharp nanogap device formed by ion migration could increase the probability of integration of a single molecule. The method offers optimal electrodes as a platform for single molecule electronics.

5. CONCLUSION

A nanogap device is a core component necessary for creating a practical electronic device in nanotechnology, and they are employed to understand physical and electrical properties of a single molecule and nanostructures, which are the building blocks of a nanoscale device and system. The nanogap device presented in this work provides feasibility for direct integration of a nanomaterial. A novel method of forming a suspended atomically sharp tip grown across metallic tips is developed, and the growth mechanism is studied. The nanogap device formed by atomically sharp tips could be compatible with molecular electronics.

A nanogap device designed is realized with optical lithography, which is the standard patterning approach in the semiconductor industry. The approach shows off outstanding advantages in productivity and repeatability. Some challenges have to be considered in using the approach in nanoscale device fabrication. The drawbacks of the optical lithography in fabrication of a nanoscale device are insufficient critical resolution and a pattern misalignment from mask aligning.

In this work, anisotropic wet chemical etching is applied to overcome the critical dimension of the optical lithography in fabricating a nanoscale device. The anisotropic etching approach allows an effective way to form zero-dimensional sharp tips consisting of nanogap devices with two time etching. The first etching process forms an atomically sharp vertex bounded by two (111) planes, and the second anisotropic etching is used to create a nanogap thorough (100) plane undercut etching for specified time. Furthermore, the novel process called double layer etch mask is developed to reduce a pattern misalignment resulting in non-uniformity in wafer scale fabrication. The double layer etch mask eliminates the impact causing the misalignment, since all of the patterns requiring nanogap formation is established with a mask in the first pattern, and the following patterning is used just to open a window for exposing the Si

layer. Therefore, the accuracy of nanogap pattern is the same as a mask resolution, which shows minimum tolerance to be achievable with optical lithography.

To achieve nanoscale devices with anisotropic wet etching in wafer scale fabrication, accurate crystallographic axis alignment is required since the etching profile is very dependent on the silicon crystal structure. The suggested method employing an optical method results in accurate crystallographic axis alignment. The achieved accuracy of crystallographic axis alignment is less than 0.05°, and a 50:1 aspect ratio of deep trench can be fabricated with the method. Also, the limitation of aspect ratio achievable with the anisotropic etching approach is studied. Although the pattern is perfectly aligned to the silicon crystallographic axis, the maximum aspect ratio is 50:1, due to finite etch rate of {111} planes. To increase the aspect ratio of deep trenches using anisotropic wet chemical etching, an improvement of the selectivity for each plane is required.

Based on the fabricated nanogap device, a nano ZnO dot light emitter was fabricated and analyzed. The nano ZnO dot was directly integrated onto the silicon nanogap device by Zn thermal oxidation. To investigate the successful conversion of Zn to ZnO, XRD was preformed, and the peaks corresponding to ZnO and Ni were obserbed. Also, the electroluminescence of a nano ZnO dot was measured, and the spectrum showed broad visible light due to the crystal structure of the thermally oxidized nano ZnO dot. The electrical property of the light emitter showed a typical MSM model. It proves that the light is from the nano ZnO dot integrated onto the nanogap device.

The suspended atomically sharp tips grown by an electric field is presented. The method is useful to reduce initial nanogap sizes by termination of DC bias as well as to form sharp tips of 1nm radius of curvature. To investigate the growth mechanism across suspended nanogap devices, in-situ TEM was performed. The growth initiated by a strong electric field was monitored in real time. Although the exact analysis of the mechanism is still controversial, the growth could be explained by the metal being ionized by electrons accumulated in the cathode. The ion is then

transported toward an anode by an electric field between the tips. The experimental results could be used as an example to understand an ion migration mechanism in nanoscale. Furthermore, the tips could be used as a platform to understand electrical, optical, and thermal properties of a single molecule.

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APPENDIX A Labview Code

Labview is a useful tool to control instruments with various communication methods such as general purpose interface bus (GPIB), and serial port. In this work, Labview programs are made to control all parameters of instruments and save the measured data for measuring I-V characteristic with HP 4145 semiconductor analyzer. Also, the Keithlely 2400 source/meter for DC biasing to nanogap device is controlled by programmed Labview program. Fig. A.1, Fig. A. 2, fig A. 3 and fig A. 4 show the parameter control screens and internal codes.

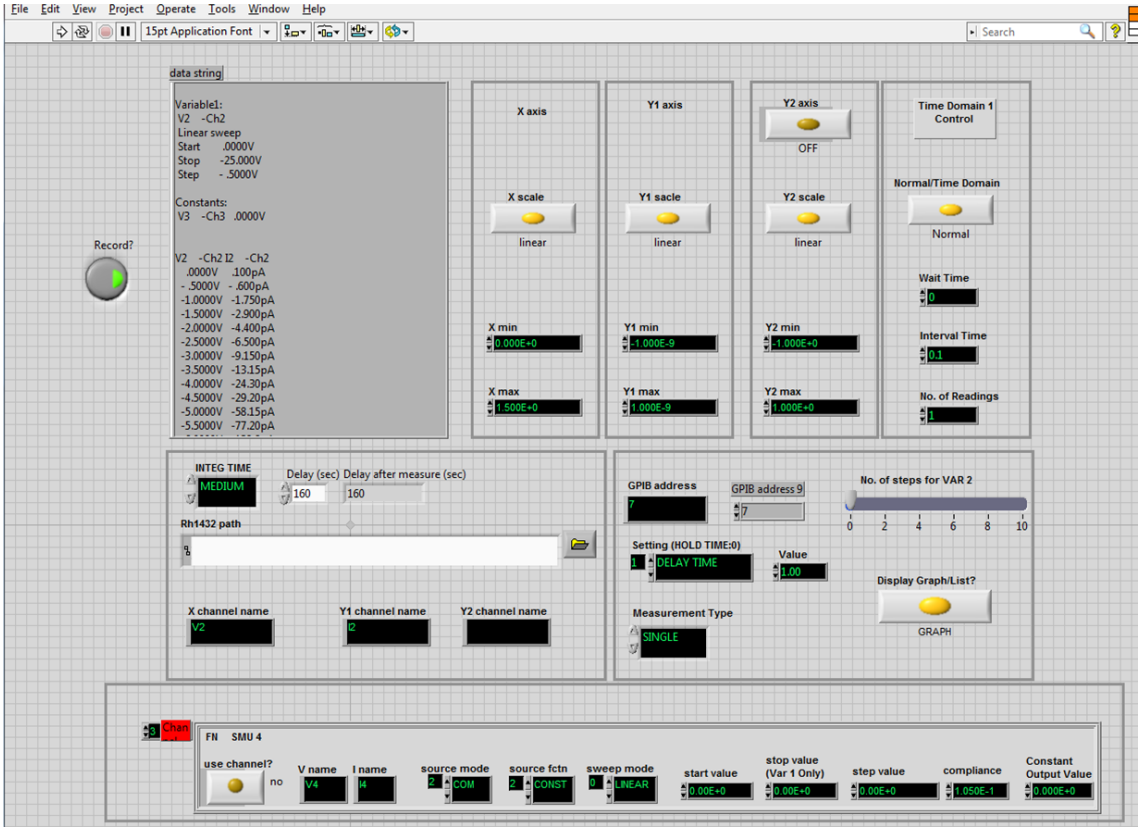


Fig. A. 1 Parameter control screen for HP 4145

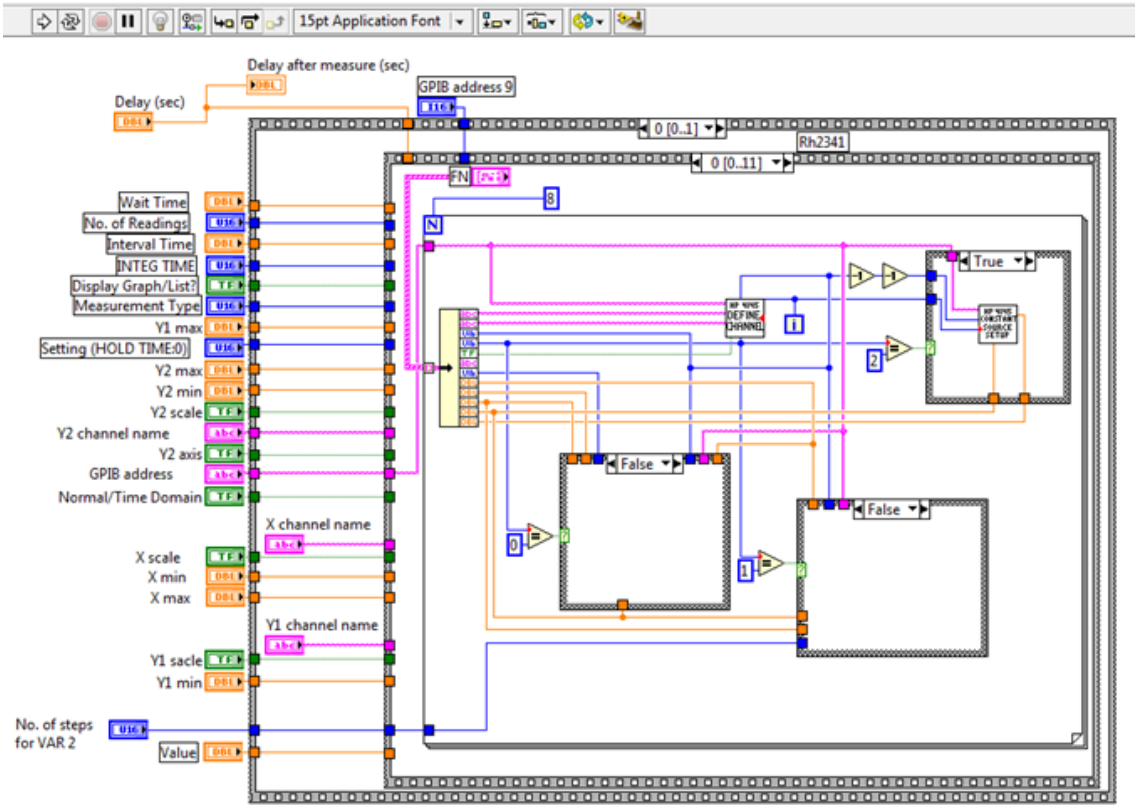


Fig. A. 2 Internal programs for HP 4145

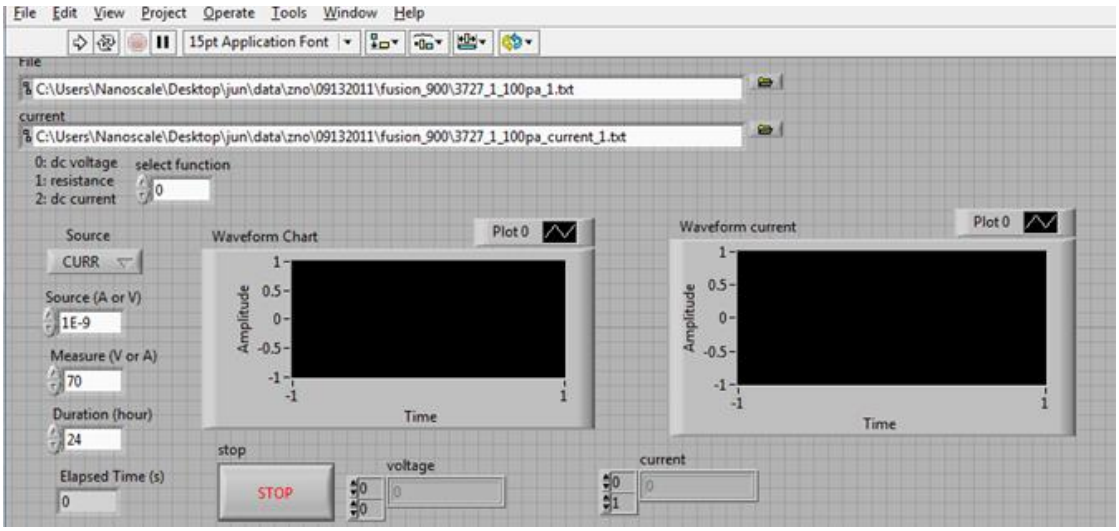
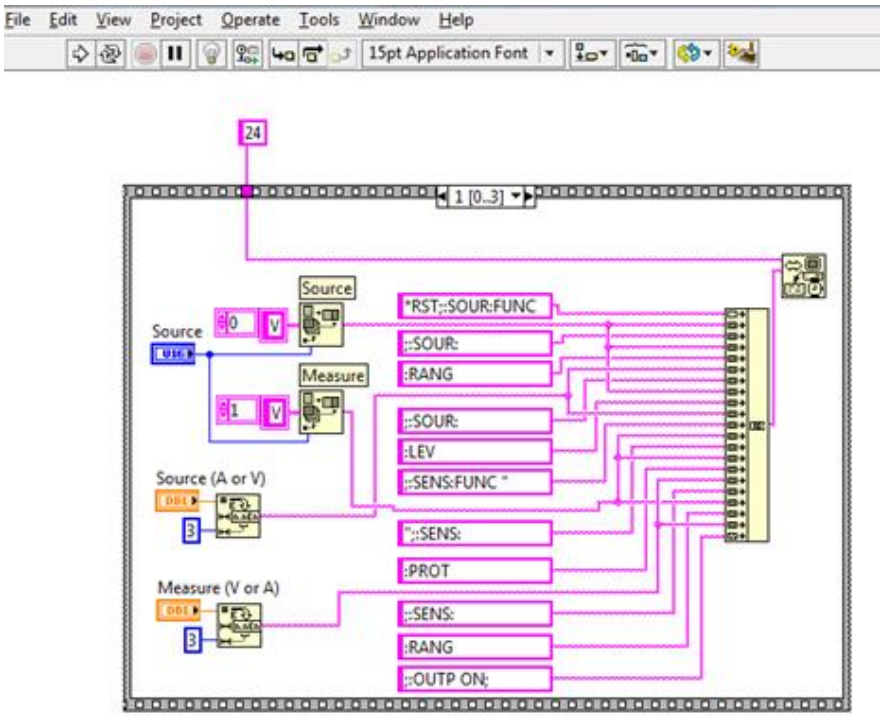
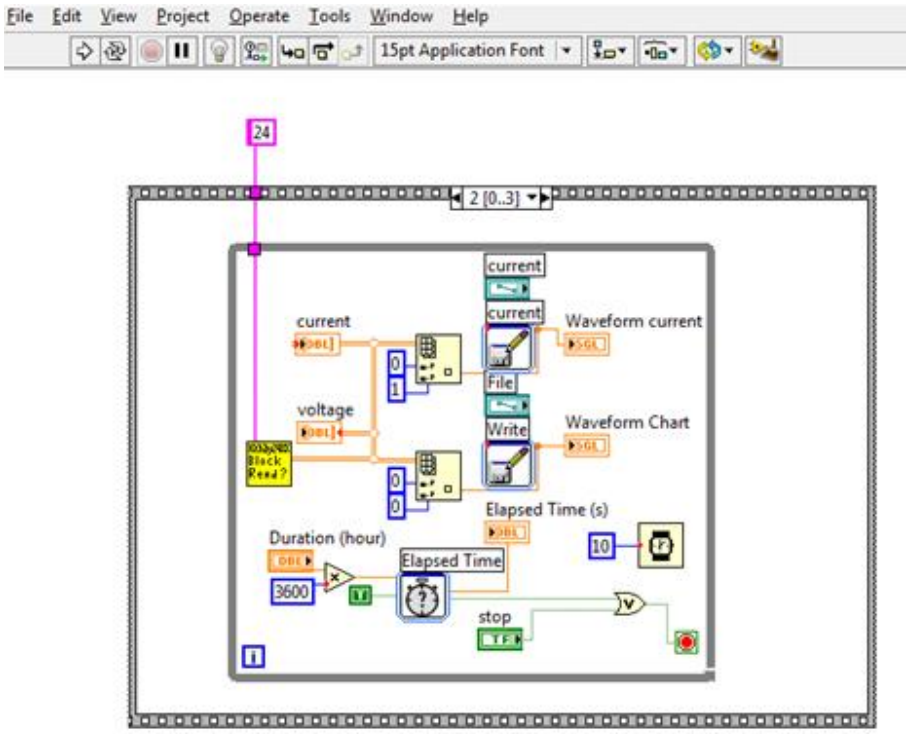


Fig. A. 3 Parameter control screen for Keithley 2400 source/meter



(a)



(b)

Fig. A. 4 Internal programs for Keithley 2400 source/meter

APPENDIX B Published Journal Papers

APPLIED PHYSICS LETTERS **98**, 121113 (2011)

Electroluminescence from a suspended tip-synthesized nano ZnO dot

Jun Hyun Han,[1] Norimasa Yoshimizu,[2] Cheng Jiang,[1] Amit Lal,[2] and Chung Hoon Lee[1,a)]
[1]*Nanoscale Devices Laboratory, Department of Electrical and Computer Engineering, Marquette University, Milwaukee, Wisconsin 53201, USA*
[2]*SonicMEMS Laboratory, School of Electrical and Computer Engineering, Cornell University, Ithaca, New York 14853, USA*

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Electroluminescence (EL) from a laterally suspended nano ZnO dot (LSNZD) integrated between two microfabricated atomically sharp probe-tips is presented. When driven by 1 μA of bias current, the LSNZD emitted light, which was easily observed by the naked eye at room temperature. The minimum number of photons emitted per a second from the LSNZD was ~9000/s at 100 nA of current, when driven by 12.5 V. The light emission mechanism and electrical characteristics of the LSNZD are explained with a metal-semiconductor-metal model. An optical wavelength spectrum of the emitted light shows major bands of emitted photons between 580 and 750 nm, which indicates the electron transitions from defects in the ZnO band gap. The device fabrication is compatible with typical integrated circuit processes and is suitable for chip- scale optoelectronics. © *2011 American Institute of Physics*. [doi:10.1063/1.3570642]

Single photon emitters have applications in quantum computing, networking, and cryptographic key generation and decoding.[1–3] Most single photon sources used are attenuated lasers operating at extremely low temperature, and their photon rate output exhibits a Poisson distribution. Yamamoto *et al.* have reported single photon emitters based on self-assembled InAs quantum dots (QDs) in GaAs with optical pumping.[1] For a practical chip-scale single photon emitter, an electrically driven device would be preferable. Electroluminescence (EL) from a p-i-n diode containing a layer of InAs QDs in the intrinsic region has also been reported.[4,5] A single QD emitting the highest flux of photons is isolated by integrating an aperture over all QDs. From the point of view of creating an array of devices, it is desirable to eliminate postprocessing.

In this letter, EL and electrical characteristics from a laterally suspended nano ZnO dot (LSNZD) are presented. The LSNZD is integrated between a micromachined free-standing nanogap fabricated on a silicon-on-insulator wafer as shown in Fig. 1. The nanogap platforms are fabricated by conventional optical lithography and anisotropic wet chemical silicon etching with a unique double-layer etch mask process. This process produces highly symmetric and reproducible nanoscale gaps as small as a few tens of nanometers by facing atomically sharp tips against each other. The radius of curvature of the tips is typically 30 nm. Suspending the LSNZD allows the elimination of the leakage current through the substrate. Details of the fabrication process of the nanogap are published elsewhere.[6] After the nanogap platform is fabricated, a 50 nm thick nickel (Ni) film is first thermally evaporated, followed by the evaporation of a 50 nm thick zinc (Zn) film without breaking vacuum. The thickness of the evaporated Zn film over the Ni film is chosen to cover the nanogap as shown in Figs. 1(b) and 1(c). The typical nanogap size obtained is 100 nm. The Ni film evaporated on the tips also serves as electrodes to electrically drive the LSNZD. After the metal film depositions, the Zn film on the device is oxidized in a quartz tube furnace [5 SCCM (SCCM denotes cubic centimeter per minute at STP) O_2 flow at 350 °C, 2 h] to form a ZnO film. After oxidation, the entire 50 nm thick Zn film is converted to ZnO film. Similar oxidation methods to generate ZnO have been reported by other researchers.[7–10]

Figure 1(c) shows the scanning electron microscope micrograph of a LSNZD between the Ni electrodes on silicon tips. The cross-sectional schematic view of the device is shown in Fig. 1(d). Only the ZnO between the nanogap is electrically active when biased. The Ni electrodes combined with the ZnO dot form a metal-semiconductor-metal (M-S-M) junction (Ni–ZnO–Ni). X-ray diffraction (XRD) of the film shows a conversion of Zn film to ZnO film by the thermal oxidation, as shown in Fig. 2. The strong peak of Ni film in the XRD data indicates that the Ni film is intact underneath the ZnO film, after exposure to a low oxidation temperature of 350 °C. Alloys of Ni–Zn can be formed at the

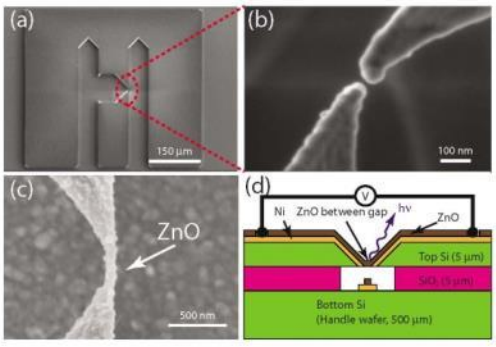

FIG. 1. (Color online) (a) Nanogap device overview, (b) nanogap before Zn/Ni metal evaporation, (c) after Zn/Ni metal evaporation on the gap followed by thermal oxidation to convert Zn film to ZnO film, and (d) cross-sectional view of the nanogap device. The gap is filled with ZnO. When a bias is applied to the gap, photons are emitted from the ZnO between the gap.

a)Electronic mail: chunghoon.lee@marquette.edu.

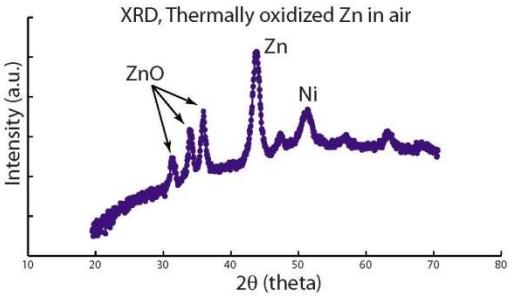

FIG. 2. (Color online) XRD data of the thermally oxidized Zn film. The data show ZnO diffraction peaks confirming conversion of Zn film to ZnO film.

boundary[11] during the thermal oxidation, which may affect the Schottky barriers of the M-S-M junction, and may introduce NiO_x impurities besides oxygen vacancies and Zn interstitials.

ZnO is a wide band gap (3.37 eV) and direct semiconductor capable of emitting ultraviolet (UV) light corresponding to the band gap. The ZnO film synthesized by thermal oxidation is typically n-type due to the native defects such as oxygen vacancies and Zn interstitials, which act as donors.[9,10] The optical emission spectrum due to these intrinsic and extrinsic defects has been reported.[12,13] The major spectral line of photoluminescence from ZnO films synthesized in a similar way as in this work has been reported to be ~380 nm (UV light) with a low intensity visual light band.[14] In contrast, the spectra of EL from ZnO structures show a broadband of emission with major peaks between 600 and 700 nm.[15] A typical spectrum obtained from the device in this work is shown in Fig. 3(a). The spectrum is very similar to the previously reported work, in which the EL shows a broad visual band but no noticeable UV

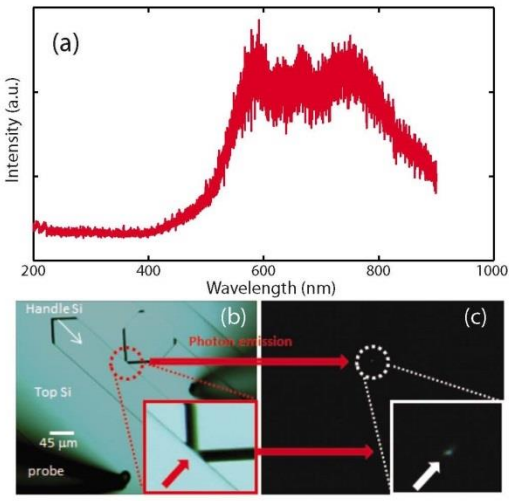

FIG. 3. (Color online) EL at 1 μA bias from the LSNZD between the gap. (a) Spectrum from the LSNZD between the naogap. Applied bias is 1 μA. (b) and (c) Insets are close-up view of the gap to show the visual light emission. The cross-sectional view (arrow in the inset) of the device is shown in Fig. 1(d).

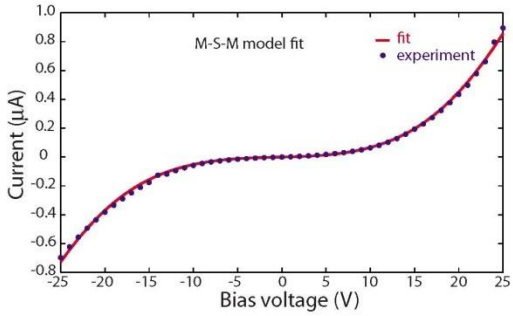

FIG. 4. (Color online) A M-S-M model fit of a measured *I-V* curve from the LSNZD. Detectable visual light (Fig. 3) has been observed at a bias voltage of 25 V.

wavelengths.[15,16] The mechanisms of the visual spectrum from ZnO due to vacancies and interstitial defects have been proposed.[13] Low UV intensity from EL could be due to relatively lower carrier density than PL and recombination of the injected carriers at defects and surfaces states more effectively than from the band edge. We believe that the visual spectrum from the LSNZD with no UV is due to dislocation-related luminescent centers including surface states and Zn vacancies.[16–18]

An optical micrograph of EL from the LSNZD is shown in Figs. 3(b) and 3(c). As described above, only the ZnO film between the nanogap is electrically active, and the light is emitted from only the ZnO between the nanogap. Figure 3(b) shows the device under and optical microscope before a bias is applied. Figure 3 shows the device under a bias of 1 μA in the dark. The light intensity from the LSNZD under the bias is bright enough to be seen through an optical microscope at 200× magnification with bare eyes as shown in Fig. 3(c).

The EL from the LSNZD can be explained with the M-S-M model as shown in Fig. 4. The work function and the electron affinity of synthesized ZnO have been reported to be 4.45 eV and 4.29 eV, respectively. The work function of Ni is 5.15 eV. The Schottky barrier heights at each junction are 0.86 eV. *I-V* measurements of the device show the typical M-S-M junction characteristic as shown in Fig. 4. The PKUMSM program[19] is used to fit the measured *I-V* data and to extract semiconductor parameters of the device such as the Schottky barriers. The extracted values of the barrier height are 0.525 eV and the 0.565 eV, respectively. The Schottky barriers at each junction are asymmetric. This asymmetry may be from the Ni–Zn alloy formation. The barrier height also deviates from the calculated value of the work functions. This difference may be from the completely depleted ZnO (Ref. 19) between the Ni covered tips. At equilibrium, the ZnO with metal contacts are completely depleted, assuming the typical doping of ZnO is $10^{17}/cm^3$. With the extracted values of the barrier heights, the energy band diagram at equilibrium is shown in Fig. 5. In a M-S-M model, V_{RT} (reach-through voltage) is defined as a voltage at which the depletion regions of J_1 and J_2 meet each other resulting in the completely depleted ZnO between the gap. When a bias less than the V_{RT} is applied to the device, the current is the sum of the reverse saturation current, generation-recombination current, and surface leakage current.[20] The

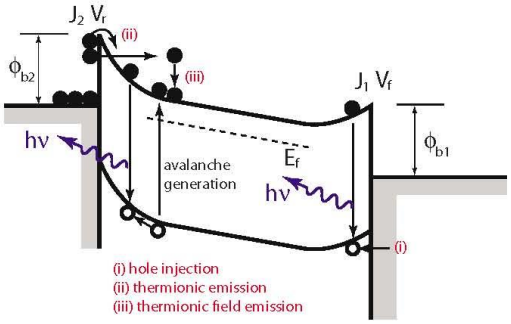

FIG. 5. (Color online) A M-S-M model of the LSNZD. Energy band diagram of Ni–ZnO–Ni under a DC bias. The left junction (J_2) is reverse biased and the right junction (J_1) is forward biased. At J_2, two electron transports are possible: thermionic emission and thermionic field emission (TFE). In TFE, electron-hole pairs can be generated by impact ionization. At J_1, holes from metal are injected. In both cases, light emission occurs. EL from the hole injection is dominant until the space-charge-limited effect occurs.

current increases exponentially with applied voltage above V_{RT} until the injected carrier density is high enough to alter the low-injection field distribution in the depletion region (the space-charge-limited effect) resulting in linear *I-V* characteristics.[20]

In the case of the LSNZD, any bias voltage is higher than the V_{RT} at the equilibrium because the LSNZD is already depleted. With this condition, the EL from the hole injection at J_1 is dominant in the LSNZD. EL from avalanche breakdown at J_2 is expected to occur at a much higher voltage, which is the voltage causing the space-charge-limited effect. In the case of LSNZD, the avalanche breakdown voltage has not been determined due to device breakdown. The measured turn-on voltage for light emission was 12.5 V. The measured light intensity from the LSNZD is shown in Fig. 6. The light intensity is taken from images using a Princeton Instruments Cascade 512B camera (CCD97). The photon-count is integrated for intervals ranging from 1 to 180 s at each measurement point and is normalized to photon-count per second. Figure 6 inset shows a close-up view of the photon rate converted from the measured intensity between the applied bias of 12.5 V and 20 V. The photon rate at 12.5 V is estimated to be ~9000/s. The photon rate increased as high as 10^7/s at 40 V. For the M-S-M devices, the holes for the EL can be injected as pulses.[21] Because the LSNZD is a piezoelectric material, emission of a single photon at a time from the LSNZD coupled with the acoustoelectric effect could be possible.[22,23]

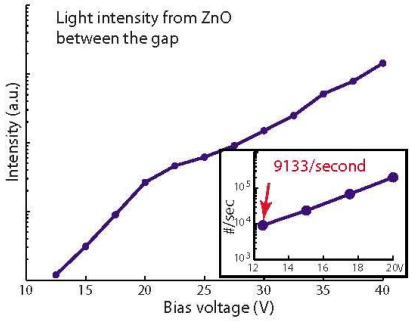

FIG. 6. (Color online) Measured light intensity from a LSNZD. The inset shows photon counts per second.

In summary, EL from a single LSNZD integrated between a micromachined nanogap is presented. A M-S-M model is used to analyze the mechanism of photon emission from the LSNZD. The measured EL spectrum shows a broad visual light band with major peaks at 680 and 750 nm. The minimum rate of measured photon emission in this work is ~9000/s with a bias voltage of 12.5 V. The feasibility of single photon emission from the single LSNZD is demonstrated. The single photon emitter is suitable for a quantum computing or quantum network applications and for chip-scale optoelectronics.

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Suspended and localized single nanostructure growth across a nanogap by an electric field

Chung-Hoon Lee[1], Jun Hyun Han[2], Susan C Schneider[1] and Fabien Josse[1]

[1] Department of Electrical and Computer Engineering, Marquette University, WI 53201, USA
[2] Department of Mechanical Engineering, Marquette University, WI 53201, USA

E-mail: chunghoon.lee@marquettte.edu

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Abstract
Direct growth of a suspended single nanostructure (SSN) at a specific location is presented. The SSN is grown across a metallic nanoscale gap by migration in air at room temperature. The nanogap is fabricated by industrial standard optical lithography and anisotropic wet chemical silicon etching. A DC current bias, 1 nA, is applied across the metallic gap to induce nanoscale migration of Zn or ZnO. The history of the voltage drop across the gap as a function of time clearly indicates the moment when migration begins. The shape of SSNs grown across the nanogap by the migration is asymmetric at each electrode due to the asymmetric electric field distribution within the nanogap. An SSN can be used as the platform for two-terminal active or passive nanoscale electronics in optoelectronics, radio frequency (RF) resonators, and chemical/biological sensors.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Electronic devices with a single nanostructure have been used as chemical/biological sensors and for tools to investigate physical phenomena in the nanoscale [1–7]. Electronic devices with reduced physical dimensions have also been used in electrical [8–10], optical [11–13], and mechanical [14, 15] applications, showing promising performance.

ZnO is a wide bandgap semiconductor [16] and a piezoelectric material [17, 18]. Due to its mechanical and chemical stability in atmosphere, ZnO has been widely used as a key component in the electrical, optical, mechanical, and sensor fields [19–25]. By using mature synthesizing techniques, various fabrication methods and shapes of ZnO nanostructures (ZNONs) have been developed [13, 26–34]. Most synthesizing methods produce ZNONs in an uncontrolled amount, in a massively parallel method, at random locations. Isolation and arrangement of a single pristine nanostructure from a batch process requires laborious serial processes that can introduce a large variation in the devices. Isolation of a single nanostructure from the ensemble and integration of the single structure with existing electronics are not only a challenge, but also time consuming. Furthermore, most devices are fabricated on a substrate that would interfere with electrical and optical functions and measurements.

In this paper, a single suspended nanostructure (SSN) grown by nanoscale migration across a nanogap is presented. This work shows a feasible way to integrate a nanoscale structure on existing electronic devices. The SSN is also an ideal configuration in electronics to minimize leakage currents. The nanogaps are fabricated by conventional optical lithography and anisotropic wet chemical silicon (Si) etching with unique double-layer etch-mask processes. These processes produce highly symmetric and reproducible nanoscale gaps as small as a few tens of nanometers with atomically sharp tips facing each other. The fabrication process does not require e-beam lithography, enabling conventional foundries to fabricate devices. Figure 1 is a scanning electron micrograph (SEM) overview of the device on which the SSN is grown, showing the nanogaps and electrical terminals.

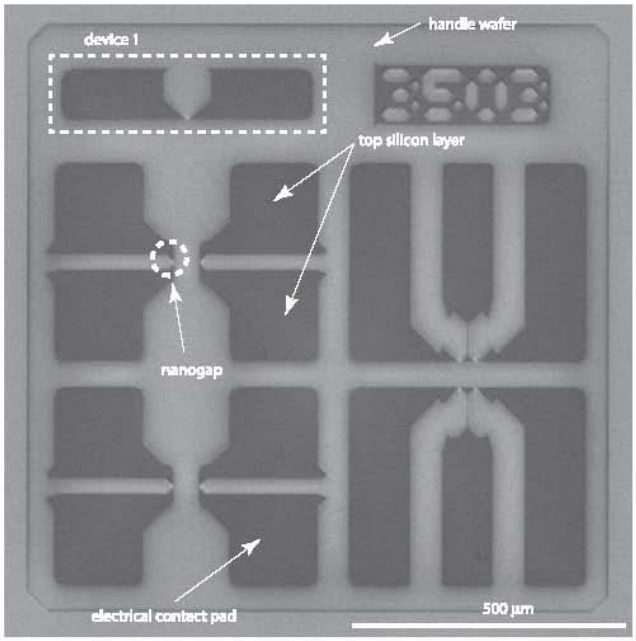

Figure 1. Overview of nanogap devices on an SOI wafer. A total of seven devices are shown. Each device consists of electrical contact pads and a nanogap.

2. Suspended nanogap fabrication

The fabrication of the nanogap starts from a silicon-on-insulator (SOI) wafer with (001) crystal orientation, 5 μm thick top Si layer, 4 μm thick buried silicon dioxide (BOX), and 600 μm thick handle wafer. The nanogap is fabricated by two sequential steps of the anisotropic wet chemical etch, potassium hydroxide (KOH). Initially, thermal SiO_2 (250 nm) film is grown, and then a low stress silicon nitride (SiN) film (300 nm) is deposited on the SOI wafer. The SiN and SiO_2 thin films serve as KOH etch-masks in subsequent fabrication processes.

At the first step of fabrication, a SiN film is patterned by optical lithography and etched by a reactive ion etch to define the overall device structure as shown in figure 2(a) representing device 1 in figure 1 for clarity. The defined pattern is aligned along the ⟨100⟩ direction of the top Si. The second optical lithography defines an etch-window for removal of the thermally gown SiO_2 film with a buffered oxide etchant (BOE) to expose Si as shown in figure 2(b). The exposed Si is etched by the first KOH Si etch. The etched Si profile is shown in figure 2(c). Due to the anisotropic characteristics of the KOH etch, the etched surfaces are the {111} and {110} planes. The {111} planes are self-terminated at an angle of 54.7° with respect to the (001) plane, while the {100} planes are undercut until the KOH etch is manually stopped. The first anisotropic Si etch is done for 20 min at 60 °C in 30% KOH. The next fabrication step is thermal oxidation of the etched Si surfaces, which serves as an etch-mask for the second KOH etch as shown in figure 2(d). The third lithography defines an etch-window for SiO_2 film removal with a BOE as shown in figure 2(e). The SiO_2 film under the photoresist (PR) protects the first etched Si surfaces during the second KOH etch. Figure 2(f) shows the etched profile of Si (dotted lines) after the second etch. At this process step, the exposed Si is not only etched, but also undercut in the ⟨100⟩ direction. After the second KOH etch the nanogaps with electrical terminal pads are fabricated as shown in figure 2(g). The KOH etch is terminated when the undercut reaches the corner of {111} planes formed at the first KOH etch step. The typical nanogap size formed with the fabrication method ranges between 40 and 80 nm. The gap is further reduced by evaporating metal layers over the tips forming the nanogap (the detail below). As a final step, the SiN film is removed in a phosphoric acid wet chemical etch followed by the BOX removal with hydrogen fluoride (49% HF). The BOX removal suspends the nanogap from the SOI handle wafer while the electrical pads are supported on the BOX, as shown in figure 2(g). A cross-sectional view of the suspended nanogap and tips is shown in figure 2(h).

3. Local SSN growth across the suspended nanogap

The nanogap is formed by moderately doped Si, p-type with 10^{16} cm^{-3} doping concentration. To increase the electrical

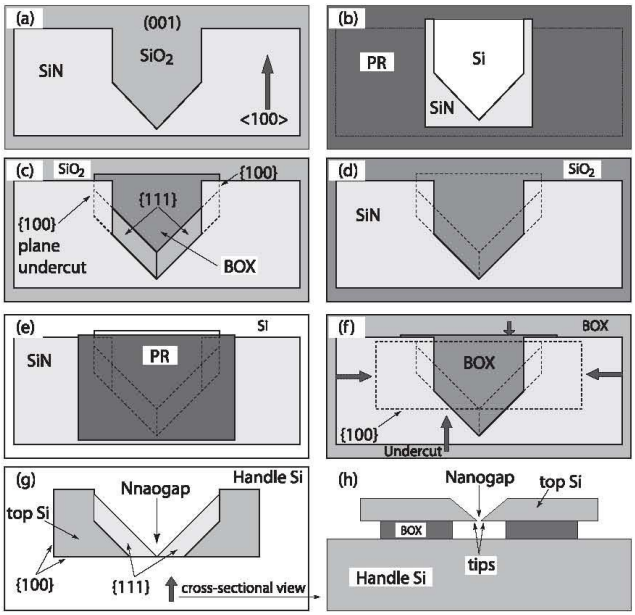

Figure 2. Process flow of nanogap fabrication. (a) SiN patterning. (b) Photolithography to selectively expose Si. (c) First KOH etch. {111} planes are self-terminated. (d) Thermal oxidation of exposed Si. (e) Photolithography exposing selected Si for the second KOH etch. (f) The second KOH etch to form the nanogap. (g) SiN film removal, and BOX undercut to suspend the nanogap. (h) Cross-sectional view of the nanogap.

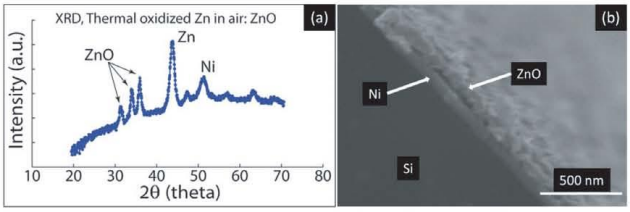

Figure 3. XRD data (a) showing the conversion of Zn to ZnO and (b) cross-sectional view of metal layers on Si. In the XRD data showing the three ZnO peaks, the peak at 51.6° indicates a Ni layer under the ZnO film after the thermal oxidation. In the SEM of the device, the Ni and ZnO layers are clearly visible. The Ni layer is uniform, while the ZnO layer shows granular texture.

conductivity of the electrical terminals for the SSN, a 30 nm thick nickel (Ni) layer is thermally evaporated over the entire device under a vacuum of 7×10^{-7} Torr. The metal evaporation is a blanket evaporation after the nanogap is fabricated (figure 2(g)). The Ni serves as the electrical leads for the SSN, which will be grown between the nanogap. The nanogap and electrode pads are fabricated on the top Si layer, which is electrically isolated from the handle wafer. Therefore, the Ni layer evaporated on the device is effectively isolated between the top layer and handle wafer, as shown in figure 2(f). A 30 nm thick zinc (Zn) metal layer is then evaporated over the Ni without breaking the vacuum to prevent oxidation of the Ni film and to promote the adhesion of the Zn film. After the metal evaporations, the device is brought to ambient conditions. Then the Zn on the device is oxidized at 500 °C for 2 h in a quartz tube furnace with 5 sccm O_2 flow. The oxidation step converts the Zn film to ZnO film. XRD data show the presence of ZnO, as shown in figure 3(a), where the peaks at 31.8°, 34.5°, and 36.2° correspond to ZnO [20, 35]. The peak at 51.6° corresponds to Ni under the ZnO film and indicates that the Ni film is intact after the Zn oxidation as shown in figure 3(b). The electrical conductivity between the electrical contact pad indicated in figure 1 and the handle wafer has been measured by a HP semiconductor analyzer right after the metal evaporation on the device. The maximum leakage current between the electrical contact pad and the handle wafer is 120

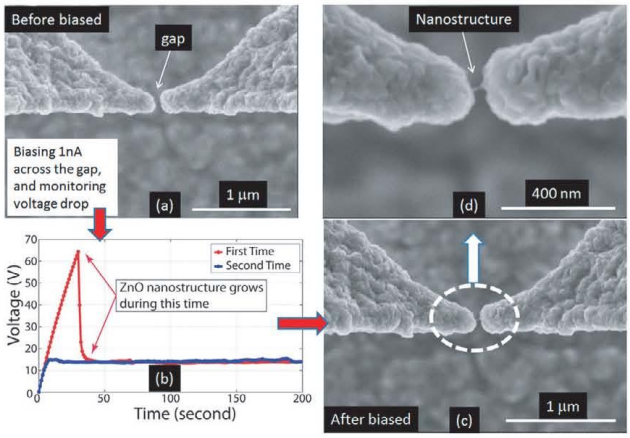

Figure 4. SSN growth between the nanogap using electromigration. (a) The tips forming the nanogap are covered with Ni/ZnO. There is still a gap at this stage. (b) A DC bias of 1 nA is applied across the gap while monitoring the voltage drop. Initially the voltage drop increases due to an open circuit. After a few seconds, the voltage drop decreases when the SSN grow between the nanogap. (c) SEM image of the device after the DC bias. (d) Magnified view of the nanogap in (c). A single nanostructure bridging the nanogap is visible.

femtoampere (fA) at a bias of 25 V. As shown in figure 1, all the devices and electrodes are separated by more than 10 μm of air, which ensures very good electrical isolation. Less than 100 fA leakage current is measured across a nanogap larger than 100 nm. Therefore, most of the current flows though the nanostructure.

Figure 4(a) shows the device with Ni/ZnO coated tips forming a nanogap. In order to account for the gap size reduction which occurs during the Ni film deposition, the initial micromachined nanogap formed by the Si tips is designed to be on the order of 40–80 nm. When the metal layers (Ni and Zn) are evaporated on the device, the micromachined nanogap is reduced by approximately 30 nm when the total metal film thickness is 60 nm. Thus, initial nanogaps formed by the Si tips which are greater than 30 nm will still have a gap after the metal evaporation stage. Finally, the SSNs are formed between the nanogap tips during the DC biasing step using a Keithley 2400 source/meter. This source is set to supply a 1 nA DC bias current with a maximum limit on the source voltage of 70 V to protect the (other) equipment used for the biasing step. When the source is applied to the device, the voltage across the device will rise as a function of time to its maximum limiting value or to the value needed to establish the 1 nA DC bias current through the device under test (the nanogap device). This voltage drop across the nanogap is monitored during the biasing step and the voltage versus time graph is shown in figure 4(b) for the device in figure 4(a). For this device, the voltage drop across the nanogap increases until 65 V, termed the breakdown-voltage, and then abruptly drops to 15 V when the gap is bridged by the SSN. Once the SSN bridge is formed across the gap, the average current density is estimated to be approximately 4.4×10^6 A m^{-2} assuming an average nanowire radius of 8.5 nm. Once the SSN bridge is formed across the nanogap, the average electric field across the SSN is estimated to be on the order of 2×10^9 V m^{-1}. It has been observed that devices with larger gap widths will dwell at the maximum voltage for up to 3 s before the SSN forms, at which time the voltage drop across the device will drop to within the range of 10–15 V. It is believed that ZnO or Zn migration occurs at the breakdown-voltage so that ZnO bridges the nanogap as shown in figure 4(c) and conduction occurs. As can be seen in the SEM image, sharp points are found on the tips. The electric field is further enhanced at the sharp point assisting the migration. As expected, most SSNs are found at the sharp point on the tips, as shown in figure 4(c). A magnified view of these tips is shown in figure 4(d) and clearly shows the nanostructure between the nanogap.

4. Discussion

Although the exact mechanism of the nanostructure growth across the nanogap is still under investigation, field ion emission or electromigration are likely candidates to explain the growth mechanism due to the high electric field. Zn ion migration in nanoscale from a ZnO film by thermally assisted electromigration has been reported, where Zn nanostructures on a ZnO film surface are formed rather than ZnO structures because the experiment is performed in a tunneling electron microscope with a high vacuum [36]. The migration of Zn ions is induced by Joule heating and electrical current flow when a tungsten probe touches the surface of the ZnO film with a DC bias. The driving forces of Zn ion migration to the ZnO film surface are both 'direct' and 'wind' force [36, 37]. In contrast, the SSN in this work is grown by electric field alone because there is no current flow (therefore, no Joule heating) until the nanogap is bridged by migration of Zn or ZnO from the tip(s). Zn/ZnO ion migration across the nanogap in our work could be due to field ion emission [38]. Zn/ZnO ions in the anode can drift in the direction of the electric field [39]. In the case of Zn

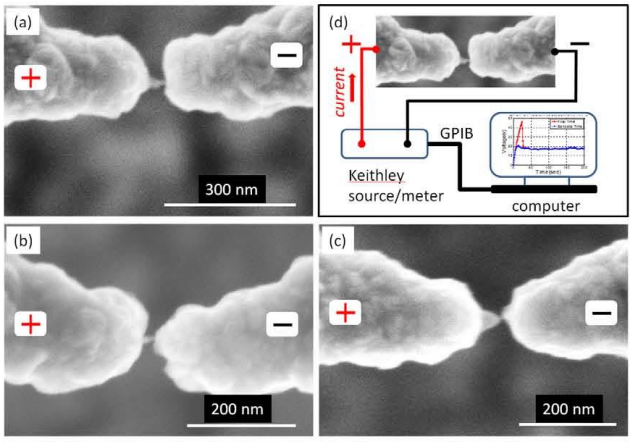

Figure 5. SEM images of SSNs between the nanogaps. Three different nanogaps, (a)–(c), show different asymmetric shapes of SSNs. (d) A Keithley source/meter is used to bias 1 nA DC current and for monitoring the voltage drop across the nanogap.

ion migration across the nanogap, the Zn ion would be oxidized to form ZnO because the experiment in this work is done in air, where O_2 is available for oxidation of Zn to ZnO. The typical electrical resistance of the nanostructures across the nanogap is in the range of gigaohms, while the electrical resistance of the Zn nanostructure integrated in a similar nanogap device is well below the megaohm range. It is most likely that the SSN is formed by ZnO because other experiments using only the Ni film or Zn film alone do not form a SSN.

It is noticed that the SSNs grown between the tips are asymmetric, as shown in figures 5(a)–(c). Figure 5(d) shows the experimental setup. The SSN on the positive terminal tip is larger than that of the negative terminal. The formation and shape of the SSNs is consistent in 20 of the 25 devices used in this work. Because the nanogap sizes of the other five samples are less than 10 nm, multiple SSNs grew across the nanogap and the shape is more symmetric. With the experimental setup in this work, the location of SSN growth initiation is undetermined. However, it is considered that the local distribution of electrons at a sharp point on the negative potential terminal will be high, resulting in the high local electric field. Electrons can tunnel through the potential barrier from ZnO at the negative electrode with high momentum due to the enhanced electric field. The momentum is high enough to ionize the ZnO or dissociate Zn into Zn ions [36] on the positive potential terminal. The ions (ZnO or Zn) can migrate to the negative terminal due to the electric field. Mass transport toward a cathode under a direct electric field has been reported [40]. The electrons which tunnel through could have vertical momentum with respect to the bias direction. Therefore, ionization of ZnO or Zn can occur in a finite solid angle at the positive terminal, so the SSN is anticipated to have a conical shape.

The physical and electrical properties of SSNs have been monitored after another DC bias of 1 nA was applied to the

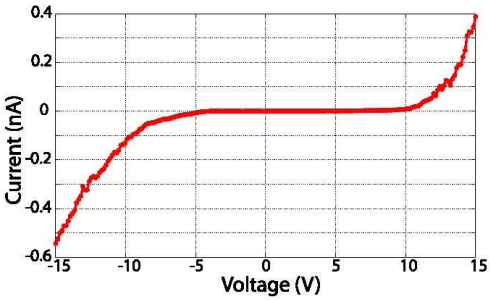

Figure 6. I–V curve of the device shown in figure 5 (a). The I–V data show M–S–M junction characteristics, which is a back-to-back Schottky diode.

structure for 24 h in air at room temperature. No further shape changes of the SSNs have been observed in SEM images and the resistance of the SSNs changes by no more than $\pm 5\%$ of the initial resistance value. The typical resistance at 1 nA bias across the SSN is 10 GΩ calculated using the value in figure 4(b). The resistance of the SSN is one order of magnitude higher than that of a ZnO nanorod [41]. To investigate the causes of the high resistance, I–V curves of the SSN are measured using an HP4145 semiconductor analyzer. In figure 6, the I–V curve is measured after the nanostructure has been grown across the nanogap. The voltage is swept across the device and the current is monitored. The voltage bias is limited to ± 15 V because of the tendency to damage the nanostructures by burn through. The I–V data in figure 6 show a typical metal–semiconductor–metal (M–S–M) junction characteristic [42, 43]. The Ni metal used as the electrode in this work will form a Schottky contact with ZnO. In the M–S–M configuration with Schottky contacts at both junctions, one

of the junctions is always reverse biased when a bias is applied. The charge carrier transportation is limited by the Schottky barrier [44]. Assuming that a typical carrier concentration of ZnO is 10^{17} cm^{-3}, the depletion width in ZnO is approximately 70 nm at each junction. The mobile carriers in SSN are completely depleted [44]. The Schottky barrier along with mobile carrier depletion and the small cross-sectional area of the SSN at the negative terminal may be the major causes of the high resistance.

5. Conclusions

Direct growth of a suspended single nanostructure (SSN) at a specific location is presented. The nanogap formed by atomically sharp tips is fabricated on an SOI wafer with a conventional optical lithography and anisotropic wet chemical Si etch. The nanogap fabrication can be CMOS compatible allowing integration with Si-based electronics. Because the fabrication of the device is versatile, various materials could be integrated across the nanogap. An SSN is grown between a nanogap by a localized electric field in ambient conditions at room temperature with a DC current bias of 1 nA. The migration event has been detected by monitoring the voltage drop across the nanogap while applying a bias current. Electrical characteristics of the SSN are discussed using the M–S–M model. As a two-terminal active or passive electronic device, the SSN can find applications in optoelectronics [28, 44, 45], RF resonators [7, 46], and chemical/biological sensors [47–49].

Acknowledgments

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A suspended nanogap formed by field-induced atomically sharp tips

Jun Hyun Han,[1] Kyung Song,[2] Shankar Radhakrishnan,[3] Sang Ho Oh,[2] and Chung Hoon Lee[1,a)]

[1]*Nanoscale Devices Laboratory, Marquette University, Milwaukee, Wisconsin 53233, USA*
[2]*Department of Materials Science and Engineering, Pohang University of Science and Technology (POSTECH), Pohang 790-784, Korea*
[3]*Agiltron Inc., 15 Presidential Way, Woburn, Massachusetts 01801, USA*

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A sub-nanometer scale suspended gap (nanogap) defined by electric field-induced atomically sharp metallic tips is presented. A strong local electric field ($>10^9$ V/m) across micro/nanomachined tips facing each other causes the metal ion migration in the form of dendrite-like growth at the cathode. The nanogap is fully isolated from the substrate eliminating growth mechanisms that involve substrate interactions. The proposed mechanism of ion transportation is verified using real-time imaging of the metal ion transportation using an *in situ* biasing in transmission electron microscope (TEM). The configuration of the micro/nanomachined suspended tips allows nanostructure growth of a wide variety of materials including metals, metal-oxides, and polymers. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4764562]

Platforms that use nanoscale gaps (nanogaps) defined by metallic tips have been investigated extensively due to their ability to synthesize and/or characterize nanoscale electronic structures.[1–6] Typically, research on nanogap platforms has focused on only reducing and controlling the size of the nanogap in sub-nanometer length scale without controlling the radii of curvature of the tips. This leads to tethering or growth of nanostructures of interest in uncontrolled orientations and material states. Additionally, in most of these platforms, the nanogaps are in direct physical contact with the substrate, making it difficult to decouple the electrical, magnetic, chemical, or mechanical interactions between the nanostructure and the substrate.[7,8]

In this letter, the ability to define a precise nanogap size and tip radius of curvature by directly controlling tip-to-tip interaction using an external electric field is presented. A nanogap platform that is truly isolated from substrate with atomically sharp tips of less than 1 nm radius of curvature is presented. Metal ion transport at the cathode tip by an externally applied electric field results in host metal dendrite growth. The grown tips forming the nanogap are self-aligned to each other due to the applied local electric field.

Metal ion migration at nanoscale is an important mechanism in ionic-electronics, e.g., in resistance switching used in memristors.[9–11] The migrated ions can be used in bottom-up synthesis of nanostructures, defined to the atomic scale. Using controlled atomically sharp tip growth and precise gap size, the nanogap can be an optimal platform for molecular electronics.

The fabrication of the nanogap has been done in two separate steps. The first step is to fabricate a suspended nanogap of length between 5 nm and 80 nm with tip radii of curvatures between 5 nm and 7 nm using bulk-micromachining. In the second step, a voltage applied across the nanogap results in metal cations to extrude out, directed by the induced electric field, forming self-aligned atomically sharp tips (with radii of curvature <1 nm). The detailed sequence for the first step to form the micromachined nanogap has been described elsewhere.[12] Fig. 1 shows a scanning electron micrograph (SEM) of the micromachined nanogap fabricated on a silicon-on-insulator (SOI) wafer, in which the nanogap is defined by patterning the silicon device layer. Typical radii of curvature of the silicon tips are in the range of 5–7 nm with nanogap lengths of 20–100 nm. The silicon tips and contact pads are then isolated from the substrate by removing the buried oxide layer in 49% aqueous hydrofluoric acid solution. The suspension of nanogap ensures mechanical and electrical isolation from the substrate. The nanogap device is coated with a low-stress silicon nitride (SiN_x) thin film to prevent silicide formation when contact metal (~60 nm of nickel) is thermally evaporated on the tips and pads. The SiN_x and metal film coating results in the reduction of the initial gap to 5–80 nm, depending on the micromachined initial gap. The metal film on the pads serves as an electrical conductor for a bias across the gap. The metal film on the tips is a source of metal ions, which become mobile when an electric field is applied across the tips. A nanogap formed by tips coated with 60 nm thick nickel layer by thermal evaporation was used to investigate the metal ion migration under an electric field. A 10 nA DC current bias is applied across the

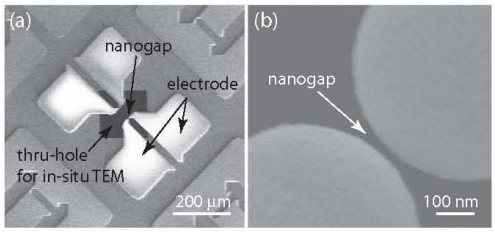

FIG. 1. (a) Overview of nanogap formed by suspended micro/nanomachined tips on an SOI wafer. Electrodes and the tips are electrically isolated from the substrate. (b) A close-up SEM view of the nanogap.

a)Electronic mail: chunghoon.lee@marquette.edu.

nanogap, and the maximum voltage drop across the nanogap is limited to 100 V (using bias compliance), that is, the voltage drop is limited by an external circuit. The nanogap forms and open circuit initially, causing the initial current to be zero. High electric field strengths ($\sim 10^9$ V/m) at the tip causes metal ions to migrate out from the negatively biased tip (cathode). The migrated ions result in the cathode to extrude out to form a dendrite-like nanostructure. The nanostructure growth by the ion migration is directed towards the anode tip, where the electric field is highest. Fig. 2 shows *in situ* TEM images of the nanostructure growth sequence in time due to the metal ion migration from the cathode tip.

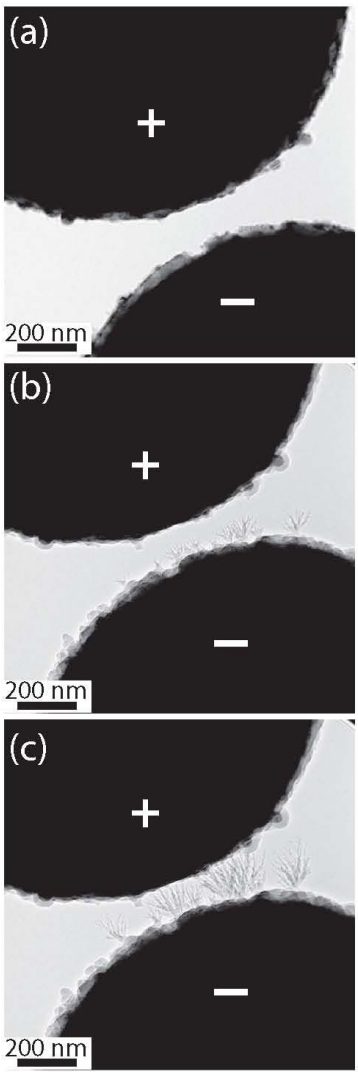

FIG. 2. *In situ* TEM images during a nanostructure growth. Bias polarity is indicated on the tips. (a) Ni covered nanogap at the beginning of bias, (b) dendrite nanostructures start to grow, (c) fully grown nanostructures.

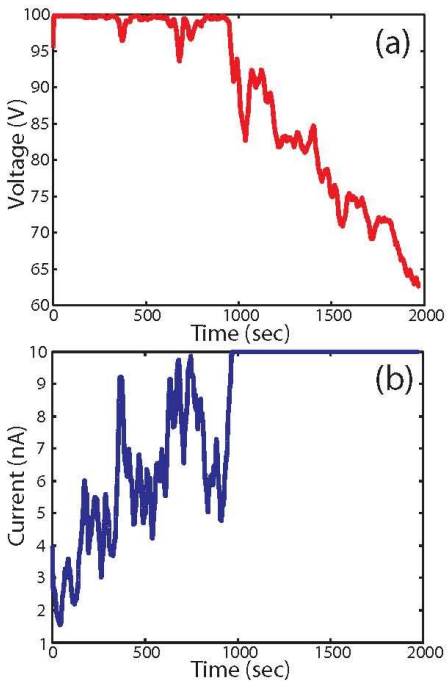

FIG. 3. Measured DC bias during the growth. (a) Voltage drop across the nanogap. (b) Current profile across the nanogap.

When the ion migration occurs at the cathode tip, the electrical current across the nanogap increases as shown in Fig. 3. Although the current fluctuates throughout the growth phase of the tip, it shows an increasing trend till it equals the set bias current of 10 nA, which indicates that the tip from the cathode has bridged the nanogap. We suggest that the fluctuation of the current is due to the multiple nanostructure growth on the cathode tip, which distorts the local electric fields. The length and growth rate of the nanostructure is shown in Fig. 4, showing a growth rate of ~ 0.04 nm/s during the most of growth duration. The growth rate of the nanostructure increases as the tip approaches the anode, which is explained by the increase in electric field across the nanogap as the distance between the tips gets progressively shorter. Results from energy-filtered TEM (EFTEM) supports this growth mechanism by showing that nickel is one of the two predominant materials grown (Fig. 5). The presence of carbon is likely an artifact due to electron-beam induced deposition during *in situ* TEM experiment.[13]

In general, nanostructure growth by metal ion migration under an electric field can be due to one or more of the following four different mechanisms: electromigration,[14] field ion emission,[15] cation migration,[8] and anion migration.[10] The mechanisms of both the field ion emission and cation migration on a substrate are caused by the electrochemical growth and dissolution of metallic filaments at the anode.[8,10,15] Cation migration is also closely related to the ion mobility in the substrate materials (specifically, in dielectrics).[8] On the other hand, anion migration has been

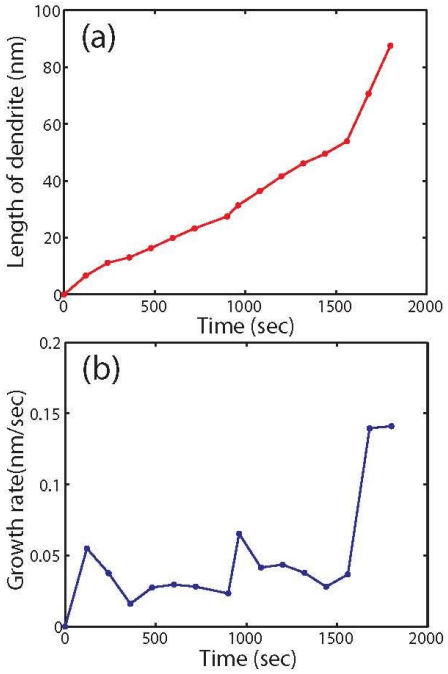

FIG. 4. (a) Length of the nanostructure growth as a function of time. (b) Growth rate.

described by the migration of oxygen vacancies toward the cathode,[10] which also depends on the interaction with the host material. In the current work, since the nanogaps are fully suspended, any direct interactions between metal ions and the substrate can be excluded. Thus the ion-migration is solely due to the interaction with the electric field and/or electron tunneling current. Eliminating the mechanisms that are explained based on substrate interaction, it is postulated that the ion migration occurs only at the cathode tips. This is also supported well by *in situ* TEMs during growth showing dendrite nanostructure growth occurring at the cathode tip with no discernible change at the anode tip. This result is in contrast to metal filament growth at the anode reported in Refs. 8 and 15. Based on the *in situ* real-time TEM images of the growth and the ex situ study reported before,[12] it is likely that the nanostructure growth is due to the ionization of Ni and/or NiO by electron tunneling (Fig. 3) and transport of the ions under the high electric field at the cathode.[16] The dendrite form of the nanostructure growth is suggested to be due to the local electric field distortion by the nanostructure.[8] The tip radius of curvature of the dendrite is typically less than 1 nm as grown.

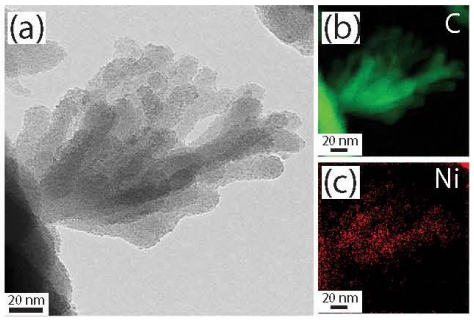

FIG. 5. Elemental mapping by EFTEM analysis for the grown nanostructure in Fig. 2. (a) the grown nanostructure, (b) carbon, and (c) Ni.

A method to fabricate a precise nanogap with atomically sharp metallic tips formed by field-induced ion transport has been presented. The growth of metallic nanostructure was imaged in real-time using *in situ* TEM and was used to identify the ion migration mechanism under the applied electric field. The composition of the grown nanostructure was demonstrated to be the same as the host material using EFTEM analysis. By coating the suspended tips with different materials such as metals, polymers, and oxide-based materials, a wide range of materials can be grown, making this a versatile platform for nanoscale synthesis and characterization. The growth by ion migration occurs at atomic scales, resulting in a dendrite nanostructure due to a localized high electric field. The distance between the tip of dendrite and the other electrode can be controlled by terminating bias at the desired nanogap size. The atomically sharp tip formed by ion-migration could be optimal electrodes as a nanogap platform for single-molecule electronics.

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A novel batch-processing method for accurate crystallographic axis alignment

Jun Hyun Han[1], **Shankar Radhakrishnan**[2] **and Chung-Hoon Lee**[1]

[1] Nanoscale Devices Laboratory, Marquette University, WI 53201, USA
[2] Agiltron Inc. 15 Presidential Way, Woburn, MA 01801, USA

E-mail: chunghoon.lee@marquettte.edu

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Abstract
A new method for the accurate alignment of lithographically-defined patterns to the crystallographic axes of substrates is presented. We provide a lower (worst-case) limit of the achievable high aspect ratio using anisotropic wet chemical silicon etch for deep trenches. The method uses the fact that the intensity of light reflected from two sets of gratings, one on the photomask and the other on the substrate, is a sharp function of their relative angular misalignment. By using pre-etched gratings on the substrate formed by wet anisotropic etching, alignment accuracies better than 50 millidegrees with respect to silicon crystallographic axes have been demonstrated. Two types of microstructures—trenches with an aspect ratio >90:1 and silicon nanowires with widths <50 nm with atomically smooth etched facets—have been fabricated using i-line lithography to illustrate some applications of this alignment method. This all-optical method is readily applicable to industry-standard optical lithography and avoids the need for any individualized process steps, enabling cost-effective micro/nanostructure manufacturing.

(Some figures may appear in colour only in the online journal)

1. Introduction

Anisotropic wet chemical etching has been extensively studied and used for the fabrication of silicon micro and nanostructures [1–6], making use of high differences in etch rates between silicon's (1 1 1) family of planes and those with other Miller indices in certain alkaline etchants [7–11]. Two particular advantages of using anisotropic wet etch of silicon are the ability to produce atomically smooth etched surfaces [12] and complex 3D nanoscale shapes [13, 14], as in the case of tips for atomic force microscopy (AFM tips). Of particular interest is the use of (1 1 0)-oriented silicon substrates to produce microstructures with vertical sidewalls, since there exist two sets of (1 1 1) family of planes that are perpendicular to a (1 1 0) plane [15], giving the ability to fabricate dense, high aspect ratio structures in silicon. Such structures can be useful in many different applications. Some areas of current interest are devices that require a high surface area with minimal damage to the silicon crystalline structure such as semiconductor PN or PiN sensor arrays [16, 17] or secondary battery electrodes [18]. Other applications such as optical to x-ray diffraction gratings [19, 20] as well as some biosensors [21] can be designed to exploit vertical, atomically smooth sidewalls. In these applications, the use of deep reactive ion etch (DRIE) is not always attractive due to high levels of sidewall roughness and crystal damage generated by the process, in spite of its ability to produce structures of aspect ratios of 50:1 or better [22]. One approach to reduce the etch damage is to use anisotropic wet etchants to smoothen out rough sidewalls. Such methods offer only limited improvement unless the etch faces are exactly along (1 1 1) planes, as any other planes would result in significant undercut and/or distortion due to the anisotropy of the etch process.

2. General principles for aligning with respect to substrate crystallographic axes

The main limitation for the accurate angular alignment (henceforth simply referred to as alignment) of a designed pattern to the substrate's crystallographic axes is that major flats in the substrates that specify the crystal orientation are typically accurate to only $\pm 0.5°$ [15, 23]. Such a misalignment

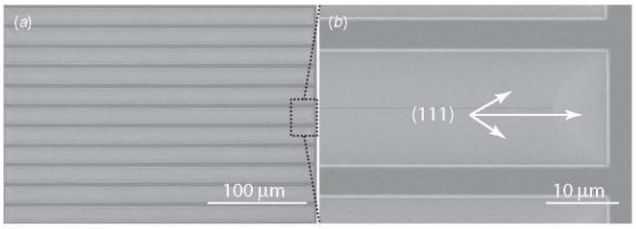

Figure 1. Rectangular gratings on the (1 0 0) silicon substrate after anisotropic wet etch. (*a*) A 12 h long etch using 30%-KOH at 70 °C. (*b*) Close-up view of the area defined by box in (*a*) showing smooth (1 1 1) crystal planes.

can change the etch rate of the crystal planes and cause significant facet undercuts, resulting in the distortion of the etched structures compared to the desired structures [7]. The general method for accurate alignment to the substrate's crystallographic axes consists of first etching a set of marks using coarse alignment (e.g. using the substrate's major flat) to the substrates axes. The marks are designed to exploit the considerably lower etch rates of (1 1 1) planes compared to non-(1 1 1) planes, typically with etch rate ratios of 1:100 or lower. Examples of such patterns are wagon-wheel-shaped, wedge-shaped and fan-out gratings that are etched using anisotropic wet chemical etchants of silicon substrates, revealing silicon crystal planes [7, 24, 25]. By inspecting the relative sizes of the patterns (typically using a scanning electron microscope (SEM)) that are misaligned to the substrate's crystallographic axes by different angles, it is possible to determine which of the angles in the design coincides with the substrate's axes the closest. Using such methods, crystal alignment accuracies of 50 to 100 millidegrees (mdeg) have been demonstrated. However, the need for several sets of marks corresponding to different levels of misalignment significantly reduces the process throughput, since each substrate requires the identification and marking of the set of marks corresponding to the closest alignment.

3. A novel all-optical crystal alignment method

In this paper, a new all-optical method is presented where gratings on a photomask are aligned to pre-etched gratings on the substrate. The intensity of reflected microscope light is a strong function of the angular misalignment between the two gratings. By integrating a photodetector at the end of the eyepiece lens of a contact mask-aligner to monitor the reflected light intensity, accurate alignment to the substrate crystallographic axes is achieved without the need for individualized wafer marking or processing. We demonstrate two types of structures that were designed to exploit the high anisotropy of certain wet etchants in silicon, showing alignment accuracy of 50 mdeg or better. First is a periodic dense array of high aspect ratio trenches that are 90 μm deep, 2 μm wide and with 4 μm pitch on (1 1 0)-oriented silicon substrates. The second are 50–100 nm wide suspended silicon nanowires with atomically smooth etch facets fabricated on (1 0 0)-oriented silicon-on-insulator (SOI) substrates.

Two periodic grating patterns, one on the substrate and the other on the optical photomask, are used to align to the substrate's crystallographic axes. The gratings on the substrate are initially defined near the substrate periphery and with an orientation coarsely aligned to the substrate's major flat. The gratings are then etched using an anisotropic wet etchant. For both (1 0 0) and (1 1 0)-oriented substrates, the gratings will be bounded by (1 1 1) planes. The coarse alignment using the major flat of the substrate can easily result in $\pm 0.5°$ misalignment with respect to the substrate's crystallographic axes. This misalignment can cause the (1 1 1) planes to show 'steps' along the grating sidewall [7]. A long anisotropic etch is therefore typically used to reduce the steps and to reveal the true crystal planes of the substrate. For e.g., due to the high etch rate ratio of higher Miller index planes to (1 1 1) plane, a 12 h long etch with a 30% wt/vol potassium hydroxide solution (30% KOH) at 70 °C has resulted in smooth (1 1 1) planes as shown in figure 1. This long etch is necessary to ensure that the (1 1 1) plane is a single plane along the crystal direction with minimal steps, which will be used as a reference for the device alignment.

The gratings on the optical photomask are then aligned to the gratings on the substrate. When the gratings on the wafer and optical mask are overlapped, the location of gratings on the substrate is aligned to be parallel and alternated with respect to the gratings on the optical mask, as shown in figure 2. In this configuration, microscope light, such as one used in a mask-aligner is shone on the overlapped gratings. The intensity of the light that is normally reflected back is measured using a photodetector mounted on an eyepiece of the contact mask-aligner. When light is shone on the overlapped gratings, the light is normally reflected only by the areas between the (1 1 1) planes on the substrate and gratings on the optical mask (chromium). The etched areas on the substrate either scatter or reflect the incident light off-normally as they are non-parallel to the substrate and hence appear dark under the optical microscope. When the gratings on the substrate and the optical mask are misaligned, the normally reflecting areas overlap each other, resulting in the reduction in the total reflected light at the photodetector, as shown in figure 2(*a*). The maximum normally reflected light intensity from the overlapped gratings is obtained when the gratings on the substrate are perfectly aligned parallel to the grating in the optical mask, as shown in figure 2(*b*). The normally reflected light intensity from the overlapped gratings is thus a strong function of the alignment

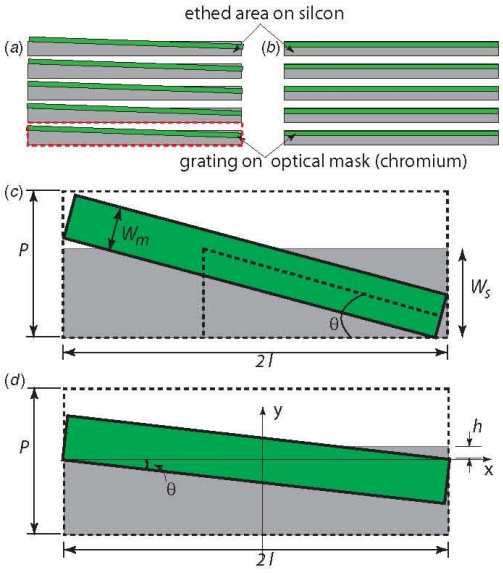

Figure 2. Schematic of alignment of gratings on wafer and optical mask: (*a*) misaligned, (*b*) aligned to the crystal direction. (*c*) Single (grating) cell illustrating the parameters of the gratings. (*d*) Close-up view of the overlapped area for calculation of fine alignment.

of the gratings on the mask and the substrate. Crystal direction alignments of 50 mdeg have been demonstrated using this method.

3.1. Initial coarse alignment

Figure 2(*a*) shows the general case where the gratings on the optical mask are slightly misaligned ($\theta < 0.5°$) and rotated with respect to the centre of the pre-etched gratings on the wafer. The relative vertical displacement of the two gratings is such that the maximum amount of the normally reflecting portion of the gratings on the photomask overlaps the etched gratings on the wafer, thus reflecting the maximum amount of light for this angular misalignment. One cell of the grating that is periodically repeated with pitch, P, is shown in figure 2(*c*). The total area per cell that reflects light normally is $2Pl - 2W_s l + A_{\text{overlap}}$, where A_{overlap} is the area of the etched groove that is covered by one grating in the mask. Here, W_s and W_m are the widths of each grating on the substrate and photomask, respectively, and l is the half-length of the gratings (on the mask and the substrate). For small angles of misalignment (i.e. $\theta < 0.5°$), A_{overlap} can be calculated as $W_m \cdot (W_s - W_m/2)/\theta$. Thus, the light intensity at the photodetector is proportional to

$$I(\theta) \propto 1 - \frac{W_s}{P} + \frac{W_m \cdot (W_s - W_m/2)}{2Pl} \cdot \frac{1}{\theta}. \quad (1)$$

This expression is valid until the gratings on the mask can be entirely enclosed by the gratings on the wafer, i.e. for all $\theta > \theta_{\text{min-coarse}} = (W_s - W_m)/2l$. It can be shown that this

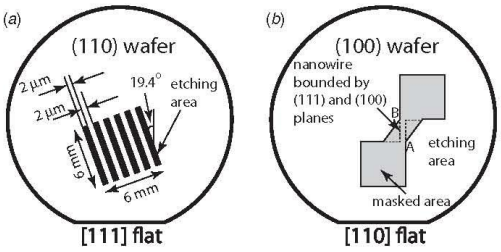

Figure 3. Device patterns. (*a*) Patterns for deep trenches on a (1 1 0) wafer with [1 1 1] major flat. (*b*) Patterns for nanowire on a (1 0 0) SOI wafer with [1 1 0] major flat.

$\theta_{\text{min-coarse}}$ represents the angular misalignment of the gratings on the wafer with respect to the crystallographic axes of the substrate. Hence, the initial coarse alignment guarantees an angular alignment better than alignment schemes only using wafer major flat ground by the manufacturer.

3.2. Fine alignment

Once the photomask and the substrate are aligned to be within $\theta_{\text{min-coarse}}$, the gratings on the optical mask are aligned to the substrate, as illustrated by the general case in figure 2(*d*). The approximate overlapped area during coarse alignment can be calculated as a function of the angular misalignment, θ. If h is the height of the portion of optical mask outside of the pre-etched silicon groove, then $h = l \tan\theta$. The overlapped area is $A_{\text{overlap}} = (l/2)h \approx (1/2)l^2\theta$. Therefore, the normalized light intensity can be obtained by total reflecting areas on the optical mask and wafer less the overlapped area,

$$I(\theta) \propto 1 - \frac{l}{2m} \cdot \theta, \quad (2)$$

where m is the distance between gratings on the optical mask and those on the wafer. The overlapped area is proportional to the misaligned angle and the length of the gratings. As can be seen from figure 2(*b*), the maximum reflected light will be registered on the photodetector when the gratings on the optical mask are parallel to and aligned inside the pre-etched gratings on the wafer. To maximize the signal at the photodetector, the grating length should be larger than the field of view of the microscope. The accuracy of angular alignment during fine alignment would typically be limited by the signal-to-noise ratio at the photodetector and/or the resolution of the rotation stage on the contact mask-aligner.

4. Device fabrication

Two types of nanostructure devices were fabricated to illustrate the use of this alignment method, usable for both (1 1 0) and (1 1 0)-oriented silicon substrates. Figure 3 shows the masks relative to the substrate surface type and the crystallographic axes, as coarsely defined by the major flat of the substrate.

In both cases, the fabrication process starts with low-pressure chemical vapor deposition of 300 nm of silicon-rich silicon nitride (SiN_x). The SiN_x film served as the etch mask

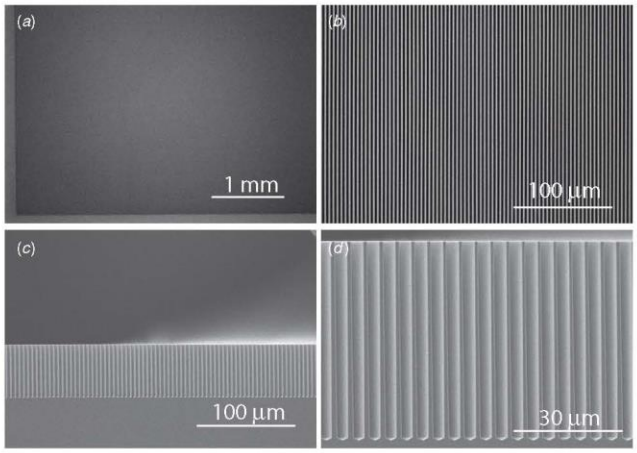

Figure 4. Deep trenches on a (1 1 0) wafer. (*a*) Top view of the 1500 trenches. (*b*) Close-up view of the (*a*). (*c*) Overview of the cross-section of the trenches. (*d*) Close-up view of (*c*).

to define the set of gratings on the substrate to be used for the crystallographic alignment. Substrate gratings that were 300 μm long, 10 μm wide with a 20 μm pitch were defined using a Karl–Suss MA-6 contact mask-aligner on both the (1 0 0) and (1 1 0)-oriented substrates, using the substrate major flats for coarse alignment. The grating patterns were transferred to the SiN_x thin film using reactive ion etching (RIE). Then, the grating patterns were etched in 30% KOH at 70 °C for 12 h. Since the alignment of the substrate gratings is only approximate, the width of etched areas is typically wider than the designed value, as shown in figure 1. After the KOH etch, the SiN_x thin film is selectively removed using hot phosphoric acid etch. The alignment method described in section 3 is then performed where the same photomask used to define the substrate gratings is aligned with respect to the pre-etched gratings on the two substrates until the light intensity at the photodetector is maximum, representing that the mask is aligned to the substrates axes with maximum possible accuracy. Two alignment marks on the photomask are lithographically transferred to the substrate. In our case, we transferred alignment keys for a GCA i-line optical stepper to the left and right of the wafer. At this stage, the silicon substrates have alignment marks that are accurately aligned to the substrate's crystallographic axes.

4.1. High aspect ratio trenches

Figure 3(*a*) shows a periodic array of a rectangular 'trench' (dark regions) structures with a width of 2 μm and a pitch of 4 μm. The trenches are 6 mm long. The pattern is designed such that the trenches are aligned to a set of (1 1 1) planes that are vertical to the (1 1 0) substrate. After the crystallographic axis alignment, a 300 nm low-stress SiN_x is deposited on the (1 1 0) silicon substrates to serve as the etch mask during deep trench etch using KOH. The above-described pattern was transferred to the SiN_x using RIE, and the trenches etched using a 30% KOH etch at 70 °C. The high aspect ratio trenches on the (1 1 0) wafer are shown in figure 4. Figure 4(*a*) shows the top view of the 6 mm long, 2 μm wide and 50 μm deep trenches. The total number of trenches is 1500 along the 6 mm die size. Figure 4(*b*) shows a close-up image of figure 4(*a*). Figures 4(*c*) and (*d*) show the cross-section views of the trench. Using high-magnification SEM, we estimated the maximum variation in etch depth of <1 μm. This represents a depth non-uniformity of less than 2%.

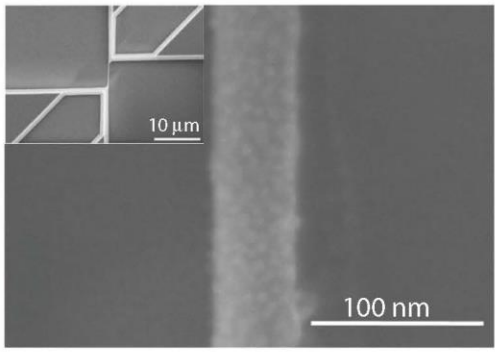

Figure 5. A fabricated suspended silicon nanowire (5 μm long, 50 nm wide and 50 nm thick). Inset is the overview of the nanowire. Due to the metal evaporation (5 nm thick) for SEM imaging, the surface and edge of the nanowire looks rough.

4.2. Silicon nanowires with sub-lithography resolution widths

Figure 5(*a*) shows the designed pattern on a (1 0 0)-oriented device layer on an SOI substrate, where the grey regions represent the masked areas. The dotted lines represent the (1 1 1) planes on the substrate with respect to the [1 1 0] major

flat. The etch of high Miller index planes results in a rapid undercut of the masked device layer until the (1 1 1) planes are exposed. The width of the resulting structure under the etch mask is then defined only by the offset of the masked areas (the distance between the dotted lines), which can be designed to be much smaller than optical resolution limits. By aligning to the crystal axis of the (1 0 0)-oriented device layer accurately, silicon nanowires of approximately 50 nm width and with atomically smooth sidewalls are presented below.

After accurate crystal alignment described in the previous section, a silicon dioxide (SiO_2) film was thermally grown on the (1 0 0) SOI substrates. The initial device layer thickness was 270 nm thick, which was thinned down to ~50 nm by controlled thermal oxidation. The thermally grown oxide was used as a KOH etch mask for the nanowire patterning. The corners A and B are offset with respect to the [1 1 0] direction as shown in figure 3(*b*). The offset between the A and B is the designed nanowire width bounded by (1 1 1) planes [6]. The initial offset (in mask layout) between A and B in figure 3(*b*) is 250 nm. This offset is reduced further by using a timed isotropic etch of the masking SiO_2 layer using a 6:1 solution of buffered oxide etchant (BOE 6:1). The device layer is then etched using a 30% KOH solution at 70 °C. The device layer undercuts under the SiO_2 mask until the (1 1 1) planes shown as dotted lines become exposed. Thus, silicon device layers that were 5 μm long, 50 nm wide and 50 nm thick were defined. Finally, the silicon device layer was released from the buried oxide layer using a 49% hydrofluoric acid etch to form 50 nm wide suspended silicon nanowires with atomically smooth sidewalls as shown in figure 5.

5. Discussion

Although anisotropic wet chemical silicon etches have been extensively used for micromachining and the processes well developed, the etch rates and etch profiles are typically dependent on a wide range of parameters such as doping concentration in silicon, chemical bath concentration, temperature and additives [26]. For high aspect ratio structures, the etch rate ratios of high Miller index planes to that of a (1 1 1) plane and the alignment are critical. To determine the maximum achievable aspect ratio for a given etch condition, a series of gratings were designed as shown in figure 6. Each grating set was rotated 50 mdeg successively with respect to the central grating set, up to ±1° in both directions. The grating in the centre series is designed to be aligned with the designated crystal plane direction, [1 1 1] direction in the trench array microstructure case. Using this method, the maximum possible etch depth as a function misaligned angle was experimentally obtained. The gratings most misaligned with the [1 1 1] crystal direction suffered the most severe undercut, as easily visualized by an optical microscope. Using the method described in this paper, we achieved the least amount of undercut for the grating set in the middle, indicating an alignment accuracy better than 50 mdeg.

In the following, we calculate the relation between the alignment accuracy and the achievable aspect ratio of deep

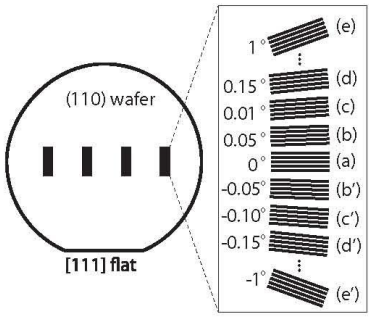

Figure 6. Printed series of gratings aligned along the pre-etched [1 1 1] direction on (1 1 0)-oriented wafer. Each grating is 0.05° rotated successively up to ±1°.

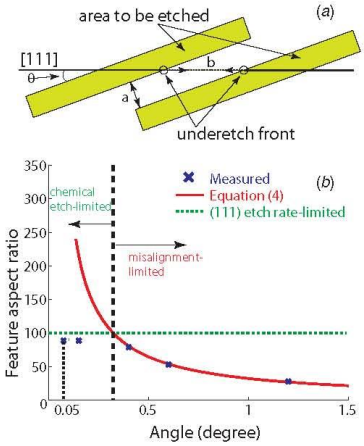

Figure 7. Limit of achievable trench depth for the case of 2 μm trench width and 4 μm pitch gratings by misalignment and (1 1 1) etch rate. (*a*) Schematic description of (*h k l*) underetch front along the [1 1 0] direction with misaligned gratings. (*b*) Etch depth as a function of misalignment angle and non-zero (1 1 1) etch rate.

trenches using wet anisotropic etching. The upper bound of the allowable misalignment to fabricate the deep trenches is shown in figure 7(*a*). The distance '*b*' is determined by the misalignment angle (θ) with respect to the [1 1 1] direction and the gap between trenches, '*a*'. Then, the distance between the undercut etch front due to the misalignment can be written as

$$b = a/\sin\theta. \tag{3}$$

The etch rate of the undercut etch front (high Miller index planes) depends on the misalignment angle [7, 15]. Let α be the etch rate of (1 1 0) planes and β be the aggregate etch rate of high Miller index planes (*h k l*) for a given KOH concentration and temperature. Then, β can be expressed as $\beta = c \times \alpha$, where c is a proportionality constant that can be found experimentally

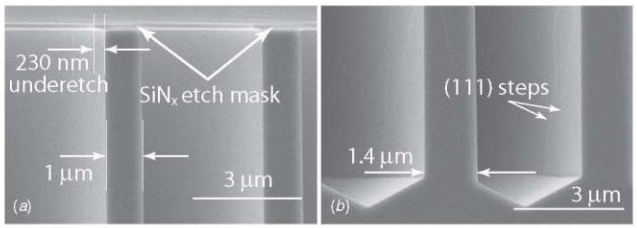

Figure 8. Close-up view of the trenches, figure 4(*d*), for misalignment analysis: (*a*) top of the wall, (*b*) bottom of the wall.

by fitting the measured etch depth. The constant c is measured to be 1.6 in 30% KOH at 80 °C as shown in figure 7(*b*), which is close to previously reported values [27]. Then, the etch depth d can be expressed as

$$d = \frac{t_{hkl} \cdot \alpha}{2}, \tag{4}$$

where $t_{hkl} = b/\beta$ is the etch time of the high Miller index planes.

Figure 7(*b*) shows the maximum trench depth as a function of the misalignment angle. Since the typical etch rate ratios of (1 1 0) and (1 0 0) planes to that of (1 1 1) are greater than 100, the undercut of high Miller index planes between the (1 1 1) plane steps (undercut front) determines the maximum etch depth before the walls etch away (laterally). The measured aspect ratio as a function of the crystal misaligned angle is shown in figure 7(*b*). For an initial spacing of 2 μm between the trench walls ('*a*'), a misalignment angle of the trench wall to the silicon (1 1 1) planes must be less than approximately 150 mdeg to etch trenches of 90 μm deep, representing an aspect ratio of ~100. This represents a point where the contribution of aspect ratio limitation due to misalignment is <10%.

In this work, an SiN_x etch mask was designed to have 2 μm openings for the gratings and was printed using a 5× reduction i-line stepper. From figure 8(*a*), the undercut is approximately 230 nm over a 50 μm trench depth etched into the substrate using 30% KOH at 70 °C. The KOH etch selectivity we obtained between (1 1 0) and (1 1 1) planes at 70 °C was approximately 100, which is close to a previously reported value of approximately 130 [12]. Higher selectivities can be achieved using a 50% KOH solution concentration at 60 °C, resulting in even higher aspect ratios.

Figure 8(*b*) shows the bottom of the fabricated trenches. As indicated in the figure, (1 1 1) steps are visible in the SEM images. The (1 1 1) steps are the result of a non-zero misalignment of the trench patterns to the crystal direction [7]. Although, the step height is difficult to measure, it is expected to be very small (of the order of a few nanometers) because of the small misalignment. The thicknesses of the walls at the top (figure 8(*a*)) and the bottom (figure 8(*b*)) are 1 and 1.4 μm, respectively. The results thus indicate that the undercut is primarily due to the finite etch rate ratio between (1 1 1) and (1 1 0) planes, approximately 100 in our case. This is also illustrated in figure 7, where an alignment to the left of the cross-over point results in microstructures limited only by the finite etch rate ratios of (1 1 1) and (1 1 0) planes in wet anisotropic etchants. As discussed above, a further increase in this ratio can result in higher aspect ratio trench structures, resulting in a misalignment-limited aspect ratio. In such cases, the practical limit of achievable alignment would be limited by the resolution of the rotation stage of the contact mask-aligner. We estimate this limit to be approximately 50 mdeg for most commercially available contact mask-aligners.

6. Conclusions

Single crystal silicon micro/nano structures are fabricated using wet chemical anisotropic etching using an all-optical method to accurately align designed patterns to the substrate's crystal directions. This method has been used to fabricate high aspect ratio trenches for dense integration and single crystal silicon nanowires using a top–down approach. Alignment accuracies better than 0.05° have been achieved using grating alignment marks and an integrated photodetector using conventional optical lithography. We provide a method to estimate the maximum depth of trenches for gratings or arrays on (1 1 0)-oriented silicon substrates. The etched facets of the structures by KOH etch result in atomically smooth (1 1 1) planes, which can be particularly useful in optical and semiconductor PN detector applications. The optical crystal alignment method introduced in this paper can expand the wet chemical anisotropic etching technique for the fabrication of various micro/nano structures.

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