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SOFT SWITCHING FOR IMPROVING THE EFFICIENCY AND POWER DENSITY OF A SINGLE-PHASE CONVERTER WITH POWER FACTOR CORRECTION

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Keywords: zero-voltage switching, power factor correction, variable switching frequency, discontinuous conduction mode, reverse recovery, unwanted turn-on, bidirectional DC-DC converter, bidirectional AC-DC converter, control of switching power converters.

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Abstract

This thesis investigates the possibilities for increasing the power conversion efficiency and power density of a single-phase single-stage AC-DC converter with power factor correction capability. Initially, the limitations are investigated for simultaneous increase of power density and efficiency in hard switched bidirectional converters. The switching frequency dependent turn-on losses of the transistors have been identified as the main limiting factor. In order to avoid the increase in total power losses with increasing the switching frequency, a control approach is proposed for achieving zero voltage switching transitions within the entire operating range of a bidirectional converter that utilizes power transistors in a bridge structure. This approach is based on operation in the discontinuous conduction mode with a variable switching frequency. Operation in the discontinuous conduction mode ensures the necessary reversed current that naturally discharges the parasitic output capacitance of the transistor and thus allows this transistor to be turned on at zero voltage. On the other hand, the varying switching frequency ensures that the converter operates close to the zero voltage switching boundary, which is defined as the minimum required current ripple at which zero voltage switching can be maintained. Operation with the minimum required current ripple is desirable as it generates the lowest magnetic core losses and conduction losses within the power circuit.

The performance and effectiveness of the investigated approach were initially verified in a bidirectional DC-DC converter. A reliable zero voltage switching was confirmed over the entire operating range of a bidirectional DC-DC converter, as well as the absence of the reverse recovery effect and the unwanted turn-on of the synchronous transistor. In order to justify its usage and demonstrate its superior performance, the proposed zero voltage switching technique was compared with a conventional continuous conduction mode operation which is characterized by hard switching commutations. After successful verification and implementation in a bidirectional DC-DC converter, the investigated zero voltage switching approach was adapted for usage in an interleaved DC-AC converter with power factor correction capability. Comprehensive analysis of the converter's operation in discontinuous conduction mode with a variable switching frequency was performed in order to derive its power loss model. The latter facilitated the design process of the converter's power circuit. A systematic approach for selecting the converter's power components has been used while targeting for an extremely high power conversion efficiency over a wide operating range and a low volume design of the converter.

The final result of the investigations performed within the scope of this thesis is the interleaved AC-DC converter with power factor correction capability. Utilization of interleaving allows for increasing the converter's power processing capability, reduces the conducted differential mode noise and shrinks the range within which the switching frequency has to vary. The proposed zero voltage switching control approach was entirely implemented within a digital signal controller and does not require any additional components within the converter's circuit. The experimental results have confirmed highly efficient operation over a wide range of operating powers. A peak efficiency of 98.4 % has been achieved at the output power of 1100 W, while the efficiency is maintained above 97 % over the entire range of output powers between 200 W and 3050 W.

UPORABA TEHNIKE MEHKEGA PREKLAPLJANJA ZA IZBOLJŠANJE UČINKOVTOSTI IN POVEČANJE GOSTOTE MOČI ENOFAZNEGA PRETVORNIKA S KOREKCIJO FAKTORJA MOČI

Ključne besede: preklapljanje pri ničelni napetosti, korekcija faktorja moči, spremenljiva stikalna frekvenca, nezvezni režim delovanja, okrevanje notranje diode, neželen vklop tranzistorja, DC-DC pretvorniki, AC-DC pretvorniki, vodenje močnostnih stikalnih pretvornikov.

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Povzetek

Doktorska disertacija raziskuje možnosti za povečanje izkoristka močnostne pretvorbe in gostote moči enofaznega enostopenjskega mostičnega usmernika s korekcijo faktorja moči. Najprej smo preučili omejitve, ki preprečujejo hkratno povečanje gostote moči in izkoristka dvosmernih trdo-preklapljanih mostičnih pretvornikov. Izgube pri vklopu močnostih tranzistorjev, ki so odvisne tudi od stikalne frekvence, prispevajo največji delež k celotnim izgubam mostičnih pretvornikov in posledično predstavljajo največjo oviro za hkratno povečanje gostote moči in izkoristka. Z namenom preprečitve povečevanja izgub pri močnostni pretvorbi z višanjem stikalne frekvence smo predlagali napreden način vodenja pretvornika, s katerim se doseže mehko preklapljanje tranzistorjev pri ničelni napetosti v celotnem območju delovanja enofaznega mostičnega pretvornika. Predlagani način vodenja temelji na obratovanju v nezveznem režimu delovanja in sprotnem prilagajanju stikalne frekvence. Z ustreznim obratovanjem v nezveznem režimu tako zagotovimo povratni tok, ki je potreben za praznjenje izhodnega parazitnega kondenzatorja močnostnega tranzistorja pred njegovim vklopom. Po izpraznitvi parazitnega izhodnega kondenzatorja je možen vklop tranzistorja pri ničelni napetosti. S časovno in bremensko-odvisnim spreminjanjem stikalne frekvence zagotovimo obratovanje na meji preklapljanja pri ničelni napetosti. Slednja predstavlja stikalno frekvenco, pri kateri dosežemo minimalni potrebni povratni tok, pri katerem je mogoče vzdrževati preklapljanje pri ničelni napetosti. Delovanje z minimalnim povratnim tokom je zaželeno z vidika minimizacije izgub v magnetnih jedrih in prevodnih izgub v močnostnem tokokrogu. Podali smo tudi navodila za načrtovanje takšnega načina vodenja, ki bo zagotovil zanesljivo preklapljanje tranzistorjev v mostični strukturi pri ničelni napetosti znotraj celotnega območja delovanja pretvornika.

Odprava prevladujočih stikalnih izgub z uvedbo mehkega preklapljanja zmanjša vpliv stikalne frekvence na izkoristek močnostne pretvorbe. Z mehkim preklapljanjem tranzistorjev pri ničelni napetosti odpravimo tudi težave z neželenim vklopom tranzistorja in okrevanjem notranje diode. Posledično je dosegljivo obratovanje pri višjih stikalnih frekvencah. Te v kombinaciji z nezveznim režimom delovanja omogočajo zmanjšanje velikosti močnostnih dušilk v vezju pretvornika in posledično povečanje gostote moči.

Delovanje in učinkovitost predlaganega načina vodenja je bilo prvotno preverjeno na dvosmernem DC-DC pretvorniku. Potrjeni so bili tako zanesljivi preklopi pri ničelni napetosti kot tudi odsotnost okrevanja notranje diode tranzistorjev in neželenega vklopa. Izvedli smo tudi primerjavo predlaganega načina vodenja v nezveznem režimu z najpogosteje uporabljanim delovanjem v zveznem režimu. Pri slednjem se preklopi tranzistorjev izvedejo pri polni zaporni napetosti. Rezultati primerjave so pokazali, da z uporabo predlaganega načina vodenja s preklapljanjem pri ničelni napetosti dosežemo višji izkoristek močnostne pretvorbe in ugodnejšo ter bolj enakomerno porazdelitev izgub v pretvorniku. Izrazito manjši je predvsem delež stikalnih izgub, ki dovoljuje uporabo manjših komponent za hlajenje in posledično omogoča povečanje gostote moči pretvornika. Izpostaviti je treba tudi dejstvo, da je za delovanje v nezveznem režimu zahtevana manjša induktivnost močnostne dušilke. Takšno induktivnost lahko dosežemo z uporabo manjšega magnetnega jedra, kar nudi možnost za dodatno zmanjšanje dimenzij pretvornika.

Po uspešnem testiranju na dvosmernem DC-DC pretvorniku smo predlagali še način vodenja v nezveznem režimu s konstantno amplitudo povratnega toka in spremenljivo stikalno frekvenco, prilagojen za uporabo v AC-DC pretvorniku s korekcijo faktorja moči. Predlagani način vodenja ne zahteva nikakršnih posegov v osnovno vezje pretvornika in ga je mogoče v celoti implementirati v digitalni signalni krmilnik. V doktorski disertaciji je podrobno predstavljeno načrtovanje obravnavanega močnostnega stikalnega pretvornika, ki je bil tudi izdelan in eksperimentalno preizkušen. Proces načrtovanja je bil usmerjen v doseganje čim višjega izkoristka močnostne pretvorbe s pretvornikom čim manjših dimenzij. Eksperimentalni rezultati potrjujejo izredno visoko učinkovitost delovanja, saj znaša maksimalni izkoristek močnostne pretvorbe 98.4 %. Slednji je dosežen pri izhodni moči 1100 W. Ob visokem maksimalnem izkoristku pa pretvornik odlikuje tudi visok izkoristek v širšem območju delovanja, ki presega 97 % v celotnem območju izhodnih moči med 200 W in 3050 W.

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
AMN	Artificial Mains Network
AWG	American Wire Gauge
CCM	Continuous Conduction Mode
CCM-HSW	Continuous Conduction Mode with Hard Switching
CISPR	International Special Committee on Radio Interference (*French*, Comité International Spécial des Perturbations Radioélectriques)
CM	Common Mode
CPLD	Complex Programmable Logic Device
CRM	Critical Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCM-ZVS	Discontinuous Conduction Mode with Zero Voltage Switching
DM	Differential Mode
DSC	Digital Signal Controller
DUT	Digital Signal Controller
EMC	Electromagnetic Compliance
EMI	Electromagnetic Interference
FPGA	Field-Programmable Gate Array
HF	High Frequency
HSW	Hard Switching
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
LF	Low Frequency
LISN	Line Impedance Stabilizer Network
LPF	Low-Pass Filter
MPP	Mollypermaloy
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
N	Neutral Line
P	Positive Line
PCB	Printed Circuit Board

PE	Protective Earth
PF	Power Factor
PFC	Power Factor Correction
PI	Proportional-Integral
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transitions

List of Symbols

A_{c}	Cross sectional area of a magnetic core
A_{L}	Specific inductance
A_{w}	Cross sectional area of bare wire
$\mathrm{Att}_{\mathrm{req}}$	Required attenuation of the EMI filter
B	Magnetic flux density (general)
B_{max}	Maximum magnetic flux density
B_{min}	Minimum magnetic flux density
B_{pk}	Peak magnetic flux density
C_{A}	High voltage side capacitance in a bidirectional DC-DC converter
C_{B}	Low voltage side capacitance in a bidirectional DC-DC converter
C_{dc}	DC-side capacitance
C_{ds}	Drain-to-source capacitance of a MOSFET
C_{eq}	Equivalent capacitance (ratio of Q_{tot} to V_{A})
C_{gd}	Gate-to-drain capacitance of a MOSFET
C_{gs}	Gate-to-source capacitance of a MOSFET
C_{lisn1}	Grid-side LISN capacitance
C_{lisn2}	Converter-side LISN capacitance
C_{oss}	Parasitic output capacitance of a MOSFET ($C_{\mathrm{gd}} + C_{\mathrm{ds}}$)
d_{ID}	Inner diameter of a toroidal magnetic core
d_{w}	Bare wire diameter
d_{wo2}	Outer diameter of a wire with Grade 2 insulation
D	Duty cycle (general)
D_{boost}	Duty cycle in boost operating mode
D_{buck}	Duty cycle in buck operating mode
E_{on}	Turn on energy of a MOSFET
E_{off}	Turn off energy of a MOSFET
E_{sw}	Switching energy of a MOSFET (general)
f_{d}	EMI filter design frequency
f_{L}	Frequency of AC voltage (line frequency)
f_{sw}	Switching frequency
$f_{\mathrm{sw,max}}$	Maximum switching frequency
$f_{\mathrm{sw,min}}$	Absolute minimum switching frequency

$f_{\mathrm{sw,min1}}$	Local minimum switching frequency
H	Magnetic field intensity (general)
H_{max}	Maximum magnetic field intensity
i	Instantaneous current (general)
i_{ac}	Instantaneous value of AC current (current drawn from the utility grid)
i_{CM}	Common mode current
i_{DM}	Differential mode current
i_{dr}	Instantaneous current through the gate driver
i_{ds}	Instantaneous drain-to-source current in a MOSFET (general)
i_{dsH}	Instantaneous current across the high-side MOSFET in a half-bridge
i_{dsL}	Instantaneous current through the low-side MOSFET in a half-bridge
i_{gd}	Instantaneous current through the capacitance C_{gd}
i_{gs}	Instantaneous current through the capacitance C_{gs}
i_{in}	Input current of the interleaved AC-DC converter on the converter side of input filter
i_{L}	Instantaneous current through the power inductor
i_{LX}	Instantaneous current through the one power inductor in an interleaved converter (X = 1,2,3)
$i_{\mathrm{L,avg}}$	Instantaneous value of average inductor current
I_{A}	High voltage side current in a bidirectional DC-DC converter
$I_{\mathrm{AC,nom}}$	Nominal AC current
I_{B}	Low voltage side current in a bidirectional DC-DC converter
$I_{\mathrm{DC,nom}}$	Nominal DC current
$I_{\mathrm{ds,rms}}$	Rms value of drain-to-source current in a MOSFET (general)
$I_{\mathrm{L,avg}}$	Average value inductor current
$I_{\mathrm{L,rms}}$	Rms value of inductor current (general)
I_{R}	Reversed current magnitude
$I_{\mathrm{R,min}}$	Minimum required magnitude of the reversed current for achieving ZVTs
I_{rrp}	Peak value of the reverse recovery current
$\hat{I}_{\mathrm{L}}$	Magnitude of the instantaneous inductor current
$\hat{I}_{\mathrm{L,avg}}$	Magnitude of average inductor current
l_{c}	Magnetic path length
L	Inductance of the power inductor

L_{ccm}	Required inductance for ensuring operation in CCM
L_{i}	No load inductance
L_{lisn}	LISN inductance
L_{min}	Minimum required inductance for achieving ZVTs
L_{req}	Required inductance of a power inductor
L_{X}	Inductance of a power inductor in an interleaved converter (X = 1,2,3)
n	Number of interleaved converter cells
N	Number of turns
P	Real power (general)
P_{cond}	Average conduction losses (general)
$P_{\mathrm{cond,X}}$	Average conduction losses in X
P_{core}	Magnetic core losses
P_{mag}	Average magnetic core losses
P_{nom}	Nominal power (general)
P_{o}	Average output power (general)
$P_{\mathrm{sw,X}}$	Average switching losses in X
P_{tot}	Total power losses
P_{wind}	Average inductor winding losses
Q	Electric charge (general)
Q_{rr}	Reverse recovery charge
Q_{tot}	Total electric charge required for achieving a ZVT
R_{dr}	Internal resistance of the gate driver
$R_{\mathrm{ds,on}}$	On-state resistance of a MOSFET
$R_{\mathrm{ds,onX}}$	On-state resistance of a MOSFET belonging to X
R_{gint}	Internal gate resistance of a MOSFET
R_{Goff}	Sink resistance of an asymmetric gate driving circuit
R_{Gon}	Source resistance of an asymmetric gate driving circuit
R_{L}	Winding resistance of an inductor (general)
R_{Lac}	AC resistance of an inductor’s winding
R_{Ldc}	DC resistance of an inductor’s winding
R_{load}	Load resistance
R_{lisn}	LISN resistance
S	Apparent power (general)

t_0	Time instant in which a resonant transition begins
t_{max}	Time instant in which the switching frequency reaches its maximum value
$t_{\mathrm{min,1}}$	Time instant in which the switching frequency reaches its local minimum
t_{res}	Time instant in which a resonant transition finishes
t_{zc}	Time instant at which the inductor current changes direction after a resonant transition
T	Duration of the mains (utility grid voltage) period
T_{bd}	Duration of the interval within which the inductor current is passed through the body diode after a resonant transition
T_{DT}	Dead time duration
$T_{\mathrm{DT,max}}$	Maximum allowed dead time duration
$T_{\mathrm{DT,min}}$	Minimum required dead time duration
$T_{\mathrm{off,delay}}$	Turn-off delay of a MOSFET
$T_{\mathrm{on,delay}}$	Turn-on delay of a MOSFET
T_{res}	Duration of a resonant switching transition
$T_{\mathrm{res,max}}$	Maximum allowed duration of the main transition period
T_{rhp}	Duration of a resonant half-period ($= \frac{\pi}{\omega_{\mathrm{o}}}$)
T_{sw}	Duration of a switching period ($T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$)
T_{zc}	Duration of the interval between t_{res} and t_{zc}
v	Instantaneous voltage (general)
v_{ac}	Instantaneous value of AC voltage (utility grid voltage when connected to the grid)
v_{CM}	Common mode voltage
v_{DM}	Differential mode voltage
v_{dc}	Instantaneous value of DC voltage
v_{ds}	Instantaneous drain-to-source voltage of a MOSFET (general)
v_{dsH}	Instantaneous voltage across the high-side MOSFET in a half-bridge
v_{dsL}	Instantaneous voltage across the low-side MOSFET in a half-bridge
v_{in}	Input voltage of the interleaved AC-DC converter on the converter side of input filter
v_{L}	Instantaneous voltage across the power inductor
V_{A}	High voltage side voltage in a bidirectional DC-DC converter
$V_{\mathrm{AC,nom}}$	Nominal AC voltage

V_{B}	Low voltage side voltage in a bidirectional DC-DC converter
V_{box}	Boxed volume (volume of a rectangular prism)
V_{dc}	Average DC-side voltage
$V_{\mathrm{DC,nom}}$	Nominal DC voltage
$V_{\mathrm{DMqp,est}}$	Estimated quasi-peak differential mode voltage
V_{dr}	Gate driver on-state output voltage
V_{DSS}	Breakdown voltage of a MOSFET
V_{L}	Volume of an inductor
V_{th}	Threshold voltage of a MOSFET
$\hat{V}_{\mathrm{ac}}$	Magnitude of AC voltage
ΔB	AC flux swing
Δi_{L}	Inductor current ripple
ΔI_{Lpp}	Peak-to-peak inductor current ripple
$\Delta I_{\mathrm{Lpp,max}}$	Maximum peak-to-peak inductor current ripple
Δv_{DC}	DC voltage ripple
η	Efficiency
$\eta_{\mathrm{AC,nom}}$	Efficiency in nominal operating point
μ_0	Permeability of free space
μ_{i}	Initial relative permeability (no DC bias)
μ_{min}	Minimum relative permeability (maximum DC bias)
μ_{r}	Relative permeability
φ	Phase displacement angle
ω	Angular frequency of AC voltage
ω_{o}	Resonant angular frequency

CHAPTER 1

INTRODUCTION

1.1 Motivation

Rapid growth in the number of power electronics interfaces connected to the electric utility grid has raised concerns over the harmonic "pollution" of the utility grid voltage. These concerns originated from the fact that power electronics utility grid interfaces draw a distorted or even pulsating current from the grid. The presence of higher harmonic components in the current drawn from the grid increases the losses in the transmission and distribution system without providing any additional real power to the load [2–7]. Since grid current harmonic elimination and power factor correction are neither economical for producers nor required by the load, compulsory standards (e.g. IEC 61000-3-2 [1], IEEE 519 [8]) have been developed that specify the maximum allowed harmonic distortion of the current drawn from the grid. Consequently, numerous harmonic reduction and power factor correction (PFC) circuits and control strategies have emerged. By widening the applicability of these standards over recent years, PFC capability has become a standard feature for all grid-connected rectifiers.

Single-phase PFC circuits utilize either passive or active PFC approaches. The passive approach is based on introducing a filter that passes only the current at the line frequency. Since such a filter has to be designed to have a very low cutoff frequency, usage of bulky inductors and capacitors is inevitable [9–16]. Due to the passive PFC circuit's limited PFC capability and the unwanted contribution to the size of the whole system, active PFC approaches are predominant in modern power electronics. The latter can achieve high quality line current waveform, unity power factor, and efficiencies of nearly 100 % in a significantly smaller case size than their passive counterparts

[17–21]. Nowadays active PFC circuits are employed in nearly all grid-connected rectifiers, ranging from various mobile and portable to stationary applications.

Active PFC circuits can be divided into two-stage [22–33] and single-stage topologies [19, 20, 34–49]. While single-stage topologies generally achieve higher efficiencies and power densities, two-stage topologies provide better dynamic response of the output and a line current waveform of higher quality. On the basis of the supported power flow directions, active PFC circuits are further divided into unidirectional and bidirectional. Since the majority of applications only require unidirectional power flow, from the utility grid to the load, PFC rectifiers utilizing unidirectional switching power converters have dominated the market until recently. With the development of new applications and technologies like vehicle-to-grid systems [50–53] and smart residential nanogrids [54], the need for bidirectional utility grid interfaces has evolved. Since neither the conventional diode bridge-based topologies nor the more recently introduced bridgeless topologies commonly used in PFC circuits can provide bidirectional power flow, utilization of the H-bridge topology has become a common choice in single-stage [19, 48] as well as in two-stage [27–33] PFC circuits. In addition to providing bidirectional power flow capability, the main advantage of using an H-bridge, also known as the full-bridge topology, is in low conduction losses and consequently high power processing capability at low to moderate switching frequencies. On the other hand, usage of an H-bridge converter also introduces several unwanted phenomena, which are common to all the converter structures utilizing two power transistors in one converter leg. Major concerns are the reverse recovery effect of the transistors' antiparallel body diodes and unwanted turn on of the transistor, the body diode of which has conducted the freewheeling current before its complementary transistor was turned on. Both phenomena cause additional losses, electromagnetic interference, and in the worst case even breakdowns the transistors. The effects of both the reverse recovery and the unwanted turn-on become more severe with higher voltage and current levels, faster switching transitions, and higher switching frequencies.

Due to the growing demand for electrical power, limited natural resources for its generation, limited capacities for its distribution, and the pollution caused when generating it from fossil fuels, there is a strong tendency towards developing highly efficient electrical equipment and devices. Usage of those highly efficient systems can limit the increasing global power demand and thus contribute to environmental sustainability. The converter's efficiency mainly depends on semiconductor losses, gate drive losses, losses in passive power components, losses in power conductors, and losses in various protection circuits, in cases where they are present. On the other hand, there is a strong tendency towards minimization and weight reduction of the power electronics interfaces, especially those designed for portable and mobile applications. An important factor on the way to achieving both high power density and high efficiency is the selection of the most suitable topology for each application. Other, no less important factors, are related to the input and output power quality requirements and the switching frequency, which determine the required sizes of the passive components within the power circuit. In addition to a proper printed circuit board layout and converter structure, passive components often represent the main objects for minimization in order to achieve higher power density [55]. A well-known and widely used way to decrease the sizes of passive components and thus increase the power density without affecting the quality of the input and output voltage and current waveforms is by increasing the switching frequency. On the other hand, operation at higher switching frequencies increases the switching losses and results in lower power conversion efficiency. From a different perspective, it is relatively easy to achieve close to 100% efficiency, when there are no size, weight, and switching frequency limitations [21, 56]. It is also not difficult to achieve high power density if high efficiency is not required. However, it is a real challenge to simultaneously achieve extremely high efficiency and power density [18, 20].

Let us consider a highly efficient PFC rectifier with a close to optimal circuit layout and an average power density, operating in hard switching mode at a moderate switching frequency of several tens of kHz. As mentioned above, it is possible to reduce the size and weight of such a converter by operating at higher switching frequencies, at which the same input and output voltage and current waveform quality can be achieved with smaller passive components [55]. The negative effect of such modification is a resulting drop in efficiency. The most significantly affected are the switching losses, which increase considerably at higher switching frequencies. As a consequence of the increased semiconductor's temperature, the conduction losses increase as well. In addition to semiconductor losses, a higher number of switching events over a mains period also induces higher losses in magnetic cores. The latter may represent a considerable share in total losses. The described example clearly demonstrates the complexity of simultaneously achieving high efficiency and high power density. It also indicates that there is a trade-off between maximum achievable efficiency and maximum achievable power density [18]. This leads to one of the main design problems in modern power electronics, which is in finding the switching frequency at which the target efficiency and target power density can be achieved.

In the above presented example of increasing the power density, it was stated that the switching losses increase significantly when the converter is operating at higher switching frequencies in hard-switching regime. In order to overcome this drawback, soft-switching approaches are widely applied to all kinds of switching power converters. The utilization of soft-switching alleviates the switching losses and significantly decreases the rate of power conversion efficiency deterioration with increasing switching frequency. In the cases where metal–oxide–semiconductor field-effect transistors (MOSFETs) are used as power transistors, the preferred soft-switching strategy is zero-voltage switching (ZVS), while in the case of utilizing insulated-gate bipolar transistors (IGBTs), zero-current switching (ZCS) is the best choice [57]. The latter will not be given special attention within this thesis since MOSFETs will be used as power transistors. The idea behind ZVS is to discharge the MOSFET's output capacitance, so that it can be turned on at zero drain-to-source voltage. Thus, the switching losses become negligible and the semiconductor losses almost insensitive to variation of the switching frequency. The way of discharging the MOSFET's output capacitances differs from one circuit topology to another but in most cases introduces unwanted effects, like higher current distortion, higher filtering requirements, higher magnetic core losses, additional components in the circuit or the need for operating with variable switching frequency.

Several approaches for achieving ZVS in unidirectional PFC rectifiers have been proposed in the literature. The majority of them are based on adding different kinds of auxiliary circuits to the main power circuit of the converter in order to discharge the output capacitor of the transistor before it is turned on [35, 39, 45, 58]. A different approach was used in [43], where ZVS was achieved in a bridgeless unidirectional PFC rectifier by using slow recovery diodes which allowed for a current reversal and a consequent discharge of the MOSFETs' parasitic capacitances. The only ZVS approach implemented in a bidirectional H-bridge PFC rectifier was proposed in [19]. The approach is based on operation on and beyond the border of critical conduction mode (CRM), which achieves ZVS within the entire operating range of converter. Similar approaches, based on operation in the discontinuous conduction mode (DCM) were proposed for bidirectional half-bridge based DC-DC converters [59–61]. The switching behavior of such DC-DC converters is analogous to the behavior of one H-bridge converter's leg. Although all the reported converters utilizing DCM-based ZVS have demonstrated highly efficient operation, it is still rather unclear how to obtain proper control parameters that will ensure reliable ZVS operation over the entire operating range of the converter. The reversed current and dead times crucially influence the switching transitions and consequently the ZVS capability. When not selected properly, ZVS may be lost in parts of the converter's operating range. This occurrence leads to a drop in power conversion efficiency and several other hard-switching related issues like body diode reverse recovery, unwanted turn-on of a transistor, or even malfunctioning of the converter.

1.2 Objectives and contributions

The objective of this thesis is to investigate the possibilities for improving the efficiency and power density of a bidirectional single-stage AC-DC converter with PFC capability. The main challenge is to reduce the operating switching frequency dependent losses, which represent the major limiting factor for reducing the size and weight of passive components in the circuit. Another objective is to achieve high quality of the input current waveform and a rather good dynamic response of the output voltage in a single-stage PFC structure.

The new contributions of this work are:

- analytical model for determining the duration of resonant switching transitions on the basis of information provided in the datasheet of power MOSFETs;
- ZVS control design guideline for achieving reliable resonant switching transitions within the entire operating range of a bidirectional DC-DC as well as AC-DC converter;
- a guideline for designing a highly efficient and small-sized single-stage PFC rectifier with a high quality input current waveform and a decent dynamic response of the output voltage;
- a fair power conversion efficiency and power loss breakdown comparison between a hard-switched and a zero-voltage switched half-bridge based bidirectional DC-DC converter;
- effective implementation of a DCM-based ZVS approach within a digital signal controller (DSC), without any modifications or additional components in the circuit of a bidirectional DC-DC converter and AC-DC converter with PFC capability;
- power loss models and estimation algorithms for a non-isolated bidirectional DC-DC and AC-DC converter operating in DCM with a variable switching frequency,
- differential mode noise estimation and identification of the worse case conducted differential mode noise in a DCM operated AC-DC converter with variable switching frequency.

1.3 Research Hypotheses

The validity of the following hypotheses has been examined within this thesis:

H1) Utilization of a soft switching technique results in a reduction of total power losses and alleviates their dependence on the switching frequency.

H2) DCM-based ZVS prevents unwanted turn-ons of transistors and their body diodes' reverse recovery induced issues.

H3) ZVS can be achieved within the entire operating range of a bidirectional converter by operating it in DCM with a reversed current of sufficient magnitude and properly selected timing parameters.

H4) The required magnitude of the reversed current and timing parameters for maintaining ZVS over the entire operating range of a bidirectional converter can be determined solely on the basis of the information provided in the datasheet of the components within the circuit.

1.4 Thesis outline

With the aim of improving the efficiency and power density of a single-phase single-stage H-bridge PFC rectifier several issues will be addressed within the scope of this thesis.

Chapter 1 begins by explaining the motivation for the investigations carried out within this thesis. The reasons for utilization of H-bridge topology in PFC rectifiers are provided, along with its main drawbacks. As the main issue, a trade-off between the efficiency and power density of switching power converters is pointed out.

Chapter 2 provides an overview of power factor correction circuits and introduces those compulsory standards which define the maximum allowed distortion of the current drawn from the utility grid. The basic structure and the operating principle of the investigated AC-DC converter with PFC capability are also presented in this chapter.

Chapter 3 investigates the main unwanted phenomena occurring in hard-switched bridge structures and provides some simple solutions for avoiding them. The semiconductor losses and their estimation are also discussed in this chapter. The chapter concludes with a demonstration of the operating switching frequency's influence on the semiconductor power losses and the size of the power inductor in a hard switched converter operating in continuous conduction mode (CCM) with a constant switching frequency.

Chapter 4 explains the DCM-based ZVS principle and provides a detailed analysis of the resonant switching transitions in a half-bridge structure. Experimental verification of the proposed ZVS approach and performance comparison with a conventional hard-switched operation in CCM are provided for the case of a bidirectional DC-DC converter. Guidelines for designing and implementing a reliable ZVS control for bidirectional DC-DC and bidirectional AC-DC converters are also provided in this chapter.

Chapter 5 presents an analytical approach to designing the power stage of the investigated AC-DC converter with the aim of achieving high power conversion efficiency in a small volume design.

Chapter 6 focuses on the AC-DC converter's control design. Initially, a cascaded control scheme is derived for single cell operation of the converter within the positive half-period of AC voltage. This is later adapted for usage over the entire range of AC voltages in an interleaved AC-DC converter operated in DCM with a variable frequency. The chapter concludes with verification of the proposed control scheme by simulation.

Chapter 7 provides experimental verification of the interleaved AC-DC converter utilizing the proposed control scheme. Power conversion efficiency is evaluated over the entire operating range of the converter.

Chapter 8 summarizes this thesis and draws some conclusions on the basis of the presented investigations and results. Finally, some outlooks and suggestions are provided for future research.

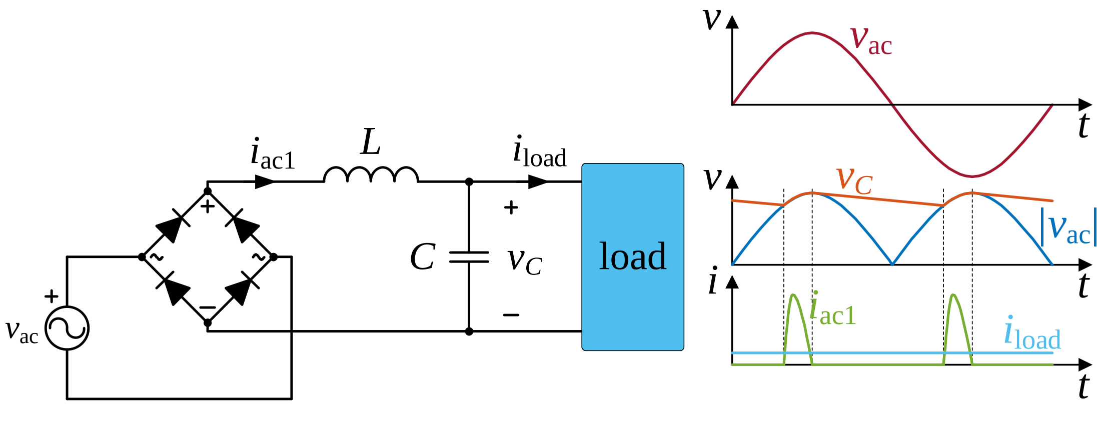
CHAPTER 2

POWER FACTOR CORRECTION

2.1 Power Factor Correction and Line Current Distortion

The main objective of power electronics interfaces is to facilitate electric energy flow between two systems. If one of these systems is the utility grid and the other system operates on a rather constant DC voltage, the power electronics interface has to provide conversion between the alternating grid voltage and the constant voltage of the other system. In the case where the power is drawn from the utility grid, AC-DC converters, also known as rectifiers, are employed. Figure 2.1(a) shows a simple and once widely used uncontrolled line-commuted rectifier. It consists of a diode bridge which provides full-wave rectification and a large filter capacitor which ensures a rather constant voltage at the output terminals of the rectifier while supplying the load. The main drawback of this structure is that it only draws current from the grid when the rectified grid voltage exceeds the voltage across the capacitor, as evident from the voltage and current waveforms in Fig. 2.1(b). Since the power is drawn from the source only during a very small part of the grid voltage period, the magnitude of these current pulses is 5 to 10 times higher than in the case of drawing the current continuously from the grid [4]. As a result, the rms current drawn from the utility grid is higher and thus generates additional losses within the transmission and distribution system, although no additional real power is supplied by the system [62]. The distorted line current also affects the shape of the grid voltage.

In order to use the generated electric power more efficiently and reduce the harmonic pollution of the utility grid, rectifiers with power factor correction capability have replaced uncontrolled line-commuted rectifiers over the past couple of decades. Although their production costs are higher



(a) (b)

Figure 2.1: Schematic diagram of a line-commuted diode rectifier (a) and the corresponding voltage and current waveforms (b).

than the ones of line-commuted rectifiers, power factor correctors are widely employed since they represent a cheaper and more environmentally friendly alternative to increasing the electric power generation, transmission, and distribution capacities. With all the loads in the system drawing a non-distorted sinusoidally shaped current from the grid, which is in phase with the grid voltage, the existing power generation, transmission, and distribution systems can supply more real power than ever before.

In general, the power factor PF is defined as the ratio between the real power P and apparent power S as

$$PF = \frac{P}{S}, \tag{2.1}$$

and indicates how effectively the power is used by the load [9]. For purely sinusoidal voltage and current, PF can be written as

$$PF = \cos\varphi, \tag{2.2}$$

where φ is the phase displacement between the grid voltage and the current drawn from the grid. Under the assumption of negligible grid voltage harmonics, such a power factor (PF) definition applies exclusively to non-switching linear loads. Since the majority of linear loads like transformers, electric motors, and generators also generate harmonics, the expression (2.2) becomes useless. In addition, the phase displacement representation of PF is also insufficient for power electronic devices, the non-linear behavior of which considerably affects the shape of the current drawn from the grid [3]. A more realistic and widely applicable expression for determining the PF is based on the assumption that a distorted current is drawn from the grid with a purely sinusoidal voltage. Under such conditions the PF is written as

$$PF = \frac{V_{\mathrm{rms}} I_{1,\mathrm{rms}} \cos\varphi}{V_{\mathrm{rms}} I_{\mathrm{rms}}} = \frac{I_{1,\mathrm{rms}}}{I_{\mathrm{rms}}} \cos\varphi = K_{\mathrm{dist}} K_{\mathrm{disp}}, \tag{2.3}$$

where V_{rms} and I_{rms} are the rms values of line voltage and line current, respectively, and $I_{1,\mathrm{rms}}$ the rms value of the fundamental component of the line current. As already explained with (2.2), $\cos\varphi$ represents the displacement factor K_{disp}. On the other hand, the ratio between $I_{1,\mathrm{rms}}$ and I_{rms} represents the distortion factor K_{dist}, which can be used for deriving another parameter for evaluating distortion of the line current, namely total harmonic distortion (THD). Originating from K_{dist}, THD is defined as [2]

$$THD = \sqrt{\frac{1}{K_{\mathrm{dist}}^2} - 1}. \tag{2.4}$$

2.2 Standardization

In order to reduce the presence of harmonics in the utility grid, several standards have been developed and accepted nationally and internationally [1, 8]. Most of the existing standards define only the current harmonic limits, while they do not specify a minimum allowed value of power factor explicitly. IEC 61000-3-2 [1] provides internationally accepted guidelines for limiting the injection of harmonic currents into the utility grid. It applies for all the devices connected to the public distribution network with an input current equal or less than 16 A per phase. The devices are divided into four classes, with current harmonic limits specified for each class, as shown in Table 2.1.

2.3 Overview of conventional PFC rectifiers

On the basis of the type of connection to the public distribution network, PFC circuits can be classified into single-phase [9, 10, 17] and three-phase interfaces [63, 64]. The latter will not be given special attention as this thesis focuses exclusively on single-phase converters. In accordance with the review reported in [10], PFC structures can be divided into the following major groups:

- passive PFC circuits,
- active two-stage PFC circuits,
- and active single-stage PFC circuits.

Figure 2.2 illustrates such classification with block schemes of structures corresponding to each group.

Table 2.1: Current harmonic limits specified by IEC 61000-3-2 [1].

Harmonics [n]	**Class A** [A]	**Class B** [A]	**Class C** [% of fund.]	**Class D** [mA/W]
Odd harmonics				
3	2.3	3.45	$30 \times \lambda$	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.6	5	0.5
11	0.33	0.495	3	0.35
13	0.21	0.315	3	3.85/13
$15 \leq \mathrm{n} \leq 39$	$0.15 \times 15/\mathrm{n}$	$0.225 \times 15/\mathrm{n}$	3	$3.85/\mathrm{n}$
Even harmonics				
2	1.08	1.62	2	–
4	0.43	0.645	–	–
6	0.30	0.45	–	–
$8 \leq \mathrm{n} \leq 40$	$0.23 \times 8/\mathrm{n}$	$0.345 \times 8/\mathrm{n}$	–	–

The simplest, cheapest, and also very reliable are passive PFC circuits. They consist of a diode bridge and a passive filter, which is built of different combinations of inductors and capacitors [11]. Due to their high power processing capabilities, passive PFC circuits are commonly used in high power applications [2]. They are also often utilized in low power applications, mainly due to their low production costs [12,13]. Another reason for successful utilization in low power applications is that IEC 61000-3-2 specifies the harmonic limits for class A and B equipment in absolute values and therefore it is not difficult to maintain harmonics within the allowed limits at low operating powers [13,14]. Although several studies [13–16] have proven that it is possible to achieve compliance with different current harmonic standards by using passive PFC circuits, the latter exhibit the following drawbacks:

- Maximum achievable power factor is always below 0.9;
- The current drawn from the grid is highly distorted;
- They are heavy and bulky, mainly due to the large filter inductor;
- Their dynamic response is poor;
- The output is unregulated.

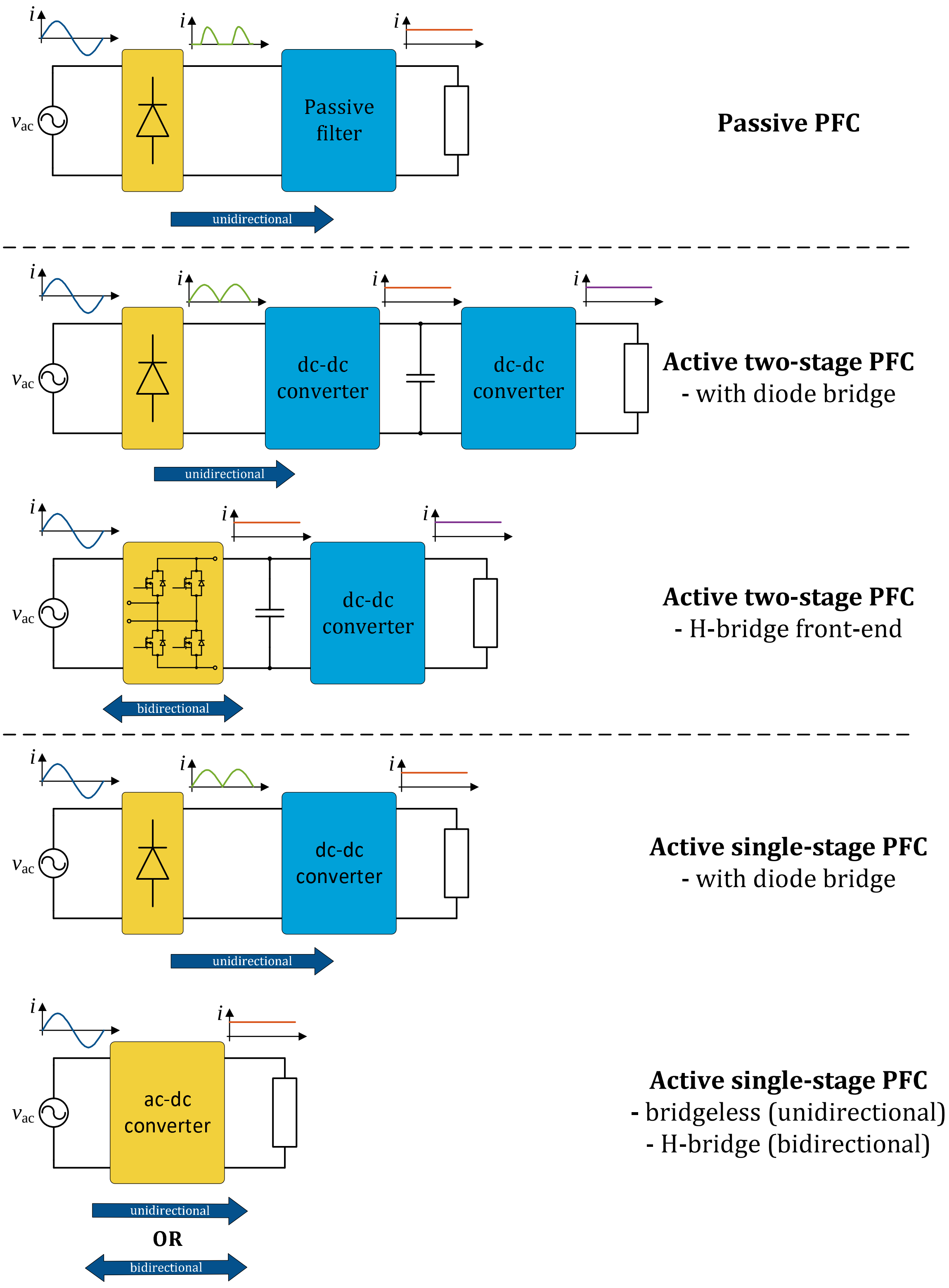

i
i
i
v_{ac}
Passive filter
unidirectional
Passive PFC
i
i
i
i
v_{ac}
dc-dc converter
dc-dc converter
unidirectional
Active two-stage PFC
- with diode bridge
i
i
i
v_{ac}
dc-dc converter
bidirectional
Active two-stage PFC
- H-bridge front-end
i
i
i
v_{ac}
dc-dc converter
unidirectional
Active single-stage PFC
- with diode bridge
i
i
v_{ac}
ac-dc converter
unidirectional
OR
bidirectional
Active single-stage PFC
- bridgeless (unidirectional)
- H-bridge (bidirectional)

Figure 2.2: General classification of PFC structures.

Despite the fact that passive PFC circuits appear to be a good choice for cost sensitive and several other above listed applications, active PFC techniques are the preferred option in modern applications due to their superior performance [22]. Among active PFC techniques, the two-stage active PFC scheme is the most common as it exhibits numerous advantageous features [17, 22]. A conventional two-stage active PFC converter consists of a diode bridge, two DC-DC converters and a DC-link capacitor which decouples both conversion stages. The diode bridge and the adjacent DC-DC converter force the current to follow the grid voltage. This same DC-DC converter also provides a low-bandwidth control of the voltage on the decoupling capacitor. For achieving a good dynamic response of the PFC unit's output stage and adapting the output voltage and current to the requirements of the load, a second DC-DC converter is employed [23, 24]. In the second stage, isolated DC-DC converters are commonly used for providing galvanic isolation between the utility grid and the converter's output [17, 25, 26]. As a complete opposite of passive PFC circuits, the just described two-stage PFC scheme achieves a very high quality line current waveform, operation with a close to unity PF, and well controlled output with a good dynamic response. In several emerging applications like smart residential nanogrids [54] and vehicle-to-grid systems [51–53], bidirectional power flow is required. For supporting that, the diode bridge and the commonly used unidirectional DC-DC converter in the first stage are replaced by an H-bridge structure, comprising four power transistors, as shown in Fig. 2.2. Several such bidirectional two-stage PFC schemes with non-isolated and isolated output stages have been reported in the literature [27–33].

In the third group of PFC structures depicted in Fig. 2.2, there are converters that utilize single-stage PFC technique. They represent a cheaper alternative to two-stage PFC converters that can achieve potentially high efficiencies at moderate output powers due to a lower number of power components within the circuit [10]. However, the increase in power density due to elimination of one conversion stage is not guaranteed since a larger output capacitor is required in single-stage structures [22]. A conventional unidirectional single-stage PFC structure consists of a diode bridge and a DC-DC converter, which performs the role of a power factor corrector [34–39]. Since both, the control of the line current and the output, have to be performed within one conversion stage, single-stage PFC converters generally provide lower attenuation of the line current harmonics than their two-stage counterparts. With the aim of improving the efficiency of PFC rectifiers, several different bridgeless PFC topologies were proposed and investigated in [40–47]. Bridgeless refers to the absence of the diode bridge, in which the biggest share of losses is generated in conventional PFC structures operating at the power of several kilowatts [41, 42]. Elimination of the diode bridge from the circuit reduces the number of devices in the conduction path and thus results in considerably lower conduction losses, especially at higher power levels. The studies in which bridgeless PFC rectifiers were compared with conventional single-stage PFC rectifiers have demonstrated higher power conversion efficiencies of bridgeless structures at the power level of several hundred watts [40] as well as at several kilowatts [41,46]. With optimization of the power components within the circuit of bridgeless PFC rectifiers, extreme efficiencies above 99% at very high power densities were reported in [18, 20]. However, all the mentioned conventional and bridgeless single-stage PFC structures only support unidirectional energy flow, which makes them useless in applications where the power has to be sent back into the utility grid. The same as for achieving bidirectional operation in two-stage PFC structures [27–33], an H-bridge converter can be employed in a single stage structure for performing the tasks of rectification and PFC [19,48,49].

2.4 Single-phase H-bridge PFC rectifier

Single phase H-bridge topology, also known as the full-bridge structure, represents one of the fundamental converter topologies in power electronics. It can support bidirectional power flow between an alternating and a constant power source. In terms of power conversion capabilities, it provides a voltage step-down feature for transferring power from a constant power source to an alternating power source (inverter or buck operating mode) and a voltage step-up feature for transferring power in the opposite direction (rectifier or boost operating mode). For this reason H-bridge topology is widely used in different kinds of inverter applications, ranging from motor drives [65–67] to distributed power generation systems [68, 69]. With the development of technologies like regenerative braking in electric vehicles [70], vehicle to grid systems [50–53], and smart residential nanogrids [54] which require bidirectional power flow between the utility grid and DC power sources, the applicability of the H-bridge structure has been extended to providing PFC functionality. In addition to supporting bidirectional operation, lower conduction losses can be achieved by using an H-bridge structure as a single-stage PFC rectifier or as a front-end converter in two-stage PFC structures. In both cases there are only two semiconductor components in the PFC stage conduction path, of which both are power transistors. The latter have better conductive properties than the power diodes in conduction paths of unidirectional bridgeless PFC structures and PFC structures that utilize diode bridges for rectification. Nonetheless, usage of the full-bridge structure also introduces several unwanted phenomena. These are common to all the hard-switched bridge structures which comprise power transistors with floating source potentials, the simplest examples of which are conventional synchronous or bidirectional DC-DC converters [59,61,71–74]. A major concern in such bridge structures is the reverse recovery effect of the synchronous transistor's (syncFET)[1] antiparallel body diode at the instant of turning on the main transistor (mainFET). For the duration of the reverse recovery phenomena, both transistors are exposed to high current change rates and high peak reverse recovery currents which significantly increase switching losses, cause electromagnetic interference, and lead to dangerous operating conditions [71,72,75]. Another drawback of hard-switched active bridge structures is the unwanted Cdv/dt-induced turn-on of the synchronous transistor (syncFET) immediately after its body diode recovers [73, 74]. This phenomenon causes additional switching losses and in the worst case even a destructive shoot-through condition. The effects of both the reverse recovery and the spurious turn-on become more severe with higher voltage and current levels, faster switching transitions, and higher switching frequencies.

For improving the performance of the H-bridge PFC rectifier in terms of power conversion efficiency and avoiding the above described issues of hard-switching bridge structures, it is desirable for transistors to operate in a soft switching regime. In applications where MOSFETs are used, as is the case in converter discussed within this thesis, the preferred option is zero-voltage switching (ZVS). By its successful utilization, the capacitive discharge which occurs at the turn-on under hard-switching conditions is avoided and thus the switching losses are eliminated [57]. ZVS operation of an H-bridge PFC rectifier has been demonstrated in [19, 20]. In both studies, ZVS was achieved by operating a conventional H-bridge converter in triangular conduction mode [2]. Highly efficient performance with high power density experimental converters was achieved in both cases. In addition to the line current, grid voltage, and output voltage measurements, a fast zero crossing

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[1] The synchronous transistor in a synchronous DC-DC converter is the one in place of the unidirectional structure's freewheeling diode. Its role is to provide a conductive path for the freewheeling current when the main channels of both transistors are in non-conductive state. Due to conduction through their body diodes synchronous transistors are subject to the reverse recovery effect. By replacing the synchronous transistor for a power diode, the DC-DC converter can still support a controlled power flow in one direction. Therefore the synchronous transistor in a synchronous boost converter is always the one with a floating source potential (high-side transistor), while the synchronous transistor of the synchronous buck converter is the one with the source connected to the ground (low-side transistor). Such definition cannot be adapted for AC-DC and DC-AC applications since the polarity of the alternating voltage is changing and the transistors within the bridge switch roles. In the remainder of this thesis the term synchronous transistor (syncFET) will be used for the transistor whose body diode conducts the freewheeling current, while the term main transistor (mainFET) will be used for the transistor which only conducts current through its main channel when opened.

[2] Triangular conduction mode is in its basics the equivalent of discontinuous conduction mode in unidirectional converters. When the inductor current is falling and stops flowing when it reaches zero in unidirectional converters, it changes direction and flows in the opposite way in bidirectional converters. For this reason the current does not have a discontinuous waveform, but maintains a triangular waveform at all times in bidirectional converters. For the sake of clarity, the term discontinuous conduction mode will be used in the remainder of this thesis for describing the operating mode beyond the border of critical conduction mode.

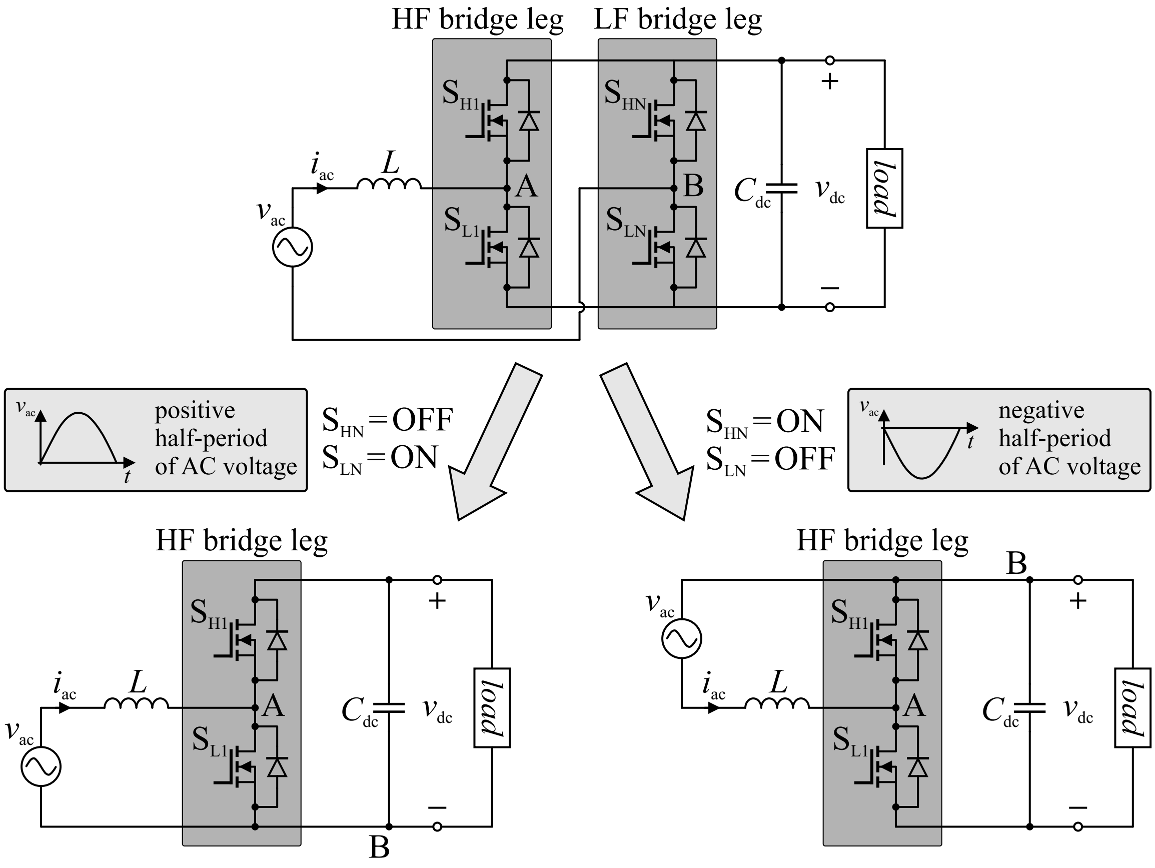

HF bridge leg
LF bridge leg
S_H1
S_HN
S_L1
S_LN
i_ac
L
v_ac
A
B
C_dc
v_dc
load
+
–
v_ac
t
positive
half-period
of AC voltage
S_HN = OFF
S_LN = ON
S_HN = ON
S_LN = OFF
negative
half-period
of AC voltage
HF bridge leg
HF bridge leg

Figure 2.3: Simplified schematic circuit of an H-bridge PFC rectifier (top) and its equivalent circuits in the positive and negative grid voltage half-period (bottom).

detection circuit was incorporated for realization of ZVS control. The control was implemented within a combination of a digital signal controller and CPLD in [20] and a combination of a digital signal controller and FPGA in [19].

The schematic circuit diagram of the investigated H-bridge PFC rectifier is shown in Fig. 2.3. Since achieving highly efficient operation of the converter represents one of the main objectives of this thesis, a hybrid pulse-width modulation (PWM) technique will be used [76]. In the case of utilizing hybrid PWM, only one converter leg is switched at high frequency, while the other leg is switched at low frequency of the utility grid voltage. Such operation results in negligible switching losses in the low-frequency switched leg since the switching transitions occur in the vicinity of the input current zero crossing. Due to this fact, transistors with the best conductive properties (which come with a worse switching performance) can be utilized in the low-frequency switched leg for reducing the conduction losses.

The transistors S_{HN} and S_{LN} of the the low-frequency switched leg serve for connecting the neutral line (N) of the AC source to either the positive or negative terminal of the output capacitor

C_{dc}, as can be seen in Fig. 2.3. By connecting N to the negative output terminal during the positive grid voltage half-period and to the positive output terminal during the negative grid voltage half-period, the hybrid modulated H-bridge operates as a synchronous DC-DC converter with a full-wave rectified grid voltage on its input terminals within both, the positive and negative, half-periods of the grid voltage. The equivalent circuits in both cases are shown in Fig. 2.3. For the sake of simplicity, the switching transition analysis and ZVS control design can be carried out on a half-bridge structure, which represents the high frequency switched converter leg.

CHAPTER 3

POWER SEMICONDUCTOR PROPERTIES

3.1 Unwanted phenomena in hard-switched bridge structures

The fundamental reason for the evolvement of synchronous DC-DC converters is the reduction of conduction losses achieved by replacing the freewheeling diode with a power transistor [77]. The latter has a considerably lower internal resistance in the conductive state than a fast Schottky diode and therefore lower conduction losses. Another favorable property of such a half-bridge synchronous rectification structure is the possibility of a bidirectional power flow [78]. In regard to this property such converters are widely used in different kinds of hybrid power systems like hybrid electric vehicles [52, 79–83] and smart residential nanogrids [28, 29]. Nonetheless, synchronous rectification also introduces several unwanted phenomena which are common to all bridge structures. A major concern in synchronous DC-DC converters is the reverse recovery effect of the syncFET's antiparallel body diode at the instant of turning on the mainFET. For the duration of the reverse recovery phenomena, both transistors are exposed to high current change rates and high peak reverse recovery currents which significantly increase switching losses, cause electromagnetic interference, and lead to dangerous operating conditions [71,72,75,84]. Another drawback of hard-switched converters that utilize synchronous rectification is the unwanted Cdv/dt-induced turn-on of the syncFET immediately after its body diode recovers [73, 74]. This phenomenon causes additional switching losses and in the worst case even a destructive shoot-through condition. The effects of both the reverse recovery and the spurious turn-on become more severe with higher voltage and

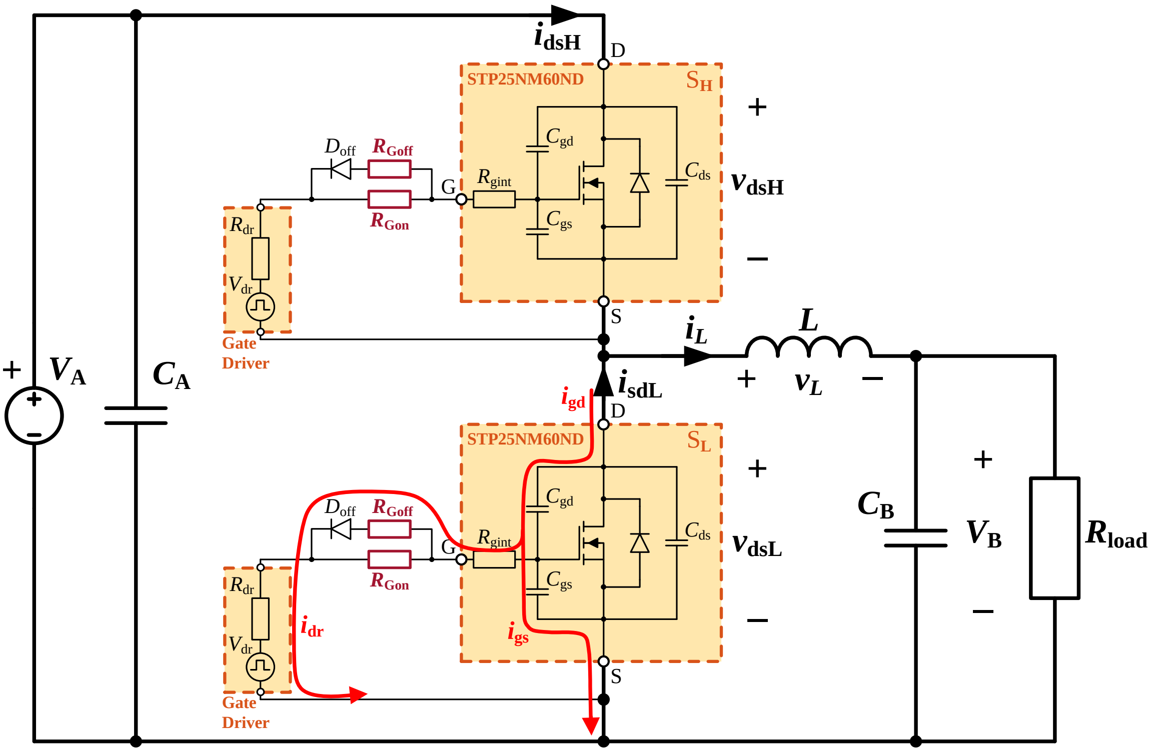
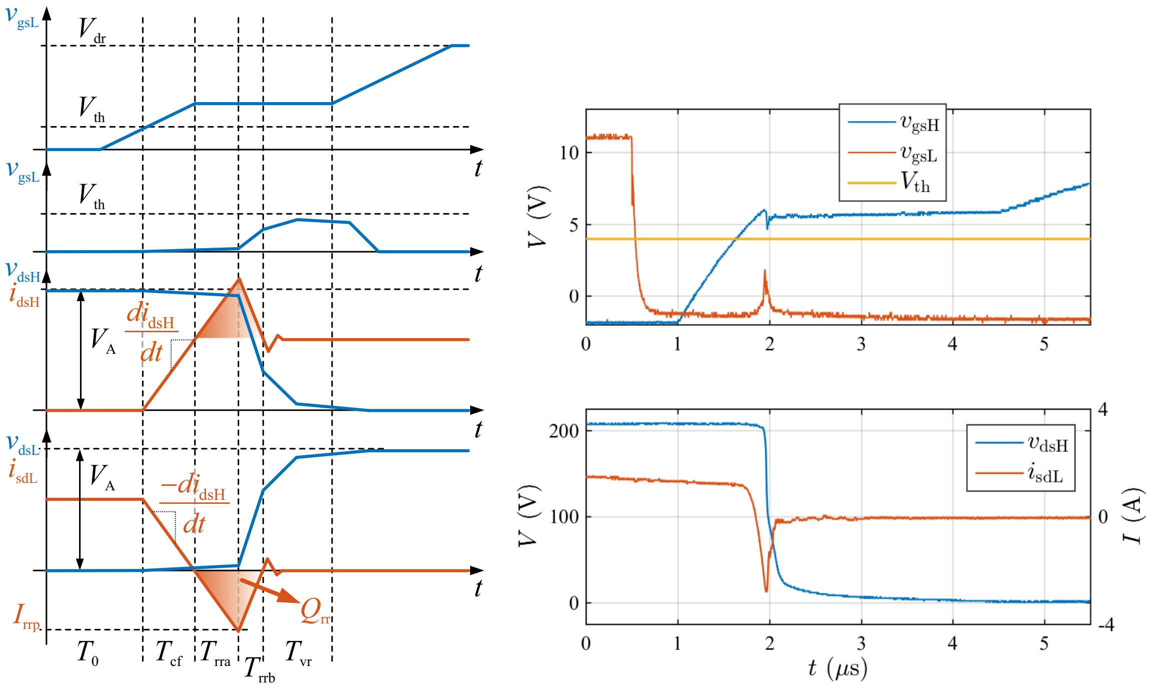

i_{dsH}
D
STP25NM60ND
$\mathrm{S_H}$
+
C_{gd}
D_{off}
R_{Goff}
G
R_{gint}
C_{ds}
v_{dsH}
R_{Gon}
C_{gs}
R_{dr}
V_{dr}
−
S
Gate Driver
+
V_{A}
C_{A}
i_L
L
i_{gd}
i_{sdL}
+
v_L
−
D
STP25NM60ND
$\mathrm{S_L}$
+
C_{gd}
D_{off}
R_{Goff}
G
R_{gint}
C_{ds}
v_{dsL}
C_{B}
+
V_{B}
−
R_{load}
R_{Gon}
R_{dr}
i_{dr}
C_{gs}
i_{gs}
V_{dr}
−
S
Gate Driver

Figure 3.1: Schematic circuit of a synchronous DC-DC converter operating in buck mode.

current levels, faster switching transitions, and higher switching frequencies.

A clear and simple explanation of both unwanted phenomena can be given on an example of a synchronous buck converter, the circuit of which is shown in Fig. 3.1. The schematic circuit also depicts a simplified MOSFET driving circuit. The simplified models of MOSFETs S_{H} and S_{L} include their internal gate resistance R_{gint} and parasitic capacitances between terminals C_{gs}, C_{gd}, and C_{ds}. The internal and external parasitic inductances of MOSFET terminals are not considered here, although their effect on both, the reverse recovery and spurious turn-on is not negligible [73, 74, 85, 86]. In a half-bridge structure utilized as a synchronous buck converter, as is the case in Fig. 3.1, the high-side transistor S_{H} always performs the role of the mainFET, while the low-side transistor acts as the syncFET.

In the CCM operation, the inductor current i_L is passed through the body diode of the syncFET during the dead time, when both transistors are turned off. At the instant at which the mainFET turns on, the body diode of the syncFET is still forward biased. There is a high concentration of charge carriers within the drift region and therefore the diode cannot stop conducting until these carriers are removed. For this reason the current through the syncFET's body diode is reducing with a certain slope, as evident from the i_{dsL} waveform within the interval T_{cf} in Fig. 3.2(a). When the current i_{dsL} reaches zero there are still minority carriers present in the drift region and therefore



(a)

(b)

Figure 3.2: Reverse recovery of the syncFET's body diode at turning on the mainFET: (a) piecewise linear approximated theoretical waveforms and (b) experimental waveforms.

the power source is shorted through the mainFET's main channel and the syncFET's body diode. Since the voltage v_{dsL} starts rising, the polarity of the voltage across the syncFET's body diode is reversed and therefore i_{dsL} starts flowing in the opposite direction. The interval T_{rra} finishes at the point in which most of the minority carriers were removed from the drift region and the diode cannot support the current anymore. At this point the peak reverse recovery current I_{rrp} is reached which denotes the beginning of interval T_{rrb}. Within T_{rrb} the syncFET's body diode current i_{sdL} falls rapidly while the remainder of minority carriers is removed. Consequently the diode becomes fully reverse-biased and the entire current i_{dsH} is passed through the inductor L towards the output of the converter. The experimental waveforms of the just described syncFET's body diode reverse recovery process are shown in Fig. 3.2(b), which confirms the piecewise linear approximated theoretical waveforms in Fig. 3.2(a).

The main and commonly discussed unwanted effect of the syncFET's body diode reverse recovery is the increase in switching losses [72,84,86–89]. A considerable current undershoot resulting from the reverse recovery process can be observed in Fig 3.2(b). This undershoot represents the shoot-through current flowing through both transistors of the half-bridge before the syncFET's body diode stops conducting, as evident from theoretical waveforms in Fig. 3.2(a). The two shaded areas represent the reverse recovery charge Q_{rr} and indicate additional switching losses in both transistors within the half-bridge. In terms of operating conditions, the reverse recovery energy Q_{rr} depends on the amplitude of the switched inductor current i_L, the rate of change of the decreasing current di_{sdL}/dt through the syncFET's body diode, and the junction temperature [3, 4]. Consequently there are two ways of reducing the reverse recovery induced switching losses. One is by optimizing the dead times during which the body diode conducts current. If the dead time is shorter than a complete turn-on transition of the body diode, the latter does not switch on completely and consequently there will be less charge to remove during the turn-off process. For achieving this, several dead time optimization schemes have been proposed [84, 86, 89–91]. However, there is a very thin line between achieving the optimum performance and selecting an insufficiently long dead time [86]. The latter causes a short-circuit across the half-bridge which leads to current spikes larger than the ones occurring during the above described reverse recovery process or in the worst case even a breakdown of the MOSFETs. Another way of reducing Q_{rr} and other reverse-recovery related issues is by limiting the slope of the current within the interval T_{cf}. In other words, this means slowing down the turn-on transition of the mainFET. With a lower rate of current change di_{dsH}/dt, lower I_{rrp} and Q_{rr} will be achieved, and consequently the reverse recovery losses will decrease. Although effective, this may not be the most efficient solution since longer switching transitions of the mainFET result in higher switching losses. On the other hand, achieving a lower I_{rrp} proves to be beneficial in terms of another unwanted phenomena in hard-switched bridge structures, known as the unwanted or spurious turn-on of the syncFET.

The unwanted turn-on of the syncFET may occur after its body diode recovers, as a consequence of high voltage and current rates of change within the interval T_{rrb}. Within this interval, the voltage v_{dsL} across the syncFET rapidly increases. The resulting positive dv_{dsL}/dt induces a current (denoted with i_{gd} in Fig. 3.1) which charges the gate of the syncFET through the parasitic capacitance C_{gd} [73, 92]. In case the voltage across C_{gs} exceeds the threshold value V_{th}, the snycFET is turned on and the power source is shorted across both MOSFETs of the half-bridge. Such a condition significantly increases the switching losses and in the worst case even causes a breakdown of the devices in the circuit.

There are several ways of preventing the unwanted turn-on of the syncFET. Selection of MOSFETs with higher threshold voltages V_{th} and gate charge ratios lower than 1 considerably improves the unwanted turn-on immunity [93]. Another thing worthy of consideration is the softness of reverse recovery. A diode (also applies to the body diodes of MOSFETs) with a softer recovery exhibits a longer duration of the interval T_{rrb} in Fig. 3.2(a) and consequently the voltage rate of change

dv_{dsL}/dt is also lower. In addition to the fact that there are few high voltage MOSFETs with soft recovery body diodes on the market, soft recovery generally increases the reverse recovery losses [87]. The unwanted turn-on immunity can be substantially increased by a proper printed-circuit board (PCB) layout. The parasitic inductances within the circuit, of which the source inductance is the most critical, amplify the effect and may push v_{gsL} way above the threshold value [85]. The design of the gate driving circuit is also very important. By applying a negative voltage across the gate and source terminals of the MOSFET during the period when it should be in a non-conductive state, the immunity to spurious turn-on can be increased [73, 74].

It is evident from Fig. 3.1 that the dv/dt induced current i_{gd} has two available paths for circulation. One is through the gate-to-source capacitance C_{gs}, while the other one is through the internal R_{gint} and external R_{Goff} gate resistors in series with the gate driver, which also has some internal resistance R_{dr}. For ensuring high immunity to unwanted turn-on, a low impedance path through the gate driving circuit has to be provided. This way the major portion of i_{gd} will flow through the gate driving circuit without charging the capacitor C_{gs}. A low impedance design of the gate driving circuit requires selection of a gate driver with high sink current capability, such as Texas Instruments' LM5112 [94], low resistance of the external gate resistor R_{Goff}, and minimization of the gate driving loop inductance. Regarding the prevention of unwanted turn-on, the optimum value of the external gate resistor R_{Goff} is zero. Since such a value of gate resistance largely increases the level of switching noise, a trade-off must be found between the desired unwanted turn-on immunity and allowed electromagnetic interference.

An asymmetric gate driving circuit [93] has proven to be very useful in bridge structures. Its main idea is in connecting a fast switching diode in parallel with the external gate resistor R_{Goff}, as shown in Fig. 3.1, and thus provide a low impedance path for the current when discharging the gate of the MOSFET. Its main advantage is that it helps to solve both the above described issues of hard-switched bridge structures. By using an external turn-on resistor R_{Gon} of higher resistance, the turn-on transitions of mainFET can be slowed down to the point at which acceptable current and voltage rates of change are achieved. On the other hand, a close to zero external turn-off resistance R_{Goff} can be used for achieving fast turn-offs and ensuring a low impedance path through the gate driving circuit for the dv/dt induced current at the turn-on of the mainFET. Regarding the selection of R_{Gon} and R_{Goff} resistance values, there is a trade-off between achieving a safe, highly efficient, and low EMI operation.

The influence of the external gate turn-on resistor R_{Gon} on switching transitions is demonstrated in Fig. 3.3. The results showed significantly lower dv_{dsH}/dt and di_{dsL}/dt when employing R_{Gon}

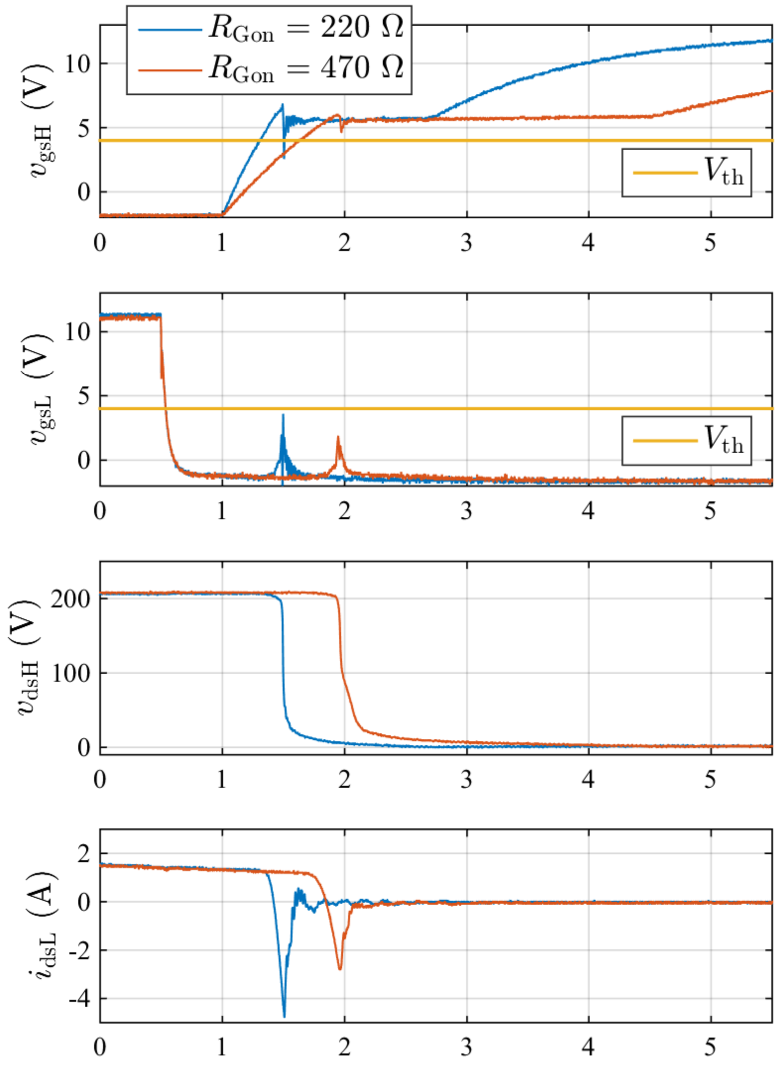


Figure 3.3: Effect of the external gate resistor R_{Gon} on switching transitions when turning on the mainFET. A turn-off resistor $R_{\text{Goff}} = 6.8\ \Omega$ was used in both presented cases.

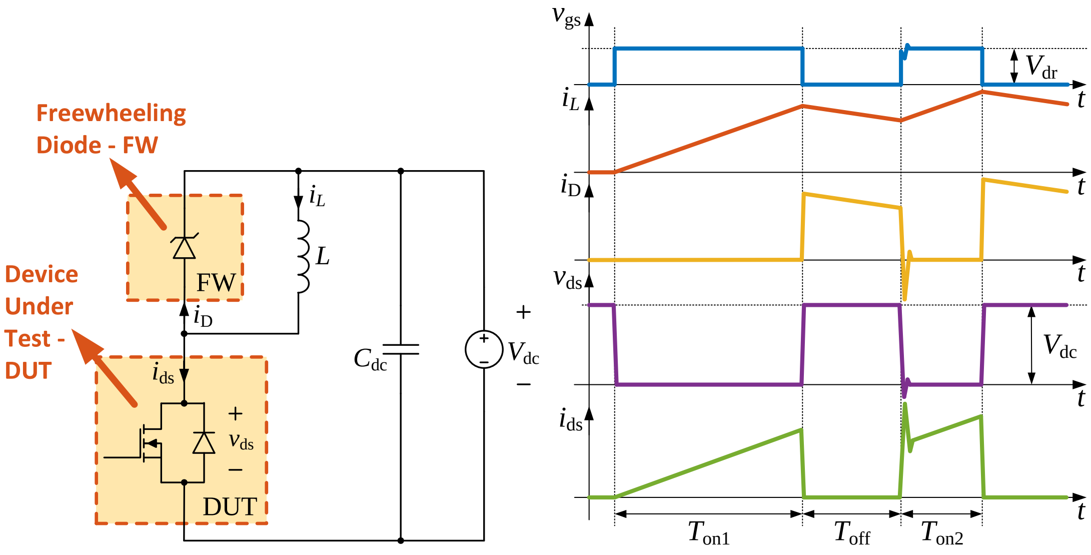
with a higher resistance. As a consequence of lower voltage rate of change across the syncFET there is also a considerably lower rise in v_{gsL} and less oscillations during the switching transition. Usage of a higher turn-on resistance R_{Gon} therefore effectively suppresses the reverse recovery effect as well as provides higher unwanted turn-on immunity. On the other hand, it also increases the mainFET's turn-on losses and introduces an additional turn-on delay, as evident from Fig. 3.3. Since the rate of voltage and current change during the switching transitions also depend on the switched voltage and current, the optimal selection of the external gate resistors R_{Gon} and R_{Goff} is the one that achieves the fastest turn-on of the mainFET at the maximum expected current during which the voltage v_{gsL} will not rise above the threshold value V_{th}.

3.2 Switching characteristic

Switching transitions in power MOSFETs are very complex processes influenced by numerous parasitic elements present within their cases as well as within the circuits in which the MOSFETs are placed. For this reason, the modeling of switching transitions and accurate calculation of switching losses is a rather challenging task. The analysis becomes even more complex when MOSFETs are used in a bridge structure, as is the case in converters discussed within this thesis. The two transistors within one converter leg affect each other, which in most cases deteriorates the switching performances of both. The reverse recovery effect and unwanted turn-on of the syncFET can be taken as examples. Although both occur within the syncFET, the resulting shoot-through current which flows through the converter leg increases switching losses in both transistors (see Fig. 3.2). Due to such effects, nonlinear parasitic capacitances between the MOSFET's terminals, and the effects of the PCB layout on switching transitions, it is very difficult to calculate switching losses accurately.

The simplest and widely used piecewise linear model for estimating switching losses [95] is acceptable for general switching loss estimation or basic switching performance comparisons of MOSFETs on the basis of information provided in the datasheet. However, the piecewise linear model is not very accurate since it considers the parasitic MOSFET capacitances as linear, and neglects all the parasitic inductances and reverse recovery losses. The effects of nonlinear parasitic capacitances on switching losses are better incorporated within the switching loss model proposed in [96, 97], while the parasitic inductances and reverse recovery effect are still neglected. In addition, the presented models require information about several MOSFET parameters, which are not common in modern high-voltage power MOSFETs. On the other hand, several analytical switching loss models for synchronous DC-DC converters have been reported, which include the effects of the parasitic capacitances, inductances, and reverse recovery [98–100]. These models allow for a fairly accurate switching loss estimation but are rather complex and require a detailed analysis of the PCB layout for extracting the values of parasitic elements involved in the models.

For avoiding uncertainty and a detailed analysis of the PCB layout and driving stage parasitics, the switching losses were calculated from the measured voltage and current waveforms during the switching transitions. The experimental switching waveforms were obtained by performing a set of inductive load switching tests. A conventional circuit for testing the switching transitions with an inductive load and the corresponding piecewise linear theoretical waveforms are shown in Fig. 3.4 [101, 102]. A fast Schottky diode is normally used for providing the path for freewheeling current while the device under test (DUT) is turned off (interval T_{off} in Fig. 3.4(b)). The Scottky



(a) (b)

Figure 3.4: Conventional inductive load switching test; (a) schematic circuit and (b) theoretical current and voltage waveforms.

diodes, especially the ones made of Silicon Carbide (SiC), have a very low to almost negligible reverse recovery charge. By utilizing them in switching transition tests, the reverse recovery effect is practically eliminated and therefore it is possible to obtain the actual switching transition times and losses of the DUT. However, this thesis focuses on MOSFETs in bridge structures where, instead of a fast Schottky diode, there is another MOSFET. The internal body diodes of MOSFETs, through which the freewheeling current is passed within dead times, exhibit a considerably worse switching performance due to higher reverse recovery charge. As a result, the turn-on transition of the mainFET (DUT in this case) always comprises the additional reverse recovery induced losses due to the presence of another MOSFET in the half-bridge. In order to capture the entire switching losses generated during the turn-on of the mainFET in a half-bridge based converter, the fast diode (FW) in Fig. 3.4(a) has to be replaced with another MOSFET. The circuit of the synchronous DC-DC converter in Fig. 3.1 can be adapted for the purpose of the inductive load switching test, as is shown in Fig. 3.5.

The list of components used within the tested converter's power and gate driving circuit is provided in Table 3.1. All the tests were carried out at the voltage of $V_{\mathrm{A}} = 400\mathrm{V}$, which represents the nominal DC voltage in the final application of converters discussed throughout this thesis. The external gate resistors R_{Gon} and R_{Goff} were selected such that the mainFET can be safely turned on at a maximum current of $i_L = 9\mathrm{A}$ at the voltage level of $V_{\mathrm{A}} = 400\mathrm{V}$. In order to obtain a

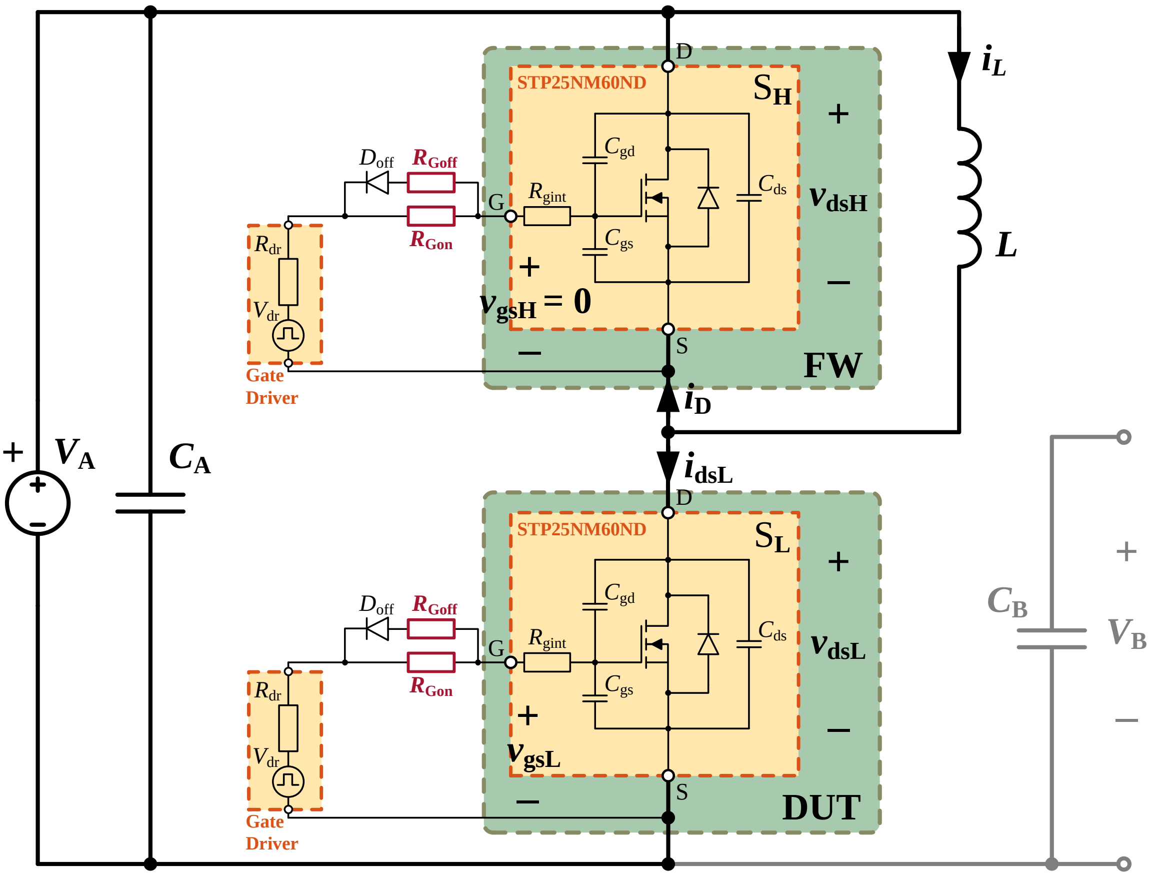

i_L
L
D
STP25NM60ND
S_H
+
v_{dsH}
−
C_{gd}
C_{ds}
R_{gint}
C_{gs}
G
D_{off}
R_{Goff}
R_{Gon}
R_{dr}
V_{dr}
Gate Driver
+
$v_{gsH} = 0$
−
S
FW
i_D
i_{dsL}
+
V_A
C_A
D
STP25NM60ND
S_L
+
v_{dsL}
−
C_{gd}
C_{ds}
R_{gint}
C_{gs}
G
D_{off}
R_{Goff}
R_{Gon}
R_{dr}
V_{dr}
Gate Driver
+
v_{gsL}
−
S
DUT
C_B
+
V_B
−

Figure 3.5: Schematic circuit of a synchronous DC-DC converter adapted for performing the inductive load switching test.

characteristic that would represent the switching energies as a function of the switched current, the switching transitions were recorded at different values of inductor current i_L. Experimental switching waveforms for the test at a moderate current level are shown in Fig. 3.6, while the waveforms of the test at the maximum turn-on current are depicted in Fig. 3.7.

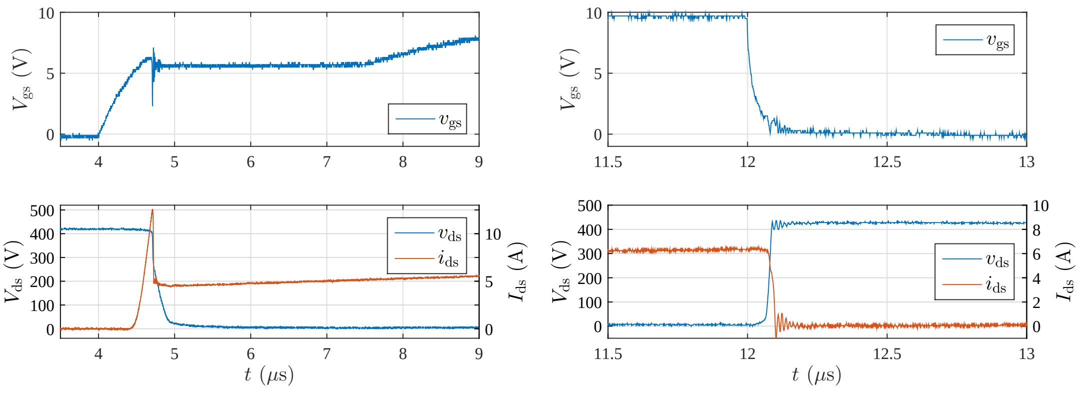
On the basis of the obtained DUT's drain-to-source voltage v_{dsL} and current i_{dsL} waveforms, the switching energies E_{sw} of turning the DUT on and off were calculated as

$$E_{\mathrm{sw}} = \int_{t_0}^{t_{end}} |v_{\mathrm{dsL}}(t) \cdot i_{\mathrm{dsL}}(t)| dt, \tag{3.1}$$

where t_0 is the time instant at which the switching transition begins and t_{end} the time instant at which the switching transition finishes. The obtained turn-on and turn-off switching characteristics are shown in Fig. 3.8. It is evident from the figure that the turn-on energy E_{on} is much higher than the turn-off energy E_{off} at all values of the switched current, which indicates that the turn-on losses will be dominant when operating a half-bridge based converter in a hard-switching regime. For the purpose of switching loss estimation in different operating points, regimes, or even applications

Table 3.1: Main power and driving circuit components of the experimental bidirectional DC-DC converter on which the switching transition tests were performed.

Symbol	**Description**
$S_{\mathrm{H}}, S_{\mathrm{L}}$	STMicroelectronics, STP25NM60ND, N-channel Power MOSFET, 600 V, 21 A
L	Power inductor, 660 μH Magnetics, High Flux, C058438A2, 48 turns, AWG17
C_{A}	High-voltage side capacitor bank 10x Panasonic, ECW-FA2J225J, 2.2μF, 630V 18x TDK, CKG57NX7T2J105M500JH, 1μF, 630V
D_{off}	Diodes Inc, 1N4148WS, Surface mount fast switching diode, SOD323
R_{Gon}	270 Ω, SMD 1206, 1 %, 0.25 W
R_{Goff}	1 Ω, SMD 1206, 1 %, 0.25 W
–	SiLabs, Si8230BB, 5kV Isolated Gate Driver, 4 A sink current



(a) (b)

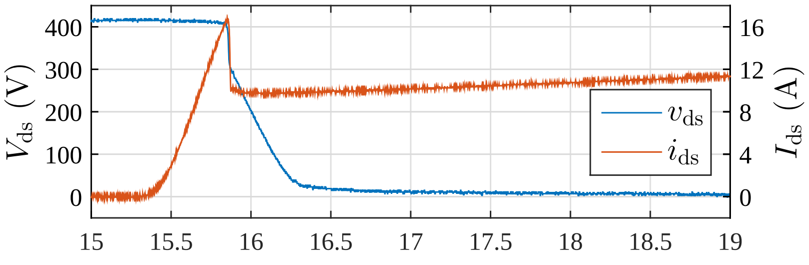
Figure 3.6: Inductive load switching test waveforms (a) for turning on the DUT at $i_L = 4.8$A and (b) turning it off at $i_L = 6.2$A.

in which a similar switching cell, driving circuit layout, and components are used, the measured switching characteristic was approximated by a second-order polynomial, yielding the following turn-on and turn-off switching energies:

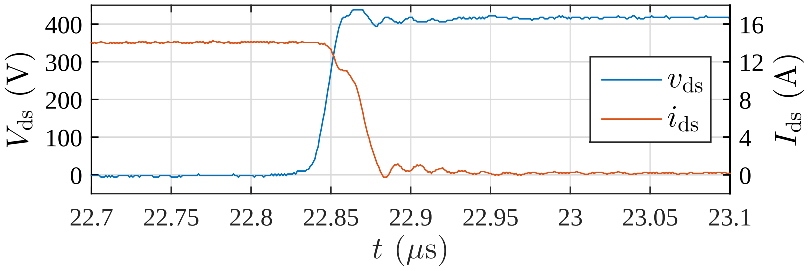
$$E_{\mathrm{on}} = 14.38\, i_L^2 + 76.36\, i_L + 57.73, \tag{3.2}$$

$$E_{\mathrm{off}} = 0.456\, i_L^2 + 2.051\, i_L + 8.497. \tag{3.3}$$

Note that the switching energies E_{on} and E_{off} are a function of the instantaneous inductor current



(a)



(b)

Figure 3.7: Inductive load switching test waveforms (a) for turning on the DUT at $i_L = 9.8$A and (b) turning it off at $i_L = 14.1$A.

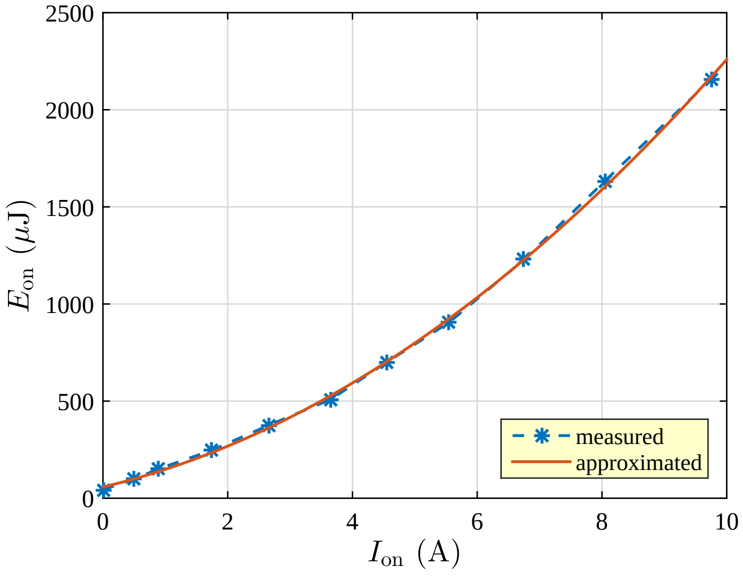
i_{L} at which a specific switching transition occurs. The switching energies calculated according to (3.2) and (3.3) are obtained in μJ.

3.3 Conduction loss

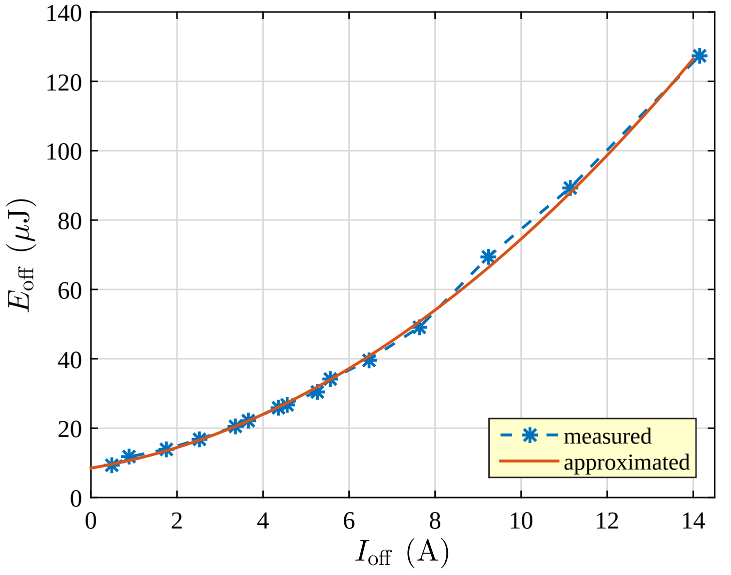
In contrast to estimating the switching losses, conduction losses in semiconductor devices are much easier to estimate. In a power MOSFET, the forward conduction losses depend exclusively on the rms current flowing through the transistor and its total drain-to-source on-resistance $R_{\text{ds,on}}$ [4, 101]. Hence, the forward conduction losses P_{cond} are calculated as

$$P_{\text{cond}} = I^2_{\text{ds,rms}} R_{\text{ds,on}}, \tag{3.4}$$

where $I_{\text{ds,rms}}$ is the rms value of the drain-to-source current through the transistor. Although $R_{\text{ds,on}}$ depends on several operating conditions like junction temperature and applied gate bias voltage [101], this does not represent a problem for estimating conduction losses since all the characteristics are usually provided in the datasheet [102]. It must be noted that there is also the reverse conduction mechanism, represented by the anti-parallel internal body diode of the MOSFET, which has different conductive properties. Due to very short time intervals within which the body diodes



(a)



(b)

Figure 3.8: Experimentally measured and approximated switching energy characteristic (a) at turning on and (b) turning off an STP25NM60ND transistor in a bridge structure.

of MOSFETs conduct the freewheeling current in the synchronous DC-DC or H-bridge AC-DC converters, their effect on conduction losses will be neglected at this point. For the purpose of conduction loss estimation, it will be assumed that the reverse conduction has the same properties as forward conduction through the main channel of the MOSFET.

When a synchronous DC-DC converter is operating in steady state, the rms inductor current $I_{\mathrm{L,rms}}$ is constant within each switching cycle and can be written as

$$I_{\mathrm{L,rms}} = \sqrt{I_{\mathrm{L,avg}}^2 + \frac{1}{12}\Delta I_{\mathrm{Lpp}}^2}, \tag{3.5}$$

where $I_{\mathrm{L,avg}}$ is the average inductor current and ΔI_{Lpp} the peak-to-peak inductor current ripple. The inductor current i_{L} is passed through one of two MOSFETs in the half-bridge at all times. In case both utilized MOSFETs are equal, they introduce the same resistance $R_{\mathrm{ds,on}}$ into the current path. Consequently, total semiconductor conduction losses P_{cond} can be calculated by assuming $I_{L,\mathrm{rms}} = I_{\mathrm{ds,rms}}$ and substituting (3.5) into (3.4). A further distribution of conduction losses among both MOSFETs in a synchronous DC-DC converter can be obtained on the basis of voltage conversion ratios as

$$P_{\mathrm{cond,S_H}} = \left(\frac{V_{\mathrm{B}}}{V_{\mathrm{A}}}\right) I_{L,\mathrm{rms}} R_{\mathrm{ds,on}}, \tag{3.6}$$

$$P_{\mathrm{cond,S_L}} = \left(1 - \frac{V_{\mathrm{B}}}{V_{\mathrm{A}}}\right) I_{L,\mathrm{rms}} R_{\mathrm{ds,on}}. \tag{3.7}$$

Although the operation of a synchronous DC-DC converter resembles the operation of the HF-switched leg of a hybrid modulated H-bridge PFC rectifier, the expressions (3.5), (3.6), and (3.7) cannot be applied for calculation of conduction losses due to the time varying ac voltage of the utility grid. Under such conditions, the local rms inductor current $I_{L,\mathrm{rms}}(\omega t)$ within each switching cycle varies in steady state operation, and can be written as

$$I_{L,\mathrm{rms}}(\omega t) = \sqrt{I_{L,\mathrm{avg}}^2(\omega t) + \frac{1}{12}\Delta I_{L\mathrm{pp}}^2(\omega t)}, \tag{3.8}$$

where $I_{L,\mathrm{avg}}(\omega t)$ is the local average inductor current, $\Delta I_{L\mathrm{pp}}(\omega t)$ the local peak-to-peak ripple of the inductor current, and ω the angular frequency of the grid voltage. In the LF-switched converter leg, one of transistors S_{NH} and S_{NL} conducts within each half-period of grid voltage. Therefore the average conduction losses P_{condSxN} over one period of grid voltage can be calculated as

$$P_{\mathrm{cond,SxN}} = \frac{1}{\omega T} \int\limits_{\omega t}^{\omega\left(t+\frac{T}{2}\right)} \left[(I_{L,\mathrm{rms}}(\omega t))^2 R_{\mathrm{ds,onLF}} \right] d\,(\omega t), \tag{3.9}$$

where $R_{\mathrm{ds,onLF}}$ represents the total drain-to-source on-resistance of each LF-switched MOSFET, while x in the subscript of $P_{\mathrm{cond,SxN}}$ replaces either H for the high-side transistor or L for the low-side transistor in the HF-switched leg. In the HF-switched converter leg, one of the transistors performs the role of a mainFET and the other one the role of a syncFET within the positive half-period of grid voltage, while their roles are switched in the negative half-period of grid voltage, as is evident from equivalent circuits in Fig. 2.3. Whenever the effective voltage conversion ratio $\frac{V_{\mathrm{ac}}}{V_{\mathrm{dc}}}$ differs from 0.5, the conduction losses in the mainFET and syncFET are different within one grid voltage half-period. In steady state operation, both half-periods are symmetric in terms of the current passed through the converter and both HF-switched transistors perform as mainFET and syncFET for the same amount of time. Therefore the average conduction losses generated on each HF-switched MOSFET over one period of grid voltage are equal and can be calculated as

$$P_{\mathrm{cond,Sx}} = \frac{1}{\omega T} \int\limits_{\omega t}^{\omega\left(t+\frac{T}{2}\right)} \left[\left(I_{L,\mathrm{rms}}(\omega t) \right)^2 R_{\mathrm{ds,onHF}} \right] d\,(\omega t), \tag{3.10}$$

where $R_{\mathrm{ds,onHF}}$ represents the total drain-to-source on-resistance of each HF-switched MOSFET, while x in the subscript of $P_{\mathrm{cond,Sx}}$ replaces either H for the high-side transistor or L for the low-side transistor in the HF-switched leg. The total semiconductor conduction losses in a hybrid modulated H-bridge PFC rectifier can be obtained as

$$P_{\mathrm{cond}} = 2P_{\mathrm{cond,Sx}} + 2P_{\mathrm{cond,SxN}}. \tag{3.11}$$

3.4 Semiconductor power loss comparison

A common and effective approach for increasing the power density and reducing the size and weight of switching power converters is to operate at higher switching frequencies. The latter allow for achieving the same quality of input and output current and voltage waveforms, with a considerably smaller sizes of passive components in the converter's circuit. Nonetheless, higher switching frequencies negatively affect the switching losses which are strongly frequency-dependent. The influence of the operating switching frequency f_{sw} on semiconductor losses and the size of the power inductor L is demonstrated in Fig. 3.9. The figure provides a comparison of particular semiconductor losses generated within a hybrid modulated PFC rectifier (see Fig. 2.3) and a synchronous DC-DC converter (see Fig. 3.1) operating in CCM at an input power of 1 kW. The operating parameters of both converters are listed in Table 3.2. The corresponding inductance of the power inductor L in Fig. 3.9 is calculated such that the maximum peak-to-peak inductor current ripple $\Delta I_{L\mathrm{pp,max}}$ equals 40 % of the average inductor current's I_L peak value. Thus, the required inductance L_{ccm} for the hybrid modulated PFC rectifier was calculated as

$$L_{\mathrm{ccm}} = \frac{V_{\mathrm{dc}}}{4 f_{\mathrm{sw}} \Delta I_{L\mathrm{pp,max}}}, \tag{3.12}$$

while the required inductance L_{ccm} for a synchronous DC-DC converter was obtained as

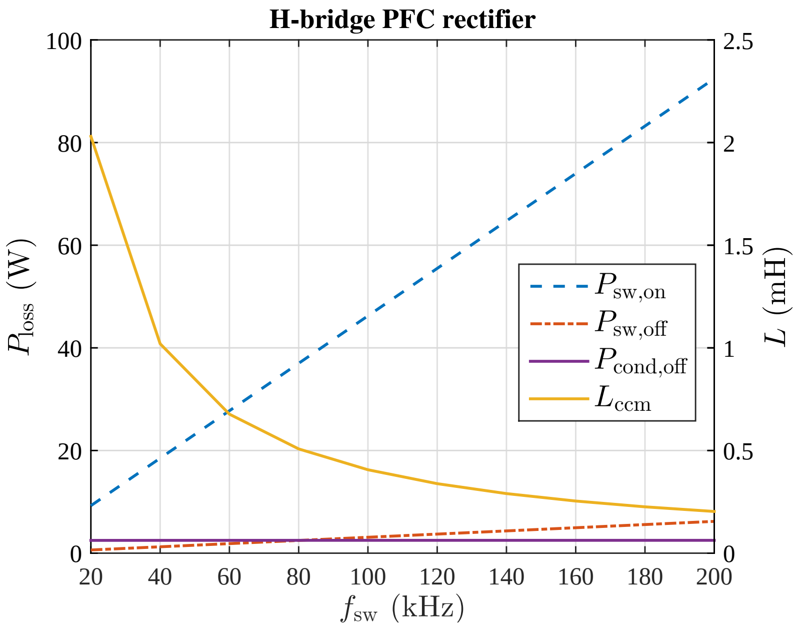
$$L_{\mathrm{ccm}} = \frac{V_{\mathrm{B}} \left(1 - \frac{V_{\mathrm{B}}}{V_{\mathrm{A}}} \right)}{f_{\mathrm{sw}} \Delta I_{L\mathrm{pp,max}}}. \tag{3.13}$$

Table 3.2: Basic parameters for semiconductor loss comparison in different bridge structures

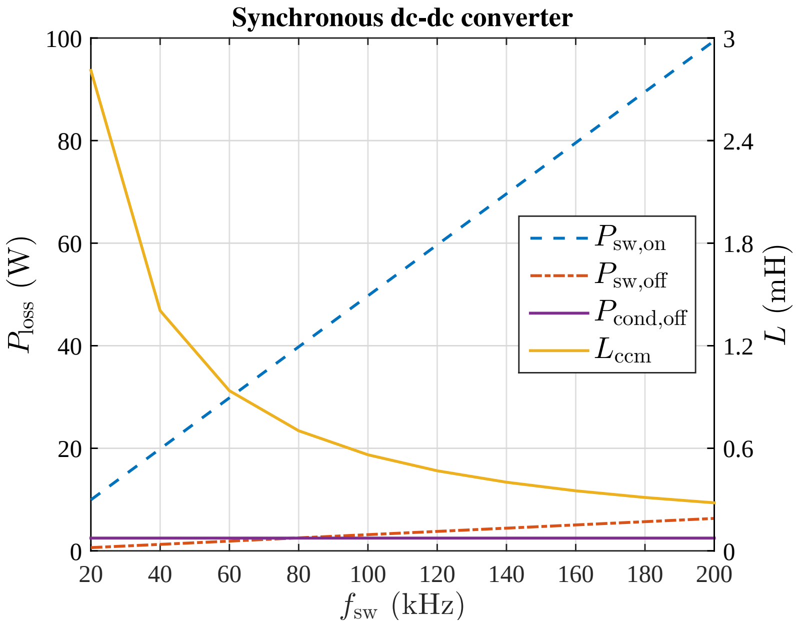
	Parameter	**Value**
H-bridge PFC rectifier	P_o	1000 W
	V_dc	400 V
	V_ac	230 V
	$\Delta I_{L\mathrm{pp,max}}$	$0.4 \cdot \hat{I}_\mathrm{ac}$
Synchronous DC-DC converter	P_o	1000 W
	V_A	400 V
	V_B	230 V
	$\Delta I_{L\mathrm{pp,max}}$	$0.4 \cdot I_\mathrm{B}$

The switching losses presented in Fig. 3.9 were calculated from (3.2) and (3.3), in which I_L represents the current at which the switching transition occurs. To be more specific, the turn-on of the mainFET always occurs at $I_L = I_{L,\mathrm{avg}} - 0.5\Delta I_{L\mathrm{pp}}$, while the turn-off of the mainFET occurs at $I_L = I_{L,\mathrm{avg}} + 0.5\Delta I_{L\mathrm{pp}}$. Except for the reverse recovery losses, which are not explicitly presented in Fig. 3.9, there are no switching losses generated in the syncFET. The causes for this will be explained in detail in the following chapter. It is evident from both Fig. 3.9(a) and Fig. 3.9(b) that the turn-on losses are dominant and, the same as turn-off losses, proportional to the switching frequency f_sw. In contrast to the switching losses, the conduction losses are not frequency dependent and, at higher switching frequencies, practically negligible in such high-voltage low-current applications.

The physical size of the power inductor is associated with the required value of its inductance L_ccm. It is evident from Fig. 3.9 that L_ccm requirements for achieving the desired $\Delta I_{L\mathrm{pp}}$ are significantly lower at higher switching frequencies f_sw. Since the switching losses increase with the switching frequency, it can be inferred that a reduction in the size of the passive components results in a lower power conversion efficiency when the converter is operating in CCM with hard-switching. In order to overcome this limitation the following chapter focuses on achieving zero-voltage switching in a half-bridge based converter.



(a)



(b)

Figure 3.9: Semiconductor loss comparison and required inductance for CCM operation L_{ccm} in a) a hybrid modulated H-bridge rectifier and b) a synchronous DC-DC converter operating at the output power of $P_{\mathrm{o}} = 1$ kW in hard-switching regime.

CHAPTER 4

ZVS IN DISCONTINUOUS CONDUCTION MODE

4.1 ZVS in discontinuous conduction mode

As it was demonstrated in Chapter 3, switching losses represent the highest share in total power loss of a high-voltage low-current hard-switched full-bridge and half-bridge converters operating at switching frequencies above 20 kHz. Further switching loss breakdown resulted in finding that turn-on losses are dominant and impose the main limiting factor for increasing the switching frequency and thus reducing the sizes of the power conditioning units, especially in high voltage applications. The reason for the dominance of turn-on losses is in the need for slowing down the switching transitions to the point where the converter can safely operate at the desired blocking voltage and load current. In other words, the MOSFET's drain-to-source voltage and current rates of change at the turn-on have to be limited in order to prevent any unwanted turn-on of the syncFET, as explained in Section 4.2.2. Lower voltage and current rates of change during switching transitions directly result in increased switching losses and a demand for high transistor cooling capacity in high voltage and higher power converters utilizing transistors in a bridge-based structure. In addition to an increased demand for cooling capacity, high switching losses also impose stringent limitations on the maximum allowed switching frequency, which is a key parameter for sizing passive components in the circuit. To sum it all up, high voltage hard switched synchronous converters generate a vast amount of switching losses and therefore require a large cooling system, as well as rather large passive components, due to operation at switching frequencies of several tens of kilohertz. In order

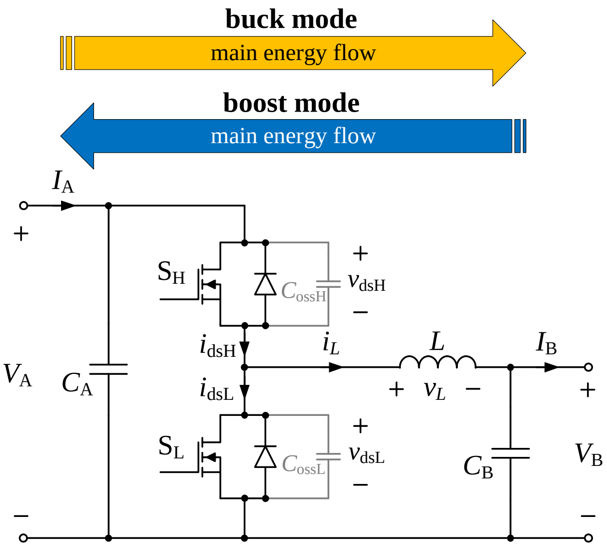


Figure 4.1: Schematic circuit diagram of a conventional nonisolated bidirectional DC-DC converter.

to reduce the size and weight of a converter and at the same time maintain high power conversion efficiency, it is necessary to operate the converter in a ZVS regime.

One way of achieving ZVS in a half-bridge based bidirectional DC-DC converter that utilizes synchronous rectification is by operating the converter in the DCM. The power circuit of the discussed bidirectional DC-DC converter is shown in Fig. 4.1. Such a converter can operate in two operating modes, depending on the direction of the main energy flow. When the average inductor current $I_{L,\mathrm{avg}}$ flows in the direction from V_{A} to V_{B} the converter operates in buck mode, in which $\mathrm{S_H}$ acts as a mainFET and $\mathrm{S_L}$ as a syncFET. In the other case, when $I_{L,\mathrm{avg}}$ flows in the opposite direction, the roles of both transistors in the circuit are exchanged. Figure 4.1 also depicts the voltage-dependent non-linear parasitic output capacitors C_{ossH} and C_{ossL} which are of significant importance when studying the switching transitions of power MOSFETs.

The mechanism for achieving zero-voltage turn-ons of both transistors within the circuit can be explained on the basis of the equivalent circuits shown in Fig. 4.2. The explanation, as well as the presented equivalent circuits, are focused on the buck operating mode. However, the same switching states and mechanisms apply for boost mode as well, it is just that the transistors switch roles and the inductor current i_L flows in the opposite direction. Each equivalent circuit in Fig. 4.2 represents one of eight different switching states inside one switching cycle of a synchronous buck converter operated in DCM. It should be noted that the equivalent circuits (a)-(d) are common to both CCM and DCM operation. After $\mathrm{S_H}$ is turned off, the main transition period begins that corresponds to the equivalent circuit (b). Assuming that the dead time is long enough, the inductor current i_L completely discharges C_{ossL}, while C_{ossH} is simultaneously charged to the input voltage V_{A}. As

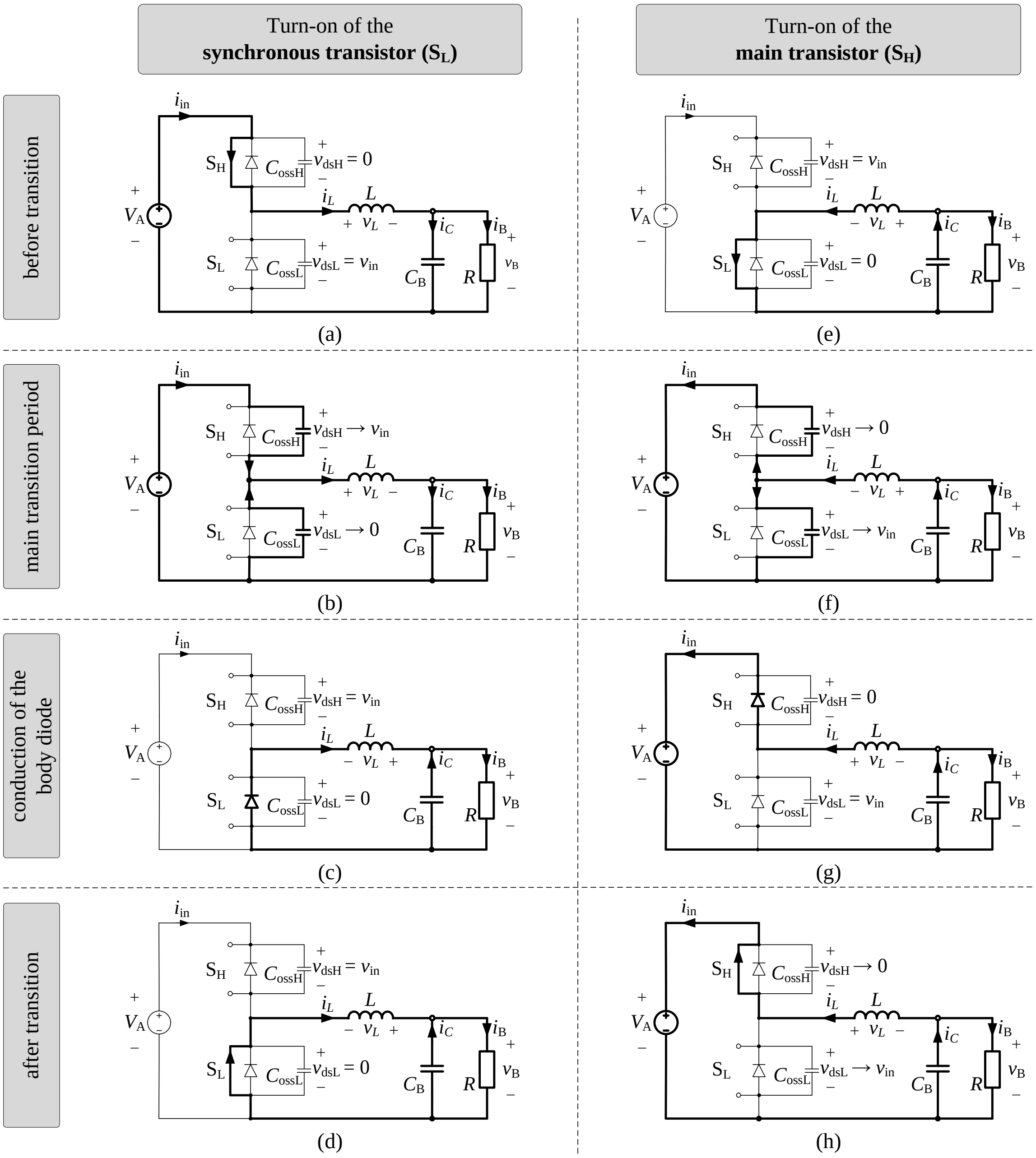

Turn-on of the
synchronous transistor (S_L)
Turn-on of the
main transistor (S_H)
before transition
main transition period
conduction of the body diode
after transition
i_in
S_H
S_L
C_ossH
C_ossL
v_dsH = 0
v_dsL = v_in
v_dsH = v_in
v_dsL = 0
v_dsH → v_in
v_dsL → 0
v_dsH → 0
v_dsL → v_in
i_L
L
v_L
i_C
i_B
C_B
R
v_B
V_A
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)

Figure 4.2: Equivalent circuit diagrams for the buck mode of a bidirectional DC-DC converter operating in DCM.

soon as the drain-to-source voltage v_{dsL} across $\mathrm{S_L}$ falls to zero, the body diode of the syncFET takes over the current, as depicted by circuit (c). In the next phase, the syncFET $\mathrm{S_L}$ is naturally turned on at zero voltage in both CCM and DCM. The antiparallel body diode of the mainFET $\mathrm{S_H}$ does not take over any current during this transition, hence the absence of reverse recovery effect in the mainFETs of the synchronous DC-DC converters.

A much more delicate issue is the turn-on transition of the mainFET, the parasitic output capacitor of which cannot be naturally discharged in the CCM operation. Therefore the mainFET is turned on at the input voltage V_{A}. Such transitions generate a considerable amount of losses, which significantly affect the power conversion efficiency when operating at higher switching frequencies and higher voltages. In addition, the turn-on of the mainFET at the input voltage proves to be problematic because it pushes the syncFET's antiparallel body diode into reverse recovery. This generates additional losses and leads to dangerous operating conditions at higher blocking voltages and load currents.

The idea behind achieving zero-voltage transitions in the DCM is in ensuring the required amount of reversed current I_{R} that can discharge the parasitic output capacitor C_{ossH} of the mainFET when operating in buck mode. The principle is evident from the equivalent circuits (e)-(h) in Fig. 4.2. The turn-off instant of $\mathrm{S_L}$ is delayed, so that the inductor current i_L changes direction, as depicted by equivalent circuit (e). The latter is the first circuit state not present in the CCM or the CCM/DCM boundary operation and is essential for achieving the conditions required for zero-voltage turn-on of the mainFET $\mathrm{S_H}$. As the syncFET $\mathrm{S_L}$ remains in the conductive state, the inductor current i_L keeps falling until it reaches the predetermined reversed current I_R required for a complete discharge of the parasitic capacitor C_{ossH}. After $\mathrm{S_L}$ is turned off, the main transition period begins. The parasitic output capacitor C_{ossL} of the syncFET is charged to the input voltage V_{A}, while the parasitic output capacitor C_{ossH} of the mainFET discharges. As soon as the drain-to-source voltage v_{dsH} across $\mathrm{S_H}$ falls to zero, the antiparallel body diode of this transistor takes over the current, as depicted by equivalent circuit (g). Subsequently, $\mathrm{S_H}$ can be turned on at zero voltage. In addition to negligible turn-on losses of $\mathrm{S_H}$, the switching states described with equivalent circuits (e)-(h) also avoid passing the current through the antiparallel body diode of $\mathrm{S_L}$ and thus eliminate the reverse recovery induced losses.

4.2 Zero-voltage turn-on of the mainFET

The key for achieving zero-voltage turn-on of the syncFET in both CCM and DCM is in providing a sufficiently long dead time, i.e. time interval between turning off the mainFET and turning on the syncFET. As the mainFET is turned off at the peak inductor current, which charges its parasitic output capacitance to the voltage V_{A} and discharges the parasitic capacitor across the syncFET in a rather short time, a close to minimum required dead time for preventing simultaneous conduction of both transistors is sufficient for achieving zero-voltage turn-on of the syncFET. In addition, an excessive dead time does not represent a threat of losing ZVS, as there is no mechanism that would cause the reversed process of recharging the parasitic capacitor across the syncFET after it is once discharged. An excessive dead time may only cause a slight increase in total conduction losses due to a longer conduction period of the mainFET's body diode.

Selection of proper timing parameters is of a much higher importance when zero-voltage turn-on of the mainFET is desired. Either, insufficiently or excessively delayed turn-on of the mainFET results in a non-zero-voltage switching transition. The latter results in increased switching losses and several other undesirable phenomenons in hard-switched synchronous converters, like unwanted turn-on of the syncFET and body diode reverse recovery. Therefore, the turn-on delay of the mainFET has to be carefully selected and implemented through the so-called "dead time" between conduction of both transistors in a synchronous converter. However, the required dead time is not an independent parameter for achieving zero-voltage transitions (ZVT). It largely depends on the selected reversed current I_R that dictates the voltage transition period duration T_{res} and the duration of the period T_{zc} before the inductor current i_L changes direction. Therefore, this section focuses on the selection of an adequate reversed current I_R and its influence on timing parameters, all depicted in Fig. 4.3. It also provides guidelines for determining proper dead time duration T_{DT} which would ensure ZVTs of both the main and the synchronous transistor in a conventional bidirectional DC-DC converter. Same as the previous section, this section also focuses on operation in the buck mode. However, the presented findings, models, and conclusions also apply to the boost mode through the aforementioned analogy between both operating modes.

4.2.1 Reversed current considerations

In order to achieve zero-voltage turn-on of the mainFET, the turn-off instant of the syncFET has to be delayed to the point at which the inductor current i_L reaches a certain value in the direction that opposes the primary energy flow in a synchronous converter. This value is designated as the reversed current I_{R}. The selection of its value is of crucial importance since an insufficient I_{R} cannot provide enough charge to completely discharge C_{ossH} and charge C_{ossL} to the voltage V_{A}. Consequently, a zero-voltage turn-on of the mainFET is not achievable. On the other hand, excessive I_R results in an increased inductor current ripple, which leads to higher magnetic core losses, as well as higher turn-off losses of both transistors in the circuit. Although zero-voltage turn-on of the mainFET is maintained in this case, any unnecessary increases in turn-off and magnetic core losses should be avoided. For the aforementioned reasons, a detailed circuit analysis of the main transition period was done.

In the initial phase it is necessary to determine the total charge Q_{tot} required to discharge C_{ossH} and charge C_{ossL} to the level of voltage V_{A}. The entire voltage transition occurs during the main

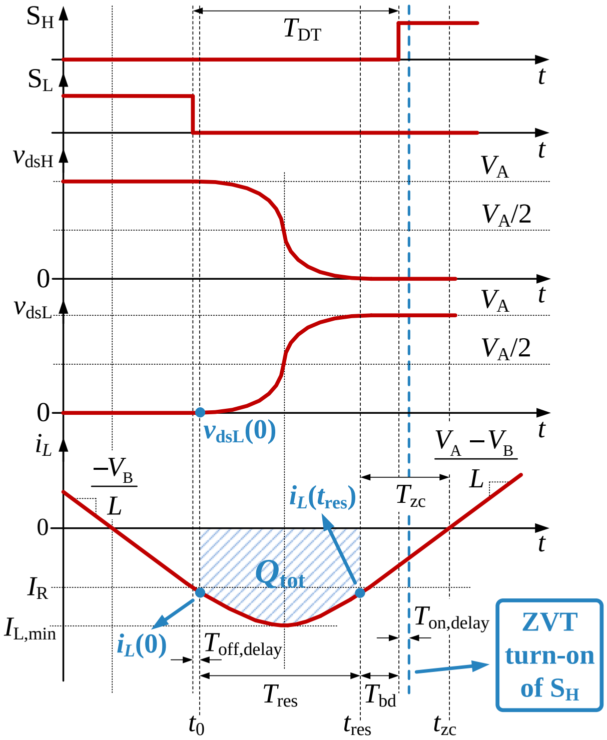


Figure 4.3: Theoretical switching waveforms for the buck mode of a synchronous DC-DC converter operating in DCM - main transition period before turning on the mainFET.

transition period, which corresponds to the equivalent circuit shown in Fig. 4.2(f). Assuming that the output voltage V_{B} in buck mode is constant and that no current is passed through the main channel of the transistor, as well as through its body diode, the equivalent circuit during the main transition period can be simplified to the one shown in Fig. 4.4. Both parasitic output capacitors C_{ossH} and C_{ossL} have nonlinear drain-to-source voltage-dependent capacitance characteristics.

On the basis of the equivalent circuit in Fig. 4.4, the inductor current $i_L(t)$ can be written as

$$i_L(t) = C_{\mathrm{ossL}}(v_{\mathrm{dsL}})\frac{dv_{\mathrm{dsL}}(t)}{dt} - C_{\mathrm{ossH}}(v_{\mathrm{dsH}})\frac{dv_{\mathrm{dsH}}(t)}{dt}, \tag{4.1}$$

where $v_{\mathrm{dsL}}(t)$ and $v_{\mathrm{dsH}}(t)$ are the drain-to-source voltages across transistors $\mathrm{S_L}$ and $\mathrm{S_H}$, respectively, and $C_{\mathrm{ossH}}(v_{\mathrm{dsL}})$ and $C_{\mathrm{ossL}}(v_{\mathrm{dsL}})$ voltage-dependent parasitic output capacitors of transistors S_{L} and S_{H}, respectively. By neglecting parasitic inductances within the power circuit, as is the case in Fig. 4.4, the relation between drain-to-source voltages across each transistor can be written as

$$v_{\mathrm{dsH}}(t) = V_{\mathrm{A}} - v_{\mathrm{dsL}}(t), \tag{4.2}$$

where V_{A} is the converter's input voltage when operating in buck mode. Substituting (4.2) into (4.1) and assuming time-invariant input voltage V_{A}, which will result in $\frac{dV_{\mathrm{A}}}{dt} = 0$, yields

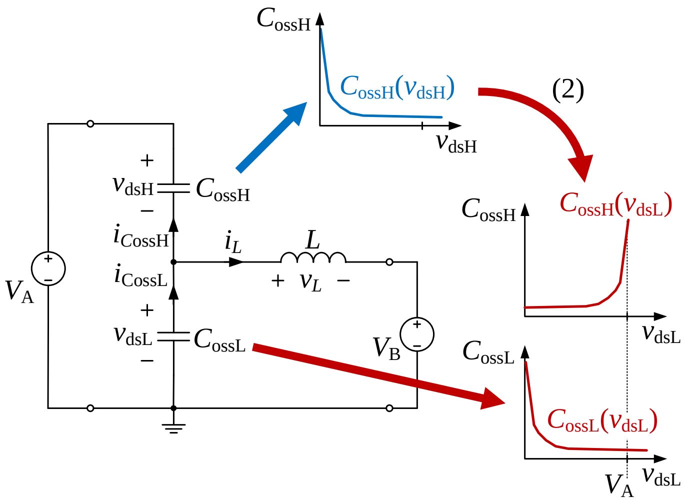

C_{ossH}
$C_{\mathrm{ossH}}(v_{\mathrm{dsH}})$
(2)
v_{dsH}
+
v_{dsH}
C_{ossH}
−
i_{CossH}
i_L
L
i_{CossL}
+ v_L −
V_{A}
+
v_{dsL}
C_{ossL}
−
V_{B}
C_{ossH}
$C_{\mathrm{ossH}}(v_{\mathrm{dsL}})$
v_{dsL}
C_{ossL}
$C_{\mathrm{ossL}}(v_{\mathrm{dsL}})$
V_{A}
v_{dsL}

Figure 4.4: Equivalent circuit of a ZVS bidirectional DC-DC converter at the beginning of dead time, right after the desired reversed current I_R is reached and the syncFET $\mathrm{S_L}$ is turned off.

$$i_L(t) = \left[C_{\mathrm{ossL}}(v_{\mathrm{dsL}}) + C_{\mathrm{ossH}}(v_{\mathrm{dsL}})\right] \frac{dv_{\mathrm{dsL}}(t)}{dt}, \tag{4.3}$$

where $C_{\mathrm{ossH}}(v_{\mathrm{dsL}})$ represents the parasitic output capacitance C_{ossH} as a function of the complementary transistor's drain-to-source voltage v_{dsL}. Such a relation is obtained on the basis of (4.2). The relation between inductor current $i_L(t)$ and electric charge $Q(t)$ can be described by

$$i_L(t) = \frac{dQ(t)}{dt}, \tag{4.4}$$

where $i_L(t)$ is defined as the rate at which charge $Q(t)$ flows through the given surface. A substitution of (4.4) into (4.3) yields

$$\frac{dQ(t)}{dv_{\mathrm{dsL}}(t)} = \left[C_{\mathrm{ossL}}(v_{\mathrm{dsL}}) + C_{\mathrm{ossH}}(v_{\mathrm{dsL}})\right], \tag{4.5}$$

where the right-hand side of the equation demonstrates a parallel connection between both parasitic capacitors $C_{\mathrm{ossH}}||C_{\mathrm{ossL}}$, which is present for the duration of the main transition period. A graphical representation of the paralleled parasitic capacitance $C_{\mathrm{ossH}}||C_{\mathrm{ossL}}$ as a function of the drain-to-source voltage v_{dsL} across the syncFET $\mathrm{S_L}$ is given in Fig. 4.5. The total charge Q_{tot} required to discharge C_{ossH}, charge C_{ossL} to V_{A}, and thus achieve zero-voltage turn-on of the mainFET $\mathrm{S_H}$, is represented by the shaded area under the $C_{\mathrm{ossH}}||C_{\mathrm{ossL}}(v_{\mathrm{dsL}})$ - curve. By isolating expression (4.5) for $Q(t)$ it is possible to calculate the total required charge Q_{tot} as

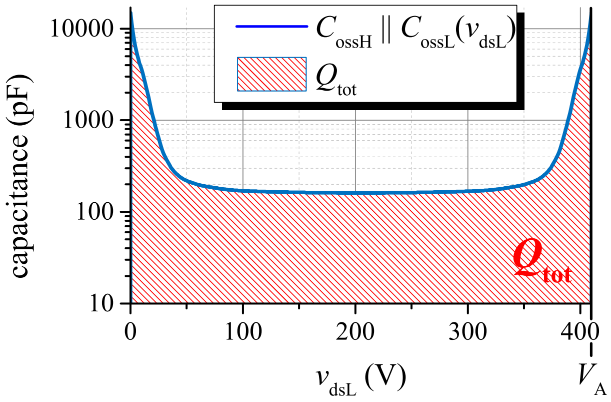


Figure 4.5: Capacitance of the parallel connected parasitic output capacitors C_{ossH} and C_{ossL} as a function of the voltage v_{dsL} during the main transition period of the discussed converter using STP25NM60ND power MOSFETs at a voltage of $V_{\text{A}} = 410\text{V}$.

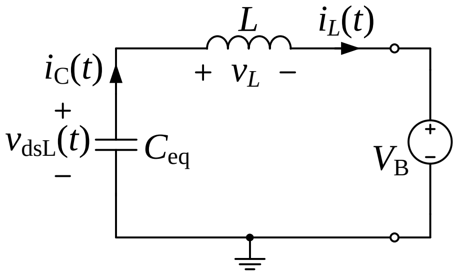


Figure 4.6: Simplified equivalent circuit of the main transition period for the buck operating mode.

$$Q_{\text{tot}} = \int_{0}^{V_{\text{A}}} \left[C_{\text{ossL}}(v_{\text{dsL}}) + C_{\text{ossH}}(v_{\text{dsL}}) \right] dv_{\text{dsL}}. \tag{4.6}$$

On the basis of total charge Q_{tot} at a given V_{A}, the equivalent capacitance C_{eq} of both transistors within the circuit during the main transition period can be obtained as

$$C_{\text{eq}} = \frac{Q_{\text{tot}}}{V_{\text{A}}}. \tag{4.7}$$

Introduction of the equivalent capacitance C_{eq} allows for a further simplification of the circuit in Fig. 4.4. The final simplified circuit of the main transition period is depicted in Fig. 4.6. It represents a driven LC circuit, which will serve as the basis for describing voltage and current transients during the main transition period. The voltage v_{dsL} across C_{eq}, which also represents the voltage across the syncFET S_{L}, can be described by a second-order linear differential equation

$$\frac{d^2 v_{\mathrm{dsL}}(t)}{dt^2} + \frac{1}{LC_{\mathrm{eq}}} v_{\mathrm{dsL}}(t) - \frac{V_{\mathrm{B}}}{LC_{\mathrm{eq}}} = 0, \tag{4.8}$$

while the inductor current i_L can be written as

$$i_L(t) = -C_{\mathrm{eq}} \frac{dv_{\mathrm{dsL}}(t)}{dt}. \tag{4.9}$$

Solving (4.8) for v_{dsL} yields

$$v_{\mathrm{dsL}}(t) = [v_{\mathrm{dsL}}(0) - V_{\mathrm{B}}] \cos(\omega_{\mathrm{o}} t) - \sqrt{\frac{L}{C_{\mathrm{eq}}}} i_L(0) \sin(\omega_{\mathrm{o}} t) + V_{\mathrm{B}}, \tag{4.10}$$

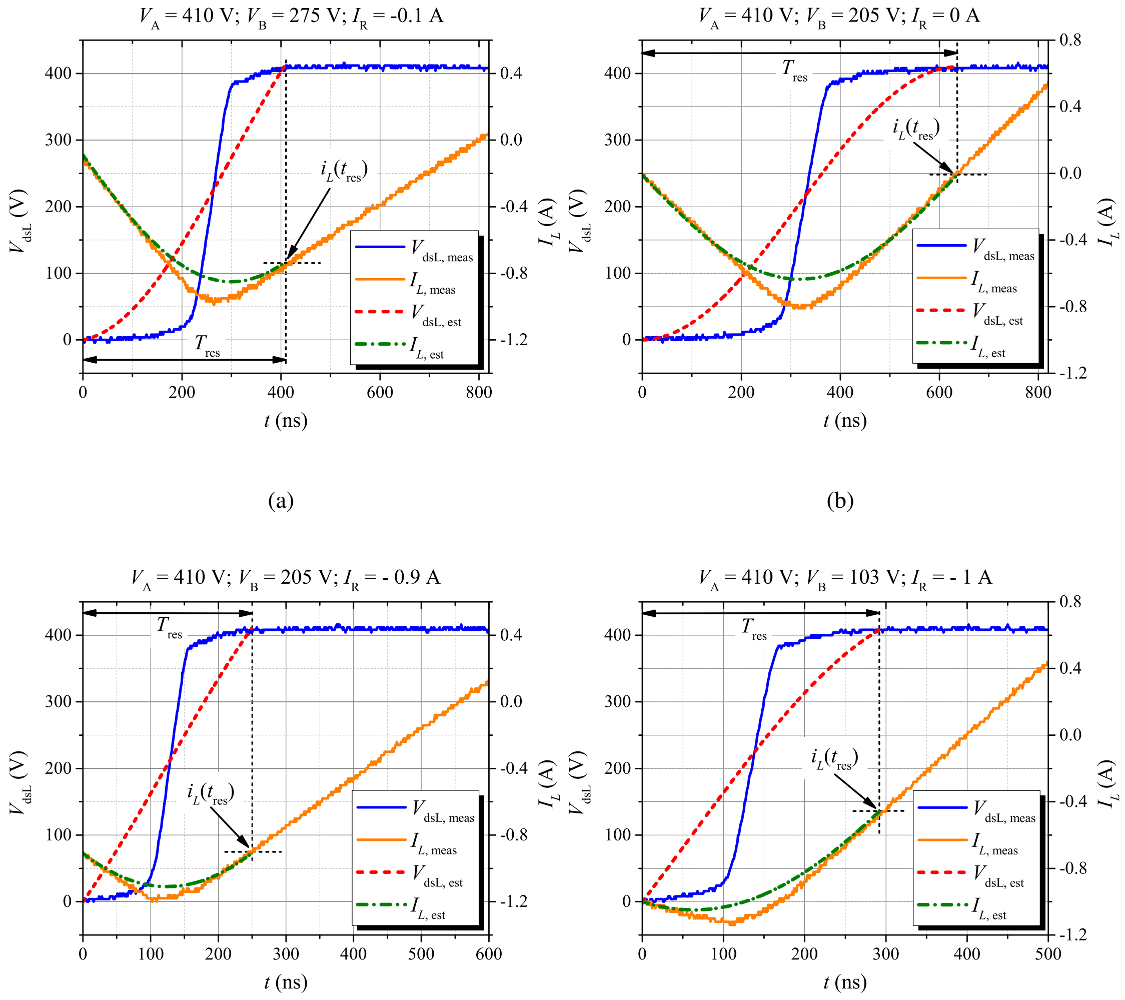
while combining (4.9) and (4.10), and isolating the obtained expression for $i_L(t)$ gives

$$i_L(t) = i_L(0) \cos(\omega_{\mathrm{o}} t) + \sqrt{\frac{L}{C_{\mathrm{eq}}}} \left(v_{\mathrm{dsL}}(0) - V_{\mathrm{B}}\right) \sin(\omega_{\mathrm{o}} t), \tag{4.11}$$

where $v_{\mathrm{dsL}}(0)$ and $i_L(0)$ are the initial values of v_{dsL} and i_L at the beginning of the main transition period, respectively, and ω_{o} the resonant frequency of the driven LC circuit from Fig. 4.6, defined as

$$\omega_{\mathrm{o}} = \sqrt{\frac{1}{LC_{\mathrm{eq}}}}. \tag{4.12}$$

Equations (4.10) and (4.11) represent the analytical model for estimating the duration of the main voltage transition period T_{res} and the inductor current $i_L(t_{\mathrm{res}})$ at the end of the main transition period, where t_{res} designates the time instant at which the main transition period finishes. The validity of the model was verified by experimental measurements carried out on a bidirectional DC-DC converter operating in the buck mode. A comprehensive description of the experimental converter is provided in Section 4.4, while the model verification results are presented in Fig. 4.7. Due to usage of the equivalent capacitance C_{eq}, which represents the mean value of the paralleled parasitic output capacitances $C_{\mathrm{ossH}}||C_{\mathrm{ossL}}$ over the whole range of voltage v_{dsL}, the model proves to be useless for estimating the dv_{dsL}/dt-slope and the inductor current extreme $i_{L,\mathrm{min}}$. However, the model allows for a rather accurate estimation of the voltage transition time T_{res} in which v_{dsH}, according to (4.2), resonates to zero. In addition, the model also proved to be useful for determining the instantaneous value of the inductor current $i_L(t_{\mathrm{res}})$ at the end of the main transition period, i.e. when v_{dsH} reaches zero. Knowing the values of both T_{res} and $i_L(t_{\mathrm{res}})$ is of crucial importance for determining the correct timing parameters, which will be discussed in the following subsection.



(a)

(b)

(c)

(d)

Figure 4.7: Resonant switching transition model verification with experimental switching transition waveforms obtained by operating a bidirectional DC-DC converter in DCM. The parameters of the experimental converter's power circuit are listed in Table 4.1, while $C_{\text{eq}} = 633$ pF and $L = 66$ μH were used as parameters for estimation with (4.10) and (4.11). The legend entries $V_{\text{dsL,meas}}$ and $I_{L,\text{meas}}$ represent the experimentally measured drain-to-source voltage v_{dsL} and inductor current i_L waveforms, respectively, while $V_{\text{dsL,est}}$ and $I_{L,\text{est}}$ represent the same voltage and current waveforms estimated by the proposed analytical model.

On the basis of Fig. 4.7 and (4.2), it can be inferred that v_{dsH} reaches zero in all the presented cases. As L and C_{eq} do not vary significantly depending on the operating conditions, the voltage conversion ratio $V_{\text{B}}/V_{\text{A}}$ and I_{R} determine whether zero-voltage turn-on of the main transistor is achievable at a given operating point. If I_{R} is insufficient for a given $V_{\text{B}}/V_{\text{A}}$, v_{dsH} would only resonate to a value which is greater than zero. Under such conditions, the so-called "valley switching" can be achieved [34]. Although superior to hard switching at full blocking voltage, it still generates a considerable amount of switching losses at higher switching frequencies. For this reason, it is essential to achieve such I_R before turning off the synchronous transistor that would result in a transient in which v_dsH would reach zero and v_dsL the level of voltage V_A.

By differentiating (4.10) in respect to time, isolating the obtained expression for t and adding the periodic nature of the voltage within an undamped LC circuit, it is possible to express the time $t_{V_\mathrm{dsL},\mathrm{ext}}$ at which v_dsL reaches its extremes as

$$t_{V_\mathrm{dsL},\mathrm{ext}} = \frac{1}{\omega_\mathrm{o}} \arctan\left(-\frac{\sqrt{\frac{L}{C_\mathrm{eq}}} i_L(0)}{v_\mathrm{dsL}(0) - V_\mathrm{B}}\right) + kT_\mathrm{rhp}, \tag{4.13}$$

where k is an integer denoting a certain extreme and T_rhp the resonant half-period in which extremes reoccur, defined as $T_\mathrm{rhp} = \frac{\pi}{\omega_\mathrm{o}}$. By neglecting the voltage drop across $R_\mathrm{ds,on}$ of the syncFET $\mathrm{S_L}$ and assuming that the maximum I_R that would cause a resonant voltage transition equals zero, the initial conditions become $v_\mathrm{dsL}(0) = 0$ and $i_L(0) = I_\mathrm{R} \leq 0$. Inserting such initial conditions into (4.13) yields

$$t_{V_\mathrm{dsL},\mathrm{max}} = \frac{1}{\omega_\mathrm{o}} \arctan\left(\frac{\sqrt{\frac{L}{C_\mathrm{eq}}} I_\mathrm{R}}{V_\mathrm{B}}\right) + T_\mathrm{rhp}, \tag{4.14}$$

where $t_{V_\mathrm{dsL},\mathrm{max}}$ represents the time at which v_dsL reaches its first maximum ($k = 1$). On the basis of (4.14), the fundamental criteria for achieving ZVS can be defined as

$$v_\mathrm{dsL}(t_{V_\mathrm{dsL},\mathrm{max}}) \geq V_\mathrm{A}, \tag{4.15}$$

where $v_\mathrm{dsL}(t_{V_\mathrm{dsL},\mathrm{max}})$ represents the maximum voltage $v_\mathrm{dsL}(t)$ that can be attained within the resonant circuit in Fig. 4.6. By substituting (4.12), (4.14), and (4.15) into (4.10), the minimum required reversed current $I_\mathrm{R,min}$ for achieving ZVTs can be written as

$$I_{R,\mathrm{min}} = -\sqrt{\frac{C_\mathrm{eq} V_\mathrm{A}(V_\mathrm{A} - 2V_\mathrm{B})}{L}}. \tag{4.16}$$

The minimum required $I_\mathrm{R,min}$ characteristic for the experimental synchronous bidirectional DC-DC converter is presented in Fig. 4.8. It must be noted that $I_\mathrm{R,min}$ does not represent the optimal reversed current magnitude, since it causes rather long switching transition durations T_res, which are not acceptable in most cases. The procedure for determining an adequate reversed current magnitude that will result in switching transitions of desirable duration is described in Section 4.3.

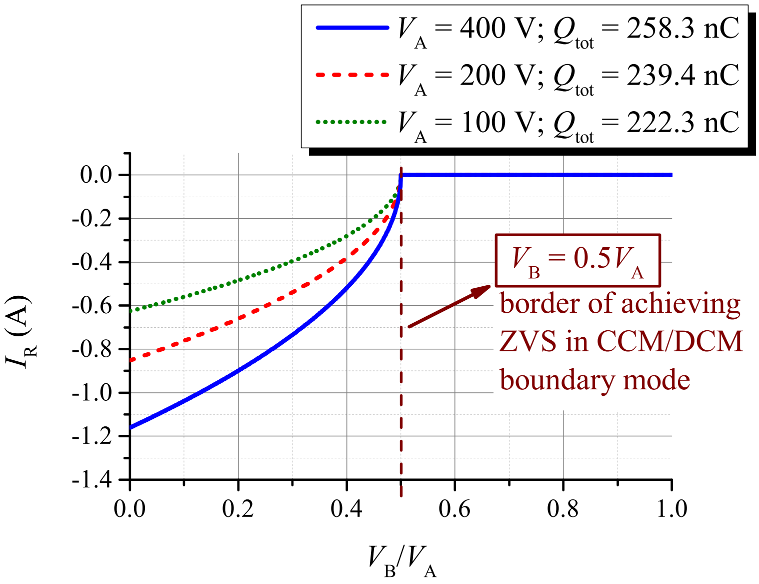


Figure 4.8: Minimum required reversed current $I_{\mathrm{R,min}}$ for achieving zero-voltage turn-on of the mainFET at different voltage conversion ratios for a synchronous bidirectional DC-DC converter utilizing STP25NM60ND power MOSFETs and an inductor with inductance $L = 66\ \mu\mathrm{H}$.

Up to this point it was assumed that both L and C_{eq} are fixed and that the ZVS capability is solely a function of I_{R} and $V_{\mathrm{B}}/V_{\mathrm{A}}$. When waiving this assumption, the conditions for achieving ZVS become much more complex. The main parameters of the equivalent circuit in Fig. 4.6, L and C_{eq}, govern the behavior of $v_{\mathrm{dsL}}(t)$ and $i_{\mathrm{L}}(t)$ during the main transition period and thus influence the magnitude of the minimum required I_{R} for achieving ZVTs. In order to avoid the demand for a very large I_{R} at certain operating points (when $V_{\mathrm{B}} < 0.5V_{\mathrm{A}}$), L and C_{eq} have to be carefully selected. The more inflexible of them is C_{eq}, which is given by the selection of the power transistors. On the other hand, there is the power inductor whose inductance L can be adapted with the aim of reducing the required I_{R} and setting the desired duration of the main transition period. By isolating (4.16) for L, an expression for the minimum required inductance L_{min} for achieving ZVTs at a desirable I_{R} is obtained as

$$L_{\mathrm{min}} = \frac{C_{\mathrm{eq}} V_{\mathrm{A}} (V_{\mathrm{A}} - 2V_{\mathrm{B}})}{{I_{\mathrm{R}}}^2}. \tag{4.17}$$

In terms of ZVT capability, a minimum value of inductance L_{min} is required only in cases when $V_{\mathrm{B}}/V_{\mathrm{A}} < 0.5$. For the remainder of possible voltage conversion ratios ($V_{\mathrm{B}}/V_{\mathrm{A}} \geq 0.5$), ZVTs can be achieved with any non-positive I_{R}, independent of the power inductor's inductance L. Nonetheless, the inductance L greatly influences the duration of the main transition period directly, as it is evident from (4.10), and indirectly through the resonant frequency of the circuit in Fig. 4.6.

By taking into account the inequality in (4.15), either (4.16) or (4.17) can be transformed into

$$L{I_{\mathrm{R}}}^2 \geq C_{\mathrm{eq}} V_{\mathrm{A}} (V_{\mathrm{A}} - 2V_{\mathrm{B}}), \tag{4.18}$$

which represents the ZVS capability criteria. The latter indicates that ZVS control design is subject to finding the most suitable combination of L and I_{R}, which will ensure ZVS with the existing C_{eq}, at a certain voltage conversion ratio $V_{\mathrm{B}}/V_{\mathrm{A}}$. The presented ZVS capability criteria (4.18) deviates from its generally accepted version reported in [59, 61], which is rather conservative and does not consider the influence of the voltage conversion ratio.

4.2.2 Dead time considerations

Once a certain larger than the minimum required amplitude of the reversed current I_{R} is selected, it is necessary to properly determine the timing parameters for achieving zero-voltage turn-on of the mainFET. The more significant delays and intervals that are present during such switching transition, when the converter operates in DCM, are depicted and labeled in Fig. 4.3. Among them, the duration of the dead time T_{DT} between conduction of both transistors is the main object of interest when implementing the control. It must be sufficiently long in order to provide enough charge (shaded area labeled with Q_{tot}) for a complete discharge of the mainFET's parasitic output capacitor before the turn-on instant of the mainFET. On the other hand T_{DT} must not be excessive, since a turn-on of the mainFET after i_L crosses zero results in re-charging of its already discharged parasitic capacitor. Both cases of improperly selected T_{DT} lead to a loss of ZVS. On the basis of the described limitations it is possible to define the minimum $T_{\mathrm{DT,min}}$ and maximum $T_{\mathrm{DT,max}}$ allowed dead time durations as

$$T_{\mathrm{DT,min}} = T_{\mathrm{off,delay}} + T_{\mathrm{res}} - T_{\mathrm{on,delay}}, \tag{4.19}$$

$$T_{\mathrm{DT,max}} = T_{\mathrm{off,delay}} + T_{\mathrm{res}} + T_{\mathrm{zc,min}} - T_{\mathrm{on,delay}}, \tag{4.20}$$

where $T_{\mathrm{off,delay}}$ is the turn-off delay of the syncFET, $T_{\mathrm{on,delay}}$ the turn-on delay of the mainFET, T_{res} the duration of the voltage transition period, and $T_{\mathrm{zc,min}}$ the minimum duration of the period before i_L crosses zero.

The delays $T_{\mathrm{off,delay}}$ and $T_{\mathrm{on,delay}}$ mainly depend on the gate driving circuit and parasitic input capacitances of the used transistors. Their detailed analysis exceeds the scope of this work. However, within the narrow range of currents in the vicinity of the mainFET's turn-on in DCM,

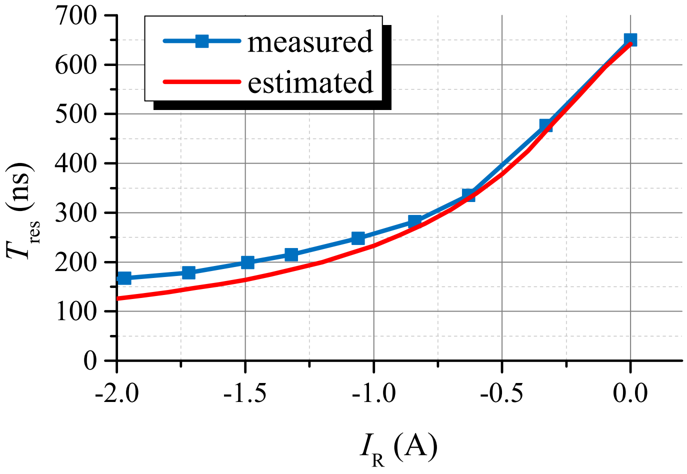


Figure 4.9: Experimental verification of the estimated voltage transition time T_{res} for $V_{\mathrm{A}} = 400$ V and $V_{\mathrm{B}} = 200$ V. The experimental synchronous bidirectional DC-DC converter uses STP25NM60ND power MOSFETs and an inductor with inductance $L = 66\ \mu$H.

both delays can be measured for the desired voltage level and assumed to be independent of i_L. As already discussed in the previous subsection, the duration of T_{res} can be estimated on the basis of (4.10). The accuracy of the T_{res} estimation was verified by experimental measurements. The results shown in Fig. 4.9 demonstrate a good match between the measured and estimated transition times, especially for lower values of I_{R}. It is also evident from this figure that the selection of I_{R} dramatically affects the transition time, since a higher current provides more charge over a given period.

As soon as the voltage transition period finishes, the body diode of the mainFET takes over the current and the interval T_{bd} begins, as it is evident in Fig. 4.3. For minimizing the conduction losses, T_{bd} should be as short as possible [103]. The interval T_{bd} finishes at the instant at which $\mathrm{S_H}$ turns on and the entire current is passed through the main channel of the transistor. This must happen before i_L crosses zero.

The minimum duration of the interval labeled T_{zc} in Fig. 4.3 that spans from the end of the voltage transition period marked with t_{res} to the point t_{zc} at which i_L crosses zero, can be calculated as

$$T_{\mathrm{zc,min}} = L\frac{i_L(t_{\mathrm{res}})}{V_{\mathrm{A}}\left(1 - \min(D_{\mathrm{buck}}, D_{\mathrm{boost}})\right)}, \tag{4.21}$$

where $i_L(t_{\mathrm{res}})$ is the inductor current at the end of the voltage transition period, D_{buck} the duty cycle in buck mode given as $D_{\mathrm{buck}} = V_{\mathrm{B}}/V_{\mathrm{A}}$ and D_{boost} the duty cycle in boost mode given as $D_{\mathrm{boost}} = 1 - V_{\mathrm{B}}/V_{\mathrm{A}}$. The instantaneous value of the inductor current $i_L(t_{\mathrm{res}})$ can be estimated from (4.11). By knowing all the parameters involved in (4.19) and (4.20), it is possible to achieve a reliable zero-voltage turn-on of the mainFET at any sufficient or excessive value of I_R (see Fig. 4.8).

4.3 ZVS control design

A nonisolated synchronous DC-DC converter operated in DCM inside the expected range of the voltage conversion ratios, can achieve ZVS with a constant, predetermined, reversed current I_R and dead time T_DT, independently of the current load conditions. In order to ensure such operation, the syncFET has to be turned off at the chosen reversed current I_R in each switching cycle. As demonstrated in Fig. 4.9, the higher the reversed current I_R the shorter the transition time T_res. By selecting a somewhat higher than the minimum required amplitude of I_R, it is possible to achieve voltage transitions with negligible durations in respect to the operating switching period T_sw. Consequently an ideal triangular shape of the inductor current i_L can be assumed with a minimum value of $I_{L,\mathrm{min}} \approx I_\mathrm{R}$. Given these assumptions, the inductor current ripple Δi_L can be written as

$$\Delta i_L = \frac{V_\mathrm{A}(1-D)DT_\mathrm{sw}}{2L}, \tag{4.22}$$

where D is the duty cycle in either buck or boost operating modes. In order to turn-off the synchronous transistor $\mathrm{S_H}$ at the desired reversed current I_R, the inductor current ripple Δi_L must equal

$$\Delta i_L = |I_{L,\mathrm{avg}}| - I_\mathrm{R}, \tag{4.23}$$

where $I_{L,\mathrm{avg}}$ is the average inductor current that has to be measured. As $I_{L,\mathrm{avg}}$ is positive for operation in the buck mode and negative when operating in the boost mode, its absolute value was used to satisfy the conditions for both operating modes. Substituting (4.23) into (4.22) and isolating the expression for T_sw yields

$$T_\mathrm{sw} = 2L\frac{V_\mathrm{A}}{(V_\mathrm{A}-V_\mathrm{B})\,V_\mathrm{B}}\left(|I_{L,\mathrm{avg}}| - I_\mathrm{R}\right), \tag{4.24}$$

which represents the equation for calculating the switching period T_sw that will ensure ZVS of a bidirectional DC-DC converter at a certain operating point. For maintaining ZVS throughout the entire operating range, under varying load conditions, the switching period T_sw has to be continuously adapted according to (4.24).

The procedure of the ZVS control design can be summarized by the following points:

1) determination of the maximum voltage $V_{\mathrm{A,max}}$ and the desirable switching frequency $f_{\mathrm{sw,des}}$ at the nominal power P_{nom};

2) determination of the maximum allowed switching frequency $f_{\mathrm{sw,max}}$ under light load conditions, which forms the criteria for the maximum allowed duration of the main transition period $T_{\mathrm{res,max}}$;

3) selection of the most suitable power transistors;

4) calculation of the total gate charge Q_{tot} and equivalent capacitance C_{eq} at $V_{\mathrm{A,max}}$ for the selected transistors, according to (4.6) and (4.7), respectively;

5) determination of the worst case voltage conversion ratio $V_{\mathrm{B}}/V_{\mathrm{A}}$ (i.e. the minimum $V_{\mathrm{B}}/V_{\mathrm{A}}$ which demands the highest I_{R} and L for achieving ZVTs);

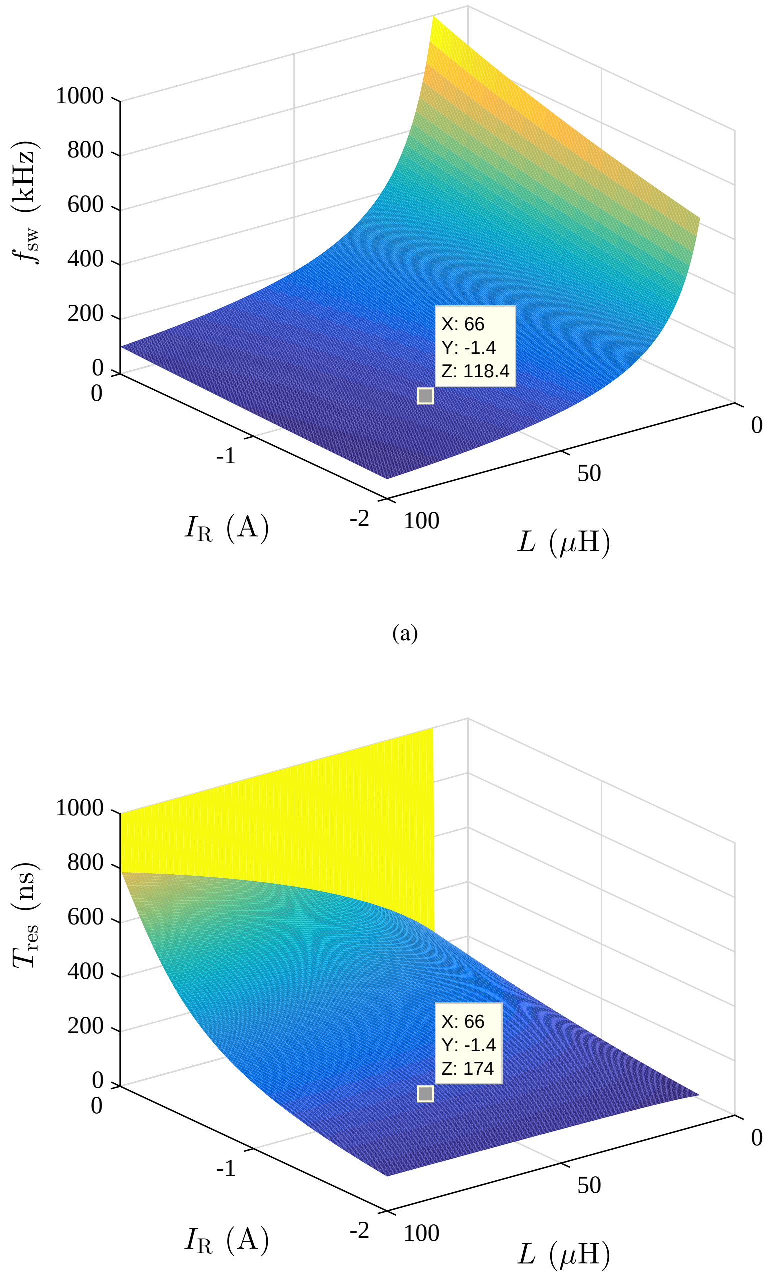
6) construction of the ZVS control design surfaces depicted in Fig. 4.10, where $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$ in Fig. 4.10(a) is obtained on the basis of (4.24) and the introduction of operating switching frequency $f_{\mathrm{sw}} = 1/T_{\mathrm{sw}}$, while $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$ in Fig. 4.10(b) is obtained on the basis of (4.10);

7) finding a combination of L and I_{R} that fulfills the criteria $T_{\mathrm{res}} \leq T_{\mathrm{res,max}}$ and $f_{\mathrm{sw}} \approx f_{\mathrm{sw,des}}$;

8) determination of a proper dead time duration T_{DT} according to (4.19) and (4.20).

In the case of designing the ZVS control for a converter with predetermined power components, which cannot be modified or replaced, the procedure becomes essentially simpler. In addition to omitting point 3), the design surfaces under point 6) are transformed into curves at the given value of L. Thus, the switching frequency f_{sw} at the nominal power and the main transition period duration T_{res} can be set by solely adjusting the magnitude of I_{R}.

From the ZVS control design surfaces in Fig. 4.10, an inductance of $L = 66\ \mu\mathrm{H}$ and reversed current of $I_{\mathrm{R}} = -1.4\ \mathrm{A}$ were selected for achieving ZVTs with $T_{\mathrm{res,max}} \leq 175\ \mathrm{ns}$ and $f_{\mathrm{sw}}(P_{\mathrm{nom}}) \approx 115\ \mathrm{kHz}$ at the chosen design parameters. One of the main control objectives is to ensure operation with a switching frequency obtained from (4.24) throughout the entire operating range of the converter. In this way, identical, predetermined initial conditions for resonant voltage transitions will be achieved in each switching cycle. Operation with a switching frequency higher than the one calculated from (4.24) must be avoided, as this would decrease I_{R}, increase T_{res}, and in extreme cases lead to a loss of ZVS. Less critical but also undesirable is the operation with a switching frequency lower than the one specified by (4.24). The resulting negative effect is the



(a)

(b)

Figure 4.10: ZVS control design surfaces (a) $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$ and (b) $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$ for the nominal output power of $P_{\mathrm{nom}} = 1\ \mathrm{kW}$, maximum voltage $V_{\mathrm{A,max}} = 400\ \mathrm{V}$, voltage conversion ratio $V_{\mathrm{B}}/V_{\mathrm{A}} = 0.5$, and power MOSFETs with $Q_{\mathrm{tot}} = 258.3\ \mathrm{nC}$ and $C_{\mathrm{eq}} = 646\ \mathrm{pF}$ at $V_{\mathrm{A,max}}$.

increased current ripple which increases the core losses in magnetic components, the turn-off losses of both transistors in the circuit, as well as total conduction losses due to a higher rms current.

A PI-based cascaded control scheme has been designed for controlling the output voltages V_A in boost mode and V_B in buck mode. Its simplified block diagram is shown in Fig. 4.11. An external output voltage control loop is used in cascade with an internal control loop for controlling the mean value of the inductor current. In the case where current control is required, the external voltage control loop can be simply disabled, and inductor current reference $I_\mathrm{L,ref}$ has to be applied instead of the output voltage reference $V_\mathrm{o,ref}$. Since the system to be controlled is nonlinear, feedback linearization was used for compensating the nonlinearities in the averaged model of the converter, as evident from Fig. 4.11. The parameters of the PI controllers were selected such that the internal current control loop achieved a bandwidth of 5 kHz and the external voltage control loop a bandwidth of 500 Hz in both buck and boost operating modes. The inductor current's control-to-output transfer function parameters, as well as the current controller's linearization algorithm, are independent of the operating mode. On the other hand, the output voltage's transfer function parameters differ in each operating mode, due to a deviation between the estimated load resistances R at the nominal output power in buck and boost modes. Another cause for different output voltage dynamics in each operating mode appears in the case where the capacitances of C_A and C_B do not match. As a consequence, the parameters of the external control loop have to be adapted during operation in accordance with the active operating mode, in order to ensure the desired bandwidth of the controller. In addition to the controller parameters, the linearization algorithm for voltage control also has to be selected in accordance with the active operating mode, as evident from Fig. 4.11. The just-described part of the control scheme ensures the desired output voltage in steady state as well as during abrupt load changes by varying the reference duty cycle D. The remainder of the control scheme is used for maintaining ZVS throughout the entire operating range of the converter, by adapting the switching frequency according to (4.24). In order to avoid unwanted oscillations in the calculated T_sw due to the noise in the measured signals and for limiting the dynamics of the switching frequency variation, a low-pass filter (LPF) with a cutoff frequency of 50 Hz is applied, as depicted in Fig. 4.11. Although it is desirable to maintain the switching frequency as constant as possible during steady state operation, the cutoff frequency of the LPF should not be set too low in order to prevent loss of ZVS during load transients. The proposed control system can be entirely implemented within a DSC and only requires measurements of the mean values of inductor current $I_{L,\mathrm{avg}}$, and voltages V_A and V_B.

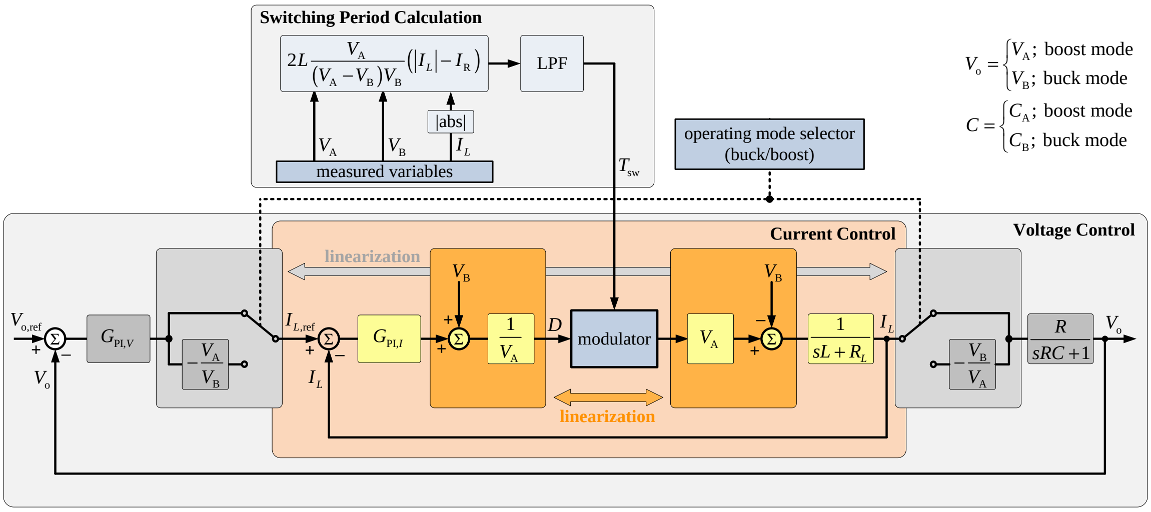

Switching Period Calculation
$2L\frac{V_\mathrm{A}}{(V_\mathrm{A}-V_\mathrm{B})V_\mathrm{B}}(|I_L|-I_\mathrm{R})$
LPF
|abs|
V_A
V_B
I_L
measured variables
T_sw
operating mode selector (buck/boost)
$V_\mathrm{o}=\begin{cases}V_\mathrm{A}; \text{ boost mode}\\ V_\mathrm{B}; \text{ buck mode}\end{cases}$
$C=\begin{cases}C_\mathrm{A}; \text{ boost mode}\\ C_\mathrm{B}; \text{ buck mode}\end{cases}$
Current Control
Voltage Control
linearization
$V_\mathrm{o,ref}$
V_o
$G_\mathrm{PI,V}$
$I_{L,\mathrm{ref}}$
I_L
$G_\mathrm{PI,I}$
$\frac{1}{V_\mathrm{A}}$
D
modulator
V_A
$\frac{1}{sL+R_L}$
$\frac{R}{sRC+1}$
linearization

Figure 4.11: Control scheme for controlling the output voltage in the active operating mode and ensuring ZVS by adapting the switching frequency.

4.4 Experimental verification

The performance of the proposed DCM-based ZVS control approach was tested and evaluated on a conventional 1-kW bidirectional DC-DC converter presented in Fig. 4.12. For the purpose of performance evaluation, this same converter was also tested in CCM operation. The latter represents the most conventional and widely used operating mode. The main advantage of CCM is the constant switching frequency, which simplifies the control design and implementation. On the other hand, its utilization results in hard-switching within the major part of the discussed converter's operating range. The power circuit components of the experimental converter are listed in Table 4.1. While the power inductor's inductance L, reversed current I_R, and dead time duration T_DT were selected as described in Section 4.3, the capacitances of C_A and C_B were selected according to the guidelines provided in [6, 104]. Since operation in CCM requires a much higher value of inductance than operation in DCM at a comparable switching frequency, two different inductors were designed in order to test the converter in both operating modes. The inductor used in the tests with constant switching frequency and operation in CCM under hard-switching conditions (HSW) is designated as HSW inductor, while the designator ZVS inductor corresponds to the one used in tests with the proposed DCM-based ZVS with variable switching frequency. Both inductors were built with Magnetics' High Flux toroidal cores [105]. One of the main design goals when designing the ZVS inductor was to achieve as much load-independent inductance as possible within the expected range of inductor current i_L. Although this design goal negatively affects the size of the inductor to a certain extent, it adds to the simplicity of the control algorithm by avoiding the need for including

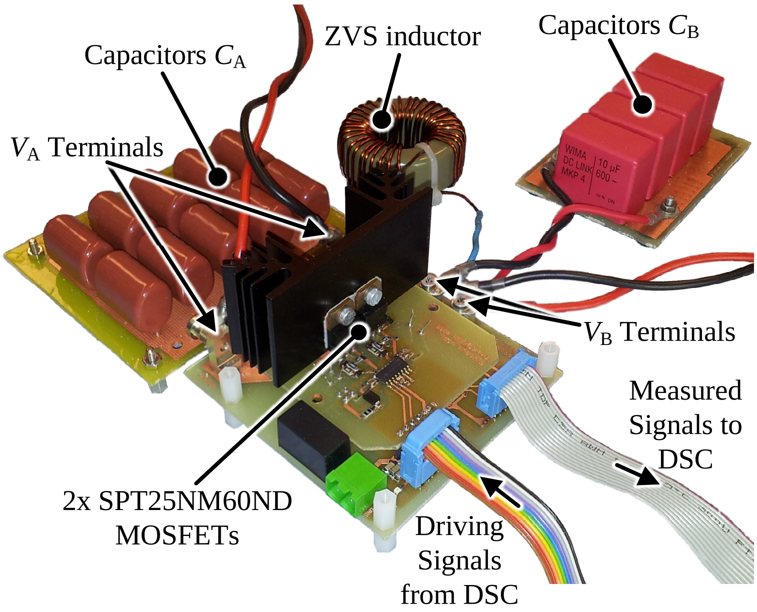

Capacitors C_A
ZVS inductor
Capacitors C_B
V_A Terminals
V_B Terminals
Measured Signals to DSC
2x SPT25NM60ND MOSFETs
Driving Signals from DSC

Figure 4.12: Experimental prototype of a conventional nonisolated bidirectional DC-DC converter.

Table 4.1: Main components and parameters of the experimental bidirectional DC-DC converter

	Symbol	Description	Value
Power Circuit Components	S_H, S_L	STMicroelectronics STP25NM60ND	600 V / 21 A
	L	HSW inductor: Magnetics, High Flux, C058438A2, 48 turns, AWG17	660 μH
		ZVS inductor: Magnetics, High Flux, C058440A2, 33 turns, AWG17	66 μH
	C_A	High-voltage side capacitor bank: 10x Panasonic, ECW-FA2J225J, 2.2μF, 630V 18x TDK, CKG57NX7T2J105M500JH, 1μF, 630V	40 μF
	C_B	Low-voltage side capacitor bank: 4x WIMA, DCP4I051006GD2KYSD, 10μF, 600V	40 μF
ZVS Control Parameters	I_R	Reversed current	-1.4 A
	T_{DT}	Dead time duration	215 ns

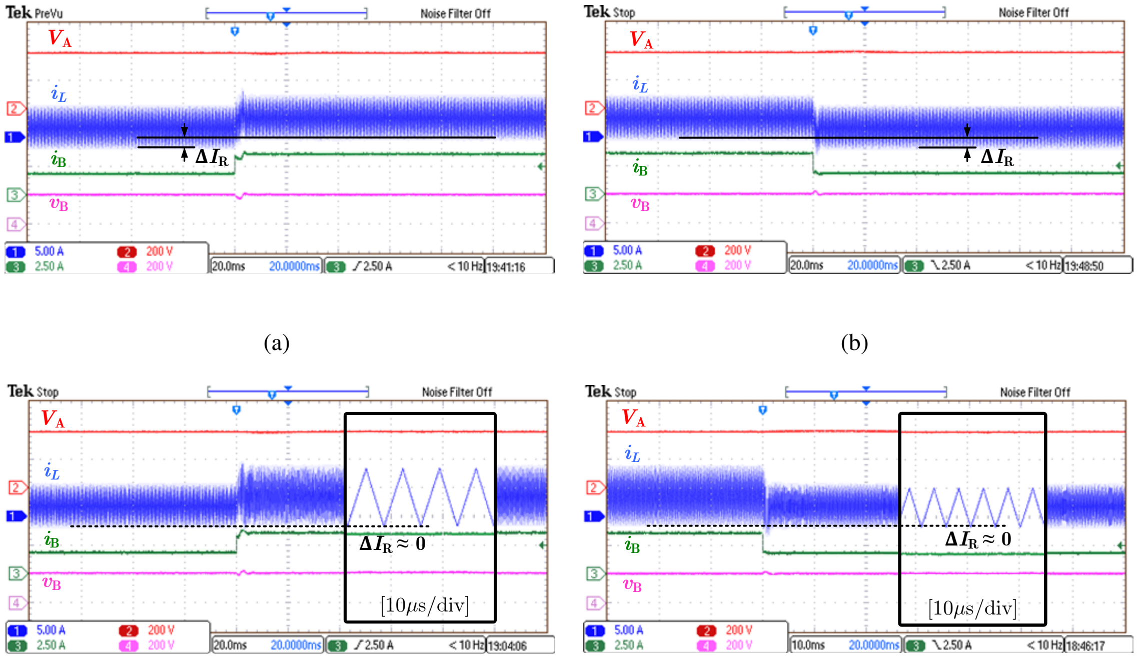
the load-dependent nonlinearity of inductance into (4.24).

The proposed control scheme shown in Fig. 4.11 was implemented into Texas Instruments' TMS320C28343 DSC. While the code is running, an interrupt is called upon in every second switching cycle. The start of conversion in analog-to-digital converters (ADCs) for acquiring values of the measured variables V_{A}, V_{B} and $I_{L,\mathrm{avg}}$ is synchronized with the beginning of the interrupt. As soon as new values are acquired from ADCs, a new value of switching period T_{sw} is calculated and passed through a digital LPF with a cutoff frequency of 50 Hz. In the remainder of the interrupt, a new value of the duty cycle D is calculated through the presented cascaded control scheme using PI controllers. Both outputs of the proposed control scheme, T_{sw} and D, are updated after each interrupt, i.e. in every second switching cycle.

The voltage and current waveforms shown in Fig.4.13 demonstrate the converter's response to an abrupt load change. The converter was operating in buck mode with an input voltage of $V_{\mathrm{A}} = 400$ V, while the output voltage was controlled at $V_{\mathrm{B}} = 200$ V. Two series of tests were carried out, in order to obtain a comparison between the converter operating in DCM with a constant and the proposed variable switching frequency. Both cases used the ZVS inductor and the same control scheme presented in Fig. 4.11. The only difference in the tests with constant switching frequency was that the desired switching frequency calculation was eliminated from the algorithm and set to $f_{\mathrm{sw}} = 195$ kHz. The results of the tests under constant switching frequency conditions, shown in Figs. 4.13(a) and 4.13(b), demonstrate both unwanted effects of such operation. The reduction of I_{R} after the load current increases, which may result in a permanent loss of ZVS, is evident from Fig. 4.13(a). On the other hand, an excessive circulating current after the load current decreases is evident from Fig. 4.13(b). In contrast, operating with the proposed variable switching frequency, as shown in Figs. 4.13(c) and 4.13(d), ensures a constant reversed current magnitude I_{R} and thus a minimum required inductor current ripple at any operating point of the converter. In this way, a safe, reliable and efficient operation with permanent ZVS is maintained throughout the entire operating range of the converter.

4.4.1 Zero-voltage switching verification

The importance of selecting a proper dead time duration T_{DT} for achieving ZVS is evident from Fig. 4.14. The turn-on instant of the MainFET in Fig. 4.14(a) occurs within the interval T_{zc}, which is achieved due to selecting a dead time duration T_{DT} within the limits specified by (4.19) and (4.20). Such turn-on of the mainFET results in a perfect ZVT with negligible losses, without any spikes or oscillations in voltage and current. In contrast, the switching transition in Fig. 4.14(b) occurs at only slightly reduced v_{dsL} due to an insufficient T_{DT}. A considerable spike in i_{dsL} can be observed, which significantly increases the switching energy and indicates a hard-switching transition. An excessively delayed turn-on of the mainFET in Fig. 4.14(c), which occurs after i_L



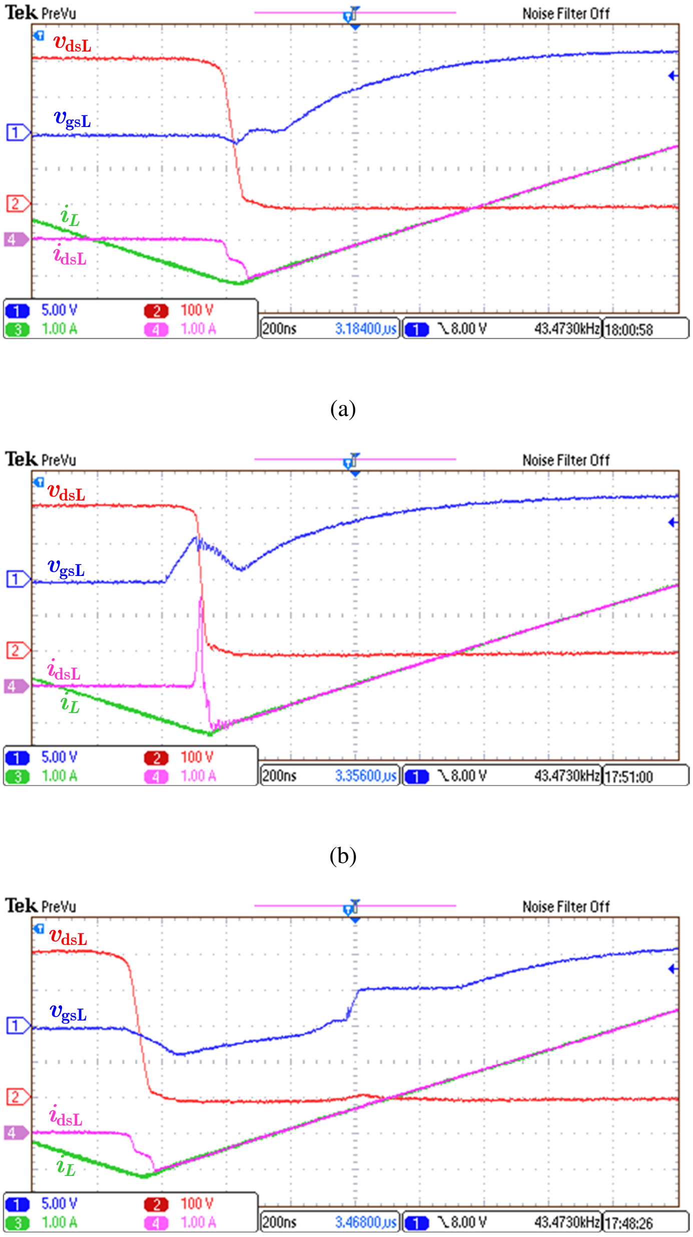
(a) (b)

(c) (d)

Figure 4.13: Load change test results for the converter operating in buck mode with output voltage control. (a) Decrease in the load resistance $R = 114\ \Omega \rightarrow 58\ \Omega$ with constant switching frequency. (b) Increase in the load resistance $R = 58\ \Omega \rightarrow 114\ \Omega$ with constant switching frequency. (c) Decrease in the load resistance $R = 114\ \Omega \rightarrow 58\ \Omega$ with variable switching frequency. (d) Increase in the load resistance $R = 58\ \Omega \rightarrow 114\ \Omega$ with variable switching frequency.

changes its direction, results in re-charging of the parasitic output capacitor C_{ossL} and consequently in a non-zero voltage switching transition. The latter is indicated by the Miller plateau that appears in v_{gsL}.

A proof for maintaining ZVS with the proposed load-adaptable switching frequency and properly selected reversed current I_{R} and timing parameter T_{DT} is given in Fig. 4.15. The switching waveforms were recorded for the tested converter operating in boost mode at 20%, 53% and 100% of the nominal output power, respectively. The boost operating mode was chosen since the mainFET's source terminal is ground-referenced in the boost mode and thus allows for easier access with the probes for measuring the mainFET's gate-to-source voltage v_{gs} and drain-to-source current i_{ds}.



(a)

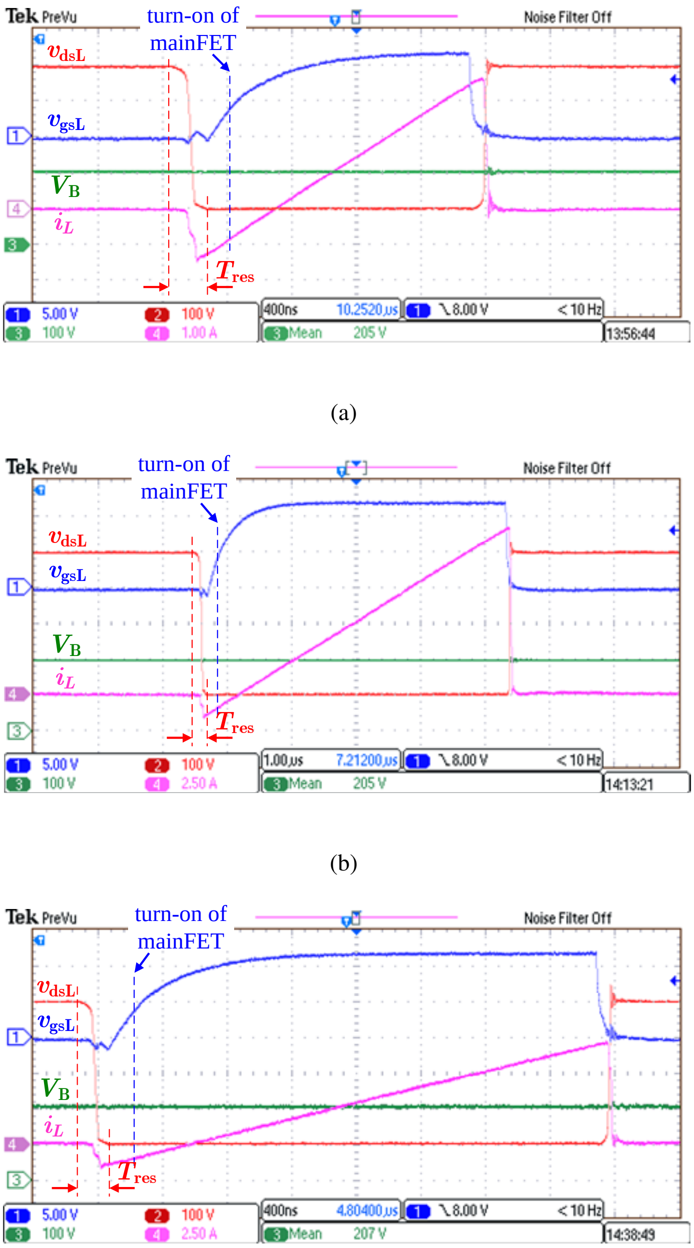
(b)

(c)

Figure 4.14: Experimental waveforms for the DCM-ZVS bidirectional DC-DC converter in boost mode with different dead time durations: (a) proper dead time duration of $T_{\rm DT} = 215$ ns, selected according to the criteria provided by (4.19) and (4.20), (b) excessive dead time duration of $T_{\rm DT} = 750$ ns, and (c) insufficient dead time duration of $T_{\rm DT} = 25$ ns. All the depicted waveforms were obtained with a reversed current of $I_{\rm R} = -1.4$ A.

4.4.2 Power conversion efficiency analysis

The final experimental testing phase focused on power conversion efficiency analysis. The efficiency of the bidirectional DC-DC converter operating with the proposed DCM-based ZVS control



(a)

(b)

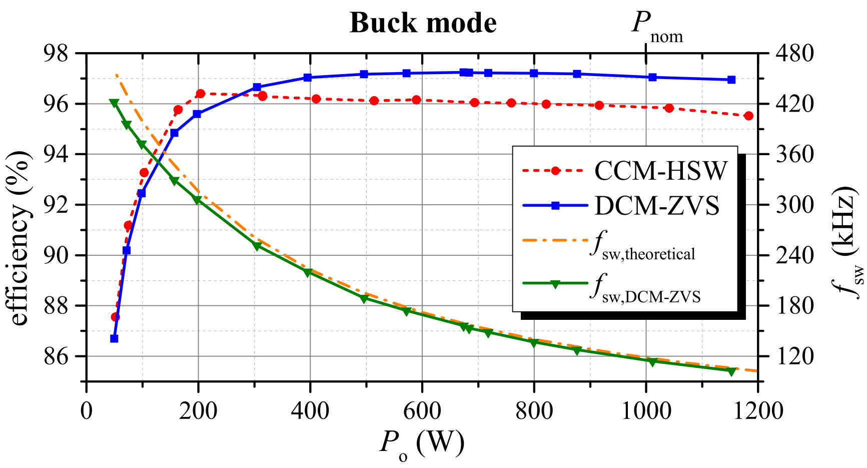
(c)

Figure 4.15: DCM-ZVS waveforms of the bidirectional DC-DC converter in boost mode at output powers of: (a) $P_{\mathrm{o}} = 200$ W, (b) $P_{\mathrm{o}} = 530$ W, and (c) $P_{\mathrm{o}} = 1000$ W. All the depicted waveforms were obtained with a reversed current of $I_{\mathrm{R}} = -1.4$ A and a dead time duration of $T_{\mathrm{DT}} = 215$ ns.

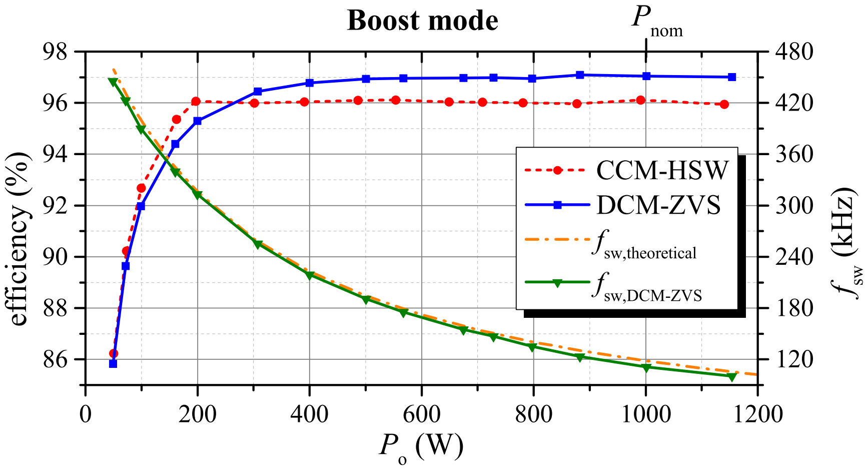
(DCM-ZVS) was measured using a Norma D 6100 Wide Band Power Analyzer in both buck and boost operating modes. For the sake of comparison and performance evaluation of the proposed control approach, the efficiency was also measured for operation in the CCM with HSW (CCM-HSW) at a constant switching frequency of $f_{\mathrm{sw}} = 50$ kHz. The measurements were carried out at voltage levels of $V_{\mathrm{A}} = 400$ V and $V_{\mathrm{B}} = 200$ V. The measured efficiencies for both tested operating modes are shown in Fig. 4.16.It must be noted that the control stage and driving stage losses are not included in the measured efficiencies. A good match between the theoretically calculated and experimentally measured switching frequency in DCM-ZVS can be observed in both figures. Such results confirm adequate performance of the ZVS control and indicate a sufficiently accurate, high bandwidth current measurement. Accurate information about the mean value of the inductor current I_L is of crucial importance due to its role in the switching period calculation (4.24). However, there is a slightly bigger mismatch between the theoretical $f_{\mathrm{sw,theoretical}}$ and experimentally measured switching frequency $f_{\mathrm{sw,DCM-ZVS}}$ in buck operating mode under light load conditions. Since it is not present to such an extent in the boost mode, this mismatch can be attributed to asymmetries and nonlinearities in the current sensing circuit, which emerge when the measured signal is in the vicinity of zero.

It is evident from Fig. 4.16 that a close-to-peak efficiency of about 97% in DCM-ZVS was maintained over a wide operating range, from 50% up to almost 120% of the nominal output power P_{nom}. Within this range, the efficiency of CCM-HSW was approximately 1% lower. However, the efficiency of CCM-HSW exceeded the efficiency of DCM-ZVS at about 30% of P_{nom}. At this point CCM-HSW turned into DCM, in which ZVS may be achieved at a significantly lower switching frequency. As an example, at 20% of P_{nom}, where the efficiency deviation in favor of CCM-HSW was the highest (less than 1% in all observed operating points), the operating switching frequency in DCM-ZVS was more than 6-times higher than the one in CCM-HSW. The power conversion efficiency exhibits a rapid drop under light load conditions due to a steep escalation of the switching frequency within this operating range. The latter may be avoided by limiting the rate of switching frequency escalation with decreasing the load at low powers. Another option is to introduce pulse skipping mode under extremely light load conditions, as proposed in [106]. However, it must be considered that a switching frequency lower than the one obtained from (4.24) increases the current ripple, which has a crucial effect on total power losses. Therefore determination of a suitable light load switching frequency profile requires further research and, at this point, remains a challenge for the future. Nonetheless, it must be considered that light load efficiency is usually lower than the one in vicinity of the nominal operating point [60, 61, 79, 106–115], therefore this cannot be considered as a unique drawback of the discussed DCM-based ZVS approach.

Although CCM-HSW demonstrated a slightly better performance under light load conditions, DCM-ZVS proved as superior within a wider range around P_{nom}. In addition to higher efficiency, DCM-ZVS achieved a more uniform power loss distribution, which is evident from Fig. 4.17. The



(a)



(b)

Figure 4.16: Measured efficiency curves and the corresponding measured and theoretical switching frequency for the proposed DCM-ZVS control. (a) Efficiency of DCM-ZVS and CCM-HSW in buck mode. (b) Efficiency of DCM-ZVS and CCM-HSW in boost mode.

total power losses generated within the power circuit of the experimental converter operating in buck mode were separated into switching losses of the mainFET $P_{\mathrm{sw,S_H}}$ and syncFET $P_{\mathrm{sw,S_L}}$, conduction losses of the mainFET $P_{\mathrm{cond,S_H}}$ and syncFET $P_{\mathrm{cond,S_L}}$, and magnetic core losses P_{mag} and winding losses P_{wind} of the inductor. Almost 30 W of losses generated on mainFET in CCM-HSW at the nominal power $P_{\mathrm{nom}} = 1000$ W was reduced to about 14 W when operating in DCM-ZVS. Such a reduction in semiconductor losses eliminates the need for forced air or liquid cooling and allows a significant decrease in the size of the converter's cooling components.

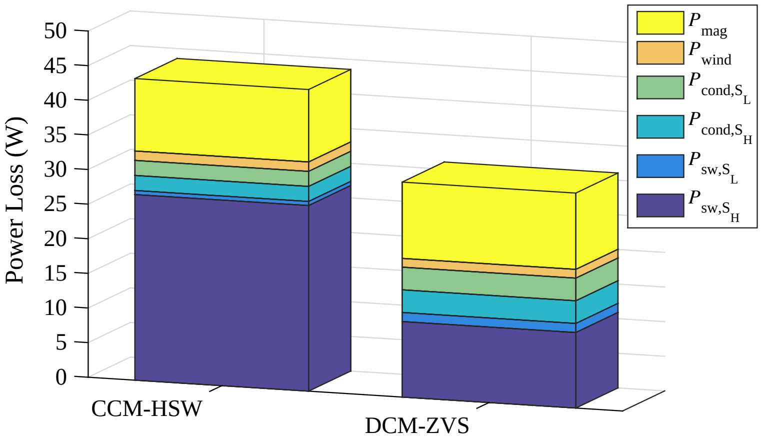


Figure 4.17: Power loss distribution comparison between the experimental converter operating in CCM-HSW and DCM-ZVS at the output power of 1 kW.

4.5 Adaptation of the ZVS control design procedure for usage in ac applications

The HF-switched converter leg of a hybrid modulated H-bridge PFC rectifier represents the main source of switching losses as well as reverse recovery and unwanted turn-on related issues when the converter is operating in CCM with hard-switching. For avoiding these unwanted phenomena and reducing the switching losses, it is desirable to ensure ZVS of the transistors (MOSFETs) within the HF-switched converter leg. Since the latter closely resembles the operation of a half-bridge within a synchronous DC-DC converter, the previously presented DCM-based ZVS approach can be utilized. The simplest way to implement the DCM-based ZVS approach is by using a predetermined constant value of the reversed current I_R, as it was presented for the case of a bidirectional DC-DC converter. While the principle of achieving ZVS within a half-bridge structure remains the same at the presence of alternating voltage and current, the conditions under which each resonant switching transition occurs are different. In the previously presented DCM-based ZVS control of a bidirectional DC-DC converter, the operating switching frequency only depends on the load. Consequently, there is no need for adapting the switching frequency in steady state operation. In contrast to DC-DC applications, the time-varying nature of alternating voltage and current demands not only for load but also for time dependent adaptation of the switching frequency. Another difference in respect to the above presented ZVS control for a DC-DC converter also originates from the alternating input voltage of an H-bridge PFC rectifier. This voltage represents an initial condition for the resonant switching transition in a DCM operated bridge structure (V_B in (4.10)) and thus considerably affects the duration of the transition. With the varying initial conditions, the switching transitions' durations vary accordingly, which adds additional complexity to the DCM-based ZVS control design procedure. Due to the just described facts the ZVS control design procedure proposed for a bidirectional DC-DC converter in Section 4.3 cannot be directly applied to a hybrid modulated H-bridge PFC rectifier but has to be properly adapted for usage in AC applications.

The theoretical voltage, current, and switching frequency waveforms of a hybrid modulated H-bridge PFC rectifier, along with its simplified schematic circuit diagram, are shown in Fig. 4.18. The voltage v_{ac} represents the alternating voltage of the utility grid, which is the input voltage of the discussed rectifier. On the other hand, the voltage v_{dc} represents a constant DC voltage of a higher amplitude than v_{ac}, which is obtained at the output of the converter. The current i_{L} is the current through the boost inductor L, which is of crucial importance for achieving ZVTs. For ensuring the required initial conditions for ZVTs, the switching frequency f_{sw} must vary such that a sufficient magnitude of the reversed current I_{R} is achieved in each switching cycle, as demonstrated by the theoretical waveforms in Fig. 4.18(a). The inductor current i_{L} must be shaped such that the average inductor current $i_{\mathrm{L,avg}}$ waveform exhibits a pure sinusoidal waveform which is in phase with the voltage v_{ac}. Operation with a high PF is achieved in this way. Due to a large HF ripple in i_{L}, the boost inductor L cannot be directly connected to the grid, as shown in the simplified schematic diagram in Fig. 4.18(b). In order to ensure compliance with the conducted electromagnetic emission regulations and standards, a suitable input filter must be applied. A detailed explanation and the guidelines for designing such a filter will be given in Chapter 5. Since it does not play a significant role in designing the ZVS control, the input filter and its effects will be neglected at this point.

As already explained in Section 2.4, the transistors $\mathrm{S_{HN}}$ and $\mathrm{S_{LN}}$ serve for connecting the mid point of the LF-switched converter leg, designated with "B" in Fig. 4.18(b), to either the high or low side of the output capacitor C_{dc}. By adequately performing this action at each zero crossing of the voltage v_{ac}, the hybrid modulated H-bridge PFC rectifier can be represented by the equivalent circuits for positive and negative half-period of the voltage v_{ac}, as shown in Figs. 4.18(c) and 4.18(d). In both cases the equivalent circuit represents a synchronous boost converter with a unipolar full-wave rectified input voltage $|v_{\mathrm{ac}}|$. Therefore the hybrid modulated H-bridge PFC rectifier's operating principle within each grid voltage half-period is similar to the one of the previously presented bidirectional DC-DC converter operating in boost mode. The only major difference is in the varying input voltage v_{ac} from which a constant output voltage v_{dc} has to be obtained.

Reliable ZVS transitions within the entire operating range of a hybrid-modulated H-bridge rectifier can be achieved by operating the converter in the DCM with a constant reversed current I_{R} of sufficient amplitude. A sufficient amplitude of I_{R} designates the value at which the duration of

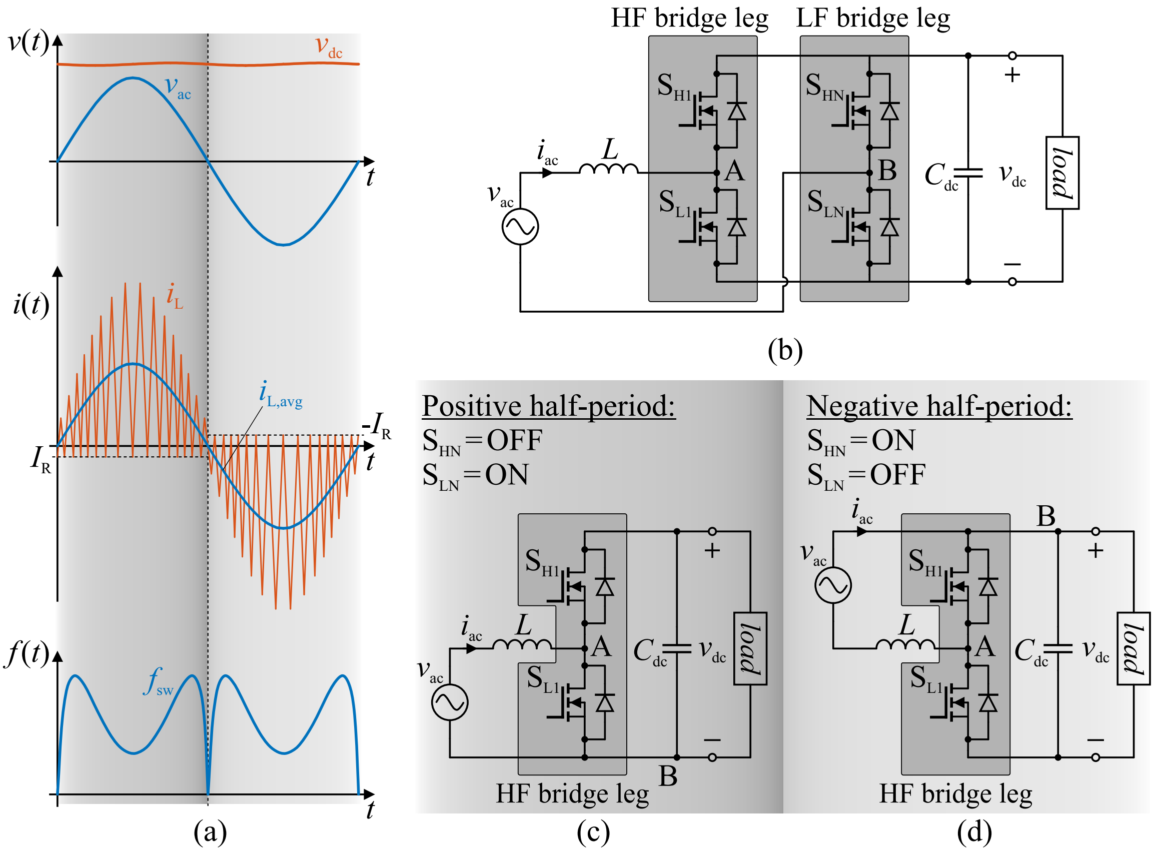

v(t)
v_{dc}
v_{ac}
t
i(t)
i_L
$i_{L,avg}$
$-I_R$
I_R
t
f(t)
f_{sw}
t
(a)
HF bridge leg
LF bridge leg
S_{H1}
S_{HN}
S_{L1}
S_{LN}
i_{ac}
L
A
B
v_{ac}
C_{dc}
v_{dc}
load
+
−
(b)
Positive half-period:
S_{HN}=OFF
S_{LN}=ON
Negative half-period:
S_{HN}=ON
S_{LN}=OFF
HF bridge leg
(c)
(d)

Figure 4.18: Single-phase hybrid-modulated H-bridge PFC rectifier: (a) Theoretical voltage, current and switching frequency waveforms, (b) basic schematic circuit, (c) equivalent circuit during the positive half-period of the grid voltage v_{ac}, and (c) equivalent circuit during the negative half-period of the grid voltage v_{ac}.

resonant switching transitions T_{res} is negligible in respect to the corresponding switching period T_{sw}. Under such conditions, an ideal triangular waveform can be assumed for the inductor current i_L, as it is depicted in Fig. 4.19. On the basis of equivalent circuits for the positive and negative half-periods of v_{ac}, the instantaneous inductor current ripple Δi_L in a hybrid-modulted H-bridge PFC rectifier can be written as

$$\Delta i_L = \frac{(V_{dc} - |v_{ac}|)\,|v_{ac}|\;T_{sw}}{2LV_{dc}}, \tag{4.25}$$

where T_{sw} is the operating switching period and $|v_{ac}|$ the full-wave rectified alternating voltage v_{ac}. The expression (4.25) can be obtained from (4.22) simply by replacing V_A with V_{dc}, and defining the duty cycle D as

$$D = 1 - \frac{|v_{ac}|}{V_{dc}}. \tag{4.26}$$

In order to ensure the required reversed current I_R within each switching cycle, the inductor

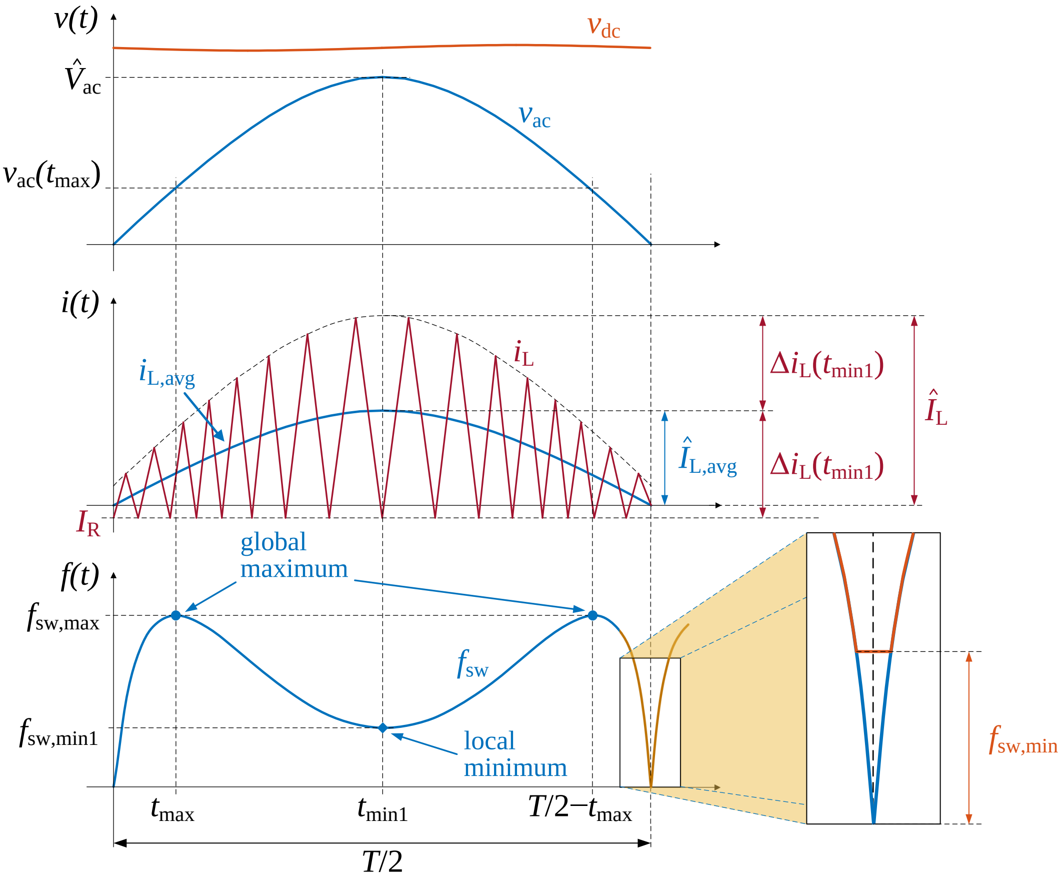

v(t)
v_{dc}
$\hat{V}_{ac}$
v_{ac}
$v_{ac}(t_{max})$
i(t)
i_L
$i_{L,avg}$
$\Delta i_L(t_{min1})$
$\hat{I}_{L,avg}$
$\Delta i_L(t_{min1})$
$\hat{I}_L$
I_R
global maximum
f(t)
$f_{sw,max}$
f_{sw}
$f_{sw,min1}$
local minimum
$f_{sw,min}$
t_{max}
t_{min1}
$T/2-t_{max}$
$T/2$

Figure 4.19: Theoretical voltage, current and switching frequency waveforms for a single-phase hybrid-modulated H-bridge PFC rectifier operating in DCM.

current ripple Δi_{L} must equal

$$\Delta i_{\mathrm{L}} = |i_{\mathrm{L,avg}}| - I_{\mathrm{R}}, \tag{4.27}$$

where $|i_{L,\mathrm{avg}}|$ is the absolute value of the average inductor current $i_{\mathrm{L,avg}}$. Absolute values of $i_{L,\mathrm{avg}}$ and v_{ac} represent the full-wave rectified voltage and current at the input of the studied converter when analyzing it on the basis of its equivalent circuits for the positive and negative half-period of ac voltage, depicted in Figs. 4.18(c) and 4.18(d), respectively.

By assuming a non-distorted utility grid voltage and a perfect control of the converter's input current, the voltage $|v_{\mathrm{ac}}|$ and current $|i_{\mathrm{L,avg}}|$ can be written as

$$|v_{\mathrm{ac}}| = \hat{V}_{\mathrm{ac}} \left|\sin(\omega t)\right|, \tag{4.28a}$$

$$|i_{\mathrm{L,avg}}| = \hat{I}_{\mathrm{L,avg}} \left|\sin(\omega t)\right|, \tag{4.28b}$$

where ω is the angular frequency of the alternating voltage v_{ac}. A substitution of (4.28a), (4.28b), and (4.27) into (4.23), and isolating the expression for T_{sw} yields

$$T_{\mathrm{sw}}(t) = 2L \frac{V_{\mathrm{dc}}}{\left(V_{\mathrm{dc}} - \hat{V}_{\mathrm{ac}} \left|\sin(\omega t)\right|\right) \hat{V}_{\mathrm{ac}} \left|\sin(\omega t)\right|} \left(\hat{I}_{L,\mathrm{avg}} \left|\sin(\omega t)\right| - I_{\mathrm{R}}\right), \tag{4.29}$$

which represents the function by which the switching period T_{sw} has to vary in order to achieve the reversed current I_{R} within each switching cycle and thus the necessary conditions for resonant ZVTs. In contrast to (4.24) which applies for calculating the switching period in a DCM-based ZVS DC-DC converter, the expression (4.29) comprises the time varying nature of the alternating voltage and current in rectifier applications. Consequently, the calculated switching period T_{sw} does not only vary with the current load conditions, but also with time. For the purpose of further analysis, the switching period T_{sw} will be represented with its inverse value, the switching frequency f_{sw}, which is calculated as

$$f_{\mathrm{sw}}(t) = \frac{\left(V_{\mathrm{dc}} - \hat{V}_{\mathrm{ac}} \left|\sin(\omega t)\right|\right) \hat{V}_{\mathrm{ac}} \left|\sin(\omega t)\right|}{2L\, V_{\mathrm{dc}} \left(\hat{I}_{L,\mathrm{avg}} \left|\sin(\omega t)\right| - I_{\mathrm{R}}\right)}. \tag{4.30}$$

The $f_{\mathrm{sw}}(t)$ waveform obtained on the basis of (4.30) has already been presented in Fig. 4.18(a) and is once again depicted in Fig. 4.19, in which the main characteristic points are marked. These characteristic points represent global and local extremes of the switching frequency waveform, which play an important role in the DCM-based ZVS control design. By differentiating (4.30) in respect to time and equalizing the obtained first time derivative with 0, the instants at which the extremes occur are obtained as

$$t_{\max} = \frac{1}{\omega} \arcsin\left[\frac{\hat{V}_{\mathrm{ac}}\, I_{\mathrm{R}} + \sqrt{\hat{V}_{\mathrm{ac}}^2\, I_{\mathrm{R}}^2 - \hat{V}_{\mathrm{ac}}\, \hat{I}_{\mathrm{ac}}\, V_{\mathrm{dc}}\, I_{\mathrm{R}}}}{\hat{V}_{\mathrm{ac}}\, \hat{I}_{\mathrm{ac}}}\right], \tag{4.31a}$$

$$t_{\mathrm{min1}} = \frac{T}{4}, \tag{4.31b}$$

where $t_{\max}$ is the time instant at which the highest switching frequency $f_{\mathrm{sw,max}}$ is reached, t_{min1} the time instant at which a local minimum $f_{\mathrm{sw,min1}}$ in switching frequency is reached, and T the period of alternating voltage v_{ac}. It can be inferred from (4.31b) that the local minimum $f_{\mathrm{sw,min1}}$ in switching frequency occurs when the alternating input voltage and current reach their peak values $\hat{V}_{\mathrm{ac}}$ and $\hat{I}_{\mathrm{ac}}$, respectively. Since the peak inductor current $\hat{I}_{\mathrm{L}}$ and the accompanying maximum inductor current ripple $\Delta i_{\mathrm{L}}(t_{min1})$ generate the highest hysteretic core losses and turn-off losses per switching period, the drop in switching frequency in this operating region is considered a favorable property of the DCM-based ZVS operation. While the local minimum $f_{\mathrm{sw,min}}$ always occurs in the middle of each AC voltage's half-period independently of the current operating conditions, the instants of maximum switching frequency $f_{\mathrm{sw,max}}$ vary depending on the current load conditions, the selected magnitude of the reversed current and the effective voltage conversion ratio. In steady state operation both global maximums of the switching frequency f_{sw} appear symmetrical in respect to the local minimum $f_{\mathrm{sw,min1}}$, as evident from Fig. 4.19.

Another critical region in the switching frequency waveform is the beginning and the end of each ac voltage half-period, where the calculated switching frequency f_{sw} exhibits an extremely high rate of change and reaches zero at the instant of v_{ac} zero crossing. Such high rates of switching frequency change and operation with very low switching frequency may cause stability issues in the converter's control. In addition to the control issues, operation within the audible range of switching frequencies below 16 kHz is not acceptable in a wide range of applications. For these reasons a minimum allowed switching frequency $f_{\mathrm{sw,min}}$ is introduced, as shown in the zoomed in part of Fig. 4.19. Since $f_{\mathrm{sw,min}}$ represents the absolute minimum of the switching frequency f_{sw}, it must be selected such that it is at all times lower than $f_{\mathrm{sw,min1}}$. In the opposite case, ZVS may be lost.

The importance of selecting the right combination of the reversed current I_{R}, power inductor's inductance L, and dead time duration T_{DT} for achieving reliable ZVTs within the entire operating range of the converter operating in DCM has already been presented for the case of a bidirectional DC-DC converter. In order to find the right combination of these critical parameters for a hybrid-modulated H-bridge PFC rectifier, the ZVS control design procedure described in Section 4.3 has been adapted to suit the operating conditions imposed by the time varying voltage, current, and switching frequency in ac applications. The resulting ZVS control design procedure is presented in the form of a flowchart in Fig. 4.20 and additionally explained in the following points:

1) specification of the parameters:

- V_{dc} - DC voltage applied across the drain and source terminals of the power transistors in the circuit,
- $\hat{V}_{\mathrm{ac}}$ - peak value of the alternating voltage v_{ac},
- $\hat{I}_{\mathrm{Lavg,max}}$ - peak value of the average inductor current $i_{\mathrm{L,avg}}$ at the highest expected input power,
- $\hat{I}_{\mathrm{Lavg,min}}$ - peak value of the average inductor current $i_{\mathrm{L,avg}}$ at the lowest expected input power,
- $f_{\mathrm{sw,min}}$ - absolute minimum switching frequency,
- $f_{\mathrm{sw,max}}$ - absolute maximum switching frequency,
- $T_{\mathrm{res,max}}$ - maximum allowed duration of a resonant switching transition;

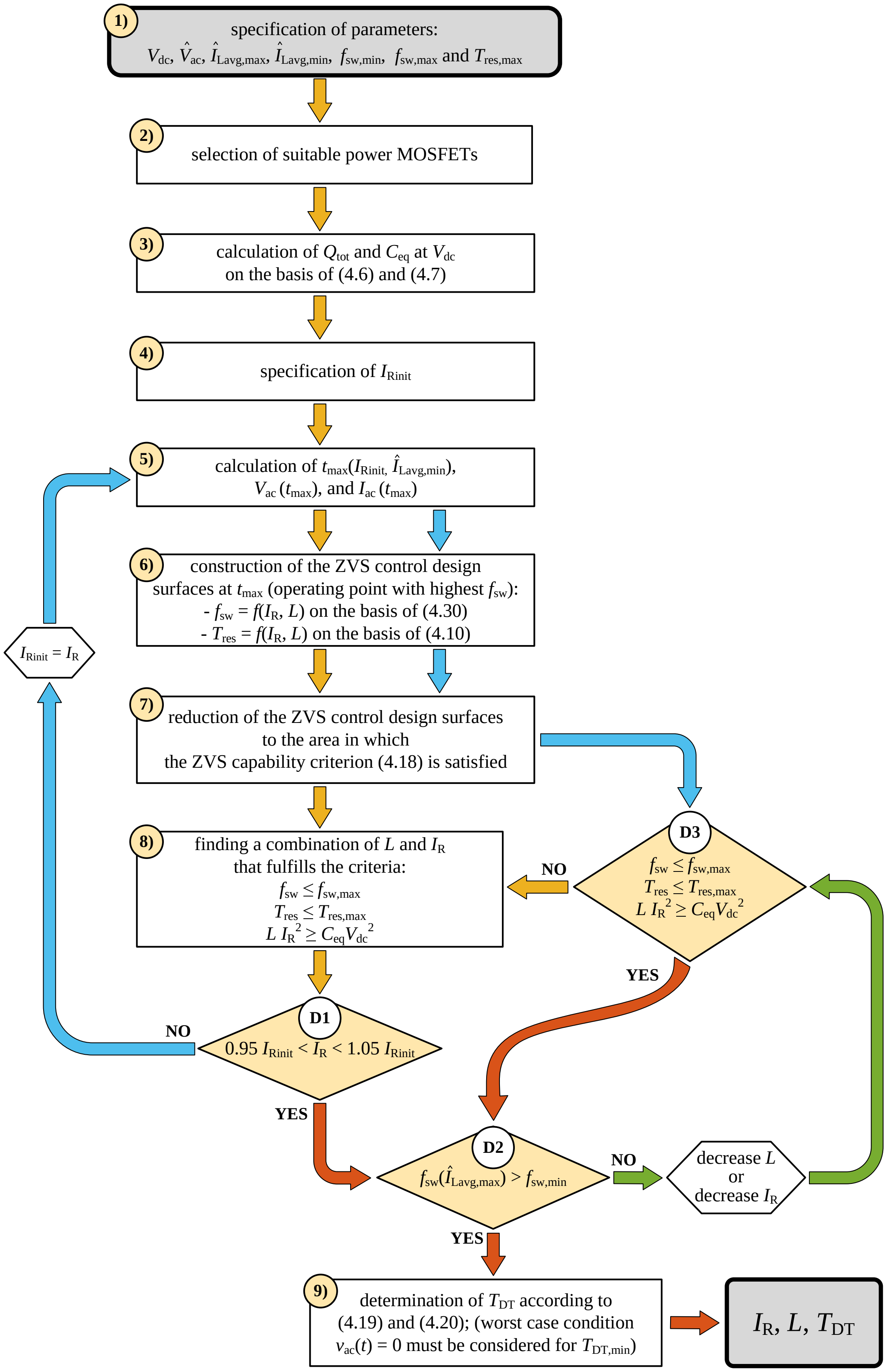

1)
specification of parameters:
V_{dc}, $\hat{V}_{ac}$, $\hat{I}_{Lavg,max}$, $\hat{I}_{Lavg,min}$, $f_{sw,min}$, $f_{sw,max}$ and $T_{res,max}$
2)
selection of suitable power MOSFETs
3)
calculation of Q_{tot} and C_{eq} at V_{dc} on the basis of (4.6) and (4.7)
4)
specification of I_{Rinit}
5)
calculation of $t_{max}(I_{Rinit}, \hat{I}_{Lavg,min})$, $V_{ac}(t_{max})$, and $I_{ac}(t_{max})$
6)
construction of the ZVS control design surfaces at t_{max} (operating point with highest f_{sw}):
- $f_{sw} = f(I_R, L)$ on the basis of (4.30)
- $T_{res} = f(I_R, L)$ on the basis of (4.10)
$I_{Rinit} = I_R$
7)
reduction of the ZVS control design surfaces to the area in which the ZVS capability criterion (4.18) is satisfied
8)
finding a combination of L and I_R that fulfills the criteria:
$f_{sw} \leq f_{sw,max}$
$T_{res} \leq T_{res,max}$
$L\,I_R^2 \geq C_{eq} V_{dc}^2$
D3
$f_{sw} \leq f_{sw,max}$
$T_{res} \leq T_{res,max}$
$L\,I_R^2 \geq C_{eq} V_{dc}^2$
NO
YES
D1
$0.95\,I_{Rinit} < I_R < 1.05\,I_{Rinit}$
NO
YES
D2
$f_{sw}(\hat{I}_{Lavg,max}) > f_{sw,min}$
NO
decrease L or decrease I_R
YES
9)
determination of T_{DT} according to (4.19) and (4.20); (worst case condition $v_{ac}(t) = 0$ must be considered for $T_{DT,min}$)
I_R, L, T_{DT}

Figure 4.20: ZVS control design flowchart for a hybrid-modulated H-bridge PFC rectifier.

2) selection of the most suitable power MOSFETs on the basis of V_{dc}, $\hat{I}_{\mathrm{Lavg,max}}$, parasitic capacitances, and other relevant parameters;

3) calculation of the total gate charge Q_{tot} and equivalent capacitance C_{eq} at V_{dc} for the selected transistors, according to (4.6) and (4.7), respectively; V_{A} in (4.6) and (4.7) must be replaced with V_{dc};

4) specification of an expected or desired value of the reversed current I_{Rinit};

5) calculation of t_{max} at I_{Rinit} and $\hat{I}_{\mathrm{Lavg,min}}$ on the basis of (4.31a) and determination of the corresponding $v_{\mathrm{ac}}(t_{\mathrm{max}})$ and $i_{\mathrm{Lavg}}(t_{\mathrm{max}})$ on the basis of (4.28a) and (4.28b), respectively; t_{max}, $v_{\mathrm{ac}}(t_{\mathrm{max}})$ and $i_{\mathrm{Lavg}}(t_{\mathrm{max}})$ define the instant at which the absolute highest switching frequency is achieved;

6) construction of the ZVS control design surfaces $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$ and $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$ at the instant t_{max} for the operating point with the highest switching frequency; $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$ is constructed on the basis of (4.30), while $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$ is constructed on the basis of (4.10) in which V_{B} is replaced by $v_{\mathrm{ac}}(t_{\mathrm{max}})$;

7) reduction of the ZVS control design surfaces to the area in which the ZVS capability criterion (4.18) is satisfied, as demonstrated in Fig. 4.21; adaptation of (4.18) to the discussed AC-DC converter requires replacement of V_{A} with V_{dc} and V_{B} with v_{ac}; the most demanding operating condition for achieving ZVS occurs at $v_{\mathrm{ac}} = 0$ and therefore the most stringent ZVS capability criterion for an AC-DC converter becomes $L\,{I_{\mathrm{R}}}^2 \geq C_{\mathrm{eq}} V_{\mathrm{dc}}^2$;

8) finding a combination of L and I_{R} that fulfills the following conditions:

$$f_{\mathrm{sw}} \leq f_{\mathrm{sw,max}}, \tag{4.32a}$$

$$T_{\mathrm{res}} \leq T_{\mathrm{res,max}}, \tag{4.32b}$$

$$L\,{I_{\mathrm{R}}}^2 \geq C_{\mathrm{eq}} V_{\mathrm{dc}}^2. \tag{4.32c}$$

D1) verification as to whether the selected I_{R} is within $\pm 5\ \%$ of the initially specified I_{Rinit} on the basis of which the ZVS control design surfaces were constructed; in the case when the condition “D1” is not fulfilled, the tasks under points 5), 6), and 7) are performed once again with $I_{\mathrm{Rinit}} = I_{\mathrm{R}}$, where I_{R} is the value selected in 9);

D2) verification as to whether the switching frequency at $\hat{I}_{\mathrm{Lavg,max}}$ is higher than the specified absolute minimum switching frequency $f_{\mathrm{sw,min}}$; in the case when the condition “D2” is not fulfilled ZVS may be lost in the vicinity of the most critical operating point in terms of power losses;

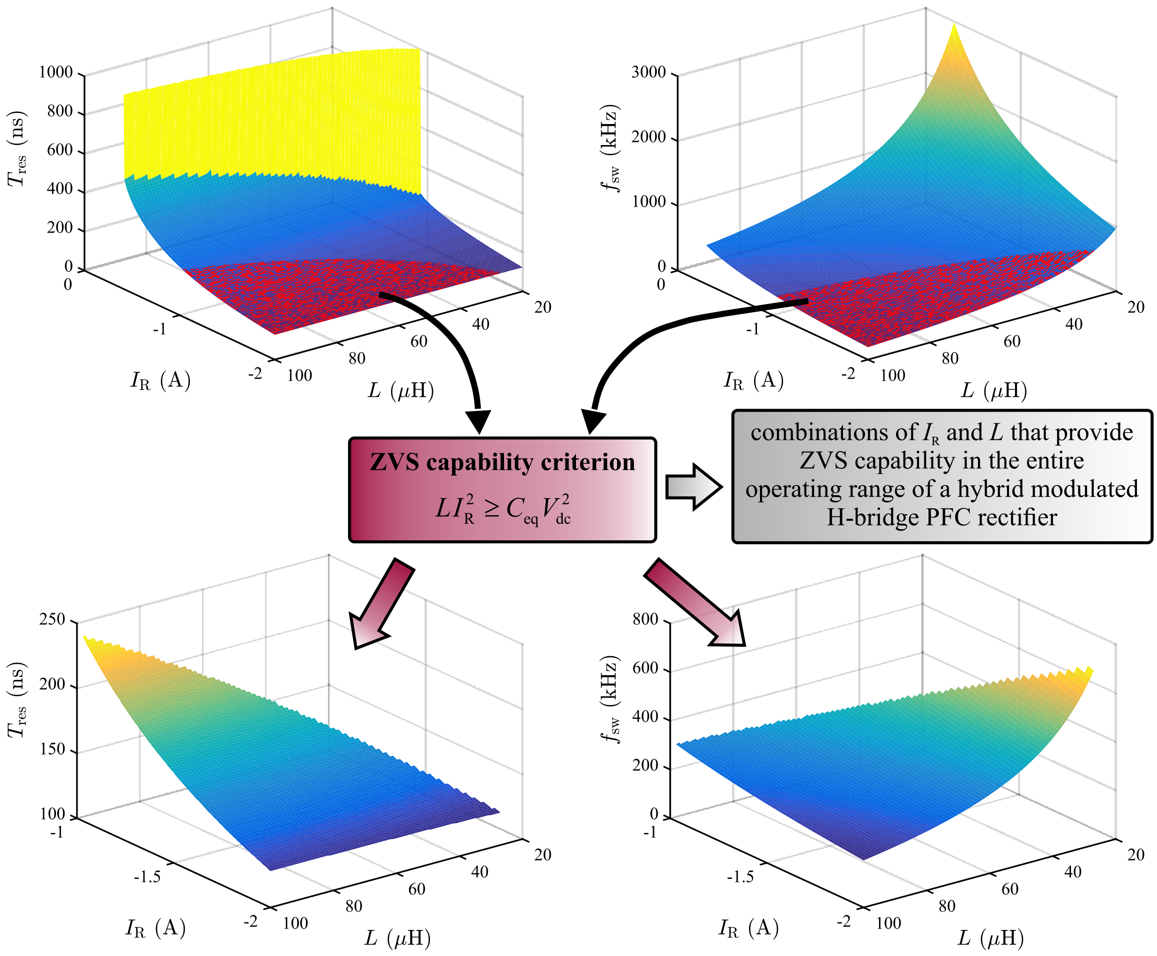


Figure 4.21: ZVS control design surfaces $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$ and $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$ and their reduction to the area in which the ZVS capability criterion is satisfied.

for avoiding this, L or I_{R} have to be decreased in order to achieve operation at higher switching frequencies;

D3) verification as to whether the criteria specified under 8) are still fulfilled after the modifications introduced after not fulfilling the conditions “D1” or “D2”; in the case when the conditions of “D3” are not fulfilled, the task under point 8) has to be performed once again;

9) determination of a proper dead time duration T_{DT} according to (4.19) and (4.20); for determining $T_{\mathrm{DT,min}}$ the worse case condition has to be considered (i.e. when the duration of the switching transition T_{res} is the longest), which occurs at $v_{\mathrm{ac}}(t) = 0$.

CHAPTER 5

DESIGN OF A ZVS H-BRIDGE AC-DC CONVERTER

5.1 Converter design specifications and objectives

The investigated single-phase non-isolated AC-DC converter is intended for usage as a utility grid interface in smart residential nanogrids [54] and in on-board electric vehicle battery chargers that will provide vehicle-to-grid functionality [51–53]. Both applications require the grid interface to support bidirectional power flow and therefore the investigated converter has to operate as both a grid-connected inverter and rectifier with PFC capability. The converter is aimed to be connected to the European low-voltage public utility grid with a nominal voltage of $V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$ and a line frequency of $f_{\mathrm{L}} = 50\,\mathrm{Hz}$. Considering the supply voltage tolerances specified in IEC60038:2009 [116], the expected AC voltage at the converter's terminals may differ by $\pm 10\ \%$ from the nominal voltage $V_{\mathrm{AC,nom}}$. With a nominal input power specified as $P_{\mathrm{nom}} = 3\,\mathrm{kW}$, the nominal AC current is $I_{\mathrm{AC,nom}} = 13\ \mathrm{A_{rms}}$. The nominal voltage across the DC terminals is defined as $V_{\mathrm{DC,nom}} = 400\mathrm{V}$, while the expected operating range of DC voltage is between 360 and 420 V. This specific DC voltage range was selected in order to achieve compatibility with common voltage levels in DC nanogrids [28, 54, 117] and on-board battery chargers for electric vehicles [50]. As a result of the specified AC and DC voltage ranges, the investigated AC-DC converter has to provide boost functionality when operating as a rectifier and buck functionality when operating as an inverter. In the rectifier operating mode, the converter has to ensure a stable voltage at its DC terminals with a maximum low frequency voltage ripple of $\Delta v_{\mathrm{DC}} = 20\ \mathrm{V}$, which accounts for $5\ \%$

of the nominal DC voltage $V_{\mathrm{DC,nom}}$.

The main objective regarding the performance of the converter is to ensure high power conversion efficiency in a wide operating range. Within the entire range from $10\ \%$ to $100\ \%$ of the nominal power P_{nom} the efficiency must be higher than 96 $\%$ for all the AC and DC voltages within the specified ranges. In addition, the converter must have an efficiency of at least 97 $\%$ at the nominal operating point. As an additional challenge, a low volume design of the converter is required, with a power density of approximately $1\ \mathrm{kW/liter}$. The latter is set as an objective due to a potential usage in on-board electric vehicle battery chargers, where the size and weight of the components are of crucial importance. In order to reduce the complexity of the power conditioning unit and reduce its own consumption, forced convection cooling using fans and water cooling should be avoided. Instead, a natural convection-based cooling system must be utilized.

The remainder of the specifications is related to achieving compliance with different kinds of power quality and electromagnetic compatibility (EMC) standards. On the basis of the converter's target applications, compliance must be achieved with EMC standards CISPR 14 [118] and CISPR 22 [119] for class B equipment. In addition, compliance with IEC 61000-3-2 [1] must be achieved as well. The latter specifies the limits for low-frequency current harmonics (up to 40^{th}) injected into the public utility grid and applies to all the electrical and electronic equipment that draws or injects a current up to and including $16\ \mathrm{A_{rms}}$ per phase. In addition to the requirements of the above-listed mandatory low-frequency and radio-frequency EMC standards, several other design objectives were set, namely the total harmonic distortion (THD) of AC current and power factor (PF). None of these parameters is specified in the directly applicable standards. Since the THD of AC current expresses the content of higher order harmonics in respect to the fundamental harmonic, it is possible to estimate its maximum permitted value from the harmonic limitations specified in IEC 61000-3-2 [1]. However, such estimation results in very loose THD requirements, which do not represent a serious challenge even for passive PFC circuits. Therefore the THD limitation was adapted from IEC 61727 [120] which applies for utility grid-interconnected photovoltaic systems. The standard specifies a THD of less than $5\ \%$ at the rated output power of the inverter. For the case of the investigated DC-AC converter, this limit was extended to the operating range between $10\ \%$ and $100\ \%$ of the nominal power P_{nom}. IEC 61727 is one of the few standards that specifies the minimum allowed PF, which has to be greater than 0.9 at output powers greater than $50\ \%$ of the inverter's rated power. Due to the high quality AC current waveform requirement imposed by the THD limit, the investigated AC-DC converter's power factor is expected to remain above 0.9 within the entire operating range between $10\ \%$ and $100\ \%$ of the nominal power P_{nom}. For the purpose

Table 5.1: Design specifications and objectives for the investigated single-phase non-isolated AC-DC converter

Parameter		**Description**	**Value**
AC-side	V_{AC}	nominal AC voltage AC voltage operating range	$V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$ $207\ \mathrm{V_{rms}} \leq V_{\mathrm{AC}} \leq 253\ \mathrm{V_{rms}}$
	I_{AC}	nominal AC current AC current operating range	$I_{\mathrm{AC,nom}} = 13\ \mathrm{A_{rms}}$ $-13\ \mathrm{A_{rms}} \leq I_{\mathrm{AC}} \leq 13\ \mathrm{A_{rms}}$
	f_{L}	line frequency	$50\ \mathrm{Hz}$
DC-side	V_{DC}	nominal DC voltage DC voltage operating range	$V_{\mathrm{DC,nom}} = 400\ \mathrm{V}$ $360\ \mathrm{V} \leq V_{\mathrm{DC}} \leq 420\ \mathrm{V}$
	I_{DC}	nominal DC current DC current operating range	$I_{\mathrm{DC,nom}} = 7.5\ \mathrm{A}$ $-7.5\ \mathrm{A} \leq I_{\mathrm{DC}} \leq 7.5\ \mathrm{A}$
	Δv_{DC}	maximum allowed DC voltage ripple	$\Delta v_{\mathrm{DC,max}} = 20\ \mathrm{V}$
η		efficiency at nominal operating point efficiency within the range: $0.1\,P_{\mathrm{nom}} \leq P \leq P_{\mathrm{nom}}$	$\eta_{\mathrm{nom}} \geq 97\ \%$ $\eta \geq 96\ \%$

EMC compliance and power quality
• compliance with the disturbance limits specified in EMC standards CISPR 14 and CISPR 22 (class B equipment)
• compliance with the current harmonic limits specified in IEC 61000-3-2
• THD $< 5\ \%$ within the operating range: $0.1\,P_{\mathrm{nom}} \leq P \leq P_{\mathrm{nom}}$
• PF > 0.9 within the operating range: $0.1\,P_{\mathrm{nom}} \leq P \leq P_{\mathrm{nom}}$

Other Design Objectives
• bidirectional power flow capability
• power density $\approx 1\ \mathrm{kW/liter}$
• natural convection-based cooling

of a clear and concise representation, all the defined specifications are summarized in Table. 5.1.

5.2 Converter structure

A single-phase H-bridge converter depicted in Fig. 2.4(a) is commonly utilized in applications where the power converter has to support bidirectional power flow, and provide AC-DC conversion with boost properties in the rectifier mode and buck properties in the inverter mode [28, 30, 32, 70]. Additional requirements for achieving a high power conversion efficiency in a wide operating range and a low volume design with natural convection-based cooling represent a fundamental design challenge. On the basis of the results obtained through the analysis of hard switching transitions in bridge structures (see Chapter 3), CCM operation with hard switching is not the best option when aiming for the specifications listed in Table 5.1. An extremely high power conversion efficiency can be achieved by designing the converter to operate with a low switching frequency in CCM. This is mainly due to very low switching losses, which also result in low cooling requirements and the possibility for using a natural convection-based cooling system. The downside of this approach is in the large size of the passive components and the resulting low power density. On the other hand, a converter designed to operate in CCM with a higher switching frequency, at which the size of the passive components can be reduced, suffers from the problem of excessive switching losses. The latter prevent the converter from achieving high efficiency and significantly increase the cooling requirements. The utilization of a larger cooling system may completely annul the gain in volume obtained by using smaller passive components. This is especially critical in the investigated case, requiring natural convection-based cooling. In order to overcome these power conversion efficiency and power density related limitations, the converter must be operated in the ZVS regime.

As has been presented in Section 4.5, a hybrid-modulated H-bridge converter can achieve ZVS when operating in DCM with a constant magnitude of the reversed current within each switching cycle. Such operation eliminates the turn-on losses of the transistors in the HF-switched bridge leg, which are otherwise dominant (see Fig.3.9) and have a detrimental effect on power conversion efficiency, cooling requirements, and maximum attainable power density. While the inductor current reversal within each switching cycle represents the key for achieving the desirable ZVS in a bridge structure, it also results in an extremely high inductor current ripple. The latter causes an increase in conduction losses, turn-off losses, and magnetic core losses, as evident from Fig. 4.17. In spite of these marginal increases, the total power losses remain significantly lower than in CCM due to the absence of the dominant turn-on losses.

Another consequence of the high inductor current ripple in DCM are the increased differential mode (DM) noise filtering requirements [19, 121–123]. Since the EMI filters in high power density CCM operated converters typically take up to 30 $\%$ of their total size [18], it is expected that this share is significantly higher for DCM operated converters. In order to avoid excessive losses in multi-stage DM filters and meeting the specified power density target, the investigated DC-AC converter's AC-side current ripple has to be suppressed. An effective way of reducing the current ripple, and consequently the DM EMI filtering requirements, is to interleave several converters [121, 122, 124]. An interleaved power converter structure comprises several parallel-connected converters, so-called interleaved cells, operating with an identical switching frequency. The switching instants of these interleaved cells are sequentially shifted for a certain fraction of the switching period, depending on the number of active cells in the structure. Consequently, the ripple currents flowing through individual interleaved cells are also displaced for the same fraction of the switching period, so that they cancel each other out. The resulting sum of the individual cell currents has a significantly lower HF ripple, the harmonic content of which is pushed to higher frequencies where smaller sized filter components can be used for its suppression.

The effects of interleaving on the input current of a hybrid-modulated H-bridge DC-AC converter operating as a rectifier are demonstrated in Fig. 5.1. Since neither the LF-switched bridge leg nor the dc-bus capacitor C_{dc} affect the HF ripple in the input current i_{in}, there is no need for their multiplication. Each interleaved cell is formed solely of the HF-switched bridge leg and the corresponding power inductor. In order to achieve a perfect sharing of the current among interleaved cells in practice and thus maximize the ripple cancellation effect, the cells have to be identical and the converter designed as symmetrically as possible. Fig. 5.1(a) shows the basic case with no interleaving. The converter operates as rectifier with a resistive load at its output and a typical DCM inductor current i_{L} waveform, achieved by varying the switching frequency according to (4.30). The input current i_{in} equals the inductor current i_{L} and has a HF peak-to-peak ripple of more than two times its average value $i_{\mathrm{in,avg}}$. In the case presented in Fig.5.1(b), two HF bridge legs with corresponding power inductors L_1 and L_2 are interleaved. It is evident from the magnified current waveforms, that the inductor currents i_{L1} and i_{L2} are phase-shifted by 180° in respect to each other. As a result the HF ripple in the input current i_{in} is significantly reduced and its fundamental frequency pushed to twice the instantaneous switching frequency of the interleaved cells. Fig.5.1(c) depicts a case with three interleaved cells. The inductor currents i_{L1}, i_{L2}, and i_{L3} are phase-shifted by 120° in respect to each other. The HF ripple in the input current i_{in} is suppressed to an even greater extent than in the case of two interleaved cells, while the fundamental frequency of the ripple is three times the converter's switching frequency. By lowering the magnitude of the HF ripple in the input current i_{in} and by shifting its fundamental frequency to higher values, the required attenuation of the DM EMI filter is decreased, which leads to a smaller volume of the EMI filter [125].

In addition to lower DM EMI filtering requirements, current sharing among the interleaved cells also provides several benefits. The power inductors and the HF-switched bridge legs do not have to be designed for carrying the entire nominal ac-side current but only its fraction, which

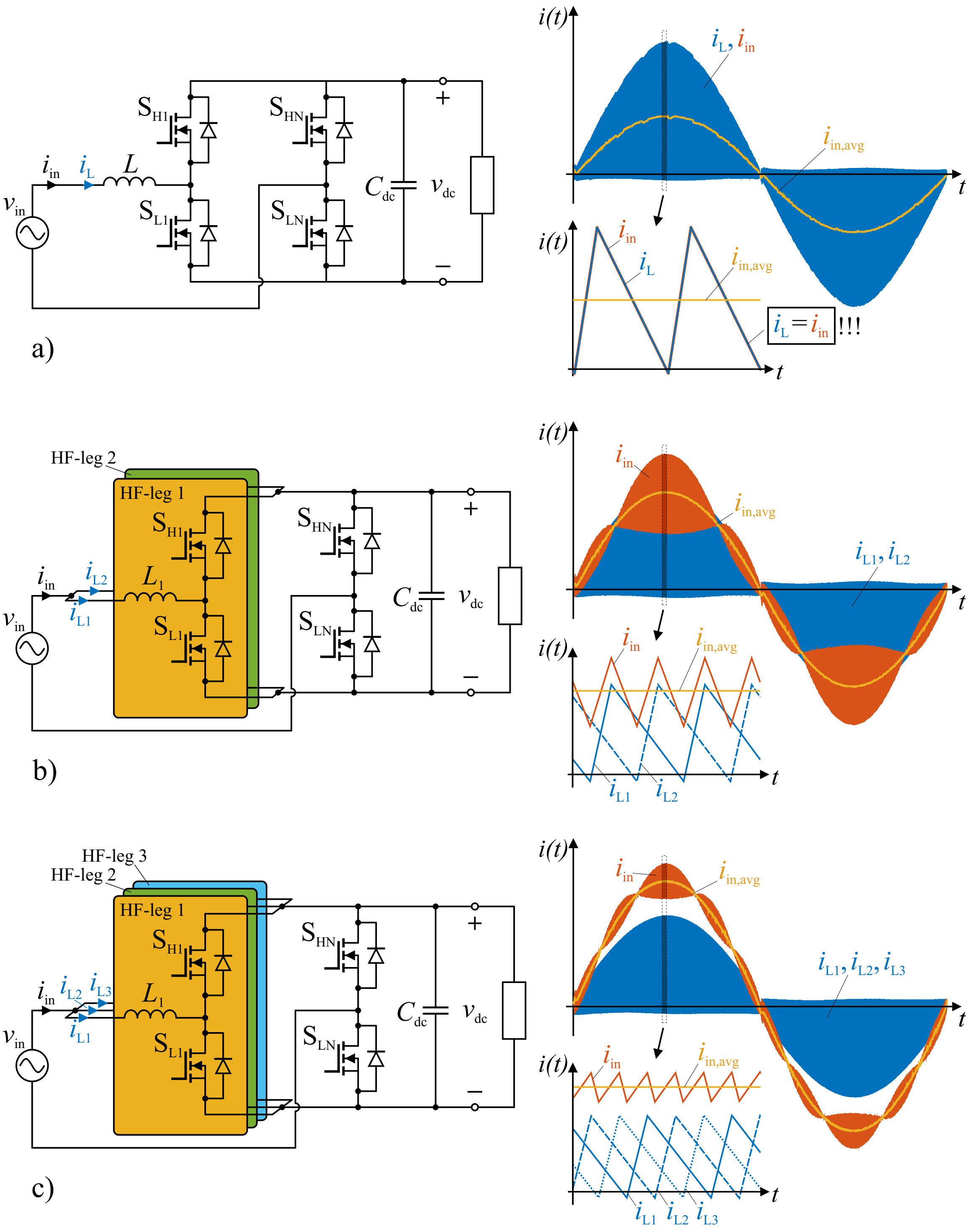

S_H1
S_HN
S_L1
S_LN
i_in
i_L
L
v_in
C_dc
v_dc
+
−
a)
i(t)
i_L, i_in
i_in,avg
t
i(t)
i_in
i_L
i_in,avg
i_L = i_in !!!
t
HF-leg 2
HF-leg 1
i_in
i_L2
i_L1
L_1
b)
i(t)
i_in
i_in,avg
i_L1, i_L2
t
i(t)
i_in
i_in,avg
i_L1
i_L2
t
HF-leg 3
HF-leg 2
HF-leg 1
i_in
i_L2
i_L3
i_L1
c)
i(t)
i_in
i_in,avg
i_L1, i_L2, i_L3
t
i(t)
i_in
i_in,avg
i_L1
i_L2
i_L3
t

Figure 5.1: Interleaved H-bridge DC-AC converter operating as a rectifier and the effects of interleaving on the input current and inductor current waveforms. For providing a fair comparison, all the presented cases depict operation at the same input power: (a) single-cell operation without interleaving, (b) two interleaved cells, and (c) three interleaved cells.

depends on the number of interleaved cells. As the peak-to-peak inductor current ripple in a DCM operated converter is higher than twice its average value, current sharing between interleaved cells also significantly affects the HF current ripple within each cell. It is evident from Fig. 5.1, how the number of interleaved cells reduces the ripple current through individual inductors. If the peak inductor current ripple i_L in the case of no interleaving is about two times the peak value of the average input current $i_\mathrm{in,avg}$, the peak inductor current ripples i_L1, i_L2, and i_L3 in the case of three interleaved cells account for only about 70 $\%$ of the average input current's $i_\mathrm{in,avg}$ peak value. As a result, there is a lower current stress on power semiconductors, lower magnetic core losses and lower conduction losses within the entire converter's circuit. The usage of several parallelled transistors and inductors in an interleaved converter does not only lead to a reduction in power losses but also to a better power loss distribution. Since the sources of heat are distributed over a wider area and not concentrated in one point, as is the case in single-cell operation, the cooling requirements as well as the cooling system design tend to be less demanding. Another favorable property of interleaving is the possibility for employing the cell shedding technique. The fundamental idea of this technique is based on turning off individual interleaved cells under light load conditions and thus improving the light load efficiency of the converter [121,126]. This functionality is especially beneficial in the case of a DCM operated converter, the switching frequency of which is increasing with decreasing the load and reaches very high values at low operating powers, as it was presented in Section 4.4. Since the switching frequency in a DCM operated converter depends on the current flowing through each cell, turning off individual interleaved cells under light load conditions would increase the current through the active cells and thus allow the converter to operate at a lower switching frequency. By proper employment of the cell shedding technique, an interleaved DCM converter can be operated within a rather narrow range of effective switching frequencies at which a high power conversion efficiency is maintained over its entire operating range.

Higher power processing capability due to current sharing between individual cells, better heat distribution, lower DM EMI filtering requirements, narrower range of operating switching frequencies due to the possibility of cell shedding, and better power conversion efficiency over a wider operating range represent arguments for utilization of an interleaved converter structure. For achieving the best performance and a low volume design, the selection of number of interleaved cells is of crucial importance. When suitable power transistors and inductors are used, a higher number of interleaved cells generally leads to lower total power losses and consequently higher power conversion efficiency. In terms of power density, the trends are not so clear. Each additional interleaved cell contributes to a reduction of the HF current ripple by canceling out the subsequent remaining harmonic component. As a result, the DM EMI filtering requirements are reduced and EMC compliance can be achieved by employing a smaller filter, which yields a gain in power density. On the other hand, the introduction of additional interleaved cells increases the size of the converter's main power circuit and thus reduces the power density.

The number of interleaved cells in the investigated DC-AC converter was selected on the basis of volume and power loss estimation. The analysis focused exclusively on the power losses and size of the HF-switched bridge leg and the power inductor, which form each interleaved cell. The losses and size of the LF-switched bridge leg, DC-side capacitor, EMI filter and control stage were not subject to a comprehensive analysis at this point. Nevertheless, understanding their dependence on the number of interleaved cells is important, and can be summarized in the following points:

- each additional interleaved cell additionally suppresses the ripple in the current flowing through the LF-switched less and reduces the conduction losses;
- lower HF ripple current results in lower power losses in the DC-side capacitor and loosens the ripple current requirements when designing the DC-side capacitor bank;
- a higher number of interleaved cells leads to a smaller size of the EMI filter and lower power losses within the filter;
- the influence of the number of interleaved cells on the size and power losses of the control stage are negligible.

According to the above listed facts, the usage of as many interleaved cells as possible would generally reduce both the power losses and the size of the converter stages surrounding these cells. The same conclusion does not apply to the part formed by the HF-switched legs and power inductors, as exceeding the optimum number of interleaved cells would result in an increased total size of the converter's power circuit, without providing a considerable reduction in total power losses and filtering requirements.

In order to obtain a fair power loss and size comparison between the cases of using different number of interleaved cells, it was selected that the HF-switched bridge legs must operate with a local minimum switching frequency of $f_{\mathrm{sw,min1}} = 50\mathrm{kHz}$ at the nominal operating point specified in Table 5.1. On the basis of this operating condition, the required inductances L_{req} of power inductors were determined as

$$L_{\mathrm{req}} = \frac{\left(V_{\mathrm{dc,nom}} - \hat{V}_{\mathrm{ac,nom}}\right)\hat{V}_{\mathrm{ac,nom}}}{2\,V_{\mathrm{dc,nom}}\,f_{\mathrm{sw,min1}}\left(\frac{2P_{\mathrm{nom}}}{n\hat{V}_{\mathrm{ac,nom}}} - I_{\mathrm{R}}\right)}, \tag{5.1}$$

Table 5.2: Power inductor configurations designed for usage with different number of interleaved cells.

Inductor properties	**No interleaving (1 cell)**	**2 interleaved cells**	**3 interleaved cells**	**4 interleaved cells**
Maximum inductor current $I_{\mathrm{L,max}}$	38.1 A	19.69 A	13.56 A	10.5 A
Magnetic core	Magnetics, MPP Toroid, 55191-A2	Magnetics, MPP Toroid, 55440-A2	Magnetics, MPP Toroid, 55256-A2	Magnetics, MPP Toroid, 55256-A2
Wire type and size	Solid wire, 15 AWG	Solid wire, 15 AWG	Solid wire, 17 AWG	Solid wire, 17 AWG
Number of turns	23	32	49	55
Winding resistance R_{L}	16 mΩ	21.4 mΩ	40 mΩ	45 mΩ
No load inductance	31.5 μH	60 μH	84 μH	105 μH
Inductance at $I_{\mathrm{L,max}}$	29.6 μH	57.9 μH	79 μH	101.6 μH
Volume V_{L}	70.93 cm^3	55.92 cm^3	32.84 cm^3	32.84 cm^3

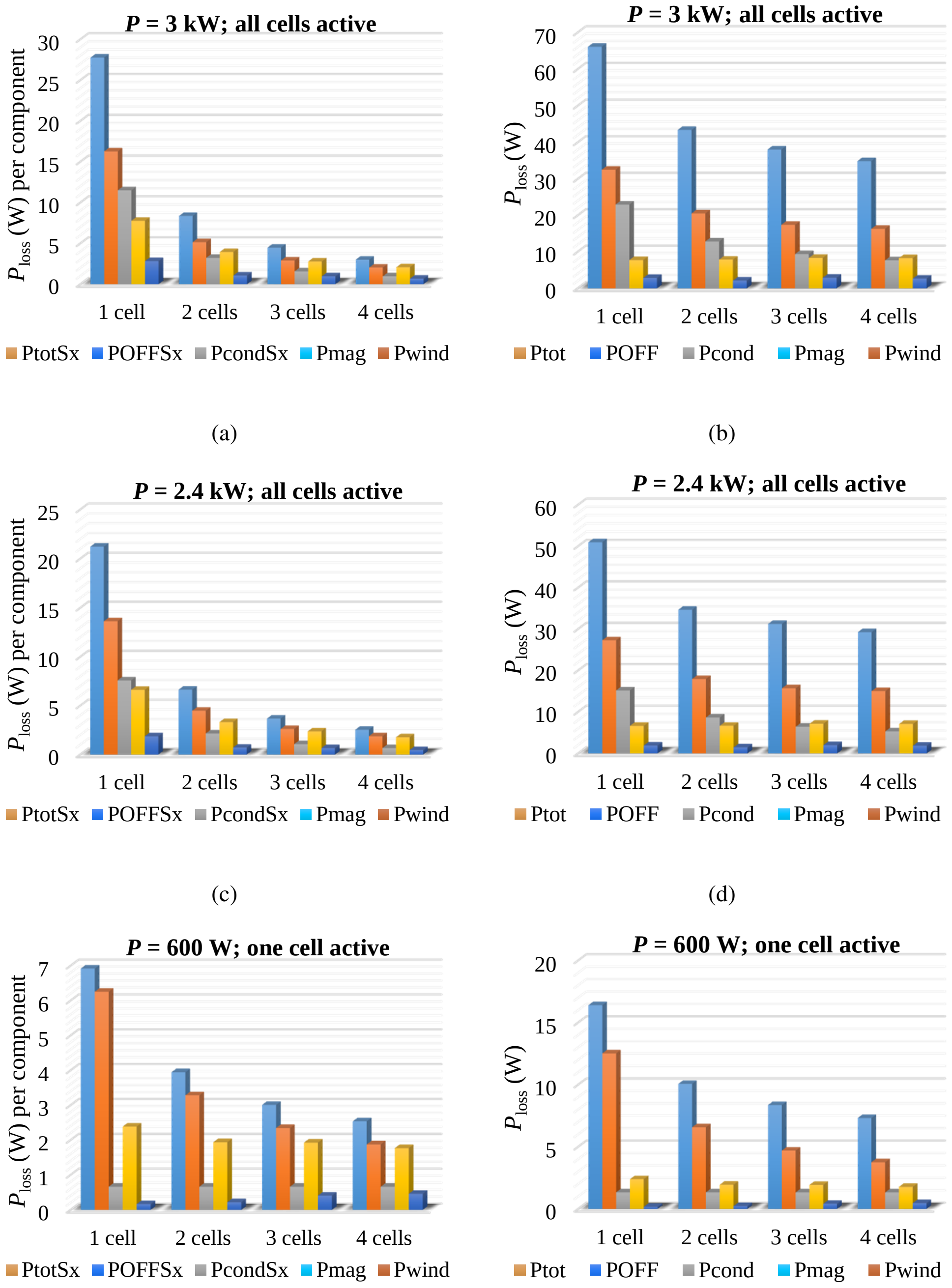
where n is the number of interleaved cells. A reversed current of $I_{\mathrm{R}} = -1.3$ A was selected for the purpose of this power loss and size analysis. It was also assumed that each combination of such reversed current and the required inductance L_{req} for $n = 1...4$ fulfills the ZVS capability criteria and thus eliminates the turn-on losses of all the transistors in HF-switched bridge legs.

For the sake of simplicity and a fairer comparison, all the inductors were designed with Magnetics' Molypermalloy (MPP) toroidal cores [127]. An iterative design procedure was used in which several different cores and configurations were analyzed. It was aimed towards the smallest achievable size and lowest power losses. One of the main design goals was also to achieve as much load-independent inductance as possible within the expected operating range of each inductor, which is essential for implementation of the DCM-based ZVS control. The best inductor configurations which were later used in the power loss and volume estimations for different numbers of interleaved cells ($n = 1...4$), are presented in Table 5.2. The information about the volume of each inductor V_{L} does not represent the volume of the inductor itself but the volume of a rectangular prism into which the inductor would fit.

While the power inductor had to be designed for each specific case due to different current ripples, rms currents, and required inductances, an identical HF-switched bridge leg consisting of the same power transistors and driving circuits can be used in the cases with up to 4 interleaved cells. The ST Microelectronics' STP25NM60ND [102] power MOSFETs in a TO-220 package were selected for performing the roles of the power transistors in the HF-switched leg. Their switching performance in a bridge structure under hard and soft switching conditions has been previously analyzed in Chapters 3 and 4. A typical volume of a half-bridge was estimated on the basis of experience with experimental converters utilizing bridge structures under operating conditions similar to the ones specified in Table 5.1. The typical half-bridge referred to in this case is a 600 V tolerant printed circuit board (PCB) design with isolated gate drivers and gate driver power supply, two TO-220 transistors, and switching cell decoupling capacitors. The volume of such a half-bridge V_{HB}, which is analogous to the volume of one HF-switched bridge leg, was estimated to $V_{\mathrm{HB}} = 31.92\,\mathrm{cm}^3$.

The charts in Fig. 5.2 provide a comparison of the generated power losses depending on the number of utilized interleaved cells. The presented results only consider the power losses generated within the interleaved cells, which represent the major part of the total power losses. Since the converter operates in DCM with an assumably sufficient magnitude of the reverse current which ensures ZVS, only turn-off losses and conduction losses will be generated in the transistors. The instantaneous turn-off losses of each MOSFET were estimated on the basis of turn-off energies within each switching period, which were calculated according to (3.3). In order to obtain the average turn-off losses over one AC voltage period, which are represented as POFFSx in Fig. 5.2, the obtained instantaneous values were numerically integrated and averaged over one ac-voltage period. The conduction losses PcondSx of one HF-switched bridge leg transistor were calculated on the basis of (3.10) by using numerical integration. The same approach was taken for the calculation of the inductor's winding losses Pwind in Figs. 5.2(a), (c), and (e), just that the resistance R_{dsonHF} in (3.10) was replaced by the winding resistance R_{L} of the inductor in each interleaved configuration. The magnetic core losses within an inductor in each interleaved configuration were calculated on the the basis of the magnetic core characteristics and loss parameters for MPP cores, provided in [128]. The parameter PtotSx was obtained as a sum of POFFSx and PcondSx and represents total power losses on each MOSFET. The parameters POFF, Pcond, Pmag, and Pwind in Figs. 5.2(b), (d), and (f) were obtained by multiplying the values in Figs. 5.2(a), (c), and (e) by the number of components within each interleaved configuration. The only exception is Ptot, which represents the average total power losses in one AC voltage period for each interleaved configuration and was obtained as a sum of POFF, Pcond, Pmag, and Pwind, shown in Figs. 5.2(b), (d), and (f).

It is evident from Figs. 5.2(a), (c), and (e), that the power losses per individual components



(a) (b)

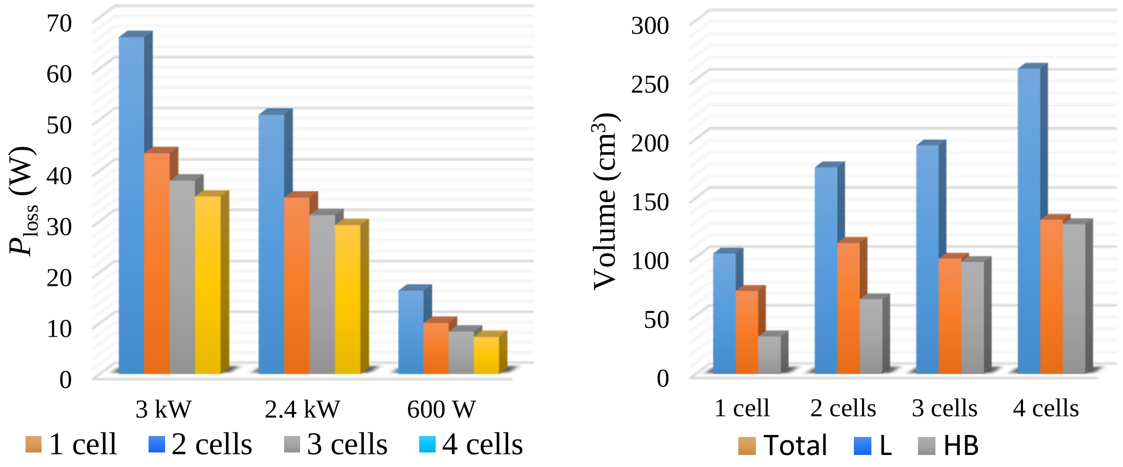
(c) (d)

(e) (f)

Figure 5.2: Average power losses over one ac-voltage period in respect to the number of utilized interleaved cells. The subfigures (a), (c), and (e) show the total losses (PtotSx), turn OFF losses (POFFSx), and conduction losses (PcondSx) per one MOSFET, and magnetic core (Pmag) and winding (Pwind) losses per one inductor. The subfigures (b), (d), and (f) show the total losses in all the interleaved cells (Ptot), which consist of total turn OFF (POFF), conduction (Pcond), magnetic core (Pmag), and winding (Pwind) losses.

are falling with increasing the number of interleaved cells. Since more cells result in more loss generating components, no final judgement can be made on the basis of losses per component. For evaluating each configuration, it is better to refer to the Figs. 5.2(b), (d), and (f), which show the cumulative losses of each configuration. It can be observed that the total magnetic core losses Pmag are maintained roughly at the same level in all cases. The same can be said for the total winding losses Pwind in Figs.(b) and (d). This is a reflection of the inductor design requirements and the iterative procedure for finding a trade-off between lowest volume and lowest loss configuration, the outcomes of which are listed in Table. 5.2. Since the same kind of transistors are used in all interleaved configurations, the conduction losses Pcond decrease when increasing the number of interleaved cells, which can be attributed to the current sharing between cells and quadratic dependence of conductive losses on the rms value of the current. The biggest absolute reduction in power losses is in all cases obtained through lower turn-off losses POFF. At the operating points presented in Figs. 5.2(b) and (d), where all the cells operate within approximately the same range of switching frequencies, the reduction in switching losses is achieved due to current sharing between individual cells and the resulting lower peak inductor current at the instants of turning OFF the transistors. A slightly different behavior of semiconductor losses is observed in Fig. 5.2(f) which presents the comparison of power losses for the 4 different interleaved configurations at the operating point in which only one cell is active in all configurations. In contrast to Figs. 5.2(b) and (d), the conduction losses Pcond are maintained roughly at the same level in all the cases. This is due to the absence of current sharing and usage of identical transistors with the same conductive properties. On the other hand, the turn-off losses POFF reduce with the number of interleaved cells although only one of them is active and all the transistors are switching the same current. The reason is in the fact that all configurations are designed to operate at the same $f_{\mathrm{sw,min1}}$ at the nominal operating point. As a consequence, the required size of inductance L_{req} grows with the number of interleaved cells. It can be inferred from (4.30), that the configuration with the highest inductance will operate with the lowest switching frequency under light load conditions, which leads to lower turn-off losses POFF. This is one of the main benefits of utilizing cell shedding in an interleaved DCM converter, since in case all the cells would be active under light load conditions, the operating switching frequency would be much higher. Nonetheless, the turn-off losses in configurations with more interleaved cells may still be lower due to current sharing between cells and the resulting lower peak current at which the transistors are turned OFF.

The average total power losses over an AC voltage period in the three observed operating points are gathered in Fig. 5.3(a) in order to provide a comparison between configurations that utilize



(a) (b)

Figure 5.3: Power loss and volume of configurations utilizing different number of interleaved cells. (a) Average power losses over an ac-voltage period in the three observed operating points. (b) Total volume (Vtotal) of each interleaved configuration as a sum of total volume of power inductors (VL) and HF-switched brdige legs (VHB).

different number of cells. The estimated total volumes (Vtot) of these configurations, consisting of the total volumes of utilized inductors (VL) and half-bridges (VHB), are provided in Fig. 5.3(b). The highest reduction in total power losses is observed when changing from single cell structure to 2 interleaved cells. This also yields a considerable increase in size as the still rather high current ripple in a 2 cell structure does not allow for usage of a significantly smaller inductor core. In addition, the DM EMI filtering requirements remain quite high in the case of 2 cell operation, which can be observed from a rather high input current ripple in Fig. 5.1(b). The reduction in power losses when going from 2 to 3 interleaved cells is not as significant as in the previous case, but still notable. A more advantageous feature of the 3 interleaved cell configuration is the almost negligible increase in volume, which is achieved due to the possibility of using smaller magnetic cores. In combination with significantly reduced DM EMI filtering requirements, resulting from the lower current ripple that can be observed in Fig. 5.1(c), a smaller size of the converter can be achieved than in the case of using 2 interleaved cells. Therefore 3 interleaved cells represent the most advantageous configuration among the four analyzed cases. In the case of using 4 interleaved cells the reduction in power losses is almost negligible, while the volume increases significantly. The reason for such increase in volume is the rather high required inductance of $L_{\mathrm{req}} = 103\ \mu\mathrm{H}$, which could not be realized for the desired operating range of currents with a core smaller than the ones used in the 3 cell configuration. There are some possibilities for reducing the size due to lower DM EMI filtering

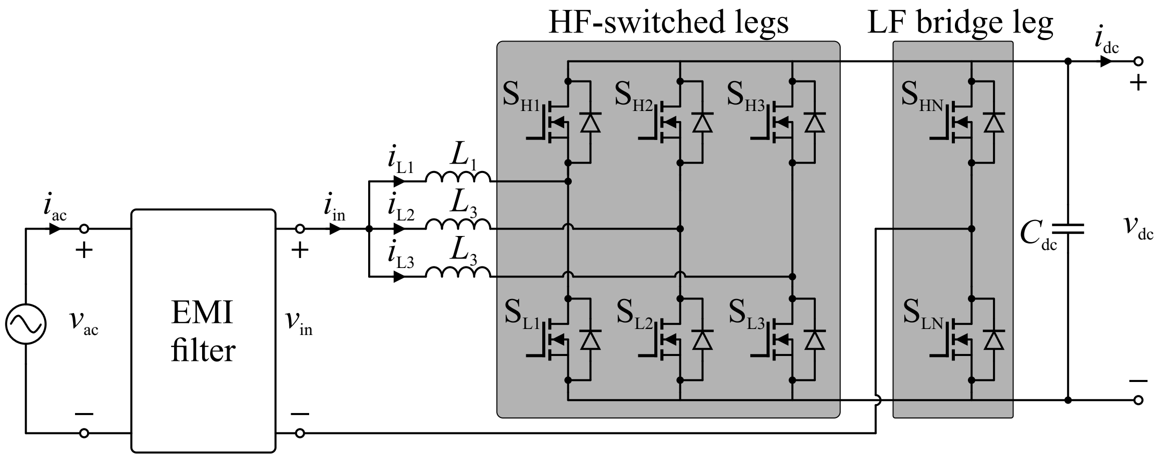


Figure 5.4: Bidirectional interleaved AC-DC converter.

requirements, but the total volume of the 4 cell configuration most probably cannot reach lower values than the volume of its 3 cell counterpart.

On the basis of the above presented analysis, a number of interleaved cells $n = 3$ was selected as the most suitable configuration for achieving the design goals specified in Table. 5.1. The schematic circuit of the selected interleaved AC-DC converter is presented in Fig. 5.4.

5.3 Component selection

The specifications listed in Table 5.1 have served as the basis for selecting the power circuit's components. An important additional design parameter is the number of interleaved cells $n = 3$, which has a strong influence on the design of inductors and selection of the components within the HF-switched bridge legs which form the interleaved cells. The power circuit's components to be selected are:

- power transistors S_{H1}, S_{L1}, S_{H2}, S_{L2}, S_{H3}, and S_{L3} in the HF-switched bridge legs and S_{HN}, and S_{LN} in the LF-switched bridge leg;
- power inductors L_1, L_2, and L_3;
- DC-side capacitor C_{dc}.

Initially, the transistors are selected, as their parasitic capacitances influence the required inductance of the power inductors which is selected in the next phase, according to the ZVS control design algorithm presented in Section 4.5. In addition to the required inductance, the reversed current I_{R}, and the maximum $T_{\mathrm{DT,max}}$ and minimum $T_{\mathrm{DT,min}}$ duration of the dead time are obtained from this algorithm, which gives the values of all the crucial parameters for ensuring ZVS in the entire operating range of the converter. Finally, the required DC-side capacitance for maintaining the DC voltage ripple within the specified limits is calculated and the DC-side capacitor bank configuration is presented. The remaining indefinite part of the interleaved DC-AC converter depicted in Fig. 5.4 is the EMI filter, the structure and design of which will be presented in the following chapter.

5.3.1 Transistors

For the voltage and current ranges specified in Table 5.1, power MOSFETs are the preferred and most common option in practice. The fundamental transistor selection criterion is the minimum required breakdown voltage $V_{\mathrm{DSS,min}}$, which consists of the maximum operating/blocking voltage $V_{\mathrm{dc,max}}$ and an additional safety margin. The maximum operating DC voltage $V_{\mathrm{dc,max}} = 440$ V is obtained by adding the maximum allowed value of the DC voltage ripple Δv_{DC} to the upper limit of the DC voltage operating range specified in Table 5.1. In order to ensure immunity to possible voltage overshoots during operation, an additional safety margin of 30 $\%$ of $V_{\mathrm{dc,max}}$ was considered. This resulted in a minimum required breakdown voltage of $V_{\mathrm{DSS,min}} = 572$ V, which made the power transistors with a breakdown voltage of $V_{\mathrm{DSS}} = 600$ V well suited for usage in the investigated converter.

The power transistors employed in the interleaved AC-DC converter shown in Fig. 5.4 can be classified into two groups. One group consists of the transistors S_{H1}, S_{L1}, S_{H2}, S_{L2}, S_{H3}, and S_{L3} in the HF-switched legs, while the other one is formed of the transistors S_{HN}, and S_{LN} in the LF-switched bridge leg. Except for the breakdown voltage requirement, there are different requirements for selecting the most suitable transistors for each group. Although the dominant turn-on losses are eliminated in all the transistors within the HF-switched bridge legs when operating in the DCM with a sufficient magnitude of the reversed current I_{R}, the remaining turn-off losses still contribute a significant portion to total power losses. For this reason, a good switching performance is of crucial importance for HF-switched transistors. The switching performance largely depends on the MOSFET's parasitic capacitances. These should not only be as low as possible for achieving low switching and gate driving losses, but also in the right proportions for providing high immunity to potential unwanted turn-on [73] at temporary hard switching commutations during load transients and start-up of the converter. It can be also inferred from the resonant voltage transition analysis in Section 4.1 that a smaller parasitic output capacitance C_{oss} results in a lower total charge Q_{tot} that has to be removed before a transistor can be turned ON at zero voltage. The most important thing when selecting the MOSFETs for the HF-switched bridge legs is to find a good balance between switching and conductive properties. In general, the MOSFETs with state-of-the-art switching characteristics come with worse conductive properties and vice versa. The minimum continuous drain current $I_{\mathrm{D,min}}$ that must be supported by each MOSFET in the HF-switched bridge legs is slightly higher than one third of the nominal AC current $I_{\mathrm{AC,nom}}$ specified in Table 5.1. This is due to the current sharing between the three interleaved cells when the converter is operating at high powers. For achieving low conduction losses it is desirable to aim for the transistors with continuous drain currents I_{D} of two to four times the maximum expected rms current. Such transistors come with a lower on-resistance $R_{\mathrm{ds,on}}$ and in most cases also lower junction-case thermal resistance $R_{\mathrm{thj-case}}$. The criteria for selecting the MOSFETs in the HF-switched bridge leg can be summarized in the following points:

- Low drain-source voltage dependent output capacitance $C_{\mathrm{oss}}(V_{\mathrm{DS}})$ which will result in a low equivalent capacitance C_{eq} and consequently loosened ZVS capability criteria (4.18);
- An internal body diode with a low reverse recovery charge Q_{rr} and short reverse recovery time t_{rr} that will allow for safe hard switching commutations that may occur during load transients and start-up of the converter;
- Low drain-source on-resistance $R_{\mathrm{ds,on}}$;
- Low junction-case thermal resistance $R_{\mathrm{thj-case}}$;
- Through-hole component package for facilitating natural convection cooling system design; TO-220 is the preferred package due to its small footprint as well as size in general;
- A low gate-source charge Q_{gs} for achieving low gate drive losses.

ST Microelectronics' STP25NM60ND [102] was selected as the power MOSFET to be used in the HF-switched bridge legs since it fulfills all the above-listed criteria. A detailed analysis of hard switching and resonant ZVS transitions when using such a MOSFET in a bridge structure has already been performed and presented in Chapters 3 and 4.

While the switching performance of the MOSFETs utilized in the HF-switched bridge legs is crucial, it is rather insignificant for the MOSFETs in the LF-switched bridge leg. The latter are being switched only twice per each AC voltage period and even in those cases, the current they have to switch is in the vicinity of zero. Therefore the switching losses generated on S_{HN}, and S_{LN} are negligible and their switching performance not a primary selection criteria. On the other hand, their conductive properties are of crucial importance. Each transistor in the LF-switched bridge leg has to support the entire AC current during each AC voltage half-period, which leads to a minimum continuous drain current of $I_{\mathrm{D,min}} \approx I_{\mathrm{ac,nom}}/2 = 6.5\ \mathrm{A_{rms}}$. In the absence of demanding switching performance requirements, the selection of the LF-switched bridge leg MOSFETs is based on finding the lowest drain-source on-resistance $R_{\mathrm{ds,on}}$ in the specified package. Of course some minor attention has to be paid to the switching characteristics as well, after all the devices will be used in a bridge structure under hard switching conditions at a rather high blocking voltage. By aiming for the best conductive properties, the ST Microelectronics' STW88N65M5 [129] have been selected for the LF-switched bridge leg due to the best drain-source on-resistance $R_{\mathrm{ds,on}}$ available in TO-247 package and decent switching performance.

The procedure for calculating the MOSFET's switching and conduction losses when utilized in a DCM-based ZVS DC-AC converter is presented in Appendix A. The information about the semiconductor losses will be required in one of the following design phases, in which the employment of the cell shedding strategy will be investigated.

5.3.2 Power Inductors and ZVS control parameters

The importance of the power inductor's inductance L on achieving ZVS and its influence on the minimum required magnitude of the reversed current I_{R} and the duration of the resonant switching transition T_{res} has been explained in Chapter 4. For facilitating the selection of such a combination of inductance L, reversed current I_{R}, and dead time duration T_{DT} that will ensure reliable ZVTs in the entire operating range of a converter utilizing transistors in a bridge structure, a ZVS control design procedure was developed. Its final form, adapted for usage in a hybrid-modulated H-bridge based DC-AC converter is summarized in the flowchart presented in Fig. 4.20. Although the procedure was developed for a non-interleaved converter, it can be directly applied for designing one interleaved cell of the interleaved DC-AC converter shown in Fig. 5.4. When operating at the nominal power, all the available interleaved cells will be active and the total AC current will be equally distributed among the cells. Therefore, each interleaved cell must be designed for one third of the nominal operating power P_{nom}. For ensuring equal distribution of the current among the cells, the cells must be identical and the converter design as symmetrical as possible. One of the fundamental conditions for achieving that is the same inductance L of the inductors L_1, L_2, and L_3.

5.3.2.1 ZVS control design procedure

The required inductance L, reversed current magnitude I_{R}, and dead time duration T_{DT} for ensuring ZVS in the DCM were determined by following the control design procedure presented in Fig. 4.20. Initially, the desirable operating parameters of the converter had to be specified. The maximum DC voltage $V_{\mathrm{dc,max}}$ has been specified as $V_{\mathrm{dc,max}} = 440$ V, which would appear in the case of operating

Table 5.3: Parameters specified in step 1) of the ZVS control design procedure.

Symbol	$V_{\mathrm{dc,max}}$	$\hat{V}_{\mathrm{ac}}$	$\hat{I}_{\mathrm{Lavg,max}}$	$\hat{I}_{\mathrm{Lavg,min}}$	$f_{\mathrm{sw,min}}$	$f_{\mathrm{sw,max}}$	$T_{\mathrm{res,max}}$
Value	440 V	325 V	6.15 A	0.615 A	25 kHz	400 kHz	200 ns

at upper limit of the dc-voltage range, specified in Table 5.1, with a maximum allowed DC voltage ripple Δv_{DC}. The peak ac-side voltage $\hat{V}_{\mathrm{ac}}$ was specified as $\hat{V}_{\mathrm{ac}} = \sqrt{2}V_{\mathrm{ac,nom}} \approx 325\mathrm{V}$. The latter is not critical in terms of ZVS capability, since the most demanding operating condition for achieving ZVS occurs at $v_{ac} = 0$. However, the peak AC-voltage is involved in the construction of the ZVS control design surfaces and calculation of the switching frequency f_{sw}, and the resonant transition duration T_{res}. The peak value of the average inductor current $\hat{I}_{\mathrm{Lavg,max}}$ at the maximum operating power has been specified as

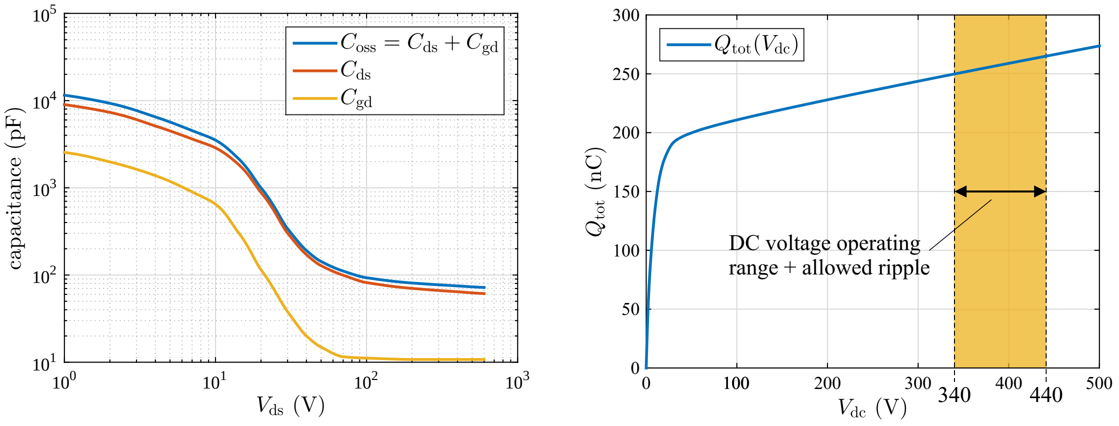
$$\hat{I}_{\mathrm{Lavg,max}} = \frac{1}{3}\sqrt{2}\,I_{\mathrm{ac,nom}} = 6.13\ \mathrm{A}, \tag{5.2}$$

where it was assumed that all the interleaved cells are active and the AC-current is equally distributed among them. For the purpose of specifying the peak value of the average inductor current $\hat{I}_{\mathrm{Lavg,min}}$ at the minimum operating power P_{min}, the latter was arbitrary selected as $P_{\mathrm{min}} = 100\ \mathrm{W}$, which accounts for approximately 3.3 $\%$ of P_{nom}. The minimum operating power represents the minimum power at which the converter should operate in DCM with the selected magnitude of the reversed current I_{R}. Beyond this point, approaches like pulse skipping [106, 130] for improving the light load efficiency can be employed. However, efficiency under extremely light load conditions exceeds the scope of this thesis and therefore the performance of the converter under the minimum operating power P_{min} will not be further discussed. On the basis of the just-defined minimum operating power P_{min} and assuming that cell shedding functionality is employed and consequently only one cell of the interleaved converter is active at P_{min}, the minimum peak value of the average inductor current $\hat{I}_{\mathrm{Lavg,min}}$ has been specified as

$$\hat{I}_{\mathrm{Lavg,min}} = \sqrt{2}\frac{P_{\mathrm{min}}}{V_{\mathrm{ac,nom}}} = 0.615\ \mathrm{A}. \tag{5.3}$$

The absolute minimum switching frequency has been defined as $f_{\mathrm{sw,min}} = 25\ \mathrm{kHz}$ and the maximum allowed switching frequency as $f_{\mathrm{sw,max}} = 400\,\mathrm{kHz}$. The maximum allowed duration of a resonant switching transition $T_{\mathrm{res,max}}$ at the switching frequency $f_{\mathrm{sw,max}}$ has been specified as $T_{\mathrm{res,max}} = 200\ \mathrm{ns}$. For providing a better overview, the values of the parameters specified in the first step are listed in Table 5.3.

Step 2) demands selection of the power MOSFETs for the HF-switched bridge leg. As explained in the previous subsection, ST Microelectronics' STP25NM60ND power MOSFETs with

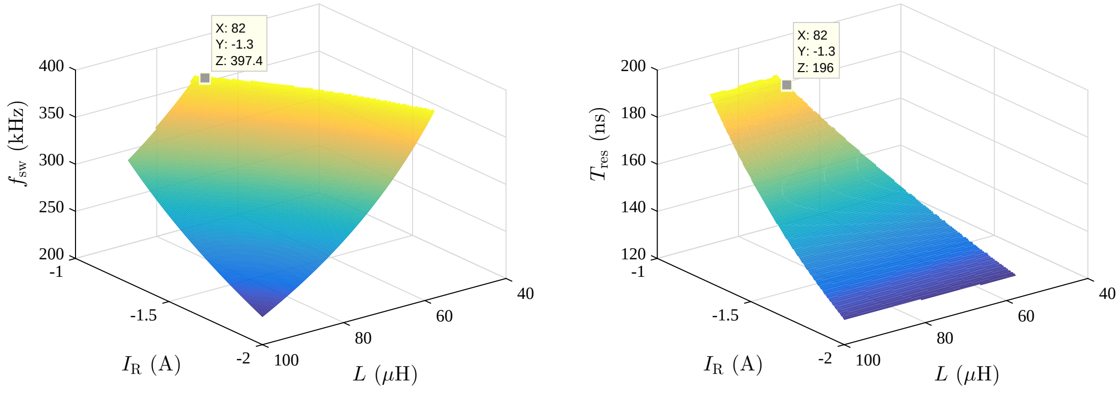


(a) (b)

Figure 5.5: (a) Non-linear voltage dependent parasitic capacitances of an STP25NM60ND MOSFET: parasitic output capacitance C_{oss} provided in the datasheet, drain-source parasitic capacitance C_{ds}, and gate-drain parasitic capacitance C_{gd}. (b) Total gate charge Q_{tot} in respect to the operating DC voltage: linear function with a low rate of change in the expected DC voltage operating range of the investigated converter.

a fast recovery diode were selected. In the following step 3), the total gate charge Q_{tot} and the equivalent capacitance C_{eq} have to be calculated for the two paralleled transistors within a bridge leg at the maximum DC voltage $V_{\mathrm{dc,max}}$. By replacing V_{A} with $V_{\mathrm{dc,max}}$ in (4.6) and (4.7), the two parameters were obtained as $Q_{\mathrm{tot}} = 264.8\,\mathrm{nC}$ and $C_{\mathrm{eq}} = 602\mathrm{pF}$ for the most critical operating point determined by $V_{\mathrm{dc,max}}$. It can be seen from Fig. 5.5(b) that the total gate charge Q_{tot} does not vary significantly within the DC voltage range specified in Table 5.1. The reason for this is evident from Fig. 5.5(a), which shows the parasitic output capacitance C_{oss} and its constituting components C_{ds} and C_{gd} in respect to the voltage V_{ds} applied across the drain and source terminals of the MOSFET. The drain-source voltage V_{ds} corresponds with the voltage V_{dc} applied across a bridge leg of the converter. At voltages higher than 100 V, the parasitic capacitance characteristics become almost flat at very low capacitances. This is reflected in a rather constant and gradual slope of the total gate charge Q_{tot} characteristic at voltages above 100 V. The latter is beneficial for the DCM-based ZVS since resonant switching transitions of a similar duration T_{res} can be expected within the entire operating range of DC-voltages.

Since the instant t_{max} in which the operating switching frequency f_{sw} reaches its maximum varies with the selected I_{R}, an initial value I_{Rinit} of the reversed current has to be selected in step 4). The initially selected value does not influence the final selection of inductance L and I_R in any way. However, selecting a realistic value of I_{Rinit} reduces the number of required iterations for



(a) (b)

Figure 5.6: Reduced ZVS design surfaces at the instant t_{max} depicting the combinations of L and I_{R} that satisfy the criteria (4.32a), (4.32b), and (4.32c). (a) $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$. (b) $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$.

satisfying the condition “D1”.

By following the design procedure between steps 5) and 9), the inductance of $L = 82\ \mu\mathrm{H}$ and a reverse current magnitude of $I_{\mathrm{R}} = -1.3$ A have been selected. This selection represents a combination of the minimum inductance L at a nearly minimum magnitude of the reversed current I_{R} that fulfills all the criteria within decision blocks D2 and D3. The final ZVS design surfaces $f_{\mathrm{sw}} = f(I_{\mathrm{R}}, L)$ and $T_{\mathrm{res}} = f(I_{\mathrm{R}}, L)$ at the instant t_{max}, reduced to the surface within the limits determined by (4.32a), (4.32b), and (4.32c) are shown in Fig. 5.6. The location of the selected combination of L and I_{R} within the surface of possible solutions indicates that the selection process was directed towards simultaneous minimization of both the inductance L and the reversed current I_{R}. Such strategy was employed under the assumptions that a lower value of inductance L allows for designing an inductor with a lower volume and that a lower magnitude of I_{R} alleviates the magnetic core and total conduction losses. The actual influence of the inductance L and the reversed current magnitude I_{R} on the maximum achievable efficiency and power density has not been studied within this thesis, but it certainly represents an interesting topic for further investigation and a challenge for the future.

Since the selected combination of L and I_{R} results in a switching frequency $f_{\mathrm{sw}}(\hat{I}_{\mathrm{Lavg,max}}) = 49.7\ \mathrm{kHz}$ at the nominal operating point, the condition specified within the decision block D2 in Fig. 4.20 is satisfied, which leads to the final step 9) of the ZVS control design procedure. The minimum $T_{\mathrm{DT,min}}$ and maximum $T_{\mathrm{DT,max}}$ dead time durations for ensuring reliable ZVTs within the entire operating range of the converter are determined within this step. Both, $T_{\mathrm{DT,min}}$ and $T_{\mathrm{DT,max}}$

Table 5.4: Required inductance and ZVS control parameters.

Description	**Symbol**	**Value**
Required inductance	L	82 μH
Required magnitude of the reversed current	I_{R}	-1.3 A
Minimum required dead time duration	$T_{\mathrm{DT,min}}$	63 ns
Maximum allowed dead time duration	$T_{\mathrm{DT,max}}$	159 ns

are determined for the operating condition in which the duration of the switching transition T_{res} is the longest. This gives the largest $T_{\mathrm{DT,min}}$ and the smallest $T_{\mathrm{DT,max}}$, which are considered safe dead time duration limits for the entire operating range of the converter. The duration of the switching transition will be the longest at the zero crossing of AC voltage when $v_{\mathrm{ac}} = 0$. On the basis of (4.10) and (4.11)[1], the duration of the resonant switching transition T_{res} at $v_{\mathrm{ac}} = 0$ is obtained as $T_{\mathrm{res}} = 257.76\,\mathrm{ns}$, while the inductor current $i_{\mathrm{L}}(t_{\mathrm{res}})$ at the end of the main transition period is obtained as $i_{\mathrm{L}}(t_{\mathrm{res}}) = -0.519$ A. By inserting these values into (4.21) and defining $\min(D_{\mathrm{buck}}, D_{\mathrm{boost}}) = \min(v_{\mathrm{ac}}/v_{\mathrm{dc}}, 1 - v_{\mathrm{ac}}/v_{\mathrm{dc}}) = 0$, the minimum duration of the interval labeled T_{zc} in Fig. 4.3 is calculated as $T_{\mathrm{zc,min}} = 96.68\mathrm{ns}$. As has been explained in Subsection 4.2.2, the delays $T_{\mathrm{off,delay}}$ and $T_{\mathrm{on,delay}}$ are practically independent of the operating point since the relevant turn OFF instants always occur at the predetermined value of the reversed current I_{R} and the turn-on instants in its vicinity. A series of experiments has been carried out for measuring the delays $T_{\mathrm{off,delay}}$ and $T_{\mathrm{on,delay}}$. Their average values have been obtained as $T_{\mathrm{on,delay}} = 240$ ns and $T_{\mathrm{off,delay}} = 45$ ns. Finally, the minimum $T_{\mathrm{DT,min}}$ and maximum $T_{\mathrm{DT,max}}$ dead time durations for ensuring reliable ZVTs within the entire operating range of the converter are calculated according to (4.19) and (4.20) as

$$T_{\mathrm{DT,min}} = T_{\mathrm{off,delay}} + T_{\mathrm{res}} - T_{\mathrm{on,delay}} = 45 + 257.76 - 240 \approx 63\mathrm{ns}, \tag{5.4a}$$

$$T_{\mathrm{DT,max}} = T_{\mathrm{off,delay}} + T_{\mathrm{res}} + T_{\mathrm{zc,min}} - T_{\mathrm{on,delay}} = 45 + 257.76 + 96.68 - 240 \approx 159\mathrm{ns}. \tag{5.4b}$$

The required inductance L and the ZVS control parameters that will ensure the desirable ZVS of the investigated AC-DC converter over its entire operating range are summarized in Table 5.4.

5.3.2.2 Inductor Design

In addition to the required inductance L_{req}, the power inductor has to be designed to achieve:

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[1] The voltage V_{A} in equations derived for the bidirectional DC-DC converter is analogous to voltage v_{dc} in the discussed bidirectional DC-AC converter, while the voltage V_{B} is analogous to the voltage v_{ac}.

- low power losses,
- low volume, and
- high stability of inductance L within the entire operating range.

The requirements for low power losses and low volume originate from the investigated converter's specifications and design objectives, which demand high power conversion efficiency and high power density. High stability of inductance over the entire operating range is crucial for maintaining ZVS capability and it also facilitates digital implementation of the DCM-based ZVS control. The stability of inductance can be represented as the ratio between the minimum inductance L_{min}, which occurs at the maximum expected inductor current i_{Lmax}, and the initial (no-load) inductance L_{i}. In the discussed case, the inductance stability criterion is defined as

$$\frac{L_{\mathrm{min}}}{L_{\mathrm{i}}} \geq 0.9. \tag{5.5}$$

In order to meet the above specified design requirements, Magnetics' MPP toroidal cores with a distributed air gap from the producer Magnetics were selected for designing the inductors. MPP cores offer very low core losses, a wide range of operating temperatures, high inductance stability in respect to the applied current and frequency independent permeability within the expected range of operating switching frequencies [127]. Toroidal cores are known for causing among the lowest radiated EMI of all the existing core shapes [131]. Due to the their geometry, the majority of magnetic flux is kept within the core boundaries and as a result, the stray magnetic field is insignificant. The large surface area of a toroidal structure provides good cooling properties. These are of high importance in the discussed DCM application, in which considerable core losses are expected due to the high inductor current ripple. The heat removal capability is best when utilizing a single layer winding. A single layer winding also allows for achieving a low self-capacitance and a high self-resonant frequency of the inductor. The latter are desirable for alleviating the influence of the power inductor's parasitic capacitances on resonant switching transitions. Therefore, only inductor configurations with single layer windings will be considered for usage in the investigated interleaved DC-AC converter.

In the initial design phase, the required number of turns N for achieving the required inductance L_{req} was calculated for a specific MPP toroidal core as

$$N = \mathrm{ceil}\left(\sqrt{\frac{L_{\mathrm{req}}}{A_{\mathrm{L}}}}\right), \tag{5.6}$$

where ceil represents the round-up operation and A_{L} the specific inductance of a core, which is provided in the datasheet for each core. The specific inductance A_{L} carries the information about the core's dimensions and the magnetic permeability of the core's material, and is defined as

$$A_{\mathrm{L}} = \frac{\mu_{\mathrm{r}}\,\mu_0\,A_{\mathrm{c}}}{l_{\mathrm{c}}}, \tag{5.7}$$

where μ_{r} is the relative permeability of the material, μ_0 the permeability of free space, A_{c} the cross sectional area of the core, and l_{c} the magnetic path/core length. Due to the round-up operation in (5.6), the actual initial inductance L_{i} under no load conditions is in most cases slightly higher than the required inductance L_{req} and is calculated by rearranging the equation (5.6) and finally inserting (5.7) as

$$L_{\mathrm{i}} = N^2 A_{\mathrm{L}} = N^2 \mu_{\mathrm{i}}\,\mu_0 \frac{A_{\mathrm{c}}}{l_{\mathrm{c}}}, \tag{5.8}$$

where μ_{i} is the initial relative permeability of the core under no load conditions. The relative permeability of the core depends on the magnetic field intensity H, which is proportional to the current i_{L} flowing through the winding of the inductor. An increase in the current results in increased magnetic field intensity, which causes a drop in relative permeability and consequently a decreased inductance. It is evident from (5.8) that the inductance of a specific core with a fixed number of turns depends exclusively on the relative permeability of the core's material. Therefore it is possible to directly translate the inductance stability criterion (5.5) into permeability stability criterion as

$$\frac{\mu_{\mathrm{min}}}{\mu_{\mathrm{i}}} \geq 0.9, \tag{5.9}$$

where μ_{min} is the minimum permeability which is reached at the maximum expected inductor current i_{Lmax}. In order to satisfy this condition, the inductor must be designed such that the maximum magnetic field intensity H_{max} resulting from the maximum expected inductor current i_{Lmax} does not push the minimum permeability μ_{min} below 90 $\%$ of the initial value μ_{i}. The maximum magnetic field intensity H_{max} can be calculated as

$$H_{\mathrm{max}} = \frac{N\,i_{\mathrm{Lmax}}}{l_{\mathrm{c}}}. \tag{5.10}$$

In the discussed case, the maximum inductor current equals $i_{\mathrm{Lmax}} = 13.6\mathrm{A}$. The producer Magnetics provides information about permeability reduction in respect to the applied magnetic field intensity for the MPP toroids in the form of a polynomial curve fit equation

$$\frac{\mu_{\mathrm{min}}}{\mu_{\mathrm{i}}} = \mathrm{a} + \mathrm{b}\,H_{\mathrm{max}} + \mathrm{c}\,H_{\mathrm{max}}^2 + d\,H_{\mathrm{max}}^3 + \mathrm{e}\,H_{\mathrm{max}}^4, \tag{5.11}$$

where a, b, c, d, and e are the coefficients for each permeability class, listed in [128]. The calculation of the permeability roll-off according to (5.11) and verification of compliance with the limit

Table 5.5: Wire sizes considered for designing the inductors.

AWG No.	Bare Diameter d_w (mm)	Outer Diameter d_wo2 (mm)	Bare Cross-Sectional Area A_w (mm^2)	DC Resistance @ 20 °C R_dc (mΩ/m)
14	1.63	1.74	2.09	8.3
15	1.45	1.56	1.65	10.4
16	1.29	1.39	1.31	13.2
17	1.15	1.25	1.04	16.6
18	1.02	1.12	0.82	21.1
19	0.912	1.00	0.65	26.4

(5.9) represents the first selection process, in which all the cores that do not provide sufficient permeability stability are eliminated. The next selection process is based on the possibility for realizing the required number of turns N in a single layer winding.

Single-conductor copper wire with polymer coating that provides Grade 2 insulation in sizes ranging from 14 AWG to 19 AWG was considered. Detailed information about each wire's dimensions and DC resistances per unit of length are given in Table. 5.5. The maximum number of turns N_max that can be fitted in the form of a single-layer winding on a specific toroidal core can be calculated as

$$N_\mathrm{max} = \mathrm{floor}\left(\frac{\pi d_\mathrm{ID} - l_\mathrm{clear}}{d_\mathrm{wo2}}\right), \tag{5.12}$$

where floor represents the round-down operation and d_ID is the inner diameter of the core, d_wo2 the outer diameter of the wire, and l_clear the clearance distance between the first and the last turn of the winding. In the presented case, a clearance distance of $l_\mathrm{clear} = 2\ \mathrm{mm}$ was used. In order to minimize the winding losses, a wire is selected with the highest cross-sectional area which allows realization of the required number of turns N in a single-layer winding. In case the highest number of turns N_max on a specific core is smaller than the required number of turns N for all sizes of wires listed in Table 5.5, this core is eliminated from further design procedure as the single-layer winding criteria cannot be satisfied.

The mean length of a turn MLT for single layer winding is provided in the datasheet for each core. It can also be easily calculated from the core dimensions. The DC resistance of the winding R_Ldc is determined as

$$R_\mathrm{Ldc} = N\,\mathrm{MLT}\,R_\mathrm{dc} + l_\mathrm{term}, \tag{5.13}$$

where R_{dc} is the DC resistance of the selected wire per unit of length, given in Table 5.5, and l_{term} the additional length of the wire for winding terminations. Although the contribution of the latter to the total DC resistance of the winding is in most cases negligible, it was considered as $l_{\mathrm{term}} = 40\ \mathrm{mm}$ in the presented case.

Once the wire for winding is selected, the total boxed volume of the inductor can be determined. The total boxed volume of the inductor represents the volume of a rectangular prism which could encompass the inductor. The usage of the inductor's boxed volume is preferred to usage of the actual volume when designing power electronics converters since it provides better information about the space that will be occupied by the inductor within the circuit and is a more appropriate measure for comparison with other core shapes. The boxed volume of single-layer wound MPP toroids analyzed within this thesis is given as

$$V_{\mathrm{box}} = (d_{\mathrm{OD}} + 2d_{\mathrm{wo2}})^2 (h + 2d_{\mathrm{wo2}}), \tag{5.14}$$

where d_{OD} is the outer core diameter and h the height of the core.

A set of MPP toroid-based inductor configurations is obtained by following the above described procedure. Detailed information for each configuration is provided in Table 5.6. All these inductors achieve the required initial inductance L_{i}, provide a sufficient inductance stability, and are wound with a single layer winding with a minimum DC resistance R_{Ldc} that can be achieved by using the wires listed in Table 5.5. Although any of these inductors could be used in the investigated interleaved DC-AC converter for ensuring the desirable ZVS operation in the DCM, it is desirable to find the combination that offers the lowest power losses with the smallest possible indctor size, and a stable inductance within the entire operating range of the converter. In order to obtain all the required information for selecting the best configuration, a power loss analysis for each inductor configuration has been made. The analysis focused on estimating the winding and core losses at the nominal operating point of the investigated DCM operated DC-AC converter. The approach for their estimation is explained in Appendix A, while the estimated total power losses P_{tot} for each inductor configuration at the nominal operating power are given in Table. 5.6. Together with the total boxed volume V_{box}, and the inductance stability ratio $\frac{L_{\mathrm{min}}}{L_{\mathrm{i}}}$, they form a set of criteria for selecting the most suitable inductor configuration.

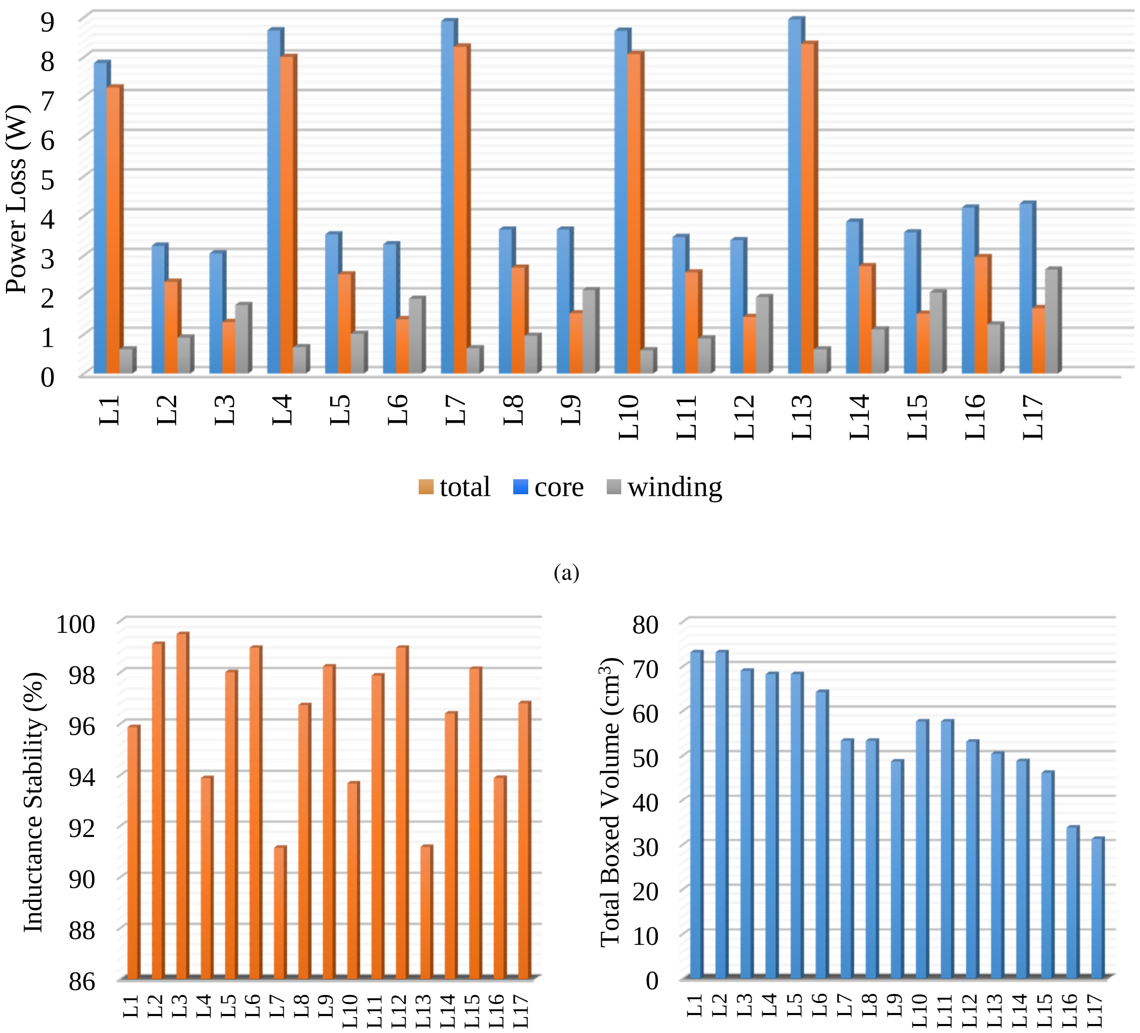
A comparison between the possible inductor configurations by each criteria is provided in Fig. 5.7. It can be observed in Fig. 5.7(a) that several configurations stand out in terms of total power losses. An extremely high share of magnetic core losses in these cases indicates that the cores used in configurations L1, L4, L7, L10, and L13 may not be suitable for usage in the investigated application. In addition, these configurations also provide among the lowest inductance

Table 5.6: Inductor configurations with a single layer winding and inductance stability ratio higher than 0.9.

Design.	Core #	N	L_i (μH)	$\frac{L_\mathrm{min}}{L_\mathrm{i}}$	AWG #	R_Ldc (mΩ)	V_box (cm^3)	P_tot (W)
L1	55192-A2	25	86.3	0.959	14	13.6	73.12	7.84
L2	55191-A2	37	82.1	0.991	14	20.0	73.12	3.24
L3	55190-A2	51	83.2	0.995	16	43.9	69.01	3.05
L4	55110-A2	33	81.7	0.939	14	14.6	68.24	8.67
L5	55111-A2	50	82.5	0.980	14	22.1	68.24	3.53
L6	55112-A2	68	83.2	0.990	16	47.9	64.24	3.28
L7	55716-A2	34	84.4	0.912	14	14.1	53.32	8.90
L8	55717-A2	51	83.2	0.967	14	21.1	53.32	3.65
L9	55718-A2	70	83.3	0.982	17	57.9	48.68	3.65
L10	55439-A2	25	84.4	0.937	14	13.0	57.65	8.66
L11	55440-A2	38	85.2	0.979	14	19.7	57.65	3.46
L12	55441-A2	51	83.2	0.990	17	53.1	53.10	3.38
L13	55090-A2	31	82.6	0.912	14	13.5	50.40	8.95
L14	55091-A2	48	85.2	0.964	15	26.4	48.77	3.85
L15	55092-A2	65	84.5	0.981	17	56.6	46.12	3.58
L16	55256-A2	49	84.0	0.939	16	31.5	33.79	4.21
L17	55257-A2	66	82.8	0.968	19	84.6	31.25	4.30

stability and are among the largest in size, as evident from Figs. 5.7(b) and 5.7(c). On the other hand, the remainder of the configurations generate a similar amount of total power losses, with L3 being the most efficient. Although L3 also provides the highest inductance stability, it may not be the best option since its volume is more than twice the volume of the smallest configurations L16 and L17.

The fact that there is no ultimate configuration which would be the best or at least among the best in all aspects calls for finding an overall best configuration. This can be done on the basis of the weighted average in which the importance of each criteria for final application is taken into account. The weighted average will consist of three components, which will reflect the total power losses, total boxed volume and inductance stability of a specific inductor configuration. Initially, the valuations of all the criteria have to be unified, which means that the same scale has to be used for measuring the power losses, volume and inductance stability. This is done by mapping the



(a)

(b)

(c)

Figure 5.7: Comparison between individual inductor configurations L1- L17 by (a) power losses, (b) inductance stability, and (c) total boxed volume.

values of P_{tot}, V_{box}, and $L_{\mathrm{min}}/L_{\mathrm{i}}$ onto a scale from 0 to 100, where 100 represents the best value in each category and 0 the worst value. The selected best and worse values for each criteria are listed in Table 5.7. Once different criteria have been mapped onto the same scale, a direct and fair comparison between them is possible. However, not all the criteria in the discussed case have the same importance. Therefore weights have to be assigned to each of them.

It was initially estimated that an inductance stability ratio higher than 0.9 is required for ensuring proper operation of the system. Since all the inductor configurations in Table 5.6 satisfy this criteria, they generally provide a good inductance stability. On the other hand, the total power losses P_{tot} and the boxed volume V_{box} represent very important parameters that affect the power conversion efficiency and power density of the investigated converter, but have not been the subject of any

Table 5.7: Evaluation and weighting of the selection criteria.

Criteria	Total Power Loss P_{tot}	Total Boxed Volume V_{box}	Inductance Stability Ratio $\frac{L_{\mathrm{min}}}{L_{\mathrm{i}}}$
best	3	30	1
worst	9	75	0.9
weights	0.4	0.4	0.2

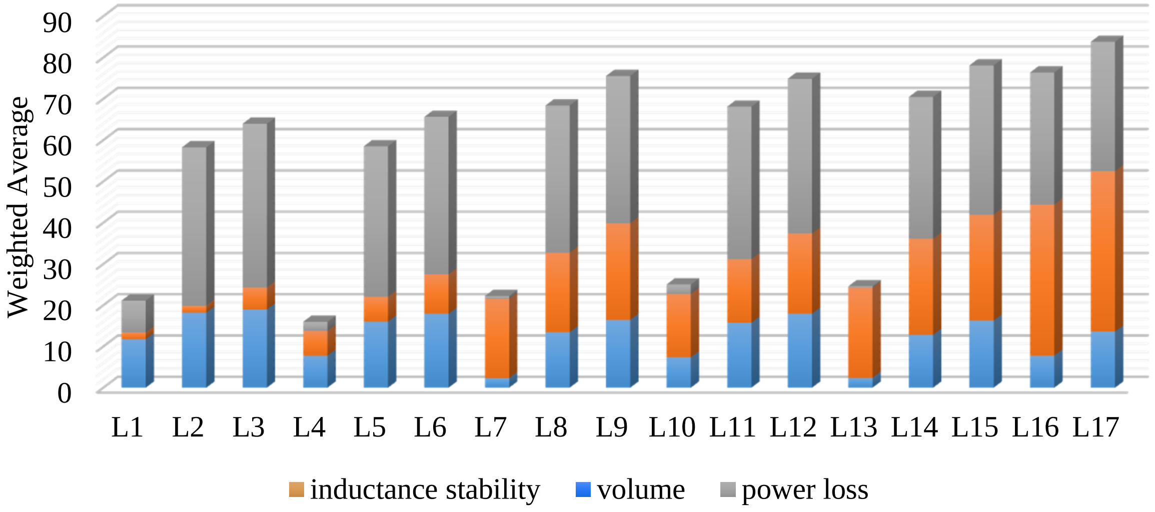


Figure 5.8: Weighted average of the analyzed inductor configurations.

previous selection process. Therefore, higher importance will be given to these two criteria when calculating the weighted average of each inductor configuration. The weights assigned to each criteria for obtaining the weighted average are listed in the bottom row of Table 5.7, while the final scores for each inductor configuration are shown in Fig. 5.8. It turned out that the configurations L15, L16, and L17 represent the overall better solutions. They are the smallest in size, generate rather low power losses, and provide a decent inductance stability. Since the cores for configurations L17 and L15, which are the first and second ranked options, were not available at the time of building the interleaved DC-AC converter's prototype, the inductor configuration L16 was selected. In comparison with the highest ranked configuration L17, L16 exhibits a slightly worse inductance stability and a somewhat larger volume. Since the cores of L16 and L17 are of the same size, the difference in volume is exclusively due to the usage of a thicker copper wire for realizing the winding in the case of L16. The larger volume is to some extent compensated with significantly reduced winding losses and somewhat lower total power losses.

5.3.3 DC-side capacitor

The DC-side capacitor C_{dc} represents an interface between the AC-side and the DC-side of the interleaved DC-AC converter shown in Fig. 5.4. Its primary task is to maintain balance between the fluctuating AC power and the quasi constant DC power. When the instantaneous AC power is higher than the instantaneous DC power, the excessive energy is stored into the capacitor. This energy is later used for supplying the load, when the relation between the instantaneous AC and DC powers is reversed. As a result of this process, a stable and almost constant DC voltage v_{dc} is obtained on the DC-side of the converter. Nonetheless, the level of the remaining LF ripple in the DC voltage largely depends on the utilized capacitor C_{dc}. For maintaining the DC voltage ripple Δv_{dc} within the specified limits, the capacitance of the DC-side capacitor C_{dc} must be carefully selected.

By assuming that the interleaved AC-DC converter operates as a PFC rectifier with a perfectly controlled input current i_{ac}, the instantaneous AC power $p_{\mathrm{ac}}(t)$ can be written as

$$p_{\mathrm{ac}}(t) = v_{\mathrm{ac}}(t)\, i_{\mathrm{ac}}(t) = \hat{V}_{\mathrm{ac}} \sin(\omega t)\ \hat{I}_{\mathrm{ac}} \sin(\omega t) = \frac{\hat{V}_{\mathrm{ac}}\, \hat{I}_{\mathrm{ac}}}{2} \left(1 - \cos(2\,\omega\, t)\right). \tag{5.15}$$

Since a high power conversion efficiency is expected for the investigated converter, the EMI filter and the switching stage losses can be neglected and the instantaneous output power $p_{\mathrm{o}}(t)$ can be considered as

$$p_{\mathrm{out}}(t) = i_{\mathrm{out}}(t)\, v_{\mathrm{dc}}(t) \approx p_{\mathrm{ac}}(t), \tag{5.16}$$

where $i_{\mathrm{out}}(t)$ is the current flowing from the AC-DC stage towards the output of the converter, as designated in Fig. 5.9. The output voltage can be written as

$$v_{\mathrm{dc}}(t) = V_{\mathrm{dc}} + v_{\mathrm{ripple}}(t), \tag{5.17}$$

where V_{dc} is the DC component of the output voltage and $v_{\mathrm{ripple}}(t)$ the ripple in the output voltage. By neglecting the presence of ripple $v_{\mathrm{ripple}}(t)$ in (5.17) and substituting it together with (5.16) into (5.15), the output current $i_{\mathrm{out}}(t)$ is obtained as

$$i_{\mathrm{out}}(t) = \underbrace{\frac{\hat{V}_{\mathrm{ac}}\, \hat{I}_{\mathrm{ac}}}{2\, V_{\mathrm{dc}}}}_{I_{\mathrm{dc}}} + \underbrace{\left(-\frac{\hat{V}_{\mathrm{ac}}\, \hat{I}_{\mathrm{ac}}}{2\, V_{\mathrm{dc}}} \cos(2\omega t)\right)}_{i_{\mathrm{C}}(t)}. \tag{5.18}$$

The expression (5.18) indicates that the current $i_{\mathrm{out}}(t)$ consists of a pure DC component I_{dc} and a varying component $i_{\mathrm{C}}(t)$ at the second harmonic frequency. According to Fig. 5.9, the DC component I_{dc} supplies the load, while the varying component $i_{\mathrm{C}}(t)$ flows through the capacitor

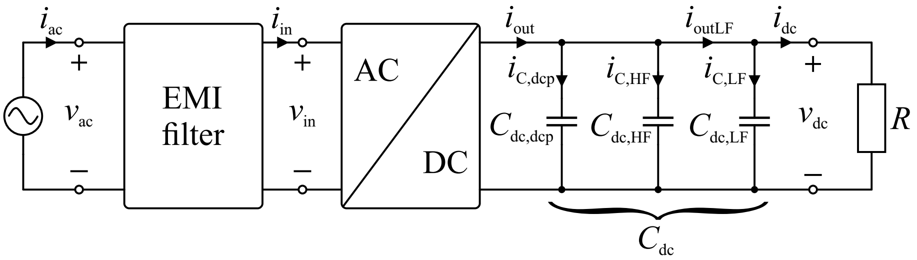


Figure 5.9: Converter block scheme with a simplified representation of the DC-side capacitor bank's structure.

C_{dc}. The varying capacitor current $i_{\text{C}}(t)$ causes voltage ripple $v_{\text{ripple}}(t)$ in the output voltage $v_{\text{dc}}(t)$, which can be written as

$$v_{\text{ripple}}(t) = \frac{1}{C_{\text{dc}}} \int_{0}^{t} i_{\text{C}}(\tau) d\tau, \tag{5.19}$$

where C_{dc} is the DC-side output capacitor. By extracting the ripple component of the current from (5.18) and inserting it into (5.19), the instantaneous output voltage ripple $v_{\text{ripple}}(t)$ is obtained as

$$v_{\text{ripple}}(t) = -\frac{\hat{V}_{\text{ac}} \hat{I}_{\text{ac}}}{4\,\omega\, C_{\text{dc}}\, V_{\text{dc}}} \sin(2\omega t). \tag{5.20}$$

Consequently, the magnitude of the output voltage ripple Δv_{DC} can be written as

$$\Delta v_{\text{DC}} = \frac{\hat{V}_{\text{ac}} \hat{I}_{\text{ac}}}{4\,\omega\, C_{\text{dc}}\, V_{\text{dc}}}. \tag{5.21}$$

By isolating (5.21) for C_{dc} and considering that $\omega = 2\pi f_{\text{L}}$, a criterion for determining the required DC-side capacitance is obtained as

$$C_{\text{dc}} \geq \frac{\hat{V}_{\text{ac}} \hat{I}_{\text{ac}}}{8\,\pi\, f_{\text{L}}\, \Delta v_{\text{DC}}\, V_{\text{dc}}}. \tag{5.22}$$

In order to ensure operation with a maximum allowed DC voltage ripple of $\Delta v_{\text{DC.max}} = 15\ \text{V}$ within the entire operating range of the investigated DC-AC converter, the required value of capacitance was calculated under the most demanding operating conditions in terms of DC voltage ripple. The latter occur when operating at the highest expected AC voltage $\hat{V}_{\text{ac,max}}$ and current $\hat{I}_{\text{ac,max}}$, and the lowest DC voltage $V_{\text{dc,min}}$. Accordingly, the minimum required capacitance $C_{\text{dc,min}}$ was obtained as

$$C_{\text{dc,min}} = \frac{\hat{V}_{\text{ac,max}} \hat{I}_{\text{ac,max}}}{8\,\pi\, f_{\text{L}}\, \Delta v_{\text{DC}}\, V_{\text{dc,min}}} = \frac{253\sqrt{2} \cdot 13\sqrt{2}}{8 \cdot \pi \cdot 50 \cdot 20 \cdot 360} \approx 730\mu\text{F}. \tag{5.23}$$

In order to prevent excessive losses and overheating, which may lead to a reduced lifetime or even a failure of the capacitors, the capacitor bank must be designed such that it supports the expected ripple current. The DC-side capacitors of the interleaved DC-AC converter are exposed to both LF and HF current ripples. The origin of the LF ripple has already been explained. By extracting the time varying component from (5.18), the LF capacitor current ripple $i_{\mathrm{C,LF}}(t)$ can be written as

$$i_{\mathrm{C,LF}}(t) = -\frac{\hat{V}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}}{2\,V_{\mathrm{dc}}}\cos(2\omega t). \tag{5.24}$$

For the investigated case, the highest expected LF ripple current magnitude $\hat{I}_{\mathrm{C,LF}}$ is calculated as

$$\hat{I}_{\mathrm{C,LF}} = \frac{\hat{V}_{\mathrm{ac,max}}\,\hat{I}_{\mathrm{ac,max}}}{2\,V_{\mathrm{dc,min}}} = \frac{253\sqrt{2}\cdot 13\sqrt{2}}{2\cdot 360} = 9.14\mathrm{A}, \tag{5.25}$$

which results in an rms ripple of $I_{\mathrm{C,LF}} = 6.46\ \mathrm{A_{rms}}$. The latter represent the minimum ripple capability of the LF DC bus capacitors. For achieving the required capacitance, small volume design, and fulfilling the ripple current criteria, 150 μF aluminum electrolytic capacitors ALC101151CD550 from producer Kemet were selected. A parallel connection of six such capacitors yields a total rms current handling capability of 7.92 $\mathrm{A_{rms}}$ at the frequency of 100 Hz and a total capacitance of $C_{\mathrm{dc,LF}} = 900\ \mu$F. The power losses on the LF capacitor bank, can be calculated as

$$P_{\mathrm{C,LF}} = n\left(\left(\frac{I_{\mathrm{C,LF}}}{n}\right)^2 \mathrm{ESR} + I_{\mathrm{leak}}\,V_{\mathrm{dc}}\right), \tag{5.26}$$

where n is the number of paralleled capacitors, ESR is the equivalent series resistance of each capacitor, and I_{leak} the leakage current of each capacitor. Information about ESR and I_{leak} for the selected capacitors is obtained from their datasheet [132].

In addition to the LF current ripple, the DC-side capacitors are also exposed to the HF current ripple. The latter represents the current that is being switched by the transistors in the switching stage of the converter. Its propagation into the LF capacitor bank formed of electrolytic capacitors could result in severe overheating and therefore it is bypassed through $C_{\mathrm{dc,HF}}$, as shown in the simplified scheme in Fig. 5.4. The capacitor $C_{\mathrm{dc,HF}}$ represents the HF DC-side capacitor bank, which is in the discussed case formed of 3 paralleled film capacitors WIMA DCP4I051506ID2KSSD. The latter have a very low dissipation factor and provide high ripple current capability [133].

The remainder of the DC-side capacitors are represented by the switching cell decoupling capacitors designated with $C_{\mathrm{dc,dcp}}$ in Fig. 5.4. The main purpose of these capacitors is to provide a low impedance path for the HF components generated at the switching transitions. They have to be placed as close as possible to the transistors in each half-bridge, in order to minimize the switching cell area and consequently its loop inductance. A smaller loop inductance results in less oscillation at the switching transitions and suppression of voltage overshoots. Multi-Layer Ceramic Capacitors of several different capacitances and small footprints were used for realization of the switching cell decoupling stage. The structure of the entire DC-side capacitor bank is summarized in Table 5.8.

Table 5.8: Structure of the DC-side capacitor bank.

Designator	Type	Description	Configuration
$C_{\mathrm{dc,dcp}}$	Multi-Layer Ceramic	TDK, C3216X7R2J333K160AA 630 V, 330 nF, SMD-1206	48 in parallel
		TDK, CKG57NX7T2J105M500JH 630 V, 1 μF, SMD-2220	11 in parallel
$C_{\mathrm{dc,HF}}$	Metallized Polypropylene Film	WIMA, DCP4I051506ID2KSSD 600 V, 15 μF, 17x34.5x31.5 mm	3 in parallel
$C_{\mathrm{dc,LF}}$	Aluminum Electrolytic Film	KEMET, ALC10A151CD550 550 V, 150 μF, ϕ30x40 mm	6 in parallel

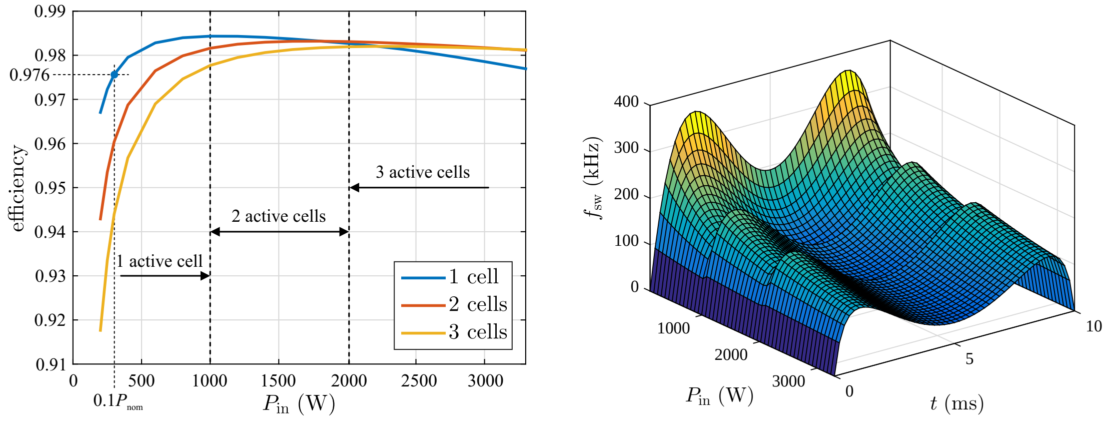
5.4 Cell Shedding Strategy

Cell shedding has to be employed in order to achieve highly efficient operation of the interleaved converter within a wide operating range. This strategy is mainly aimed at improving the light load efficiency of the interleaved converter, as it is well-known that a typical efficiency curve exhibits a rapid drop at power levels below 20 to 10 $\%$ of the nominal power [134]. In DCM operated converters with variable switching frequency, the drop in light load efficiency is even more significant since their switching frequency increases under light load conditions, as evident from Fig. 4.16. By gradually turning off individual interleaved cells and thus increase the current in the remaining active cells, the escalation of switching frequency is prevented, which benefits the light load power conversion efficiency. The downside of employing the phase shedding technique is a reduction of the ripple cancellation effect, which results in higher EMI filtering requirements in respect to the case when all the available cells are active [126]. For this reason, the tendency is to operate with as many cells as possible for achieving the desirable power conversion efficiency.

By using the power loss estimation algorithms presented in Appendix A, the total power losses were estimated for the investigated interleaved AC-DC converter operating with three, two or only one active interleaved cell throughout its entire operating range. The power loss analysis included estimation of the turn-off and conduction losses of the HF-switched MOSFETs, conduction losses of the LF-switched MOSFETs, magnetic core and winding losses of the inductors, and losses in the LF capacitor bank. These loss components constitute the major part of the converter's total power losses and were used for estimating the converter's power conversion efficiency. Fig. 5.10(a) provides an efficiency comparison for operating with a different number of active interleaved cells. One thing that has to be considered when selecting the number of active interleaved cells within a certain operating range, are the absolute maximum current ratings of the utilized devices. The critical components in the investigated converter are the power inductors, which were designed to operate at the powers up to one third of the converter's nominal power P_{nom}. By significantly exceeding this operating power limit, the effective inductance could drop below the admissible 90 $\%$ of its initial value, which could endanger ZVS operation. Another thing to consider is the local minimum switching frequency $f_{\mathrm{sw,min1}}$ that has to be maintained above the minimum allowed switching frequency $f_{\mathrm{sw,min}}$. When operating at an excessively high power with an insufficient number of cells, this condition is not fulfilled and consequently ZVS may be lost. An argument for preventing the operation with an insufficient number of cells is the reduced ripple cancellation and increased EMI filtering requirements, which could considerably add to the total volume of the filter. However, the efficiency curves in Fig. 5.10(a) generally talk in favor of a lower number of active switching cells. In terms of power conversion efficiency, operation with three active cells is only justified when operating above the nominal input power of $P_{\mathrm{nom}} = 3000$ W. Furthermore, when the power is decreasing, the single cell operation should begin at about 1700 W, which would result in a maximum inductor current of $i_{\mathrm{Lmax}} \approx 22$A. The latter is almost twice the current the inductor was designed for and would also significantly increase the filtering requirements. It must be taken into account that the presented efficiency curves only apply for the DCM-based ZVS operation and that as soon as ZVS is lost, the efficiency drops considerably. With the aim of optimizing the efficiency and at the same time ensuring a safe and reliable ZVS operation with a low DM noise, the following cell shedding strategy was selected:

- single cell operation up to approximately 33 $\%$ of P_{nom},
- two cell operation between 33 $\%$ and 66 $\%$ of P_{nom},
- and three cell operation above 66 $\%$ of P_{nom}.

The operating ranges are also designated in Fig. 5.10(a) and represent very important information for designing the EMI filter. The highlighted point in the single cell efficiency curve indicates that the required 96 $\%$ efficiency down to the power as low as 10 $\%$ of P_{nom} is only achieved if cell shedding is applied such that only one cell is active under light load conditions. On the basis of the selected phase shedding strategy the required variation of the operating switching frequency is shown in Fig. 5.10(b). It is evident that the frequency does not vary much in respect to the operating power within the greater part of the converter's operating range. Nonetheless, very high switching frequencies are required when operating at a low power level.



(a)

(b)

Figure 5.10: (a) Estimated power conversion efficiency for operation with a different number of active interleaved cells over the entire operating range of the converter. (b) Required switching variation for the selected phase shedding strategy.

5.5 EMI filter design

According to the design specifications listed in Table 5.1, the investigated AC-DC converter must achieve compliance with the disturbance limits specified in standards CISPR 14 [118] and CISPR 22 [119]. The electromagnetic disturbances are transmitted by radiation and conduction. Up to the frequency of approximately 10 MHz the dominant disturbance transmission mode is conduction, while radiation prevails at frequencies above 10 MHz [135]. Only conducted disturbances are considered within this thesis. They are generally divided into differential mode (DM) and common mode (CM) noise emissions. The source of CM noise are the parasitic components, primarily the parasitic capacitances to ground, at the points in the circuit exposed to high voltage rates of change [136, 137]. On the other hand, the DM noise in a switching power converter is represented by the ripple current at the switching frequency and its higher order harmonics. The DM noise emissions are generally dominant in the frequency range below 2 MHz, while the CM noise emissions are dominant at higher frequencies [138].

Due to the dominance of the DM noise emissions at lower frequencies, the total size of EMI filters in switching power converters is mainly dictated by the size of the DM noise filtering components. The contribution of the DM filter is even greater in DCM and CRM operated converters, due to the extremely high inductor current ripple [139, 140]. For the described reasons, the EMI filter design procedure presented within this thesis is primarily focused on eliminating the DM noise with a low volume DM EMI filter.

The presented cell shedding strategy and the resulting operating ranges in which a specific number of interleaved cells is active represent the basis for designing the DM EMI filter. It is evident from Fig. 5.1 that the input current ripple i_{in} is the highest in the case of single cell operation. Although the average input current $i_{\mathrm{in,avg}}$ is higher in case of two and three cell operation due to the higher power that is processed at the same voltage level, the resulting HF ripple in i_{in} is lower in magnitude due to interleaving. In addition, its harmonic content is pushed towards higher frequencies where the filtering requirements are less demanding. The filtering requirements can be expressed through the filter's cutoff frequency. The most demanding case is represented by the lowest required filter cutoff frequency, the practical realization of which demands the largest passive components.

In order to determine the required cutoff frequency of the filter, which represents a fundamental filter design specification, the level of conducted DM noise has to be obtained. In general there are two common approaches for designing the DM EMI filter. The most common and accurate approach is based on experimental measurements carried out on a prototype of the converter without the presence of an input filter. By using a suitable CM/DM separator [141–143], the actual conducted CM and DM emission levels are obtained separately. While accuracy is the advantage of such an approach, the drawback is that the input filter is not incorporated within the converter before the second version of the prototype. A less accurate alternative to the experimental measurement based approach is the usage of a numerical calculation procedure for estimating the conducted emissions, such as presented in [144]. Its advantages are the possibility for integrating the EMI filter design procedure into the design procedure of the converter's power stage and eliminating the need for the initial version of the prototype, which serves for obtaining the EMI filter design requirements.

For a better integration of the EMI filter into the investigated converter, a numerical estimation method was used which allows for designing an almost final filter that suppresses the DM noise under the specified limits. Due to operation in DCM, a rather high DM noise is expected. The quasi-peak DM noise in CCM operated converters with fixed switching frequency can be estimated by following the design procedure described in [144]. However, the procedure cannot be directly adapted for usage in the investigated DCM operated converter with a constant magnitude of the reversed current, as its switching frequency varies over time and instantaneous load conditions. As a result, the operating point with the highest rms-value of the current ripple does not necessarily represent the most critical point for designing the DM EMI filter, as is the case in converters operating with a constant switching frequency. It is evident from Fig. 4.19, that the highest current ripple will appear at t_{min1} where the AC voltage reaches its peak. At this instant the switching frequency reaches its local minimum $f_{\mathrm{sw,min1}}$ and in case the latter is below 150 kHz, which represents the lower limit of the frequency range covered by EMI standards, the first component that has to be attenuated is the first harmonic at the frequency above 150 kHz. Due to the decay of the harmonic component magnitudes with increasing frequency, the required attenuation at the point of the highest current ripple may be lower than the one required for a lower-in-magnitude ripple current at a frequency closer to 150 kHz. The complexity and importance of finding the worst case conducted EMI noise in a variable switching frequency operated converter is presented in [139, 140, 145] for the case of a CRM boost PFC converter. However, the obtained results do not directly apply for the AC-DC converter investigated within this thesis, as the switching frequency variation pattern of a CRM boost PFC converter is different to the one presented in Fig. 4.19.

According to CISPR 16-2-1 [146], a Line Impedance Stabilizer Network (LISN) also known as the Artificial Mains Network (AMN) must be inserted between the device under test and the utility grid when performing conducted EMI measurements. The utilization of LISN achieves reproducibility of measurements at different locations, as its large filtering components eliminate the influence of the grid impedance variation on the tested converter. In addition, the presence of a LISN also blocks the propagation of conducted emissions from the utility grid to the device under test and thus ensures that only noise generated by the tested device is sensed by the EMI receiver [147]. A simplified structure of a LISN used for measuring the conducted noise of a single-phase AC-DC converter is shown in Fig. 5.11. Among different types and configurations of LISNs specified in CISPR 16-1-2 [148], the $50\Omega/50\mu$H LISN is the most commonly used [149]. This configuration comes with the following parameters of components depicted in Fig. 5.11:

- $L_{\mathrm{lisnp}} = L_{\mathrm{lisnn}} = L_{\mathrm{lisn}} = 50\mu\mathrm{H}$,
- $R_{\mathrm{lisnp}} = R_{\mathrm{lisnn}} = R_{\mathrm{lisn}} = 50\Omega$,
- $C_{\mathrm{lisn1p}} = C_{\mathrm{lisn1n}} = C_{\mathrm{lisn1}} = 8\mu\mathrm{F}$,
- $C_{\mathrm{lisn2p}} = C_{\mathrm{lisn2n}} = C_{\mathrm{lisn2}} = 250\mathrm{nF}$.

The capacitors C_{lisn1p} and C_{lisn1n} are utilized for diverting the noise present in the utility grid from the measurement device and prevent its presence within the measurement results. The inductors L_{lisnp} and L_{lisnn} represent a very high impedance in the frequency range covered by the EMI standards and therefore the HF conducted noise generated by the AC-DC converter under test does not propagate through the LISN toward the utility grid. On the other hand, the capacitors C_{lisn2p} and C_{lisn2n} represent a short circuit for this HF conducted noise and therefore all the HF noise components are terminated through the resistors R_{lisnp} and R_{lisnn}. The latter represent the

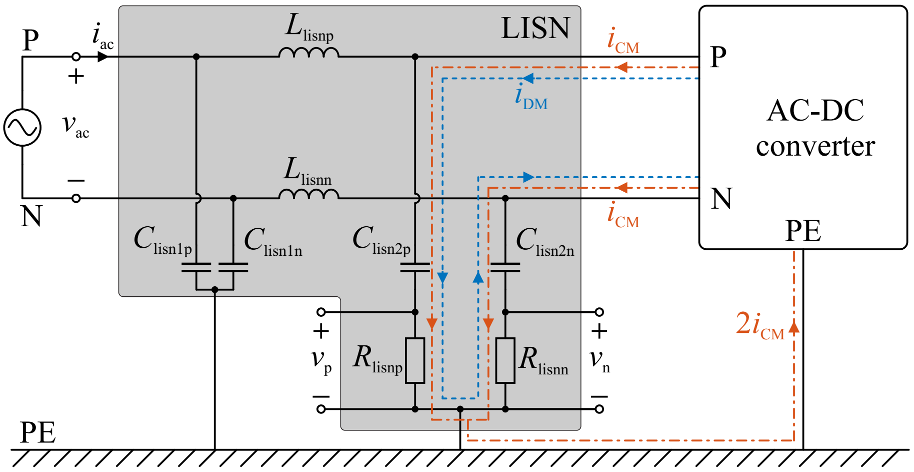


Figure 5.11: Simplified circuit of a LISN within a conducted EMI measurement setup.

input impedance of the EMI test receiver (spectrum analyzer). In order to achieve compliance with EMI standards [118, 119], the voltages v_p and v_n must not exceed the imposed limits for conducted disturbance.

The paths of DM currents i_DM and CM currents i_CM are marked in Fig. 5.11. While the CM currents flow in the same direction through the phase (P) and the neutral (N) conductors toward the protective earth (PE), the DM current flow in one direction through the phase conductor and return in the opposite direction through the neutral conductor. Since both the DM and the CM currents within the conducted emission regulatory frequency range are terminated through the resistors R_lisnp and R_lisnn, the measured voltages v_p and v_n contain information about both, the CM noise and the DM noise. On the basis of Fig. 5.11, the voltages v_p and v_n can be written as

$$v_\mathrm{p} = R_\mathrm{lisn}\left(i_\mathrm{CM} + i_\mathrm{DM}\right), \tag{5.27a}$$

$$v_\mathrm{n} = R_\mathrm{lisn}\left(i_\mathrm{CM} - i_\mathrm{DM}\right). \tag{5.27b}$$

The measured v_p and v_n must be further processed by the spectrum analyzer in order to obtain the quasi-peak or average value of the total conducted noise within the regulatory frequency range. Compliance with the applicable EMI standards is achieved when the quasi-peak or average conducted noise obtained from both, v_p and v_n is within the limits imposed by the standards.

Although the information about the total conducted noise comprised in v_p and v_n is sufficient for verifying compliance with most of the EMI standards, it is commonly considered superficial information for designing EMI filters. In order to avoid overdimensioning of the EMI filter and to select the most suitable filter structure that would result in the lowest power losses and smallest total filter size, it is important to know the exact level of CM and DM noise, separately. Several CM/DM noise separators have been developed for this purpose [141–143]. They require simultaneous measurement of voltages v_{p} and v_{n} on the basis of which the DM voltage v_{DM} and CM voltage v_{CM} can be extracted as

$$v_{\mathrm{DM}} = \frac{1}{2}\left(v_{\mathrm{p}} - v_{\mathrm{n}}\right), \tag{5.28a}$$

$$v_{\mathrm{CM}} = \frac{1}{2}\left(v_{\mathrm{p}} + v_{\mathrm{n}}\right). \tag{5.28b}$$

By introducing (5.27a) and (5.27b) into (5.28), the DM and CM voltages are obtained as

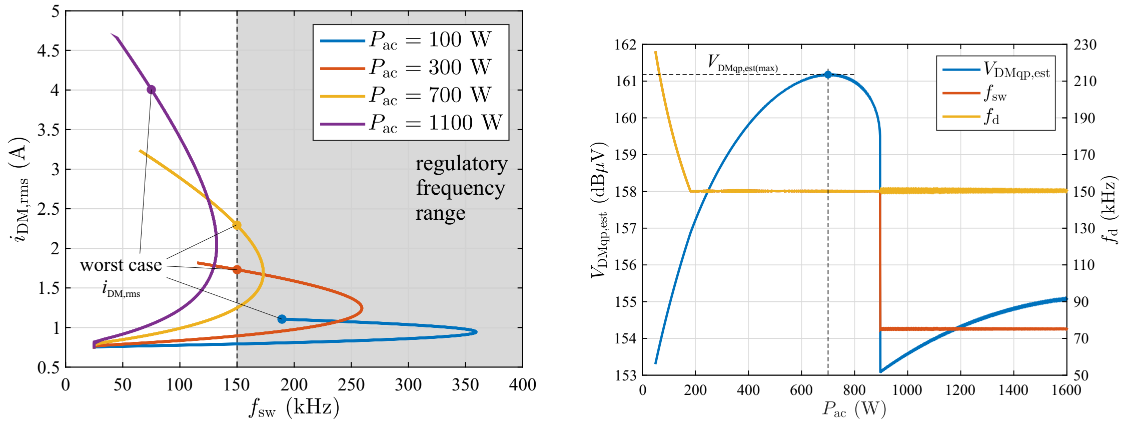
$$v_{\mathrm{DM}} = R_{\mathrm{lisn}}\, i_{\mathrm{DM}}, \tag{5.29a}$$

$$v_{\mathrm{CM}} = R_{\mathrm{lisn}}\, i_{\mathrm{CM}}. \tag{5.29b}$$

The common mode current i_{CM} depends on the parasitic components and therefore its accurate estimation is a very complex task [150–152]. On the other hand, the differential mode current i_{DM} is the current i_{L} flowing through the power inductor, limited to the frequency range that is blocked by the LISN's inductors and thus passed through the LISN's resistors R_{lisnp} and R_{lisnn}. It is essentially the HF ripple in i_{L} with a frequency that equals the converter's switching frequency and can be easily estimated in the design phase by simulation or analytical modeling.

By eliminating the average inductor current $i_{\mathrm{L,avg}}$ from (3.8), which is analogous to insertion of the LISN inductors L_{lisnp} and L_{lisnn} in practice, and inserting the modified expression (3.8) into the algorithm for calculating the inductor's winding losses presented in Appendix A, the local rms value $i_{\mathrm{DM,rms}}$ of the differential mode current is obtained. Fig. 5.12(a) shows the local rms differential mode current $i_{\mathrm{DM,rms}}$ in respect to the corresponding switching frequency f_{sw} at which it occurs in the investigated AC-DC converter operating at three different power levels. As the switching frequency varies over time and the load, the differential mode noise varies accordingly. It is evident from Fig. 5.12(a) that $i_{\mathrm{DM,rms}}$ is the highest at the highest rms AC power of $P_{\mathrm{ac}} = 1100\mathrm{W}$. On the other hand, the switching frequency is the lowest at the highest operating power. By considering that the spectrum of a triangular current exhibits a descending characteristic of approximately -40 dB/decade within the discussed frequency range [135], the operation at the highest power most probably does not generate the highest conducted DM noise within the regulatory frequency range. In general, it is more likely that the highest $i_{\mathrm{DM,rms}}$ to enter the regulatory frequency range will cause the worst case DM noise.

A term design frequency f_{d} is introduced for the purpose of determining the DM EMI filter requirements. It represents the frequency of the first harmonic of the DM current to enter the regulatory frequency range. In case the switching frequency f_{sw} equals or is higher than 150 kHz,



(a) (b)

Figure 5.12: (a) Appearance of the worst case DM current $i_{\mathrm{DM,rms}}$, which defines the DM EMI filter design criteria. (b) Highest estimated DM noise $V_{\mathrm{DMqp,est}}$ and the corresponding switching frequency f_{sw} and design frequency f_{d} in respect to the operating power.

the design frequency is $f_{\mathrm{d}} = f_{\mathrm{sw}}$. On the other hand, when f_{sw} is lower than 150 kHz, the design frequency is determined as

$$f_{\mathrm{d}} = \mathrm{ceil}\left(\frac{150 \cdot 10^3}{f_{\mathrm{sw}}}\right) f_{\mathrm{sw}}, \tag{5.30}$$

where the function ceil represents the round-up operation. Assuming that the rms value of the inductor's current ripple represents an adequate measure for estimating the quasi-peak differential mode voltage $V_{\mathrm{DMqp,est}}$ obtained from an EMI receiver [144], $V_{\mathrm{DMqp,est}}$ can be calculated as

$$V_{\mathrm{DMqp,est}}(f_{\mathrm{d}}) = 20 \log \left(R_{\mathrm{lisn}}\, i_{\mathrm{DM,rms}} \left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{d}}}\right)^2 \frac{1}{\mu \mathrm{V}} \right), \tag{5.31}$$

where μV denotes the voltage of 1 μV, which is used as the base quantity in respect to which the limits for the conducted electromagnetic noise are specified in standards [118, 119]. Due to the usage of μV as the reference, the quasi-peak DM voltage $V_{\mathrm{DMqp,est}}$ is expressed in dBμV.

Fig. 5.12(b) was constructed by calculating $V_{\mathrm{DMqp,est}}$ over the entire operating range of the investigated AC-DC converter operating with a single active cell (no interleaving) and extracting the worst case DM noise that occurs at each rms input power P_{ac}. In the major part of the analyzed operating power range, the design frequency f_{d} is at the lower boundary of the regulatory frequency range, as it approximately equals $f_{\mathrm{d}} = 150$ kHz. At moderate operating powers, between 180 W and 900 W, the worst case DM noise is a result of the highest current ripple at the switching frequency of $f_{\mathrm{sw}} = 150$ kHz. Under light load conditions, when the operating power is below 180 W, the worst case DM noise appears at the frequency that corresponds with the maximum

$i_{\mathrm{DM,rms}}$. In both cases, the design frequency is $f_{\mathrm{d}} = f_{\mathrm{sw}}$. At the operating power of approximately $P_{\mathrm{ac}} \approx 900$ W, the estimated quasi-peak DM voltage $V_{\mathrm{DMqp,est}}$ exhibits a considerable drop. The reason is in the fact that the switching frequency f_{sw} remains outside the regulatory frequency range at all times, as evident from the $i_{\mathrm{DM,rms}}$-characteristic for the power of $P_{\mathrm{ac}} = 1100$ W in Fig. 5.12(a). As a result, the DM noise within the regulatory frequency range is lower at operating powers above 900 W, although the magnitude of the DM current $i_{\mathrm{DM,rms}}$ is higher. It is evident from Fig. 5.12(b) that the most critical DM noise at higher operating powers is generated at the switching frequency of $f_{\mathrm{sw}} = 75$ kHz, as its second harmonic falls onto the border of the regulatory frequency range. The same as in case of operating at moderate powers, the design frequency is $f_{\mathrm{d}} = 150$ kHz.

On the basis of the estimated quasi-peak differential mode voltage $V_{\mathrm{DMqp,est}}$, the required attenuation $\mathrm{Att}_{\mathrm{req}}$ of the DM EMI filter at the design frequency f_{d} is calculated as [144]

$$\mathrm{Att}_{\mathrm{req}}(f_{\mathrm{d}}) = V_{\mathrm{DMqp,est}}(f_{\mathrm{d}}) - \mathrm{StdLim}(f_{\mathrm{d}}) + \mathrm{Margin}, \tag{5.32}$$

where $\mathrm{StdLim}(f_{\mathrm{d}})$ is the conducted noise limit in $\mathrm{dB}\mu\mathrm{V}$ imposed by the applicable standard, and Margin the additional safety margin. As specified in Table 5.1, the investigated converter has to comply with the conducted emission limits defined in CISPR 14 [118] and CISPR 22 [119]. The more stringent limits specified in CISPR 22 for Class B equipment match with the limits given in CISPR 14, and therefore designing for compliance with both standards can be unified. By considering a safety margin of $\mathrm{Margin} = 10$ dB, the required attenuation $\mathrm{Att}_{\mathrm{req}}$ at the design frequency of $f_{\mathrm{d}} = 150$ kHz is obtained as $\mathrm{Att}_{\mathrm{req}}(f_{\mathrm{d}}) = 105$ dB. This represents the most demanding DM EMI filter design requirement, as the required attenuation is the highest within the analyzed range, while the design frequency is the lowest. The operating point at which the required attenuation $\mathrm{Att}_{\mathrm{req}}$ is the highest appears at the power of $P_{\mathrm{ac}} = 704$ W and corresponds with the highest estimated quasi-peak DM voltage $V_{\mathrm{DMqp,est(max)}}$, evident from Fig. 5.12(b).

The required attenuation of $\mathrm{Att}_{\mathrm{req}}(f_{\mathrm{d}}) = 105$ dB is difficult to realize in a single stage DM EMI filter. Its cutoff frequency f_{c} would have to be approximately $f_{\mathrm{c}} \approx 350$ Hz, which would demand for very large passive components. Therefore, a multi-stage DM EMI filter was designed. According to [125], the usage of a 3-stage LC filter would result in a close to minimum total size of the DM EMI filter with $\mathrm{Att}_{\mathrm{req}}(f_{\mathrm{d}}) = 105$ dB and $f_{\mathrm{d}} = 150$ kHz. The basic structure of a 3-stage LC filter is shown in Fig. 5.13. The minimum volume of such a filter is achieved when it is formed of three identical stages, with the same capacitances and inductances within each stage [125]. The problem of such design strategy is that the third stage of the filter is influenced by the impedance of the utility grid, which may vary considerably depending on the grid impedance at the point of

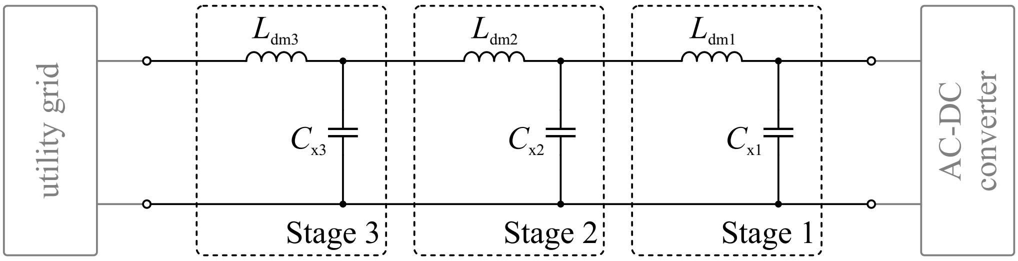


Figure 5.13: Ideal 3-stage low-pass filter structure composed of a series connection of LC stages.

connection. In order to reduce the effect of the grid impedance on the attenuation and impedance of the DM EMI filter, the resonant frequency of the third stage f_{o3} was set higher than the resonant frequencies of the first and second stage. Therefore the desirable relation between the resonant frequencies of individual filter stages can be written as

$$f_{\mathrm{o1}} = f_{\mathrm{o2}} = \frac{1}{k_{\mathrm{n}}} f_{\mathrm{o3}}, \tag{5.33}$$

where f_{o1}, f_{o2}, and f_{o3} are the resonant frequencies of individual filter stages and k_{n} the ratio between the resonant frequencies of the third stage and the resonant frequencies of the other two stages. In the presented case k_{n} was arbitrarily selected as $k_{\mathrm{n}} = 3$. In order to compensate for the increase in total filter volume introduced by increasing the resonant frequency of the third filter stage, the inductance L_{dm3} will not be realized by an inductor in practice. Its role will be taken over by the LISN inductors during EMC measurements or by the inductance of the utility grid at the point of connection during normal operation [153]. For the purpose of designing the DM EMI filter, the inductance L_{dm3} will be considered as $L_{\mathrm{dm3}} = 2\,L_{\mathrm{lisn}}$.

The transfer functions of the 3-stage LC filter presented in Fig. 5.13 are of a sixth order, which makes analytical analysis very complex. For this reason, the DM EMI filter was designed on the basis of LC filters' asymptotic attenuation [149]. The resonant frequencies of individual filter stages can be written as

$$f_{\mathrm{ox}} = \frac{1}{2\pi\sqrt{L_{\mathrm{x}} C_{\mathrm{x}}}}; \quad x = \{1, 2, 3\}\,, \tag{5.34}$$

where x denotes a specific filter stage. For achieving the same resonant frequencies of the first and second filter stage, as defined by (5.33), the capacitances and inductances within both stages must be $C_{\mathrm{x1}} = C_{\mathrm{x2}} = C_{\mathrm{x}}$ and $L_{\mathrm{dm1}} = L_{\mathrm{dm2}} = L_{\mathrm{dm}}$. By considering the asymptotic attenuation of LC filters at high frequencies, the attenuation $\mathrm{Att}_{\mathrm{3st}}$ of the discussed 3-stage LC filter can be written as

$$\mathrm{Att}_{\mathrm{req}} = (2\pi f_{\mathrm{d}})^6 (L_{\mathrm{dm}} C_{\mathrm{x}})^2 L_{\mathrm{dm3}} C_{\mathrm{x3}}. \tag{5.35}$$

By isolating the time constant $L_{\mathrm{x}} C_{\mathrm{x}}$ for each filter stage from (5.34), substituting the obtained expressions into (5.35), and considering that the required attenuation $\mathrm{Att}_{\mathrm{req}}(f_{\mathrm{d}})$ is given in dB, (5.35) is rearranged as

$$10^{\frac{\mathrm{Att_{req}}(f_\mathrm{d})}{20}} = \frac{f_\mathrm{d}^6}{f_\mathrm{o1}^4\, f_\mathrm{o3}^2}. \tag{5.36}$$

Substituting (5.33) into (5.36) and isolating f_o1 from the expression yields

$$f_\mathrm{o1} = \sqrt[6]{\frac{f_\mathrm{d}^6}{k_\mathrm{n}^2 \cdot 10^{\frac{\mathrm{Att_{req}}(f_\mathrm{d})}{20}}}}. \tag{5.37}$$

On the basis of (5.37) and (5.33), the required resonant frequencies for all three stages of the DM filter were determined as $f_\mathrm{o1} = f_\mathrm{o2} = 13.9\,\mathrm{kHz}$ and $f_\mathrm{o3} = 41.6\,\mathrm{kHz}$. As the inductance of the third filter stage is given as $L_\mathrm{dm3} = 2\,L_\mathrm{lisn} = 100\,\mu\mathrm{H}$ for the purpose of designing the filter, the capacitance C_x of the third stage is directly obtained from (5.34) for $x = 3$ as $C_\mathrm{x3} \approx 150\,\mathrm{nF}$. In contrast to the third filter stage, there is more flexibility when determining the capacitances C_x and inductances L_dm of the remaining filter stages, as none of them is predetermined. However, there are several limitations and design trade-offs. The capacitances of the DM filter capacitors determine the reactive power drawn from the utility grid and therefore the tendency for using smaller capacitances [149, 154]. Nonetheless, an excessive reduction of the DM capacitances results in an increased size of the inductor in an LC filter, as well as higher AC voltage ripple [149, 153]. For achieving balance between the total size of the filter, the reactive power drawn from the grid and the AC voltage ripple, the DM capacitors were selected as $C_\mathrm{x1} = C_\mathrm{x2} = C_\mathrm{x} = 1.12\,\mu\mathrm{F}$. Consequently, the required inductances in the first and second stage of DM EMI filter were obtained as $L_\mathrm{dm1} = L_\mathrm{dm2} = L_\mathrm{dm} = 118\,\mu\mathrm{H}$.

The filter must be properly damped in order to avoid resonant peaks in the discussed DM EMI filter's attenuation characteristic. In comparison with an ideal filter shown in Fig. 5.13, the resonant peaks are partially damped in a practical filter due to the parasitics within the filter's components [149]. As the design of the filter is usually directed towards achieving the lowest possible power losses, the parasitics and their affects tend to be minimized. Therefore, additional damping circuits have to be incorporated. According to the guidelines presented in [6], a series $R - L$ damping network with a bypass inductor $L_\mathrm{d} = L_\mathrm{dm}$ and a damping resistor $R_\mathrm{d} = 5.4\Omega$ was designed for damping the resonant peaks of the first and second filter stages. For the third stage of the filter, a parallel $R - C$ damping network was designed with a damping capacitor $C_\mathrm{d} = C_\mathrm{x3}$ and a damping resistor $R_\mathrm{d3} = 37\Omega$. The final structure of the DM EMI filter, including the described damping networks is shown in Fig. 5.14.

The effects of the auxiliary damping networks on the attenuation characteristic of the discussed DM EMI filter are evident from Fig. 5.15(a). It can be observed that the resonant peaks are well

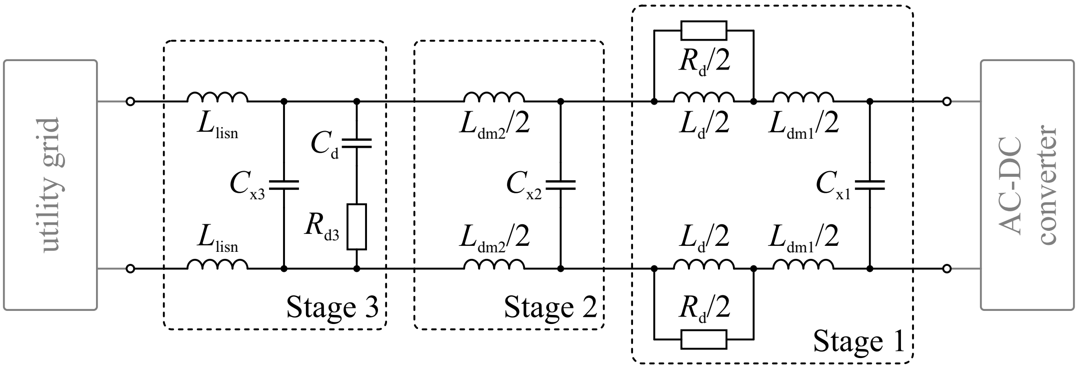
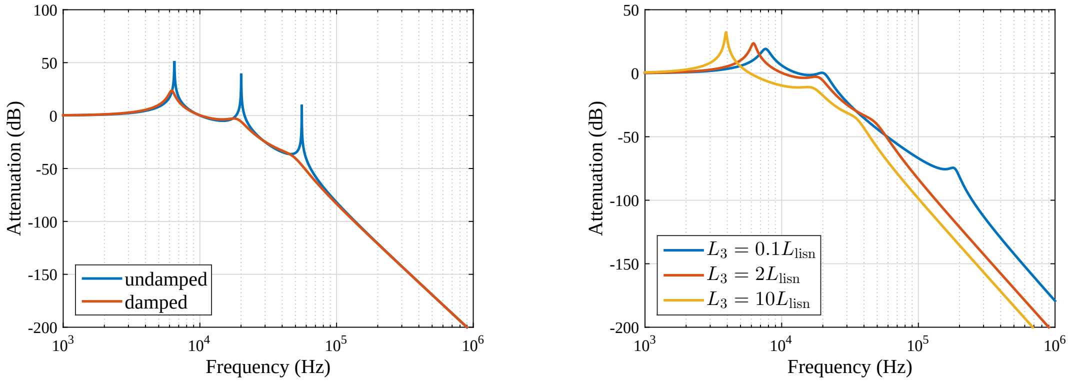


Figure 5.14: Final structure of a 3-stage DM filter including auxiliary damping networks in Stage 1 and Stage 3.

suppressed without affecting the attenuation of the filter within the regulatory frequency range. Nonetheless, the attenuation of the described DM EMI filter changes with impedance of the source. During the design phase it was assumed that the LISN's inductor acts as the inductor in the third stage, which ensures stable attenuation characteristics and adequate suppression of the DM noise during EMC measurements. Once the LISN is disconnected and the converter is connected directly to the utility grid, the attenuation characteristic varies depending on the grid impedance at the point of connection. The latter determines the inductance L_{dm3} in the third filter stage, under the assumption of a purely inductive character of the grid impedance. Although the third filter stage was designed to have a higher resonant frequency and thus a lesser influence on the attenuation characteristic than the first and second stage, an extremely high or low grid impedance may shift the characteristic, as shown in Fig. 5.15(b). Especially critical is the third stage inductance of $L_3 = 10L_{\text{lisn}}$, as the lowest in frequency resonant peak is shifted to the frequency of 3 kHz and increased in magnitude. On the other hand, extremely low grid impedances have a beneficial effect on the lowest in frequency resonant peak as its magnitude is suppressed. However, the high frequency attenuation is reduced, which leads to a higher conducted emissions while operating under such conditions.

A single stage π-type CM EMI filter has been designed even though the conducted CM emissions were not comprehensively analyzed. According to the information technology safety regulations imposed by IEC 60950-1 [155], the maximum earth leakage current I_{lkg} should not exceed 3.5 mA for any movable or stationary equipment connected to PE. This limitation indirectly imposes the maximum total capacitance $C_{\text{y,max}}$ of all the Y-capacitors within the CM EMI filter, which can be calculated as

$$C_{\text{y,max}} = \frac{I_{\text{lkg}}}{\omega_{\text{L}}\,\hat{V}_{\text{ac}}} - \Sigma C_{\text{par}}, \tag{5.38}$$



(a) (b)

Figure 5.15: (a) Attenuation characteristic of a damped and undamped 3-stage DM EMI filter. (b) Influence of the utility grid's impedance (inductance) on the filter's attenuation characteristic.

where ω_{L} is the angular frequency of the grid voltage and ΣC_{par} the sum of all the parasitic capacitances between the converter's components and PE. By considering the nominal magnitude of the grid voltage $\hat{V}_{\mathrm{ac}} = 325$ V, an angular frequency of $\omega_{\mathrm{L}} = 2\,\pi\,50\ \mathrm{rad/s}$, and neglecting the parasitic capacitances, the maximum total capacitance $C_{\mathrm{y,max}}$ is obtained as $C_{\mathrm{y,max}} = 34.3\ \mathrm{nF}$. With the aim of not exceeding this value, the Y-capacitors' capacitance C_{y1} on the converter side was selected as $C_{\mathrm{y1}} = 9.4\ \mathrm{nF}$, while the grid side capacitance to earth C_{y2} was selected as $C_{\mathrm{y2}} = 4.7\ \mathrm{nF}$. The CM choke inserted between them was selected such that an attenuation of approximately -26 dB at the frequency of 150 kHz is achieved for suppressing the conducted CM emissions. The final structure of the described EMI filter, comprising the CM and the DM filter stages, is presented in Fig. 5.16, while its constituting components are listed in Table 5.9.

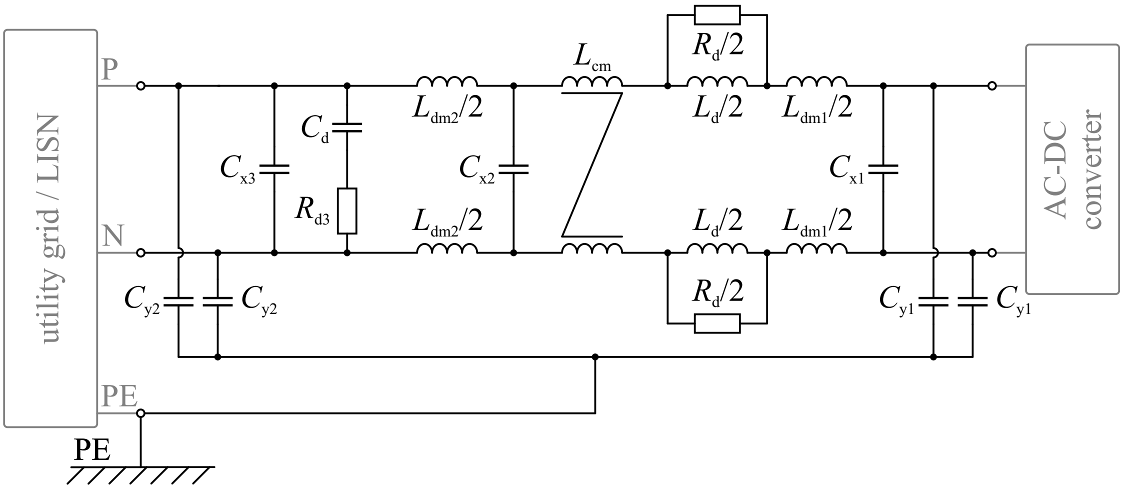

utility grid / LISN
P
N
PE
PE
C_{x3}
C_d
R_{d3}
$L_{dm2}/2$
$L_{dm2}/2$
C_{x2}
L_{cm}
$R_d/2$
$L_d/2$
$L_{dm1}/2$
$L_d/2$
$L_{dm1}/2$
$R_d/2$
C_{x1}
C_{y2}
C_{y2}
C_{y1}
C_{y1}
AC-DC converter

Figure 5.16: Final structure of the EMI input filter for the investigated DC-AC converter.

Table 5.9: EMI filter components.

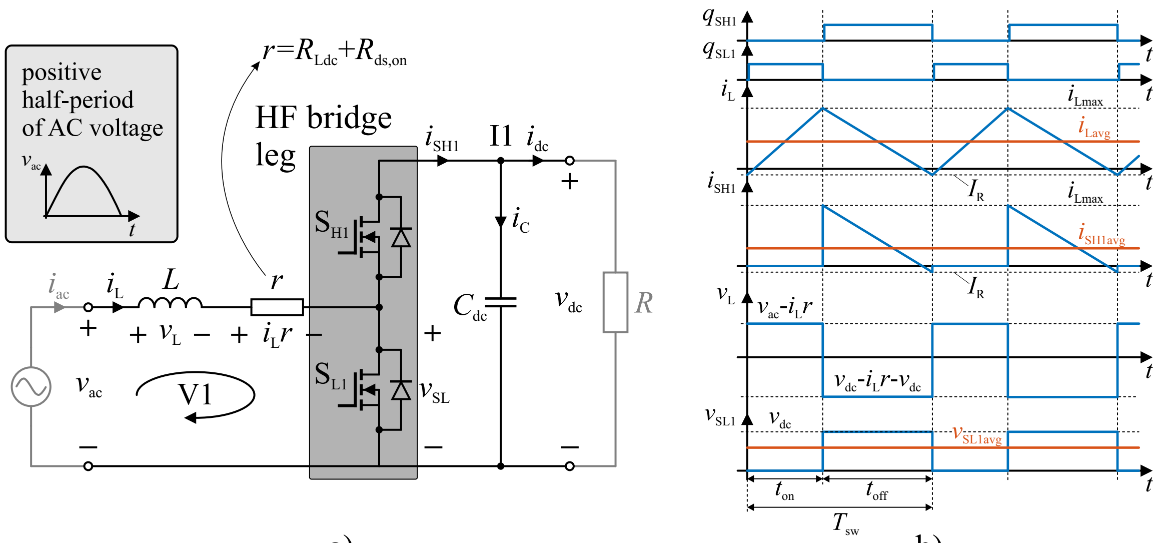
Designator	Description	Specification
C_{x1}, C_{x2}	X2 capacitor (two in parallel)	Kemet, F861, 310 VAC, 0.56 μF
C_{x3}, C_d	X2 capacitor	WIMA, MKP-X2, 305VAC, 0.15 μF
C_{y1}	Y2 capacitor (two in parallel)	WIMA, MKP-Y2, 300VAC, 4.7 nF
C_{y2}	Y2 capacitor	WIMA, MKP-Y2, 300VAC, 4.7 nF
R_{d3}	SMD resistor (2x2 structure - 1 W)	1206, 0.25 W, 37.4 Ω
$R_d/2$	SMD resistor (2x2 structure - 1 W)	1206, 0.25 W, 2.7 Ω
$L_{dm1}/2$, $L_d/2$ $L_{dm2}/2$	Inductor	Magnetics, High-Flux Toroid 58083-A2, 28 turns, 15 AWG
L_{cm}	CM Choke	Vacuumschmelze, T60405-R6123-X221

CHAPTER 6

CONTROL OF THE CONVERTER

This chapter focuses on control of the investigated AC-DC converter operating as a rectifier with power correction capability. In this operating regime the main control objective is to ensure that a sinusoidal AC current is drawn from the utility grid, in phase with the utility grid voltage. Another important goal is to ensure a stable and properly regulated DC voltage at the output of the converter. In addition, it is desirable for this DC output voltage to have a good dynamic response. A common approach for simultaneously controlling both, the AC current and the DC voltage, is to apply a cascaded control scheme consisting of two control loops. In such a control scheme, the external voltage loop manipulates the AC current reference in order to maintain the DC voltage at the desired level, while the internal AC current control loop generates the reference signal for driving the transistors. As a result, a properly shaped AC current is drawn from the utility grid, with an amplitude required for maintaining the DC voltage on the predetermined level. The required shape of the AC current is imposed by the standards, in the form of maximum allowed harmonic currents injected into the grid, as explained in Section 2.2. In addition to achieving compliance with the harmonic limits specified in IEC 61000-3-2 [1], the control of the investigated AC-DC converter must be designed such that the THD of the AC current does not exceed 5 $\%$ within the operating range from 10 $\%$ to 100 $\%$ of the nominal operating power P_{nom}.

In the first part of this chapter, the input current and the output voltage control are derived for single cell operation of the converter within the positive half-period of AC voltage. Afterwards, the derived voltage and current controllers are incorporated within a cascaded control scheme for controlling the investigated interleaved AC-DC converter. Finally, the performance of the proposed control system is evaluated from the aspect of power quality.



a) b)

Figure 6.1: (a) Equivalent circuit of a hybrid modulated AC-DC converter for the positive half-period of AC voltage and (b) the corresponding current and voltage waveforms.

6.1 Current Control

An equivalent circuit of a hybrid modulated AC-DC converter for the positive half-period of AC voltage is presented in Fig. 6.1. By applying the Kirchhoff's voltage law (KVL) to the loop designated with V1, the AC voltage v_{ac} across the input terminals of the converter can be written as

$$v_{\mathrm{ac}}(t) = L\frac{di_{\mathrm{L}}(t)}{dt} + r\, i_{\mathrm{L}}(t) + v_{\mathrm{SL1}}(t), \tag{6.1}$$

where $v_{\mathrm{SL1}}(t)$ is the instantaneous drain-source voltage across the transistor $\mathrm{S_{L1}}$ and r the equivalent series resistance that combines the inductor's winding resistance R_{Ldc} and the drain-source on-resistance $R_{\mathrm{ds,on}}$ of one MOSFET in the conduction path. By neglecting the conduction during dead times as well as the skin effect and proximity effect in the inductor's winding, the value of r can be assumed as constant and independent of the switching states. It is evident from the theoretical waveforms on the right-hand side of Fig. 6.1, that the voltage $v_{\mathrm{SL1}}(t)$ is pulsating with an assumably ideal square wave waveform between 0 and the output DC voltage v_{dc}. On the basis of this simplification, its average value $v_{\mathrm{SL1avg}}(t)$ over one switching cycle T_{sw} is obtained as

$$v_{\mathrm{SL1avg}}(t) = \langle v_{\mathrm{SL1}}(t)\rangle_{T_{\mathrm{sw}}} = \frac{1}{T_{\mathrm{sw}}}\int\limits_{t}^{t+T_{\mathrm{sw}}} v_{\mathrm{SL1}}(\tau)\, d\tau = \langle v_{\mathrm{dc}}(t)\rangle_{T_{\mathrm{sw}}} \underbrace{\left(1 - \frac{\langle t_{\mathrm{on}}(t)\rangle_{T_{\mathrm{sw}}}}{T_{\mathrm{sw}}}\right)}_{\langle m(t)\rangle_{T_{\mathrm{sw}}}}, \tag{6.2}$$

where $\langle v_{\mathrm{dc}}(t)\rangle_{T_{\mathrm{sw}}}$ is the averaged value of the DC voltage over one switching period T_{sw}, $\langle t_{\mathrm{on}}(t)\rangle_{T_{\mathrm{sw}}}$ the averaged conduction state interval of $\mathrm{S_{L1}}$, and $\langle m(t)\rangle_{T_{\mathrm{sw}}}$ the voltage conversion ratio in the corresponding switching cycle. The averaged voltage conversion ratio $\langle m(t)\rangle_{T_{\mathrm{sw}}}$ is defined as

$$\langle m(t)\rangle_{T\mathrm{sw}} = \frac{\langle v_{\mathrm{ac}}(t)\rangle_{T_{\mathrm{sw}}}}{\langle v_{\mathrm{dc}}(t)\rangle_{T_{\mathrm{sw}}}}. \tag{6.3}$$

The same as for $v_{\mathrm{SL1}}(t)$ can be done for obtaining the average inductor current $i_{\mathrm{Lavg}}(t)$. Averaging all the time dependent variables in (6.1) over one switching period T_{sw} yields

$$L\frac{d\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{sw}}}}{dt} + r\,\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{sw}}} = \langle v_{\mathrm{ac}}(t)\rangle_{T_{\mathrm{sw}}} - \langle v_{\mathrm{dc}}(t)\rangle_{T_{\mathrm{sw}}}\langle m(t)\rangle_{T_{\mathrm{sw}}}. \tag{6.4}$$

The averaged model (6.4) must be linearized in order to be able to apply the linear control theory for designing the internal current control loop. For this purpose a new variable $\langle v_{\mathrm{i}}(t)\rangle_{T_{\mathrm{sw}}}$ which represents the output of a linear controller is introduced as

$$\langle v_{\mathrm{i}}(t)\rangle_{T_{\mathrm{sw}}} = \langle v_{\mathrm{ac}}(t)\rangle_{T_{\mathrm{sw}}} - \langle v_{\mathrm{dc}}(t)\rangle_{T_{\mathrm{sw}}}\langle m(t)\rangle_{T_{\mathrm{sw}}}. \tag{6.5}$$

Isolating the expression (6.5) for $\langle m(t)\rangle_{T_{\mathrm{sw}}}$ yields

$$\langle m(t)\rangle_{T_{\mathrm{sw}}} = \frac{1}{\langle v_{\mathrm{dc}}(t)\rangle_{T_{\mathrm{sw}}}}\left(\langle v_{\mathrm{ac}}(t)\rangle_{T_{\mathrm{sw}}} - \langle v_{\mathrm{i}}(t)\rangle_{T_{\mathrm{sw}}}\right), \tag{6.6}$$

which represents the linearization algorithm for the current control loop. On the basis of (6.4), and (6.6), a control scheme with feedback linearization can be designed for controlling the inductor current i_{L}, as shown in Fig. 6.2(a). For better transparency, a simplified representation of the averaged variables was adapted in the figure, where $x(t)$ denotes the average value $\langle x(t)\rangle_{T_{\mathrm{sw}}}$ over one switching period.

The shaded block on the left-hand side of the block scheme in Fig. 6.2(a) represents the linearization algorithm defined by (6.5), which compensates the controlled system's nonlinearity within the shaded block on the right-hand side of the figure. The modulator G_{m} represents the boundary between the controlling and the controlled part of the system. Therefore the output of the linearization algorithm, which represents the averaged voltage conversion ratio and at the same time the reference signal for driving the transistors, is designated with $m_{\mathrm{ref}}(t)$, while the actual voltage conversion ratio is labeled with $m(t)$.

As the operations within the shaded blocks in Fig. 6.2(a) cancel each other out, the control scheme can be simplified to the one shown in Fig. 6.2(b). The latter represents the linearized current control scheme in s-domain, which is more appropriate for selecting the compensator $G_{\mathrm{C,i1}}$ and its parameters. In addition, it allows for performing the frequency response analysis. The denotation $X(s)$ in Fig. 6.2(b) is used for representing the time domain average values $\langle x(t)\rangle$ in s-domain. The controlled plant G_{L} is transformed into s-domain by substituting (6.6) into (6.4) and applying

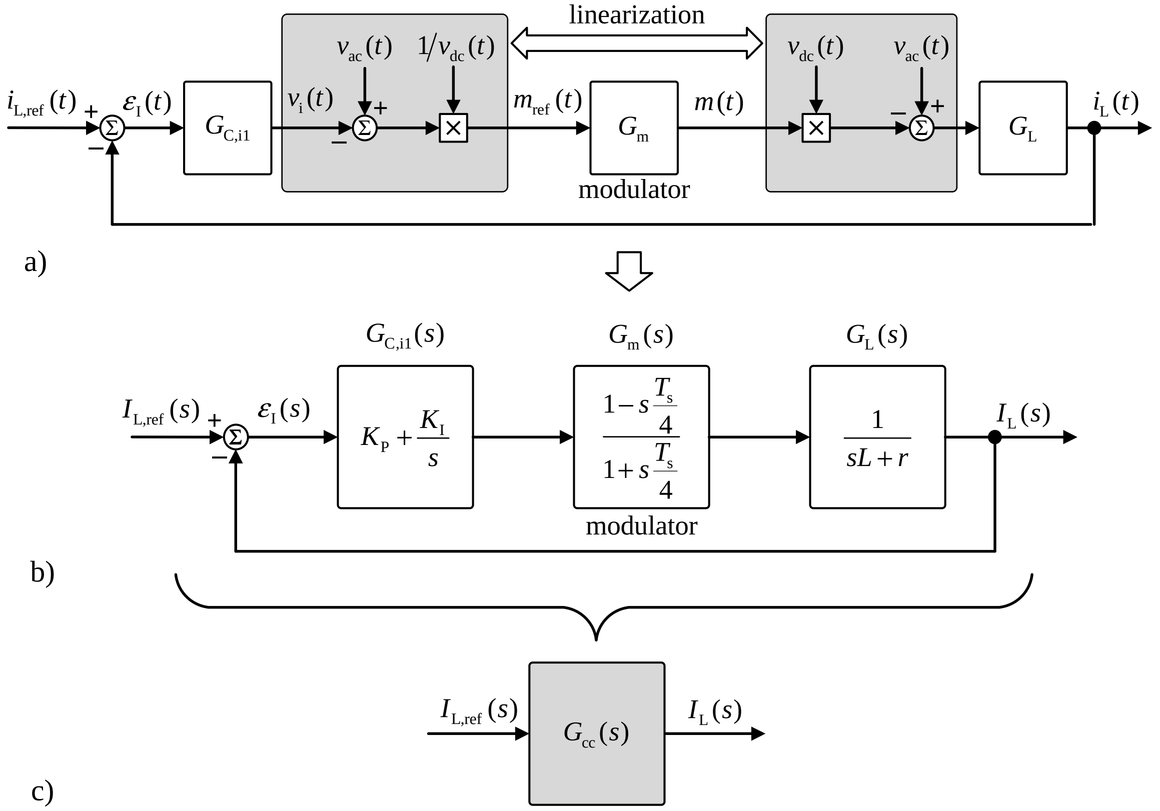

a)
linearization
$i_{L,ref}(t)$
$\varepsilon_I(t)$
$G_{C,i1}$
$v_i(t)$
$v_{ac}(t)$
$1/v_{dc}(t)$
$m_{ref}(t)$
G_m
modulator
$m(t)$
$v_{dc}(t)$
$v_{ac}(t)$
G_L
$i_L(t)$
b)
$G_{C,i1}(s)$
$G_m(s)$
$G_L(s)$
$I_{L,ref}(s)$
$\varepsilon_I(s)$
$K_p + \frac{K_I}{s}$
$\frac{1-s\frac{T_s}{4}}{1+s\frac{T_s}{4}}$
modulator
$\frac{1}{sL+r}$
$I_L(s)$
c)
$I_{L,ref}(s)$
$G_{cc}(s)$
$I_L(s)$

Figure 6.2: Block diagram representation of the current control loop (a) in time domain, (b) in s-domain, and (c) as a single block representing the current controller's simplified closed loop transfer function $G_{\mathrm{cc}}(s)$.

Laplace transform over the obtained expression, which yields

$$G_{\mathrm{L}}(s) = \frac{I_{\mathrm{L}}(s)}{V_{\mathrm{i}}(s)} = \frac{1}{sL + r}. \tag{6.7}$$

In a digital implementation of the control, the modulator introduces a certain delay since the update of the reference signal for driving the transistors is performed only at the beginning of each switching cycle. In the presented case, the modulator's response delay was modeled by its first-order Padé approximation as

$$G_{\mathrm{m}}(s) = \frac{1 - s\frac{T_{\mathrm{s}}}{4}}{1 + s\frac{T_{\mathrm{s}}}{4}}, \tag{6.8}$$

where $G_{\mathrm{m}}(s)$ is the modulator's transfer function and T_{s} the sampling period, which also corresponds with the control algorithm execution cycles and modulator's update cycles. For converters operating with a high switching frequency and utilizing a digital average current control, as is the case with the investigated AC-DC converter, the sampling time T_{s} does not have to equal the switching period T_{sw}. Since the variation of the controlled variable's average value over one switching cycle is insignificant, the sampling time T_s can be an integer multiple of the switching period T_s, defined as

$$T_\mathrm{s} = m\,T_\mathrm{sw}; \quad m = 1,\ 2,\ 3... \tag{6.9}$$

The main benefit of such sampling strategy is in loosening the limitations imposed by the DSC on the maximum achievable switching frequency, while the performance of the control system is not considerably alleviated.

The importance of the modulator's delay approximated with (6.8) and its influence on the controlled system depends on the ratio between the system's and the modulator's time constants. In the discussed case the modulator's delay can be neglected only if the following condition is fulfilled:

$$\frac{T_\mathrm{s}}{4} \ll \frac{L}{r}. \tag{6.10}$$

By considering the minimum allowed switching frequency of $f_\mathrm{sw,min} = 25\,\mathrm{kHz}$, converter's parameters specified in Chapter 5, and execution of the control algorithm in every second switching cycle ($m = 2$), the system's time constant is at least 10 times larger than the modulator's time constant. For this reason, the modulator's response delay can be neglected when designing the control and the system to be controlled is reduced to $G_\mathrm{L}(s)$, which is a first-order system. A proportional-integral (PI) controller was used as the compensator $G_\mathrm{C,i1}(s)$. Its parameters can be tuned such that the poles in $G_\mathrm{L}(s)$ are compensated and the entire current control can be simplified into a single block, as shown in Fig. 6.2(c). The latter represents a first order system with a transfer function

$$G_\mathrm{cc}(s) = \frac{1}{1 + s\frac{1}{2\pi f_\mathrm{cc}}}, \tag{6.11}$$

where f_cc is the current controller's cutoff frequency which determines its bandwidth. The obtained simplified model of the current control loop will be used for designing the DC voltage control in the following section. For the presented case, the PI controller's parameters were selected as $K_\mathrm{P} = 1.55$ and $K_\mathrm{I} = 3393$, resulting in a cutoff frequency of $f_\mathrm{cc} = 3000$ Hz.

6.2 Voltage Control

Applying the Kirchhoff's current law on the node designated with I1 in Fig. 6.1 gives

$$i_\mathrm{SH1}(t) = i_\mathrm{C}(t) + i_\mathrm{dc}(t), \tag{6.12}$$

where $i_\mathrm{SH1}(t)$ is the current flowing through the transistor $\mathrm{S_{H1}}$ towards the output stage of the converter, $i_\mathrm{C}(t)$ the current through the DC-side capacitor, and $i_\mathrm{dc}(t)$ the converter's output current for supplying the load. The currents $i_{\mathrm{C}}(t)$ and $i_{\mathrm{dc}}(t)$ can be written as

$$i_{\mathrm{C}}(t) = C_{\mathrm{dc}} \frac{dv_{\mathrm{dc}}(t)}{dt}, \tag{6.13a}$$

$$i_{\mathrm{dc}}(t) = \frac{1}{R} v_{\mathrm{dc}}(t), \tag{6.13b}$$

where R is the load resistance, C_{dc} the capacitance of the DC-side capacitor bank, and v_{dc} the controlled DC output voltage of the converter.

Assuming a perfect current control and an ideal AC voltage waveform, free of any harmonics above fundamental, the instantaneous input power $p_{\mathrm{ac}}(t)$ of the investigated DC-AC converter can be written as

$$p_{\mathrm{ac}}(t) = v_{\mathrm{ac}}(t)\, i_{\mathrm{ac}}(t) = \hat{V}_{\mathrm{ac}}(t) \hat{I}_{\mathrm{ac}}(t) \sin^2(\omega t)\,, \tag{6.14}$$

where $\hat{V}_{\mathrm{ac}}(t)$ and $\hat{I}_{\mathrm{ac}}(t)$ are instantaneous AC voltage and current magnitudes, respectively. On the other hand, the converter's output power $p_{\mathrm{o}}(t)$ can be represented as

$$p_{\mathrm{o}}(t) = i_{\mathrm{SH1avg}}(t)\, v_{\mathrm{dc}}(t), \tag{6.15}$$

where $i_{\mathrm{SH1avg}}(t)$ is the average value of $i_{\mathrm{SH1}}(t)$ over one switching period T_{sw}. It must be pointed out that the main purpose of the external voltage control loop is to determine the amount of power that has to be drawn from the source for maintaining the DC-side voltage v_{dc} on the desired level. As the AC voltage v_{ac} in grid connected applications is fixed and cannot be significantly affected by rather small local loads, the power drawn from the utility grid can be manipulated exclusively by varying the AC current's magnitude $\hat{I}_{\mathrm{ac}}(t)$ when operating with a close to unity power factor, as evident from (6.14). Since the input filter, interfacing the converter's power circuit and the utility grid, does not influence the phase and the magnitude of the low frequency harmonic components of $i_{\mathrm{ac}}(t)$, the latter can be replaced by the average inductor current $i_{\mathrm{Lavg}}(t) = \hat{I}_{\mathrm{Lavg}}(t) \sin(\omega t)$.

Due to the discussed converter's high power conversion efficiency within the entire operating range, the generated power losses can be neglected and the instantaneous output power $p_{\mathrm{o}}(t)$ can be considered equal to the instantaneous input power $p_{\mathrm{ac}}(t)$. Consequently, the average current $i_{\mathrm{SH1avg}}(t)$ flowing into the output stage of the converter can be obtained on the basis of (6.14) and (6.15) as

$$i_{\mathrm{SH1avg}}(t) = \frac{\hat{V}_{\mathrm{ac}}(t)\, \hat{I}_{\mathrm{Lavg}}(t)}{v_{\mathrm{dc}}(t)} \sin^2(\omega t)\,. \tag{6.16}$$

In order to avoid any unwanted line current distortion caused by the presence of the higher order harmonics within the current controller's reference signal $i_{\mathrm{L,ref}}$, the bandwidth of the voltage control loop has to be lower than the line frequency of $f_{\mathrm{L}} = 50\,\mathrm{Hz}$. Under such conditions, the voltage control loop can be designed on the basis of a low frequency model, in which all the involved variables are averaged across one AC voltage half period $T/2$. Averaging (6.16) over $T/2$ yields

$$\langle i_{\mathrm{SH1avg}}(t)\rangle_{T/2} = \frac{2}{T}\int_{t}^{t+T/2} i_{\mathrm{SH1avg}}(\tau)d\tau = \frac{\left\langle \hat{V}_{\mathrm{ac}}(t)\right\rangle_{T/2}\left\langle \hat{I}_{\mathrm{ac}}(t)\right\rangle_{T/2}}{2\left\langle v_{\mathrm{dc}}(t)\right\rangle_{T/2}}, \tag{6.17}$$

where $\langle i_{\mathrm{SH1avg}}(t)\rangle_{T/2}$ is the average current flowing towards the output stage of converter, $\langle v_{\mathrm{dc}}(t)\rangle_{T/2}$ the average voltage on the DC-side capacitor C_{dc}, and $\left\langle \hat{V}_{\mathrm{ac}}(t)\right\rangle_{T/2}$ and $\left\langle \hat{I}_{\mathrm{ac}}(t)\right\rangle_{T/2}$ the averaged magnitudes of AC voltage and current over one AC voltage half-period.

Averaging (6.12) over $T/2$ and subsequently inserting (6.17) into the obtained expression yields

$$C_{\mathrm{dc}}\frac{d\langle v_{\mathrm{dc}}(t)\rangle_{T/2}}{dt} + \frac{1}{R}\langle v_{\mathrm{dc}}(t)\rangle_{T/2} = \frac{\left\langle \hat{V}_{\mathrm{ac}}(t)\right\rangle_{T/2}\left\langle \hat{I}_{\mathrm{Lavg}}(t)\right\rangle_{T/2}}{2\left\langle v_{\mathrm{dc}}(t)\right\rangle_{T/2}}, \tag{6.18}$$

which represents the low frequency model of the system to be controlled by the external control loop. Like in the case of designing the current controller, the system equation is non-linear. In order to compensate the nonlinearities, a new variable $\langle v_v(t)\rangle_{T/2}$ is introduced as

$$\langle v_v(t)\rangle_{T/2} = \frac{\left\langle \hat{V}_{\mathrm{ac}}(t)\right\rangle_{T/2}\left\langle \hat{I}_{\mathrm{ac}}(t)\right\rangle_{T/2}}{2\left\langle v_{\mathrm{dc}}(t)\right\rangle_{T/2}}, \tag{6.19}$$

By isolating (6.19) for $\left\langle \hat{I}_{\mathrm{Lavg}}(t)\right\rangle_{T/2}$ and assuming a perfect current control which allows for replacing $\left\langle \hat{I}_{Lavg}(t)\right\rangle_{T/2}$ with its reference, the voltage control linearization algorithm is obtained as

$$\left\langle \hat{I}_{\mathrm{L,ref}}(t)\right\rangle_{T/2} = \frac{2\langle v_v(t)\rangle_{T/2}\langle v_{\mathrm{dc}}(t)\rangle_{T/2}}{\left\langle \hat{V}_{\mathrm{ac}}(t)\right\rangle_{T/2}}, \tag{6.20}$$

where $\left\langle \hat{I}_{\mathrm{L,ref}}(t)\right\rangle_{T/2}$ is the peak current reference, which represents the input of the internal current control loop.

On the basis of (6.18) and (6.20) the DC voltage control loop with feedback linearization can be designed as shown in Fig. 6.3(a). The block scheme in Fig. 6.3(a) depicts the low frequency model of the external voltage control loop, in which all the involved variables are averaged over one AC voltage half-period. A simplified representation of the variables was adapted, according to which the averaged values $\langle x(t)\rangle_{T/2}$ are represented simply as $x(t)$. The block that separates the controlled system in the right-hand side of the scheme from the controlling system on the opposite side of the scheme represents the internal current control loop. The latter has to ensure a high quality sinusoidal waveform of the current i_{L}, which must be in phase with the AC voltage v_{ac} for

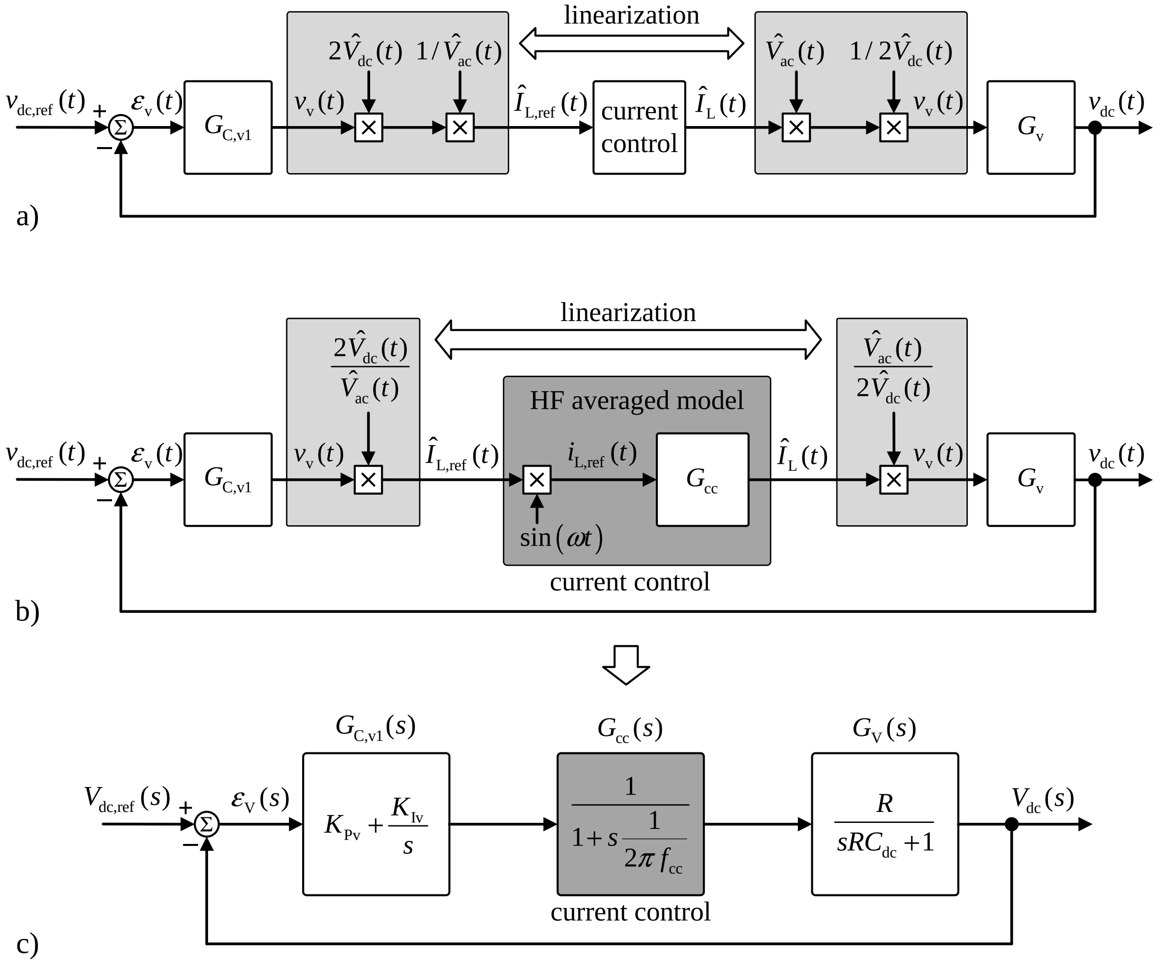

linearization
$2\hat{V}_{dc}(t)$
$1/\hat{V}_{ac}(t)$
$\hat{V}_{ac}(t)$
$1/2\hat{V}_{dc}(t)$
$v_{dc,ref}(t)$
$\varepsilon_v(t)$
$G_{C,v1}$
$v_v(t)$
$\hat{I}_{L,ref}(t)$
current control
$\hat{I}_L(t)$
G_v
$v_{dc}(t)$
a)
$\frac{2\hat{V}_{dc}(t)}{\hat{V}_{ac}(t)}$
$\frac{\hat{V}_{ac}(t)}{2\hat{V}_{dc}(t)}$
HF averaged model
$i_{L,ref}(t)$
G_{cc}
$\sin(\omega t)$
b)
$G_{C,v1}(s)$
$G_{cc}(s)$
$G_V(s)$
$V_{dc,ref}(s)$
$\varepsilon_V(s)$
$K_{Pv}+\frac{K_{Iv}}{s}$
$\frac{1}{1+s\frac{1}{2\pi f_{cc}}}$
$\frac{R}{sRC_{dc}+1}$
$V_{dc}(s)$
c)

Figure 6.3: Block diagrams of the voltage control loop: (a) basic time domain representation of the LF model, (b) extended time domain representation indicating the necessary current reference adaptation and interaction with the HF averaged model of the internal current control loop, (c) s-domain representation for frequency response analysis and tuning the controller's parameters.

achieving operation with a unity power factor. In order to satisfy both criteria, the current reference $i_{\mathrm{L,ref}}(t)$ must have the following form:

$$i_{\mathrm{L,ref}}(t) = \hat{I}_{\mathrm{L,ref}}(t)\sin(\omega t)\,, \tag{6.21}$$

while the argument ωt must coincide with the angle of the AC voltage v_{ac}. The required adaptation of the peak reference current $\hat{I}_{\mathrm{L,ref}}(t)$ obtained from the external voltage control loop is evident from the extended block presented in Fig. 6.3(b). This figure also indicates that the proposed cascaded control scheme combines two models in different time scales. Due to the fast dynamics of the input current, the internal control loop was derived on the basis of a high frequency (HF) averaged model (6.4). On the other hand, the external voltage control loop was derived on the basis of the low frequency (LF) model (6.18), in order to eliminate the time varying components from the DC-side voltage and current. For ensuring adequate performance of the cascaded control scheme and a proper time scale separation between the fast AC current and slow DC voltage dynamics, the crossover frequency of the voltage control loop f_{vc} must be set well below the fundamental frequency of the AC voltage f_{L}. On the other hand, the cutoff frequency f_{cc} of the internal current control loop was set much higher than f_{L}, at $f_{\mathrm{cc}} = 3000\mathrm{Hz}$, which allows for proper tracking of the sinusoidal current reference.

An s-domain representation of the simplified linearized external control loop is provided in Fig. 6.3(c). The system to be controlled consists of a series connection of the simplified current control's transfer function $G_{\mathrm{cc}}(s)$ and the transfer function $G_{\mathrm{v}}(s)$. The latter is obtained by substituting (6.19) into (6.18) and applying Laplace transform over the obtained expression, which finally yields

$$G_{\mathrm{v}}(s) = \frac{V_{\mathrm{dc}}(s)}{V_{\mathrm{v}}(s)} = \frac{R}{sRC_{\mathrm{dc}} + R}. \tag{6.22}$$

The first order approximation of the current control's transfer function $G_{\mathrm{cc}}(s)$ is given by (6.11). Like in the case of the internal current control loop, a PI controller was selected as the compensator $G_{\mathrm{C,v1}}(s)$. By setting the PI controller's parameters to $K_{\mathrm{Pv}} = 0.08$ and $K_{\mathrm{I}} = 4.7$, the voltage control loop's bandwidth is limited to 15 Hz.

6.3 Synthesis of the control system

The input current and voltage control derived in the preceding section have to be properly combined and adapted for controlling the interleaved AC-DC converter operating with a variable switching frequency. The entire system control is depicted in Fig. 6.4.

Due to the analogy between the converter's operation within the positive and the negative half-periods of AC voltage, the voltage and current controllers derived for the positive half-period can be utilized within the negative half-period as well. However, this can be done only in the case where the modulation strategy is adequately adapted at the zero-crossing of AC voltage. The AC voltage zero crossings are especially critical in hybrid modulated H-bridge converters, as they demand for a change in the converter's structure. The demanded change in the structure is executed by complementary switching of the transistors within the LF bridge leg at the reversal of AC voltage's polarity and a switch in the roles of transistors within the HF bridge leg (see Section 2.4). Therefore, the duty cycle of one transistor in a HF switched bridge leg instantly jumps from 0 to 1, while the duty cycle of the other one instantly falls from 1 to 0. As the modulation reference m_{ref} calculated by the

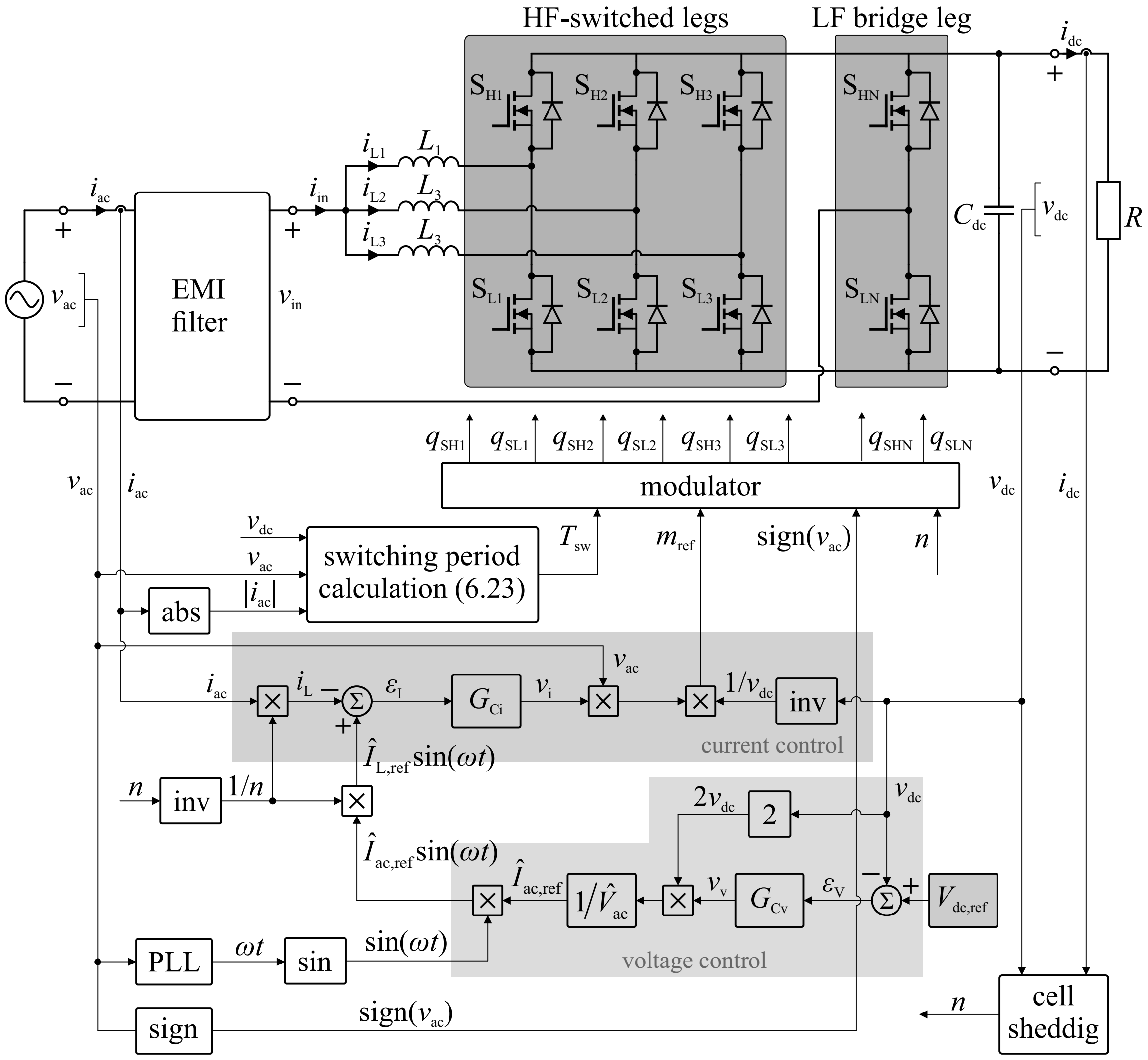

HF-switched legs
LF bridge leg
S_{H1}
S_{H2}
S_{H3}
S_{HN}
S_{L1}
S_{L2}
S_{L3}
S_{LN}
i_{dc}
+
C_{dc}
v_{dc}
R
−
i_{L1}
L_1
i_{L2}
L_3
i_{L3}
L_3
i_{ac}
i_{in}
+
+
v_{ac}
EMI filter
v_{in}
−
−
q_{SH1}
q_{SL1}
q_{SH2}
q_{SL2}
q_{SH3}
q_{SL3}
q_{SHN}
q_{SLN}
modulator
v_{ac}
i_{ac}
v_{dc}
i_{dc}
v_{dc}
v_{ac}
switching period calculation (6.23)
$|i_{ac}|$
abs
T_{sw}
m_{ref}
sign(v_{ac})
n
v_{ac}
i_{ac}
i_L
−
Σ
+
ε_I
G_{Ci}
v_i
$1/v_{dc}$
inv
current control
$\hat{I}_{L,ref}\sin(\omega t)$
n
inv
$1/n$
$2v_{dc}$
2
v_{dc}
$\hat{I}_{ac,ref}\sin(\omega t)$
$\hat{I}_{ac,ref}$
$1/\hat{V}_{ac}$
v_v
G_{Cv}
ε_V
−
+
Σ
$V_{dc,ref}$
PLL
ωt
sin
$\sin(\omega t)$
voltage control
n
cell sheddig
sign
sign(v_{ac})

Figure 6.4: Simplified block diagram of the converter's control.

current control loop corresponds with the duty cycle of one of the transistors within a HF switched bridge leg, the modulation strategy has to ensure that the calculated m_{ref} is recognized as the reference duty cycle for the high-side transistors $\mathrm{S_{H1}}$, $\mathrm{S_{H2}}$, and $\mathrm{S_{H3}}$ within the positive half-period and as the reference duty cycle for the low-side transistors $\mathrm{S_{L1}}$, $\mathrm{S_{L2}}$, and $\mathrm{S_{L3}}$ within the negative half period of AC voltage. By doing so, the proposed control scheme can be used over the entire period of AC voltage with its output being a continuous signal in steady state operation, despite the discrete changes in the converter's structure at zero crossings of AC voltage. The switching of the LF bridge transistors and the roles of transistors within HF bridge legs are consequently determined by the polarity of AC voltage. Its detection is depicted in Fig. 6.4 by applying the "sign" operation over the sensed voltage v_{ac} and passing the obtained information about the sign of AC voltage to the modulator.

In order to ensure safe and reliable operation with multiple interleaved cells, the modulator must continuously maintain such phase shift between the PWM carrier signals for each HF bridge leg that the switching instants of transistors within active cells occur sequentially in specific time intervals defined by the number of active cells and the instantaneous switching period. The duration of the time intervals between switching instants in different HF bridge legs varies over time even in steady state, as the investigated converter operates with a variable switching frequency which depends on the AC voltage.

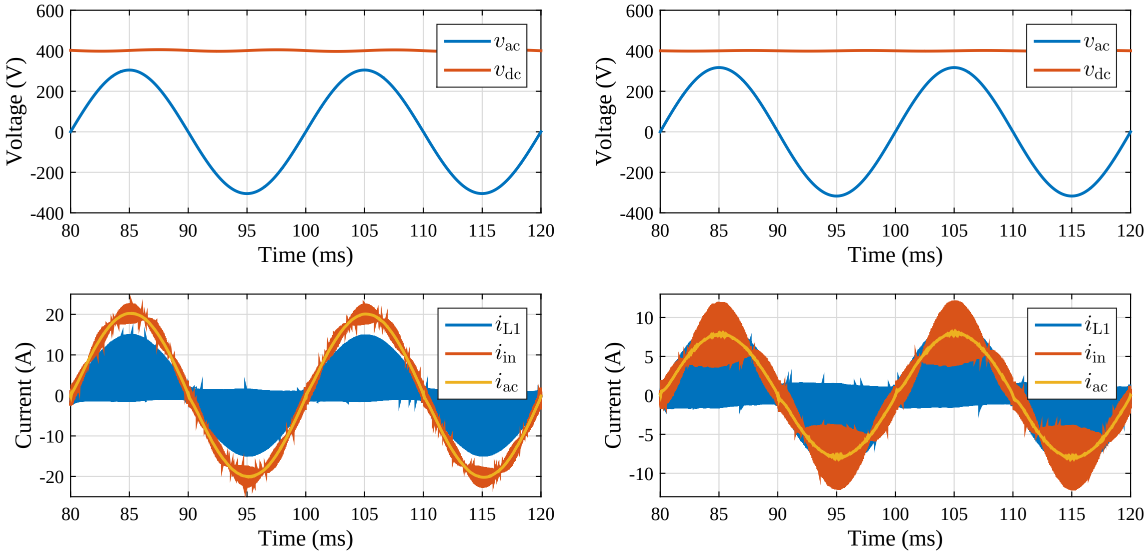
Several modifications have to be incorporated into the cascaded control scheme presented in Sections 8.1 and 8.2 for its utilization in the investigated interleaved converter. The current control loop shown in Fig. 6.2(b) has been designed for controlling the current through one of the inductors L_1, L_2, or L_3. It has also been assumed that the current through that specific inductor is directly sensed and used in the feedback loop. However, due to the operation in DCM with a high inductor current ripple at frequencies above 100 kHz, direct sensing of the inductor current in AC applications is quite challenging. The Hall-effect sensors available on the market neither provide a sufficient bandwidth, nor a satisfactory step response, which is crucial at higher rates of current change. Not because an extremely high bandwidth current measurement would be required, but because the exposed drawbacks introduce time delays into the LF components of the sensed signal which is unacceptable for operation with variable switching frequency. On the other hand, the current sensing transformers may provide a sufficient bandwidth and dynamic response. Nonetheless, they may also introduce additional losses into the circuit and therefore their utilization was avoided. The current sensing issue is easily solved by sensing the current on the grid side of the input EMI filter, as shown in Fig. 6.4. In this point of the circuit, the current is essentially sinusoidal with a fundamental frequency of 50 Hz and an insignificant content of higher-order harmonics. Therefore, a Hall-effect sensor can be used without introducing an observable delay into the sensed signal. By placing the current sensor to the grid side of the input filter, the conditions assumed when deriving the current control loop change, as the EMI filer is inserted into the system. In such case, it must be ensured that the filter does not interfere with the controlled system within the frequency range of the controller's bandwidth. As the lowest-in-magnitude resonant peak in the attenuation characteristic of the EMI filter presented in Section 5.5 appears at the frequency of approximately 6 kHz and the filter's output impedance-based control stability criterion [156] is fulfilled within the entire control bandwidth, the presence of the input filter was neglected in the system control design. Consequently it was assumed that the sensed current i_{ac} equals the average current through all the inductors $i_{\mathrm{in,avg}}$. Since the current control has been designed for controlling the current through one inductor, proper scaling of the sensed current i_{ac} is required. The scaling factor is determined by the number of active switching cells n. In accordance with the phase shedding strategy proposed in Section 5.4, the number of active cells is gradually decreased when the operating power is decreasing. The phase shedding strategy is implemented by fitting the calculated value of the instantaneous output power P_{dc} into the operating ranges defined in Section 5.4. The outcome is the number of active interleaved cells n. The latter represents the factor for scaling the sensed current i_{ac} to obtain the current i_{L} through a single power inductor. In addition to scaling the sensed current i_{ac} on the basis of the number of active interleaved cells, the reference current $\hat{I}_{\mathrm{ac,ref}}$ obtained from the voltage control loop must be divided by n as well. By scaling both the sensed current i_{ac} and the reference current $\hat{I}_{\mathrm{ac,ref}}$ according with n, the current controller's bandwidth remains unaffected by the number of active interleaved cells and constant over the entire operating range of the investigated AC-DC converter. In order to avoid unnecessary introduction of the AC voltage distortion into the current reference, a phase-locked loop (PLL) with a modified-mixer phase detector [157] is utilized for generating a purely sinusoidal waveform in phase with the AC voltage.

As presented in Section 4.5, the switching period of the discussed converter varies with time, voltage conversion ratio, and the load conditions. The expression (4.29) according to which the switching period T_{sw} has to vary in order to achieve the desirable magnitude of the reversed current I_{R} within each switching cycle is valid for single cell operation only, where the current through a single power inductor is sensed. By assuming a symmetrical structure of the converter and a perfect sharing of current between the HF bridge legs, the expression (4.29) can be extended for usage in an interleaved AC-DC converter as

$$T_{\mathrm{sw}} = 2L \frac{v_{\mathrm{dc}}}{\left(v_{\mathrm{dc}} - v_{\mathrm{ac}}\right) v_{\mathrm{ac}}} \left(\frac{|i_{\mathrm{ac}}|}{n} - I_{\mathrm{R}} \right), \tag{6.23}$$

where L is the inductance of a single power inductor, I_{R} the predetermined desirable magnitude of the reversed current, n the number of interleaved cells, v_{dc} and v_{ac} the sensed values of the DC and AC voltage, respectively, and $|i_{\mathrm{ac}}|$ the absolute value of the sensed AC current. By varying the switching period according to (6.23), ZVS can be maintained within the entire operating range of the converter, independent of the number of active interleaved cells.

The performance of the proposed control scheme was tested by simulation. The results presented in Fig. 6.5 indicated that a sinusoidal AC current i_{ac} is drawn from the power source. On the other hand, the voltage v_{dc} is controlled at 400 V, which corresponds with the voltage reference $V_{\mathrm{dc,ref}}$. The current i_{L1} flowing through a single power inductor has the desirable waveform with a rather constant magnitude of the reversed current I_{R} that ensure ZVS of the transistors within the HF switched bridge legs. The variations of the reversed current's magnitude around its predeter-

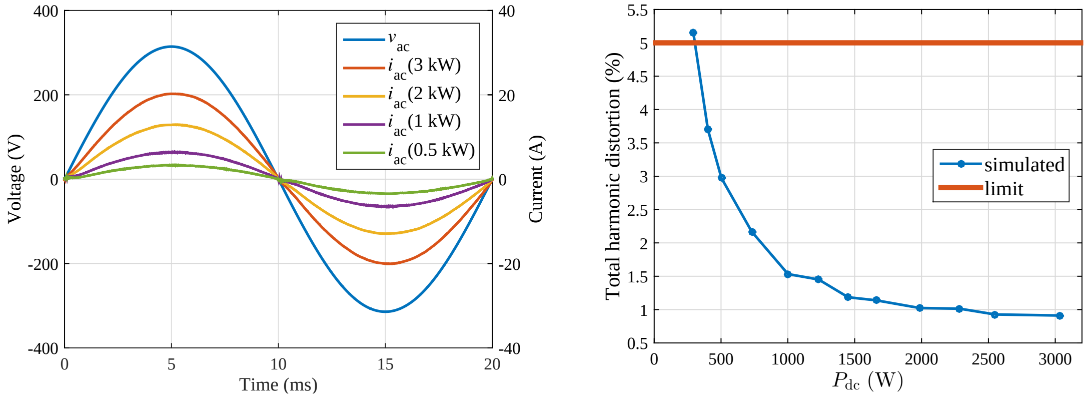


(a) (b)

Figure 6.5: Simulation results for operating with (a) three interleaved cells at the power of $P_{\mathrm{dc}} = 3030$ W and (b) two interleaved cells at the power of $P_{\mathrm{dc}} = 1230$ W.

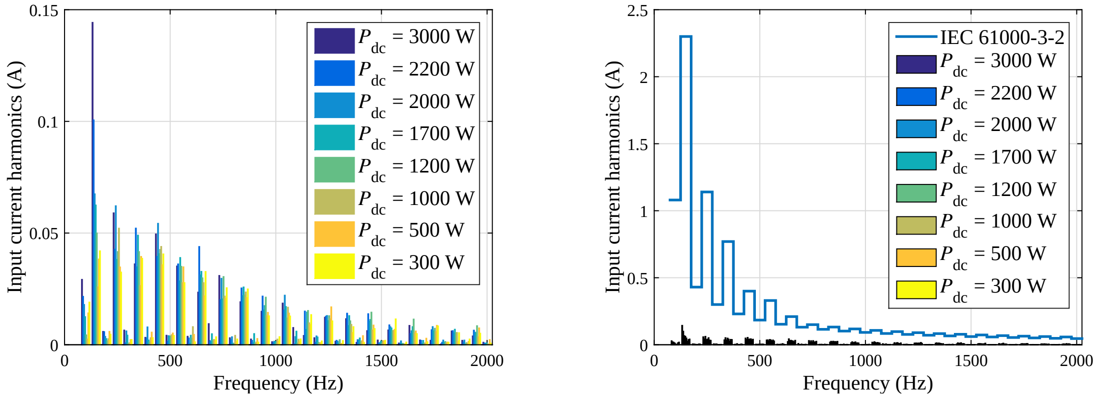
mined value occur as a consequence of the switching period estimation according to (6.23). The sensed values of v_{dc}, v_{ac}, and i_{ac} contain higher order harmonics which distort the theoretical shape of switching frequency variation depicted in Fig. 4.19. In a close to ideal simulation environment, the 100 Hz ripple in the output DC voltage v_{dc} represents the main source of switching period waveform distortion and accompanying fluctuation of the reversed current's magnitude around the desirable value of $I_{\mathrm{R}} = -1.3$ A. It is also evident from the current waveforms presented in Fig. 6.5 that the current i_{in} on the converter side of the input EMI filter has a lower magnitude of the HF ripple when operating with 3 interleaved cells than in the case of two cell operation.

The AC current and voltage waveforms presented in Fig. 6.6(a) indicate that the proposed control shapes the input AC current i_{ac} in phase with the AC voltage v_{ac}, which yields a close to unity displacement factor K_{disp} (see Section 2.1. The remaining condition for achieving operation with a close to unity power factor is low current distortion. The level of current distortion is commonly measured by THD. As specified in Table 5.1, the THD of the investigated AC-DC converter's input current i_{ac} must be lower than 5 %, within the entire operating range between 10 % and 100 % of the nominal output power. The results of THD analysis are shown in Fig. 6.6(b) and confirm a low distortion of the converter's input current i_{ac}. Operation with a close to unity power factor is ensured by maintaining the THD within the specified limits and achieving a low displacement factor K_{disp} by shaping the AC current in phase with voltage.



(a) (b)

Figure 6.6: (a) AC input current i_{ac} in respect to AC voltage v_{ac} at different operating powers. (b) Total harmonic distortion of the AC input current.



(a) (b)

Figure 6.7: (a) Higher order harmonics in the input current at different operating powers and (b) their comparison to the harmonic current limits specified in IEC 61000-3-2 [1].

The THD characteristic of the converter's input current i_{ac} presented in Fig. 6.6(b) was obtained on the basis of harmonic analysis, the results of which are shown in Fig. 6.7. The compliance with the harmonic limits specified in IEC 61000-3-2 [1] was verified by comparing each harmonic component of i_{ac} with the limits defined in the standard (see Table 2.1). As the standard [1] specifies the limits for Class A and B equipment in absolute values and applies for the equipment connected to the utility grid that draws a current of less or equal to 16 A per phase, the limits may appear as very loose for a 3 kW converter, such as investigated within this thesis. This is confirmed in Fig. 6.7(b), from which it is evident that the harmonic content of the current i_{ac} is well below the specified limits within the entire operating range of the converter.

CHAPTER 7

EXPERIMENTAL RESULTS

The purpose of this chapter is to experimentally verify the proposed control scheme and evaluate power conversion efficiency over the entire operating range of the converter. According to the design procedure described in Chapter 5, an experimental prototype of the investigated interleaved AC-DC converter was built. The experimental prototype is shown in Fig. 7.1, in which the constituting components of the converter are labeled. The control was implemented into the Texas Instruments' Delfino C28343 Control Card.

The experimental voltage and current waveforms in Fig. 7.2 demonstrate proper interleaving operation of the converter. It is evident that the inductor current waveforms are sequentially shifted for one third of the switching period in the case of three cell operation represented by Fig. 7.2(a). On the other hand, the inductor current waveforms and the corresponding switching instants are shifted for a half of the switching period when operating with two interleaved cells, as can be observed in Fig. 7.2(b). The square-wave like pulsating waveforms in Fig. 7.2 represent the drain-source voltage v_{dsL1} of the low-side MOSFET $\mathrm{S_{L1}}$, which exhibits practically no overshoot at the voltage of $v_{\mathrm{dc}} = 400$ V.

In order to evaluate the performance of the experimental converter utilizing the proposed control scheme, power conversion efficiency was measured over its entire operating range. A Norma D 6100 Wide Band Power Analyzer was used for performing this task. The measured efficiency characteristics for operating with a different number of interleaved cells are shown in Fig. 7.3(a), while the corresponding power loss characteristic is shown in Fig. 7.3(b). It can be observed that the peak efficiency of 98.4 % is achieved at the output power of $P_{\mathrm{dc}} = 1100$ W, when two interleaved cells are active. Furthermore, the power conversion efficiency is maintained above 98 % within

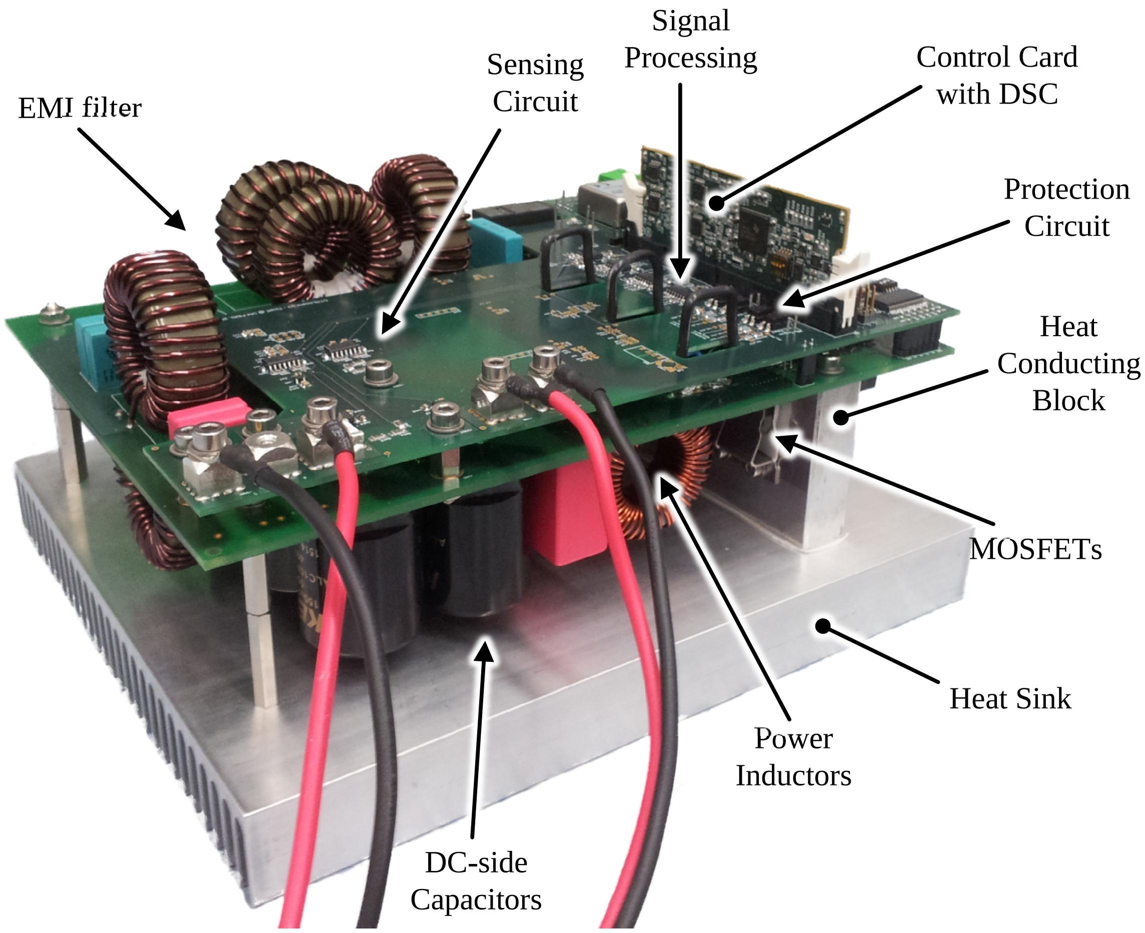
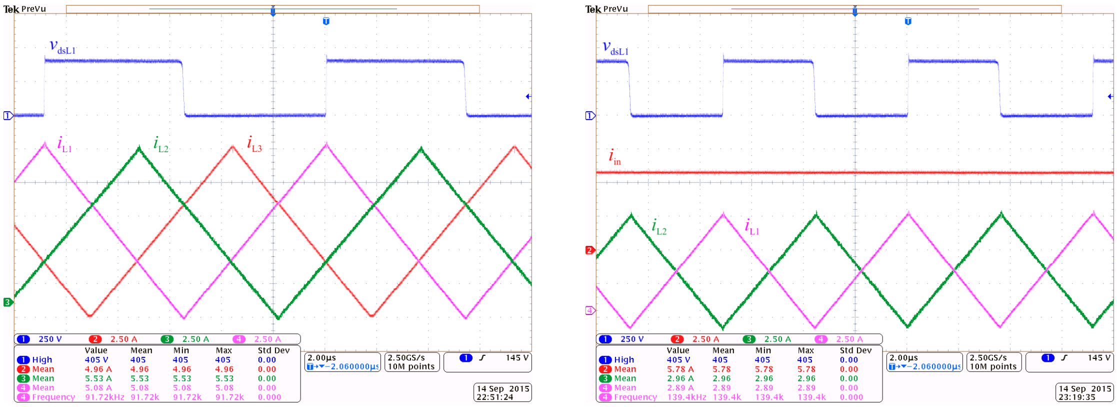

EMI filter
Sensing Circuit
Signal Processing
Control Card with DSC
Protection Circuit
Heat Conducting Block
MOSFETs
Heat Sink
Power Inductors
DC-side Capacitors

Figure 7.1: Experimental prototype of the investigated interleaved AC-DC converter.



```
1  250 V      2  2.50 A     3  2.50 A     4  2.50 A
               Value     Mean     Min      Max      Std Dev
1 High         405 V     405      405      405      0.00
2 Mean         4.96 A    4.96     4.96     4.96     0.00
3 Mean         5.53 A    5.53     5.53     5.53     0.00
4 Mean         5.08 A    5.08     5.08     5.08     0.00
4 Frequency    91.72kHz  91.72k   91.72k   91.72k   0.000
2.00µs  T→▼−2.060000µs   2.50GS/s 10M points   1 ſ 145 V
14 Sep 2015 22:51:24
```

```
1  250 V      2  2.50 A     3  2.50 A     4  2.50 A
               Value     Mean     Min      Max      Std Dev
1 High         405 V     405      405      405      0.00
2 Mean         5.78 A    5.78     5.78     5.78     0.00
3 Mean         2.96 A    2.96     2.96     2.96     0.00
4 Mean         2.89 A    2.89     2.89     2.89     0.00
4 Frequency    139.4kHz  139.4k   139.4k   139.4k   0.000
2.00µs  T→▼−2.060000µs   2.50GS/s 10M points   1 ſ 145 V
14 Sep 2015 23:19:35
```

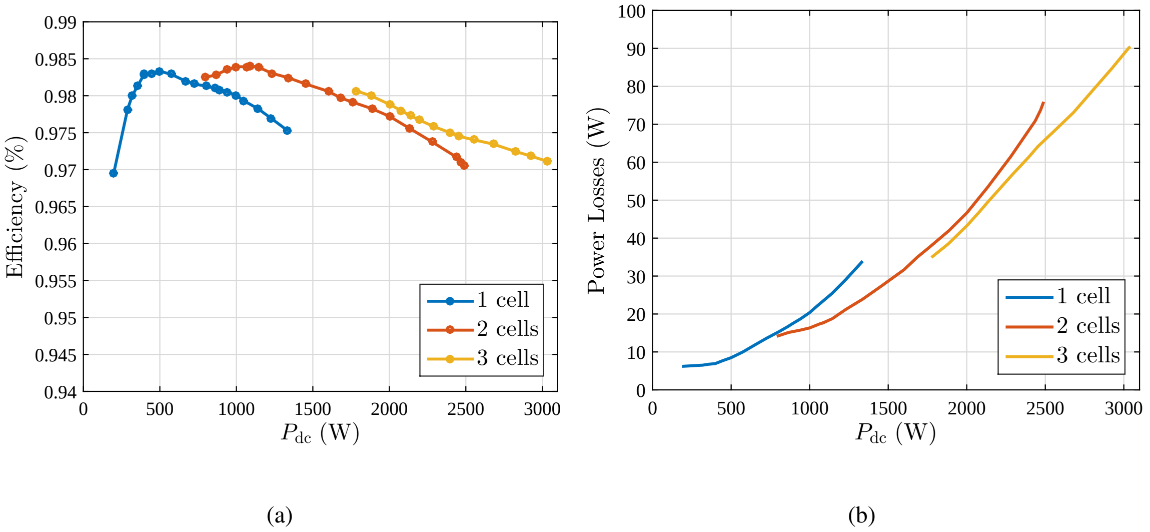
(a) (b)

Figure 7.2: Operation in boost mode with (a) three interleaved cells at the power of $P_{\mathrm{dc}} = 3$ kW and (b) two interleaved cells at the power of $P_{\mathrm{dc}} = 1.1$ kW.

the operating range between $P_{\mathrm{dc}} = 300$ W and $P_{\mathrm{dc}} = 1850$ W, and above 97 % within the range between $P_{\mathrm{dc}} = 200$ W and $P_{\mathrm{dc}} = 3050$ W. The efficiency characteristics in Fig. 7.3(a) indicate that the peak efficiency is achieved at the power of approximately 500 W per interleaved cell, which yields the maximum efficiency at 500 W for single cell operation, at approximately 1000 W for operation with two interleaved cells and most probably at 1500 W for the case of three interleaved cells. In comparison with the estimated power conversion efficiency shown in Fig. 5.10(a), the maximum efficiency for a certain number of cells is shifted to lower operating powers in practice, which indicates that the phase shedding strategy presented in Section 5.4 must be adapted in order to maximize the efficiency over the entire operating range. In contrast to the analytically estimated efficiency, the experimentally measured efficiency also exhibits a slightly steeper drop at higher operating powers. The reason for this may be in the practical realization of the converter, which comprises additional components within the circuit, such as a relay, a fuse, power terminals, board-to-board connectors and PCB traces. None of these auxiliary components were considered when estimating the losses, while all of them introduce an additional resistance into the current path. The latter may be the cause for a higher rate of efficiency reduction with increasing the operating power, as they increase the total conduction losses.

It is evident from Fig.7.3(b) that the total power losses approximately equal 90 W at the maximum tested operating power. On the basis of the power loss models presented in Chapter 5 and Appendix A, it is estimated that about 65 % of total power losses are generated on the MOSFETs at this operating point. As a result, the heat sink attached to the MOSFET must be able to handle the power of approximately 60 W. As this thesis did not focus on the thermal model of the converter and optimization of the cooling system, the heat sink was selected arbitrarily. Consequently, the utilized extruded heat sink shown in Fig.7.1 provides a significantly larger cooling capacity than required and thus unnecessarily increases the volume of the converter. The total boxed volume of the experimental prototype shown in Fig. 7.1 approximately equals 4.11 liter, which results in a nominal power density of 0.73 kW/liter. Due to the low cooling requirements resulting from operation with ZVS, the extruded heat sink could be removed, and the heat conductor block connected directly to the housing of the converter. By assuming a housing in the form of a rectangular prism without the presence of an extruded heat sink, the total volume of the experimental prototype could be reduced to 2.98 liter. This would result in a power density of approximately 1.01 kW/liter at the nominal output power of $P_{\mathrm{dc}} = 3000\,\mathrm{W}$. Further improvements in power density could be achieved by optimizing the converter's power circuit components and layout, which remains a challenge for the future.

Fig. 7.4 represents the measured AC voltage v_{ac} and current i_{ac} at the input terminals of the interleaved AC-DC converter, as well as the output DC voltage v_{dc} and the current i_{L1} through the



(a)

(b)

Figure 7.3: (a) Measured power conversion efficiency and (b) total power losses over the entire range of output powers P_{dc}.

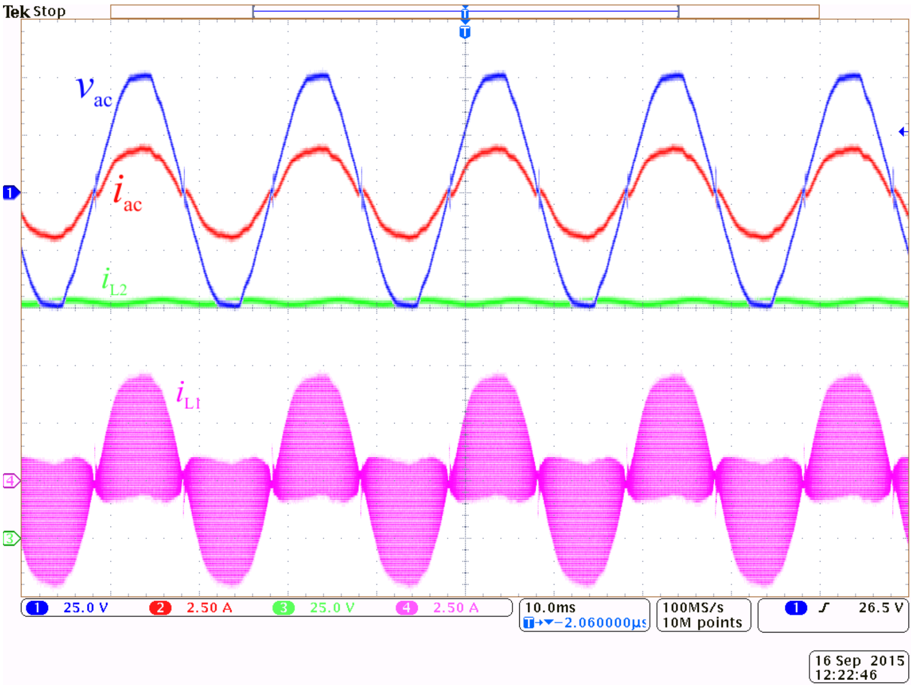

Tek Stop
v_{ac}
i_{ac}
i_{L2}
i_{L1}
1
4
3
1 25.0 V
2 2.50 A
3 25.0 V
4 2.50 A
10.0ms
T→▼−2.060000µs
100MS/s
10M points
1 ƒ 26.5 V
16 Sep 2015
12:22:46

Figure 7.4: Experimental voltage and current waveforms of the investigated interleaved AC-DC converter operating as a rectifier.

inductor L_1. It is evident that the input current i_{ac} is controlled in phase with the AC voltage v_{ac} and maintains a sinusoidal waveform although the waveform of AC voltage is notably distorted. A typical DCM waveform of the inductor current i_{L1} can be observed in the figure.

CHAPTER 8

CONCLUSION AND FUTURE WORK

8.1 General Conclusion

The analysis of hard-switched bridge structure issues, namely the reverse recovery effect and the unwanted turn-on of a transistor, has led to the conclusion that the rate of current change at the turn-on of the mainFET has to be properly limited. Limiting the current rate of change results in a longer duration of switching transitions and consequently increased switching losses. Due to the switching frequency dependent nature of switching losses, a hard-switched bridge-based converter has to operate at a frequency of several tens of kilohertz when a power of few kilowatts has to be processed and a rather high power conversion efficiency is required. Consequently, high power density design of such a converter is not achievable. For increasing the limits of achievable power densities and power conversion efficiencies, switching losses must be eliminated or at least suppressed. This thesis focused on achieving ZVS within the entire operating range of the converter by operating it in the DCM. On the basis of a detailed analysis resonant switching transitions, guidelines are provided for determining the required reversed current and dead time duration for ensuring reliable zero-voltage transitions. The selection of these parameters according to the provided guidelines does not require any experimental tests or simulations during the phase of designing the ZVS control since all the required information can be obtained from the datasheet of components within the power circuit. For practical realization of the desirable switching transitions a control strategy was proposed which is based on operation in DCM and adaptation of the switching frequency. The latter ensures a sufficient magnitude of the reversed current in each switching cycle. In combination with properly selected dead times such control strategy ensures reliable zero-voltage switching transitions of both transistors in the HF-switched leg of the converter. Thus the dominant turn on losses are eliminated and the influence of the switching frequency on power conversion efficiency is significantly reduced. In addition, all the spurious turn-on and body diode reverse recovery related issues and power losses are avoided. The proposed approach does not require any auxiliary circuitry or components and can be entirely implemented within a DSC. Due to operation in the DCM, the power inductor's inductance can be significantly smaller than the one required for the CCM operation at the same operating point. On the other hand, operation with ZVS allows for increasing the switching frequency without a negative effect on the power conversion efficiency. Therefore, a combination of DCM and ZVS offers high potential for reducing the size of the power inductor. Another benefit in terms of power density is a reduction in the size of the heat sink, which is possible due to lower power dissipation on the transistors when operating with ZVS.

A successful practical implementation of the proposed approach requires carefully selected values of the reversed current, power inductor's inductance, and timing parameters, which can be determined by using the experimentally verified analytical models derived in the scope of this thesis. As has been proved, these parameters are of crucial importance for achieving ZVS and ensuring a safe and reliable operation of the converter over its entire operating range. The presented experimental results have confirmed the effectiveness and superior performance of the proposed approach in comparison with HSW operation in CCM. Despite operating at higher switching frequencies, the proposed ZVS approach achieved higher power conversion efficiency over the entire operating area above $1/3$ of the converter's nominal output power. In addition to higher efficiency at moderate and heavy loads, a considerable increase in power density is obtainable. Operating in DCM at higher switching frequencies allows for reducing the size of the power inductor and also, to some degree, the capacitors in the circuit, while a more convenient power loss distribution alleviates the cooling requirements and allows for continuous operation at higher power levels.

8.2 Evaluation of Hypotheses

H1) *Utilization of a soft switching technique results in a reduction of total power losses and alleviates their dependence on the switching frequency.*

The power conversion efficiency comparison of the conventional CCM operation and the proposed DCM operation with ZVS has shown that the latter achieves a higher efficiency, which signifies lower total power losses. In addition, a rather flat power conversion efficiency characteristics over a wide range of operating powers is obtained with converters using the DCM-based ZVS approach. By considering the fact that the operating switching frequency increases when the load decreases and that the resulting change in the power conversion efficiency is insignificant, it can be concluded that the dependence of total power losses on the switching frequency is lower than in the case of operating in CCM with hard commutations, where strongly frequency dependent turn-on losses are dominant.

H2) *DCM-based ZVS prevents unwanted turn-on of transistors and their body diodes' reverse recovery induced issues.*

The unwanted turn-on of a transistor and the reverse recovery of its body diode increase switching losses and may lead to dangerous operating conditions. As has been demonstrated in Chapter 3, their presence is evident from the gate-to-source voltages and the currents through transistors during the switching transitions in a CCM operated converter with hard commutations. The experimental waveforms of ZVS transitions in DCM operation presented in Chapter 4 do not exhibit any oscillations or spikes within the gate-to-source voltages and currents through transistors, which would indicate an unwanted turn-on or reverse recovery process. This observation confirms the prevention of the unwanted turn-on of transistors and their body diodes' reverse recovery effect by utilization of the proposed DCM-based ZVS technique.

H3) *ZVS can be achieved within the entire operating range of a bidirectional converter by operating it in DCM with a reversed current of sufficient magnitude and properly selected timing parameters.*

The experimental results presented in Chapter 4 demonstrate that the proposed DCM-based ZVS approach ensures ZVS under different load conditions and voltage conversion ratios, as long as a sufficient reversed current is achieved within each switching cycle and a proper dead time duration is provided. Thereby, the hypothesis is confirmed. Such reversed current and dead time duration that would ensure ZVS over the entire operating range of a bidirectional converter operating in DCM can be obtained on the basis of the resonant switching transition model derived within this thesis and the proposed DCM-based control design procedures for DC-DC and AC-DC converters.

H4) *The required magnitude of the reversed current and timing parameters for maintaining ZVS over the entire operating range of a bidirectional converter can be determined solely on the basis of the information provided in the datasheet of the components within the circuit.*

According to the resonant switching transition model derived and verified within this thesis, the determination of the required reversed current for achieving ZVS demands for information about the operating input and output voltages, inductance of the power inductor, and the nonlinear parasitic output capacitance characteristic of the utilized MOSFETs. The voltage levels represent one of the fundamental design specifications for each switching power converter and can be thus assumed as given in the phase of selecting the reversed current magnitude. On the other hand, the value of inductance can be either predetermined or selected during the ZVS control design phase. The remaining parameter involved in the ZVS capability criterion (4.18) is the equivalent capacitance C_{eq}. The latter is a function of the MOSFET's voltage-dependent nonlinear parasitic output capacitance, the characteristic of which is given in the datasheet of the utilized MOSFET. On the basis of the listed facts, it is indisputable that the required reversed current is determined solely on the basis of the operating voltage levels, which are a prerequisite for designing any kind of switching power converter, and the information provided in the datasheet of the selected transistors.

The determination of the interval of allowed dead time durations requires information about the duration of the resonant switching transition, duration of the interval before the inductor current changes direction, and turn-on and turn-off delays of the utilized MOSFET. The first two can be estimated by using the resonant switching transition model and the already known parameters for determining the required reversed current. As the turn-on and turn-off delays do not only depend on the utilized transistors but also on the gate driving circuit, additional information is required about the structure of the gate driving circuit and internal resistances of the selected gate driver chip. The latter is provided in the datasheet for the majority of commercial gate driver chips, and thus allows for analytical estimation of the driven MOSFET's turn-on and turn-off delays. Consequently, it can be concluded that both the reversed current and the timing parameters for achieving reliable ZVS within the entire operating range of the converter can be determined solely on the basis of the fundamental converter design specifications and information provided in the datasheet of the components within the circuit, which confirms this hypothesis.

8.3 Future Work

Future work on improving the power density and efficiency of the investigated AC-DC converter may be related to its hardware realization, control system, or other approaches for optimizing its structure, power processing capability, power density or increasing the light load efficiency. In terms of hardware realization special attention should be given to the power inductor design. The existing requirement for load independent value of inductance within the entire operating range of the converter could be omitted, which would result in a possibility for additionally reducing the size of the power inductor. However, such modification would make the control implementation more complex as the inductance considered for calculation of the desired switching frequency would vary with load. Further reduction in the total volume of the converter and a resulting increase in power density could be achieved by optimizing the converter's cooling system and the power circuit layout.

As it is evident from the presented power conversion efficiency analysis for a bidirectional DC-DC converter, the DCM-based ZVS approach suffers from low light load efficiency due to operation at very high switching frequencies within that operating range. For eliminating this drawback, a different switching frequency variation profile should be derived, which would improve the light load efficiency. An effective solution may also be pulse-skipping operating mode.

The DCM-based ZVS approach has demonstrated highly efficient operation over a wide operating range of a DC-DC and an AC-DC converter. Therefore, an interesting challenge for the future is combining both converters into a two-stage structure, which is commonly used in battery charging applications. The expected benefits of such structure are higher output voltage dynamics and a reduced size of the DC-side (intermediate) capacitor in AC-DC stage due to loosened requirements for voltage regulation on the intermediate capacitor. As a result of highly efficient individual stages, a high power conversion efficiency of the obtained two-stage structure is expected.

APPENDIX A

Power losses in a DCM-based ZVS DC-AC converter with variable switching frequency

A.1 Semiconductor losses

The semiconductor losses refer to the power losses generated within the HF and LF switched MOSFETs in the hybrid-modulated interleaved AC-DC converter. Since the LF-switched MOSFET are only switched twice per each AC voltage period, their switching losses are negligible and will therefore not be a subject of estimation. As a result there are only conduction losses generated on the LF-switched MOSFETs. By operating the interleaved AC-DC converter in DCM with a sufficient magnitude of the reversed current, ZVS is achieved. The latter eliminates the turn-on losses in all the HF-switched transistors. In addition, all the reverse recovery and unwanted turn-on induced losses are eliminated since both phenomena are avoided when operating with ZVS. As a result, only turn-off and conduction losses are generated in the HF-switched MOSFETs.

Due to the time and load dependent variation of the switching frequency the estimation of the turn-off losses and conduction losses becomes much more complex than the case of CCM operation. When estimating the switching losses in a fixed-frequency CCM operated converter the number of switching transitions within one grid voltage half-period is easily obtained by dividing the duration of the observed interval with the switching period T_{sw}. This number is independent of the operating point and therefore the estimation of switching losses as well as the description of their dependence on the operating point is much simpler. Determining the total number of switching transitions within one AC voltage half-period is rather complex in the investigated variable switching frequency converter, since the number of switching transitions varies with the load and the switching losses over one switching period vary depending on the instantaneous switching frequency and the load conditions. A similar estimation problem occurs in the case of conduction losses, the estimation of which is based on calculating the rms current flowing through the transistor within each switching period.

The proposed semiconductor loss estimation is based on numerical integration with a variable integration step. The variable integration step is introduced due to time dependent variation of the switching frequency. Fig. A.1 depicts the theoretical voltage, current, and modulation signal waveforms of a DCM operated bidirectional AC-DC converter. The waveforms resemble the digital implementation of the proposed control. At the time instant $t(\mathrm{n})$, the analog-to-digital conversion is started and a sample of the AC voltage v_{ac} and current i_{ac} are taken. These values are used for calculating the duration of the subsequent switching period. A similar approach is taken for estimating the semiconductor losses, where the calculated switching period T_{sw} represents the integration step. The local rms current ripple $\Delta i_{\mathrm{Lpp}}(\mathrm{n})$ is calculated according to (3.8), on the basis of $i_{\mathrm{Lavg}}(\mathrm{n})$ which represents a sample taken from $i_{\mathrm{ac}}(\mathrm{t})$ at the instant $t(\mathrm{n})$. On the other hand, the peak current $i_{\mathrm{Lmax}}(\mathrm{n})$ at which a MOSFET is turned off is determined on the basis of the instantaneous AC current $i_{\mathrm{ac}}(t)$ sampled at $t(\mathrm{n})+T_{\mathrm{dPK}}(\mathrm{n})$, where $T_{\mathrm{dPK}}(\mathrm{n})$ represents the time interval between $t(\mathrm{n})$ and the instant in which the peak inductor current $i_{\mathrm{Lmax}}(\mathrm{n})$. The main objective in the turn-off loss estimation procedure is to accurately determine the current $i_{\mathrm{Lmax}}(\mathrm{n})$ at which the switching transition occurs. In the case presented in Fig. A.1, the sampling instants occur when the counter, which represents a PWM carrier signal, reaches zero. This results in sampling in the middle of current falling period. Another option is to take the sample when the counter equals period, in the middle of the inductor current rising period. In this case the delay $T_{\mathrm{dPK}}(\mathrm{n})$ before the inductor current reaches its peak value $i_{\mathrm{Lmax}}(\mathrm{n})$ must be properly adapted.

The conduction and switching loss estimation algorithm is presented in the form of a flowchart in Fig. A.2. The outputs of the algorithm $P_{\mathrm{OFF,Sx}}$ and $P_{\mathrm{cond,Sx}}$ represent the average switching and conduction losses in each HF-switched bridge leg over one AC voltage period. Although the algorithm is designed for MOSFETs in the HF bridge leg, it can be easily adapted for calculating the conduction losses of a MOSFET in the LF bridge leg. The adaptation requires specification of proper $R_{\mathrm{ds,on}}$ for a LF-switched MOSFET, and a multiplication of the current $i_{\mathrm{Lrms}}(\mathrm{n})$ for a factor representing the number of active interleaved cells. Since the ripple in the current through

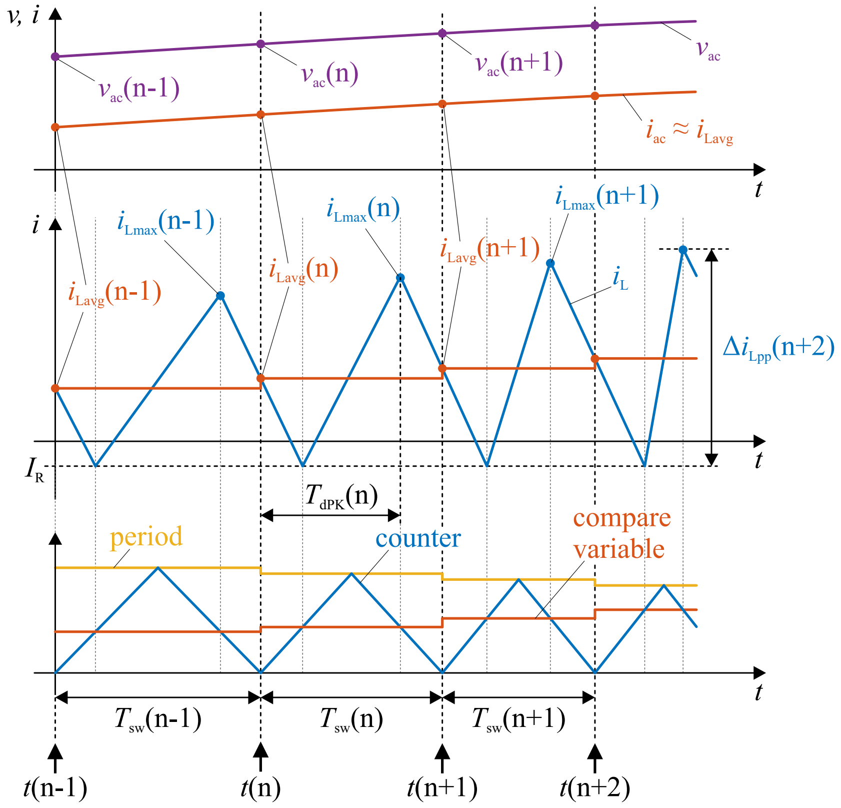

v, i
$v_{ac}(n-1)$
$v_{ac}(n)$
$v_{ac}(n+1)$
v_{ac}
$i_{ac} \approx i_{Lavg}$
t
i
$i_{Lmax}(n-1)$
$i_{Lmax}(n)$
$i_{Lmax}(n+1)$
$i_{Lavg}(n-1)$
$i_{Lavg}(n)$
$i_{Lavg}(n+1)$
i_L
$\Delta i_{Lpp}(n+2)$
I_R
t
$T_{dPK}(n)$
period
counter
compare variable
t
$T_{sw}(n-1)$
$T_{sw}(n)$
$T_{sw}(n+1)$
t(n-1)
t(n)
t(n+1)
t(n+2)

Figure A.1: Theoretical voltage, current, and modulation signal waveforms for a DCM operated bidirectional AC-DC converter with variable switching frequency.

the transistors S_{HN} and S_{LN} of the LF-switched bridge leg is reduced when several HF bridge legs are interleaved, the described adaptation of the conduction loss algorithm will lead to a minor overestimation.

A.2 Magnetic core and winding losses

Power losses in an inductor are generally classified into magnetic core and winding losses. Magnetic core losses consist of hysteresis and eddy current losses, while the total winding losses are proportional to the resistance of the inductor's winding. The latter depends on the effective cross sectional area, the length of the used wire, and the specific resistance of the wire's material. Two unwanted effects are present in high frequency magnetic components, which reduce the effective cross sectional area of the wire and thus increase winding losses. These are proximity effect and skin effect. At high frequencies the current within a conductor is pushed towards the surface of the conductor. Thus, the majority of the current flows between the surface and one skin depth δ. The

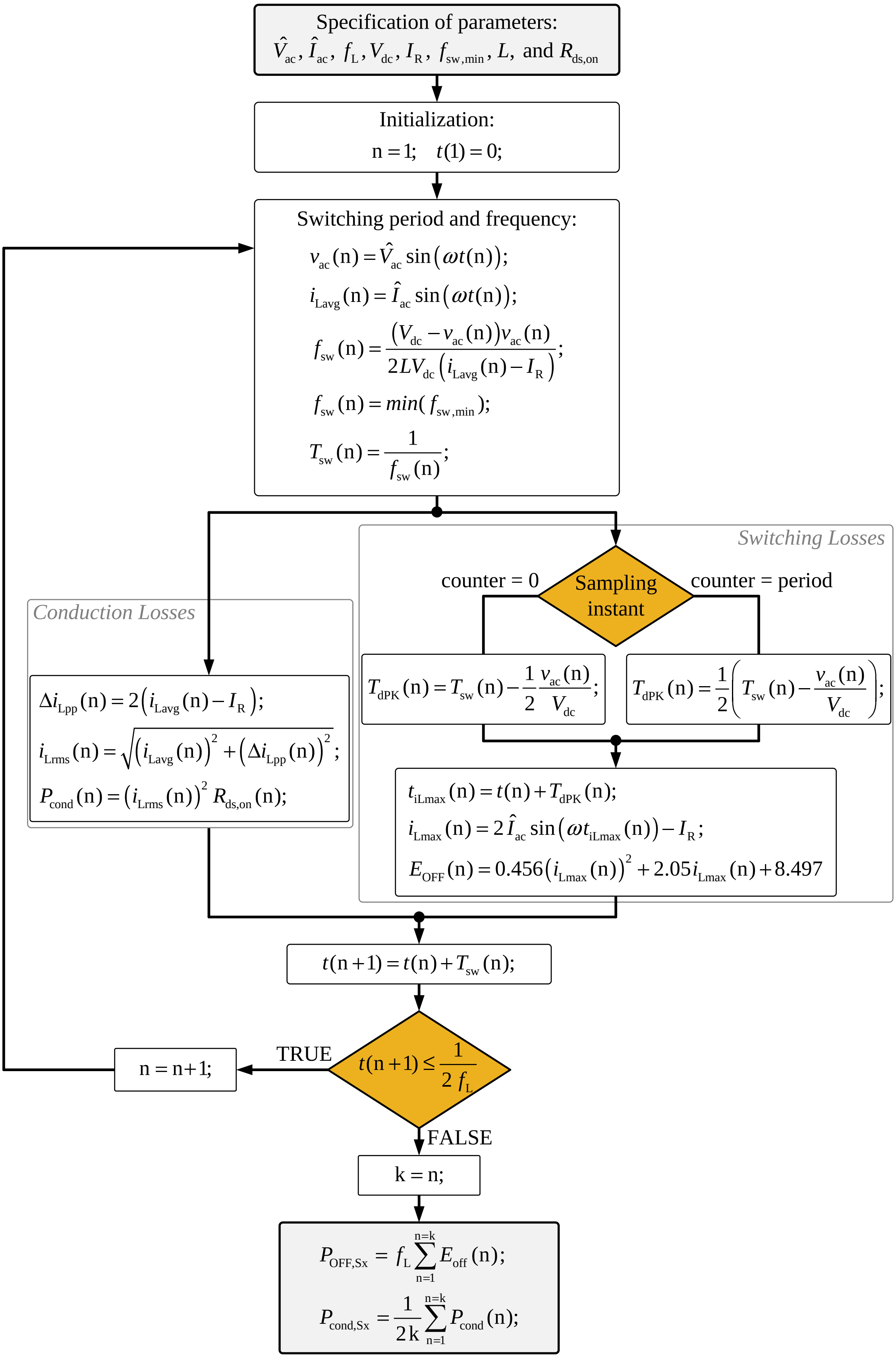

Specification of parameters:
$\hat{V}_{ac}, \hat{I}_{ac}, f_L, V_{dc}, I_R, f_{sw,min}, L,$ and $R_{ds,on}$
Initialization:
$n=1; \quad t(1)=0;$
Switching period and frequency:
$v_{ac}(n)=\hat{V}_{ac}\sin(\omega t(n));$
$i_{Lavg}(n)=\hat{I}_{ac}\sin(\omega t(n));$
$f_{sw}(n)=\frac{(V_{dc}-v_{ac}(n))v_{ac}(n)}{2LV_{dc}(i_{Lavg}(n)-I_R)};$
$f_{sw}(n)=min(f_{sw,min});$
$T_{sw}(n)=\frac{1}{f_{sw}(n)};$
Switching Losses
counter = 0
Sampling instant
counter = period
Conduction Losses
$\Delta i_{Lpp}(n)=2(i_{Lavg}(n)-I_R);$
$i_{Lrms}(n)=\sqrt{(i_{Lavg}(n))^2+(\Delta i_{Lpp}(n))^2};$
$P_{cond}(n)=(i_{Lrms}(n))^2 R_{ds,on}(n);$
$T_{dPK}(n)=T_{sw}(n)-\frac{1}{2}\frac{v_{ac}(n)}{V_{dc}};$
$T_{dPK}(n)=\frac{1}{2}\left(T_{sw}(n)-\frac{v_{ac}(n)}{V_{dc}}\right);$
$t_{iLmax}(n)=t(n)+T_{dPK}(n);$
$i_{Lmax}(n)=2\hat{I}_{ac}\sin(\omega t_{iLmax}(n))-I_R;$
$E_{OFF}(n)=0.456(i_{Lmax}(n))^2+2.05i_{Lmax}(n)+8.497$
$t(n+1)=t(n)+T_{sw}(n);$
TRUE
$t(n+1)\leq\frac{1}{2f_L}$
$n=n+1;$
FALSE
$k=n;$
$P_{OFF,Sx}=f_L\sum_{n=1}^{n=k}E_{off}(n);$
$P_{cond,Sx}=\frac{1}{2k}\sum_{n=1}^{n=k}P_{cond}(n);$

Figure A.2: Semiconductor loss estimation algorithm.

latter can be calculated as [158]

$$\delta = \frac{1}{\sqrt{\pi \mu \sigma f_{\mathrm{sw}}}}, \tag{A.1}$$

where μ is the absolute permeability and σ the specific conductivity of the conductive material. The resulting increased effective resistance of the conductor, which is also known as the AC resistance R_{Lac} of the winding, is obtained as

$$R_{\mathrm{Lac}} = R_{\mathrm{Ldc}} \left(1 + \frac{0.0625\, d_{\mathrm{wo2}}^4}{48\, \delta^4 + 0.05\, d_{\mathrm{wo2}}^4} \right), \tag{A.2}$$

where d_{w} is the diameter of the wire. While the increase in effective resistance of the winding due to skin effect is included in the power loss estimation with (A.2), the proximity effect induced additional reduction of the wire's effective diameter will be neglected. The latter is minimized by using single-layer winding, as was the case for all the inductors studied within this thesis.

The total core loss of the inductor P_{core} can be estimated on the basis of the Steinmetz equation

$$P_{\mathrm{v}} = \mathrm{a}\, (B_{\mathrm{pk}})^{\mathrm{b}} (f_{\mathrm{sw}})^{\mathrm{c}}, \tag{A.3}$$

where P_{v} represents the time averaged power loss per unit of volume, B_{pk} is the peak magnetic flux density, while a, b, c are the empirically determined core loss parameters. The latter are commonly provided in the datasheet of a magnetic core. The producer Magnetics provides parameters a, b, and c for each permeability class of the MPP cores analyzed within this thesis. The latter can be used for calculating the average core losses according to (A.3), under the condition that B_{pk} is determined as half of AC flux swing ΔB:

$$B_{\mathrm{pk}} = \frac{\Delta B}{2} = \frac{B_{\mathrm{max}} - B_{\mathrm{min}}}{2}. \tag{A.4}$$

The AC flux swing ΔB is obtained from the B-H characteristic of the core as a difference between the magnetic flux density at the maximum H_{max} and the minimum H_{min} magnetic field intensity, as evident from Fig. A.3. The magnetic field intensity H is proportional to the inductor current i_{L} and is calculated as

$$H = \frac{N}{l_{\mathrm{c}}} i_{\mathrm{L}}. \tag{A.5}$$

For the proposed DCM operation with a constant magnitude of the reversed current, the minimum magnetic field intensity H_{min} is always constant, while the maximum magnetic field intensity H_{max} depends on the peak inductor current i_{Lmax}, which can be determined in the same way as in the above presented MOSFET turn-off loss estimation.

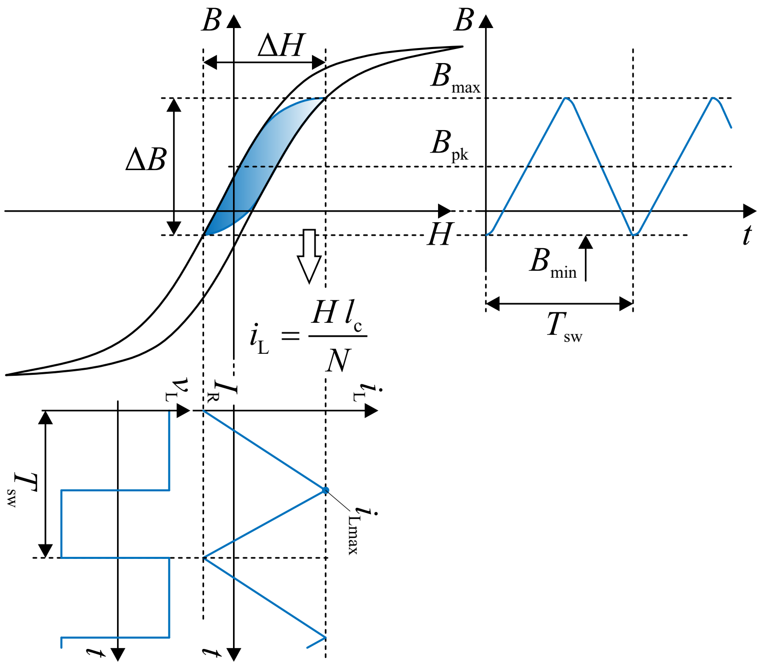


Figure A.3: Magnetic flux density B as a function of the inductor current i_{L}.

On the basis of (A.3)-(A.5) and the magnetic core's datasheet information, the time averaged core losses P_{core} for a specific Magnetics' MPP core can be calculated as

$$P_{\mathrm{core}} = \mathrm{a} \left(\frac{B_{\mathrm{max}} - B_{\mathrm{min}}}{2} \right)^{\mathrm{b}} (f_{\mathrm{sw}})^{\mathrm{c}} A_{\mathrm{c}}\, l_{\mathrm{c}}, \tag{A.6}$$

where A_{c} is the cross-sectional area of the core and l_{c} the mean magnetic path length, which represents the mean diameter of the core.

It must be considered that the magnetic core losses calculated from (A.6) represent only an approximate estimation of the actual core losses. There are several application related factors, like the form of excitation, DCM operation, and duty cycle variation, which influence the actual core losses and are not reflected in the estimated core losses. Nonetheless, the proposed core loss estimation method is suitable for a basic estimation and comparison of magnetic cores made of the same material and used in the same application, as is the case within this thesis.

For estimating the average magnetic core losses $P_{\mathrm{core,Lx}}$ and winding losses $P_{\mathrm{wind,Lx}}$ over one AC voltage period for each inductor within the interleaved AC-DC converter, the algorithm presented in Fig. A.4 was developed. Due to the load and time dependent variation of the switching frequency, numerical integration with a variable integration step has to be used.

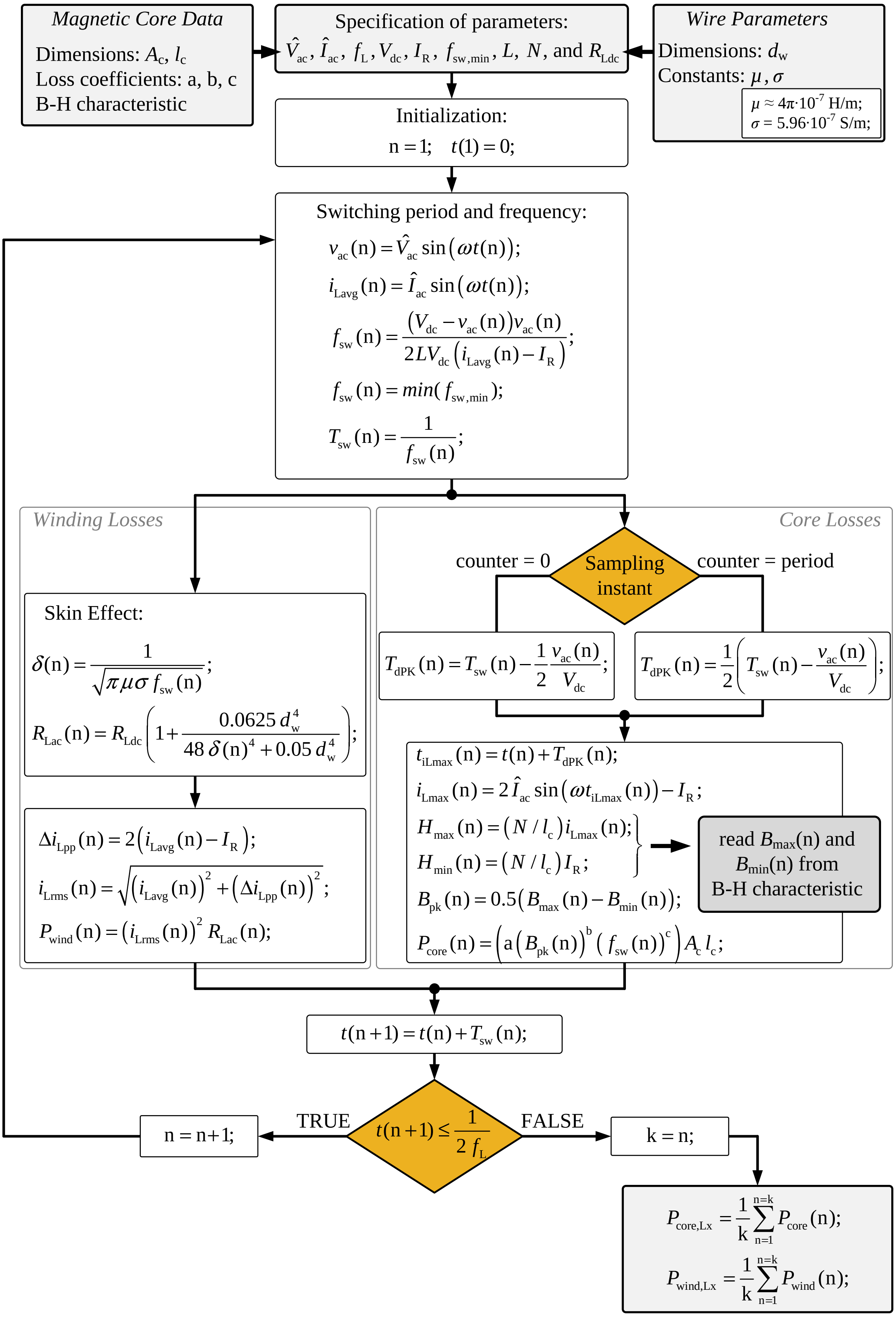

Magnetic Core Data
Dimensions: A_c, l_c
Loss coefficients: a, b, c
B-H characteristic
Specification of parameters:
$\hat{V}_{ac}, \hat{I}_{ac}, f_L, V_{dc}, I_R, f_{sw,min}, L, N$, and R_{Ldc}
Wire Parameters
Dimensions: d_w
Constants: μ, σ
$\mu \approx 4\pi \cdot 10^{-7}$ H/m;
$\sigma = 5.96 \cdot 10^{-7}$ S/m;
Initialization:
$n = 1; \quad t(1) = 0;$
Switching period and frequency:
$v_{ac}(n) = \hat{V}_{ac} \sin(\omega t(n));$
$i_{Lavg}(n) = \hat{I}_{ac} \sin(\omega t(n));$
$f_{sw}(n) = \frac{(V_{dc} - v_{ac}(n)) v_{ac}(n)}{2 L V_{dc} (i_{Lavg}(n) - I_R)};$
$f_{sw}(n) = min(f_{sw,min});$
$T_{sw}(n) = \frac{1}{f_{sw}(n)};$
Winding Losses
Skin Effect:
$\delta(n) = \frac{1}{\sqrt{\pi \mu \sigma f_{sw}(n)}};$
$R_{Lac}(n) = R_{Ldc}\left(1 + \frac{0.0625\, d_w^4}{48\, \delta(n)^4 + 0.05\, d_w^4}\right);$
$\Delta i_{Lpp}(n) = 2(i_{Lavg}(n) - I_R);$
$i_{Lrms}(n) = \sqrt{(i_{Lavg}(n))^2 + (\Delta i_{Lpp}(n))^2};$
$P_{wind}(n) = (i_{Lrms}(n))^2 R_{Lac}(n);$
Core Losses
counter = 0
Sampling instant
counter = period
$T_{dPK}(n) = T_{sw}(n) - \frac{1}{2}\frac{v_{ac}(n)}{V_{dc}};$
$T_{dPK}(n) = \frac{1}{2}\left(T_{sw}(n) - \frac{v_{ac}(n)}{V_{dc}}\right);$
$t_{iLmax}(n) = t(n) + T_{dPK}(n);$
$i_{Lmax}(n) = 2\hat{I}_{ac} \sin(\omega t_{iLmax}(n)) - I_R;$
$H_{max}(n) = (N / l_c) i_{Lmax}(n);$
$H_{min}(n) = (N / l_c) I_R;$
read B_{max}(n) and B_{min}(n) from B-H characteristic
$B_{pk}(n) = 0.5(B_{max}(n) - B_{min}(n));$
$P_{core}(n) = \left(a (B_{pk}(n))^b (f_{sw}(n))^c\right) A_c l_c;$
$t(n+1) = t(n) + T_{sw}(n);$
TRUE
$t(n+1) \leq \frac{1}{2 f_L}$
FALSE
n = n+1;
k = n;
$P_{core,Lx} = \frac{1}{k}\sum_{n=1}^{n=k} P_{core}(n);$
$P_{wind,Lx} = \frac{1}{k}\sum_{n=1}^{n=k} P_{wind}(n);$

Figure A.4: Magnetic core and winding loss estimation algorithm.

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Curriculum Vitae

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List of Publications

Journal Papers:

1. T. Konjedic, L. Korošec, M. Truntič, C. Restrepo, M. Rodič, and M. Milanovič, "DCM-based zero-voltage switching control of a bidirectional DC-DC converter with variable switching frequency," *Power Electronics, IEEE Transactions on*, accepted for publication, doi: 10.1109/TPEL.2015.2449322.
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Conference Papers:

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