05141 Abstracts Collection
Power-aware Computing Systems
— Dagstuhl Seminar —

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Abstract. From 03.04.05 to 08.04.05, the Dagstuhl Seminar 05141 "Power-aware Computing Systems" was held in the International Conference and Research Center (IBFI), Schloss Dagstuhl. During the seminar, several participants presented their current research, and ongoing work and discussed open problems. Abstracts of the presentations given during the seminar as well as abstracts of seminar results and ideas are collected in this paper. The first section describes the seminar topics and goals. Links to extended abstracts or full papers are provided, if available.

Keywords. Energy Dissipation, Power Reduction, Measurement, Management, Performance

05141 Summary – Power-aware Computing Systems

This paper summarizes the objectives and structure of a seminar with the same title, held from April 3rd to April 8th 2005 at Schloss Dagstuhl, Germany.

Keywords: Power-aware architectures

Joint work of: Benini, Luca; Kremer, Uli; Probst, Christian W.; Schelkens, Peter

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2005/321

Reconfigurable ASIPs (Application Specific Instruction Set Processors)

Gerd Ascheid (RWTH Aachen, D)

This is the second part of a joint presentation with Rainer Leupers (see his abstract). It demonstrates - based on a DVB-T example - how energy-efficiency can be obtained with application-specific complex instructions. The ASIP approach allows flexibility even for the high processing speed tasks which today often are implemented using ASIC blocks.

When we consider multi-standard devices, the number of required special instructions may become too high (resulting in too large a chip area). This can be avoided by adding a configurable section to the ASIP. Companies like Stretch already offer processors with reconfigurable sections. However, the interfaces are fixed and the configurable sections are not application specific. The presentation shows how the approach must be generalized so that the issues of multi-standard devices can be addressed. These extensions represent additional challenges for the processor design flow. A principal design flow is proposed and the open questions and challenges are discussed.

Keywords: Application Specific Processors, ASIP, reconfigurable, energy-efficient

Joint work of: Ascheid, Gerd; Chattopadhyay, Anupam; Schliebusch, Oliver; Meyr, Heinrich

Compiler-Driven Power Optimizations In The Register File Of Processor-Based Systems

José Luis Ayala (ETSI Telecomunication - Madrid, E)

The complexity of the register file is currently one of the main factors for determining the cycle time of high performance wide-issue microprocessors due to its access time and size. Both parameters are directly related to the number of read and write ports of the register file and can be managed from a code compilation-level. Therefore, it is a priority goal to reduce this complexity in order to allow the efficient implementation of complex superscalar machines. This work presents a modified register assignment and a banked architecture which efficiently reduces the number of required ports. It also analyzes the effect of the loop unrolling compiler optimization and proposes several power-efficient modifications to this mechanism. Both register assignment and loop unrolling mechanisms are modified to improve the energy savings while avoiding a hard performance impact.

Keywords: Register file, power reduction, compiler optimization, loop unrolling, banked architecture

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2005/305

Separation Of Memory Protection And Energy-Aware Memory Mapping

Frank Bellosa (Universität Karlsruhe, D)

Policies for physical memory management and for memory power mode control should be relocated to the system software of a programmable memory management controller (MMC).

Similar to the mapping of virtual to physical addresses done by an MMU of a processor, this controller offers another level of mapping from physical addresses to real addresses in multi-bank multi-technology (DRAM, MRAM, FLASH) memory system.

Furthermore, the programmable memory controller is responsible for the allocation and migration of memory according to power and performance demands.

Our approach dissociates the aspects of memory protection and sharing from the aspect of energy-aware management of real memory.

In this way, legacy operating systems do not have to be extended to reduce memory power dissipation, and power-aware memory is no longer limited to CPUs with an MMU.

Keywords: Operating System, Memory Management, Power Management

Advanced Power Management Of SoC Platforms

Luca Benini (Università di Bologna, I)

Advanced power management is critical for SoC platforms targeting wireless mobile applications. In this talk we will describe power management strategies exploiting both basic and advanced power control mechanisms, as available in state-of-the-art, low power SoCs. We will consider both low-leakage standby modes and variable-voltage, variable-frequency operations.

Looking forward, we will discuss the opportunities and challenges in power management of SoC platforms with multiple power supply and clock frequency domains.

Complexity aspects in MCTF wavelet based video coding

Tom Clerckx (Vrije Universiteit Brussel, B)

Computer networks and the internet have taken an important role in modern society. Together with their development, the need for digital video transmission over these networks has grown. To cope with the user demands and limitations of the network, compression of the video material has become an important issue. Additionally, many video-applications require flexibility in terms of scalability and complexity (e.g. HD/SD-TV, video-surveillance). Current ITU-T and

ISO/IEC video compression standards (MPEG-x, H.26-x) lack efficient support for these types of scalability. Wavelet-based compression techniques have been proposed to tackle this problem, of which the Motion Compensated Temporal Filtering (MCTF)-based architectures couple state-of-the-art performance with full (quality, resolution, and frame-rate) scalability. However, a significant drawback of these architectures is their high complexity.

The computational and memory complexity of both spatial domain (SD) MCTF and in-band (IB) MCTF video codec instantiations are examined in this study. Comparisons in terms of complexity versus performance are presented for both types of codecs. This presentation indicates how complexity scalability can be achieved in such video-codecs, and analyses some of the trade-offs between complexity and coding performance. Finally, guidelines on how to implement a fully scalable video-codec that incorporates quality, temporal, resolution and complexity scalability are given.

Keywords: Scalable video-coding, complexity scalability, motion compensated temporal filtering, memory complexity, MPEG-21

Joint work of: Clerckx, Tom; Munteanu, Adrian; Andreopoulos, Yiannis; Schelkens, Peter

An Integrated Hardware/Software Approach To Multithreaded Processor Optimization

Sandhya Dwarkadas (University of Rochester, USA)

Growing transistor budgets have resulted in the ability to support the concurrent execution of several threads on a single chip. However, design complexity, power dissipation, and wire scaling limitations create significant barriers to their actual realization. In this talk, I will present on-going work that explores a whole-system view to on-line power-performance optimization — at the architecture, compiler, and operating system level — in the context of observed technology trends and multithreaded workloads and processors. I will begin by presenting results on the performance and energy efficiency of various processor partitioning options. A clustered multithreaded processor (CMT) combines the utilization advantages of simultaneous multithreading (SMT) with the clock speed and power advantages of chip multiprocessors (CMPs). A CMT processor exposes the tradeoff between communication and parallelism, allowing individual applications to dynamically adjust the amount of resources requested and utilized. The flexibility provided by the architecture can be exploited through program analysis and operating system support. I will describe our work in the area of program phase detection and behavior prediction. Behavior prediction can then be used to perform resource-aware scheduling and allocation of resources at the application, operating system, and hardware levels. I will conclude with a discussion of on-going work at each of these levels.

Keywords: Multithreading, power-performance optimization, dynamic tuning, clustering

Power-Aware, High-Performance Computing

Vince Freeh (North Carolina State University, USA)

This talk presents several ideas for power management in high-performance computing (HPC) using a power-aware cluster, consisting of AMD processors with frequency- and voltage-scaling. This talk first discusses the energy-time tradeoff of HPC applications, showing that there is a tradeoff between energy and time. It then introduces a metric, operations per miss, for memory pressure, and shows that this is a good predictor for energy-time tradeoff. The talks shows how OPN and other measurement can be used to improve power efficiency by switching DVS states. The talk explains over-provision for power in a data center and shows its corresponding benefits.

Inter-program Optimizations For Disk Energy Reduction

Jerry Hom (Rutgers Univ. - Piscataway, USA)

Compiler support for power and energy management has been shown to be effective in reducing overall power dissipation and energy consumption of programs, for instance through compiler-directed resource hibernation and dynamic frequency and voltage scaling. The multi-programming model with virtual memory presents a virtualized view of the machine such that compilers typically take single programs as input, without the knowledge of other programs that may run at the same time on the target machine. This work investigates the benefits of optimizing sets of programs with the goal of reducing overall disk energy.

The two key ideas are to synchronize the disk accesses across a group of programs thereby allowing longer disk idle periods, and to utilize execution context knowledge to allocate maximal buffer sizes. The compiler inserts runtime system calls for profiling the application and disk, uses execution context in allocating buffers, and synchronizes disk accesses with an inverse barrier policy. Data prefetching has been added to mitigate the overhead of synchronization.

Experimental results are based on three streaming applications and their subsets. The experiments show that inter-program optimizations can have significant disk energy savings over individually optimized programs. Applying the most aggressive inter-program optimizations result in energy savings of up to 49%, and saving 34% on average.

Keywords: Compiler, inter-program, optimization, execution context, synchronization, inverse barrier

Joint work of: Hom, Jerry; Kremer, Ulrich

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2005/308

Toward An Evaluation Infrastructure For Power And Energy Management

Ulrich Kremer (Rutgers Univ. - Piscataway, USA)

Execution-driven simulators are often used for power/energy and performance evaluation.

Simulators can provide semantic details but they provide insufficient speed or accuracy for compiler and OS research. Physical measurement is fast and objective but lacks a semantic connection between the measurement result and the evaluated program. It is the goal of this research to bring together the advantages of simulation and physical measurement. Power and energy behavior is obtained through physical measurement. Simulation is used for observing the connection between power and energy behavior and the evaluated program.

Our preliminary results demonstrate the ability of this infrastructure to capture detailed power behavior of user selected program regions. To simplify the power/energy evaluation of programs with long execution times and overcome the limitation of physical devices, we propose using the SimPoints methodology developed by researchers at UC San Diego to find representative slices of a program. Through simulation, we validate the feasibility of the SimPoint idea in simplifying power/energy evaluation. We expect that this infrastructure will help researchers in OS/compiler power/energy optimization to evaluate their optimizations more efficiently and observe more optimization opportunities.

Keywords: Simulators, Compilers, Power, Energy, Evaluation

Joint work of: Kremer, Ulrich; Hu, Chunling; Jimenez, Daniel

Layered Approach For Low-Power Network-On-Chip Implementation

Kangmin Lee (KAIST - Daejeon, ROK)

A 1.6GHz on-chip network integrating two processors, memories, and a FPGA provides 11.2GB/s bandwidth in 0.18um 6M CMOS technology. The 2-level hierarchical star-connected network is implemented with various low-power techniques at each layer. For example, low-swing differential signaling at physical layer, crossbar partial activation and Mux-Tree-based crossbar scheduler at network layer, serialized low-energy encoding at transport layer and low-power topology and frequency scaling at system layer. The on-chip network dissipates less than 51W at 1.6V supporting GALS mode. The fabricated chip is successfully measured and demonstrates image processing and 3D-graphics applications.

Keywords: Network-on-Chip, Low-Power Implementation

Computing Systems In Power-Constrained Applications

Se-Joong Lee (KAIST - Daejeon, ROK)

Power-constrained applications such as portable, wearable, and implantable computing applications, are addressed. And, relevant computing systems developed in our lab are introduced. In portable computing application, digital convergence urges a mobile device to have high multimedia-processing-performance as well as advanced communication functionality. As an effort to reduce the power consumption in such a mobile device is introduced. The increased SoC complexity also urges us to adopt more sophisticated communication architecture, which is called on-chip network chips. Some implementation works and low-power features for the OCN are also summarized. Wearable computing seems to be the next station for the portable computing. However, the difference is the fact that wearable computing devices are distributed over human body area rather than merged into a single device. A hearing aid chip is shown as an example of stand-alone wearable computing device, and human body communication is introduced for low-power body area networking. Finally, implantable computing is also addressed as an ultra-low-power computing system.

Keywords: Power-constrained applications, implantable system, portable system, wearable system, embedded DRAM, on-chip network

Fast, Energy-Efficient And Timing Predictable Memory Accesses Enabled By Memory-Architecture-Aware Compilation

Peter Marwedel (Universität Dortmund, D)

The design of future high-performance embedded systems is hampered by at least two problems: First, the required hardware needs more energy than is available from batteries. Second, the speed gap between processors and memories is widening also for embedded systems and cache-based approaches for bridging this gap are not designed for timing predictability.

In this talk we show that we can improve the average memory latency, the worst case memory latency and the energy-efficiency by moving decisions about the location of memory objects from run-time to design time. Scratch pad memories (SPMs) provide the key architectural feature enabling these improvements. Tool support for SPMs is currently rather poor. By exposing the memory architecture to the compiler, this existing architectural feature can be exploited.

We present approaches for utilizing SPMs in several ways. These include both static as well as dynamic techniques for assigning objects to SPMs. The latter correspond to a kind of compiler-controlled paging for the scratch pad. Sharing SPMs across different processes is also considered. We show that both the energy consumption as well as the computed worst case execution time (WCET) can be reduced signficantly.

Keywords: Embedded software, low-power, compiler, low-power, memory, scratch-pad, energy efficiency, timing predictability, WCET, memory wall

Joint work of: Marwedel, Peter; Wehmeyer, Lars; Verma, Manish

Energy Conservation in Memory Hierarchies using Power-Aware Cached-DRAM

Daniel Mossé (University of Pittsburgh, USA)

Main memory has become one of the largest contributors to overall energy consumption and offers many opportunities for power/energy reduction. In this paper, we propose a new memory organization, called *Power-Aware Cached-DRAM* (PA-CDRAM), that integrates a moderately sized cache directly into a memory device. We use this cache to turn a memory bank off immediately after a memory access to reduce energy consumption. While other work has used CDRAM to improve memory performance, we modify CDRAM to reduce energy consumption.

In this paper, we describe our memory organization and describe the challenges for achieving low energy consumption and how to address them. We evaluate the approach using a cycle accurate processor and memory simulator. Our results show that PA-CDRAM achieves an average 28% improvement in the energy-delay product when compared to a time-out power management technique.

Keywords: Memory power management, cached DRAM

Joint work of: AbouGhazaleh, Nevine; Childer, Bruce; Mossé, Daniel; Melhem, Rami

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2005/304

Design Of Power Aware Reconfigurable Systems

Vijaykrishnan Narayanan (Penn State University, USA)

Field Programmable Gate Arrays (FPGAs) are being increasingly used for new designs. With the emergence of FPGAs designed in sub-90nm technology, leakage power consumption has become a major concern. This talk will present various approaches that have been developed by my research group to reduce the leakage power consumption. First, a leakage-saving technique for FPGAs that involves dividing the FPGA fabric into small regions and switching on/off the power supply to each region using a sleep transistor in order to conserve leakage energy will be presented. Specifically, the regions not used by the placed design are supply gated. Next, a new placement strategy to increase the number

of regions that can be supply gated will be discussed. I will also show how the supply gating technique is extended to exploit idleness in different parts of the same design during different time periods.

The next part of the talk will present a programmable dual-VDD architecture in which the supply voltage of the logic blocks and routing blocks are programmed to reduce power consumption by assigning low-VDD to non-critical paths in the design, while assigning high-VDD to the timing critical paths in the design to meet timing constraints.

I will also briefly address the use of dynamic reconfiguration to handle thermal hotspots and the influence of power optimizations on FPGA on soft error rates.

Keywords: Reconfigurable Systems, Field Programmable Gate Arrays, Power, Leakage Energy

Low-Power Interconnection Networks

Li-Shuan Peh (Princeton University, USA)

Systems from microprocessors to supercomputers, from embedded systems-on-a-chip to Internet routers are becoming increasingly interconnected, relying on network fabrics to scale up. With networks taking up a substantial portion of a system's imited power budget, it is now critical to explore low-power interconnection networks.

In this talk, I'll first discuss the challenges faced as we move from high-performance networks, to networks that have to deliver the high performance requirements under tight power budgets. These challenges span fairly disparate areas, from theoretical analysis, to design tools, architectures as well as circuits. I'll briefly survey my group's research into each of these areas, before zooming in on several of the efforts, from theoretical power analysis, to network thermal management and power-aware opto-electronic networked systems.

Keywords: Low Power, Interconnection Networks, Design Tools

Joint work of: Peh, Li-Shiuan

Coherent Or Not Coherent? What Programming Model For Energy-Efficient MPSoCs?

Massimo Poncino (Politecnico di Torino, I)

Shared memory is a common interprocessor communication paradigm for single-chip multi-processor platforms. Snoop-based cache coherence is a very successful technique that provides a clean shared-memory programming abstraction in general-purpose chip multiprocessors, but there is no consensus on its usage in resource-constrained multiprocessor systems on chips (MPSoCs) for embedded applications.

This work aims at providing a comparative energy and performance analysis of cache coherence support schemes in MPSoCs.

Thanks to the use of a complete multiprocessor simulation platform, which relies on accurate technology-homogeneous power models, we were able to explore different cache-coherents hared-memory communication schemes for a number of cache configurations and workloads.

Keywords: Shared Memory, Cache Coherence, Multiprocessors

Stochastic Learning Feedback Hybrid Automata For Dynamic Power Management In Embedded Systems

Sandeep K. Shukla (Virginia Polytechnic Institute, USA)

The trade-off involved in Dynamic Power Management (DPM) techniques is between the reductions of energy consumption and latency suffered by the tasks. Such trade-offs need to be decided at runtime, making DPM an on-line problem.

We formulate DPM as a hybrid automaton control problem and integrate stochastic control. The control strategy is learnt dynamically using Stochastic Learning Hybrid Automata (SLHA) with feedback learning algorithms. Simulation-based experiments show the expediency of the feedback systems in stationary environments. Further experiments reveal that SLHA attains better trade-offs than several former predictive algorithms under certain trace data.

Keywords: Dynamic Power Management, Stochastic Learning Automata, Learning, Hybrid Control for DPM

Joint work of: Erbes, Teodora; Shukla, Sandeep; Kachroo, Pushkin

Challenges In An Era Of Physically-Aware Architecture, Variability, And Expected-Case Design

Kevin Skadron (University of Virginia, USA)

This talk reviews a series of open questions and challenges for the architecture and related communities. The focus is on physical phenomena, variability, and expected-case design.

Architecture is becoming increasingly coupled to physical phenomena.

Already architects have embraced dynamic power, static power, and soft errors as interesting problems. Thermal management has recently been reconginized an another interesting problems. Other physical phenomena are likely to require attention, like the impact of parameter variations. But the clean abstraction that architects are accustomed to is likely to break down, with accurate simulation requiring detailed architectural modeling of low-level physical effects that are typically ignored or abstracted into very simple representations. Examples of phenomena that can no longer be ignored include layout (e.g., wire routing) and parameter variations.

In fact, physical variability is only one source of variability that architects must learn to manage. Simple, single-core, single-threaded simulations already ignore important sources of behavioral variability like context switching, external events, and so forth, casting the accuracy of these simulations into doubt. Trends toward multi-core and multi-threaded architectures and the consequent explosion of workload variability exacerbate the challenges. New modeling techniques based on stochastic modeling and statistical analysis are needed.

Expected-case instead of worst-case design presents further challenges and opportunities for architects. For example, growing power densities have already forced manufacturers to design cooling solutions for less than worst-case behavior, instead targeting typical-case behavior. Atypical behavior that exceeds the cooling solution's capabilities requires some adaptation to maintain correct and safe behavior: for example, thermal stress typically invokes throttling to reduce power density. Solutions like these trade manufacturing costs and design margins for runtime costs like slower performance. Thermal management can be improved by spreading computation in space instead of time, and new multi-core, multi-clustered, and tiled architectures raise rich opportunities.

But expected-case design also presents problems, like increasing variability and severe consequences for atypical behavior. Even severe security vulnerabilities are possible.

The goal of this talk is primarily to describe trends and provoke questions and discussion.

Keywords: Low-level physical phenomena, variability, thermal, temperature

A Quick Thermal Tutorial

Kevin Skadron (University of Virginia, USA)

This short tutorial covers thermal issues from an architecture perspective. It includes basic motivation on why thermal management presents intersting opportunities to architects, basic heat transfer and modeling, a quick overview of some of the main dynamic thermal management techniques, etc.

Keywords: Thermal management architecture

Methodologies For Designing Power-Aware Smart Card Systems

Christian Steger (TU Graz, A)

Smart cards are some of the smallest computing platforms in use today. They have limited resources, but a huge number of functional requirements. The requirement for multi-application cards increases the demand for high performance and security even more, whereas the limits given by size and energy consumption remain constant.

We describe new methodologies for designing and implementing entire systems with regard to power awareness and required performance. To make use of this power-saving potential, also the higher layers of the system - the operating system layer and the application domain layer - are required to be designed together with the rest of the system.

HW/SW co-design methodologies enable the gain of system-level optimization. The first part presents the abstraction of smart cards to optimize system architecture and memory system. Both functional and transactional-level models are presented and discussed. The proposed design flow and preliminary results of the evaluation are depicted.

Another central part of this methodology is a cycle-accurate instruction-set simulator for secure software development.

The underlaying energy model is designed to decouple instruction and data dependent energy dissipation, which leads to an independent characterization process and allows stepwise model refinement to increase estimation accuracy. The model has been evaluated for a high-performance smart card CPU and a use-case for secure software is given.

Keywords: Smart cards, power awareness, HW/SW codesign, cycle-accurate instruction-set simulator

Joint work of: Steger, Christian; Neffe, Ulrich; Rothbart, Klaus, Mühlberger, Andreas; Rieger, Edgar; Weiss, Reinhold

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2005/306

Full Paper: http://www.iti.tugraz.at/de/research/powercard/index.html

Buffer Space And Delay VS. Energy - Predictability VS. Efficiency

Lothar Thiele (ETH Zürich, CH)

We present a new scheme for dynamic voltage and frequency scaling (DVS) for processing multimedia streams on architectures with severely restricted buffers. In conŋ trast to many previously studied DVS algorithms, our scheme does not completely rely on buffers as a means for averaging the burstiness in multimedia workloads. It uses a combination of offline analysis and runtime monitoring to obtain worst case bounds on the workload and then revises these bounds at runtime. Most previous DVS algorithms require application dependent adaptation schemes (such as changing the processor's voltage/frequency at frame boundaries or at the end of certain tasks). As a result such schemes might not be feasible to implement in resource constrained architectures. Our scheme, on the other hand, is fully scalable in that adaptation intervals can solely be determined from architectural constraints.

Smaller intervals lead to higher energy savings, but at the cost of higher overheads. However, qualityŋofŋservice guarantees (e.g. buffers do not over flow, or delay conŋ straints) can be given irrespective of the adaptation intervals chosen.

Keywords: Buffer optimization, stream processing, energy optimization, dynamic voltage scaling

Joint work of: Thiele, Lothar; Maxiaguine, Alexander

Continuous Compiler Driven Dynamic Voltage Scaling

Vasanth Venkatachalam (Univ. California - Irvine, USA)

Though there has been ample work in dynamic power management, most of this work is either hardware or operating system based and thus has a limited ability to optimize the structure of executing programs. Static compiler techniques, however, compile and optimize a program only once, namely before it executes. When the program's behavior changes, the decisions made at compile time become suboptimal. To combine the advantages of these two worlds we are developing a continuous compilation system for power management. The system continuously monitors an executing program to determine its "hotspots", and reoptimizes these hotspots to use reduced clock frequency and voltage settings. This talk describes our ongoing efforts to build this system.

Keywords: Continuous compilation, dynamic power and energy management, runtime measurements

A Multilevel Introspective Dynamic Optimization System For Holistic Power-Aware Computing

Vasanth Venkatachalam (Univ. California - Irvine, USA)

Power consumption is rapidly becoming the dominant limiting factor for further improvements in computer design. Curiously, this applies both at the "high end" of workstations and servers and the "low end" of handheld devices and embedded computers. At the high-end, the challenge lies in dealing with exponentially growing power densities. At the low-end, there is a demand to make mobile devices more powerful and longer lasting, but battery technology is not improving at the same rate that power consumption is rising. Traditional power-management research is fragmented; techniques are being developed at specific levels, without fully exploring their synergy with other levels.

Most software techniques target either operating systems or compilers but do not explore the interaction between the two layers. These techniques also have not fully explored the potential of virtual machines for power management.

In contrast, we are developing a system that integrates information from multiple levels of software and hardware, connecting these levels through a communication channel. At the heart of this system are a virtual machine that compiles and dynamically profiles code, and an optimizer that reoptimizes all code, including that of applications and the virtual machine itself.

We believe this introspective, holistic approach enables more informed power-management decisions.

Keywords: Power-aware Computing, Virtual Machines, Dynamic Optimization

Joint work of: Venkatachalam, Vasanth; Probst, Christian W.; Franz, Michael

Full Paper: http://drops.dagstuhl.de/opus/volltexte/2005/309

Power Optimization In Advanced Channel Coding

Norbert Wehn (TU Kaiserslautern, D)

Channel Coding is an important building block in the outer modem of baseband processing of wireless communication systems. Turbo-Codes and LDPC codes are the most efficient coding techniques known today. They are already in use of many standards (e.g., UMTS, DVB) and in discussion for emerging standards (e.g., WLAN).

The implementation of these coding techniques requires facing many challenges. In this talk we will discuss some of these challenges and will put special emphasis on low power implementations.

Keywords: Wireless communication, channel coding, low power

Extended Abstract: http://drops.dagstuhl.de/opus/volltexte/2005/307