DC-18 GHz MMIC tapered distributed power amplifier

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***Abstract*— A DC-18 GHz MMIC tapered power distributed amplifier has been designed and simulated in GaAs technology. The amplifier has been designed according to the theory for power and efficiency maximization based on tapered drain lines. Small- and large-signal simulations have been carried out to evaluate the amplifier's behaviour. Results suggest that it is possible to achieve a good performance in terms of output power and efficiency for a wide bandwidth.**

I. Introduction

Advances in ultra wideband communications, as well as services integration in multifunctional platforms for defence and military systems, increasingly demand broadband amplifiers. Additionally, many of those applications require high power and high efficiency, and solid-state monolithic solutions address those requirements achieving high-level integration and subsequent benefits such as low production cost. But MMIC broadband amplifiers suffer from parasitic elements and other design restrictions that reduce gain and efficiency at high-frequency bands of interest [1], needing of careful design and optimization techniques.

Power combining techniques have shown to improve output power and power-added efficiency (PAE) at high frequencies and, specifically, distributed power amplifiers (DPAs) have revealed excellent results. Therefore, comprehensive studies have been carried out on uniform DPAs proving that, under certain phase conditions, all active devices involved face same load impedance, giving maximum power to the output load [2].

Although DPAs stand out in flat gain, linear phase response and low return losses over a wide bandwidth, PAE does not typically exceeds 20 %, mainly due to the fact that drain current is split into two branches, one of them loaded with a dummy termination. Consequently, different techniques have been developed to enhance DPA's efficiency. In 1948 [3], tapered lines were introduced in distributed amplifiers as a way to operate them into a lower output drain-line impedance, while achieving to direct the entire drain current to the output load, with open-circuited dummy port.

Recent research on this area have developed optimum input and output artificial transmission lines design methods, making up uniform and non-uniform distributed architectures that fulfill load-line requirement of each transistor size for optimum power operation [4], manufacturing a single-stage MMIC made of six non-uniform cells giving 1-W output power with 7-dB associated gain and 20 % PAE over a multioctave bandwidth. Narendra *et al.* [5] manufactures a non-uniform DPA employing a broadband impedance transformer, with output power of 600 mW, 9 dB gain and PAE greater than 30 % in the frequency range from 10 to 1800 MHz.

This paper presents simulations in AWR design environment for an optimized 3-stage tapered DC-18 GHz MMIC DPA, in GaAs technology, for maximum gain and PAE fulfillment over wide bandwidth. Equal periphery active devices have been chosen, biased in class-A mode. Significant improvements have been achieved by using PHMET devices combined in tapered distributed optimized architecture, exceeding previous research.

II. Theory of operation

Tapered drain lines provide an increase in power and efficiency in distributed amplifiers by means of the removal of the load impedance in the idle port. The equivalent circuit of a generic tapered drain line in a distributed amplifier is depicted in Fig. 1, where:

- $I_{d1}, I_{d2}, I_{d3}...$ are the currents injected by each active device into the drain line.
- $I_1, I_2, I_3...$ and $V_1, V_2, V_3...$ are the currents and voltages at the beginning of each transmission drain line section.
- $Z_{0d1}, Z_{0d2}, Z_{0d3}...$ and $\theta_{d1}, \theta_{d2}, \theta_{d3}...$ are the characteristic impedances and electrical lengths of each transmission drain line section.

This circuit can be analyzed by means of the transmission line theory, which leads to the following relations,

$$I_k = I_{d1}e^{-j(\theta_{d1}+\cdots+\theta_{dk})} + I_{d2}e^{-j(\theta_{d2}+\cdots+\theta_{dk})} + \cdots + I_{dk}e^{-j\theta_{dk}} \tag{1}$$

$$V_k = \frac{I_{d1}}{G_{d1}}e^{-j(\theta_{d1}+\theta_{d2}+\cdots+\theta_{dk})} \tag{2}$$

if the characteristic line admittances take the following values [4]:

$$Y_{0dk} = G_{d1} + G_{d2} + \cdots + G_{dk} \tag{3}$$

being $G_{d1}, G_{d2}...$ the optimum load admittances of the active devices for a given class of operation.

From equation (1) it can be inferred that the total output current of a distributed amplifier based on tapered drain lines