

Noise Optimization of Amorphous $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ Uncooled Microbolometer

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The undersigned, appointed by the dean of the Graduate School,
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NOISE OPTIMIZATION OF AMORPHOUS $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ UNCOOLED
MICROBOLOMETER

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ABSTRACT

A detailed investigation of reduction of low-frequency noise voltage power spectral density (PSD) of silicon germanium oxide ($\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$) uncooled infrared (IR) microbolometers has been performed. The experimental methods used to conduct the research are presented. The noise reduction was achieved by passivating $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ with Si_3N_4 layers and by annealing the devices in vacuum at 200 °C, 250 °C, or 300 °C with different time interval from 1 to 5 hours.

First, uncooled IR microbolometers with a pixel area of $40 \times 40 \mu\text{m}^2$ were fabricated (by another research team member) on four wafers with different $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ compositions while the other layer thicknesses were fixed. The IR sensitive layer was passivated with Si_3N_4 thin films for the purpose of reducing the noise. Second, the temperature coefficient of resistance (TCR) and the corresponding resistivity (ρ) of each devices were measured as a function of temperature between 0 – 70 °C. The measured TCR and resistivity were -3.518/K and $0.763 \times 10^3 \text{ V}^2/\text{Hz}$, -2.590/K and $1.170 \times 10^3 \text{ V}^2/\text{Hz}$, -3.864/K and $3.573 \times 10^3 \text{ V}^2/\text{Hz}$ and -3.103 and $0.730 \times 10^3 \text{ V}^2/\text{Hz}$ for devices from W01, W02, W03 and W04, respectively. The voltage noise PSD was then measured using a bias current between 0.07 - 0.6 μA across many devices from each wafer, with each device given a unique number for the purpose of tracking them. Before annealing, the lowest noise voltage PSD measured at the corner frequency of several devices (W01D21, W02D45, W03D36 and W04D33) from the four fabricated wafers were $7.59 \times 10^{-15} \text{ V}^2/\text{Hz}$, $1.89 \times 10^{-14} \text{ V}^2/\text{Hz}$, $1.82 \times 10^{-14} \text{ V}^2/\text{Hz}$, and $2.79 \times 10^{-14} \text{ V}^2/\text{Hz}$, at 25 Hz, 12 Hz, 190 Hz, and 160 Hz respectively. The corresponding $1/f$ -noise coefficients, K_f , were $3.65 \times 10^{-}$

¹⁴, 3.01×10^{-14} , 1.97×10^{-14} , and 2.74×10^{-13} respectively. To optimize and reduce the measured noise, the same measured devices and others from each wafer were annealed in vacuum (4mTorr) with different time interval from 1 to 5 hours at either 200 °C, or 250 °C, or 300 °C. The measurements demonstrated that the voltage noise PSD was reduced as the annealing time interval was increased to a certain time period, after that the voltage noise PSD started to increase again. For example, the lowest measured noise of each device (W01D21, W03D45 and W04D33) from the four wafers at the corner frequency, after 3h or 4 h time interval, was 1.96×10^{-14} V²/Hz at 12 Hz, 1.5×10^{-14} V²/Hz at 77.5 Hz, 2.11×10^{-14} V²/Hz at 12 Hz, respectively. However, in wafer 02 (02D45), the voltage noise PSD was 1.13×10^{-14} V²/Hz at 23 Hz with 1 h period of annealing. Thus, the results demonstrated that the voltage noise PSD of device W04D33 was significantly lowered after annealing at 300 °C for 4 hours. Annealing devices at higher temperature 300 °C reduced the low frequency voltage noise PSD more than that of 200 °C and 250 °C temperature.

The measured Hooge's parameter of the three devices from W04 after annealing were 2.39×10^{-13} for W04D43 at 200 °C in 2h period, 2.19×10^{-16} for W04D11 at 250 °C in 3 h period and 1.36×10^{-14} for W04D33 at 300 °C in 3 h period. Other devices from W01, W02 and W03 the measured Hooge's parameters decreased after annealing. For example, before annealing the noise parameters (γ , β and K_f) of the device W01D22 were 1.26, 2.24 and 1.44×10^{-12} which are 0.95, 2.00 and 2.02×10^{-13} after annealing, and for the device W03D45 the noise parameters were 1.59, 3.71 and 1.19×10^{-12} but which were seen 1.50, 1.88 and 7.23×10^{-14} after annealing, respectively. However, annealing of devices reduced the noise parameter K_f . This clearly indicates that annealing the device

at higher temperature enabled the reduction of $1/f$ -noise. The possible reasons for the reduction of voltage noise are the dangling bonds, grain boundary and crystal structure were repaired in sensing layer after heating the devices. Trapping-detrapping mechanism stated inside the interfacial oxide was also a potential source of increasing $1/f$ noise.

CHAPTER 1

INTRODUCTION AND BACKGROUND

This chapter will introduce and define the thermal infrared detectors. It will also introduce infrared (IR) uncooled microbolometer. The Uncooled IR microbolometers performance is impacted by the noise that is the random fluctuations in the voltage or current at their terminals. This chapter will also discuss the most important noise sources found in these devices. It also presents a general review and comparison of $1/f$ -noise between several infrared detectors and materials. A general outline of this thesis is presented at the end of the chapter.

1.1 Thermal detector

Thermal detector exhibits a change of some measurable electrical property that accompanies a change in the temperature of the sensitive element due to the absorption of IR radiation. This device has the ability to absorb radiation from X-rays to radio-wave range, and it does not require a cryo-cooling apparatus for operation. It consists of a sensitive pixel connected to a heat sink via the support/electrode arms (See Figure 1.1). The IR radiation falling on the detectors goes into heating the detector's pixel. Hence, heat flows from the pixel to the surrounding via conduction mechanism through the support arms, and convection mechanism through the surrounding air, and radiation mechanisms. Therefore, we have to carefully design the support/electrode arms in order to reduce the thermal conductance path and to meet the thermal time response

requirements. Thermal detectors have three main types: uncooled microbolometers, pyroelectric detectors, and thermopile detectors. In this thesis, I will focus on noise study of uncooled $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ microbolometer.

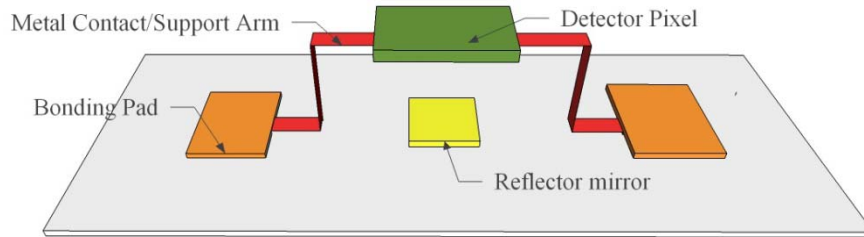


Figure 1.1 Thermal detector connected to its heat sink via an electrode arms.

A microbolometer is defined as a device whose resistance changes with temperature, associated with the absorption of IR radiation. A schematic of the microbolometer operation is shown in Figure 1.2. The microbolometer performance is determined by certain figures of merit such as temperature coefficient of resistance (TCR), responsivity (R_v), and detectivity (D^*). TCR shows how rapidly the resistance changes with respect to change in temperature, the voltage responsivity is defined as the output voltage divided by the input power falling on the detector, and detectivity measures signal to noise ratio and normalizes the detector performance with respect to its size.

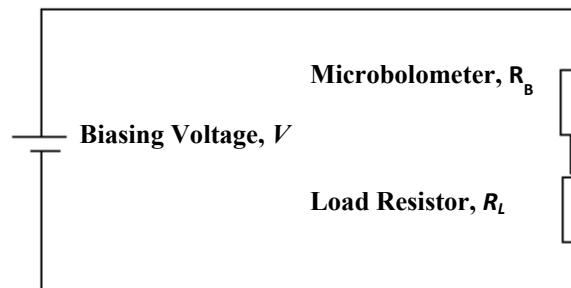


Figure 1.2 A Schematic of the microbolometer operation.

1.2 Low frequency noise of semiconductor

Noise is an inevitable part of any electronic circuits or devices. It is unwanted electrical signal that degrades the quality of the devices or systems by interfering with the original signal. It is defined as the random and uncorrelated fluctuations in current, and voltage of a physical quantity. It is expressed as a power spectral density (S_v).

$$S_v = \frac{V_n^2}{\Delta f} \quad (1.1)$$

Where V_n is the noise voltage (RMS) and Δf is the frequency bandwidth. The noise cannot be completely eliminated from any device or system due to the nature of the materials itself [1, 2]. The noise in electronic devices is treated as a problem for the semiconductor industry. Schottky predicted the occurrence of frequency-independent white noise in 1918 [3]. Several years later, Johnson successfully measured it but discovered unexpected “flicker” noise at low frequency referred to as $1/f$ -noise [4]. This low-frequency $1/f$ -noise decreases the performance of semiconductor devices that operates mainly at low frequencies.

There are several types of noise that exist in uncooled microbolometers; the noise is generated by the sensitive element, which includes, Johnson noise, $1/f$ -noise, and shot noise [5, 6]. In addition, there are other types of noise seen in the microbolometer which includes temperature fluctuation noise, background noise and random telegraph noise. The total noise voltage is given by the sum of squares of the contributions due to Johnson noise, $1/f$ -noise, temperature fluctuation noise, and background noise. Our uncooled microbolometers have primarily been operated in the regime where Johnson noise is the dominant noise mechanism. In this project, we have studied voltage noise PSD and

reduced the $1/f$ -noise at different bias currents, and at different annealing temperatures (200 °C, 250 °C, and 300 °C) and time intervals, and determined some sources of $1/f$ -noise.

1.2.1 Thermal Noise

Thermal noise is often referred to as Johnson noise or white noise. It is generated by the random fluctuation and collision of charge carriers with a lattice under thermal equilibrium conditions since it does not require bias to be observed. The small fluctuations in charge carrier values specified by the most probable distribution are very small, but they are sufficient to produce small noise potentials within a device. Mathematically, neglecting quantum mechanical effects, the power spectral density of the open circuit noise voltage across the terminals of a resistor, R , is given by [5, 6]

$$S_v(f) = \frac{V_j^2}{\Delta f} = 4K_BTR \quad (1.2)$$

where, K_B is the Boltzmann constant, R is the resistance of the device, T is the equilibrium and Δf is the bandwidth. Johnson's noise is independent of the resistor composition, constant across the frequency domain, and is inherent in the detecting element and cannot be avoided.

1.2.2 Flicker noise or $1/f$ -noise

The flicker or excess noise, is also referred to as $1/f$ -noise, is observed at low frequencies such that it becomes dominant over other sources of noise [7], usually due to the fluctuations in both carrier concentration and carrier mobilities arising from carrier trapping and detrapping mechanisms and surface state scattering. The $1/f$ -noise also

depends on the deposition techniques, material, dimensions and electrical contacts. Another aspect of $1/f$ -noise is its volume dependency. Thus, increasing the thickness of the IR sensitive film will reduce the noise level significantly. However, this will result in large thermal mass and hence lower performance of the microbolometer and a larger thermal time constant [8]. Electrical noise increases at lower frequencies due to the increasing contribution of $1/f$ -noise, and at high frequency—it becomes equal to Johnson noise [9]. The noise generation mechanism is still not clear. The $1/f$ -noise and $1/f$ -noise-corner-frequency (f_c) can be determined using Hooge's empirical equation [10]. At corner frequency, $1/f$ -noise equals the Johnson noise:

$$S_v = \frac{\Delta V_{1/f}^2}{\Delta f} = \frac{K_f V_{dc}^\beta}{f^\gamma} \quad (1.3)$$

$$\frac{\Delta V_n^2}{\Delta f} = \frac{\alpha_H I_b^2 R^2}{f_c N} = 4k_B TR \quad (1.4)$$

where S_v is the noise voltage PSD, f' is the electrical frequency with γ close to 1 for $1/f$ -noise [11], K_f is the $1/f$ -noise coefficient. It is given by α_H/N , where α_H gives the magnitude of $1/f$ -noise; N is the number of fluctuators in the sample and is volume dependent. Therefore, K_f is related to the volume normalized inherent noise. It depends on the quality of the crystal, bulk materials of device and on the scattering mechanisms that determine the mobility μ . V_{dc}^β is the DC bias voltage that equals $I_B \times R$ where the value of β is 2. According to the Clarke and Voss hypothesis model, $1/f$ -noise comes from spontaneous fluctuations on a material [12]. This model has a good agreement with the microbolometer $1/f$ -noise since TCR (temperature coefficient of resistance) leads to more $1/f$ -noise:

$$\frac{(\Delta R)}{R} = (TCR)\Delta T \quad (1.5)$$

Where $\frac{\Delta R}{R}$ at 1 Hz is equivalent to the noise figure of merit.

1.2.3 Temperature fluctuation noise

In uncooled microbolometer, temperature fluctuation noise (V_{TF}) arises from the fluctuations in the heat exchange between the isolated sensor and its heat sink. This variance in temperature is caused of temperature fluctuation which is called thermal fluctuation noise. It is given by [12]:

$$V_{TF}^2 = \frac{\Delta V_{TF}^2}{\Delta f} = \frac{(2I_b R \beta T)^2 k_B}{G (1 + 4\pi^2 f^2 \tau^2)} \quad (1.6)$$

1.2.4 Background temperature noise

Background temperature noise (V_{BG}) arises of radiative heat exchange between microbolometer at temperature T_d and surrounding environment at temperature T_b [13] which is given by

$$V_{BG}^2 = \frac{\Delta V_{BG}^2}{\sqrt{\Delta f}} = \frac{(I_b R \beta)^2 [8A \eta \sigma k_B (T_d^5 + T_b^5)]}{G^2 (1 + \omega^2 \tau^2)} \quad (1.7)$$

Where T is the detector temperature and k_B is Boltzmann's constant, and G is the thermal conductance. The summation of total individual noise represents the total bolometer noise and it is written by:

$$V_n^2 = V_J^2 + V_{1/f}^2 + V_{BG}^2 + V_{TF}^2 \quad (1.8)$$

1.3 Overview of the uncooled microbolometer Temperature Coefficient of Resistance and voltage noise

A microbolometer is a thermal sensor that exhibits a change in resistance with respect to a change of temperature of the sensing material accompanying the absorption of IR radiation [14]. It consists of a thin microbridge suspended above a silicon substrate. The bridge is supported by two narrow arms, which serve as a support structure with conductive legs and thermal isolation legs. Encapsulated in the center of the bridge is a thin layer of IR sensitive material. The performance of the microbolometers can be improved substantially, which means they can reach the temperature fluctuation noise performance if noise is eliminated or reduced. The reduction of noise is crucial to the next generation of uncooled thermal cameras since it will allow their detectors to reach the background limited noise performance and further improve the noise equivalent temperature difference (NETD). This will include the noise generated by the IR sensing element (Johnson noise, and $1/f$ or flicker noise), temperature fluctuation noise, and background voltage noise.

Several IR sensitive materials have been used in uncooled IR detection, including vanadium oxide (VO_x) [15-17], amorphous silicon (*a*:Si) [11, 18-21], yttrium barium copper oxide (YBaCuO) [22, 23], silicon germanium (SiGe) [20], silicon germanium oxide (Si-Ge-O) [7, 24-30], metals [31, 32], and *poly*:SiGe[9, 33] (See Table 1.2). These cameras are mainly based on two mainstream materials, namely, Vanadium Oxide (VO_x) and amorphous silicon (*a*:Si) technology, and have comparable performance. They have been used for full production of cutting edge cameras for many years. VO_x has a low $1/f$ -noise of 2.339×10^{-8} V/Hz^{1/2} at 5 Hz with a bias of 19.3 μ A [34]. YBaCuO films achieve

TCR between 3-3.5%/K and $1/f$ -noise of $4 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 7 Hz with $0.41 \text{ } \mu\text{A}$, but this material fails to use conventionally in semiconductor processing [22, 23]. Though SiGe exhibits upper limit to TCR which is 2.5 - 3%/K, the resistivity of SiGe can be kept low by controlling the doping level. Processing of *poly*:SiGe materials to achieve the desired crystallinity requires temperatures as high as 650°C [11]. The noise of *poly*:SiGe is $1 \times 10^{-11} \text{ V}^2/\text{Hz}$ at 1 Hz frequency and *poly*:Si is $36 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 10 Hz [35].

Several research groups have studied Si-Ge-O compound as an IR sensitive material (See Table 1.2). For example, Ahmed *et al.* reported the TCR value of $-4.88\%/K$ with high resistivity of $38 \text{ k}\Omega\text{-cm}$ for $\text{Si}_x\text{Ge}_{1-x}\text{O}_y$ with 2.5 atomic % of Si and 18.8 atomic % O_2 [28]. In addition, the measured voltage noise PSD was $7 \times 10^{-13} \text{ V}^2/\text{Hz}$ at 250 Hz with $4 \text{ } \mu\text{A}$, and the calculated noise coefficient K_f value was 2.9×10^{-11} . The voltage noise value and the corner frequency were high. Clement *et al.* deposited GeSi with atomic composition 85% and 15% respectively in argon or oxygen environment [29]. They were able to measure under optimum conditions a resistivity and a corresponding TCR of $10 \text{ k}\Omega\text{-cm}$ and $-5\%/K$, respectively. A similar deposition method was performed by Rana *et al.* [7]. In earlier work, they fixed a piece of silicon (cut from silicon wafer) to a Ge target and deposited using one power source. In later work they deposited $\text{Si}_{0.15}\text{Ge}_{0.85}$ from one target in an argon/oxygen environment [30]. Their findings agreed with Ahmed *et al.* However, this study used a specific film concentration $\text{Si}_{0.15}\text{Ge}_{0.85}\text{O}_y$ while the O_2 was varied between 0-9%. The $1/f$ -noise was optimized by annealing the devices at 250°C in forming gases using the rapid thermal annealing system. The measured $1/f$ -noise at 70 Hz was $1 \times 10^{-15} \text{ V}^2/\text{Hz}$ using $0.3 \text{ } \mu\text{A}$. The calculated $1/f$ -noise coefficient K_f was 2.21×10^{-10} [36]. In this work, it is reporting the reduction of the voltage noise power spectral density

(PSD) of uncooled $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ microbolometers by passivating the devices with Si_3N_4 layers and annealing them at 200 °C, 250 °C, or 300 °C in vacuum at different time intervals. Four sets of devices with different Si-Ge-O element compositions were studied in detail. The atomic composition of Si, Ge, and O_2 on the deposited thin films were determined using energy dispersive X-ray spectroscopy (EDX).

Table 1.1 Temperature coefficient of resistance (TCR) of common uncooled infrared materials.

IR materials	TCR (%/K)	References
<i>a</i> :Si	-(2 - 3.9)	[37-44]
VO _x	-(2 - 2.4)	[45, 46]
YBaCuO	-(2.88 - 3.5)	[22, 23]
Si-Ge	-(2 - 3)	[9, 47]
Metal	-0.2	[48]

Table 1.2 The most recent results of noise voltage PSD.

Reported Noise Performance	References
$1 \times 10^{-15} \text{ V}^2/\text{Hz}$ at 70 Hz with 0.3 μA	[49]
6.4×10^{-15} - $14.4 \times 10^{-15} \text{ V}^2/\text{Hz}$ at 10 Hz with 0.1 μA	[50]
$7 \times 10^{-13} \text{ V}^2/\text{Hz}$ at 250 Hz with 4 μA	[36]
$7.59 \times 10^{-15} \text{ V}^2/\text{Hz}$ at 25 Hz with 0.7 μA	Reported this thesis

1.4 Outline of this thesis

Chapter 2 is an overview of the IR microbolometer working principle. Also, the design and the fabrication processes are discussed in this chapter along with a description of this research's experimental setup. The final chapter 3 is a summary of the research presented herein.

CHAPTER 2

DEVICE FABRICATION AND EXPERIMENT

This chapter will focus on the design of uncooled $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ microbolometers and the experimental set up for resistance versus temperature, and $1/f$ -noise characterization.

2.1 Microbolometer design and fabrication

The microbolometer is designed with pixel sizes of $25 \times 25 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$, enabling the fabrication of mega pixel format arrays. It consists of a thin Si_3N_4 bridge suspended above a silicon substrate as shown in Figure 2.1. The bridge is supported by two narrow arms of Si_3N_4 and NiCr films. The arms serve as support structure with

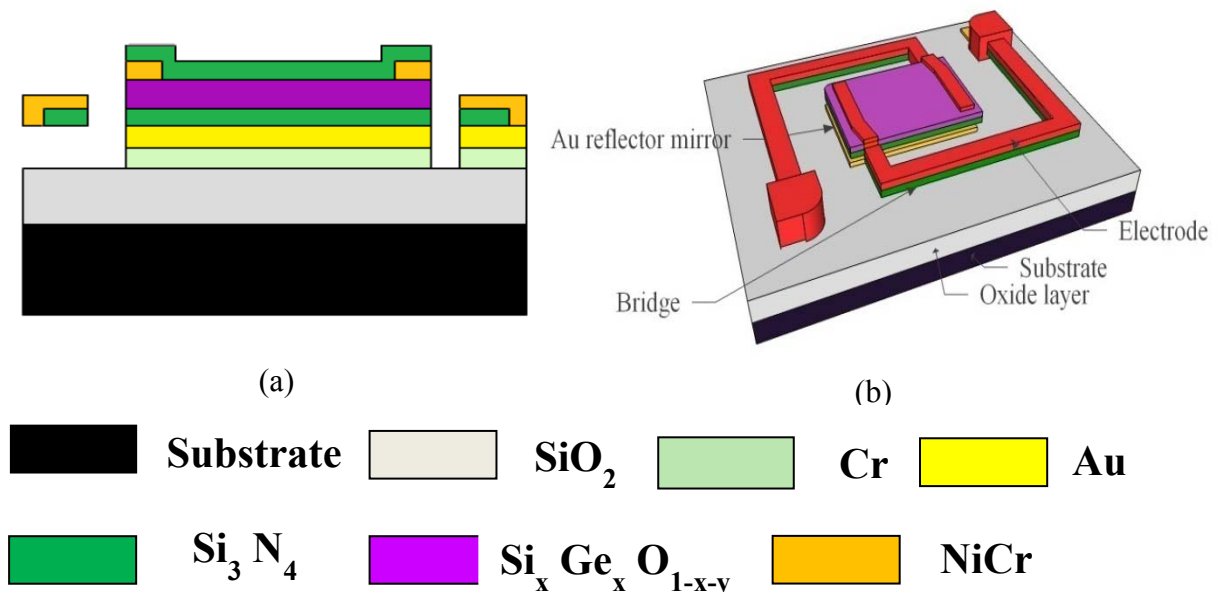


Figure 2.1 Microbolometer fabrication steps: (a) cross sectional view, (b) top view of the tested device.

conductive legs and thermal isolation legs. Encapsulated in the center of the Si_3N_4 bridge is a thin layer of Si-Ge-O IR sensitive material and thin titanium (*Ti*) absorber.

The Si_3N_4 was chosen for its excellent thermal properties, processing characteristics and high infrared absorption. The IR sensing layer of the Si-Ge-O is on top of a polyimide sacrificial layer. Subsequent etching of the sacrificial layer provides the air gap that thermally isolates the microbolometer. A thin film of gold (Au) layer under the polyimide sacrificial layer acts as a mirror for the resonant cavity between the mirror and Si-Ge-O thin film layer. This optical resonant cavity plays an important role in the absorption of infrared radiation for the suspended microbolometer since it is wavelength dependent. With the appropriate design, the resonant cavity maximizes the IR absorption and hence maximizes the responsivity with an absorption peak in the long wavelength band. The resonant cavity can be created between the incoming and reflected waves if the cavity depth is tuned accordingly: $d_n = [(2n - 1) - (\varphi_1 - \varphi_2)]\lambda/4$, where d_n is the depth of the air gap, n is an integer, λ is the wavelength and φ_1 , and φ_2 are the phase differences between the incoming and reflected light [16]. This work is mainly focused on measuring the noise behavior of Si-Ge-O thin film. Therefore, we have not used the sacrificial polyimide layer and top Ti absorber layer in the device in order to speed up fabrication process. The microbolometers' fabrication was implemented on top of silicon substrates using surface micromachining technology. All microbolometer layers were deposited by an RF magnetron sputtering system in an Argon environment at room temperature, and at a low pressure of 4 mTorr with a base pressure below 5×10^{-6} Torr, and were patterned using lift-off process. Two different shapes of supporting arm structure were implemented as shown in Figure 2.1 (a). The devices were fabricated by

another group member and it will be part of his thesis. Optical images of the fabricated devices are shown in Figure 2.2.

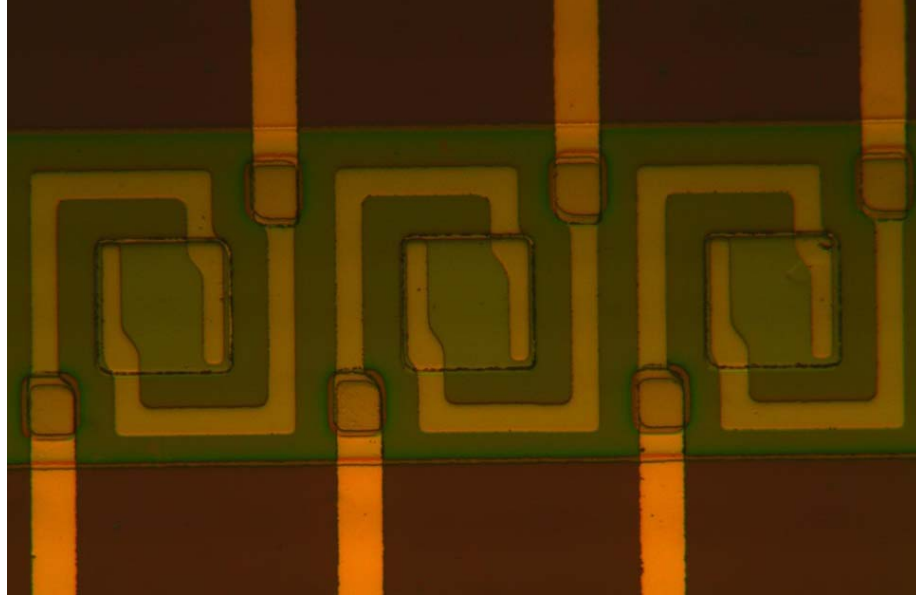


Figure 2.2 Optical images of the fabricated microbolometer with a pixel area of $40 \times 40 \mu\text{m}^2$ without an air gap.

2.2 Experimental set up and details

The noise voltage power spectral density (PSD) of amorphous $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ based microbolometers were optimized and reduced by annealing the devices in vacuum at 200 °C, 250 °C or 300 °C with a ramp rate of 10 °C/min with an annealing duration between 1 to 5 hours . The noise measurements were performed on devices without air gaps with various Si-Ge-O compositions. Many devices from four wafers with different compositions of Si-Ge-O were measured before and after annealing at different bias currents. The noise measurements were performed in air inside a cryostat (DE 202 cold head), which was placed inside a shielding room in order to isolate the microbolometer from any external sources of noise. The output voltage was fed to a dynamic signal analyzer (HP 35670A) through a low noise preamplifier (Signal Recovery Model #5113).

Each device was voltage biased using Ni-Cd battery and 1 M Ω metal resistor connected in series with the device as shown in Figure 2.4 (a). The applied currents ranged between 0.07-0.6 μ A.

To determine the atomic composition and electrical characterization of the IR sensing layer of the device, the Si_xGe_yO_{1-x-y} thin films was deposited on an n-type Si wafer and on a glass substrate simultaneously in step (4) of device fabrication as mentioned in the previous section. The film compositions of the IR sensing layer (Si_xGe_yO_{1-x-y}) were measured using energy-dispersive X-ray spectroscopy (EDX) in a FEI Quanta 600 FEG ESEM system. The Si_xGe_yO_{1-x-y} films deposited on bare silicon wafer were used for this purpose.

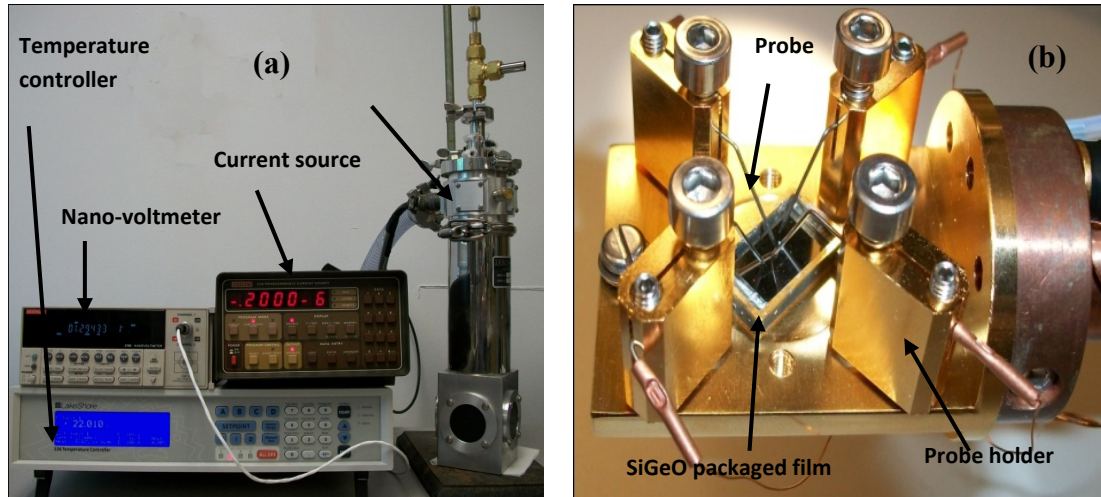


Figure 2.3 Experimental set up for TCR and resistivity measurements: a) the whole setup (computer is not shown), b) a Si-Ge-O packaged sample mounted on the base stage of a special 4-probe sample holder inside the cryostat.

For electrical characterization, the Si_xGe_yO_{1-x-y} films deposited on a glass slide was diced into small dies with an area of approximately 1 \times 0.5 cm² and then mounted in a ceramic flat pack package by a heat conductive epoxy. The package was heated at 150° for 5 min

to cure the epoxy. The sample was then mounted firmly on the base stage of a special 4-probe sample holder inside a closed-cycle cryostat (Janis VPF-100 cryostat). The resistance versus temperature (R-T) characteristics, electrical resistivity and the corresponding temperature coefficient of resistance (TCR) measurements were performed using a 4-point probe technique (see Figure 2.3). A programmable current source (Keithley Model 220) was used to apply a fixed current, and a high precision voltmeter (Keithley Model 2182 Nanovoltmeter) was used to measure the voltage across the two inner probes. The temperature was varied from 0 °C to 70 °C with 1 °C intervals, and controlled by a temperature controller (Lakeshore 336 Temperature Controller). At each temperature set-point, 150 data points were collected and averaged to measure the resistance versus temperature (R-T) behavior. The TCR shows how rapidly the resistance of a material responds to a change in temperature. It is given by:

$$TCR = \frac{1}{R} \frac{dR}{dT} = -\frac{E_a}{kT^2} \quad (2.1)$$

$$R(T) = R_0 \exp\left(\frac{E_a}{kT}\right) \quad (2.2)$$

Where E_a is the activation energy, k is the Boltzmann constant $R(T)$ is the resistance at temperature T , R_0 is the initial resistance. The E_a was calculated from the slope of Arrhenius plot. Hooge's empirical Eq. 1.3 for the $1/f$ -noise is used in order to determine the noise parameters:

$$S_v = \frac{K_f V_{dc}^\beta}{f^\gamma} \quad (2.3)$$

The value of β , γ , and K_f were determined by taking the logarithm of Eq. (2.3):

$$\text{Log}_{10} S_V = \beta \log_{10} V_{DC} - \gamma \text{Log}_{10} f + \text{Log}_{10} K_f \quad (2.4)$$

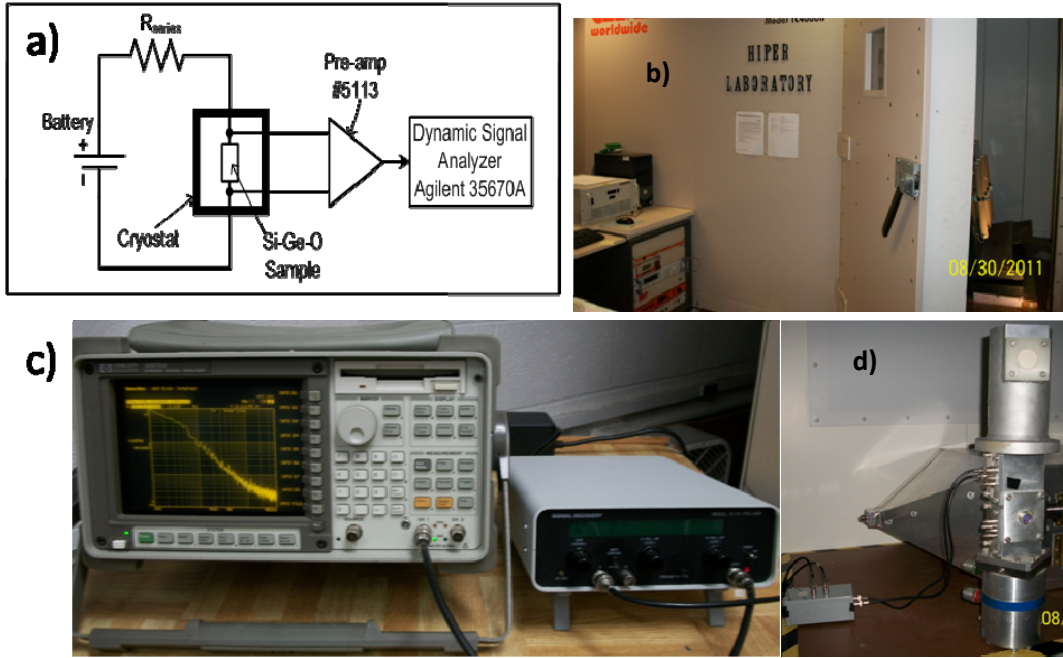


Figure 2.4 Noise measurement setup, from left to right a) schematic, b) Shielding room d) Measuring instruments (DSA and Pre-amplifier), d) APD Cryostat inside the shielding room.

This is a straight line equation of $\log_{10}(S_V)$ versus $\log_{10}(V_{DC})$ where β is the slope, and the last two terms of Eq.3.4 are constant for a specific frequency. Thus, the value of β can be determined from the average slope of $\log_{10}(S_V)$ versus $\log_{10}(I_b)$ plot using 1, 5 and 10 Hz at different levels of applied bias current. Similarly, the value γ can be determined from the average slope of $\log_{10}(S_V)$ versus $\log_{10}(f)$ plot at the same constant currents in the frequency range 1-10 Hz. The average value of K_f can be determined by substituting the calculated value of γ and β for each bias current into Eq. 2.3 at 1 Hz, 5 Hz and 10 Hz.

CHAPTER 3

RESULTS AND DISCUSSIONS

Chapter 3 discusses the noise study of uncooled $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ bolometer with four different compositions. The aim is to optimize the $1/f$ -noise by annealing the devices in vacuum at 200° C, 250° C or 300° C.

3.1 Resistivity and TCR as a function of temperature

This thesis features these four $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ compositions, which were selected from over 250 deposited and characterized films [24]. The film compositions and electrical properties of the fabricated four wafers are listed in Table 3.1. The TCR and the corresponding resistivity of devices from the four wafers were plotted as a function of temperature as shown in Figure 3.1.1. These figures includes four films with a relatively high TCR along with low resistivity values measured at room temperature of -3.518 %/K, and $763 \Omega\text{-cm}$, -2.590 and $1.170 \text{ k}\Omega\text{-cm}$, -3.864% /K and $3.573 \text{ k}\Omega\text{-cm}$, and -3.103 %/K, and $730 \Omega\text{-cm}$ using $\text{Si}_{0.053}\text{Ge}_{0.875}\text{O}_{0.072}$, $\text{Si}_{0.041}\text{Ge}_{0.902}\text{O}_{0.057}$, $\text{Si}_{0.081}\text{Ge}_{0.853}\text{O}_{0.066}$ and $\text{Si}_{0.034}\text{Ge}_{0.899}\text{O}_{0.067}$, respectively. The TCR denoted by “Measured,” was plotted from the measured data directly. The TCR denoted by “Calculated,” was determined and plotted using Eq.3.1, where the E_a was deduced from the slope of Arrhenius plot. It is noted that the R-T behavior of the $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ films in the device were exponential and followed the relation in Eq.3.2. At room temperature, wafer 02 showed the lowest value of TCR while the other three wafers have TCR values at room temperature of -3.103% /K, -3.518% /K, and -3.864% /K. The figure shows that TCR values around room temperature of

wafer 03 (Figure 3.2c) were not stable with large fluctuations which may have resulted in a higher $1/f$ -noise value. In addition, the devices did not work with a large number of biasing current since the resistivity is very high. The current-voltage (I-V) characteristics were measured before and after annealing the fabricated devices. It was found to be linear. Thus, the devices do not suffer Joule-heating effect. The linear region of wafer 03, and wafer 01 is -300 nA to 300 nA, -760 nA to 760 nA, respectively.

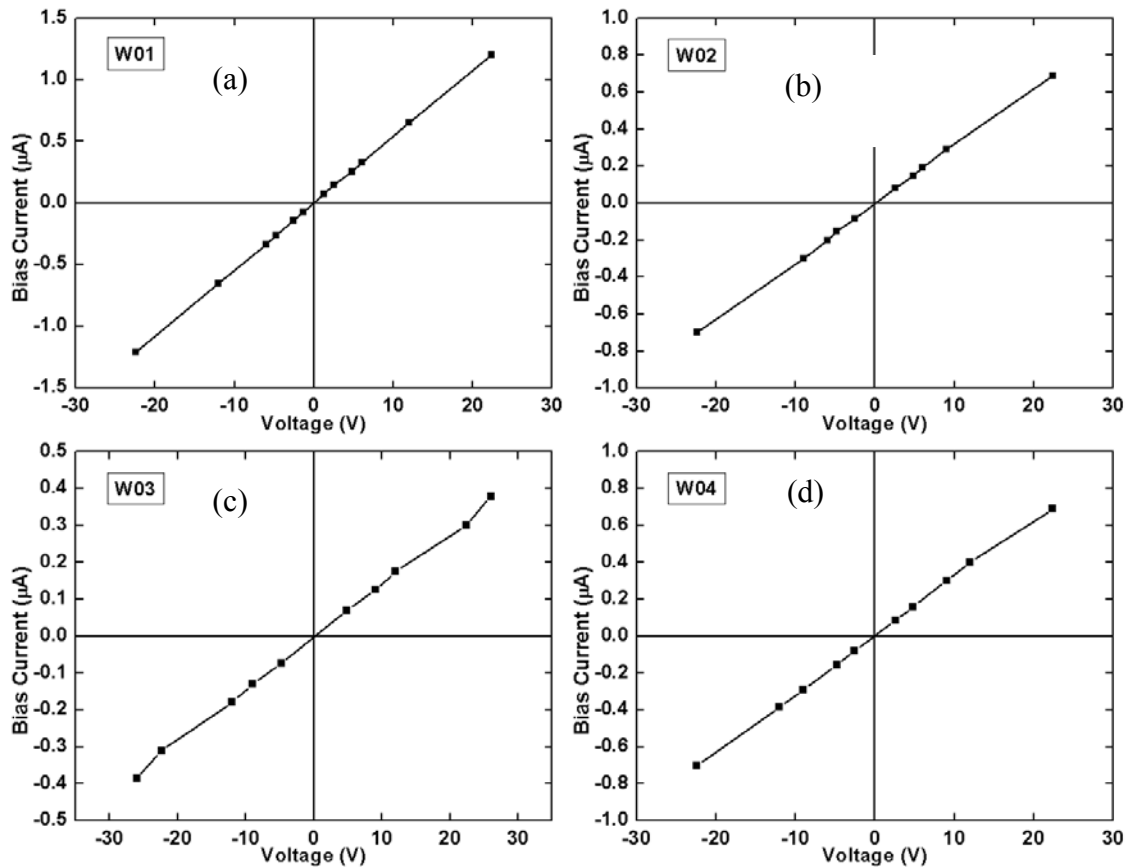


Figure 3.1 I-V graph from (a) wafer W01, (b) wafer W02, (c) W03 and (d) W04.

Table 3.1 Film composition and electrical properties of the devices.

Wafer	Film Composition	Resistivity ($\times 10^3 \Omega\text{-cm}$)	TCR (%/K)	Activation Energy E_a (eV)
W01	$\text{Si}_{0.053}\text{Ge}_{0.875}\text{O}_{0.072}$	0.763	-3.518	0.2656
W02	$\text{Si}_{0.041}\text{Ge}_{0.902}\text{O}_{0.057}$	1.170	-2.590	0.1956
W03	$\text{Si}_{0.081}\text{Ge}_{0.853}\text{O}_{0.066}$	3.573	-3.864	0.2917
W04	$\text{Si}_{0.034}\text{Ge}_{0.899}\text{O}_{0.067}$	0.730	-3.103	0.2402

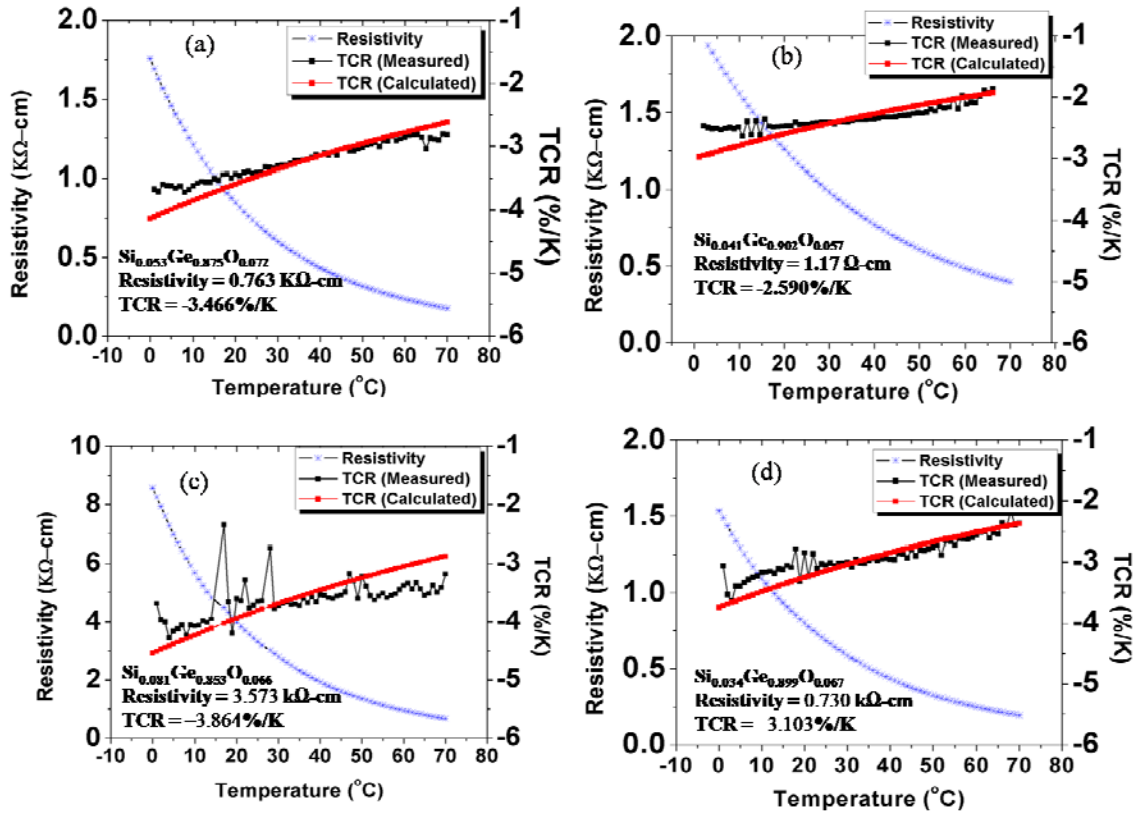


Figure 3.2 Resistivity and TCR versus temperature for devices from (a) wafer W01, (b) wafer W02, (c) W03 and (d) W04.

3.2 Noise study of metal resistor

Each device was voltage biased using Ni-Cd battery and 1 M Ω load resistor connected in series with the device. The applied currents ranged between 0.08-0.6 μ A. We have selected metal resistor because they have much lower $1/f$ -noise than that of carbon resistors [4], [51]. The measured $1/f$ -noise of 11.5 k Ω , 51 k Ω , and 1 M Ω metal resistors are shown in Figure 3.2.1. The $1/f$ -noise corner frequencies were 6 Hz, 3 Hz and 2.5 Hz, respectively. The figure also shows how increasing the resistance increases PSD voltage noise without applying any biasing current or voltage, since Johnson noise is linearly dependent on resistance and excess fluctuation of electrons at room temperature.

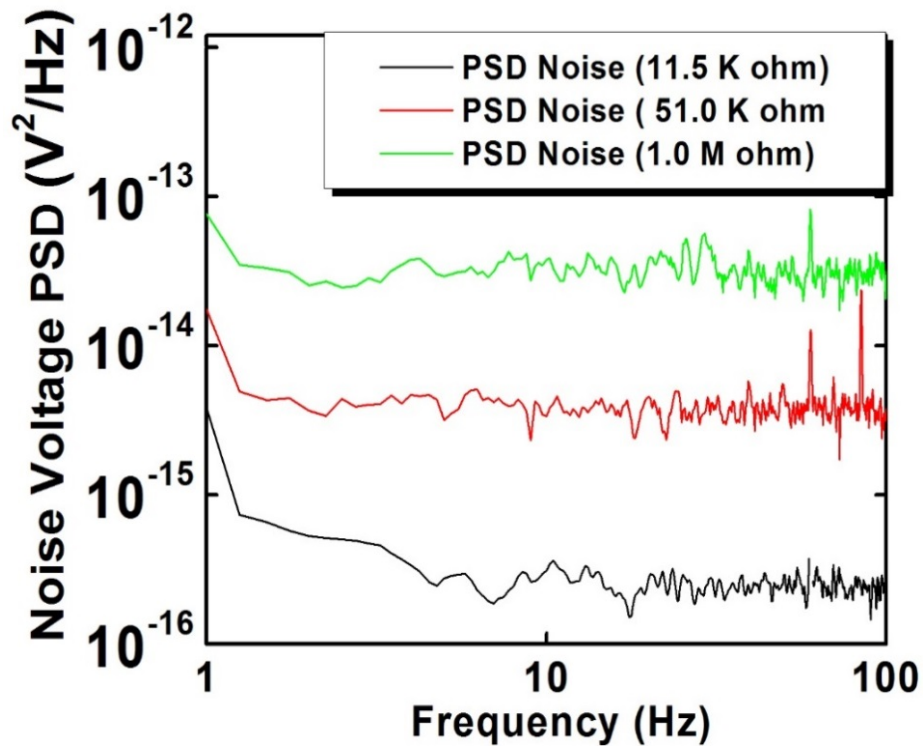


Figure 3.2.1 PSD noise comparison with different metal resistances: 11.5 K Ω , 51K Ω and 1 M Ω without biasing current.

3.3 Noise Study of Microbolometer

3.3.1 Noise study of microbolometer before annealing

We have measured the voltage noise PSD of the fabricated wafers as a function of frequency at bias current between 0.07 – 0.6 μA before and after annealing. Figure 3.3.1.1 and Figure 3.3.1.2 show the noise spectrum of devices from wafer W01 (namely W01D21), W02 (namely W02D45), W03 (namely W03D46) and wafer W04 (namely W04D33) before annealing. The figure clearly demonstrates that the noise increases as the biasing current increases in all devices. The lowest measured noise voltage PSD with an acceptable Hooge's parameters for these devices were $7.59 \times 10^{-15} \text{ V}^2/\text{Hz}$, $1.89 \times 10^{-14} \text{ V}^2/\text{Hz}$, $3.24 \times 10^{-14} \text{ V}^2/\text{Hz}$, and $2.79 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 25 Hz, 12 Hz, 70 Hz, and 160 Hz corner frequency, respectively, using 70 nA or 80 nA bias current. The corresponding Hooge's parameters γ , β , and K_f were as follow: (W01) 1.19, 1.71, 3.65×10^{-14} , (W02) 1.83, 2.17, 2.35×10^{-12} , (W03) 1.85, 2.0, 3.19×10^{-16} , and (W04) 1.58, 2.19, 2.74×10^{-13} , respectively. The ($1/f$ -noise) corner frequency is smaller in wafer 02 than that of the other three wafers. Before annealing, the Hooge's parameters and $1/f$ -noise at the corner frequency for the four wafers are shown in Table 3.2. We see in the table that the average value of γ was close to 1, ranged between 0.91 - 1.26 for wafer W01 and W02 indicating the dominant $1/f$ -noise at low frequencies. On other hand, for the wafer W03 and W04 we found that γ is closer to 2, indicating the presence of brown noise before annealing. This noise may have come from different part of the device, and from several sources of noise, i.e. surface defects, dangling bond, etc [1, 61]. The value of K_f for different devices from the four wafers before annealing was ranged from 1.6×10^{-16} for wafer 03 to 3.65×10^{-14} for W01. The lower values of this

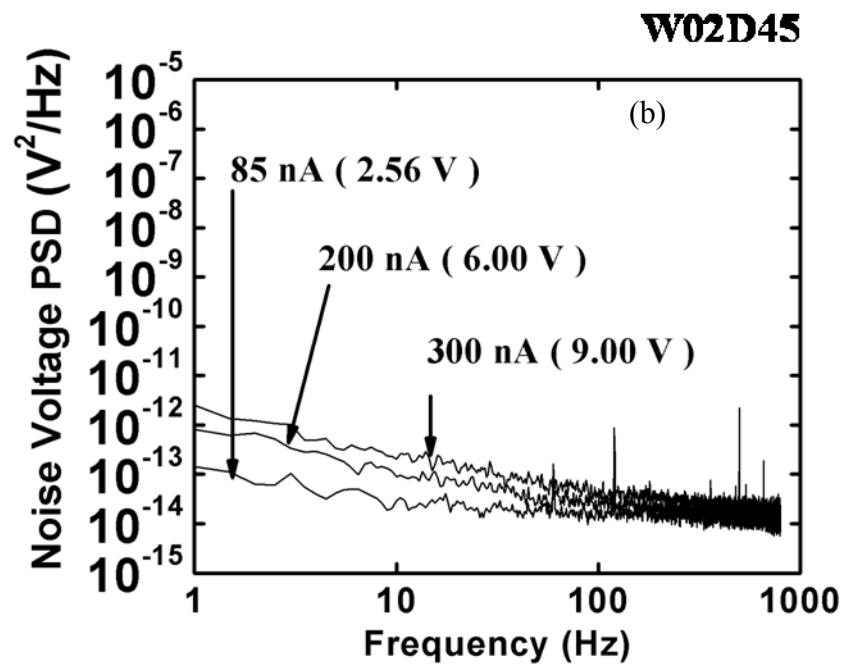
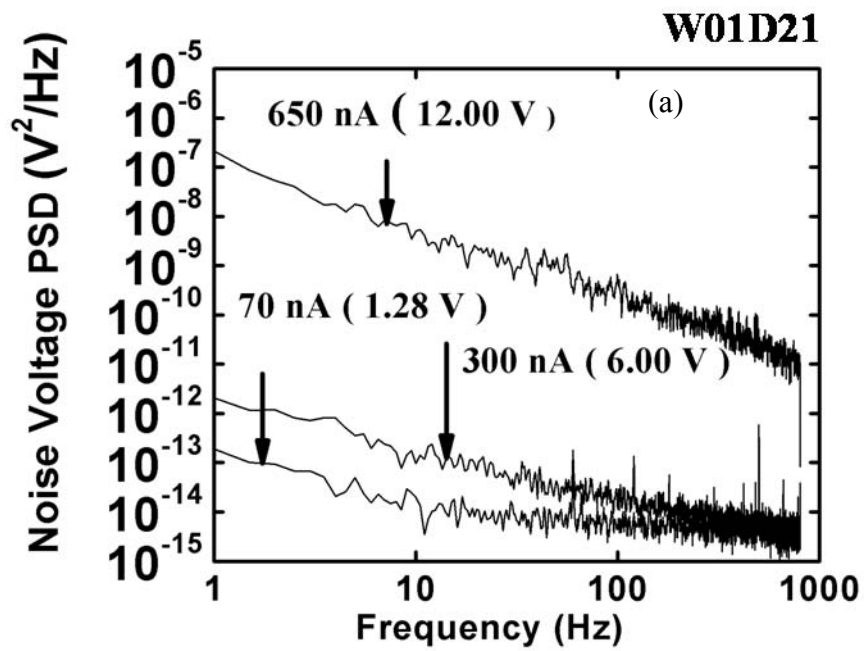


Figure 3.3.1.1 PSD noise with different biasing currents for before annealing: devices a) W01D21; b) W02D45

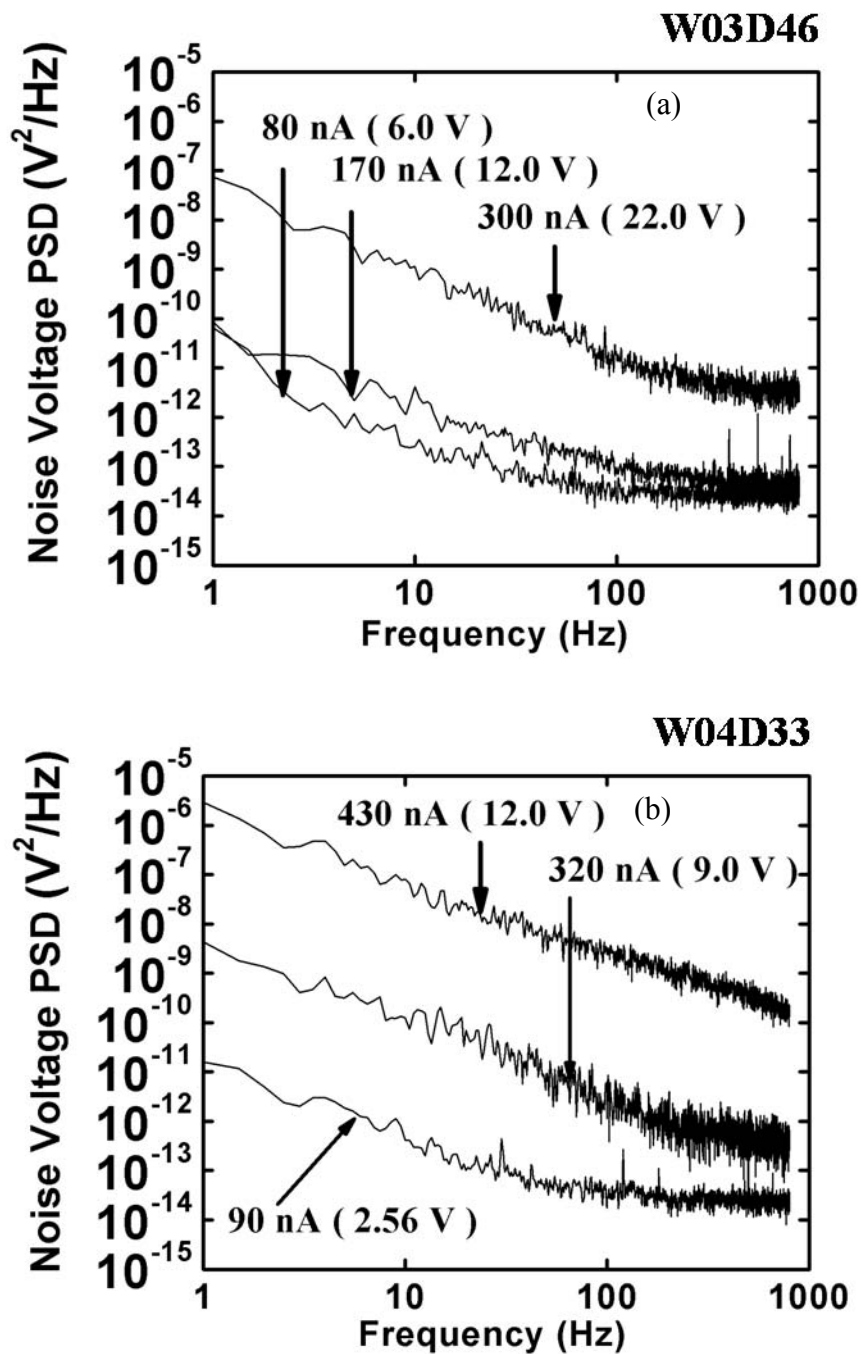


Figure 3.3.1.2 PSD noise with different biasing currents for before annealing: devices a) 03D46, b) W04D33

range demonstrate that some film compositions have a relatively low voltage noise PSD. The results shows that the voltage noise PSD of the four wafers were different before annealing devices with the lowest being observed in wafer W01 and the highest is in wafer W04. This indicates that the noise sources in the bolometer are due to the presence of trapping states, detrapping of carriers, and defects in $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ sensing layer. In this work, it will be shown that annealing the devices in vacuum will markedly eliminate the brown noise effect, and thus reinstating $1/f$ -noise as the main contributor. The encapsulation of $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ thin film with two Si_3N_4 passivation layers plays a dominant role in minimizing the surroundings and surface state effects in $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ which in turn reduces $1/f$ -noise [52]. This might have diminished the electron – hole recombination rate by lowering the density of interface traps. This results in decreasing the dangling bond, and thus reduces the $1/f$ -noise [5]. In addition, the passivation layers might have increased the mobility of the surface state in $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ thin films, which can be a result of dislocations, chemical residues and metallic sputter depositions on the surface [53, 54]. This will also lead to a lower $1/f$ -noise. Additionally, we have not observed any sudden increase in the noise level across the frequency spectrum in Figure 3.3.1. Thus, our devices do not suffer from generation – recombination (g-r) noise.

3.3.2 Noise study of microbolometer after annealing

Many devices from the same four wafers were annealed at 200 °C, 250 °C or 300 °C from 1 to 5 hours with a constant ramp of 20°C/min using a bias current of 0.07 μA . Figure 3.3.2 shows the measured noise voltage PSD for 12 devices from wafer W01, W02, W03, and W04 before and after annealing at 200 °C, 250 °C, and 300 °C for duration from 1 hour to 5 hours using a bias current of 0.07 μA . The corresponding

Hooge's parameters for the devices from the four wafers are presented in Table 3.3, Table 3.4, Table 3.5 and Table 3.6, respectively. The results show that annealing the devices has reduced the voltage noise PSD significantly on one wafer (W04). However, this reduction was not lower than that of the lowest measured voltage noise in the other devices before annealing

Table 3.2 Noise parameters of the devices before annealing for wafers W01 to W04.

Wafer	Device No.	γ	β	K_f	Noise PSD (V^2/Hz) at corner freq
W01	W01D21	1.19	1.71	3.65×10^{-14}	7.59×10^{-15} at 25 Hz with 70 nA
	W01D22	1.26	2.24	1.44×10^{-12}	1.88×10^{-14} at 80 Hz with 70 nA
	W01D52	0.93	2.21	3.46×10^{-13}	3.56×10^{-14} at 30 Hz with 80 nA
W02	W02D63	1.83	2.17	2.35×10^{-12}	1.47×10^{-14} at 50 Hz with 80 nA
	W02D64	1.37	1.58	4.94×10^{-13}	1.08×10^{-13} at 10.5 Hz with 80 nA
	W02D62	0.91	2.07	3.31×10^{-14}	2.54×10^{-14} at 11 Hz with 80 nA
	W02D45	0.91	1.93	3.01×10^{-14}	1.89×10^{-14} at 12 Hz with 85 nA
W03	W03D36	1.33	3.24	1.97×10^{-14}	1.82×10^{-14} at 190 Hz with 70 nA
	W03D45	1.59	3.71	1.19×10^{-12}	3.15×10^{-14} at 70 Hz with 80 nA
	W03D46	1.85	2.00	3.19×10^{-16}	3.24×10^{-14} at 70 Hz with 80 nA
	W03D48	1.61	4.92	1.6010^{-16}	4.16×10^{-14} at 11 Hz with 75 nA
W04	W04D43	1.78	2.62	3.33×10^{-11}	4.12×10^{-14} at 200 Hz with 80 nA
	W04D11	2.00	1.83	6.02×10^{-10}	5.58×10^{-13} at 200 Hz with 80 nA
	W04D33	1.58	2.19	2.74×10^{-13}	2.79×10^{-14} at 160 Hz with 90 nA

In addition, the $1/f$ -noise PSD was decreased significantly on devices that have abnormally high $1/f$ -noise before annealing (Figure. 3.3.2.5 b). The voltage noise PSD of the devices was decreased as the annealing time increased. For example, the lowest measured noise is $1.96 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 12 Hz for the device (W04D33) that annealed at 300 °C. After 4 hours of annealing, the voltage noise starts to increase again. It is noted that annealing at higher temperature 300 °C reduced the low frequency voltage noise PSD more than that of 200 °C and 250 °C temperature. The average value of γ was close to 1, was 0.8 for device W04D33, after 4 hours of annealing at 300 °C. This results clearly indicates that annealing have reduced the effect of any other noise sources, making the $1/f$ -noise as the main contributing source. The corresponding $1/f$ -noise coefficient (K_f) of device W04D33 was changed from 2.74×10^{-13} to 1.84×10^{-14} after 4 hours of annealing at 300 °C. The K_f value starts to increase after annealing at higher time interval. This increase is attributed to the reduction in $1/f$ -noise and the increase of β with increasing annealing time interval. In addition, the results show that annealing the devices has reduced the voltage noise PSD significantly on one wafer (wafer W04), and the $1/f$ -noise PSD was decreased significantly on devices that had abnormally high $1/f$ -noise before annealing (Figure. 3.3.2.1-3.3.2.6).

As the annealing time interval of the devices increases, the electrical noise level was reduced. This indicates that annealing at a specific time interval reduced the trapping states or defects in $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ sensing layer. After 3-4 hours of annealing, the corner frequency was shifted from around 70 Hz to around 12 Hz which indicates that Johnson noise can be observed after 12 Hz. Before 12 Hz, the frequency is dominated by $1/f$ -noise.

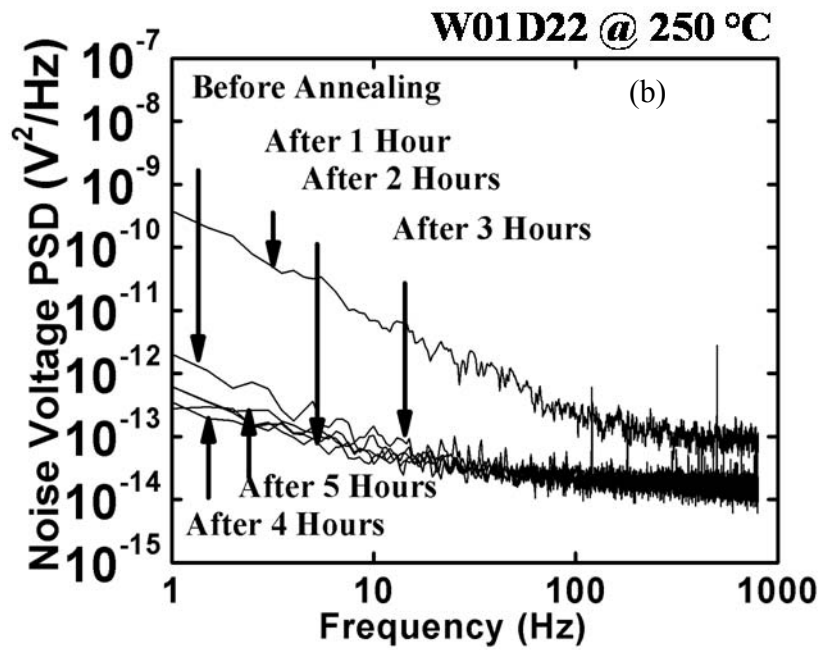
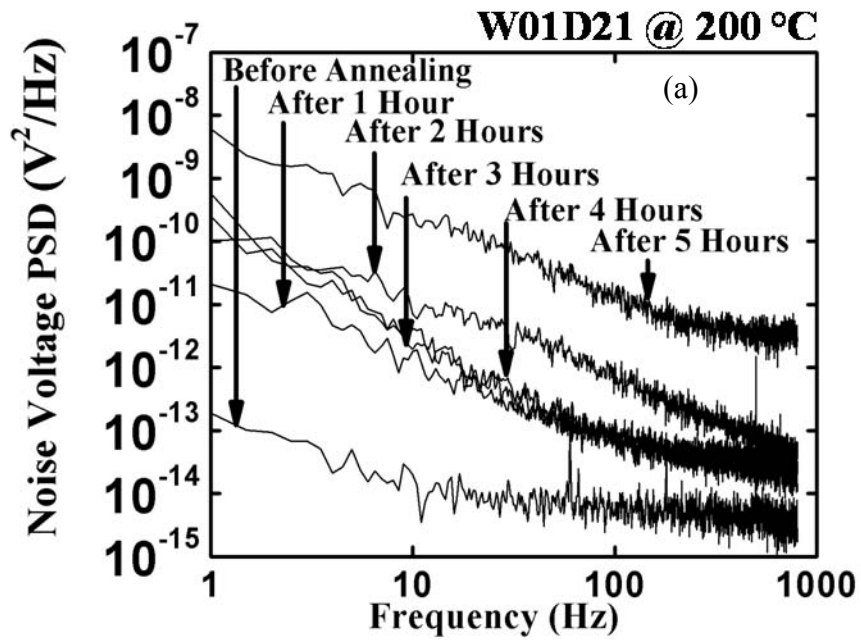


Figure 3.3.2.1 Noise PSD before and after annealing for different durations: devices a) W01D21, b) W01D22 annealed at 200°C, 250°C respectively.

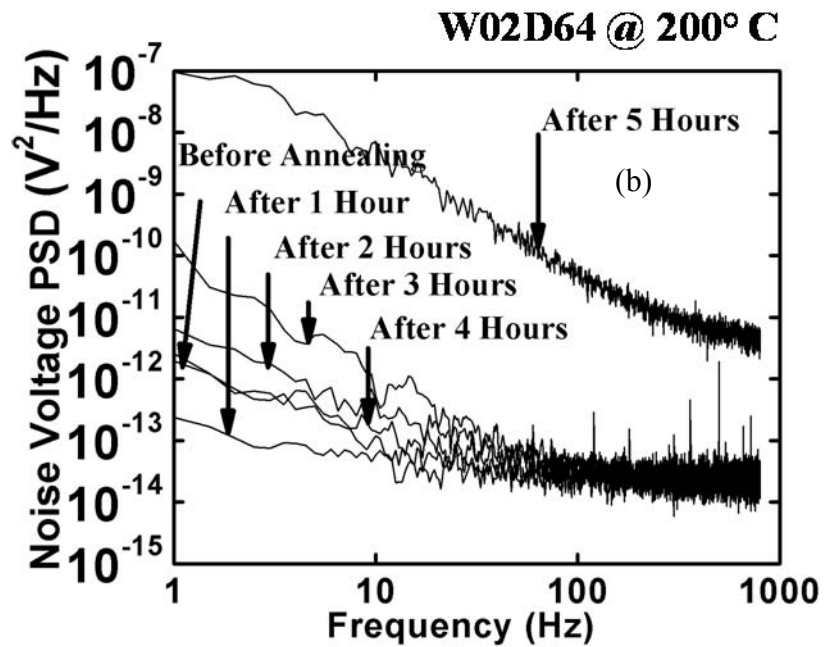
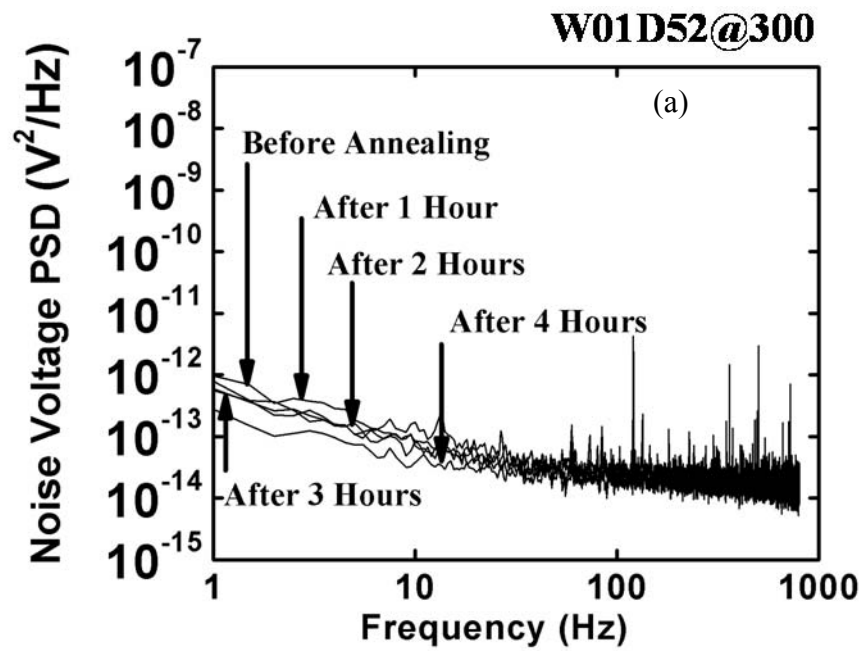


Figure 3.3.2.2 Noise PSD before and after annealing for different durations: devices a) W01D52, b) W02D64 annealed at 300°C, 200°C respectively.

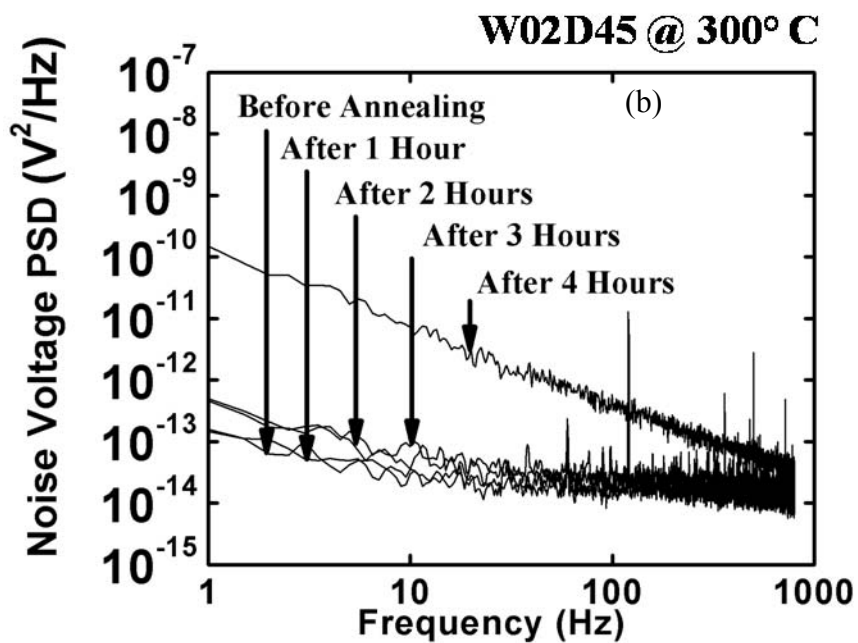
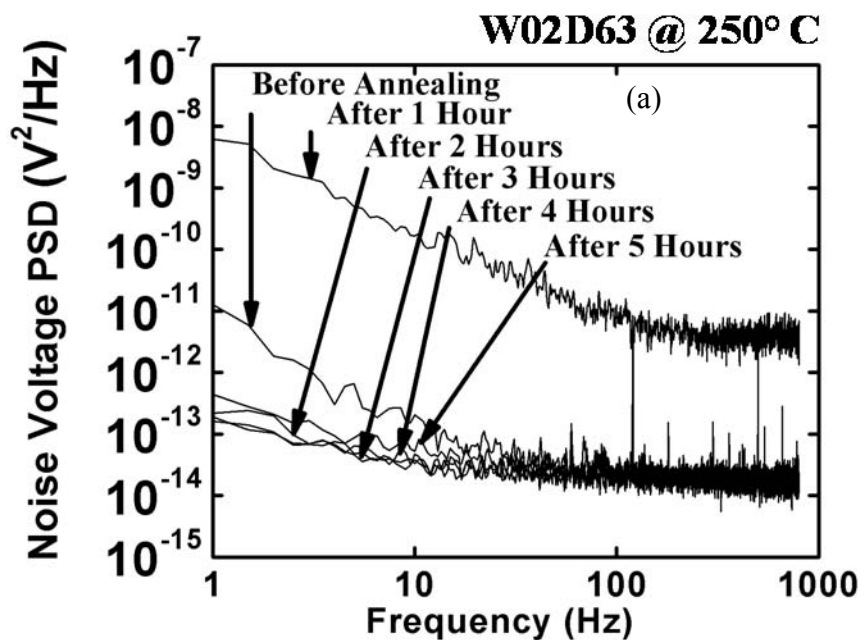


Figure 3.3.2.3 Noise PSD before and after annealing for different durations: devices a) W02D64, b) W02D45 annealed at 250°C, 300°C respectively.

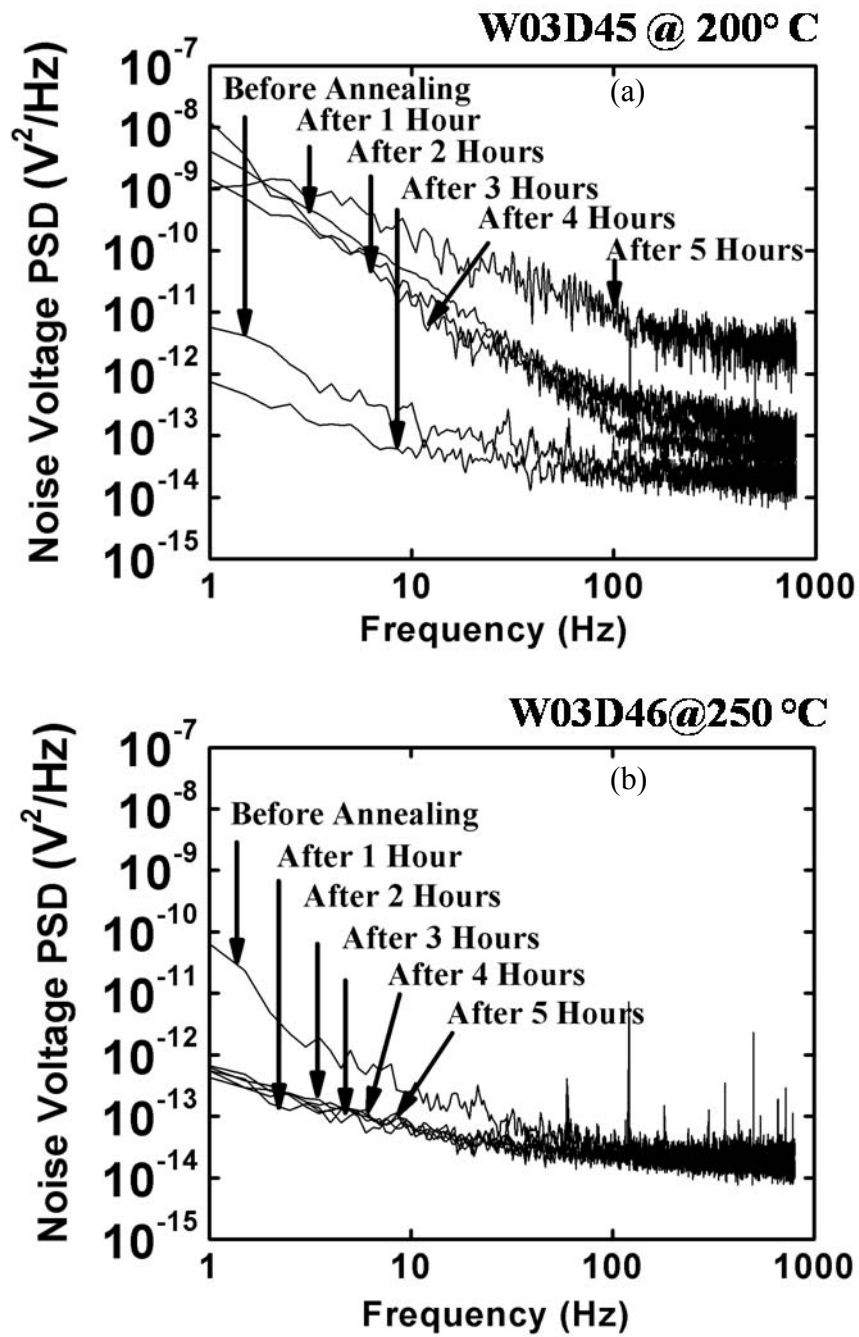


Figure 3.3.2.4 Noise PSD before and after annealing for different durations: devices a) W01D52, b) W02D64 annealed at 300°C, 200°C respectively.

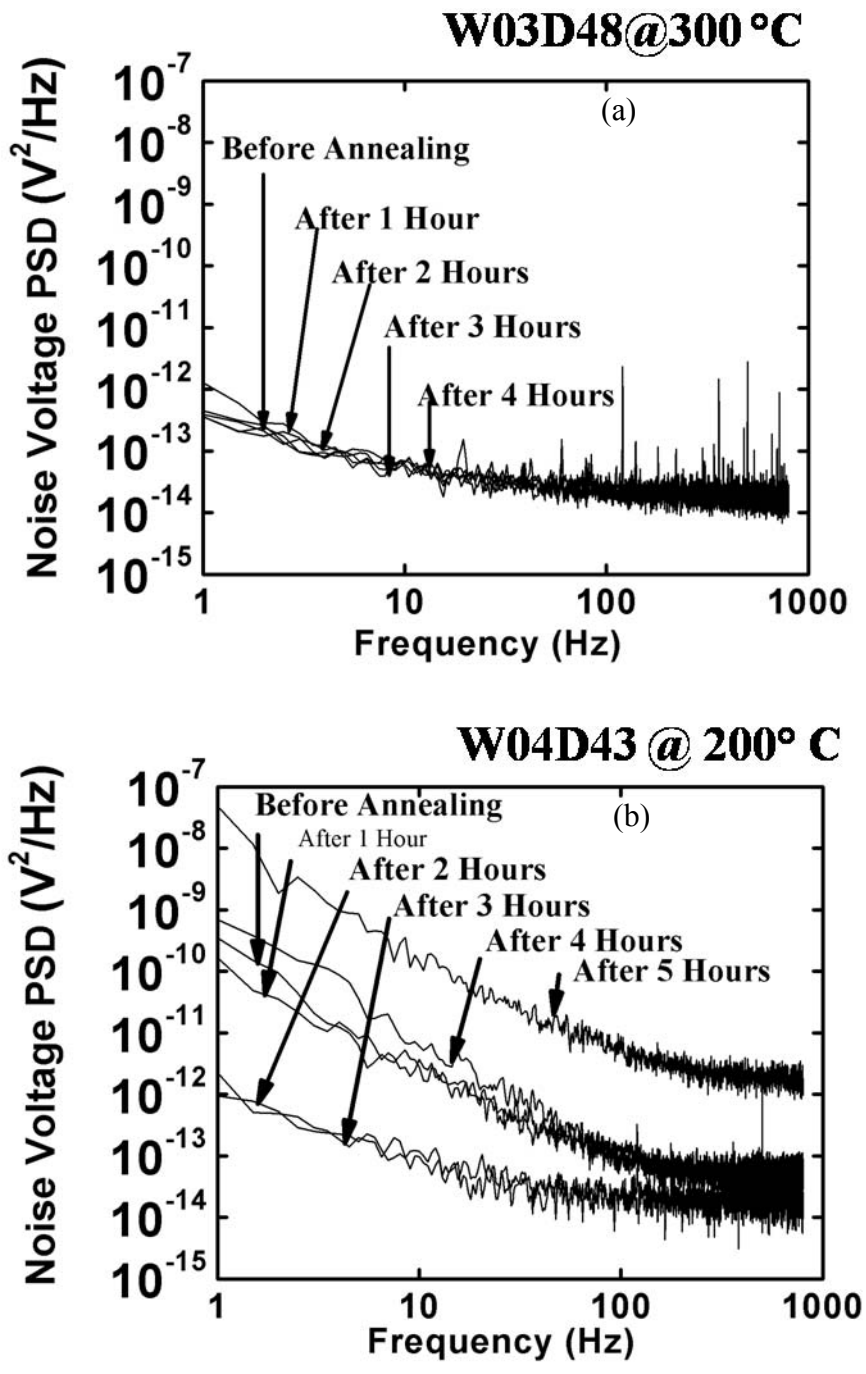


Figure 3.3.2.5 Noise PSD before and after annealing for different durations: devices a) W03D48, b) W04D43 annealed at 300°C, 200°C respectively.

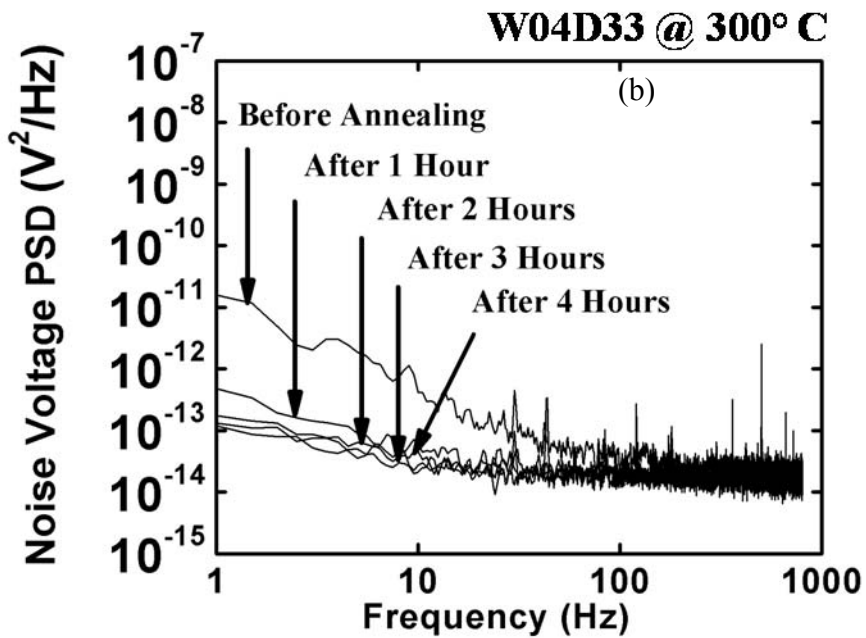
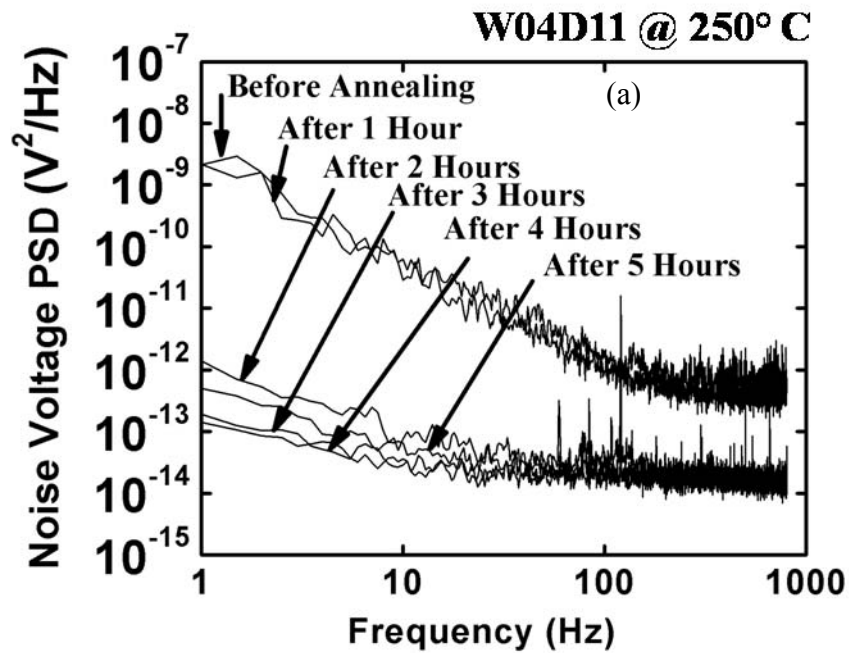


Figure 3.3.2.6 Noise PSD before and after annealing for different durations: devices a) W04D11, b) W04D33 annealed at 250°C, 300°C respectively.

Table 3.3 Variation of Hooge's parameters in different devices with different annealing time intervals for WaferW01.

Annealing Duration (Hours)	W01D21 @ 200 °C			W01D22 @ 250 °C			W01D52 @ 300 °C		
	γ	β	K_f	γ	β	K_f	γ	β	K_f
0	1.19	1.71	3.65×10^{-14}	1.26	2.24	1.44×10^{-12}	0.93	2.21	3.46×10^{-13}
1	1.06	2.68	7.53×10^{-12}	1.60	1.73	8.49×10^{-11}	1.03	2.00	6.34×10^{-13}
2	1.13	1.94	9.74×10^{-11}	1.00	1.88	2.23×10^{-13}	1.01	2.38	5.00×10^{-13}
3	1.62	2.00	8.02×10^{-11}	1.02	1.99	3.90×10^{-13}	0.92	2.11	3.26×10^{-13}
4	1.48	1.70	1.27×10^{-10}	0.95	2.00	2.02×10^{-13}	0.86	2.30	1.44×10^{-13}
5	1.58	0.65	8.90×10^{-09}	0.88	3.82	1.96×10^{-14}			

In for W 01, the annealing at 200 °C and 300 °C did not help reducing the voltage noise PSD. In fact, the noise was increased after annealing the devices at these temperatures, e.g., the value of γ for (W01D21) was increased from 1.19 before annealing to 1.58 after annealing for 5 hours at 200 °C, while K_f was increased from 3.65×10^{-14} to 8.90×10^{-09} for the same duration of annealing. On the other hand, at 250 °C, the noise level was slightly decreased for (W01D22). The value of γ was decreased from 1.26 before annealing to 0.88 after annealing for 5 hours, while K_f was decreased from 1.44×10^{-12} to 1.96×10^{-14} for the same duration of annealing. The decrease in K_f value indicates reduction in the noise level of the device.

In W 02, the voltage noise was slightly decreased after annealing the device for 1 hour at 200 °C. For example, for device (W02D64) the voltage noise PSD was reduced from 1.94×10^{-12} V²/Hz to 2.36×10^{-13} V²/Hz at 1 Hz with 70 nA. After 1 h, the voltage noise was increased with the highest measured noise was at 5 hours of annealing. The

value of γ for (W02D64) was increased from 1.37 before annealing to 0.79 after annealing for 1 hour at 200 °C, while K_f was increased from 4.94×10^{-13} to 5.12×10^{-14} for the same duration of annealing. At 250 °C, the noise level was decreased for (W02D63). The value of γ was decreased from 1.83 before annealing to 0.74 after annealing for 3 hours, while K_f was decreased from 2.35×10^{-12} to 5.96×10^{-14} for the same duration of annealing. The same behavior was observed for annealing at 300 °C.

In for W 03, the voltage noise was decreased after annealing the device at 200 °C, 250 °C, and 300 °C. For device (W03D45) the voltage noise PSD was reduced from 9.8×10^{-14} V²/Hz to 3.26×10^{-14} V²/Hz at 20 Hz with 70 nA. After 3 h , the voltage noise was increased.

Table 3.4 Variation of Hooge's parameters in different devices with different annealing time intervals for WaferW02.

Annealing Duration (Hours)	W02D64 @ 200° C			W02D63 @ 250° C			W02D45 @ 300° C		
	γ	β	K_f	γ	β	K_f	γ	β	K_f
0	1.37	1.58	4.94×10^{-13}	1.83	2.17	2.35×10^{-12}	0.91	1.79	3.73×10^{-14}
1	0.79	1.71	5.12×10^{-14}	1.37	2.23	2.08×10^{-10}	0.83	1.60	4.12×10^{-14}
2	1.47	2.60	8.94×10^{-12}	1.26	2.83	2.12×10^{-14}	0.87	1.67	4.65×10^{-14}
3	0.67	0.55	6.09×10^{-12}	0.74	1.19	5.96×10^{-14}	0.81	1.88	2.88×10^{-14}
4	1.57	4.74	6.00×10^{-14}	0.75	1.22	6.90×10^{-14}	1.21	0.33	6.23×10^{-11}
5	1.70	3.23	6.07×10^{-09}	0.95	2.00	3.70×10^{-14}			

The value of γ was decreased from 1.59 before annealing to 1.50 after annealing for 3 hours at 200 °C, while K_f was increased from 1.19×10^{-12} to 7.23×10^{-14} for the same duration of annealing. At 250 °C a similar behavior was observed, the noise level was

decreased for (W03D46). The value of γ was decreased from 1.84 before annealing to 0.96 after annealing for 3 hours, while K_f was decreased from 1.56×10^{-12} to 2.74×10^{-14} for the same duration of annealing. The annealing at 300 °C for various time intervals did not change the noise level at all. However, the γ and K_f were changed from 1.61 and 1.60×10^{-16} to 1.05 and 2.26×10^{-14} after 2 hours of annealing, respectively.

Table 3.5 Variation of Hooge's parameters in different devices with different annealing time intervals for wafer W03.

Annealing Duration (Hours)	W03D45 @ 200° C			W03D46 @ 250° C			W03D48 @ 300° C		
	γ	β	K_f	γ	β	K_f	γ	β	K_f
0	1.59	3.71	1.19×10^{-12}	1.84	1.62	1.56×10^{-12}	1.61	4.92	1.60×10^{-16}
1	1.54	4.04	2.58×10^{-13}	0.88	1.96	1.74×10^{-14}	1.20	3.05	3.32×10^{-15}
2	1.88	2.87	5.19×10^{-12}	0.98	2.13	1.27×10^{-14}	1.05	2.05	2.26×10^{-14}
3	1.50	1.88	7.23×10^{-14}	0.96	1.73	2.74×10^{-14}	1.46	3.38	1.97×10^{-15}
4	1.92	1.18	1.53×10^{-09}	0.87	1.54	3.67×10^{-14}	1.01	0.85	6.55×10^{-14}
5	1.72	1.81	5.98×10^{-11}	0.92	1.66	3.70×10^{-14}			

We have plotted the lowest measured voltage noise PSD at 0.07 μ A of the four wafers before and after annealing at 300 °C (Figure 3.3.3). The results show that three wafers have relatively similar noise level while wafer W04 has the highest voltage noise before annealing. This might be due to the higher Ge concentration in the film. The voltage noise PSD after annealing was comparable with wafer W03 with the highest voltage noise. A potential source of $1/f$ -noise is the bond formation of $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ sensing layer in terms of Si-O and Ge-O bond formation [28, 29]. The bonds might have

resulted in large number of defects in the film and thus contributed to the presence of $1/f$ -noise.

Table 3.6 Variation of Hooge's parameters in different devices with different annealing time intervals for wafer W04.

Annealing Duration (Hours)	W04D43@ 200° C			W04D11@ 250° C			W04D33@ 300° C		
	γ	β	K_f	γ	β	K_f	γ	β	K_f
0	1.78	2.62	3.33×10^{-11}	2.00	1.83	6.02×10^{-10}	1.58	2.19	2.74×10^{-13}
1	1.87	1.82	2.30×10^{-11}	1.80	6.33	5.87×10^{-08}	0.95	1.43	1.81×10^{-13}
2	0.99	2.04	2.39×10^{-13}	0.82	2.51	2.42×10^{-13}	1.37	3.50	1.56×10^{-14}
3	1.22	2.41	4.16×10^{-13}	0.76	1.55	2.19×10^{-16}	0.81	2.56	1.36×10^{-14}
4	2.07	2.59	9.55×10^{-09}	1.06	3.92	7.17×10^{-15}	0.80	2.33	1.84×10^{-14}
5	1.83	0.20	6.77×10^{-08}	1.18	2.81	4.43×10^{-14}			

The bonding Si with O creates paramagnetic defects which leads to unpair of electron with a silicon dangling bond [55]. Similarly, Ge-O and Ge-Ge bonding leads to dangling bond of Ge. The XRD study of the four wafers, confirmed the presence of dangling bonds since we have not observed any sharp peak in the spectrum, suggesting amorphous nature of all films, and lack of long range order. In addition, to the presence of dangling bonds, the presence of deep traps and recombination centers in Si-Ge bond, and the interface between NiCr metal and $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ semiconductor film might have contributed to the increase in $1/f$ -noise level [35, 56]. The metal semiconductor interface might have contributed to the noise level due to the cleanliness of the contacts and the possible formation of Schottky junction [28]. After 4 hours annealing in vacuum at low

pressure, we have observed significant reduction in noise in wafer W04, and slight reduction in the wafer W01. This indicates that annealing in vacuum has reduced the number of dangling bond, recombination centers, and impacted the metal-semiconductor interface. After 3-5 hours of annealing, the voltage noise PSD starts to increase significantly. This might be due to the increase of dangling bonds, low field mobility [54] and the oxide traps [57]. In addition, the long exposure to heat during annealing might have increased some source of $1/f$ -noise such as the dislocations, surface and bulk phenomena [19, 23, 58, 59]. From Table 3.7, it is seen that after annealing noise voltage

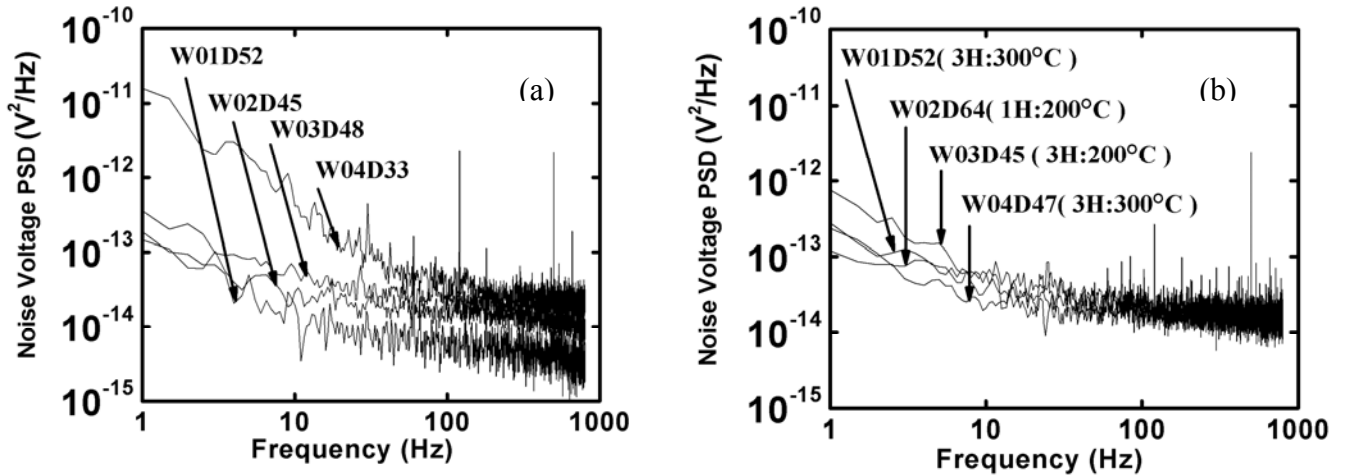


Figure 3.3.3 Comparison with low PSD noise: a) before annealing and b) after annealing from four wafers W01-W04 at biasing current of 80 nA.

PSD decreases for device number W02D45, W03D45 and W04D33 but device number W01D21 shows opposite behavior. Moreover, corner frequency reduces for W01D21 and W04D33 whereas other two devices W02D45 and W03D45 increase from 12 Hz to 23 Hz and 70 Hz to 77.5 Hz. Therefore, after heating the devices the corner frequency decreases since the slope decreased. For example, device W01D21 the value of γ decreased from 1.19 to 1.06, device W02D45 was 0.91 to 0.83 at 1 h interval, device

W03D45 was 1.59 to 1.50 at 3 h interval and device W04D33 was 1.58 to 0.80 at 4 h intervals. The value of β also decreased.

Table 3.7 Comparison with Low voltage noise PSD before and after annealing at the corner frequency.

Wafer	Before Annealing		After Annealing		
	Noise Voltage PSD (V ² /Hz)	Corner Frequency (Hz)	Noise Voltage PSD (V ² /Hz)	Annealing Interval (Hour)	Corner Frequency (Hz)
W01D21	7.59×10^{-15}	25	6.2×10^{-13}	1h@200°C	12
W02D45	1.89×10^{-14}	12	1.13×10^{-14}	1h@300°C	23
W03D45	3.15×10^{-14}	70	1.5×10^{-14}	3h@200°C	77.5
W04D33	2.79×10^{-13}	160	1.96×10^{-14}	4h@300°C	12

We have also compared the voltage noise PSD at 30 Hz camera frame rate. Table 3.8 represents the noise voltage PSD for before and after annealing at 30 Hz. The noise voltage PSD was the highest for device W03D46 from wafer 03 before and after annealing at 30 Hz. The device W04D33 from wafer 04 demonstrated the lowest noise after annealing which reduced from 4.5×10^{-13} to 1.30×10^{-14} (V²/Hz). The results show that annealing has reduced the voltage noise PSD in all wafers.

Table 3.8 Comparison with low noise voltage PSD before and after annealing at 30 Hz-IR thermal camera frame rate.

Wafer	Noise Voltage PSD	Noise Voltage PSD
	Before Annealing (V²/Hz)	After Annealing (V²/Hz)
W01D52	3.89×10^{-14}	2.59×10^{-14}
W02D63	4.77×10^{-14}	2.33×10^{-14}
W03D46	8.1×10^{-14}	3.42×10^{-14}
W04D33	4.5×10^{-13}	1.30×10^{-14}

CHAPTER 4

CONCLUSION

This thesis is focused on measuring and reducing the low-frequency noise voltage power spectral density (PSD) of silicon germanium oxide ($\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$) uncooled IR microbolometers. These microbolometers were fabricated on four silicon wafers with four different compositions of silicon germanium oxide (namely $\text{Si}_{0.053}\text{Ge}_{0.875}\text{O}_{0.072}$ is W01, $\text{Si}_{0.041}\text{Ge}_{0.902}\text{O}_{0.057}$ is W02, $\text{Si}_{0.081}\text{Ge}_{0.853}\text{O}_{0.066}$ is W03 and $\text{Si}_{0.034}\text{Ge}_{0.899}\text{O}_{0.067}$ is W04). The microbolometer pixel area was $40 \times 40 \mu\text{m}^2$. The noise reduction was achieved by passivating $\text{Si}_x\text{Ge}_y\text{O}_{1-x-y}$ with Si_3N_4 layers and by annealing the devices in vacuum at 200 °C, 250 °C, or 300 °C with different time interval from 1 to 5 hours. The noise measurements results demonstrate that the voltage noise PSD depends on the percentage of silicon, germanium and oxygen. For example, a large concentration of germanium has reduced the performance of the microbolometer since it had a high voltage noise PSD.

The measured TCR and resistivity at room temperature were $-3.518/\text{K}$ and $0.763 \times 10^3 \Omega \cdot \text{cm}$, $-2.590/\text{K}$ and $1.170 \times 10^3 \Omega \cdot \text{cm}$, $-3.864/\text{K}$ and $3.573 \times 10^3 \Omega \cdot \text{cm}$ and $-3.103/\text{K}$ and $0.730 \times 10^3 \Omega \cdot \text{cm}$ for devices from W01, W02, W03 and W04, respectively. The TCR is relatively high in comparison with other IR material. The corresponding resistivities were less than $1000 \Omega \cdot \text{cm}$, within the acceptable range for W01, and W04. The current-voltage of these devices were linear suggesting that they did not suffer from Joule-heating effect up to $0.8\text{--}1 \mu\text{A}$, with the exception of wafer 3, it was up to $0.2 \mu\text{A}$.

The lowest measured voltage noise PSD at the corner frequency of several devices (W01D21, W02D45, W03D36 and W04D33) from the four fabricated wafers before annealing were $7.59 \times 10^{-15} \text{ V}^2/\text{Hz}$ at 80 Hz, $1.89 \times 10^{-14} \text{ V}^2/\text{Hz}$ 11 Hz, $1.82 \times 10^{-14} \text{ V}^2/\text{Hz}$ 190 Hz, and $2.79 \times 10^{-14} \text{ V}^2/\text{Hz}$ 160 Hz respectively. These values are relatively high since the corner frequency was above 30 HZ camera frame rate with the exception of wafer 2 where the corner frequency was at 11 Hz. The corresponding $1/f$ -noise coefficients for the four wafers, K_f , were 3.65×10^{-14} , 3.01×10^{-14} , 1.97×10^{-14} , and 2.74×10^{-13} respectively. These results demonstrate that devices from W01 (W01D21) have the lowest measured noise at the corner frequency (80 Hz). In contrast, W04 (W04D33) demonstrated the highest voltage noise PSD and the highest corner frequency (160 Hz).

The annealing of these devices and others from the same four wafers in vacuum at 4 m Torr for a time interval between 1-5 hours with each time interval increase by 1 hour at either 200 °C, or 250 °C, or 300 °C have reduced the voltage noise PSD. The measurements showed that the voltage noise PSD was reduced as the annealing time interval was increased to a certain time period, after that the voltage noise PSD started to increase again. For example, the lowest measured noise of each device from the four wafers at the corner frequency (W01D21, W03D45 and W04D33) after 3h or 4 h time interval, was $1.96 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 12 Hz, $1.5 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 77.5 Hz, $2.11 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 12 Hz, respectively. However, in wafer 02 (02D45) the voltage noise PSD was $1.13 \times 10^{-14} \text{ V}^2/\text{Hz}$ at 23 Hz with 1 h period of annealing. In addition, the results presented that the voltage noise PSD of device W04D33 was significantly lowered after annealing at 300 °C for 4 hours while in devices in W01, W02, and W03, the noise was reduced slightly with the exception of W01D21 at 200 °C, in fact increased after annealing. It is clear that

annealing at higher temperature 300 °C has reduced the low frequency voltage noise PSD more than that of 200 °C and 250 °C temperature.

The measured Hooge's parameter of the three devices from W04 after annealing were 2.39×10^{-13} for W04D43 at 200 °C in 2 h period, 2.19×10^{-16} for W04D11 at 250 °C in 3 h period and 1.36×10^{-14} for W04D33 at 300 °C in 3 h period. Other devices from W01, W02 and W03 the measured Hooge's parameters decreased after annealing. For example, before annealing the noise parameters (γ , β and K_f) of the device W01D22 were 1.26, 2.24 and 1.44×10^{-12} which are 0.95, 2.00 and 2.02×10^{-13} after annealing, and for the device W03D45 the noise parameters were 1.59, 3.71 and 1.19×10^{-12} but which are seen 1.50, 1.88 and 7.23×10^{-14} after annealing, respectively. However, annealing of devices reduced the noise parameter K_f . Moreover, noise voltage PSD showed diminishing trend after heating devices at 30 Hz camera frame rate. This clearly indicates that annealing the device at higher temperature enabled the reduction of $1/f$ -noise. The possible reasons for the reduction of voltage noise are the dangling bonds, grain boundary and crystal structure were repaired in sensing layer after heating the devices. Trapping-detrapping mechanism stated inside the interfacial oxide was also a potential source of increasing $1/f$ -noise. The problem of whether or not more annealing time intervals might have increased dislocation or the number of dangling bonds would be a good topic for future study. Future study is also needed to look at whether the annealing time created defects in sensing layers leading to further increase in the noise voltage PSD.

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