DESIGN OF A LOW-POWER ANALOG CIRCUIT FOR AN IMPLANTABLE RFID-ENABLED DEVICE WITH PASSIVE PRESSURE SENSOR

A THESIS IN
Electrical Engineering

Presented to the Faculty of the University
of Missouri-Kansas City in partial fulfillment of
the requirments for the degree

MASTER OF SCIENCE

by
SAGNIK KAR

B.TECH., S.R.M. UNIVERSITY, 2008

Kansas City, Missouri
2011

DESIGN OF A LOW-POWER ANALOG CIRCUIT FOR
AN IMPLANTABLE RFID-ENABLED DEVICE
WITH PASSIVE PRESSURE SENSOR

Sagnik Kar, Candidate for the Master of Science Degree
University of Missouri-Kansas City, 2011

ABSTRACT

A low-power analog core for an implantable RFID-enabled pressure measurement system is designed. The analog core includes the power generation block for the system, the clock extractor for the digital core and the pressure sensor data converter. Circuit design constraints of low-power consumption and small form factor were followed in the implementation of the analog core. A new low-power analog-to-digital converter (ADC) for the pressure sensor is designed. The designed data converter is implemented using charge-distribution technique which consumes 90 μW of power and has a resolution of 12 bits making it suitable for such energy-constrained applications. The designed ADC is targeted towards a commercially available passive capacitive pressure sensor (microFab E1.3N). Cadence Virtuoso 6.1 Analog Design Environment simulators are used to design, test and compare the schematic and post-layout simulations of the components. The developed analog circuit will be a part of an implantable RFID chip with passive sensors which can communicate with RFID readers.

The faculty listed below, appointed by the Dean of the School of Computing and Engineering have examined a thesis titled "Design of a Low-Power Analog Circuit for an Implantable RFID-Enabled Device with Passive Pressure Sensor," presented by Sagnik Kar, candidate for the Masters of Science in Electrical Engineering degree, and certify that in their opinion it is worthy of acceptance.

Supervisory Committee

Walter D. Leon-Salas, Ph.D., Committee Chair
Department of Electrical Engineering

Ghulam Chaudhry, Ph.D.
Department of Electrical Engineering

Deb Chatterjee, Ph.D.
Department of Electrical Engineering

CONTENTS

LIST OF ILLUSTRATIONS

Figure Page

LIST OF TABLES

ACKNOWLEDGEMENTS

Working on a thesis research project has been a very exciting experience. This excitement can become very challenging in a few occasions. In these few trying times motivation plays an important role to reinforce the confidence. I would like to thank my father, who has continuously motivated me. Being an IIT-Delhi alumni, he has always mentioned some his greatest challenges during his maters coursework. This has guided me to be more careful and more diligent at my approach towards research. I also thank my mother who has been ever caring and has pushed me to achieve the very best.

My thesis advisor, Prof. Walter D. Leon-Salas, has been my mentor in all the academic endeavors at UMKC. From the very first course of 'Analog IC Design', he has encouraged me to think logically. His mode of instruction, problem solving techniques and critical reasoning has been the driving force for this research. Being his research assistant has benefited the progress of the thesis immensely and has enabled me to publish my first IEEE conference publication. Also, I am thankful for the various graduate teaching assistant positions in the Department of Computer Science and Electrical Engineering (CSEE) which have been helpful to extend my knowledge base.

I would also like to thank Prof. Ghulam Chaudhry and Prof. Deb Chatterjee who are on my thesis committee for their continued support towards my thesis as well as academic progress. I am thankful to them for offering specialized courses like VLSI design has been very helpful in many parts of thesis. I would also like to thank my fellow researchers who have aided me with their useful insights during the course of my thesis work.

CHAPTER 1

INTRODUCTION

1.1 Implantable Sensors

The last two decades have witnessed a surge in research involving applications of electronic sensing technology. Electronic sensors measure real-world physical quantities in both engineering as well as biomedical applications and convert them to signals which can be processed to develop an understanding of the physical quantity. Many different types of electronic sensors are classified based on application, form factor, power requirement and resolution. The ability to measure the smallest change in the physical quantity is often very important in applications which define the electronic sensor's resolution. High resolution sensing applications include biosensors, pressure sensors, temperature sensors, etc. Form factor and power requirement are other important parameters which are determined by the location/placement of the sensor. Applications involving wireless, miniaturized and implantable sensing often require low-power consumption and small form factor. Many of these power constrained miniaturized-implantable sensors are passive sensors which do not require a battery for operation.

In recent years greater emphasis is given on research involving low-power, miniaturized-wireless sensors which can be used in a wide variety of applications where minimum human intervention and higher mobility is a requirement. A good example of such a requirement is in biomedical application involving post-op diagnostics of patients affected by heart failure. According to recent studies [1] – [5], heart failure affects

approximately 2% of the adult population in developed countries and 6%–10% of people over the age of 65. During the first year after diagnosis, mortality rates of 30%–40% have been reported, and after five years, this percentage increases to 60%–70% [5]–[7]. The burden imposed by advanced heart failure is compounded by frequent hospitalizations due to congestive or low-output symptoms, renal and respiratory dysfunction, anemia, arrhythmia, and other systemic complications. Frequent hospitalizations can be minimized by the use of wireless implantable sensors to remotely monitor vital heart function and renal function parameters.

Sensors which are widely employed in implantable sensing purposes are broadly categorized into active and passive types. Passive sensors are advantageous over active sensors as they do not need power source to generate an output, although the output may be very low in magnitude and may need amplification before they can be used for signal processing. To reduce wiring and tethering wireless implantable sensors are often implemented using passive sensors. Power source for the supporting system used with these passive sensors is obtained by the use of RF inductive coupling along with full-wave rectification as is done in Radio Frequency Identification (RFID). RFID-enabled sensors are classified into two variants: active and passive sensors. Active sensors have the advantage of increased communication range but require a battery which limits the scope of such a device in implantable applications. The lifetime of such a sensor is limited by the battery capacity. This limitation is compensated by the use of passive RFID-enabled sensors which use passive circuits that do not require an internal power source and uses backscattering modulation to transmit data back to the reader, thereby,

providing unlimited sensor-lifetime, although the communication range is limited. Comparatively, passive RFID-enabled sensors have longer lifetime and are more affordable as it does not require regular battery replacements.

Many biomedical diagnostics involve cardiovascular blood pressure measurement and intraocular fluid pressure measurement. These pressure measurements can be efficiently addressed by the use of capacitive sensors. A capacitive sensor has a fixed bottom plate and a flexible top plate whose displacement varies with the application of pressure on the top plate. This variation in displacement changes the distance between the two plates which changes the capacitance of the sensor. Commercial miniature capacitive sensors exhibit a large fixed capacitance and a small variable capacitance. The change in this small variable capacitance corresponds to the applied pressure or displacement on the capacitive sensor. The variance in capacitance in the sensor corresponds to the real-world physical quantity. The analog signal is converted to its digital equivalent by the use of a Capacitance to Digital Converter (CDC). A digital representation of pressure is preferred for higher robustness to noise during data transmission and simpler data processing.

1.2 Prior work

A brief literature survey of previously published research work is presented. Some of the circuits presented in this thesis are based on the research papers presented in the following paragraphs and on text book material. Some circuits in this thesis are original and innovative.

One of the earliest works on passive telemetry IC for biomedical applications was presented by Q. Huang et al [8] in 1998. The authors propose a low-power, single-chip, one-channel, fully implantable micro-transponder system. The circuit is powered by an external RF source of 27 MHz or 40 MHz. The circuit is implemented in a 2 μm 40-V BiCMOS technology. The system uses a magneto-resistive strain gauge bridge to measure distance between the artery walls after every systole (phase of heart contraction). The system uses a BiCMOS RF/DC converter. For the analog front end, a fully differential operational transconductance amplifier with a gain of 26dB and a CMRR of more than 60 dB is used to amplify the low voltage levels from the sensors. To decrease the effect of any externally induced noise, a low-pass 50Hz notch filter with a Q factor of 2 is implemented. The authors have designed a 9-bit dual-slope Analog to Digital Converter (ADC) to digitize the analog signal from the sensor after amplification. The data from the ADC is placed in a parallel in serial out shift register (PISO) which is then converted to a low-duty-cycle pulse position modulation (PPM) signal and transmitted using amplitude modulation. The total power consumption is 0.5mW. The core area of the chip is 3.6 x 4.3 mm^2. The main drawback of this architecture is the use of dual-slope ADC, which counts in both the charge and discharge phase, requiring up-to 8 ms to finish one conversion cycle. The ADC also has a high power consumption of 250 μW. Another drawback is the RF/DC converter which has an efficiency of less than 30% at 27/40 MHz. This causes a decrease in the operating range to maintain adequate power levels for operation.

Another research paper which is very helpful for the analog front-end design was presented by Sauer et al [9]. The paper demonstrates power harvesting and telemetry function in CMOS for implanted devices. The demonstrated testbed comprises a wireless data communication system which is also used to power the system. The use of sensors to acquire implantable data is not demonstrated in this paper. The system operates on a radio frequency of 4 MHz which supplies 2.7 mA at 3.3 V over a distance of 25 mm. The proposed chip is fabricated on a 0.5 μm CMOS technology. The analog front-end in that paper elaborates the inductive coupling theory and its application. A generic quad PMOS transistor rectifier is used with an external RC filter to remove voltage ripples. The rectified voltage is fed to the voltage regulator and the voltage reference circuit to obtain a stable voltage supply. A series of inverters are used as a clock recovery circuit to be used in the data encoding and modulation blocks. The main drawback of this design is that a minimum of 7 V is required to be present on the coil for an output voltage of 3.3 V. This limits the range of operation of the sensor. Another drawback is in the design of the voltage regulator where the pass transistor does not switch on completely. This reduces the current supplied to the circuit.

Exponential growth in research interest of implantable sensor technology in the previous few years has produced several research proposals of innovative ADC designs for sensors.

The research paper by Y. Yanng et al [10] proposes a time based energy efficient ADC. The authors propose a novel current-mode algorithm which performs the analog to digital conversion in 5N clock cycles in contrast to the 2^{N+1} clock cycles required by a

conventional dual slope ADC. The proposed system is implemented in a 0.35 μm CMOS technology and has a precision of 12 bits at a sampling frequency of 31.25 kHz. The total power dissipated is 75 μW with a voltage supply of 3 V. The system uses an alternating voltage-to-time and time-to-voltage conversion which provides error cancellation of comparator offset, delay and switching charge-injection. The proposed novel current mode algorithm consists of two distinct stages. The first stage calculates the first two most significant bits (MSB) in a method identical to a conventional dual slope ADC. The second stage iteratively calculates the remaining bits by a subtraction-and-amplification process similar to the one used in a successive subranging converter. The main drawback of this system is the assumption of a constant comparator delay which in fact changes slightly as a function of the voltage at which the comparator is triggered. This causes discontinuities in the INL plot. Another drawback lies in the algorithm which implements a time-based converter that digitizes asynchronous time intervals with respect to a clock period in the second phase. This limits the bit precision scaling like O(N) instead of $O(N^2)$ as in conventional time to digital converters (TDC).

Another paper worth mentioning was presented by B. George et al [11] in 2006. It reports a triple-slope differential capacitance type ADC specially designed for sensors used in the measurement of pressure, displacement and acceleration. The authors propose two innovations from the traditional dual-slope ADC. The first is that the RC in a conventional dual slope ADC is replaced with a switched-capacitor integrator and the second deviation is that the control logic is altered to perform three integrations instead of the two in a conventional ADC. The system consists of two variable capacitors which are

set by the change in measuring attributes. Using the principles of charge distribution the charge in both the capacitor is transferred subsequently to a feedback capacitor and measured for greater accuracy. The drawback of this design is the use of large variable capacitors of 240 pF. Implantable capacitive pressure sensors have a very small capacitive component when compared to this, making it difficult to be used with implanted sensors. The worst case error of the proposed system is less than 0.5%, however is the use of triple slope technique as it has high power requirements.

Among the most recent research paper on wireless bio-signal acquisition system implemented on a hawk-moth was presented by Yeager et al [12] in 2010. The authors present a fully passive 900 MHz RFID tag IC capable of addressability , full EPC Class 1 Generation 2 protocol compatibility , an integrated noise chopper-stabilized micro-power sensor interface amplifier and an 8 bit ADC. The analog core consists of ultra low-power linear regulators, band-gap reference and bias current generator to provide a stable bias and voltage/current supply for the chip. A six stage voltage-doubling charge-pump topology is used as a RF rectifier. Specially designed zero-V_{th} diode connected NMOS devices are used for high sensitivity and efficiency. The authors use cascode devices in bias current generators and voltage regulators to maintain a constant output current and voltage. Three low-drop-out linear regulators provide stable supplies for the 1.2 V analog core, 0.7 V digital core and an auxiliary 1.8 V supply for any off-chip ICs. Bandgap references are used to provide stable voltages across 0-100^{o}C temperature ranges. The sensor input signal (e.g., EEG, EMG, thermocouple) is first amplified with the on-chip low-noise chopper-stabilized amplifier. An 8-bit successive-approximation (SA) ADC

then digitizes the sensor data. The sensor data is associated with a person or animal by means of a unique tag ID (UID). The digital core consists of the on-chip controller logic that encodes the UID and ADC data into a gen2-compatible packet in response to reader commands. The UID and sensor data is available for real-time use by a PC through ethernet connection to the reader. The RF communication range is stated as 3m. The bio-signal acquisition system consumes 9.2 μA with a voltage supply of 3 V. The system is fabricated in a 0.13um CMOS process. The total IC area is 2.0 mm^2. The main drawback of this proposed system is the use of UHF RF signal which is susceptible to attenuation due to moisture and hence decreasing the signal to noise ratio. In a previous study conducted by Vaillancourt et al [13] in 1997 it is demonstrated that RF energy between 1 and 10MHz penetrates the body with minimum energy loss. This makes the use of UHF signal highly inefficient for implantable purposes. Another drawback is the use of the 8 bit SA ADC. For implantable applications a higher resolution ADC is desirable and the conventional SA ADC architecture can be modified to reduce power consumption and total conversion time. Although the chip covers a small area, the PCB used to support the chip is very large at 0.91 cm x 0.73 cm. The use of external micro-powered opamp for additional thermocouple gain and the off-chip L-match network increases the PCB area. This makes it undesirable for implantable applications.

MicroFAB, an industry leading manufacturer of pressure sensors, has introduced a capacitive pressure sensor, E1.3N [14], which can be used in a wide range of applications. This sensor has a miniaturized form factor of 0.6 x 1.2 x 0.48 mm^3, a high

measuring range of 0.5 to 1.3 bars and a fixed capacitance of 5.7pF. These specifications enable the use of this pressure sensor with the designed CDC in this thesis.

1.3 Contribution of this thesis

This thesis is part of a project whose long-term goal is to develop a passive RFID-enabled sensor which can be used in implantable applications. Such a sensor will have two parts: the analog core and the digital core. The analog core is responsible to provide the required voltage levels from rectification of the incoming RF input and to convert the analog signals from the passive sensor to its digital equivalent which will be sent back to the reader. The digital core is responsible to decode the incoming signal, execute commands and transmit data back to the reader. In this thesis we have developed an analog core to be implemented with a passive capacitive sensor powered by inductive RF coupling. The designed has been sent for fabrication through MOSIS and a chip test bed has been created.

1.4 Plan of work

A detailed background study on various analog front-end components such as the RF rectifier, low-drop-out regulator, voltage references, current generators, power-on-reset circuit and the ADC will be discussed in chapter 2. Chapter 3 will present the design of the implemented CDC and all the other front-end analog components along with all the theoretical calculation involved. Results will be discussed in Chapter 4. Chapter 5 will provide conclusion and future work of this thesis.

CHAPTER 2

BACKGROUND

2.1 Introduction

This chapter focuses on the underlying principles used in the implementation of system design. Section 2.2 gives an in-detail description of the operating principles involved in an inductively coupled passive RFID system. Section 2.3 describes different type of sensors based on different classifications and an in-detail description of the E1.3N capacitance absolute sensor implemented in this thesis. Section 2.4 gives the conclusion of this chapter.

2.2 Inductive coupling

The analog core designed in this thesis proposal is an integral part of a wirelessly powered passive RFID transponder. The passive RFID transponder comprises of an inductively coupled antenna for communication/power generation and an electronic data-carrying/data-processing chip. Inductively coupled passive transponders derive all the energy needed for the operation of the chip from a RFID reader.

2.2.1 Magnetic field strength

Inductive coupling uses two inductor coils placed relatively close to each other as seen in Fig 2.1 [15]. The reader's antenna coil generates a strong, high frequency magnetic field which penetrates the cross-section of the coil area and the area around the coil. A small part of the emitted field pattern penetrates the coil of the transponder which is placed at some

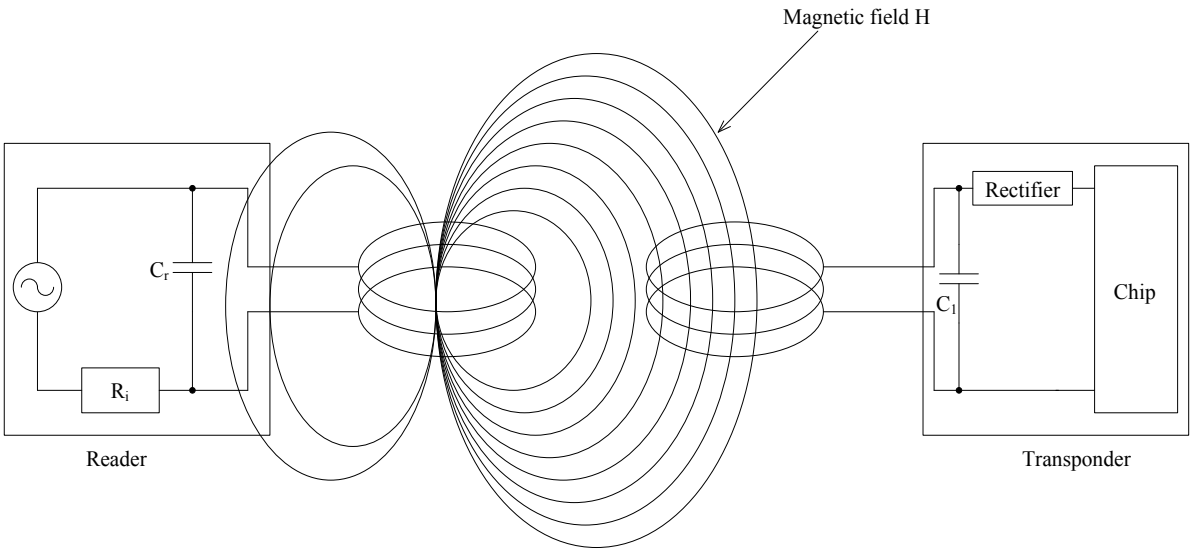
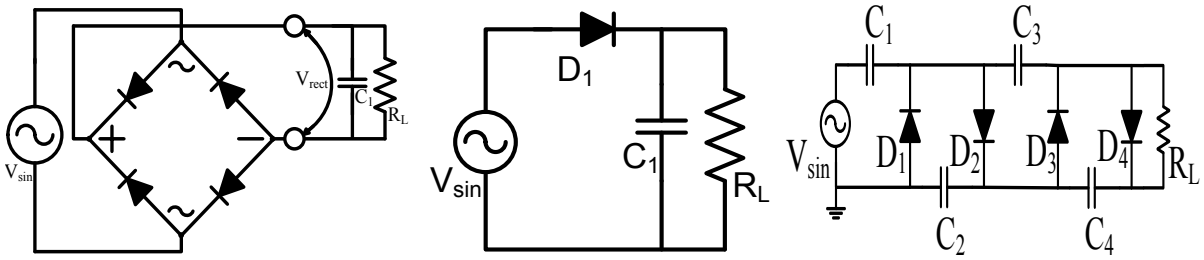


Fig 2.1. A generic power supply setup for an inductively coupled passive transponder

distance from the reader coil. A voltage V_i is generated at the transponder's coil which is then rectified to serve as a voltage source for the electronic chip. The capacitor C_r is connected in parallel with the reader's antenna coil. The value of C_r is selected such that it works with the coil-inductance of the antenna to form a parallel resonant circuit. This circuit will have a resonance frequency that corresponds to the transmission frequency of the reader. This resonance set-up creates very high currents at the antenna coil which can be used to set required field strengths for the operation of a remote transponder. The capacitor C_1 along with the antenna coil of the transponder forms another resonant circuit tuned to the transmission frequency of the reader. A voltage V_i is generated at the transponder coil which reaches its maximum due to the resonant circuit setup in both the reader and the transponder. An alternating voltage produced at the transponder antenna, in most practical cases where RF signals are used. This alternating voltage is rectified before it is supplied as a voltage source

to the chip. Different types of rectifiers are used in practice depending on the type of application. Fig 2.2 shows different types of rectifiers in use. Fig 2.2 (a) shows the full wave diode bridge rectifier. This has a higher efficiency over the half wave rectifier shown in Fig 2.2 (b). The full wave rectifier converts the alternating current (AC) to a direct current (DC)



(a) (b) (c)

Fig 2.2. Different types of rectifiers used, (a) full wave diode bridge rectifier, (b) half wave rectifier, (c) voltage multiplying rectifier

in both its positive and negative phase, thus providing a constant voltage at V_{rect}. The capacitor C_1 is used as a smoothing capacitor to reduce the ripple after rectification. Whereas, the half wave rectifier converts the AC into its corresponding DC only in the positive cycle, thus reducing the rectifier's efficiency. Fig 2.2 (c) shows a voltage multiplier circuit (Villard cascade voltage multiplier), which converts AC electrical of low voltage to a higher DC voltage by means of capacitors and diodes. The voltage multiplier is capable of producing very high voltages by increasing the number of cascade diode-capacitor combination. Due to their use in large voltage bearing applications, capacitors with high charge bearing capacity and diodes capable of withstanding large break down voltages are used.

The magnetic field strength H depicted by the magnetic flux lines is associated with the flow of current I [15] which is given by:

$$\sum I = \oint \vec{H}.\overrightarrow{ds} \tag{1}$$

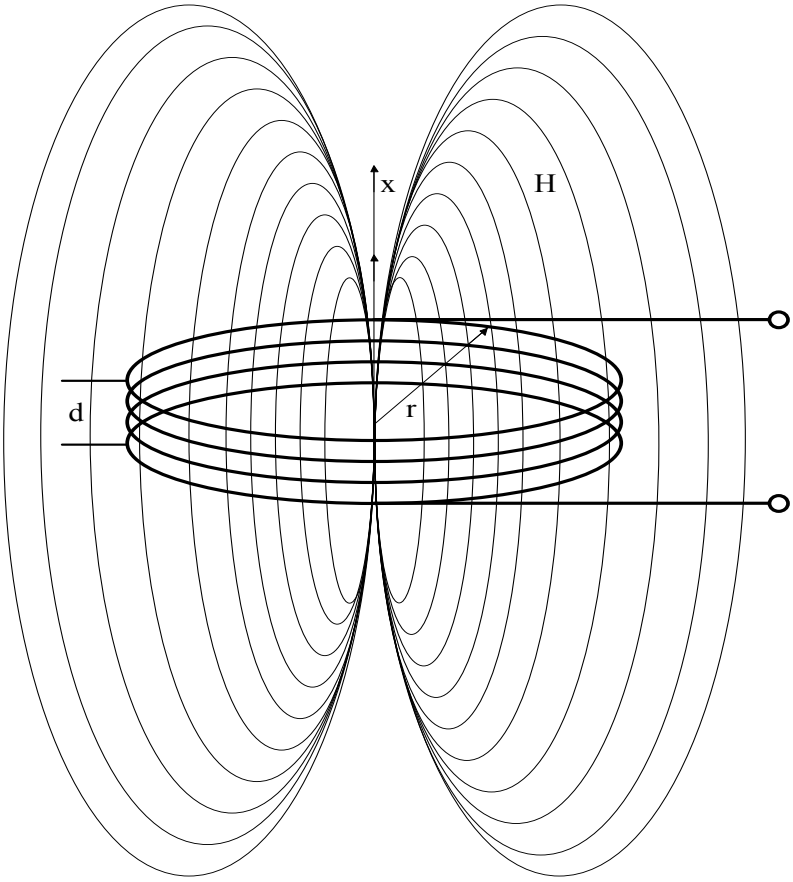


Fig 2.3. Magnetic flux around a short cylindrical coil

The magnetic field strength H for a short cylindrical coil antenna shown in Fig 2.3 similar to the type used in the antennas of inductively coupled RFID systems [15] is given as:

$$H = \frac{I.N.r^2}{2\sqrt{(r^2+x^2)^3}} \tag{2}$$

where N is the number of windings of the coil, r is the radius of the coil and x is the distance from the center of the coil in the x direction.

From equation (2) we can conclude that if the magnetic flux measuring point moves away from the center of the coil along the coil's axis (x axis), then the magnetic field strength H will decrease as the distance x is increase. The boundary conditions which apply to this equation are: d << r and x < λ/2π. So, at a distance x = 0 from the center of the antenna, equation (2) can be simplified as:

$$H = \frac{I.N}{2r} \tag{3}$$

For a rectangular conductor loop with edge length *a* x *b* at a distance *x* is given by the following expression [17]:

$$H = \frac{N\ .I\ .a.b}{4\pi\sqrt{\left(\frac{a}{2}\right)^2+\left(\frac{b}{2}\right)^2+x^2}}.\left(\frac{1}{\left(\frac{a}{2}\right)^2+\ x^2}+\frac{1}{\left(\frac{b}{2}\right)^2+\ x^2}\right) \tag{4}$$

2.2.2 Magnetic flux and magnetic flux density

The total number of lines of magnetic flux that pass through the inside of the cylindrical coil, in this case, is denoted by magnetic flux Φ. The magnetic flux Φ is expressed as [15]:

$$\Phi = B\ .\ A \tag{5}$$

where, B is the magnetic flux density and A is the effective area of the coil. The magnetic flux density is related to the magnetic field strength by the following equation [15]:

$$B = \mu_0\ .\ \mu_r\ .\ H \tag{6}$$

where, μ_0 is the magnetic field constant which describes the permeability of vacuum and μ_r is the relative permeability of the dielectric.

A cylindrical conduction loop is made up of N number of loops of the same area A and conducts the same amount of current I, each loop contributes same proportion of magnetic flux Φ to a total flux Ψ given by [15]:

$$\Psi = \sum_N \Phi_N = N \,.\, \Phi = N \,.\, \mu_0 \,.\, \mu_r \,.\, H \,.\, A \tag{7}$$

2.2.3 Self-inductance and mutual inductance

The ratio of total flux Ψ that is generated in an area enclosed by current I, to the current in the conductor enclosing it is denoted by inductance L. Inductance L can be expressed as [19]:

$$L = \frac{\Psi}{I} = \frac{N \,.\, \Phi}{I} = \frac{N \,.\, \mu_0 \,.\, \mu_r \,.\, H \,.\, A}{I} \tag{8}$$

The coupling of two circuits via a magnetic field is defined by mutual inductance M. Mutual inductance M as seen in Fig 2.4. [15] is formed by the coupling of partial magnetic field between the two inductance coil. Fig 2.4 shows two coils 1 and 2 of area A_1 and A_2 respectively. The coil 1 is driven by current I_1 which generates a magnetic flux of $\Phi(I_1)$ having a total flux of $\Psi(I_1)$. This flux is partially induced in the coil 2 producing a flux density of $B_2(I_1)$ and a total induced flux $\Psi_2(I_1)$. The magnitude of the coupling flux Ψ_{21} depends upon the geometry of the conductor loops, the relative position of both the coils and

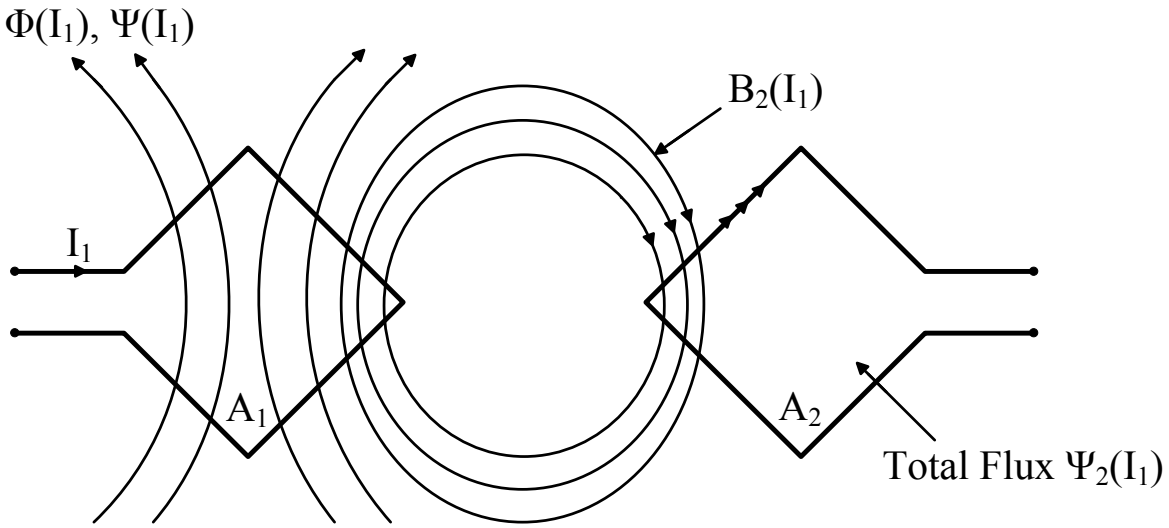


Fig 2.4. Mutual Inductance M_{21} demonstrated by partial coupling of magnetic flow

the permittivity of the medium between the two coils. This partially induced flux demonstrates mutual inductance M_{21} which is read as the inductance induced in coil 2 due to the inductance of coil 1. The principle of mutual inductance is responsible for the working of most inductively coupled passive RFID systems.

Similarly, a mutual inductance M_{12} can also be defined as a setup in which current I_1 flows through coil 2, thereby determining the flux Ψ_{12} in loop 1. In this setup, the following relationship applies [15]:

$$M = M_{12} = M_{21} \tag{9}$$

The mutual inductance M_{12} is expressed as [15]:

$$M_{21} = \frac{\Psi_{21}(I_1)}{I_1} = \oint_0^{A_2} \frac{B_2(I_1)}{I_1} \, . dA_2 \tag{10}$$

Considering the case of uniform magnetic field strength H along the x axis the mutual inductance M_{21} between the two coils can be calculated using equation (10) and expressed as [15]:

$$M_{21} = \frac{B_2(I_1).N_2.A_2}{I_1} = \frac{\mu_0.H(I_1).N_2.A_2}{I_1} \quad (11)$$

Replacing $H(I_1)$ from equation (2) and assuming the coils are circular in form with area πr^2, equation (11) is written as :

$$M_{12} = \frac{\mu_0.N_1.r_1^2.N_2.r_2^2.\pi}{2\sqrt{(r_1^2+x^2)^3}} \quad (12)$$

A few boundary conditions must be satisfied for expression (12): the area $A_2 <= A_1$ should be maintained and the x axis of both the coils should be placed on the same plane.

2.2.4 Coupling coefficient and Faraday's law

The coupling coefficient k is a qualitative determination of the flux coupling of two conductor loops. An expression for K for conductor loops independent of their geometric dimensions is [15]:

$$k = \frac{M}{\sqrt{L_1.L_2}} \quad (13)$$

where, M is the mutual inductance of the coil, L1 and L2 are the self-inductances of coil 1 and 2 respectively. The coupling coefficient k varies between two extreme cases 0<= k <= 1. In cases where k = 0, means that there is no magnetic coupling mainly caused due to great distances between the coils or due to magnetic shielding. In cases where k = 1, means that 100% magnetic coupling caused due to complete flux induction with the coils placed in the same plane.

The coupling coefficient k varies according to the distance x between the two coils. An expression for a circular coil antenna can be given as [15]:

$$k(x) \approx \frac{r_{transp}^2 . r_{reader}^2}{\sqrt{r_{transp} . r_{reader}} . (x^2 + r_{reader}^2)^3} \quad (14)$$

In equation (14) r_{transp} and r_{reader} denote the radius of the transponder and reader respectively and x denotes the distance between the reader and transponder. From this expression it is inferred that k(x) can be 1 i.e. 100% magnetic coupling is only possible if the distance between the two loops x is 0 and the antenna radius of both the reader and the transponder are equal. In this case both the conductor loops are in the same plane and are exposed to the same magnetic flux Ψ. In practical application the coupling coefficient as be as low as 0.01 [15].

The above discussion demonstrated the induction of magnetic flux to the transponder coil. The following discussion will demonstrate the formation of electric field at the transponder coil and hence the generation of voltage.

According to Faraday's law, any change to magnetic flux Φ generates an electric field strength E_i. The contour integral of the electric field strength along the surface of the conductor generates a voltage V_i which can be generally expressed as [15]:

$$V_i = \oint E_i \, . \, ds = -\frac{N . d\Phi(t)}{dt} \quad (15)$$

An effective analysis on the voltage created on the transponder coil can be made with an electrical equivalent of the circuit involving the inductor coils shown in Fig 2.5. Inductors L_1 and L_2 represent circular coil 1 and 2 of Fig 2.4. Both the coils are placed close to each other

on the same plane. Resistance R_2 is the coil resistance of the transponder antenna. The current consumption of the chip in Fig. 2.1 is symbolized by the load resistor R_L.

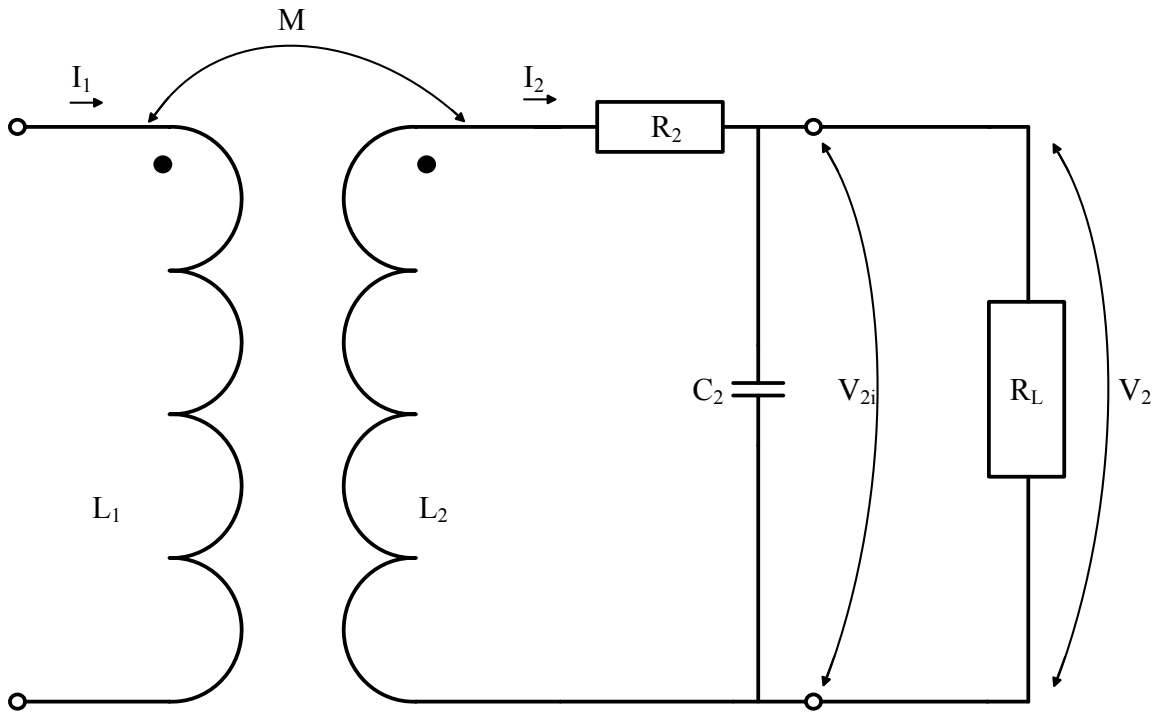


Fig 2.5. Equivalent circuit for a magnetically coupled conductor loops

A time varying flux in the inductor loop L_1 induces a voltage V_{2i} in the inductor loop L_2 due to mutual inductance M. The flow of current I_2 creates additional voltage drop across the coil resistance R_2 creating voltage V_{2i}. The current through L_2 also generates a magnetic flux, which opposes the magnetic flux $\Psi_1(I_1)$. Capacitor C_2 is the tuning capacitor used to raise the coil voltage. Since, in most practical purposes I_1 and I_2 are sinusoidal alternating currents a complex representation of the voltage generated at the load resistor is obtained.

The solution to the real part of the complex equation leads to a final answer with respect to the known parameters of the system [9]:

$$V_2 = \frac{\omega k \sqrt{L_1 L_2}\, I_1}{\sqrt{\left(\frac{\omega L_2}{R_L} + \omega R_2 C_2\right)^2 + \left(1 - \omega^2 L_2 C_2 + \frac{R_2}{R_L}\right)^2}} \quad (16)$$

where, $\omega = 2\pi f$. The frequency of the RF signal is represented by f. Based on this equation system specifications can be chosen.

2.3 Capacitive pressure sensor

In this section different type sensor, their classification and their usage is discussed. We will focus on the capacitive type pressure sensor in particular. Also, as detailed explanation of the E1.3N capacitive pressure sensor will be provided.

2.3.1 Sensors

As briefly described in chapter 1, sensors are devices which are capable of converting a sensed physical quantity into a signal that can be interpreted to meaningful information by a reader or an instrument. Sensors have a wide variety of applications which include automobile, machines, aerospace, medicine, manufacturing and robotics, etc. Sensors are often used in applications to measure very small changes in the physical quantity which require high sensitivity. Many types of sensor form factor are available ranging from large to microscopic sensors. Large sensors often have an impact on what they measure for instance the temperature measurement of a glass of hot water using a mercury thermometer. In this case heat transfer takes place between the hot water and the mercury thermometer. This causes the measured temperature to be lower than the actual temperature of the hot water. Although the magnitude of difference between the actual temperature and measured

temperature is not very large, high precision applications demand near-accurate measurement. This necessitates the design of sensors which have minimum effect on the measured quantity. Reducing the form factor of sensors often suffice this requirement and also has many other advantages. Recent advancements have enabled micro-sensors manufacturing in a microscopic scale using the micro-electro-mechanical systems (MEMS) technology.

2.3.2 Pressure sensors

Many different types of sensors are developed for specific applications. A few types of sensors are: chemical sensor, automotive sensor, electric current/potential sensor, flow sensor and pressure sensor, etc. For the application of sensors in this thesis, a pressure sensor is chosen. A pressure senor typically measures pressure of liquids or gases. A pressure sensor usually acts as a transducer which generates an electrical signal as a function of the imposed pressure. Pressure sensors vary drastically with changes in manufacturing process, technology, performance requirements, design factor and application suitability. Pressure sensors are classified in terms of pressure range, temperature of operation and type of pressure the sensor measures. Based on type of pressure measured, pressure sensors are divided into five categories [16]: gauge pressure sensor, vacuum pressure sensor, differential pressure sensor, sealed pressure sensor and absolute pressure sensor. Gauge pressure sensors are used in applications which need calibration to measure pressure relative to atmospheric pressure at a given location. A good example of this type is a tire pressure gauge which reads 0 PSI when it is actually 14.7 PSI (atmospheric pressure) in the tire. Vacuum pressure sensors are used to measure pressure less than the atmospheric pressure, also known as a

measurement of negative gauge pressure. Differential pressure sensors are used to measure the difference between two or more pressures induced as input to the sensing unit. A good example of this type of sensor is a level detector sensor installed in a pressurized vessel. Sealed pressure sensors are similar to gauge pressure sensors expect that it has a fixed pre-calibration to measure pressure relative to pressure at sea-level. The final type of pressure measurement sensor is the absolute pressure sensor which measures relative pressure to perfect vacuum (0 PSI) [17]. These sensors are commonly used to measure changes in barometric pressure or altimeters.

Based on pressure sensing technology, force collector type analog pressure sensors are widely used to measure strain due to applied force over an area. Absolute pressure sensors which are fabricated using Si MEMS are usually either piezo-resistance type or capacitance type. Capacitive pressure sensors are advantageous in many for many applications like biomedical sensing, automotive sensing, control system applications, etc. This is because of their relatively high sensitivity, better hysteresis and repeatability characteristics, low-temperature dependence and low-power consumption compared to piezoresistive pressure sensors [17]. The structure of a capacitive pressure sensor comprises a cavity Si Layer which forms the vacuum cavity, a Si diaphragm used with the upper electrode which also provides the capacitance change, and a glass substrate used to form the lower electrode and provide the air gap [17].

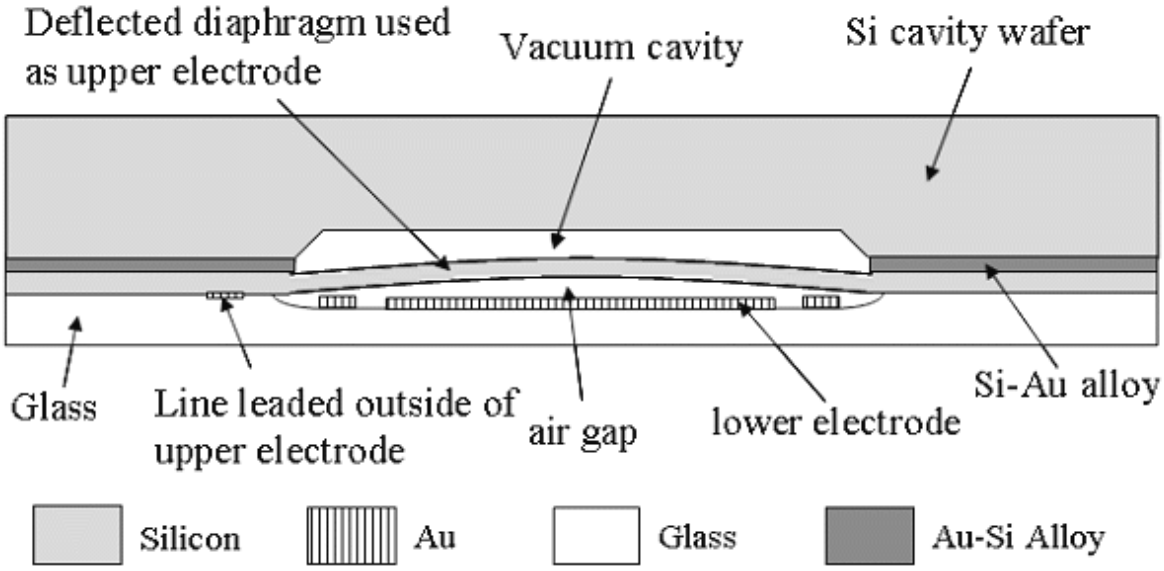


Fig 2.6 Capacitive absolute pressure sensor cross-sectional view

A good example of a capacitive absolute pressure sensor was presented by Lee. K. R., et al [17] in 2006. The cross-sectional view of the proposed sensor is depicted in Fig 2.6. In this we can verify the basic building blocks of the pressure sensor. Since this pressure sensor measures the applied pressure with reference to absolute vacuum, a sealed vacuum cavity is formed along the inner portion of the Si cavity wafer. This cavity is sealed using silicon diaphragm which is flexible. The diaphragm is also used as the upper electrode of the capacitor type pressure sensor. The bottom plate of the capacitive pressure sensor is formed by a fixed electrode located at the glass seal at the other end. Air pressure applied to the sensor forms an air gap between the two electrodes which causes the change in capacitance. Si-Au alloy is used to create the seal between the diaphragm and the Si cavity wafer. When no pressure is applied the diaphragm returns to a perfectly flat state. In this implementation an initial capacitance of 2.18pF at absolute vacuum was measured with the diaphragm

thickness of 20μm. A maximum deflection of 2.57pF in capacitance was measured with a pressure difference of 5hPa to 1000hPa.

2.3.3 Capacitive absolute pressure sensor E1.3N

The pressure sensor implemented in this thesis proposal is the microFAB capacitive pressure sensor E1.3N [14]. The E1.3N is a surface micro-machined capacitive absolute pressure sensor fabricated on non-conducting fused silica substrate. The selection of this pressure sensor was based on the fact that capacitive absolute pressure sensors are advantageous than their resistive counter parts as discussed previously. The main advantage of this pressure sensor is its miniature form factor of 0.6 x 1.2 x 0.48 mm^3, making it feasible to be used in implantable applications. The ultra-small size and low-power dissipation of this device is advantageous for biomedical applications involving wireless system design. The sensor exhibits a measuring pressure range of 0.5-1.3 bars. The maximum pressure limit for this sensor is measured at 9 bars with no physical damage. The limited sensing range allows the measurement of relatively smaller pressure quantities with higher accuracy. This feature enables its use in low pressure applications like intravascular/intraocular fluid pressure measurement, storage pressure chambers, etc. The physical design considerations of this sensor are also advantageous. The choice of non-conducting fuse silica eliminates all parasitic capacitances to the substrate. Remaining parasitic capacitance is controlled via a mask design. This maintains high accuracy in sensor design, fabrication and application. The sensor has large bond pads which allows chip mount by the use of conductive adhesive.

The enlarged view of the E1.3N pressure sensor is shown in fig 2.7. The sensor is designed as a surface micro-machined plate capacitor array with deformable pressure sensitive membranes on top of insulated counter electrodes. The capacitor array sense area is sensitive to pressure changes and consists of flexible membrane which deflects with increase

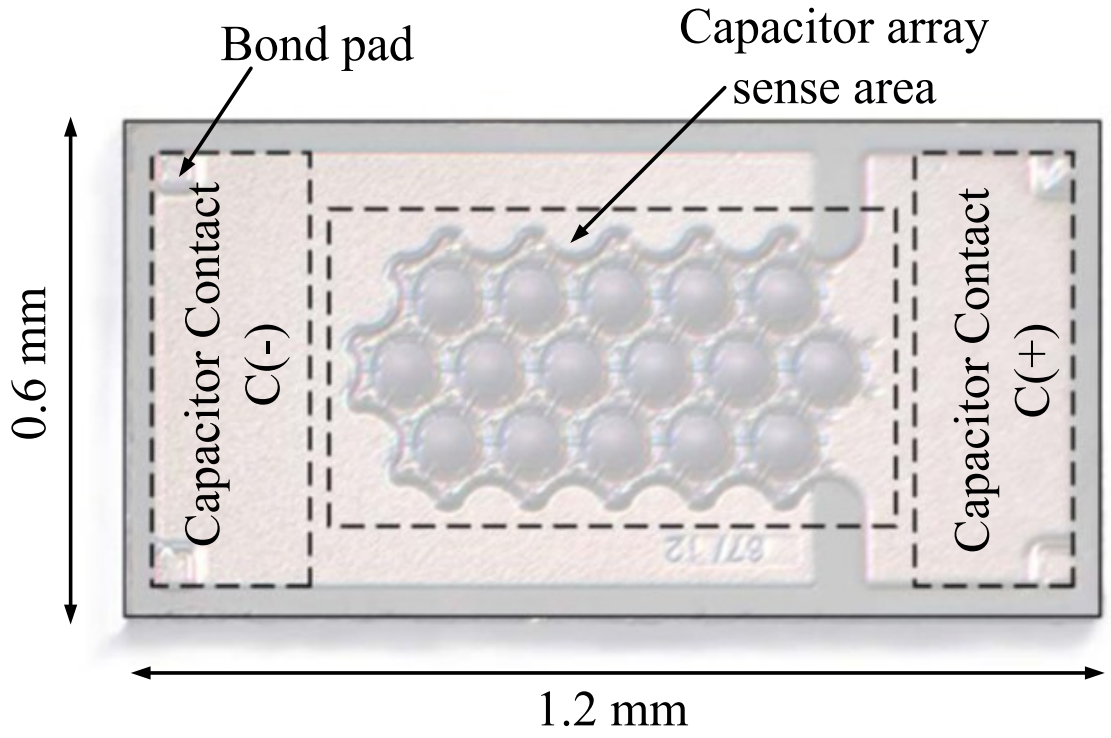


Fig 2.7 Enlarged view of E1.3N

pressure. The top flexible membrane has a dielectric insulation beneath which allows the sensor to operate in normal and touch-mode. In the normal mode of operation the flexible diaphragm deflects freely and does not touch the bottom electrode plate. This is when the applied pressure is below the measurable range of operation. When pressure increases the sensor enters the touch mode. The flexible membrane sinks down until it touches the bottom

electrode. This happens when maximum measurable pressure is applied. In case of a further increase in pressure the stress on the diaphragm does not increase significantly. This enables the high pressure bearing capacity of the sensor. The normal mode of operation is the preferred mode of operation for E1.3N which enables high accuracy and very small hysteresis. Applications which require relatively high pressure measurement can use sensors which have higher pressure bearing capacity at the expense of reduced accuracy.

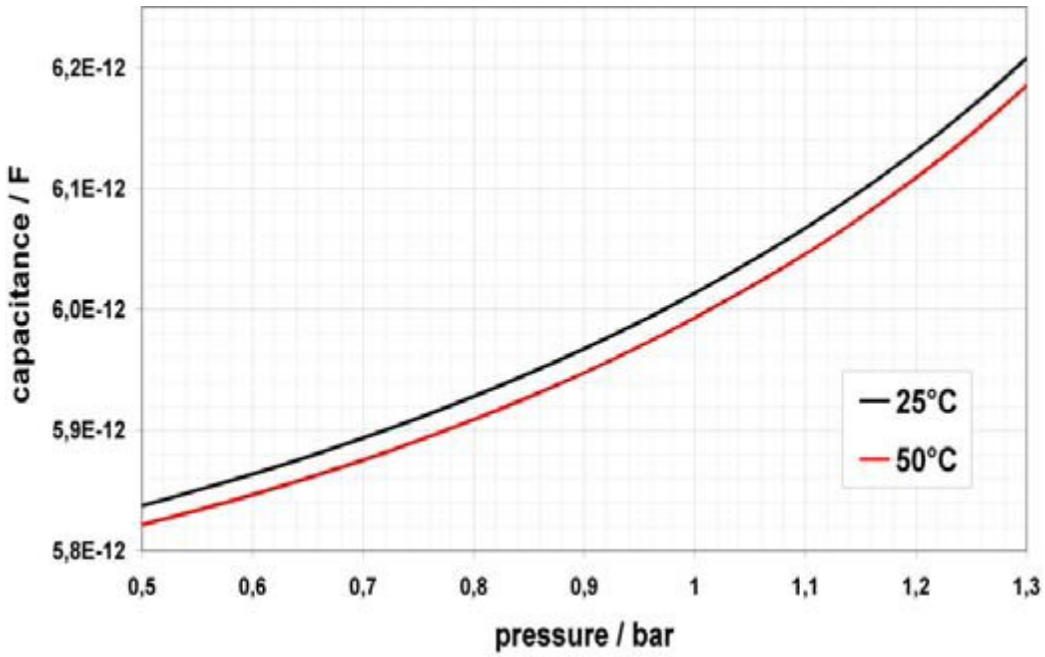


Fig 2.8 Capacitance vs. pressure plots

A sealed vacuum chamber created inside the sensor acts as a reference during measurement in a capacitive absolute pressure sensor. This vacuum chamber creates a fixed value of capacitance. The applied pressure on the sensor is determined as a variable capacitance over the fixed part. In the case of E1.3N the fixed capacitance is determined to be 5.734pF. The graph plot shown in fig 2.8 elaborates the capacitance vs. pressure plot

measured in different temperatures. The graph shown in fig 2.8, demonstrates the range of the variable capacitance component. 0.5 bars of atmospheric pressure correspond to approximately 5.8pF of total capacitance, which means a variable capacitance of 0.1pF. Similarly, 1.3 bars of applied pressure corresponds to 6.2pF of total capacitance, which means a variable capacitance of 0.5pF. Finally, it can be inferred that a pressure measurement of 0.5 bars - 1.3 bars corresponds to an analog equivalent of 0.1 pF – 0.5pF of capacitance. This capacitance is converted to its digital equivalent with the use of a capacitance to digital converter (CDC). The digital signal is suited better than the analog signal for its higher immunity to noise and to increase communications robustness of the RFID tag.

2.4 Conclusion

The electromagnetic field theory responsible for power generation in the transponder is discussed. A detailed description of sensors and its types have been discussed in the earlier section. The characteristics of the E1.3N capacitive sensor have been analyzed in detail. The following chapter will discuss the design factor of the analog core involving the design of the CDC and its supporting blocks.

CHAPTER 3

DESIGN

3.1 Introduction

This chapter focuses on design aspects of the transponder analog core. The construction of each analog block is explained in detail.

3.2 Design constraints

Implantable medical electronics are differentiated from most of the other electronic-system implementations by their unique combination of extreme low-power and high-reliability requirements [18]. Inductively coupled RF-powered systems are constrained on power due to the fact that electromagnetic field intensity decays exponentially with distance. These constraints place a burden on power management within the integrated circuits (ICs).

Many implantable systems widely utilize analog signal processing, due to the fact that digital signal processing consumes much higher power and area requirements [18]. Most of this design is done as subthreshold analog design to take advantage of low bias currents and high gain. The subthreshold regime offers the highest gain at a given current and maximum headroom due to low V_{gs} and V_{dsat}. However, many other analog applications, which are focused on speed and have moderate power requirements, are operated in strong inversion for this reason.

Various modifications can be implemented in the design of digital blocks for implantable low-power systems. At the system and IC level, this often includes turning off blocks and/ or clocks when they are not required to perform a task. Another IC level low-

power implementation technique is the lowering of supply voltage down to the sum of the p- and n-channel thresholds and selective duplication of functions, circuits, or tasks at the expense of area [18]. Minimization of total power dissipation in the clock network is crucial. Well-designed clock trees with layers of clock gating along with appropriate selection of asynchronous circuits greatly contributes to lower power consumption.

3.3 System Architecture

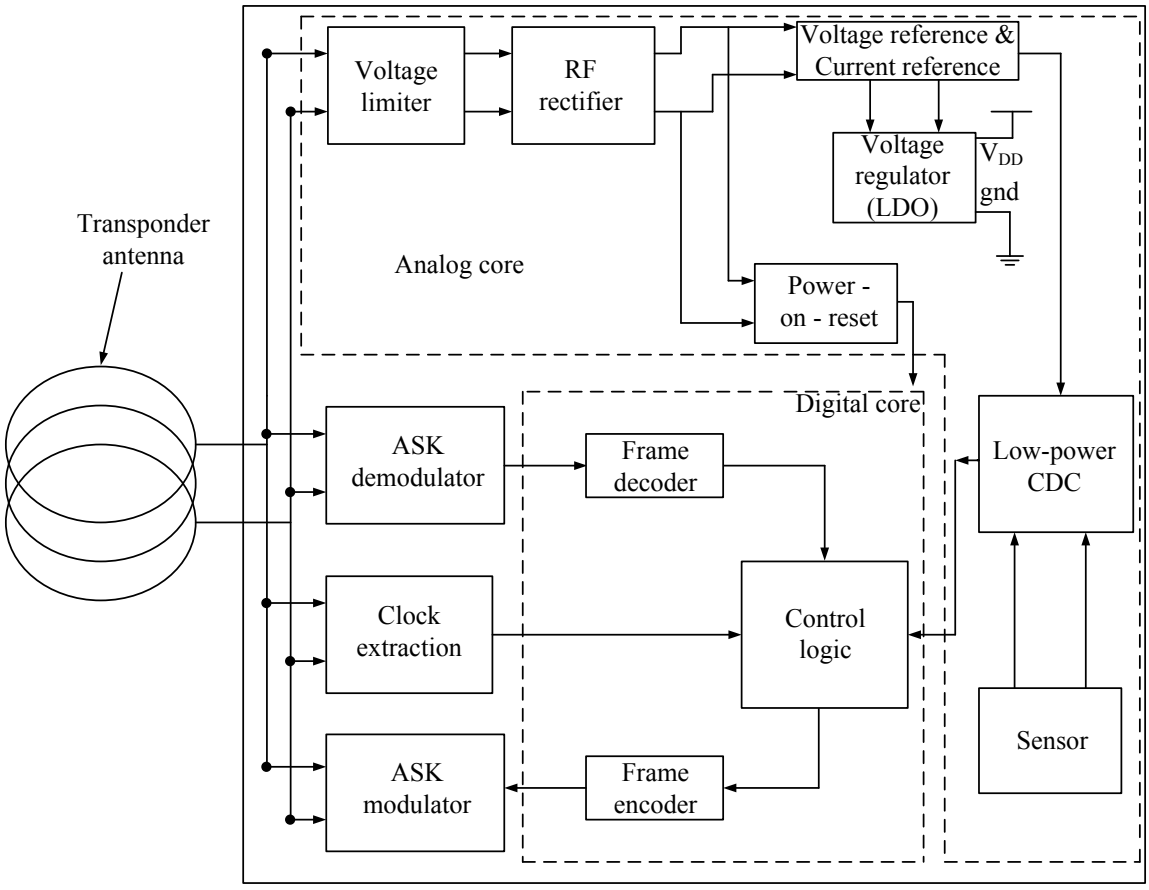


Fig 3.1a Transponder block diagram

The transponder system architecture is shown in Fig 3.1a. The system is divided into two fundamental building blocks, namely: the analog core and the digital core.

The analog core is responsible for system power generation and sensor signal demodulation. The extended view of the analog core is shown in Fig. 3.1b.

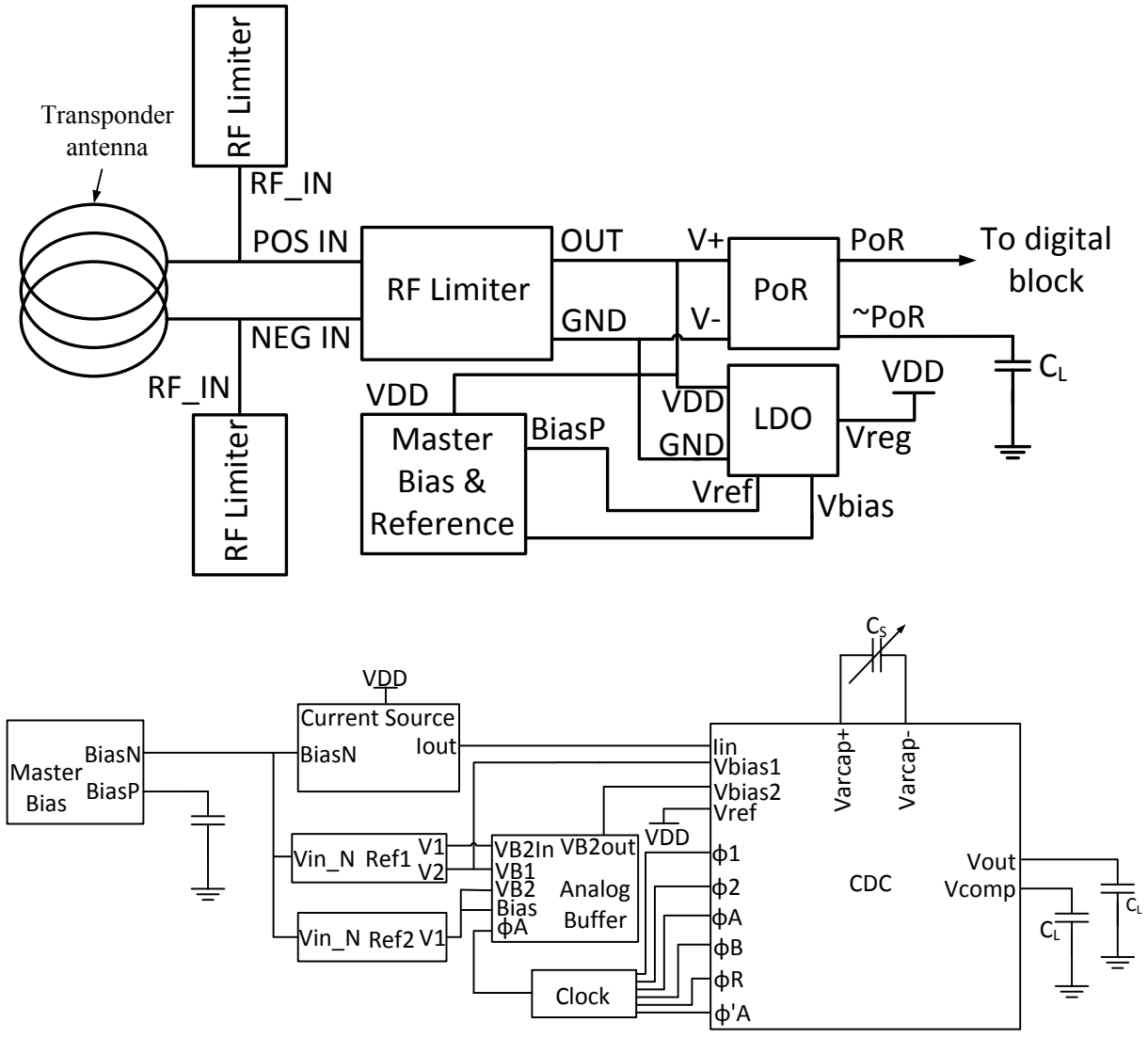


Fig 3.1b Analog block extended view

It comprises of number of sub-blocks. The transponder antenna is connected to the RF limiter. The RF limiter acts as a load to the antenna and prevents the internal components from any damage due to high voltage generated due to near field RF coupling. This is then

connected to the RF rectifier which provides a rectified voltage from the alternating RF signals received at the transponder antenna. The power-on-reset (POR) block generates a positive reset pulse which is applied to the digital core when the system turns on. The reset pulse ensures the digital core to return to its initial state before data processing. The RF limiter is further connected to a low-dropout (LDO) voltage regulator. This voltage regulator provides a precise and stable power supply. A stable power supply is essential for accurate reference voltages and appropriate functioning of both the analog and digital core. The corresponding block is responsible for the generation of different voltage and current references required by the CDC. The low-power CDC is connected to the sensor as its interface to digitize the real-world physical signals.

The digital core is responsible for transponder communication with a RFID reader. Transponder communication follows the ISO 15693 standard to extends its compatibility with commercially available RFID readers. The communication from the reader to the transponder uses an amplitude shift keying (ASK) modulation technique. The data coded ASK signal representing a request from the reader is first demodulated using the ASK demodulator. The data is then extracted from the ASK modulated signal and processed by the frame decoder to determine the request from the reader. Once the frame bits are identified they are further provided to the control logic. The control logic performs the instruction in the frame bits such as read from memory, write to memory, etc. The clock signal to the control logic is provided by a clock extractor circuit which generates the master clock signal required by the digital core from the RF signal from the reader.

In this thesis, the analog core has been designed and implemented. The following sections will described design parameters involved in the implantation of the analog core in detail.

3.4 Full-wave rectifier

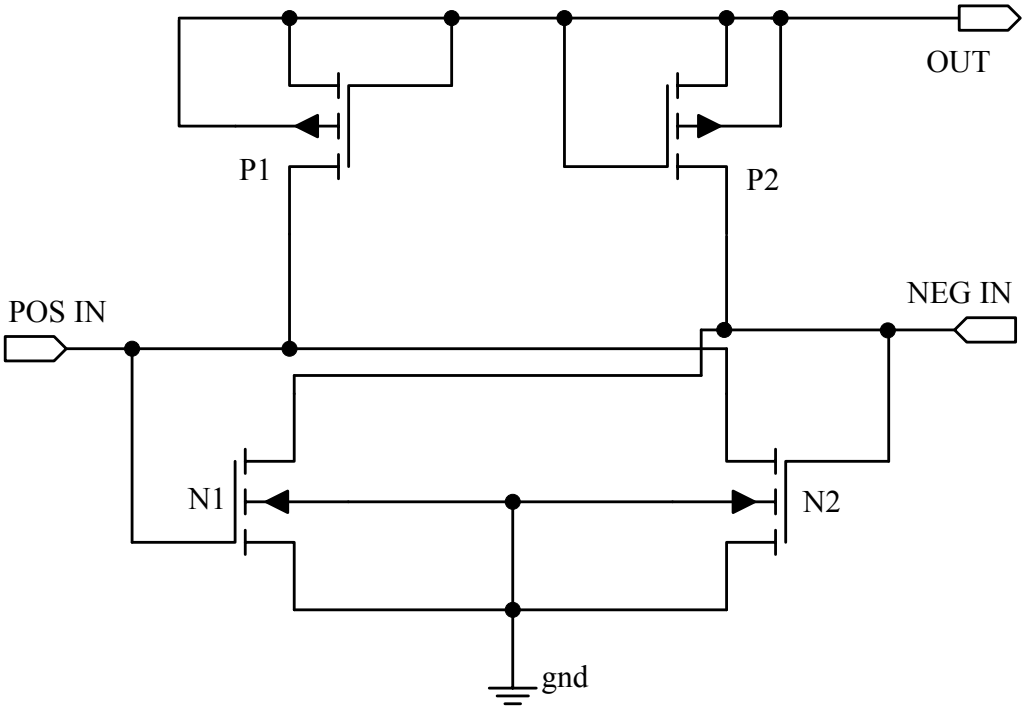


Fig 3.2 Full-wave rectifier schematic view

The full wave RF rectifier shown in Fig 3.2 is implemented in this design to provide the power supply for the entire system. The full-wave rectification is accomplished by using a CMOS equivalent of a quad-diode full-wave bridge rectifier configuration. The transistors P1 and P2 are connected in a basic diode configuration while N1 and N2 are connected in a switching configuration. This configuration achieves higher rectified voltages. The working of this circuit is as follows. When a positive going RF signal is applied to transistor N1, it

switches on making the negative going RF pulse applied to the gate of N2 to become zero. At this time the positive RF pulse appears at the drain of transistor P1. Transistor P1 is connected in a basic diode configuration which allows the voltage at the drain to appear at the source with voltage drop approximately equal to the threshold voltage of the PMOS. The same working continues in the negative cycle of the RF signal when N2 switches on and P2 acts as the diode. The transistor sizes are mentioned in Table 3.1. Large transistor sizes were selected to provide large output currents to drive the entire system.

Table 3.1 Full-wave rectifier transistor sizes

Transistor	W	L
P1	150 µm	600 nm
P2	150 µm	600 nm
N1	300 µm	600 nm
N2	300 µm	600 nm

The test circuit shown in Fig 3.3 shows the full-wave rectifier connected to a RF test signal. The RF test signal has a frequency of 13.56 MHz with amplitude of 20 V_{P-P} to simulate real world RF conditions. The RC network at the output of the rectifier operates as a filter to reduce AC ripples after rectification. The resistance of 10 KΩ simulates a load resistance to test its effect on the output voltage.

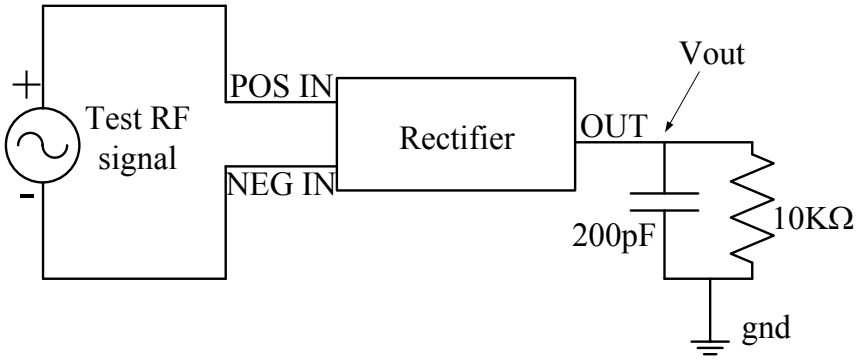


Fig 3.3 Full-wave rectifier test circuit

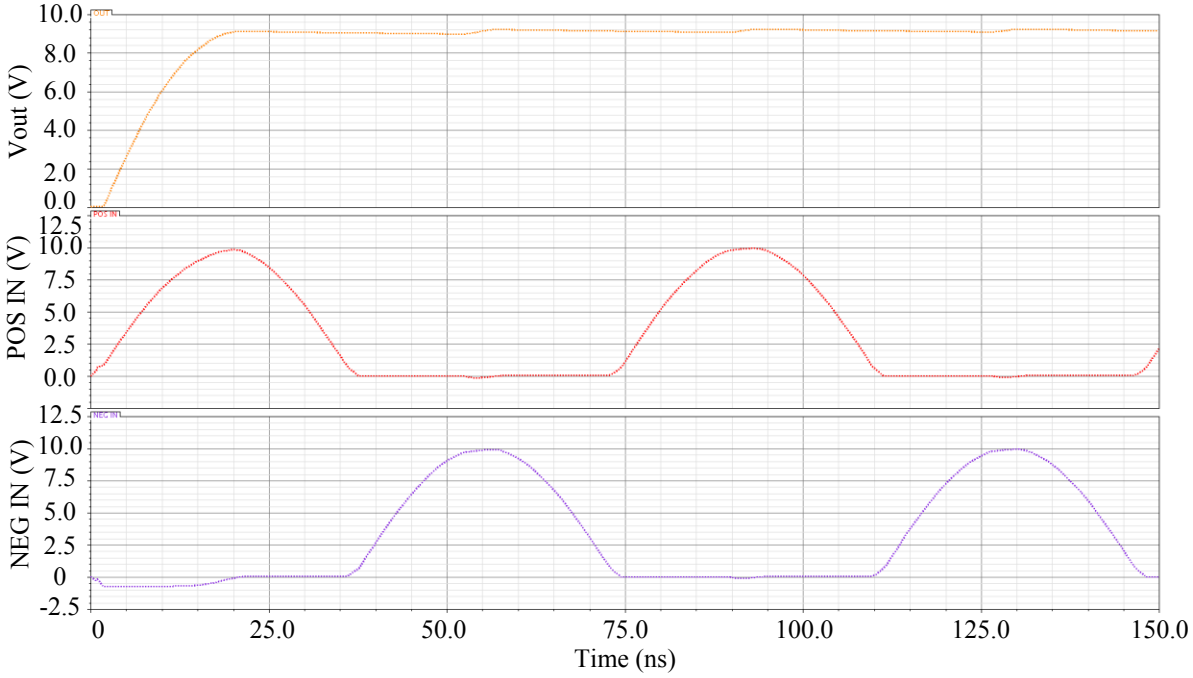


Fig 3.4 Full-wave rectified voltage simulation

Fig 3.4 shows the output voltage simulations of the test circuit. The voltage output was noted as 9.1 V for the given test signal. Fig 3.5 shows the output current at the rectifier. The output current was noted as 910 µA.

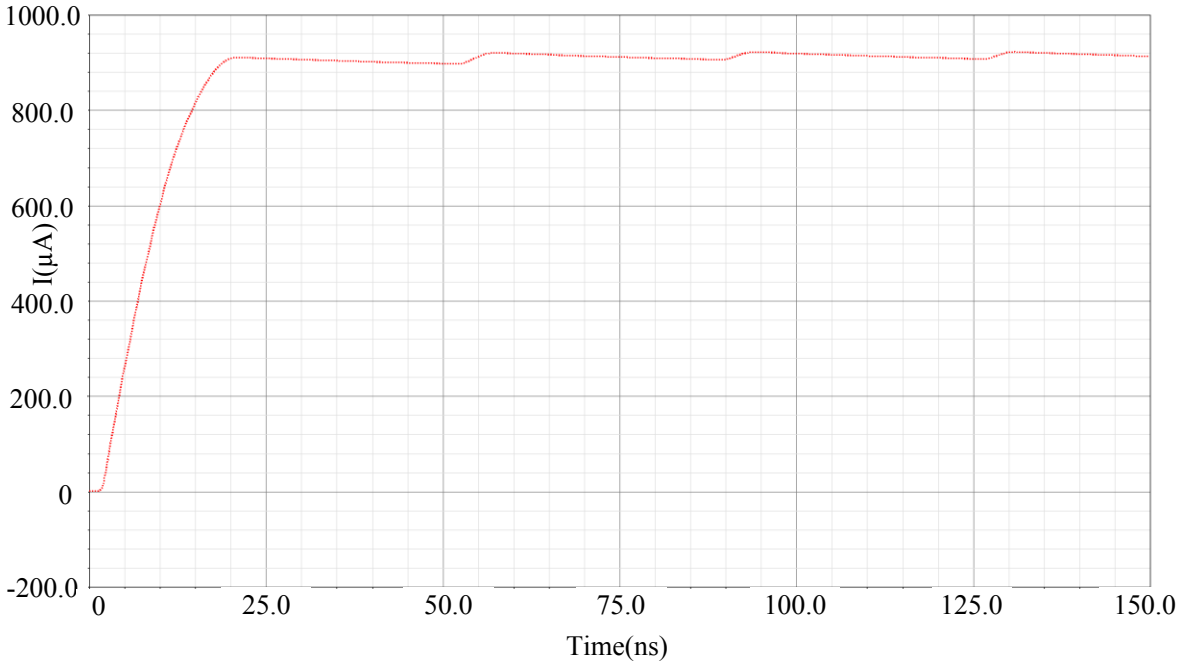


Fig 3.5 Full-wave rectified current simulation

3.5 RF voltage limiter

Near field RF signal coupling generates high voltages at the transponder coil. The RF voltage limiter protects the transponder system from damages caused to CMOS gate-oxide breakdown due to an excessive coupling voltage from the reader for a short operation distance. The RF voltage limiter circuit is shown in Fig 3.6. The RF signal is sensed by the RF_IN pin of the circuit which is a stacked diode voltage referenced to the ground of the chip. The stacked diode PMOS ladder is designed keeping in mind the following relationship:

$$V_{rect} = 7.V_{GS} + I_D.R1$$

Where

$$V_{GS} = |V_{THP}| + \sqrt{\frac{2.I_D}{\mu_p.\ C_{ox}.\ \frac{W}{L}}}$$

In the above equation the value inside the square root is minimized by using large transistor aspect ratios, also in-turn making I_D very small which makes the following relation possible:

$$V_{rect} \cong 7.|V_{THP}|$$

$$V_{rect} \cong 7 \times 0.82 \text{ V}$$

$$V_{rect} \cong 5.74 \text{ V}$$

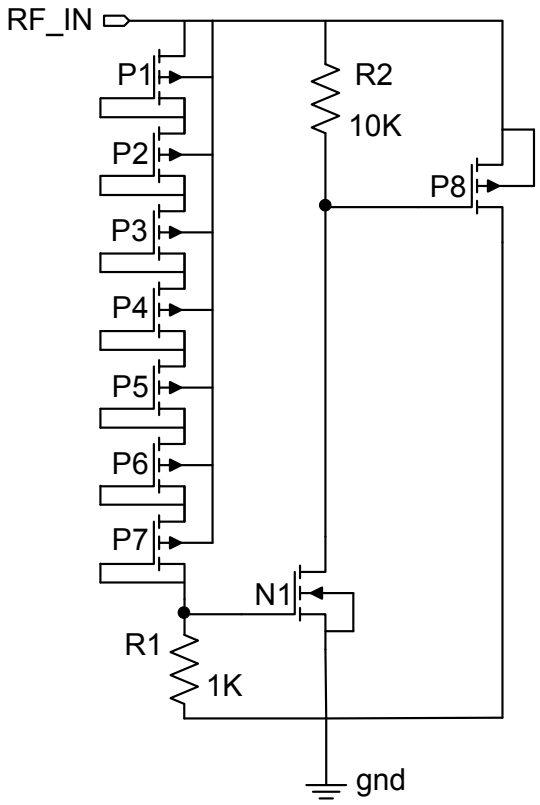


Fig 3.6 RF voltage limiter schematic

This means that when the RF signal goes above 5.74 V then the RF voltage limiter kicks in reducing the effective voltage. Above 5.74V the additional voltage appears at the gate of the NMOS N1. After a certain limit transistor N1 gradually switches on. Once N1 is completely switched on, the potential at the gate of PMOS P8 starts decreasing. To avoid the

RF signal to be limited completely, a resistor R2 is used to maintain a voltage drop across the RF signal and the drain of N1. As the voltage at the gate of P8 continues to drop as the result of N1 switching on, P8 starts turning on. At this time the transistor P8 acts a shunt and limits any applied RF signal from increasing largely. The RF voltage limiter acts as a load to the antenna to limit high amplitude RF signal. As seen in the test circuit in Fig 3.7 the RF_Limiter is connected to both the positive and negative input of the rectifier.

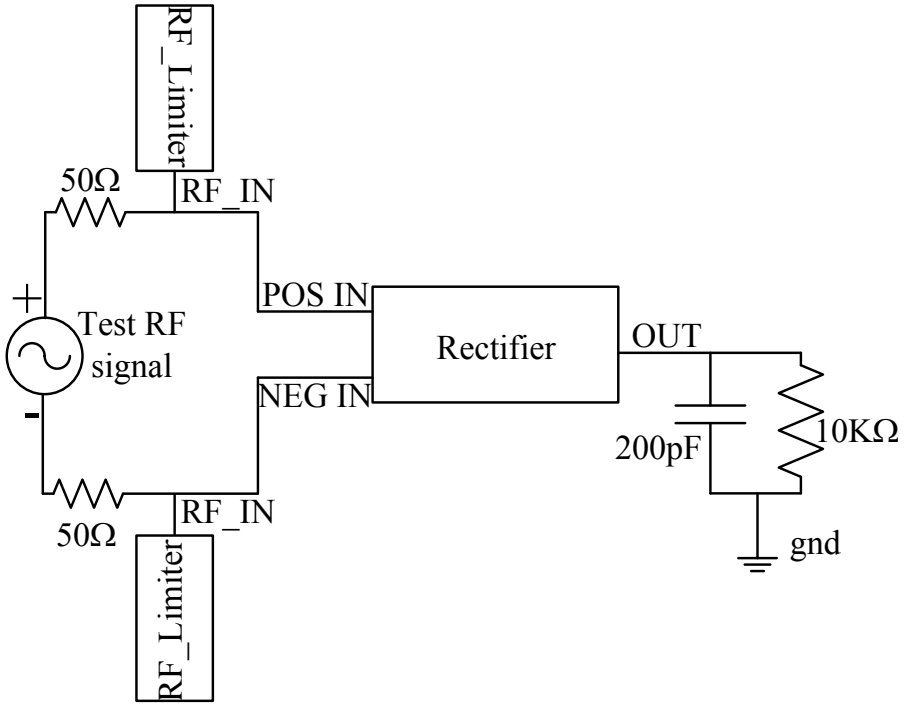


Fig 3.7 RF voltage limiter and rectifier test circuit

An off-chip L-match network transforms to 50 Ω; alternately, this matching network can be easily absorbed into the antenna as in commercial designs [12]. The applied test signal is a 13.56 MHz sine wave with amplitude of 60 V_{P-P}. Fig 3.8 shows the limited voltage at the

output of the RF limiter. The voltage has been limited to 17 V $_{p\text{-}p}$. Fig 3.9 shows the output voltage of the circuit. It can be seen that the applied RF signal is now reduced to 13 V, which is below the CMOS gate-oxide breakdown voltage. Fig 3.10 shows the output current after the test circuit and was measured at 1.25 mA. Table 3.2 shows the aspect ratio of the transistors used in the RF voltage limiter. It can be noted that the aspect ratio of the transistors used in the stacked diode ladder are considerably large at 100 µm/0.6 µm. The remaining transistors are also large taking into consideration the large amount of voltage to be regulated.

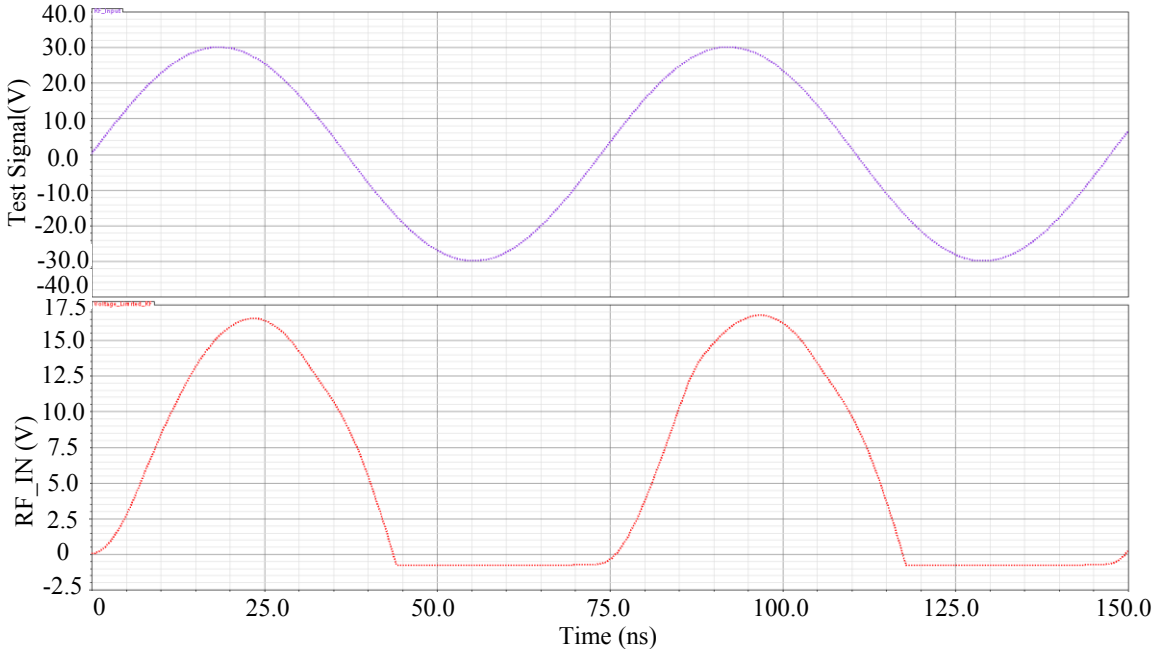


Fig 3.8 RF voltage limiter output voltage

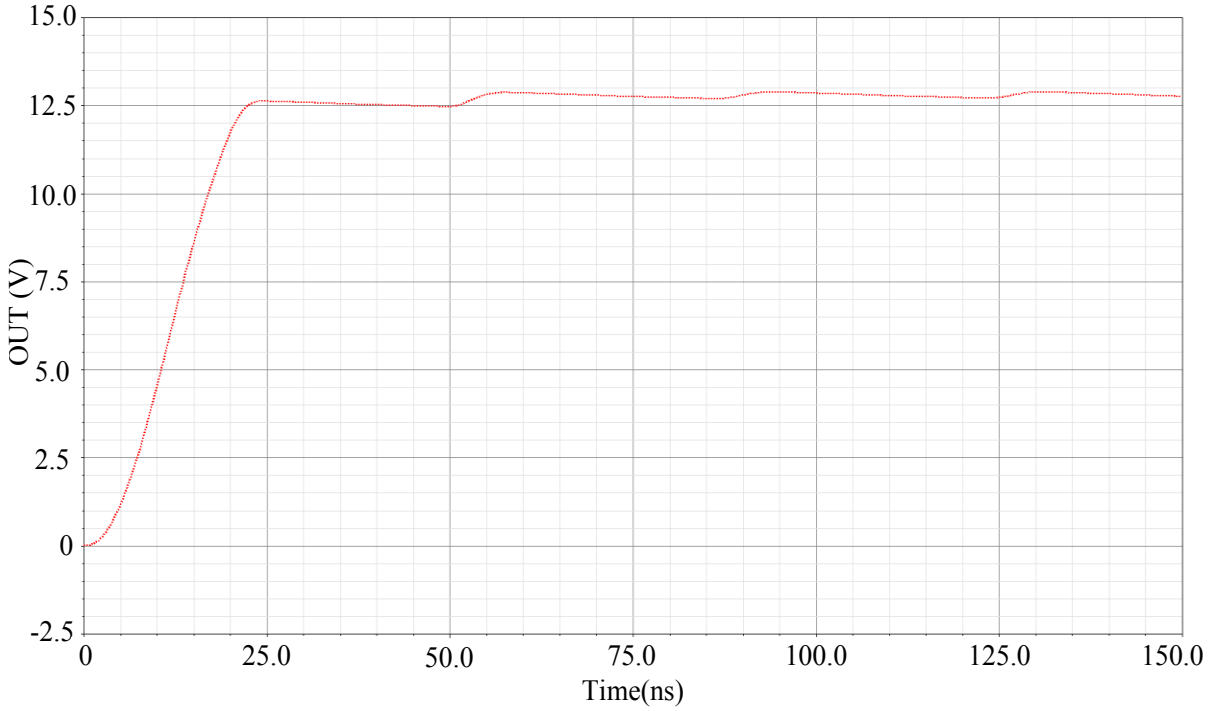


Fig 3.9 RF voltage limiter and rectifier output voltage

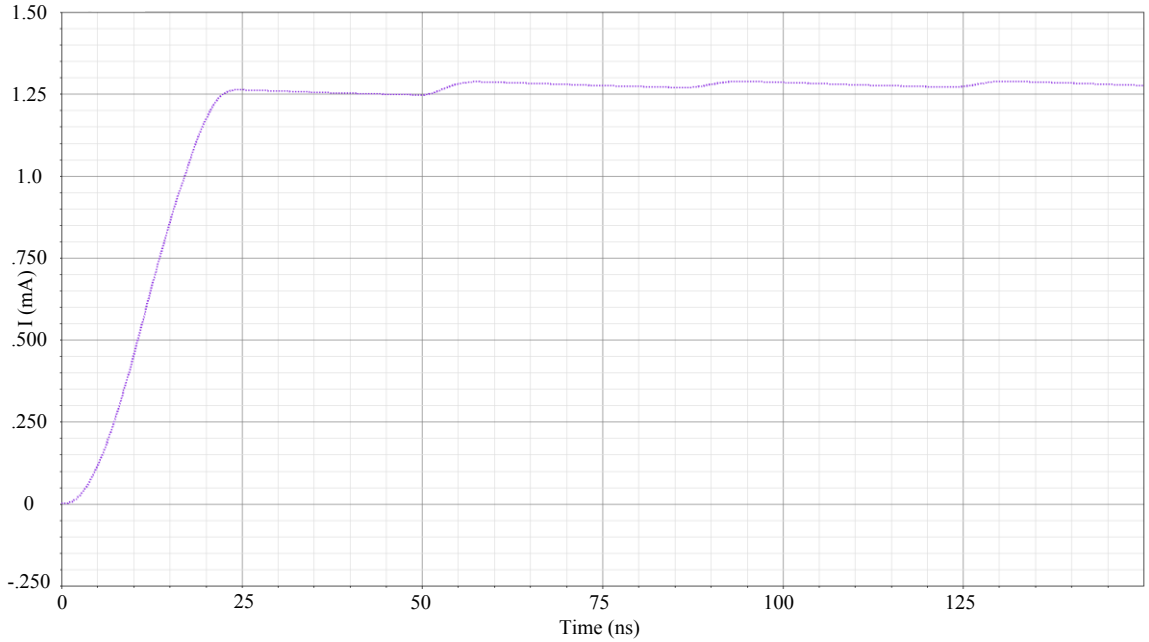


Fig 3.10 RF voltage limiter and rectifier output current

Table 3.2 RF voltage limiter transistor sizes

Transistor	W	L
P1	100 µm	600 nm
P2	100 µm	600 nm
P3	100 µm	600 nm
P4	100 µm	600 nm
P5	100 µm	600 nm
P6	100 µm	600 nm
P7	100 µm	600 nm
P8	150 µm	600 nm
N1	100 µm	600 nm

3.6 Power-on-reset

The purpose of the power-on-reset circuit is to provide a reset signal to the digital core when the transponder receives sufficient RF power for operation. This reset signal is instrumental in setting all the digital components to its initial state. Only after the reset signal is applied, the digital core can properly starts its operation. The design of the power-on-reset

involves a non-stable system which comprises two branches containing transistor P2-N1 and P3-N2 (see Fig 3.11) [20]. When the circuit powers up, either of these branches switches on and the other branch switches off. The OR gate compares the two signals insuring a power-on-reset for the logic blocks.

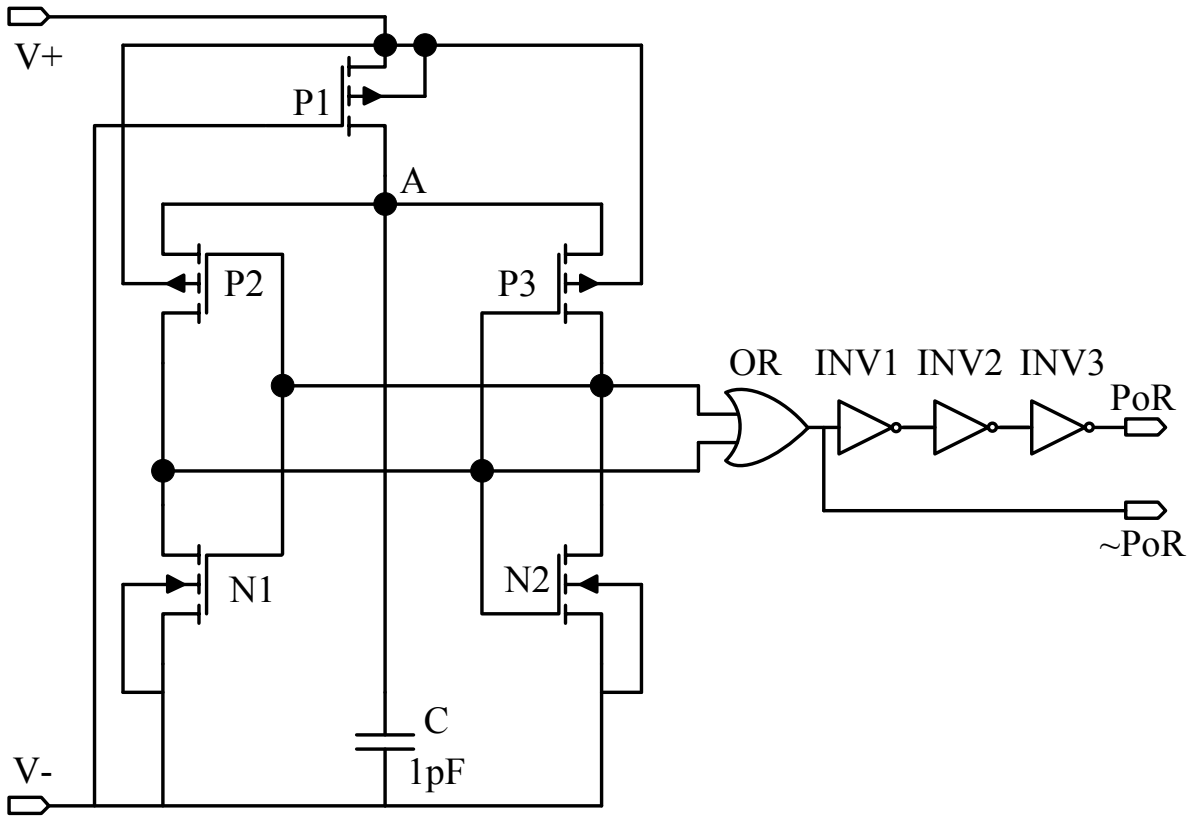


Fig 3.11 Power-on-reset schematic

The gate of transistor P1 is connected to the ground at the output of the rectifier. Transistor P1 switches on. The transistor P1 is chosen to be longer in size to limit the amount of current supplied to the capacitor C. The capacitor C allows a slow charging of node A to force a delay between the rise of the voltage supply and the power-on-reset. A large capacitor

also damps the circuit to avoid parasitic oscillations. The long P1 transistor insures slow charging of the capacitor. An array of inverters are stacked at the end of the OR gate to provide a strong reset pulse at the end. The three inverters are arranged in ascending order according to their sizes. The second inverter is thrice the size of the first one and so on. The transistor sizes of the power-on-reset circuit in given in Table 3.3.

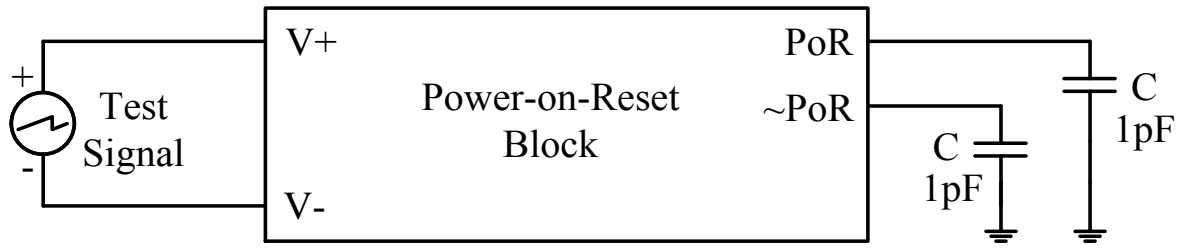


Fig 3.12 Power-on-reset test circuit

The test circuit of the power-on-reset block is shown in Fig 3.12. The test signal is an incremental ramp which stabilized for a certain period of time and then decreases. The output waveform can be noted from Fig 3.13. The reset signal is activated from 0.7V to 3V of the input waveform. The V_{DD} applied to the OR gate and the inverters is the same as that of the input waveform, so the shape of the output waveform. This is done to eliminate the need of the LDO voltage regulator to provide a stable supply voltage.

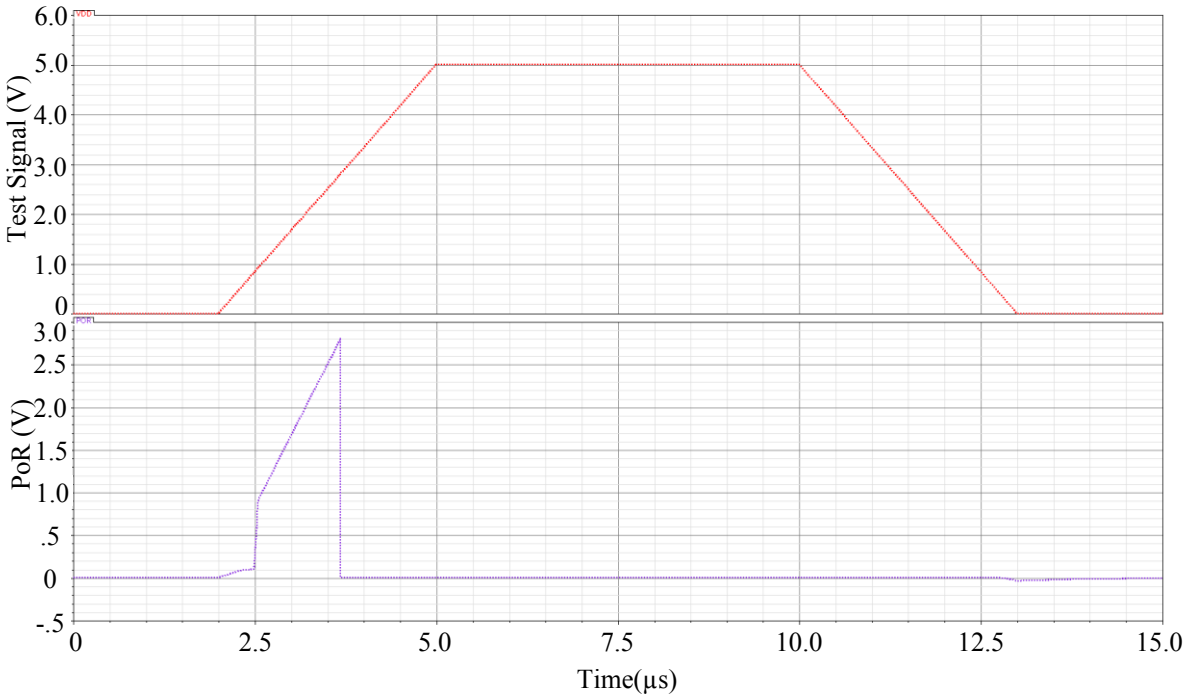


Fig 3.13 Power-on-reset test circuit waveform

Table 3.3 Power-on-reset transistor sizes

Transistor	W	L
P1	1.5 µm	8 µm
P2	4.8 µm	8 µm
P3	4.8 µm	8 µm
N1	4.8 µm	8 µm
N2	4.8 µm	8 µm

3.7 Low-drop-out (LDO) voltage regulator

The low-drop-out voltage regulator is used to provide a stable supply voltage to the entire system, including the analog and the digital core. Fig 3.14 [19] shows the basic topology of the voltage regulator. A stable voltage reference V_{REF} is used with an amplifier to generate a regulated voltage, V_{REG} [21]. For an ideal case considering a finite open-loop gain A_{OL}, the generated regulated voltage is given by:

$$V_{REG} = A_{OL} \cdot (V_p - V_m)$$

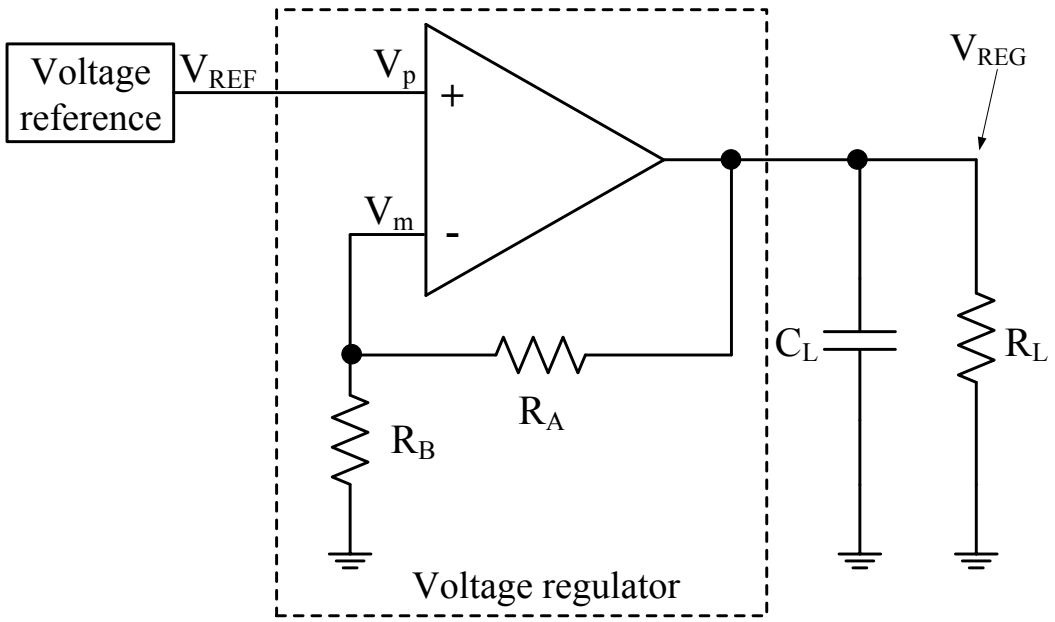


Fig 3.14 Schematic of a voltage regulator

The negative feedback makes the regulated voltage stable across process and temperature changes. Simplifying the above equation, $V_m = V_{REG} . \frac{R_B}{R_A + R_B}$ and $V_p = V_{REF}$.

Substituting these components, we can write:

$$V_{REG} = V_{REF} . \left(\frac{1}{\frac{1}{A_{OL}} + \frac{R_B}{R_A + R_B}} \right) \tag{3.1}$$

If we consider an infinite open-loop gain for an ideal case then the above expression can be written as:

$$V_{REG} = V_{REF} . \left(1 + \frac{R_A}{R_B}\right) \tag{3.2}$$

The schematic of the implemented LDO voltage regulator is shown in Fig. 3.15. An operational trans-conductance amplifier (OTA) which consists of a differential amplifier with current mirror loads is used in the LDO. When appropriate voltage levels are applied at the inputs of the differential stage in the OTA, current flows through both the branches of the differential pair. Since current mirror loads are used in the construction of the OTA, same amount of current is forced in each of them respectively. This sets the voltage level at the gate of transistor N5, since it is in current mirror configuration with N4, which in turn will be the same as the gate potential of transistor P1.

In saturation for P1: $V_{SD} \geq V_{SG} - |V_{THP}|$

Solving: $V_D < V_G - |V_{THP}|$

We get, $V_G > 2.2V$

From the above analysis the gate voltage of transistor N5 is also known. This turns on transistor N5 and the gate of pass transistor P5 is grounded which allows turning it on completely and is used to provide a significant amount of current to the load. A capacitor connected between the V_{REG} and ground acts as a bypass capacitor which is used to supply charge to the load for fast current transients and also reduces the required bandwidth of the regulator. A large C_L is used to filter the load's fast current transients. To isolate the load from the second-stage, transistor P5 later forms a common source amplifier with transistor N6. A large C_L makes the regulator more stable, slowing the response of the op-amp. The reduction of the speed of the op-amp is offset by the fact that a larger load capacitance can supply more charge to a fast current transient before the op-amp must respond. The compensation capacitance C_C is used for large signal purposes. A smaller value of C_C is used to avoid the poles associated with the output node to move to a higher frequency. If V_{REG} drops suddenly, the decrease in voltage is fed back directly to the gate of P5 through C_C. This turns P5 on quickly and allows it to pull V_{REG} back up bypassing the slower feedback of the op-amp. Large values of R1 and R2 were selected to minimize the flow of current to ground from the pass transistor. Using equation 3.6.2 and assuming infinite open-loop gain: $V_{REF} = 2$ V, $R_A = 200$ KΩ and $R_B = 400$ KΩ.

$$V_{REG} = 2 . \left(1 + \frac{200\ K\Omega}{400\ K\Omega}\right)$$

$$V_{REG} = 3\ V$$

Thus, the ideal regulated voltage is 3V to be supplied to the whole system. The transistor sizes are given in Table 3.4.

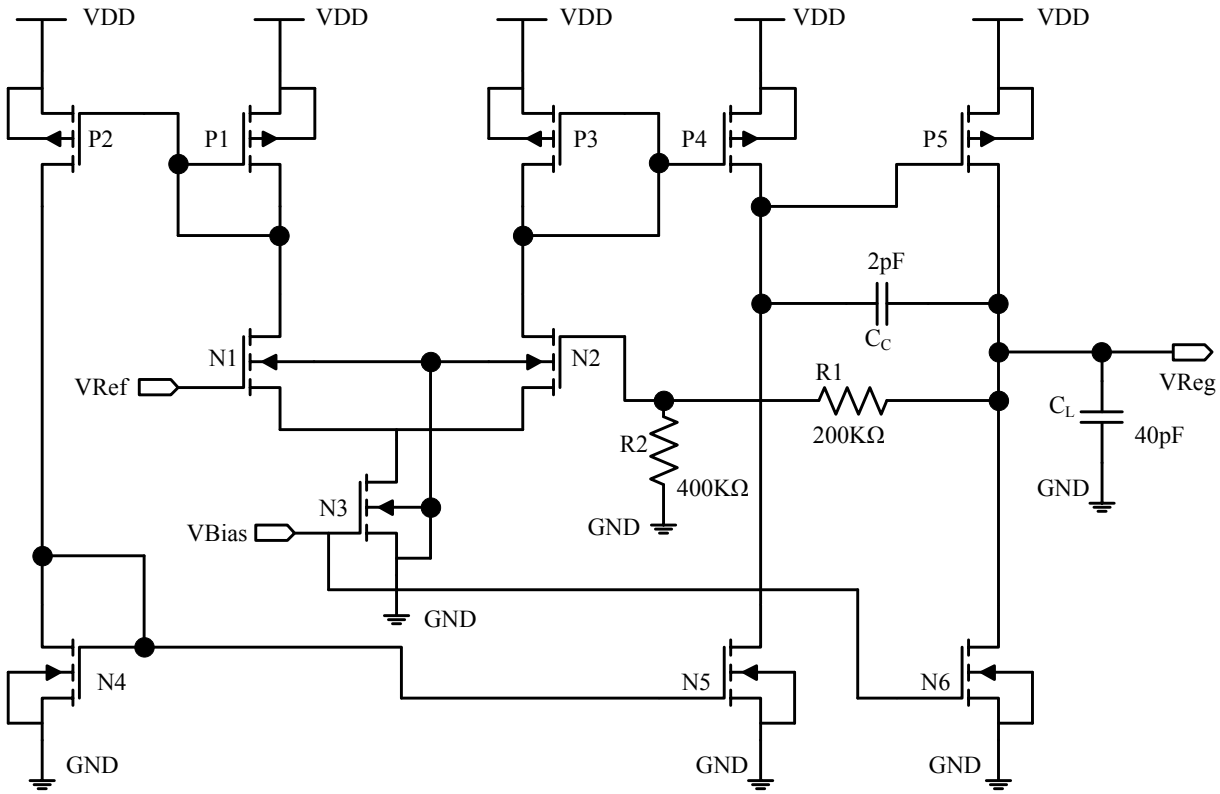


Fig 3.15 LDO voltage regulator schematic

Table 3.4 LDO Transistor sizes

Transistor	W	L
P1	60 µm	2 µm
P2	60 µm	2 µm

P3	60 µm	2 µm
P4	60 µm	2 µm
P5	800 µm	1.2 µm
N1	30 µm	2 µm
N2	30 µm	2 µm
N3	100 µm	2 µm
N4	10 µm	2 µm
N5	10 µm	2 µm
N6	10 µm	2 µm

Various test circuits are presented in the following pages to characterize the LDO completely. Fig 3.16 shows a circuit to test the line regulation. In this test circuit the supply voltage is applied in the form of a sine wave of 5 V offset with amplitude of $1V_{P-P}$. The frequency of the sine wave is 10 KHz. This test voltage has a 20% change in the line voltage. The regulated voltage will be measured at the end of the LDO. Fig 3.17 shows the simulated results of the line regulated voltage. The regulated voltage has a 0.1% change averaging at 3.026 V. This shows that the rate of change in the supply voltage is reduced in the regulated voltage. That means the LDO is successfully regulating the supply voltage.

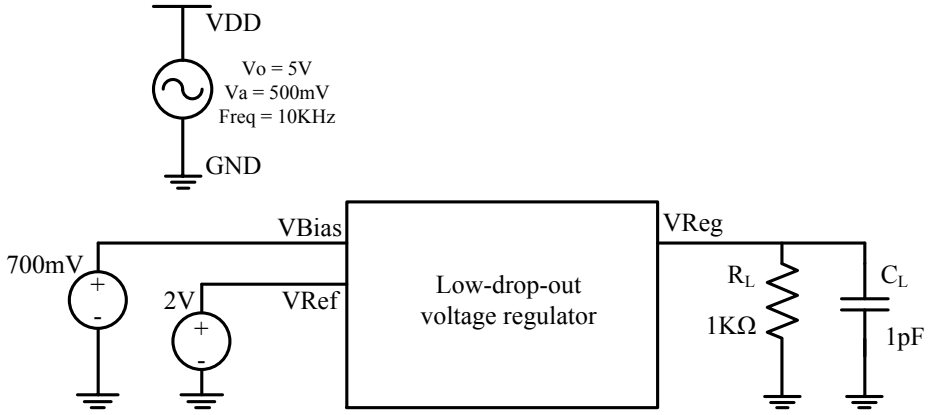


Fig 3.16 LDO voltage regulator line regulation test circuit

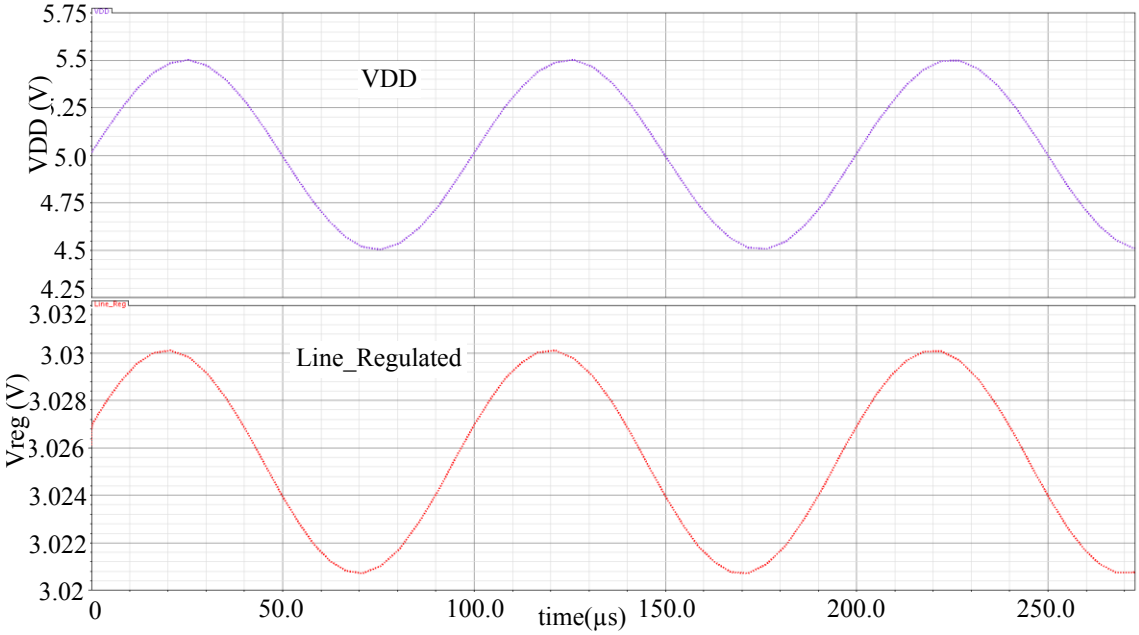


Fig 3.17 LDO voltage regulator line regulation waveform

The next test circuit shown in Fig. 3.18 is to characterize load regulation. In this test circuit, an alternating current is applied as a load to the LDO. The alternating load current is a sine wave of 10 KHz frequency, 500 µA of offset current with 20% variation of 100 µA. A stable supply of 4V is used in this test circuit. The simulated waveform of this test circuit is

shown in Fig. 3.19. It is observed from the simulation that a 20% change in load current generated a 0.0073% change in the regulated voltage averaging at 3.0193 V.

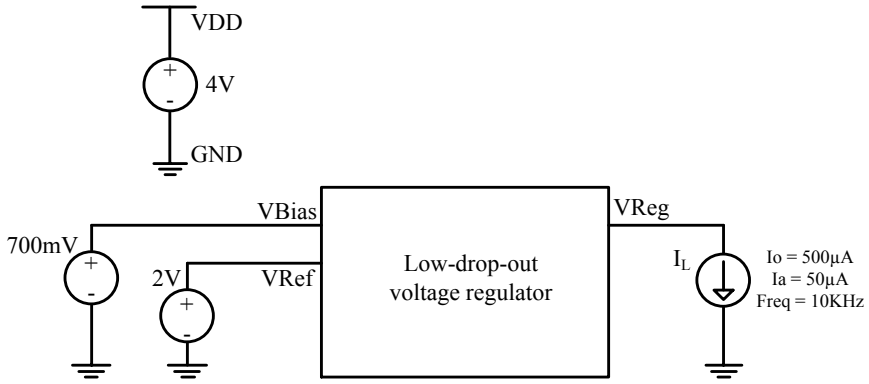


Fig 3.18 LDO voltage regulator load regulation test circuit

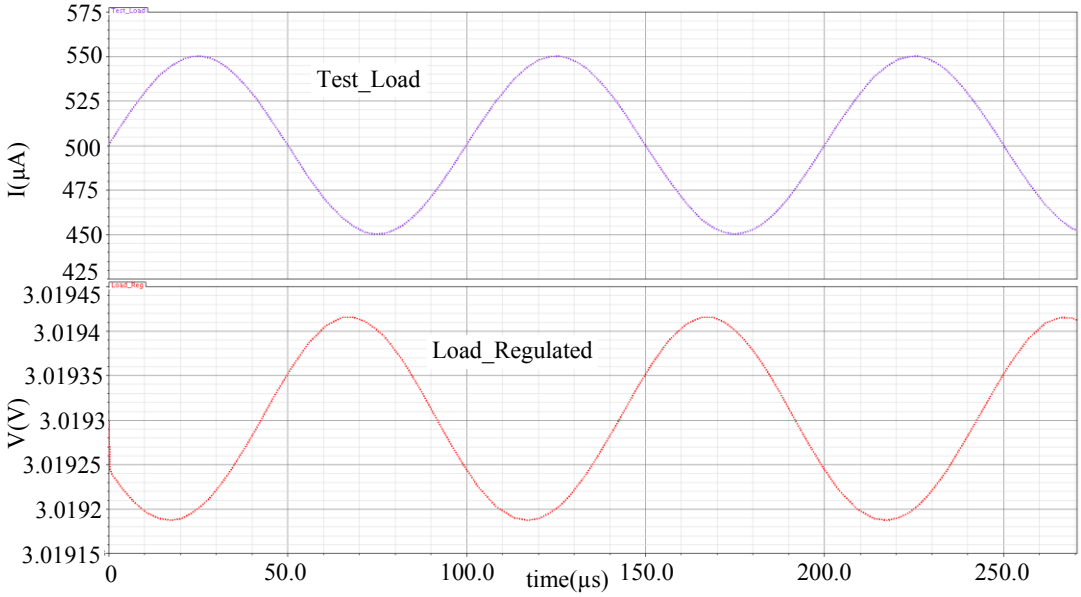


Fig 3.19 LDO voltage regulator load regulation waveform

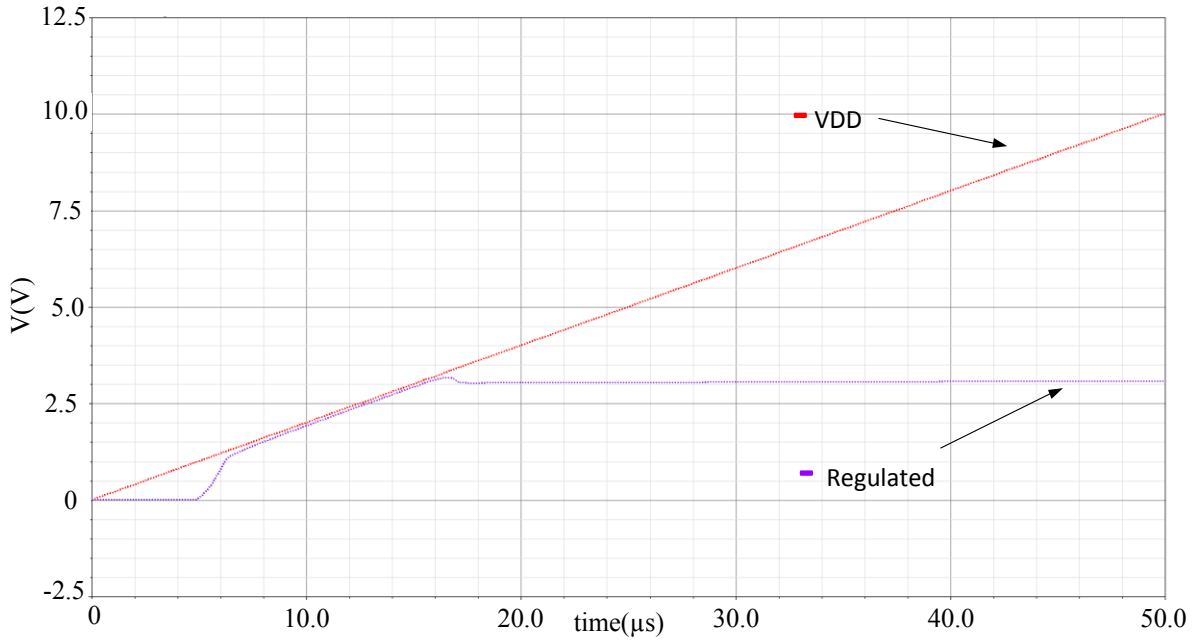


Fig 3.20 LDO voltage regulator ramp input test waveform

The main function of the LDO is to provide a stable output voltage even when the supply voltage is changing. To test this condition a ramp wave is applied as a supply voltage. A ramp wave of 0-10 V in a time period of 50 µs is applied as test supply voltage. Fig 3.20 shows the simulated waveform of the supply voltage and the regulated voltage. It can be clearly noted that the LDO starts regulating at 3.3 V of supply voltage proving a stable 3.05 V at the output. The regulation is stable even though the applied supply voltage is increasing continuously. Also the design has been tested to provide a stable regulated voltage even when greater than 20 mA of current appears at the load.

3.8 Master-Bias voltage reference

Voltage references are an integral part of analog and mixed signal systems like the one designed in this thesis. In most system design there are requirements of different voltage levels by different functional blocks in the system. A master-bias voltage reference generator provides a fixed voltage value which is then used to generate other required bias voltage levels.

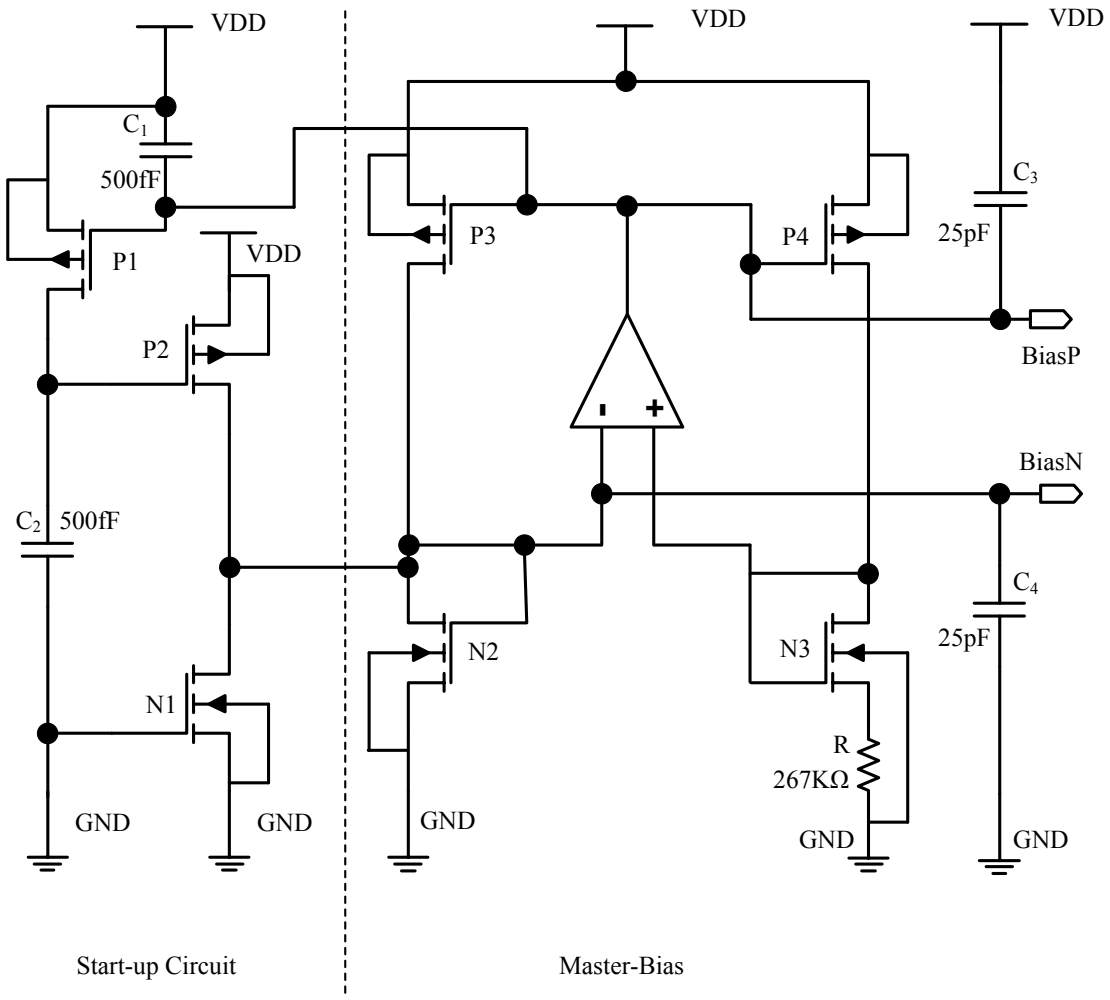


Fig 3.21 Master-bias voltage reference generator

The master-bias voltage reference generator is shown in Fig 3.21 [19]. This voltage reference consists of a start-up circuit and the master-bias circuit. At start-up, there is no current flowing through R. For this reason a startup circuit is used to provide the required current flow. At power-up C_2 is discharged and C_1 holds the source of P1at VDD keeping P1 off. When the circuit is switched on, current flows through transistor P2 and charges capacitor C_2. Once this capacitor is charged to VDD by P1, transistor P2 shuts off. C1 and C2 are selected to be large enough to be able to supply the master-bias loop with sufficient charge to operate. The gate of transistor N1 is tied to ground keeping it off. The gate can be connected to VDD to provide a reset to the master bias reference circuit. After the master-bias loop has enough charge in it, the startup circuit shuts down. During the operation of the reference circuit, no current flows in the startup circuit.

The master-bias voltage reference is a beta-multiplier biasing circuit [19] with the multiplying factor K = 4, because the size of N3 is four times the size of N2. To reduce the sensitivity of the voltage reference generator to changes in VDD the variations in the drain-to-source voltages of the NMOS devices are needed to be reduced. For this purpose a basic single stage op-amp is used. The amplifier is used to compare the drain voltage of the transistor N2 with the drain voltage of transistor N3 and regulate them to be equal. N3's output resistance increases due to this. When the gate voltage of N3 is above the gate voltage of N2, the amplifiers output voltage increases. This increases the gate voltage at P3 and P4, lowering the current it supplies and causing N3's gate to drop. The same happens with the current sourced by P3 which inturn decreases N2's gate voltage. Both the gate voltage drops are symmetrical because the gates of both P3 and P4 are tied together. The beta-multiplier is

an example of a positive feedback circuit. The addition of a resistor kills the open loop gain making it less than one which makes it stable. The size of the resistor cannot be too small or the system can become unstable. The resistor R is also used to set the current in the beta-multiplier given by the expression:

$$R = \sqrt{\frac{2}{I_{REF} \cdot \beta_{N2}} (1 - \frac{1}{\sqrt{K}})^2} \qquad (3.3)$$

where, I_{REF} is the current flowing through R, K is the beta factor, $\beta_{N2} = KP_{N2} \cdot \frac{W}{L}$

For a desired I_{REF} of 200 nA in each of the branches of the master-bias generator a resistor value of 267 KΩ was used. For a feedback amplifier with only single high-impedance node, to make it stable the gate of N3 is connected to its drain. This also reduces the gain around the loop. To make the reference even more stable capacitors C_3 and C_4 are added. The high-impedance node is a critical point to add the compensation capacitor. Without these capacitors an applied step voltage makes the currents to oscillate showing it to be unstable. The transistor sizes are shown in Table 3.5.

Table 3.5 Master-bias voltage regulator transistor sizes

Transistor	W	L
P1	6 µm	6 µm
P2	6 µm	6 µm
P3	100 µm	2 µm

P4	100 µm	2 µm
N1	6 µm	6 µm
N2	50 µm	2 µm
N3	200 µm	2 µm

The test circuit of the master voltage reference is shown in Fig 3.22. The simulations are shown in Fig 3.23. It should be noted that it takes about 500 µs to start the circuit.

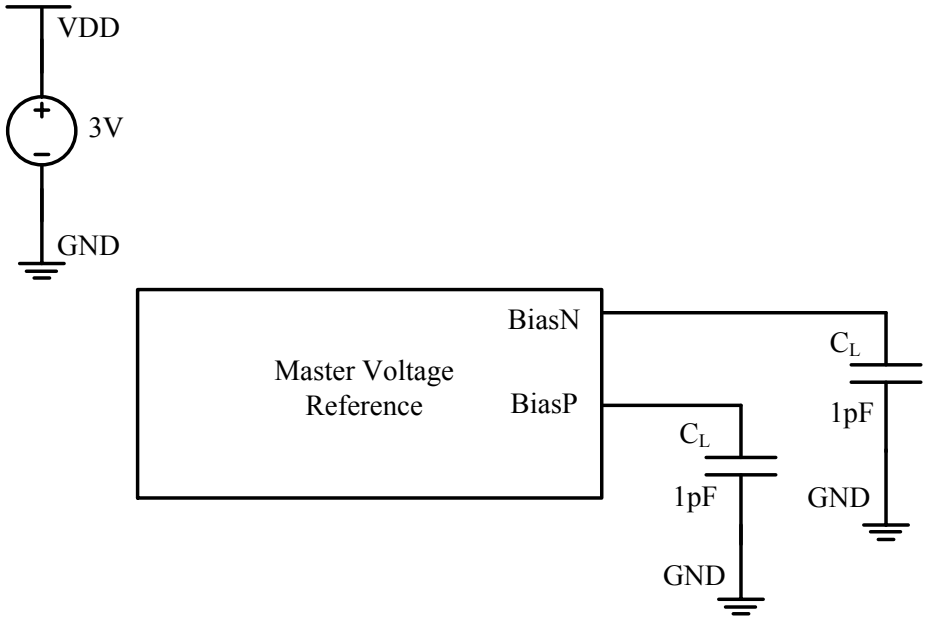


Fig 3.22 Master-bias voltage reference test circuit

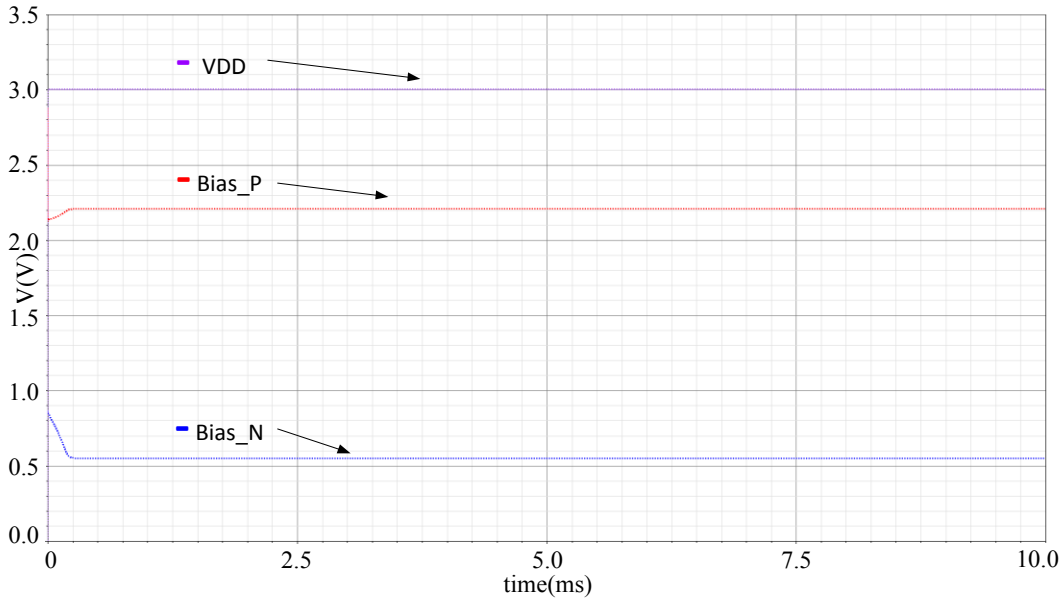


Fig 3.23 Master-bias voltage reference output voltage simulated waveform

The Bias_N reference voltage was measured to be 550 mV and Bias_P was measured to be 2.2 V. Bias_N will be used as a voltage reference for other reference circuits. The current consumption is shown in Fig 3.24. The current consumption was measured at 871.1 nA.

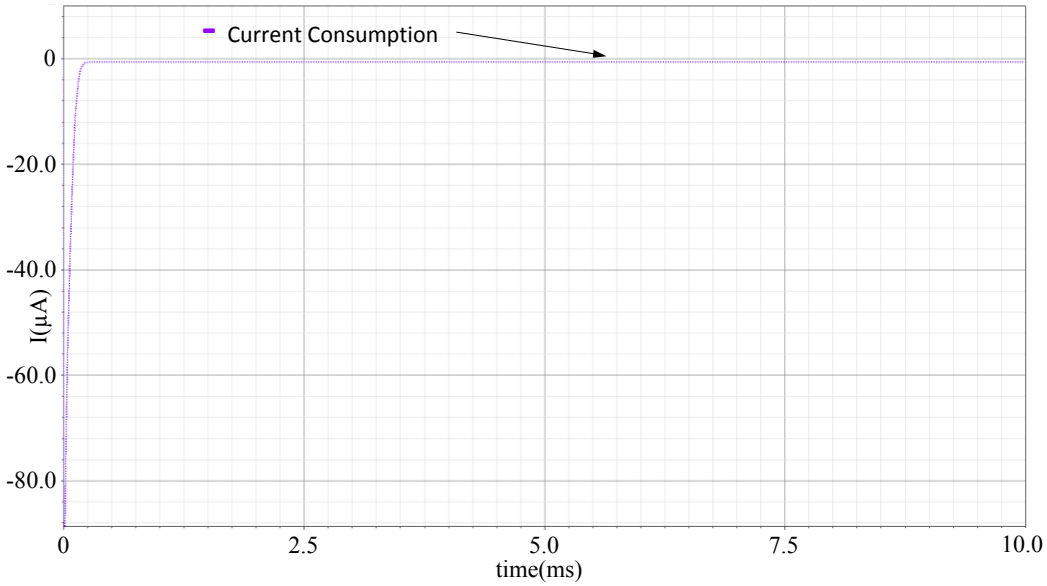


Fig 3.24 Master-bias voltage reference current consumption simulated waveform

3.9 Voltage references

The analog core of the transponder system consists of two voltage references which are driven by the master bias voltage reference. These voltage references are used to supply the required voltage levels to other circuits in the transponder. The first voltage reference is shown in Fig. 3.25. This voltage reference is designed using a stack of diode connected PMOS transistors (P1-P3) which are then connected to the NMOS transistor N1. Transistor N1 is driven by the Bias_N from the master bias voltage reference. The voltage levels at the gate of N1 determine the amount of current flowing through it. The stacked diode configuration experiences a V_{GS} drop after on PMOS transistor. The drop in voltage can be calculated by the following equation:

$$V_{GS} = |V_{THP}| + \sqrt{\frac{2.I_D}{\mu_p.\ C_{ox}.\ \frac{W}{L}}} \tag{3.4}$$

It should be noted from equation 3.4 that the required voltage drop can be achieved by adjusting the aspect ratio (W/L) of the transistor. The output voltages are taken at the gate of each PMOS transistor. The transistor sizes of this design are shown in Table 3.6.

Table 3.6 Transistor sizes of the voltage reference 1

Transistor	W	L
P1	17 µm	1.2 µm
P2	67.2 µm	1.2 µm

P3	67.2µm	1.2 µm
N1	17 µm	2 µm

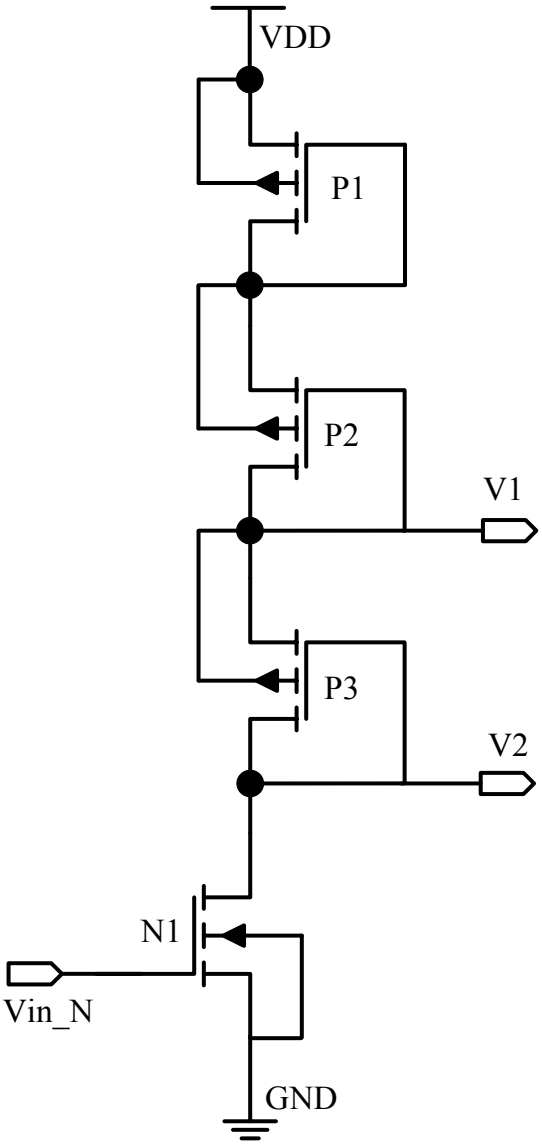


Fig 3.25 Voltage reference 1 schematic diagram

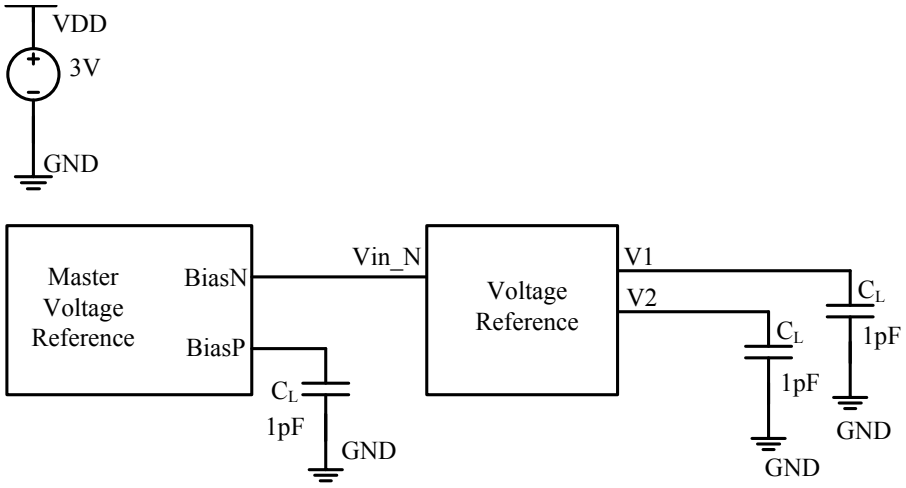


Fig 3.26 Voltage reference 1 test circuit

The test circuit for the voltage reference is shown in Fig 3.26. In this the master voltage reference output BiasN is connected to the voltage reference circuit. The generated voltage references are simulated across a capacitive load can be seen in Fig 3.27 with V1 = 1.45 V, V2 = 782 mV and BiasN = 550 mV. The current consumption of the entire system can be seen in Fig 3.28 which equals to 916.27 nA.

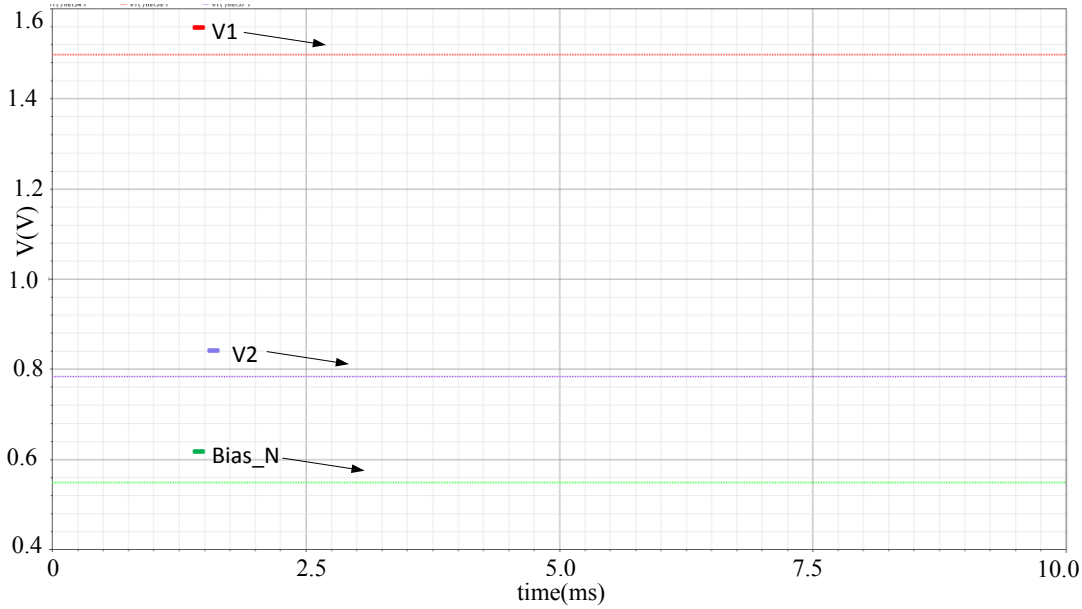


Fig 3.27 Voltage reference 1 simulated waveform

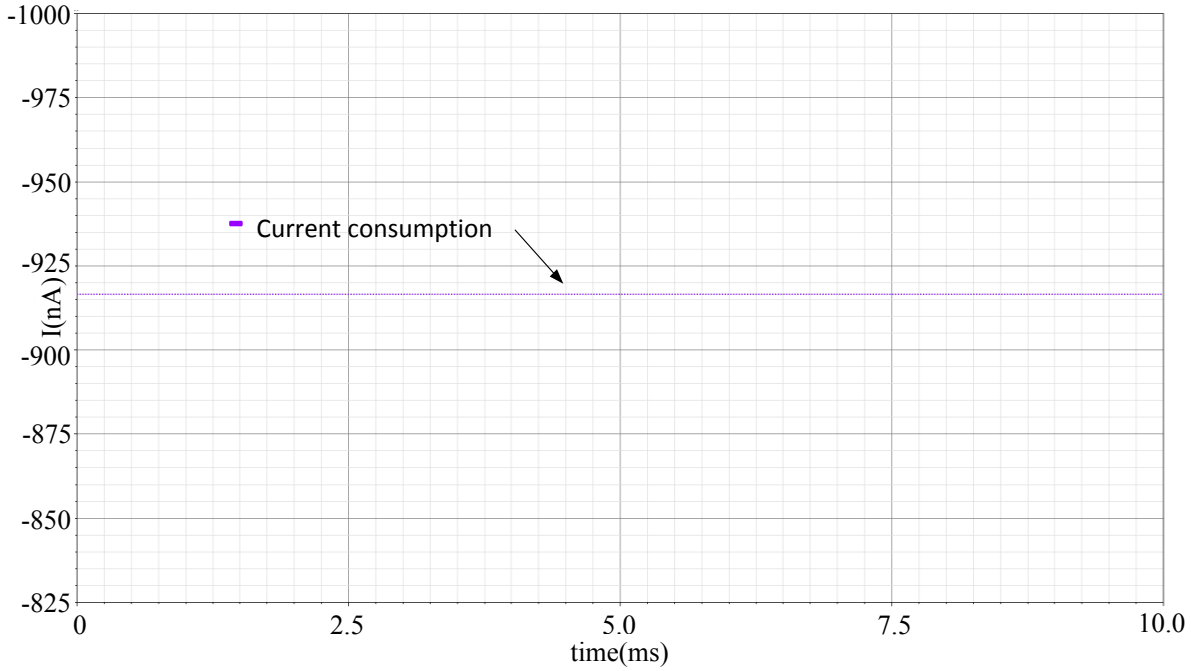


Fig 3.28 Voltage reference 1 current consumption

The second voltage reference is shown in Fig. 3.29. This voltage reference works on the same principles as the first voltage reference. This voltage reference circuit is used to design only one voltage level. The reason for the design of this voltage reference is to provide a 1 V supply voltage for the analog buffer used in the discharge phase of the CDC, which will be explained in detail later. This voltage reference is also driven by the BiasN output voltage of the master bias. The transistor sizes are given in Table 3. 7.

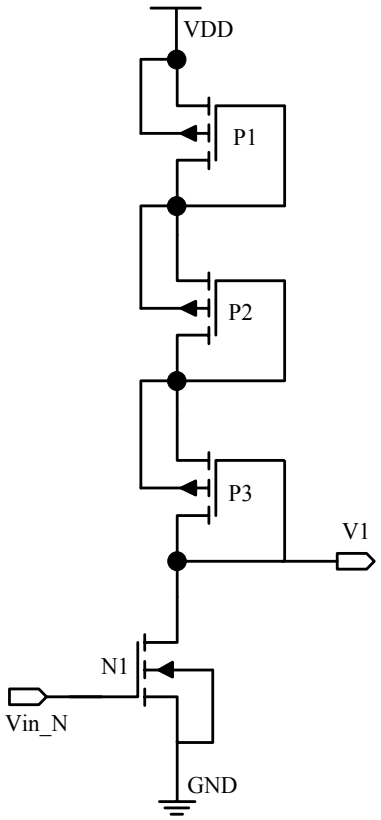


Fig 3.29 Voltage reference 2 schematic diagram

Table 3.7 Transistor sizes of the voltage reference 2

Transistor	W	L
P1	14µm	0.6µm
P2	14µm	0.6µm
P3	14µm	0.6µm
N1	16µm	2µm

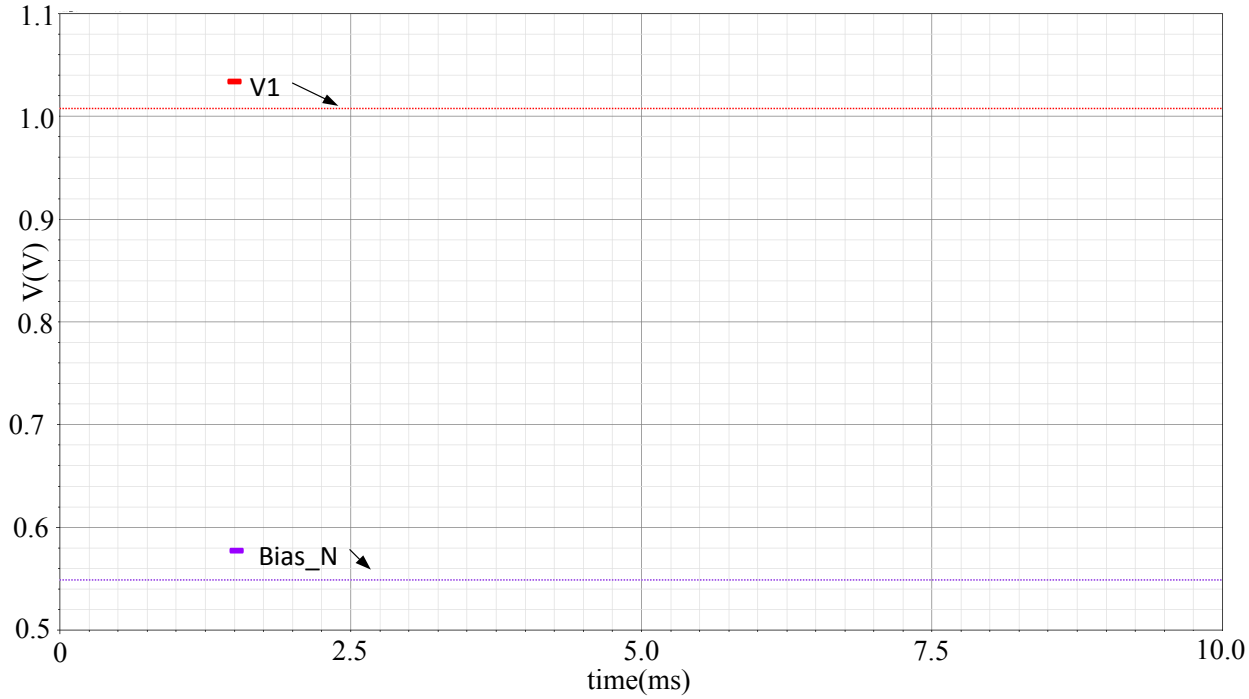


Fig 3.30 Voltage reference 2 simulated waveform

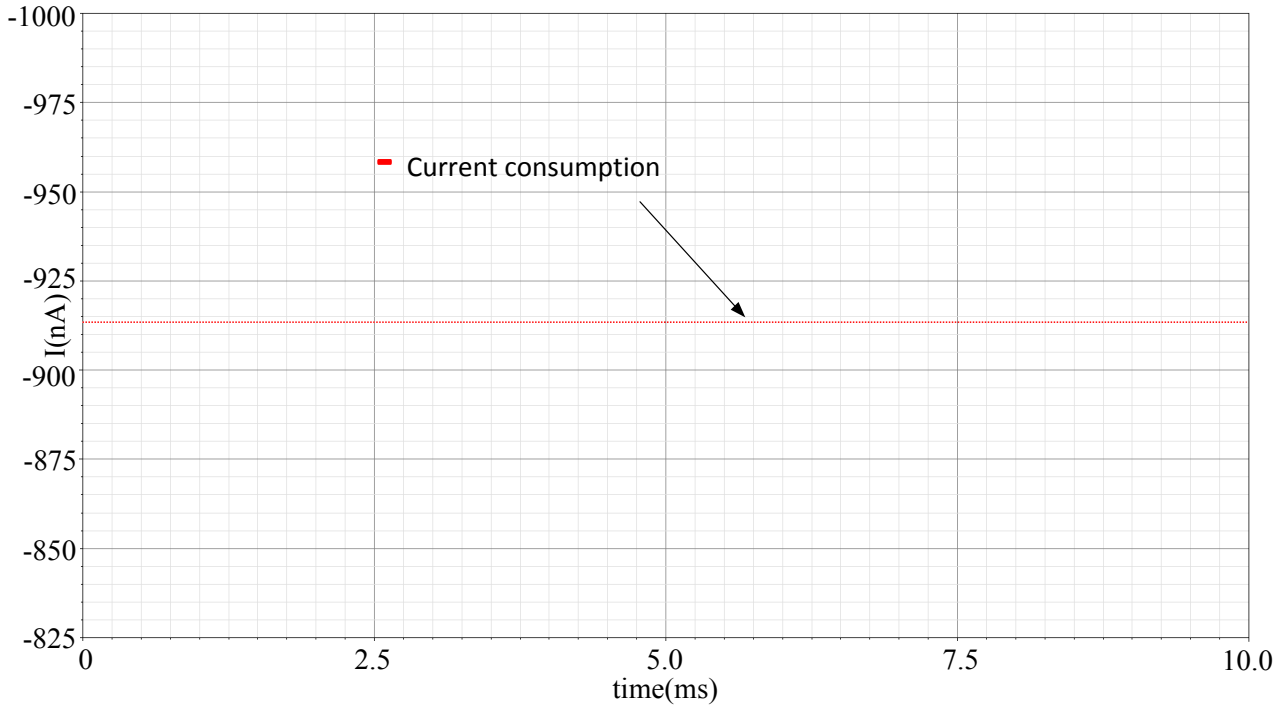


Fig 3.31 Voltage reference 2 current consumption

Same test circuit is implemented to test this reference circuit as that of the earlier one. Fig 3.30 shows the output voltage of the reference circuit. It can be noted that the output voltage is measured at 1.007 V. Fig 3.31 shows the total current consumption of the entire circuit. The current consumption is measured at 913.2622 nA.

3.10 Wide-swing Current Source

The wide-swing current source is used in the discharge phase of the CDC. The designed current source is shown in Fig. 3.32. The current source comprises of two current mirror branches. The current flowing in these branches is controlled by the voltage at the gate of transistor N1 and N2. These NMOS transistors are driven by the BiasN voltage from the master voltage bias circuit. The aspect ratio of the transistor P1 and P3 have to be designed for desirable current source operation. The procedure is as follows:

Let us assume current I_{ref} flowing in the branches of the current mirrors.

For PMOS P3 we have,

$$I_{ref} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_3}{L_3} \cdot (V_{GS3} - V_{TH3})^2 \quad (3.5)$$

Rewriting this as,

$$I_{ref} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W_3}{L_3} \cdot (V_{GS1} + V_{DS\,sat2} - V_{TH3})^2 \quad (3.6)$$

Since the gate of P2 and P1 are tied and both have the same aspect ratios,

$$V_{GS1} = V_{GS2}$$

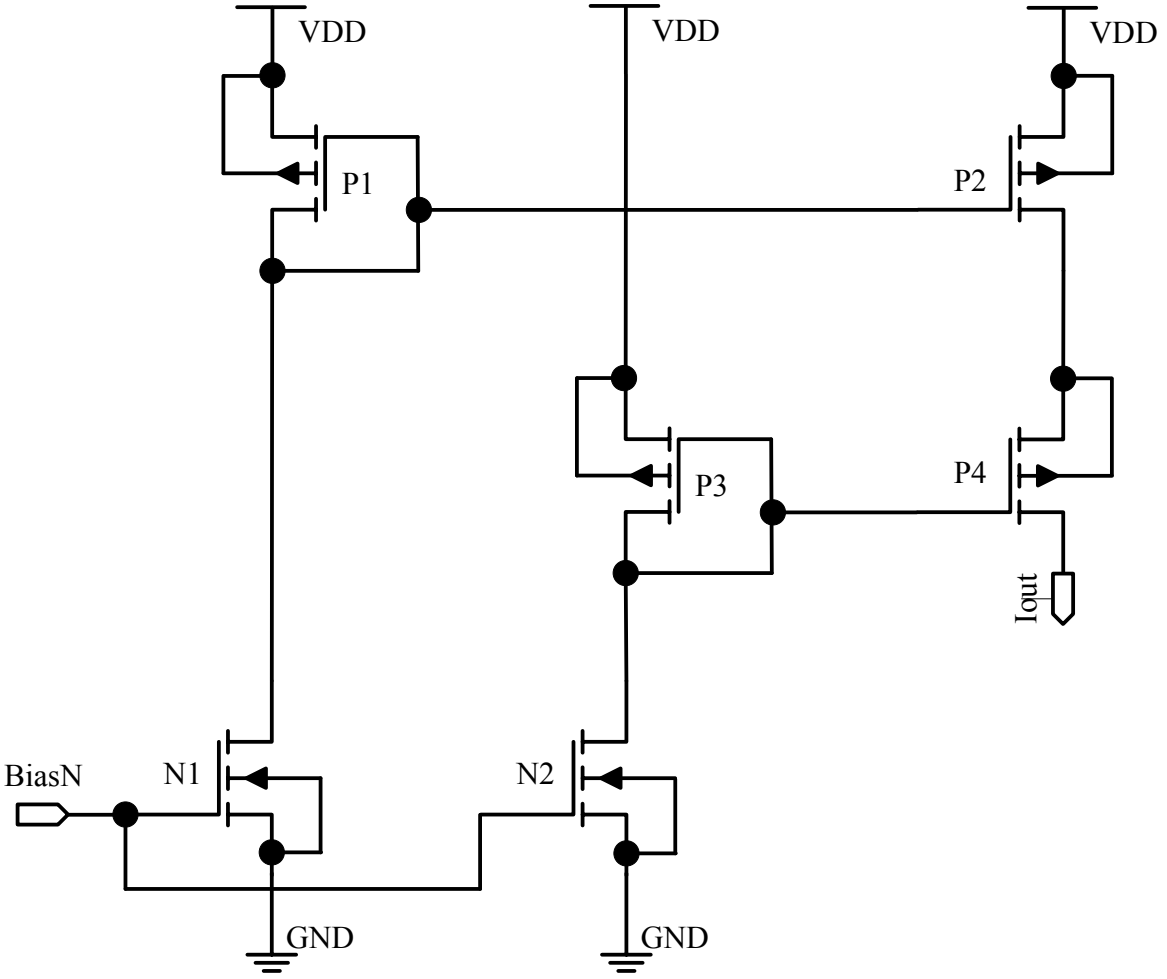


Fig 3.32 Wide-swing current source

Thus, $V_{DSsat2} = V_{GS1} - V_{TH2}$

$$I_{ref} = \frac{1}{2} . \mu_n . C_{ox} . \frac{W_3}{L_3} . (V_{GS1} + V_{GS1} - V_{TH2} - V_{TH3})^2 \quad (3.7)$$

If $V_{TH2} = V_{TH3}$, then,

$$I_{ref} = \frac{1}{2} . \mu_n . C_{ox} . \frac{W_3}{L_3} . (2V_{GS1} - 2V_{TH})^2 \quad (3.8)$$

Thus,

$$I_{ref} = \frac{1}{2} . \mu_n . C_{ox} . \frac{W_3}{L_3} . 4(V_{GS1} - V_{TH})^2 \quad (3.9)$$

Now, for PMOS transistor P1:

$$(V_{GS1} - V_{TH1})^2 = \frac{2 . I_{ref}}{\mu_n . C_{ox} . \frac{W_1}{L_1}} \quad (3.10)$$

Replacing in the earlier equation, $L_3 = 4\ L_1$, (if $W_1 = W_3$)

Also we take L3 = 5 L1, to ensure that P1 and P3 are in saturation.

Table 3.8 Transistor sizes of the wide-swing current source

Transistor	W	L
P1	30µm	2µm
P2	30µm	2µm
P3	30µm	10µm
P4	30µm	2µm
N1	7.65µm	2µm
N2	7.65µm	2µm

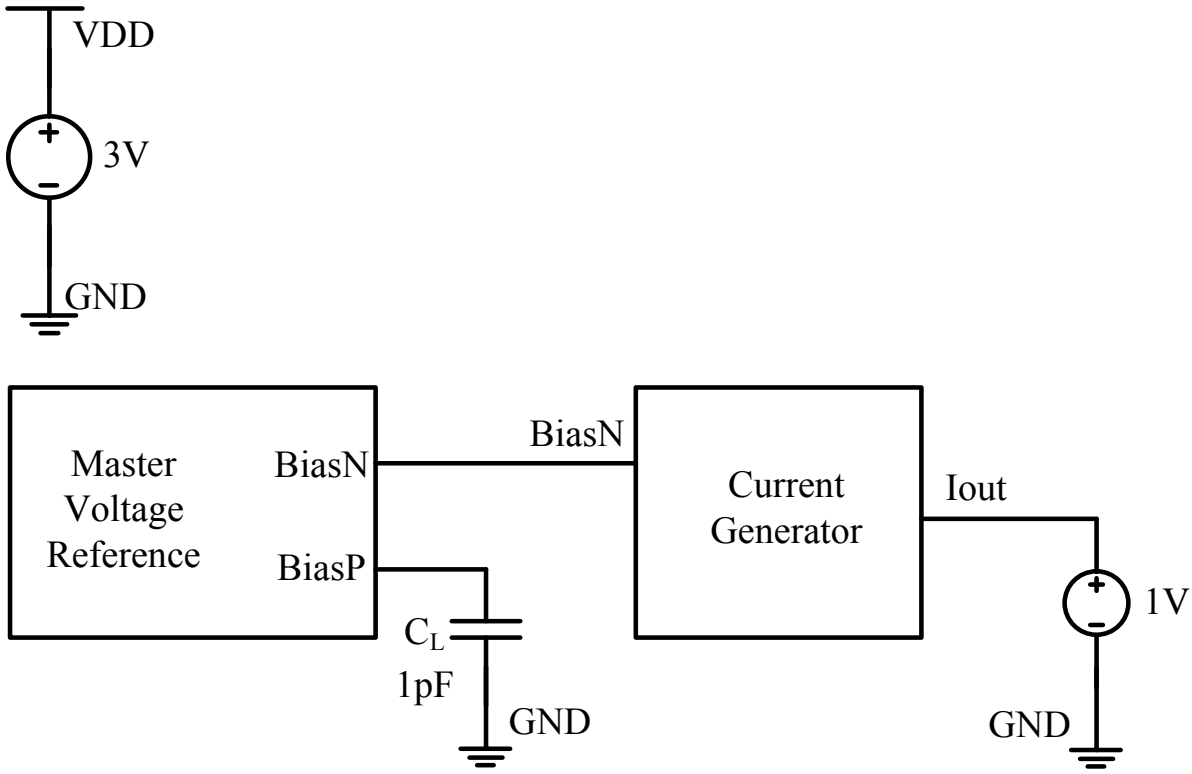


Fig 3.33 Wide-swing current source test circuit

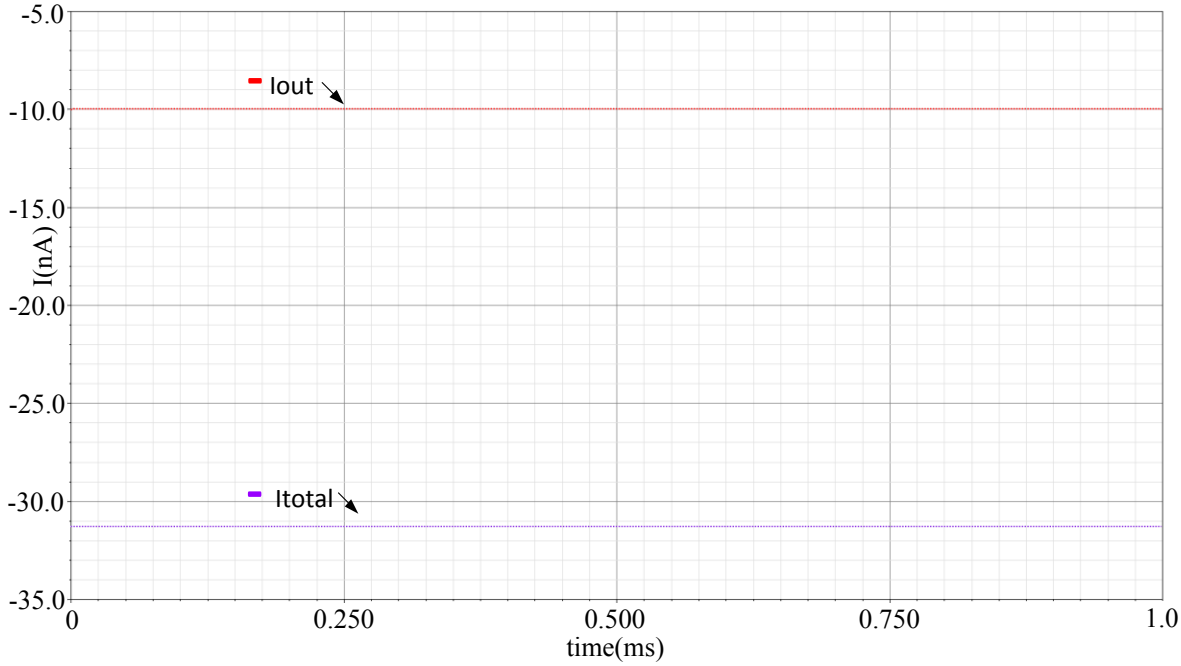


Fig 3.34 Wide-swing current source output simulation and current consumption

The transistor sizes are shown in table 3.8. It can be noticed that $L_3 = 5\ L_1$. The test circuit is shown in Fig 3.33. The test circuit consists of the current source being driven by the master voltage bias. The value of the current sourced is measured across an ideal voltage source connected in the opposite direction. Fig 3.34 shows the current sourced by the designed circuit as well as the total current consumption of the current source. The current sourced is measured at 10.24 nA and the total current consumption is measured at 31.323 nA.

3.11 Capacitance to digital converter:

The data converter for this system is selected to be a capacitance to digital converter (CDC). The schematic of the CDC is shown in Fig. 3.35. The passive capacitive sensor is shown as capacitor C_S in the CDC. C_S is a variable capacitor which changes its value proportional to the applied pressure. These type of capacitve pressure sensor exhibits a large fixed value of capacitance and a small variable value of capacitance. Capacitance C_{ref} has a value equal to the nominal fixed capacitance of C_S. A feedback capacitor C_{fb} is connected in the negative feedback loop of the integrator. The wide swing current sorce is shown as I_{ref} in the schematic. Voltage levels V_{ref}, V_{bias1} and V_{bias2} are derived from the voltage references. The switches are designed using transmission gates (TG).

The working of the CDC is divided into four phases. These different phases of operation are shown in Fig. 3.36. In reset phase, Φ_R and Φ'_A are closed discharging C_{fb}. In charging phase, Φ_A, Φ_1 and Φ_R are closed. In this phase C_S is charged to V_{ref} and C_{ref} is charged to V_{b2}. In charge distribution phase, Φ_A, Φ'_A and Φ_2 are closed. In this phase charge distribution takes place between C_S and C_{ref}. The residual charge is accumulated in C_{fb}. The total amount

of variable charge accumulated in C_{fb} will be further converted into time in the discharge phase.

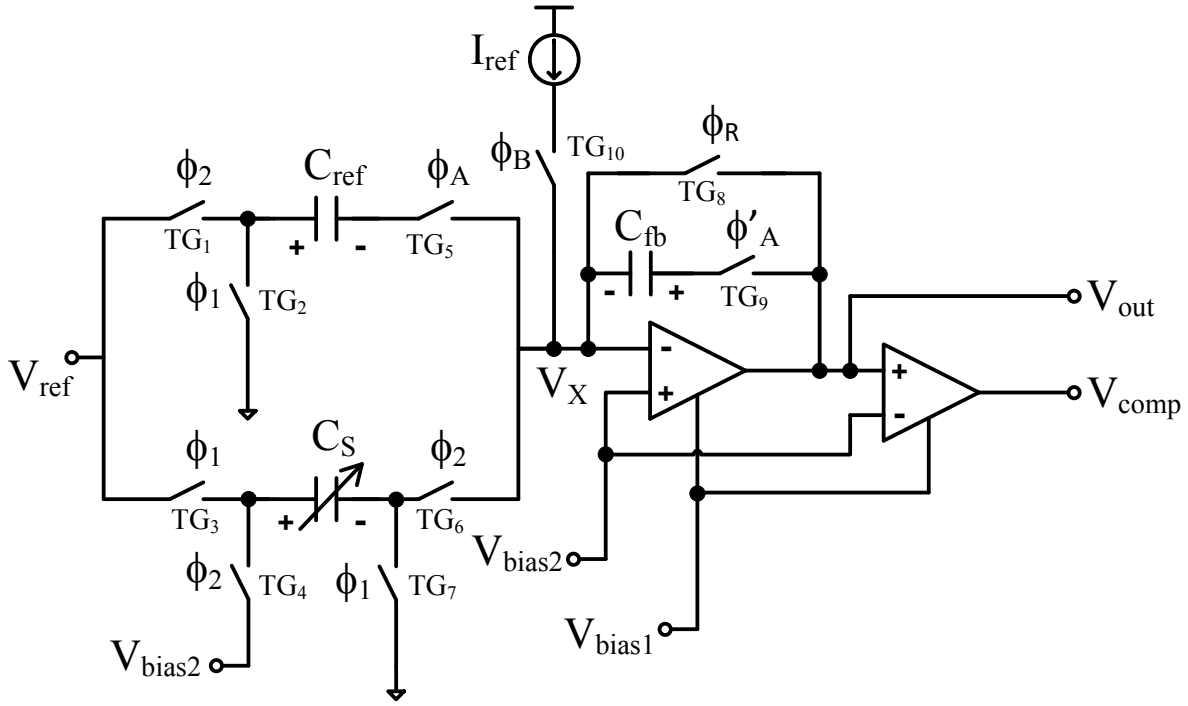


Fig 3.35 Capacitance to digital converter schematic

In the last phase, the discharge phase, switches Φ_B and Φ'_A are closed. In this phase the current source is used to drain the charges from C_{fb}. The time taken to discharge this amount of charge is measured. The output of the integrator is given to a comparator which produces a clean pulse when V_{out} moves below V_{bias2}. This pulse at V_{comp} can be given to a counter as an enable signal which will produce digital outputs. The CDC resolution was calculated to be 12 bits on 13.56 MHz clock.

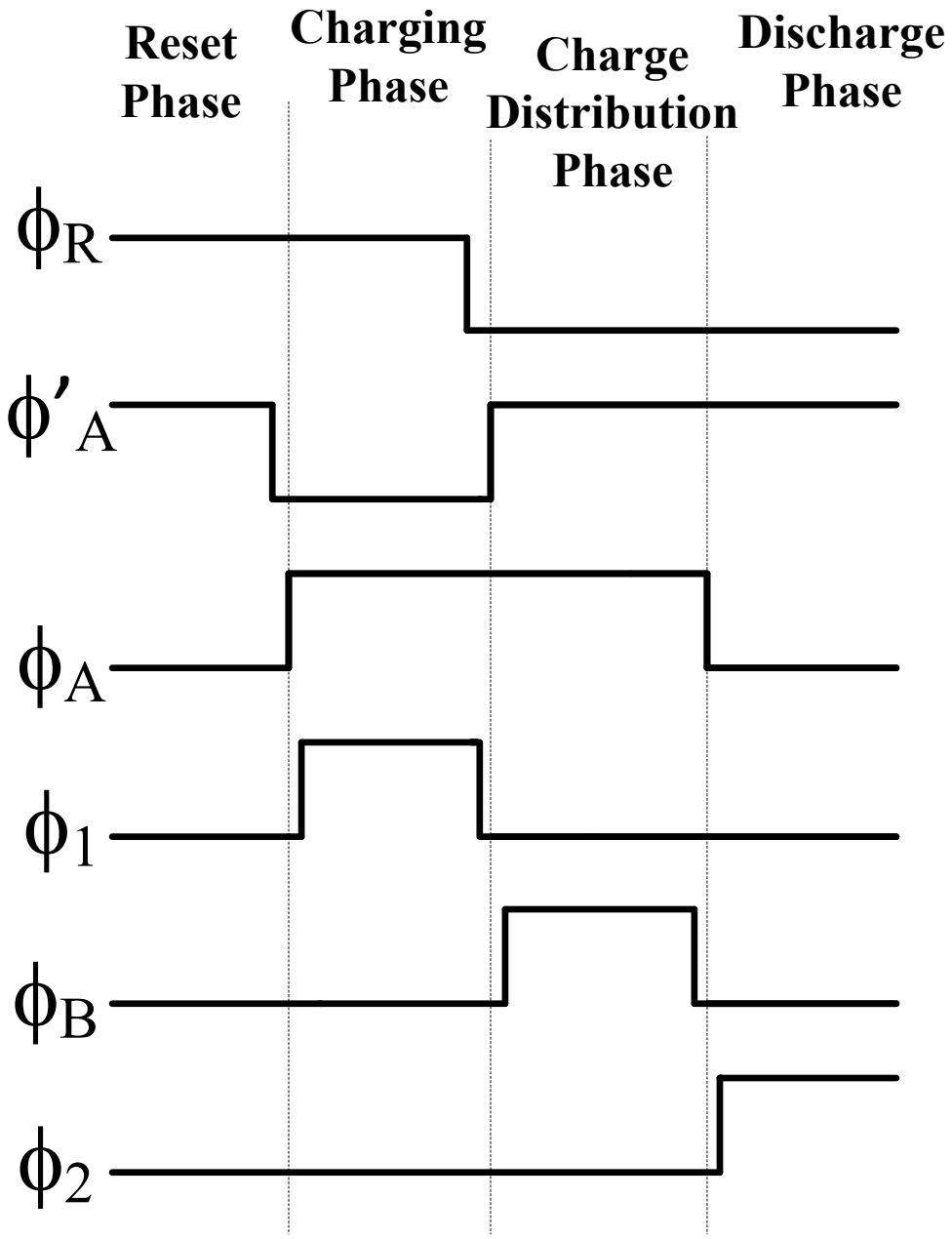


Fig 3.36 CDC operating phases and clocking

Analog buffer:

During charging and discharge phase it can be noted that Φ_A is active. To avoid the loading of the voltage reference 1 supplying 1.5 V to V_{bias2} input of the op-amp an analog buffer is used while Φ_A is active. The analog buffer is shown Fig 3.37. The analog buffer consists of a 2:1 multiplexer (MUX), the output of which is connected to the bias of the op-amp. The MUX has its select pin connected to the Φ_A. The two inputs of the MUX are provided by two voltage levels. The connectivity can be noted from Fig 3.1b. The op-amp used as the buffer is in negative feedback configuration. The positive terminal of the op-amp is connected to the voltage reference 1 supplying 1.5 V. When Φ_A is active the bias is increased to a higher voltage level providing an increased amount of current in the branches of the op-amp increasing its gain and increasing its response time, thus, providing a stable voltage to the CDC op-amp. The internal schematic of the MUX is shown in Fig. 3.38.

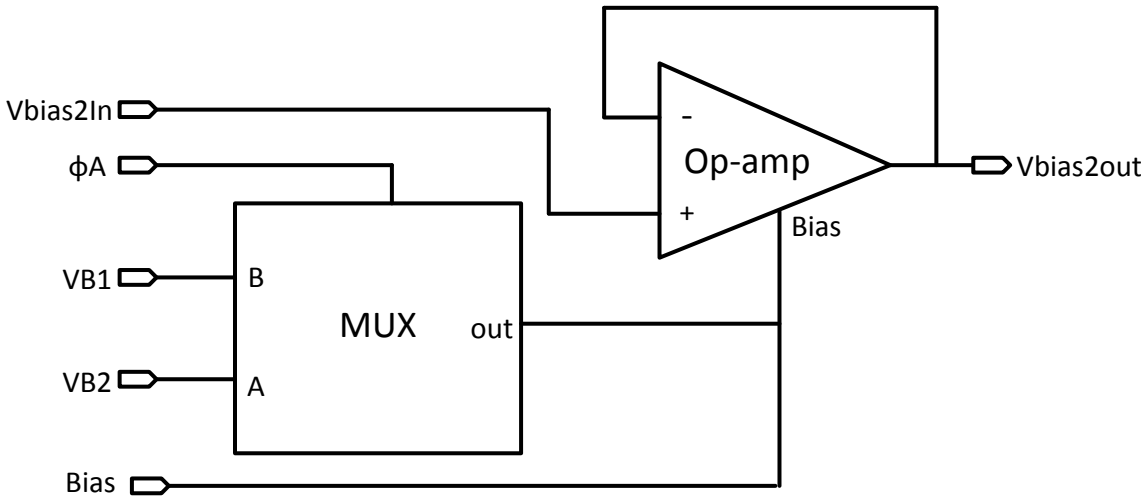


Fig 3.37 Analog buffer schematic

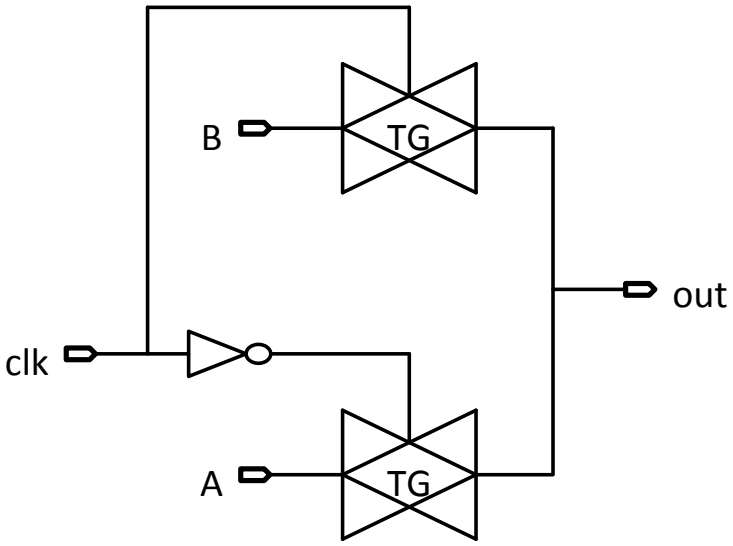


Fig 3.38 MUX schematic

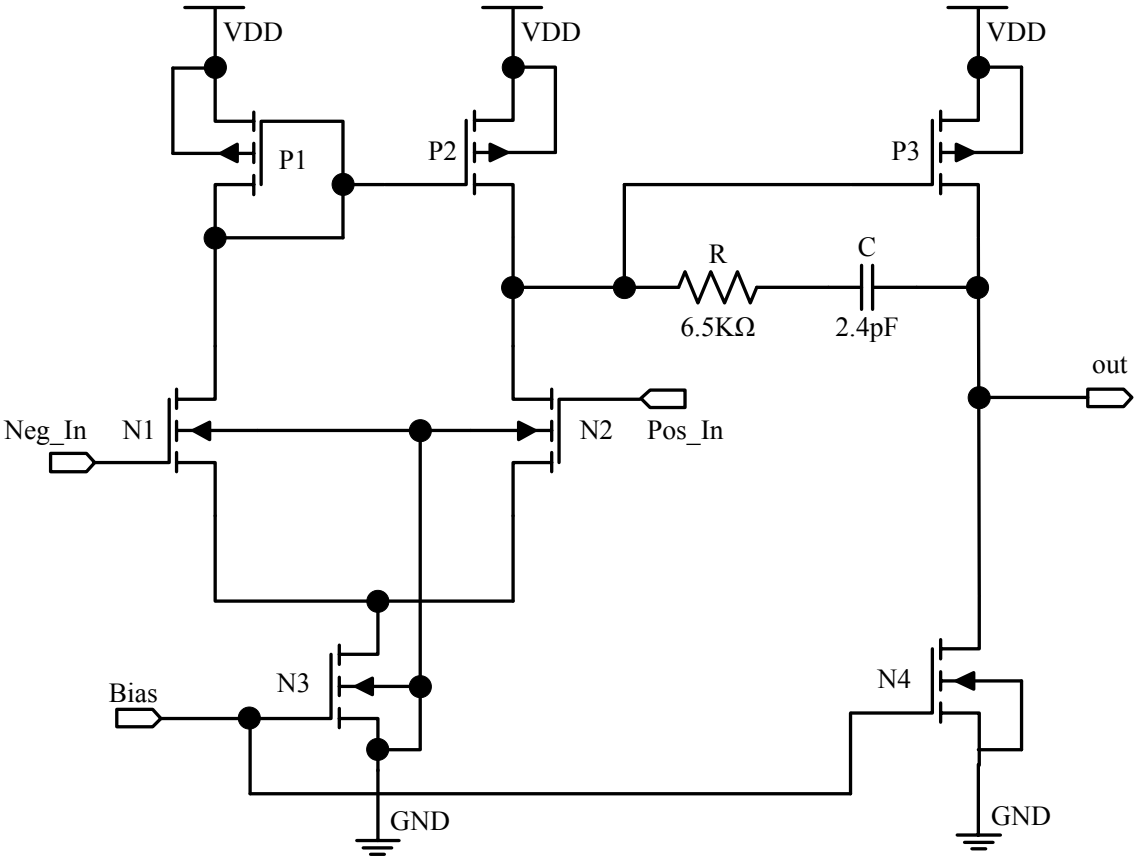


Fig 3.39 Op-amp schematic

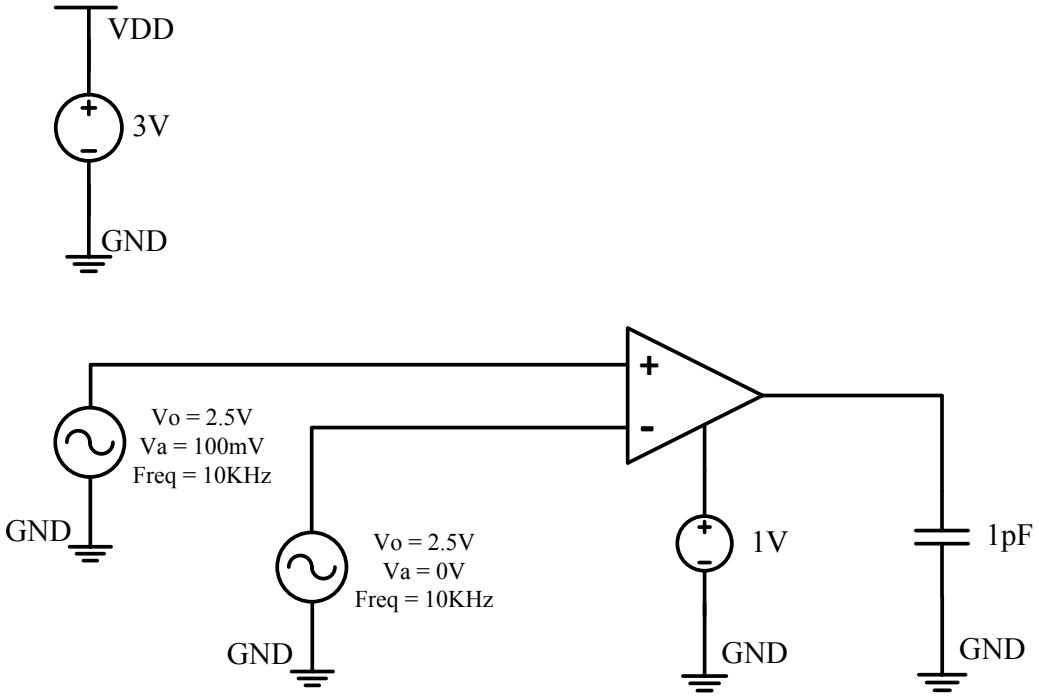


Fig 3.40 Op-amp test circuit

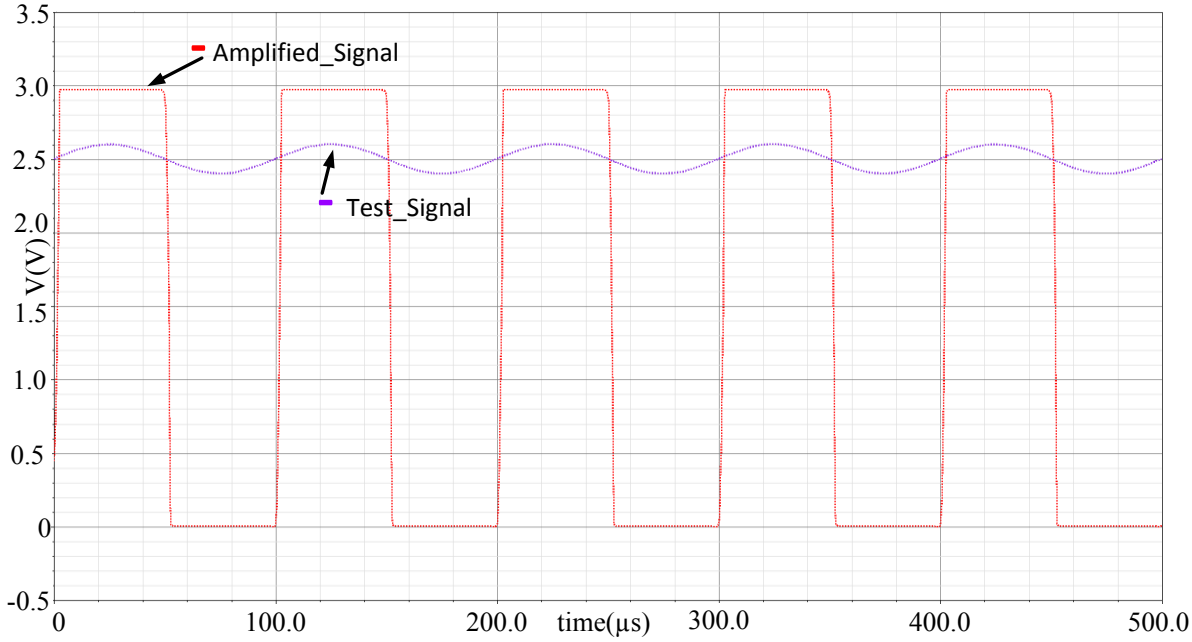


Fig 3.41 Op-amp amplified waveform

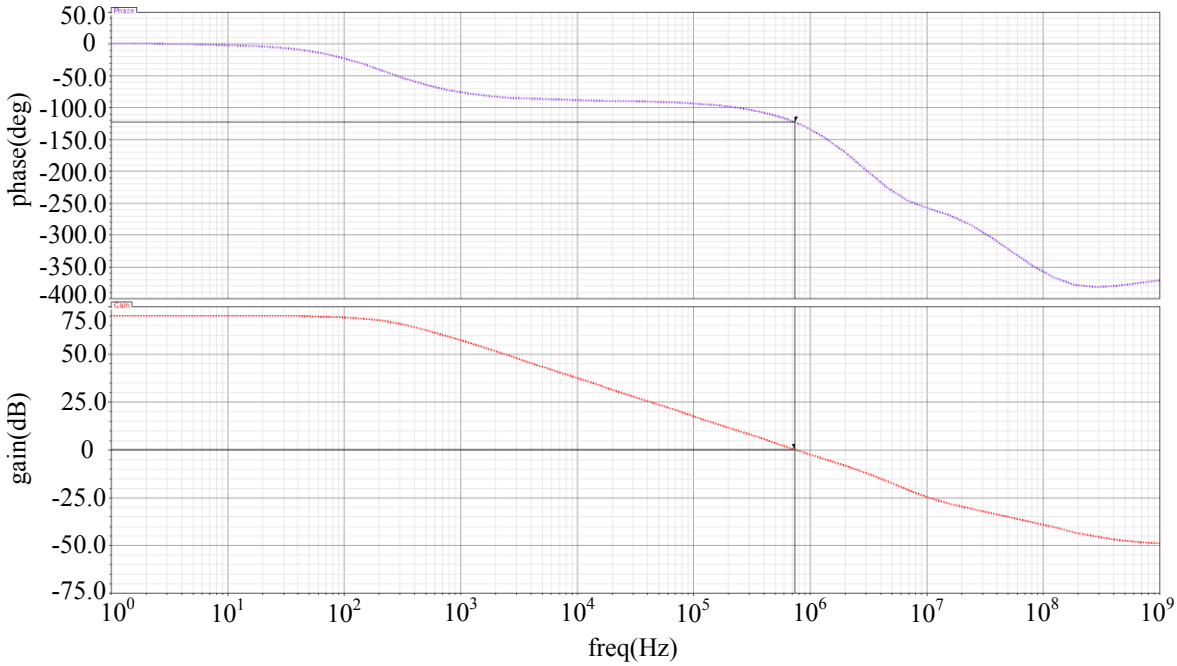


Fig 3.42 Op-amp gain and stability waveform

The transmission gates (TGs) used in the MUX are constructed using minimum device sizes of both NMOS and PMOS. The pin named bias in the analog buffer is internally connected and is also given as a separate pin for testing purposes in chip testing utilities. The schematic of the op-amp used in the construction of the CDC and analog buffer is shown in Fig. 3.39. The op-amp is a 2-stage differential amplifier having a gain of 70 dB and a phase margin of 60^o. A test circuit for the op-amp is shown in Fig 3.40. The open loop gain of the op-amp is measured in this setup. A 13.56 MHz sine wave of 100 mV with a DC component of 2.5V is applied to the positive terminal. The negative terminal is connected to a DC supply of 2.5 V. The amplified signal is seen in Fig. 3.41. The simulations of gain and stability is shown inn Fig. 3.42. The op-amp is designed to have low-power consumption at 7 μW. The transistor sizes in the op-amp are given in table 3.9.

Table 3.9 Transistor sizes of op-amp

Transistor	W	L
P1	50 µm	1.2 µm
P2	50 µm	1.2 µm
P3	120 µm	1.2 µm
N1	100 µm	1.2 µm
N2	100 µm	1.2 µm
N3	9 µm	1 µm
N4	15 µm	1.2 µm

The simulation of a 6.2 pF of test capacitance for C_S is shown in Fig. 3.43. The four phases of operation are shown in Fig 3.43. The waveform depicts Vout which is taken at the output of the integrator. It can be seen that the voltage level gradually decreases in the discharge phase. All the voltage levels at different phases can be theoretically calculated as shown below in the calculation section. Also noted in the waveform is the effect of charge injection from switches involved in the change in phases. The waveform marked Vcomp is taken at the comparator output. A clean pulse is obtained by using an AND gate at the output of the comparator and the discharge phase clock pulse. The width of the pulse generated is

proportional of the variable part of C_S. The pulse waveform can be fed to a counter with a desired clock frequency to obtain the digital equivalent.

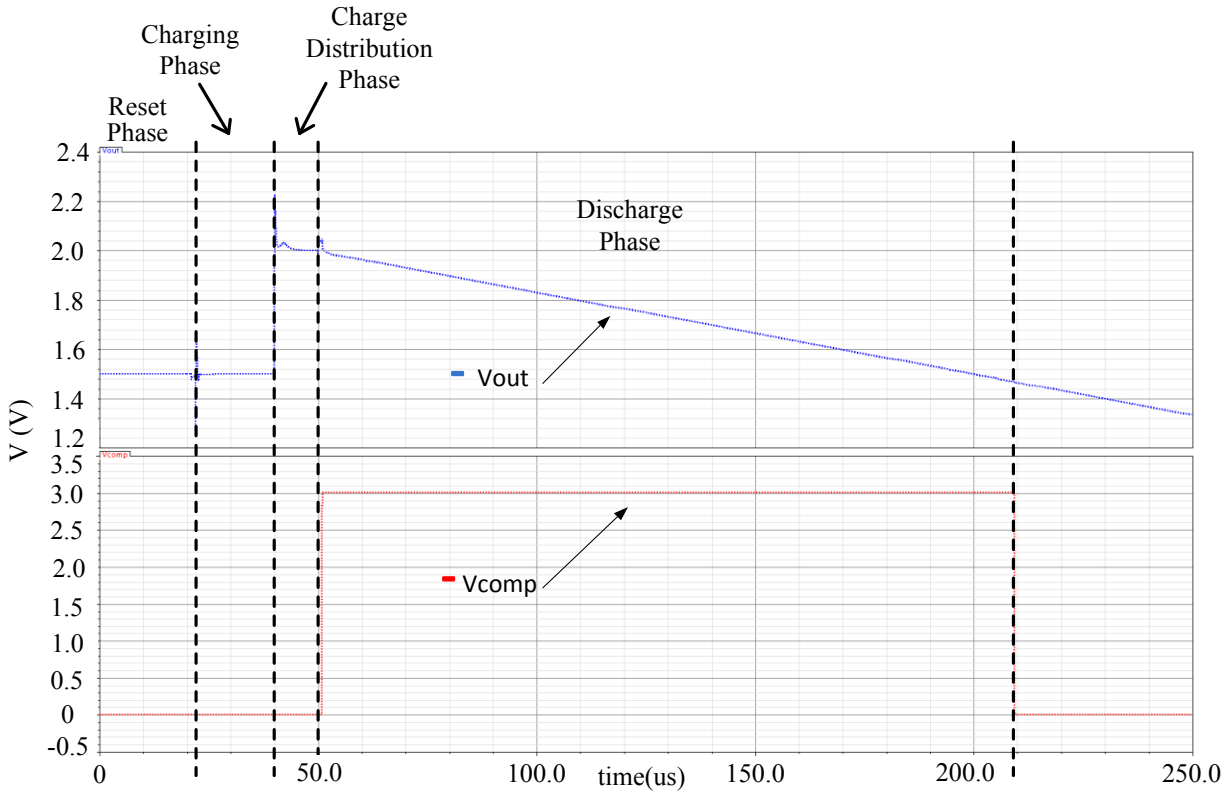


Fig 3.43 CDC waveform for 6.2 pF of C_S

Capacitance to Digital Converter Calculations:

In this section we present the capacitance to time conversion calculations. Two types of calculations are presented, ideal case calculation and calculations involving charge injection and op-amp offset.

Ideal CDC case: (without op-amp offset and charge injection)

Reset phase: switches TG_8 and TG_9 are closed, all other switches are open.

Equivalent Circuit:

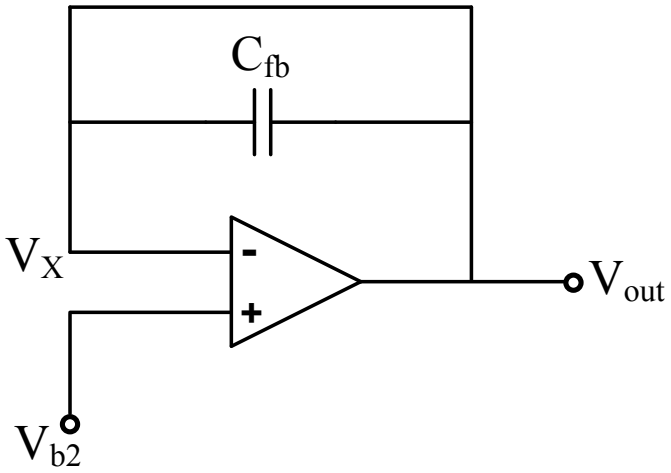


Fig 3.44 CDC reset phase equivalent circuit

At this time: $Q_{fb} = 0$ (charge in C_{fb})

$V_{fb} = 0$ (voltage across C_{fb})

$V_x = V_{b2} = V_{out}$

Charging phase: switches TG_5, TG_2, TG_3, TG_7 and TG_9 are closed, all other switches are open. Equivalent Circuit:

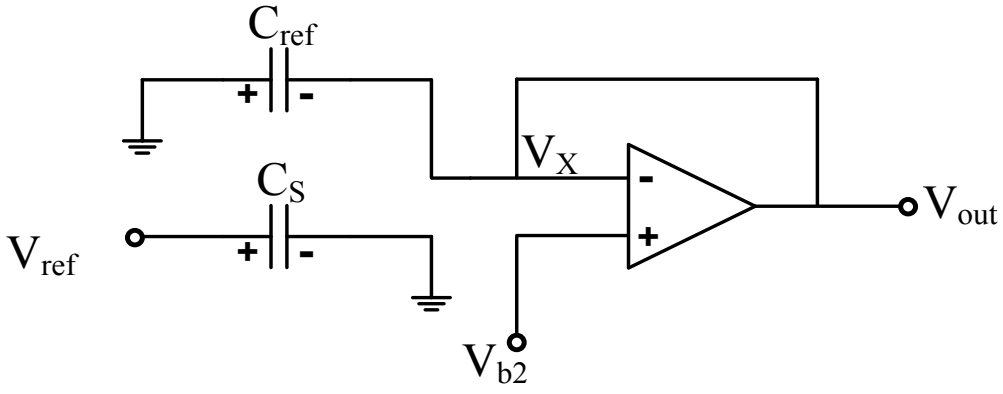


Fig 3.45 CDC charging phase equivalent circuit

At this time: $V_x = V_{b2}$

$$Q_{ref1} = -V_{b2} \cdot C_{ref} \quad (3.11)$$

$$Q_{s1} = V_{ref} \cdot C_s = Vref \cdot (C_x + C_{ref}) \quad (3.12)$$

Charge distribution phase: Switches TG_5, TG_9, TG_1, TG_4 and TG_6 are closed, all other switches are open

Equivalent Circuit:

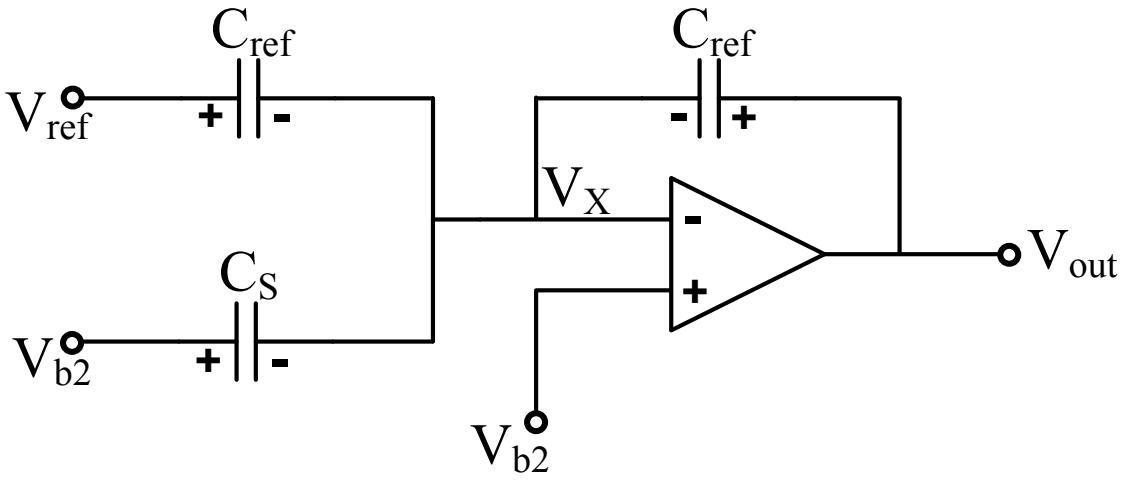


Fig 3.46 CDC charge distribution phase equivalent circuit

At this time: $V_{out} = V_{b2} + V_{fb}$

$$Q_{s2} = (V_{b2} - V_{b2}) \cdot C_s = 0 \quad (3.13)$$

$$Q_{ref2} = (V_{ref} - V_{b2}) \cdot C_{ref} \quad (3.14)$$

The difference in charges between the charging phase and charge distribution phase is given by the following equations:

$$\Delta Q_s = Q_{s1} - Q_{s2} \quad (3.15)$$

$$= V_{ref} \cdot (C_x + C_{ref}) - 0$$

$$\Delta Q_s = V_{ref} \,.\, (C_x + C_{ref}) \tag{3.16}$$

Thus, C_S is fully discharged.

Also, $$\Delta Q_{ref} = Q_{ref1} - Q_{ref2} \tag{3.17}$$

$$= - V_{b2}.C_{ref} - (V_{ref} - V_{b2})C_{ref}$$

$$= - V_{ref} \,.\, C_{ref} \tag{3.18}$$

Therefore, total charge accumulated in the feedback capacitor:

$$Q_{fb} = \Delta Q_s + \Delta Q_{ref}$$

$$= V_{ref} \,.\, (C_x + C_{ref}) - V_{ref} \,.\, C_{ref}$$

$$Q_{fb} = V_{ref} \,.\, C_x \tag{3.19}$$

Re-writing $V_{out} = V_{b2} + \frac{Q_{fb}}{C_{fb}}$

$$= V_{b2} + \frac{V_{ref}.C_x}{C_{fb}} \tag{3.20}$$

<u>Discharge phase</u>: switches TG_{10}, TG_9 are closed, all other switches are open

At this time: positive charges from the current source I_{ref} are supplied to the feedback capacitor.

Thus, $$V_{out} = V_{b2} + \frac{V_{ref}.C_x}{C_{fb}} - \frac{1}{C_{fb}} \int_{T_1}^{T_2} I \, dt \tag{3.21}$$

$$V_{out} = V_{b2} + \frac{V_{ref}.C_x}{C_{fb}} - \frac{I}{C_{fb}} (T_2 - T_1) \tag{3.22}$$

Where, T_1 is the time when positive charges from the current generator start discharging the feedback capacitor C_{fb}. We will set $T_1 = 0$. T_2 is the time when $V_{out} = V_{b2}$

Thus, $$V_{out} = V_{b2} + \frac{V_{ref}.C_x}{C_{fb}} - \frac{I}{C_{fb}} (T_2) \tag{3.23}$$

Equivalent circuit:

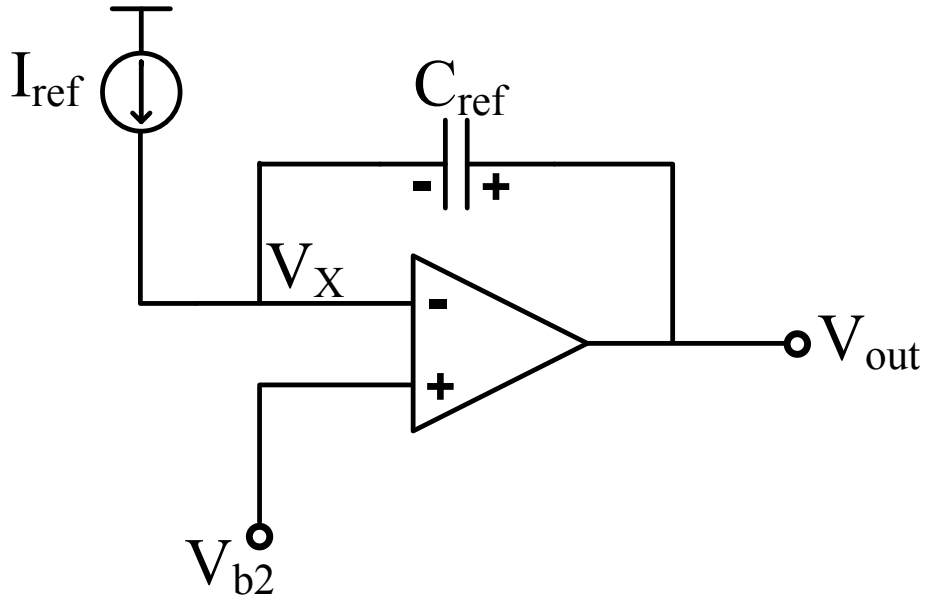


Fig 3.47 CDC discharge phase equivalent circuit

Finally, rearranging and cancelling similar terms:

$$T_2 = \frac{C_x . V_{ref}}{I} \tag{3.24}$$

From the above equation we show that the variable part of C_S is converted to time by the proposed CDC circuit.

Non-Idealities:

In this section we will perform calculations considering charge injection and opamp offset:

The charge injection of a transmission gate (TG) is calculated.

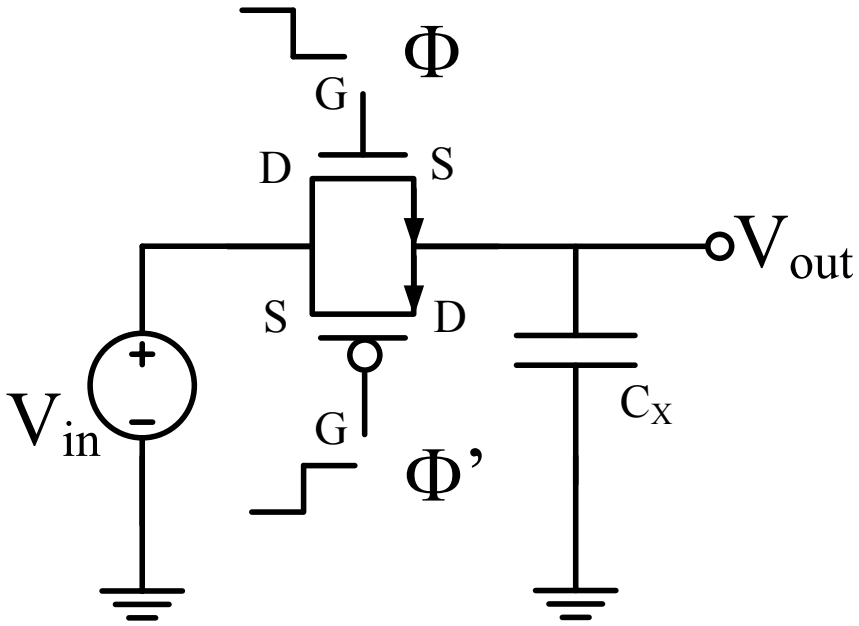


Fig 3.48 Transmission gate charge injection setup

Charge accumulated in NMOS when transistor is on:

$$Q_N = - C_{ox} . W . L . (V_{eff})$$

$$= - C_{ox} . W . L . (V_{GS} - V_{THN})$$

$$= - C_{ox} . W . L . (V_{DD} - V_{in} - V_{THN})$$

Charge accumulated in PMOS when it is on:

$$Q_P = C_{ox} . W . L . (V_{eff})$$

$$= C_{ox} . W . L . (V_{SG} - |V_{THP}|)$$

$$= C_{ox} . W . L . (V_{in} - |V_{THP}|)$$

Total charge accumulated:

$$Q_{TOTAL} = Q_N + Q_P$$

$$= - C_{ox} . W . L . (V_{DD} - V_{in} - V_{THN}) + C_{ox} . W . L . (V_{in} - |V_{THP}|)$$

$$Q_{TOTAL} = C_{ox} \cdot W \cdot L \cdot (- V_{DD} + 2V_{in} + V_{THN} - |V_{THP}|)$$

The effective charge injection is given by:

$$Q_{INJ} = \frac{Q_{TOTAL}}{2}$$

$$Q_{INJ} = \frac{C_{ox} \cdot W \cdot L \cdot (- V_{DD} + 2V_{in} + V_{THN} - |V_{THP}|)}{2} \quad (3.25)$$

Therefore, the effective voltage change at C_X:

$$\Delta V_X = \frac{Q_{TOTAL}}{2 \cdot C_X}$$

Reset phase: Switches (TG_8 and TG_9) are closed, all other switches are open

Equivalent Circuit:

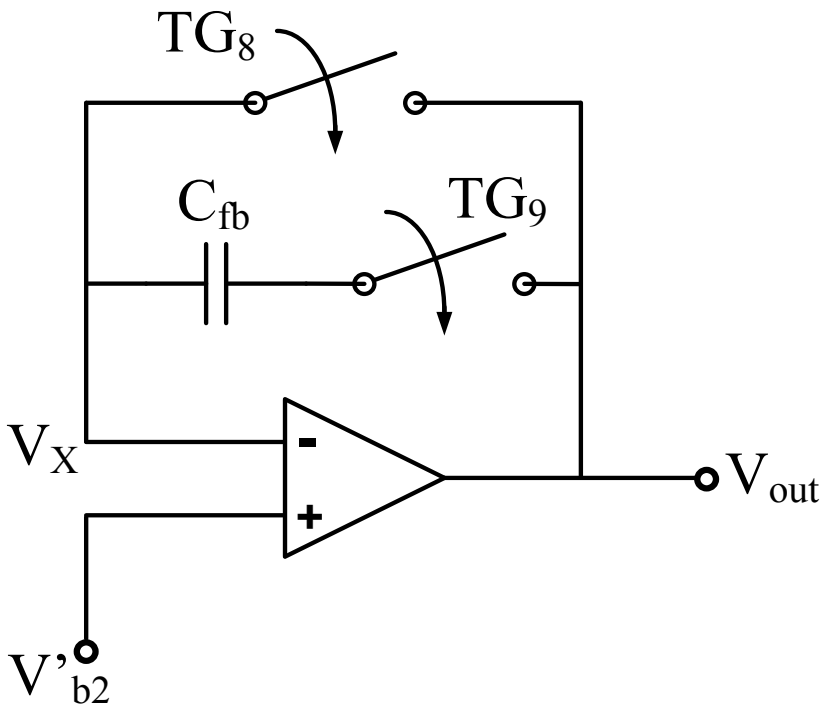


Fig 3.49 CDC reset phase equivalent circuit – charge injection model

Taking opamp offset into consideration: $V'_{b2} = V_{b2} + V_{off1}$

At this time: $Q_{fb} = 0$

$$V_{fb} = 0$$

$$V_x = V'_{b2} = V_{b2} + V_{off1} = V_{out}$$

So, charge accumulated in TG_8:

$$Q_8 = Cox \,.\, W.\, L.\, (-\, V_{DD} + 2V'_{b2} + V_{THN} - |V_{THP}|)$$

Also, charge accumulated at TG_9:

$$Q_9 = Cox \,.\, W.\, L.\, (-\, V_{DD} + 2V'_{b2} + V_{THN} - |V_{THP}|)$$

Charging phase: Switches Φ_A, Φ_1 and Φ_R (TG_5, TG_2, TG_3, TG_7 and TG_9) are closed, all other switches are open.

Equivalent Circuit:

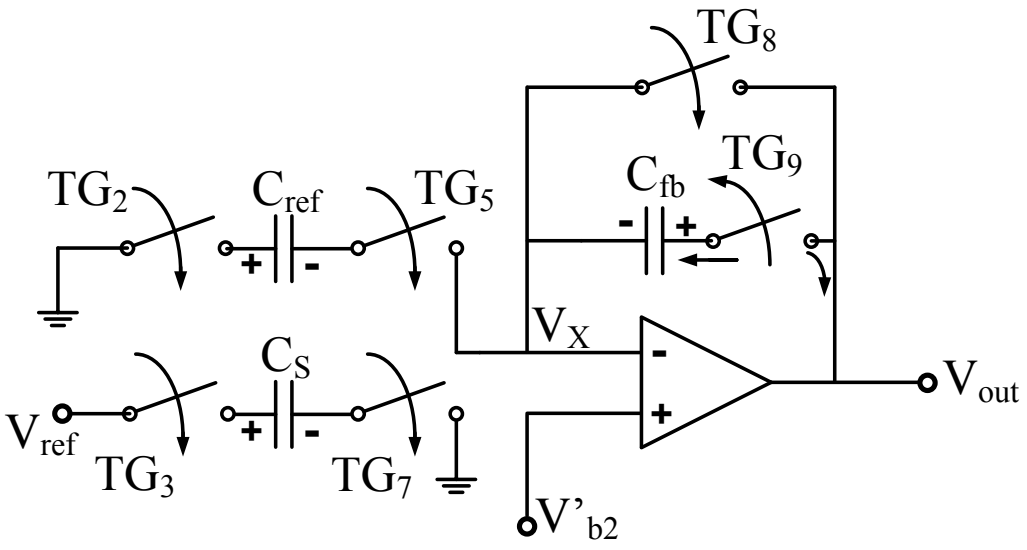


Fig 3.50 CDC charging phase equivalent circuit – charge injection model

At this time: TG_9 opens (during Φ'_A).

Thus, the effective charge injection becomes $\frac{Q_9}{2}$

And the charge accumulated in C_{fb} is:

$$Q_{fb1} = \frac{Q_9}{2} = \frac{C_{ox} \cdot W \cdot L \cdot (-V_{DD} + 2V'_{b2} + V_{THN} - |V_{THP}|)}{2}$$

Also, $Q_{ref1} = - V'_{b2} \cdot C_{ref}$

$$Q_{s1} = V_{ref} \cdot C_s = V_{ref} (C_{ref} + C_x)$$

The, charge accumulated in the various TGs in this phase is:

At TG_5 $Q_5 = C_{ox} \cdot W. L. (- V_{DD} + 2V'_{b2} + V_{THN} - |V_{THP}|)$

At TG_2 $Q_2 = C_{ox} \cdot W. L. (- V_{DD} + V_{THN} - |V_{THP}|)$

At TG_3 $Q_3 = C_{ox} \cdot W. L. (- V_{DD} + 2V_{ref} + V_{THN} - |V_{THP}|)$

At TG_7 $Q_7 = C_{ox} \cdot W. L. (- V_{DD} + V_{THN} - |V_{THP}|)$

Charge distribution phase: Switches TG_5, TG_9, TG_1, TG_4 and TG_6 are closed, all other switches are open.

First, consider when TG_2, TG_3, TG_7, TG_8 are open charge injection from TG_8 enters C_{fb} at the negative terminal.

Thus, $Q_{fb2} = Q_{fb1} - \frac{Q_8}{2} = 0$

It can be inferred from the above equation that C_{fb} is fully discharged.

Equivalent Circuit:

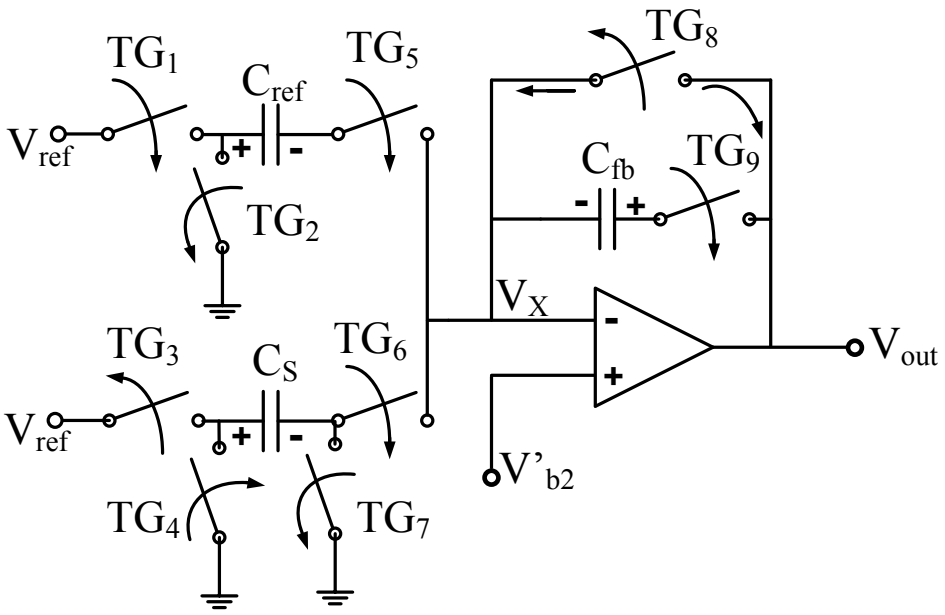


Fig 3.51 CDC charge distribution phase equivalent circuit – charge injection model

Charge injection from TG_2 flows into C_{ref}.

Thus, $Q_{ref2} = \frac{Q_2}{2} + Q_{ref1}$

$$Q_{ref2} = \frac{C_{ox} \cdot W \cdot L \cdot (-V_{DD} + V_{THN} - |V_{THP}|)}{2} - V'_{b2} \cdot C_{ref}$$

Also, charge injection from TG_3 and TG_7 flows to C_s.

So, $Q_s = V_{ref}(C_{ref} + C_x) + \frac{C_{ox}}{2} \cdot W \cdot L \cdot (-V_{DD} + 2V_{ref} + V_{THN} - |V_{THP}|)$

$$- \frac{C_{ox}}{2} \cdot W \cdot L \cdot (-V_{DD} + V_{THN} - |V_{THP}|)$$

$$= V_{ref}(C_{ref} + C_x) + C_{ox} \cdot W \cdot L \cdot V_{ref}$$

Consider TG_1, TG_5, TG_4, TG_6, TG_9 are closed.

Thus, $V_{out} = V'_{b2} + V_{fb}$

$$Q_{s3} = V_{eff} \,.\, C_s = (V_{b2} - V'_{b2}) \,.\, C_s = - V_{off1} \,.\, C_s$$

$$Q_{ref3} = V_{eff} \,.\, C_{ref} = (V_{ref} - V'_{b2}) \,.\, C_{ref}$$

Thus, change in charge in C_S is:

$$\Delta Q_s = Q_{s2} - Q_{s3}$$

$$= V_{ref} (C_{ref} + C_x) + V_{off1} (C_{ref} + C_x) + C_{ox} \, W. \, L. \, V_{ref} \qquad (3.26)$$

$$\Delta Q_{ref} = Q_{ref2} - Q_{ref3}$$

$$= \frac{C_{ox} \,.\, W \,.\, L \,.\, (-V_{DD} + V_{THN} - |V_{THP}|)}{2} - V'_{b2} \,.\, C_{ref} - (V_{ref} - V'_{b2}) \,.\, C_{ref}$$

$$= \frac{C_{ox} \,.\, W \,.\, L \,.\, (-V_{DD} + V_{THN} - |V_{THP}|)}{2} - V_{ref} \,.\, C_{ref} \qquad (3.27)$$

Thus, the total charge transferred to the feedback capacitor is:

$$Q_{fb1} = \Delta Q_s + \Delta Q_{ref}$$

$$= V_{ref} (C_{ref} + C_x) + V_{off} (C_{ref} + C_x) + C_{ox} \, W. \, L. \, V_{ref}$$

$$+ \frac{C_{ox} \,.\, W \,.\, L \,.\, (-V_{DD} + V_{THN} - |V_{THP}|)}{2} - V_{ref} \,.\, C_{ref}$$

$$Q_{fb1} = V_{ref} \,.\, C_x + V_{off} \,.\, C_s + \frac{C_{ox} \,.\, W \,.\, L \,.\, (2V_{ref} - V_{DD} + V_{THN} - |V_{THP}|)}{2} \qquad (3.28)$$

Discharge phase: Switches TG_{10}, TG_9 are closed, all other switches are open.

Equivalent circuit:

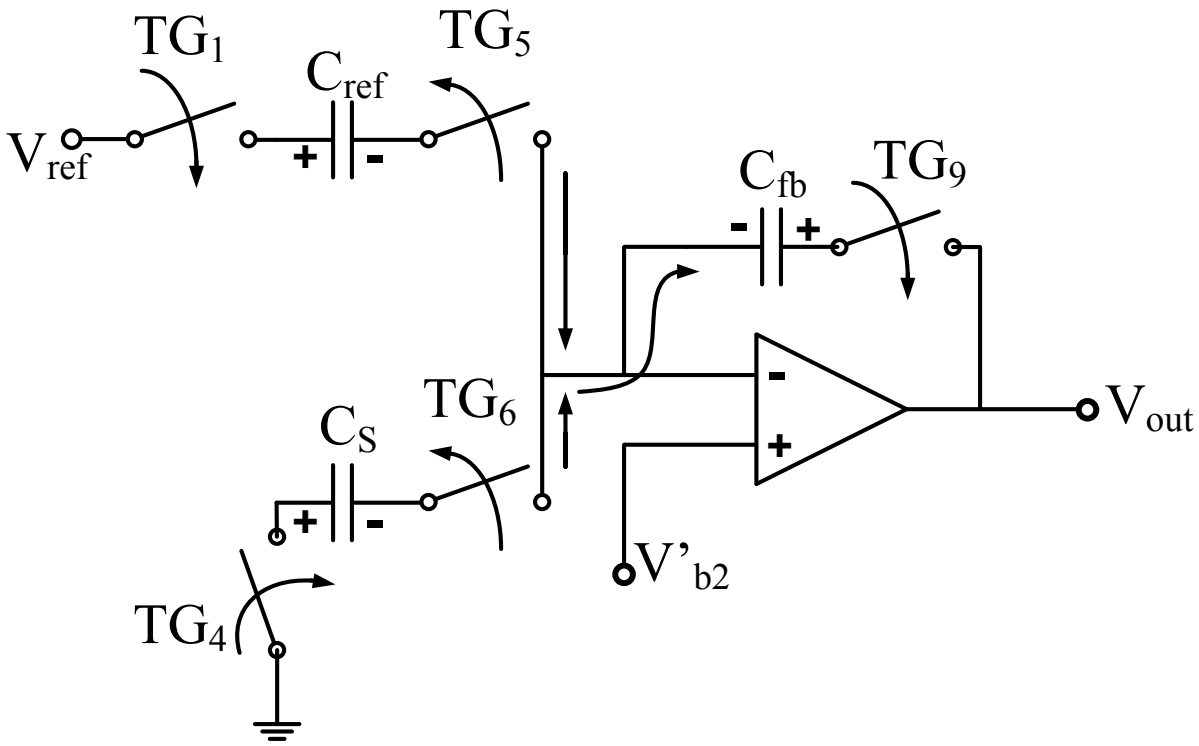


Fig 3.52 CDC discharge phase equivalent circuit- 1 – charge injection model

First, taking into account total charge injection from TG_5 and TG_6:

$$Q_{total} = \frac{Q_5}{2} + \frac{Q_6}{2}$$

$$= Cox.\ W.\ L.\ (2V'_{b2} - V_{DD} + V_{THN} - |V_{THP}|) \quad (3.29)$$

So, effect of calculated charge injection on feedback capacitor C_{fb}:

$$Q_{fb2} = Q_{fb1} - Q_{total}$$

$$= V_{ref} . C_x + V_{off1} . C_s + \frac{C_{ox} . W . L . [2V_{ref} - V_{DD} + V_{THN} - |V_{THP}|]}{2}$$

$$- Cox. W. L. (2V'_{b2} - V_{DD} + V_{THN} - |V_{THP}|) \quad (3.30)$$

At this time, consider TG_{10} is closed.

Equivalent circuit:

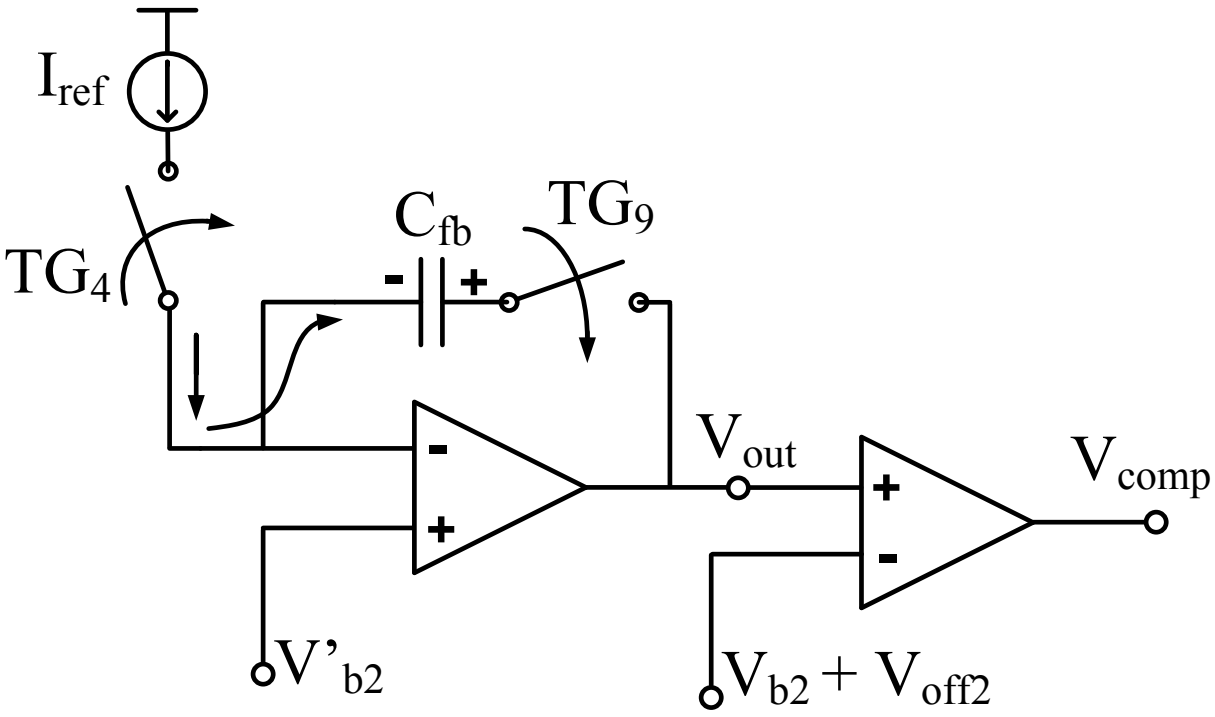


Fig 3.53 CDC discharge phase equivalent circuit 2 – charge injection model

Calculations:

$$V_{out} = V'_{b2} + \frac{Q_{fb2}}{C_{fb}} - \frac{1}{C_{fb}} \int_{T_1}^{T_2} I \, dt$$

$$= V'_{b2} + \frac{Q_{fb2}}{C_{fb}} - \frac{I}{C_{fb}} (T_2 - T_1) \quad (3.31)$$

Assume $T_1 = 0$ and T_2 when $V_{out} = V_{b2} + V_{off2}$

Where, V_{off2} is the offset of the comparator op amp.

Thus, $T_2 = -(V_{out} - V'_{b2} + \frac{Q_{fb2}}{C_{fb}}) \cdot \frac{C_{fb}}{I}$

$$= -(V_{b2} + V_{off2} - V_{b2} - V_{off1} - \frac{Q_{fb2}}{C_{fb}}) \cdot \frac{C_{fb}}{I}$$

$$= \frac{(V_{off1} - V_{off2})C_{fb}}{I} + \frac{Q_{fb2}}{I} \quad (3.32)$$

For simplification of calculation if the following conditions are considered:

$$V_{THN} \cong |V_{THP}| \text{ and } 2V_{b2} = V_{DD} \text{ and } V_{ref} = V_{DD}$$

Then, the total time taken for capacitance to digital conversion can be expressed as:

$$T_2 = \frac{V_{ref}.C_x}{I} + \frac{V_{off1}.C_s}{I} + \frac{C_{ox}.W.L.V_{ref}}{2.I} - \frac{C_{ox}W.L.2.V_{off1}}{I} + \frac{(V_{off1} - V_{off2})C_{fb}}{I} \quad (3.33)$$

Where, I is the supplied current from the current source.

Equation 3.33 shows the time equivalent of the capacitance taking into account the charge injection and opamp offset.

3.12 Clock Extractor:

The clock extractor circuit is responsible for the master clock generation for the digital block. The clock extractor circuit is designed using an inverter chain containing three inverters as shown in Fig. 3.54. The first inverter branch prevents the transponder antenna from being loaded by the internal circuitry. The effect is cascaded by the third branch as well which separates the internal circuitry from the transponder antenna. The second inverter branch inverts the signal coming from the first inverter. The in-coming RF wave is inverted multiple times to achieve a clock pulse of the same frequency, which can be later converted into required frequencies by the use of frequency dividers. The schematic simulation of the clock extractor involves the RF input of 13.56 MHz to the RF IN pin and the clock pulse is observed at the CLK OUT pin which can be seen Fig 5.55.

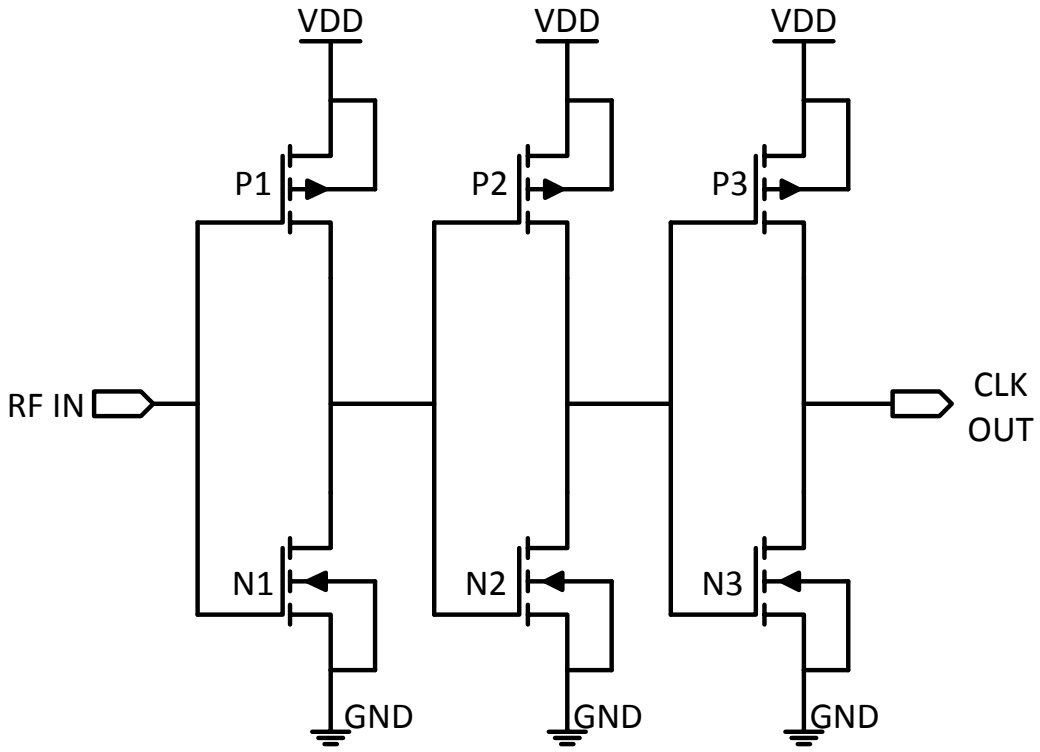


Fig 3.54 Clock extractor schematic

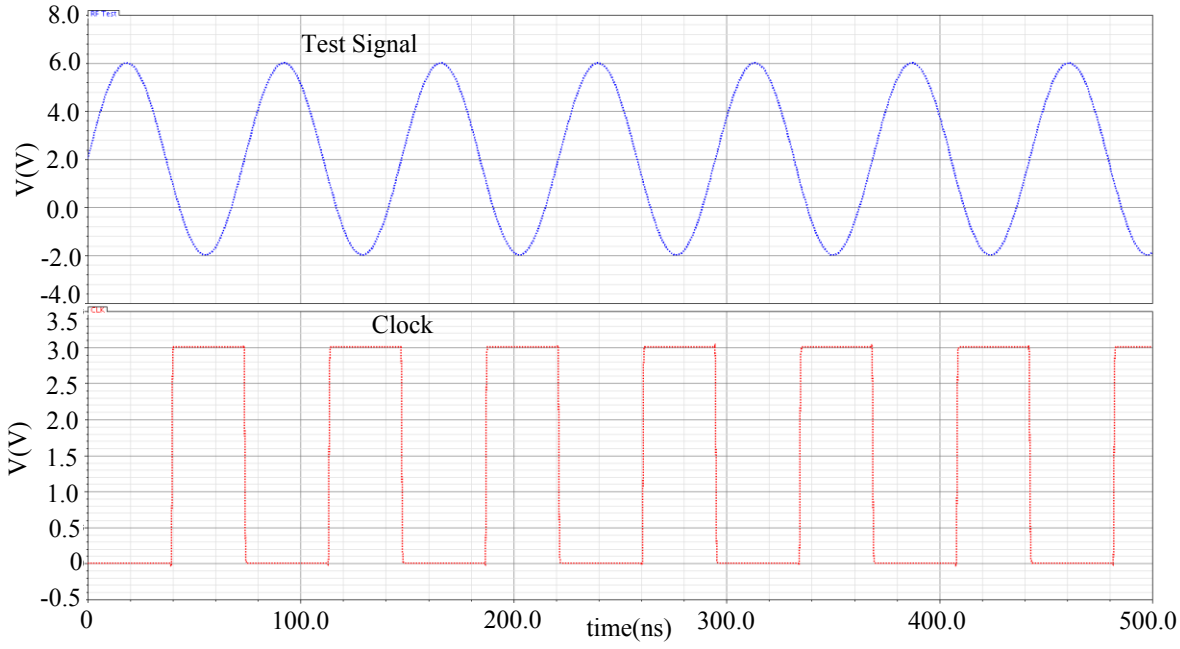


Fig 3.55 Clock extractor schematic simulation

Table 3.10 Transistor sizes of cock extractor

Transistor	W	L
P1	13.5 µm	600 nm
P2	40.5 µm	600 nm
P3	121.5 µm	600 nm
N1	4.5 µm	600 nm
N2	13.5 µm	600 nm
N3	40.5 µm	600 nm

The transistor sizes of the clock extractor schematic are given in Table 3.10.

3.13 Modulator and Demodulator:

Both the modulator and demodulator circuits are designed in collaboration with my colleague H.S. Kumar Swamy. In this section the schematic of both the circuits are shown. The modulator performs load modulation and consists of a single-large NMOS transistor. The RF signal is fed to the drain of N1 and the control signal is provided to the gate of the transistor. When the gate is high a dip in voltage of the applied RF waveform is observed showing load modulation is performed. The control signal can be an encoded digital signal from the digital core. The schematic of the modulator is shown in Fig. 3.56. The simulated waveform is shown in Fig 3.57. The transistor size of N1 is given in Table 3.11.

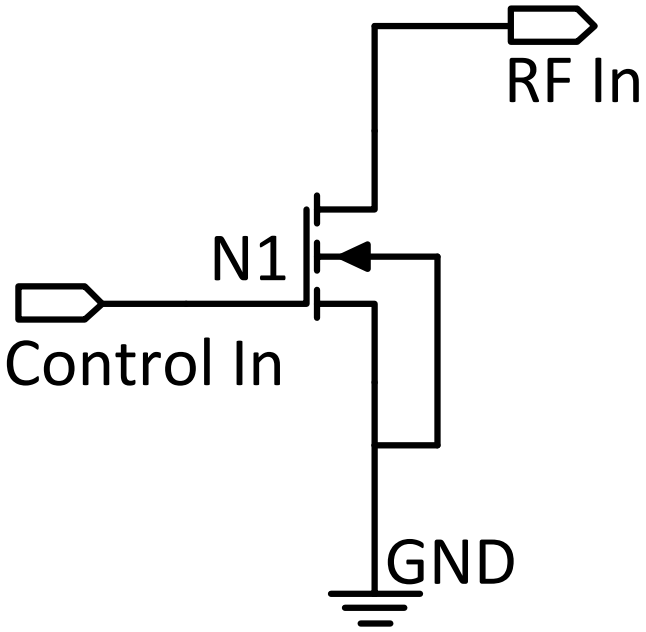


Fig 3.56 Modulator schematic

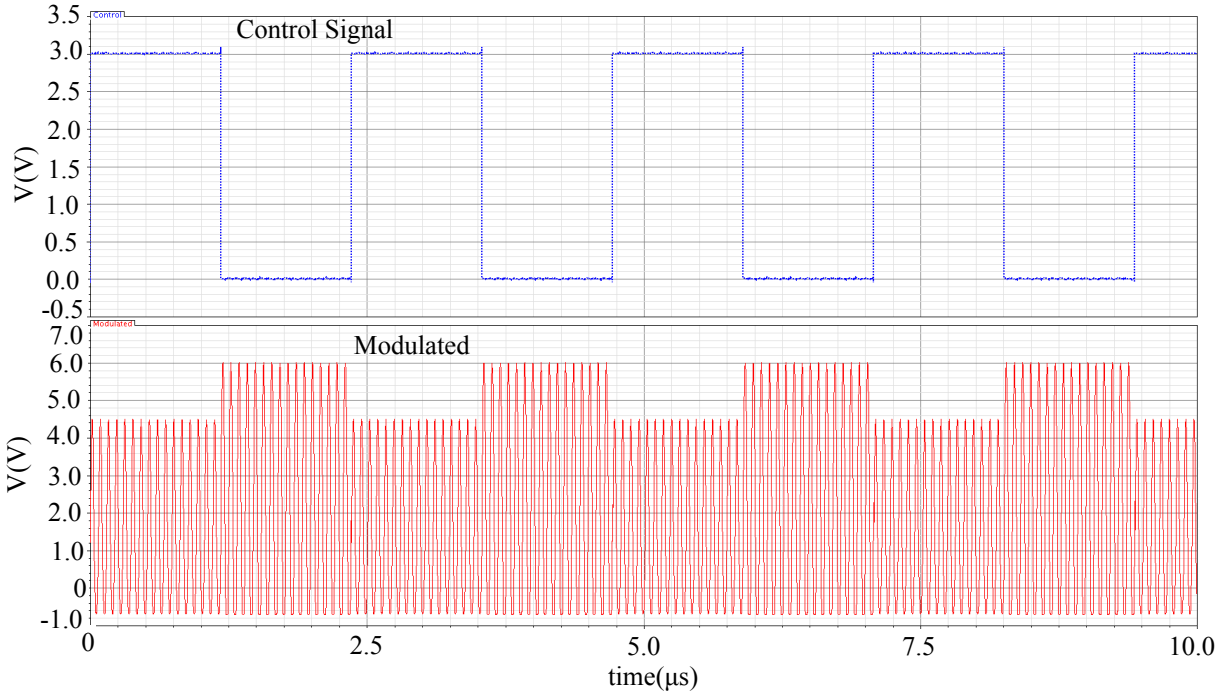


Fig 3.57 Modulator schematic output waveform

Table 3.11 Transistor size of modulator

Transistor	W	L
N1	60 µm	600 nm

The demodulator schematic is shown in Fig 3.58. The in-coming RF signal which contains encoded data is fed to an envelope detector. The envelop detector consists of a diode which removes the modulation envelope and it is fed to the input of the demodulator. The demodulator consists of a voltage divider circuit and a large capacitor C1. Due to large sized resistor R1 and R2, the capacitor charges very slowly. R3 and C2 form the matching network for the external transponder antenna. The op-amp used is the same as the one used in the CDC. The op-amp is used to detect the bits in the in-coming RF transmission. A clear bit is produced at Demod Out pin when the voltage across the capacitor C1 which is given to the positive input of the op-amp is greater than the negative input.

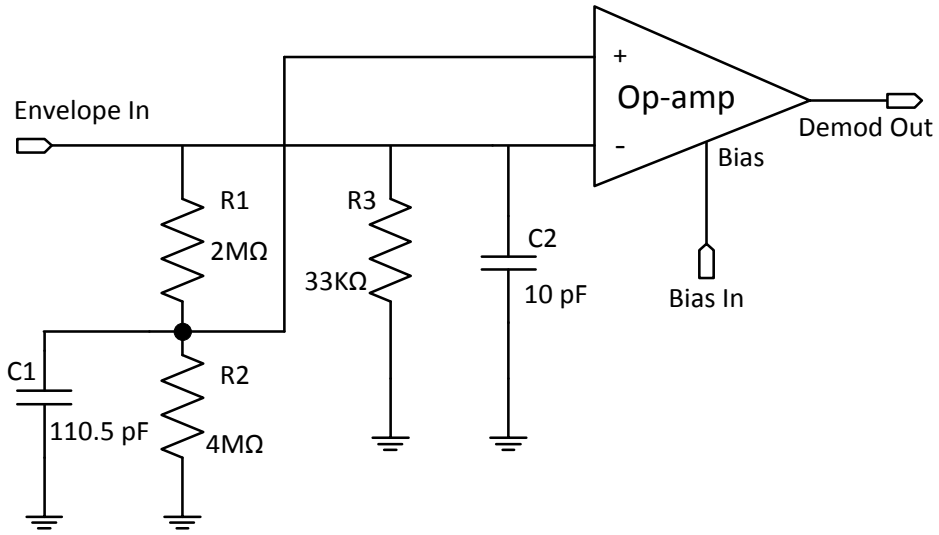


Fig 3.58 De-modulator schematic

3.14 Conclusion:

The analog blocks have been explained in detail. The following chapter discusses about the layout of the analog core. The entire layout and total current consumption is shown and the final chip is also shown.

CHAPTER 4

RESULTS

4.1 Introduction

In this chapter the results of the entire analog core are discussed. The layout of each analog block is shown along with all the post-layout simulations. The layouts were designed using the NCSU kit with a 0.6 µm CMOS target process.

4.2 RF Rectifier

The RF rectifier layout is shows in Fig 4.1. The layout of the PMOS and NMOS transistors have been broken down into multiple number of fingers and guard rings have been placed to reduce effect of etching. The whole layout is surrounded by guard rings of ground connectivity for better substrate connection. Voltage and current simulations are shown in Fig 4.2 and 4.3 respectively. The layout measures 96.3 µm x 89.7 µm.

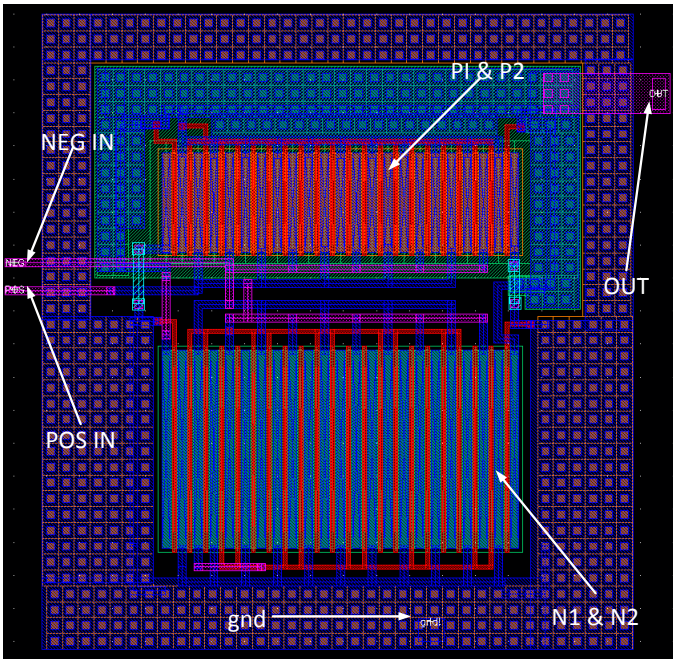


Fig 4.1 RF Rectifier layout

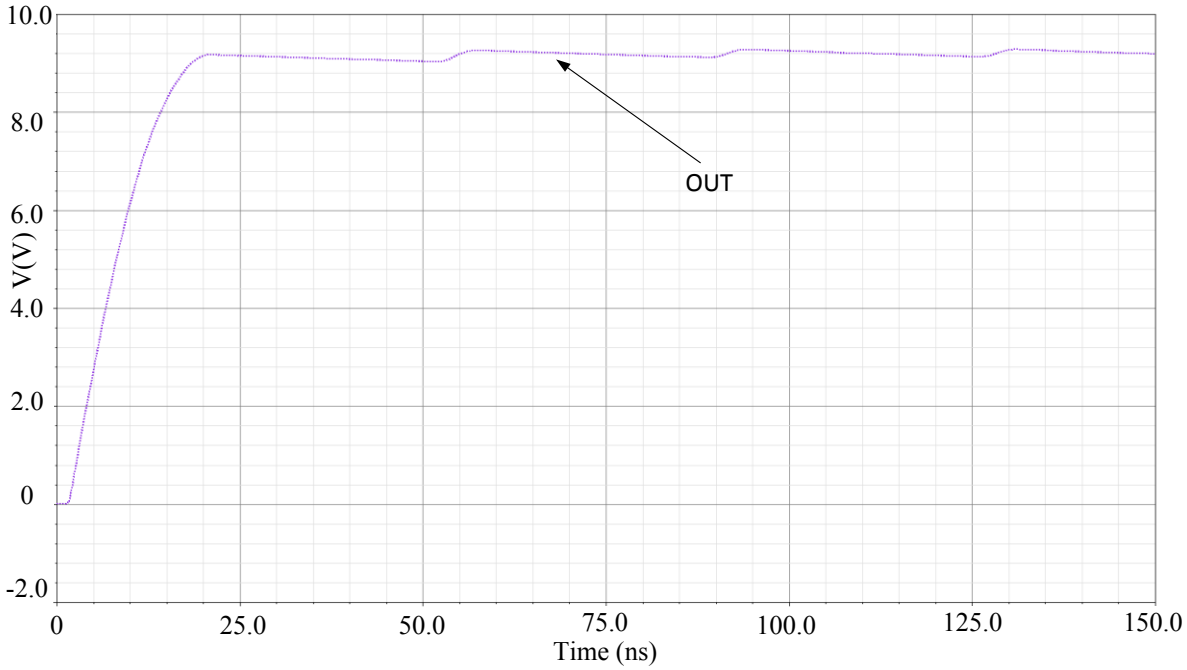


Fig 4.2 RF Rectifier post-layout voltage

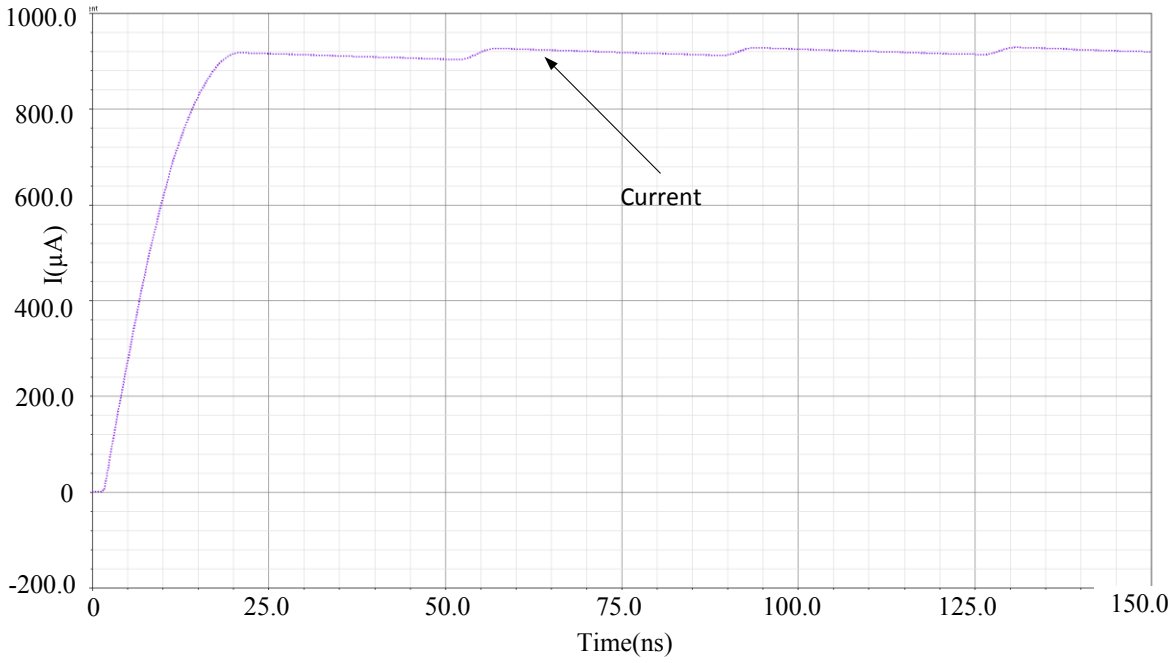


Fig 4.3 RF Rectifier post-layout output current

4.3 RF Limiter

The layout of the RF limiter is shown in Fig. 4.4. Same methodologies are used in the layout of this as of the earlier layout. The resistor layout is made in serpentine form. The layout measures 79.8 µm x 132.3 µm. The output voltage simulation of the RF Limiter is shown in Fig. 4.5.

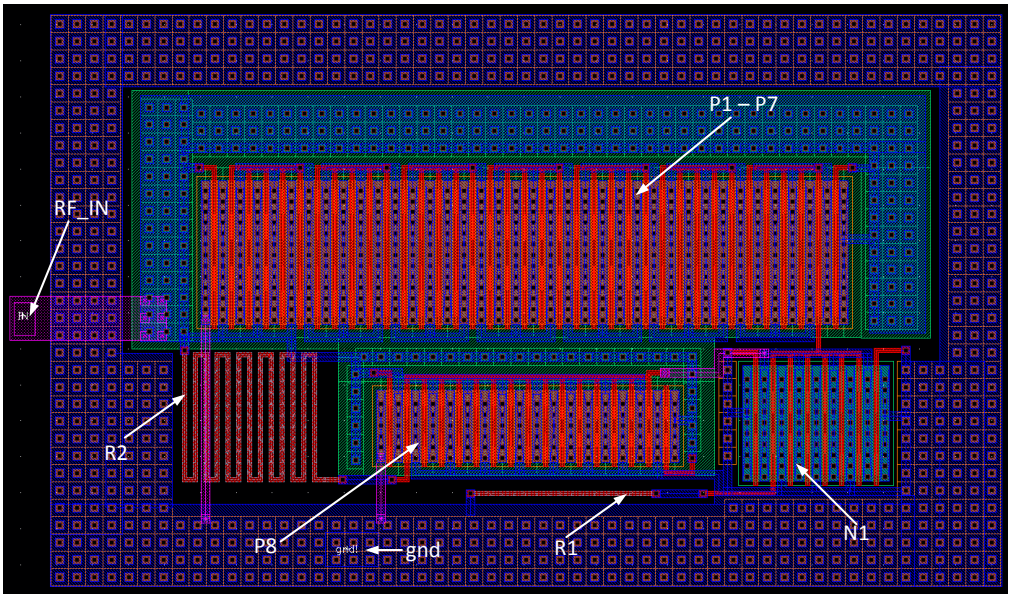


Fig 4.4 RF Limiter layout

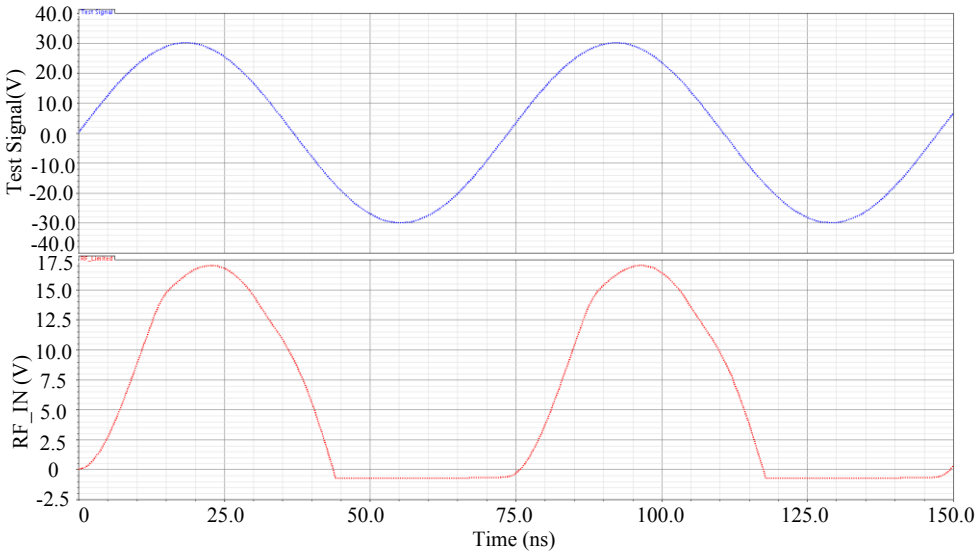


Fig 4.5 RF Limiter post-layout voltage

The output current and voltage simulation of the RF rectifier, post RF limiter is shown in Fig. 4.6 and 4.7 respectively.

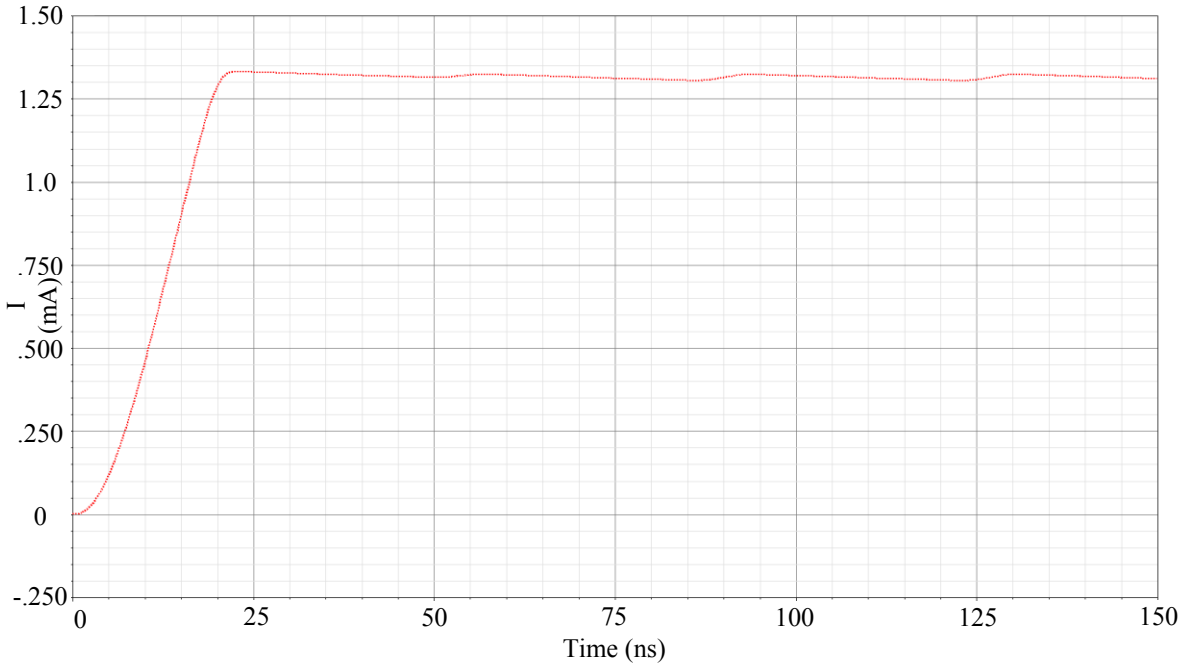


Fig 4.6 RF Limiter post-layout current

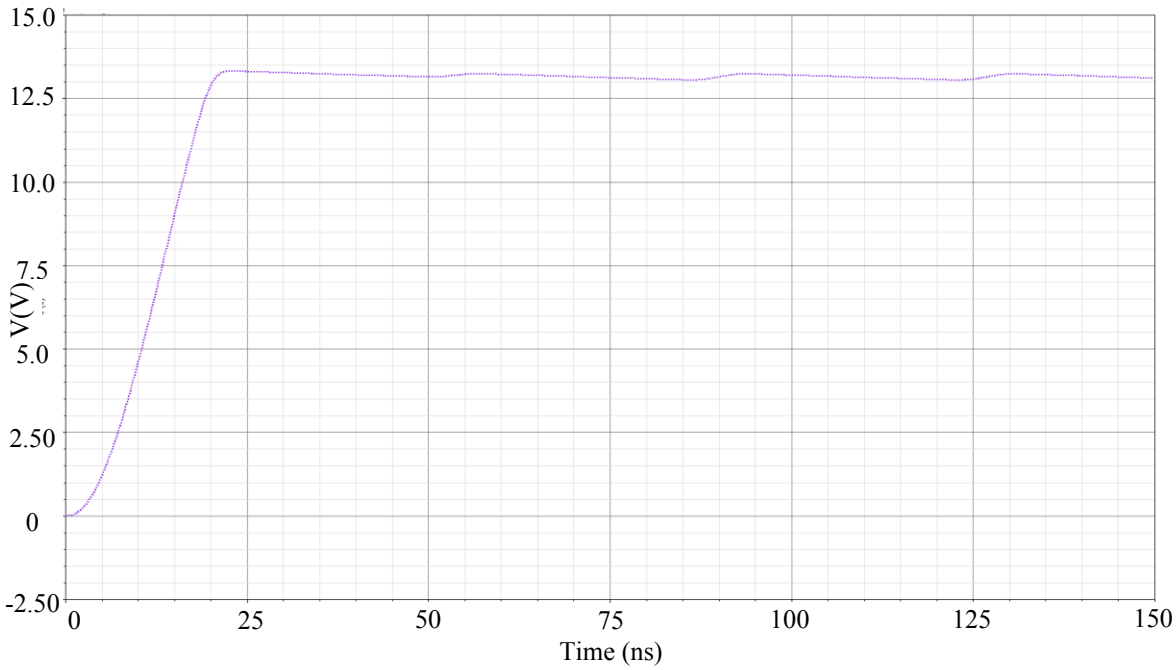


Fig 4.7 RF Limiter post-layout voltage

4.4 Power-on-Reset

The power-on-reset layout is shown in Fig. 4.8. The test signal and output voltage simulations are shown in Fig 4.9. The layout measures 72.750 µm x 157.65 µm.

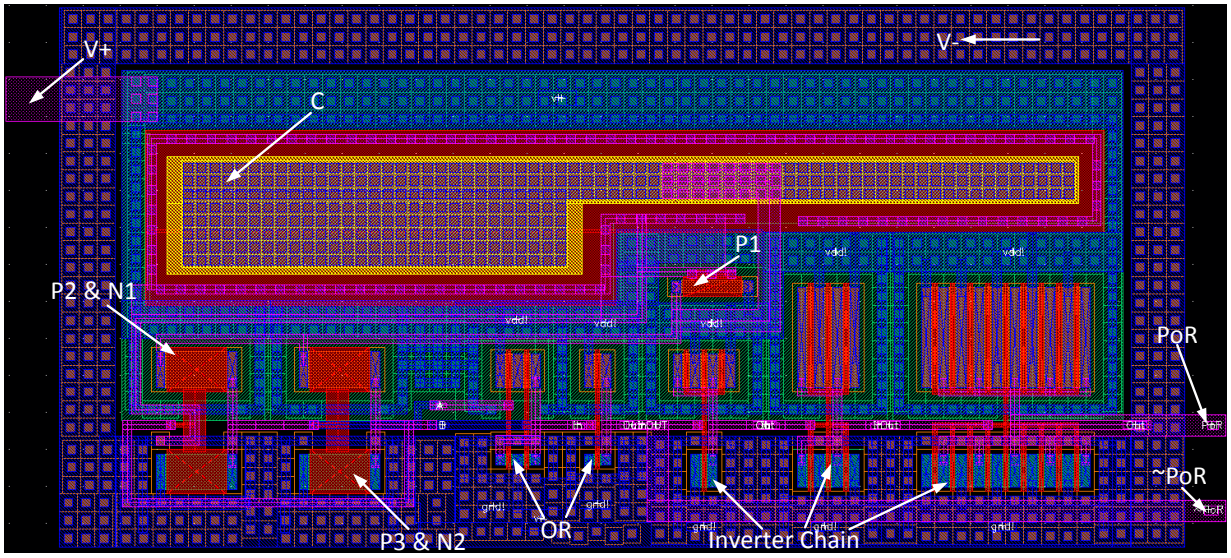


Fig 4.8 Power-on-reset layout

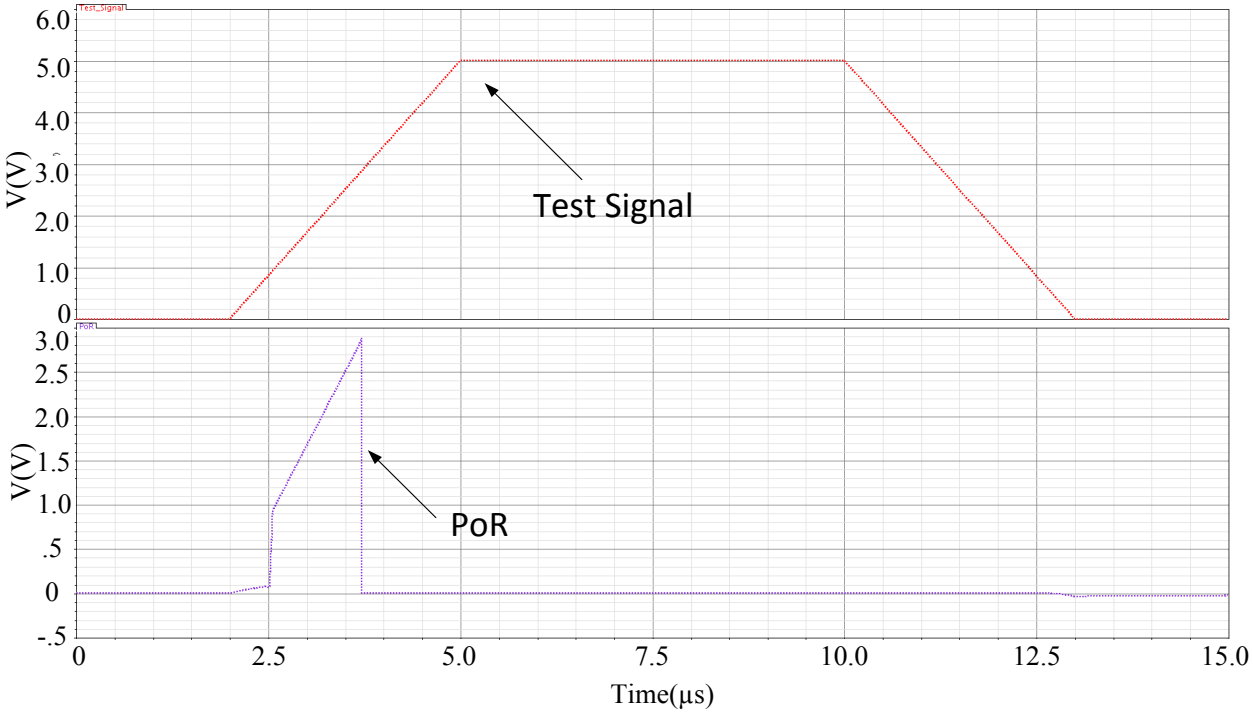


Fig 4.9 Power-on-reset post-layout voltage

4.5 Low-Drop-Out Voltage Regulator

Two LDOs have been constructed. The first one, does not include the feed-back resistors and thus, can be used to provide any required voltage level by using external resistors. This is done to increase the flexibility in LDO output-voltage configuration. The second layout includes the feed-back resistor and corresponds to the schematic design.

4.5.1 LDO 1

The layout of the low-drop-out voltage regulator without the feed-back resistors is shown in Fig. 4.10. The layout measures 295.200 µm x 341.850 µm.

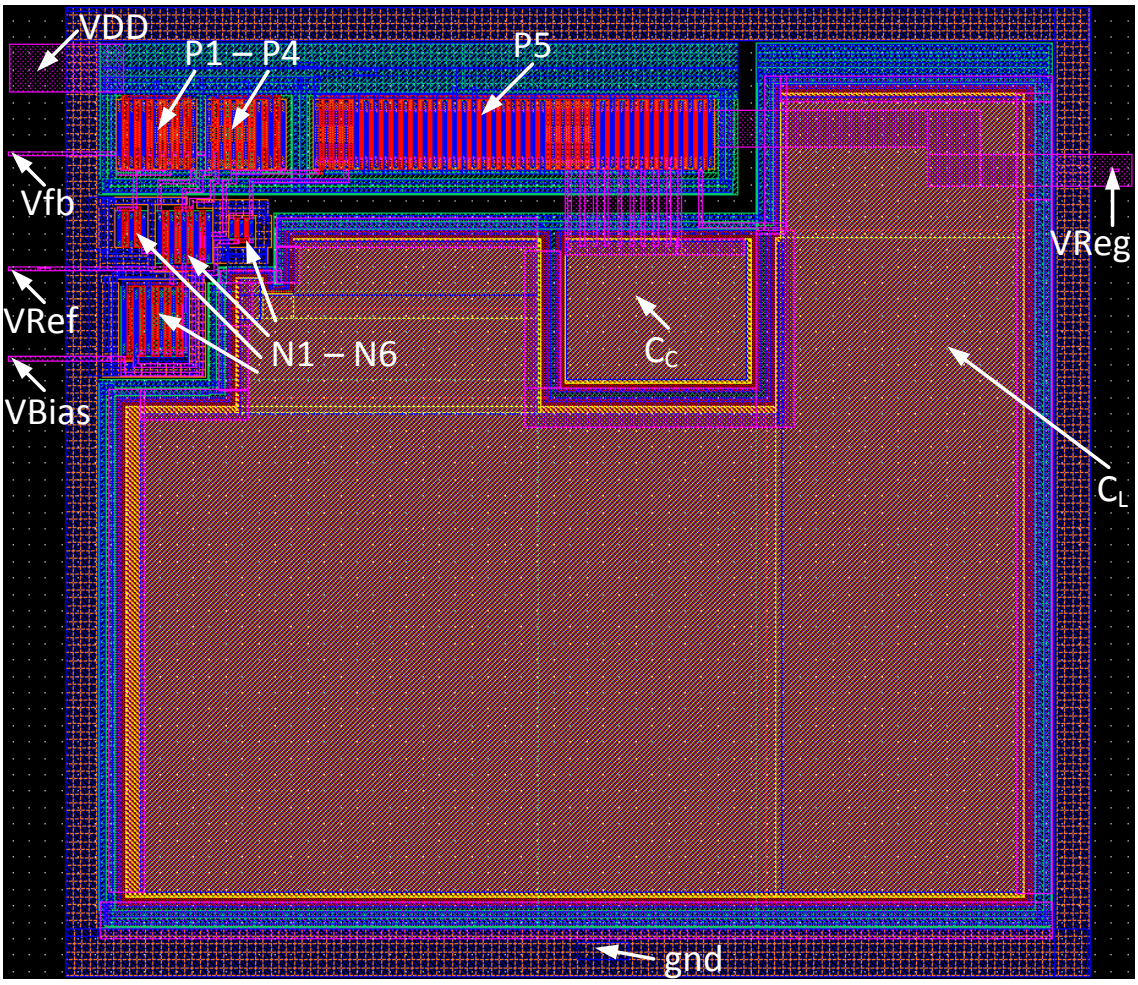


Fig 4.10 Low-drop-out voltage regulator 1 layout

4.5.2 Low-drop-out voltage regulator 2

The layout of the low-drop-out voltage regulator is shown in Fig. 4.11. This layout is made with the resistors for the feed-back voltage for fixed output-voltage purposes. The layout measures 297 µm x 342.150 µm.

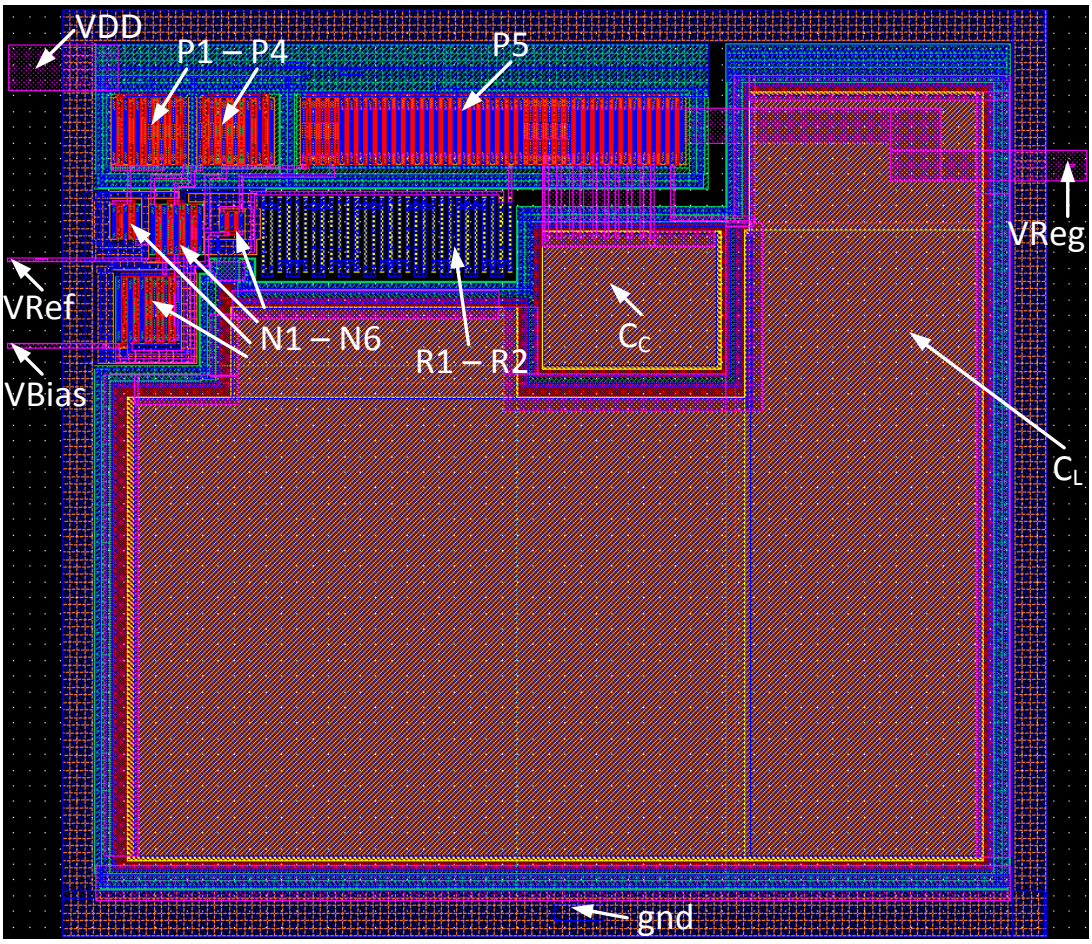


Fig 4.11 Low-drop-out voltage regulator 2 layout

The post layout simulations of the re-configurable LDO1 with same R1 and R2 value as the schematic is shown in Fig 4.12. Post layout simulation of the LDO2 is shown in Fig. 4.13. Both the post-layout and pre-layout simulations match, showing the layouts are operational.

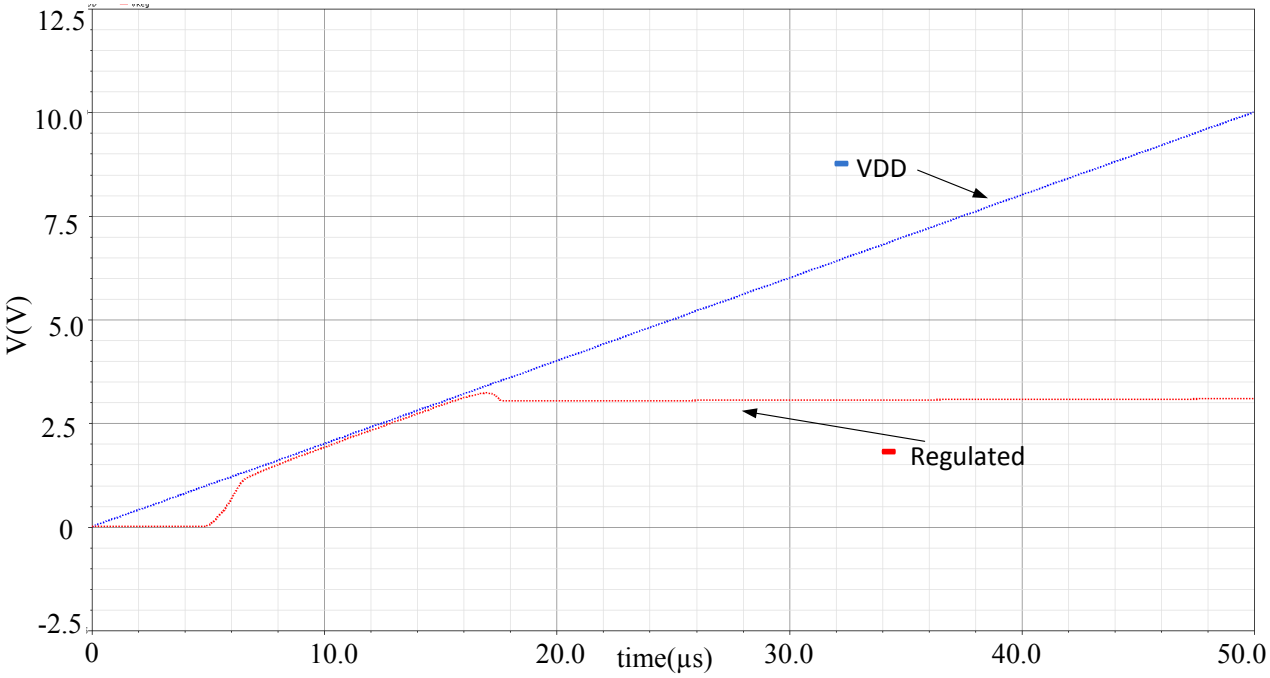


Fig 4.12 LDO 1 post-layout output voltage simulation

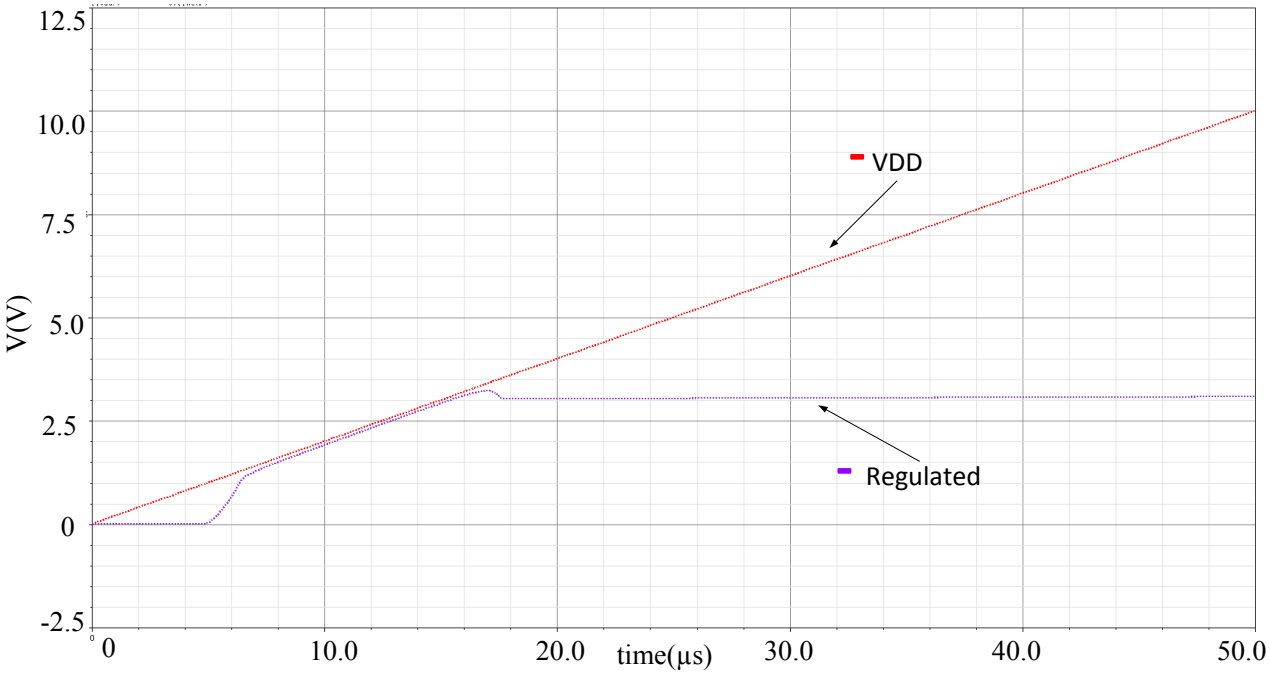


Fig 4.13 LDO 2 post-layout output voltage simulation

4.6 Master bias voltage reference

The layout of the master bias voltage reference is shown in Fig. 4.14. The layout measures 315.450 µm x 306.150 µm.

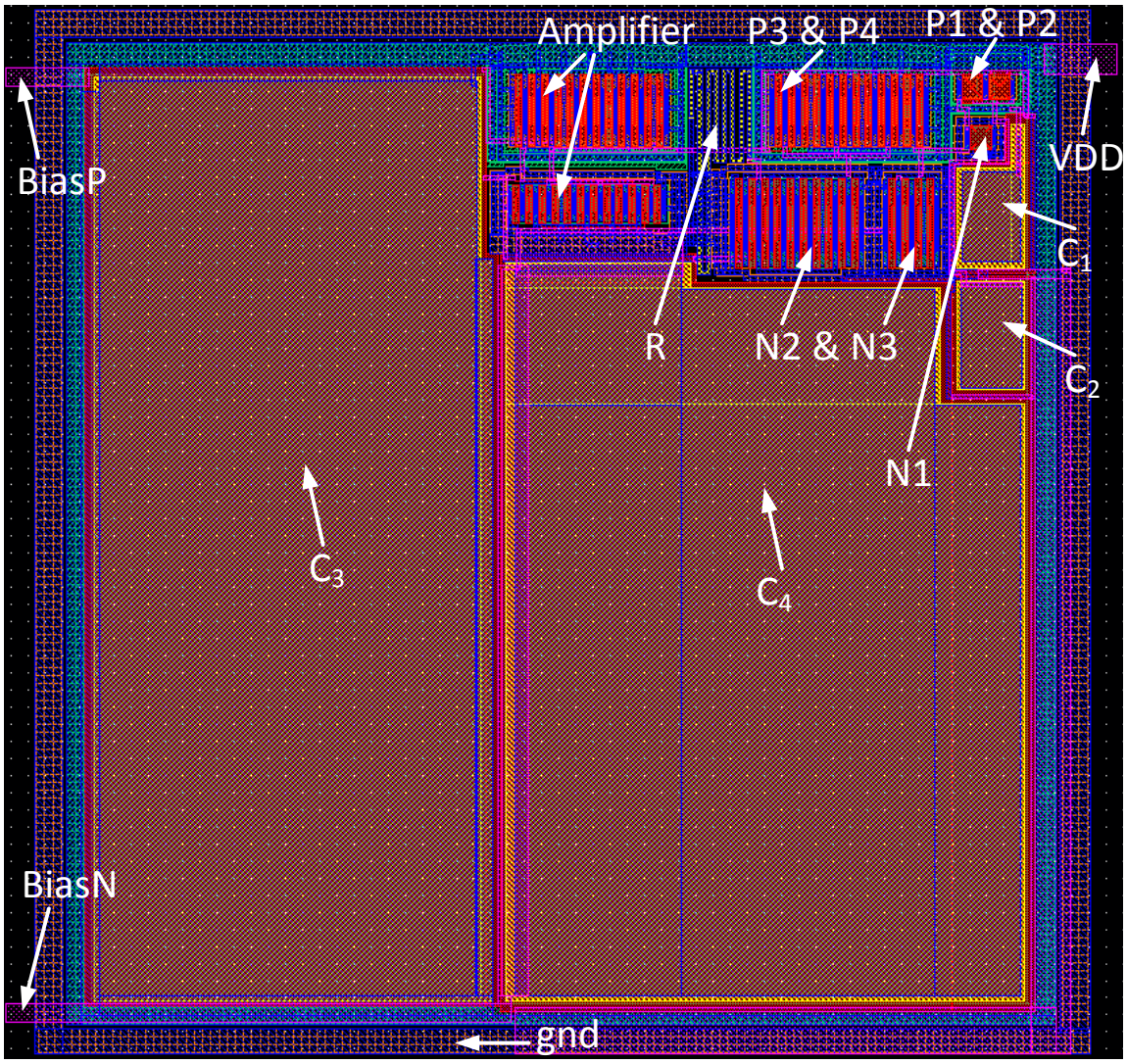


Fig 4.14 Master-bias voltage reference generator layout

The post-layout output voltage simulations are shown in Fig 4.15. This simulation matches with the pre-layout schematic simulation, showing the layout is operational. The current consumption is shown in Fig. 4.16.

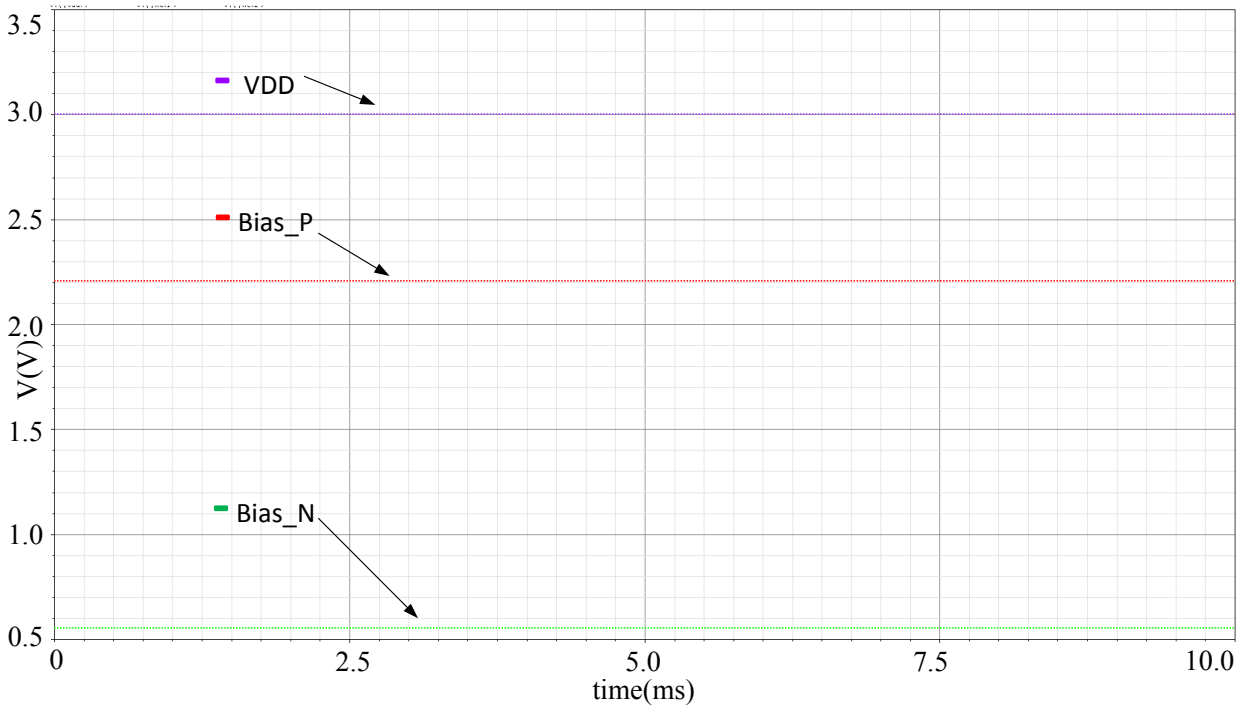


Fig. 4.15 Master-Bias Post-layout output voltage simulation

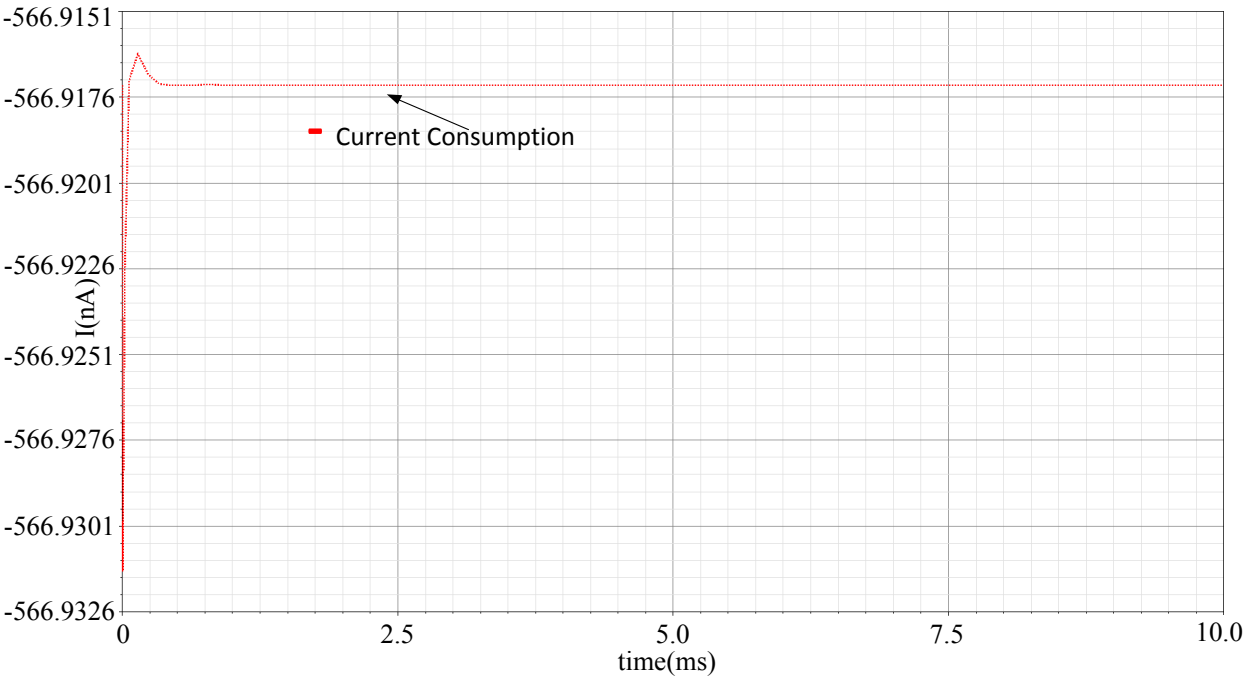


Fig. 4.16 Master-Bias Post-layout current consumption

4.7 Voltage reference 1

The layout of the voltage reference 1 circuit is shown in Fig. 4.13. The layout measures 98.550 µm x 74.400 µm.

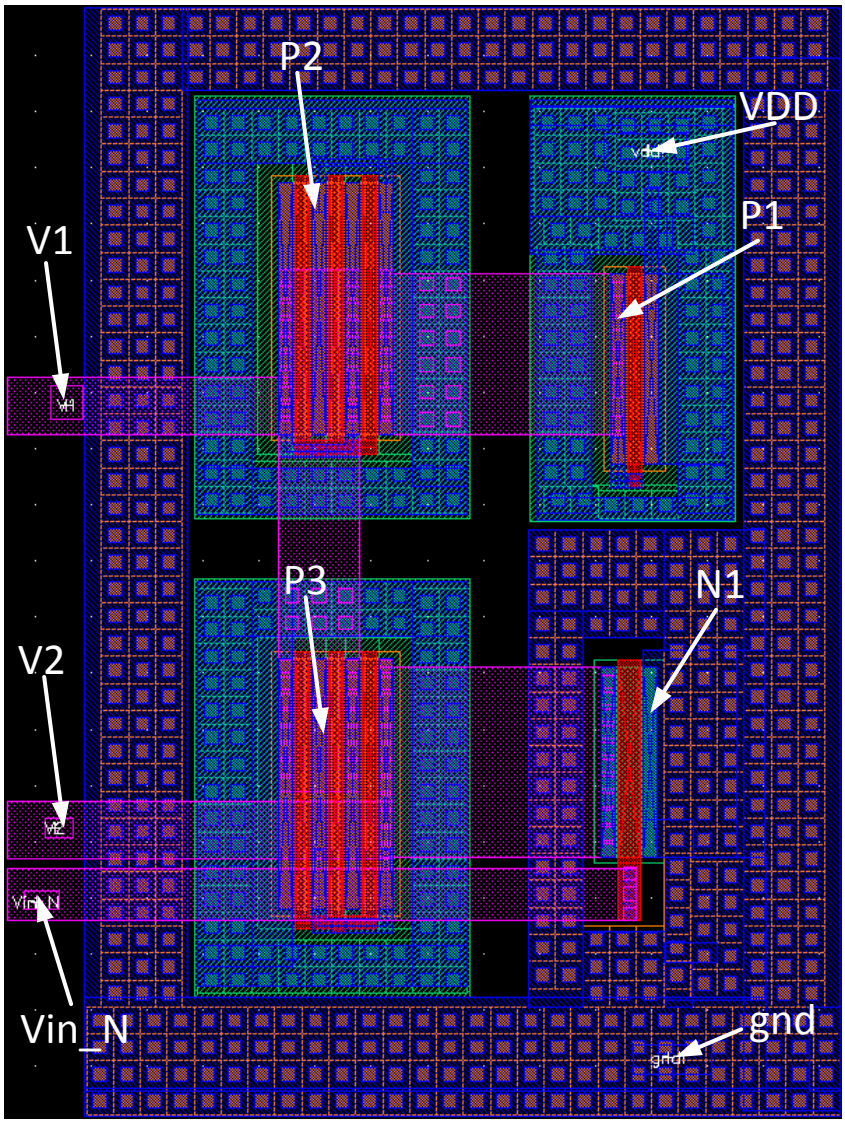


Fig 4.17 Voltage reference 1 layout

The post-layout output voltage simulation is shown in Fig 4.18, confirming a functional layout construction.

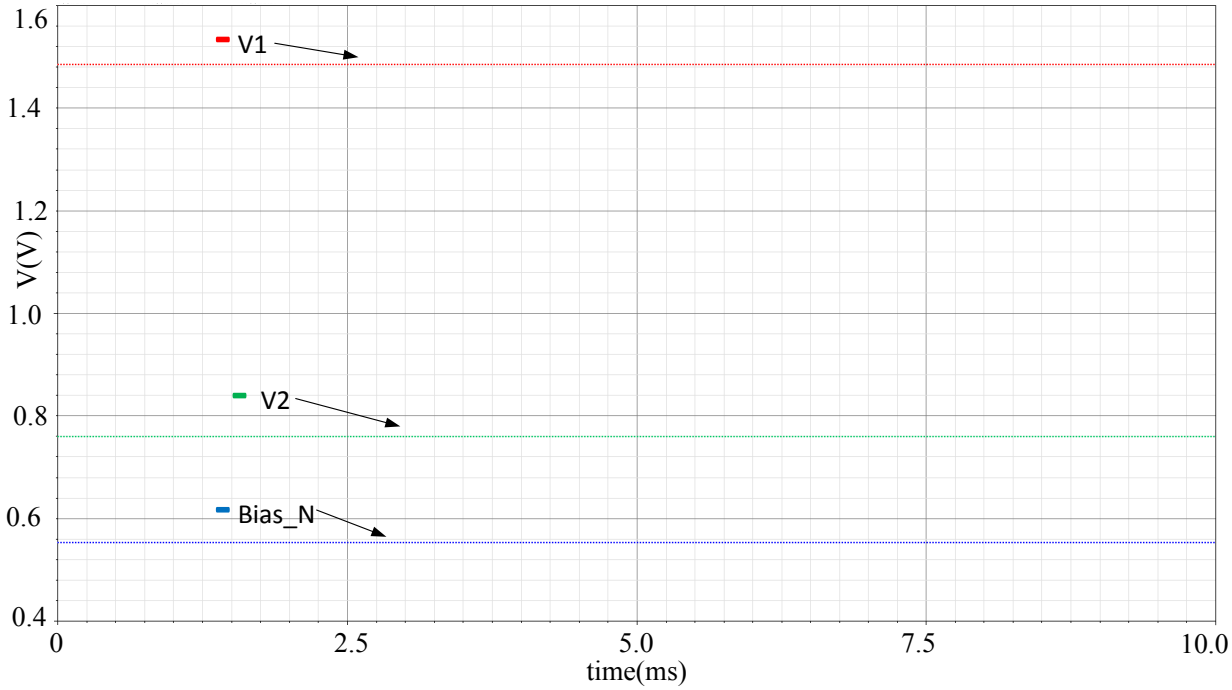


Fig 4.18 Voltage reference 1 post-layout output voltage simulation

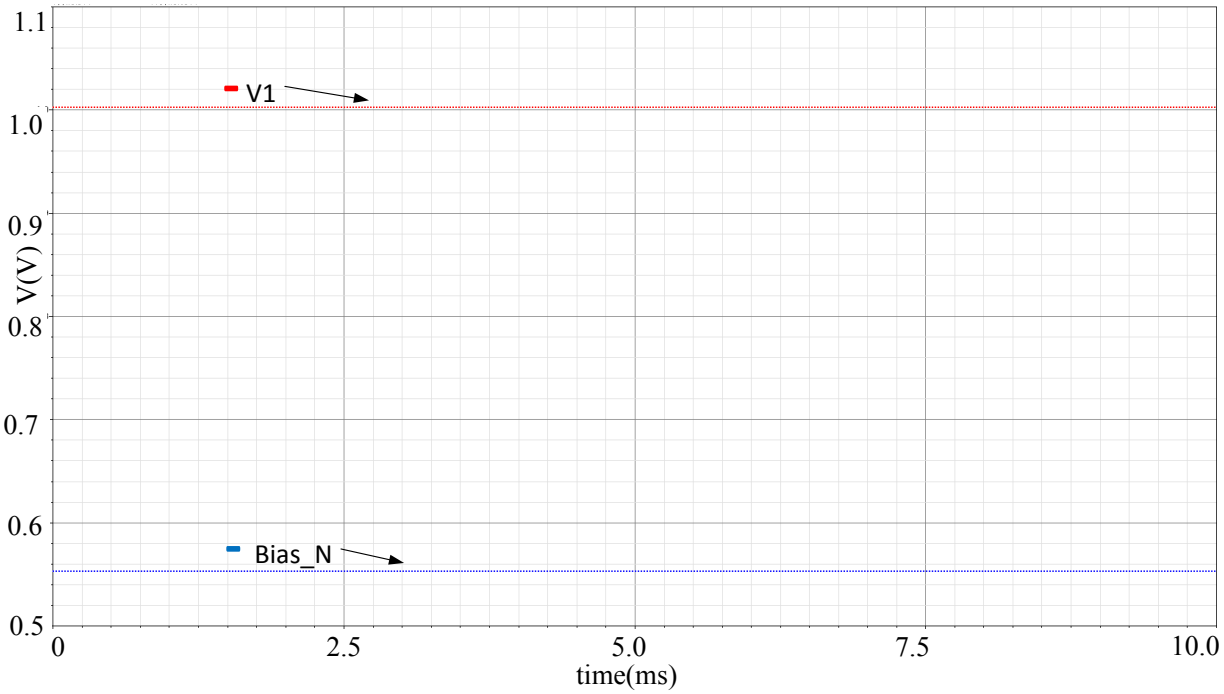


Fig 4.19 Voltage reference 2 post-layout output voltage simulation

4.8 Voltage reference 2

The layout of the voltage reference 2 circuit is shown in Fig. 4.20. The layout measures 65.250 µm x 66.30 µm.

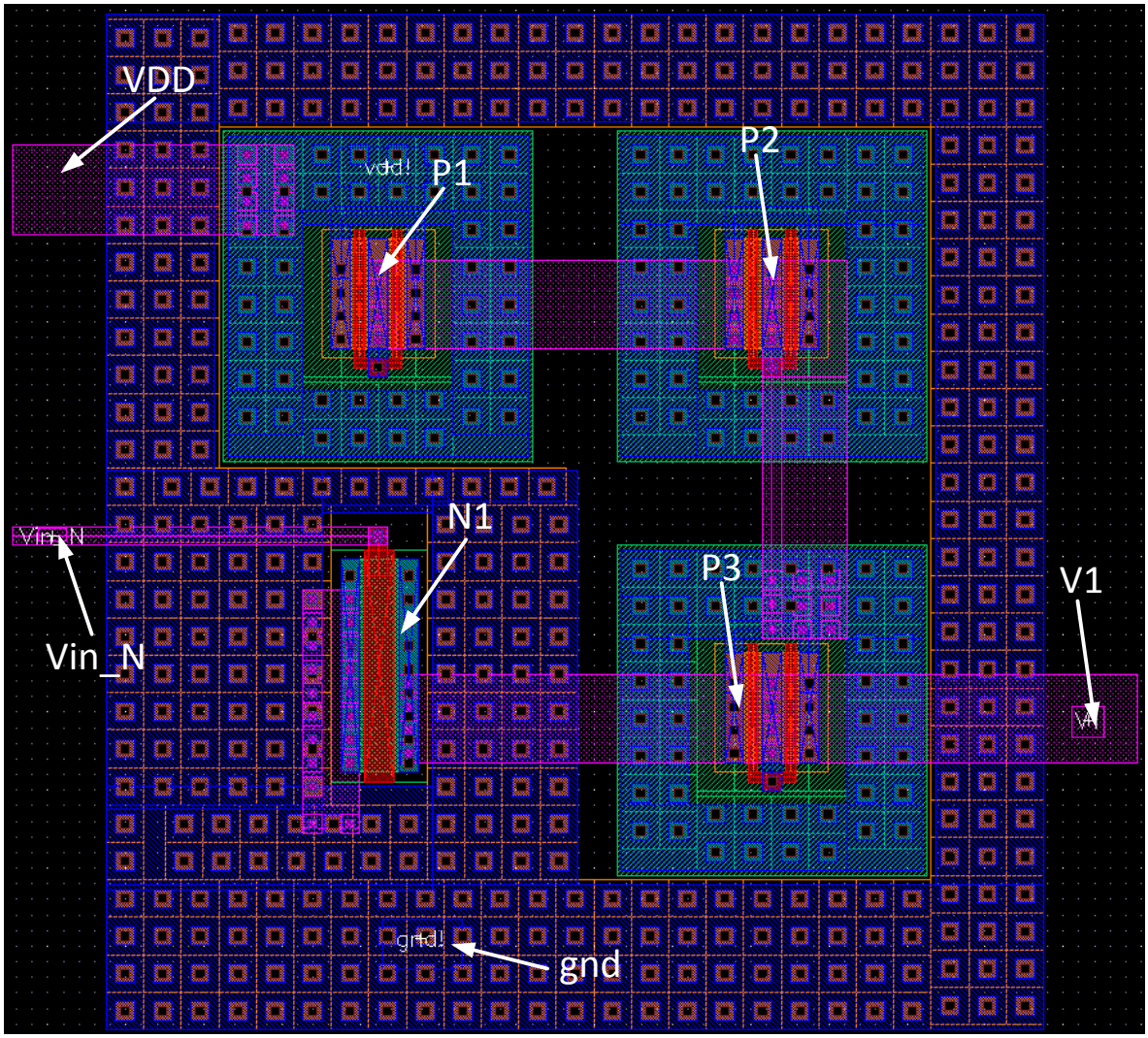


Fig 4.20 Voltage reference 2 layout

The post-layout output voltage simulation is shown in Fig 4.19, confirming a functional layout construction.

4.9 Wide-swing current source

The layout of the wide swing current source is shown in Fig. 4.21. The layout measures 89.850 µm x 74.40 µm. The post-layout output current simulation is shown in Fig 4.22, confirming a functional layout construction

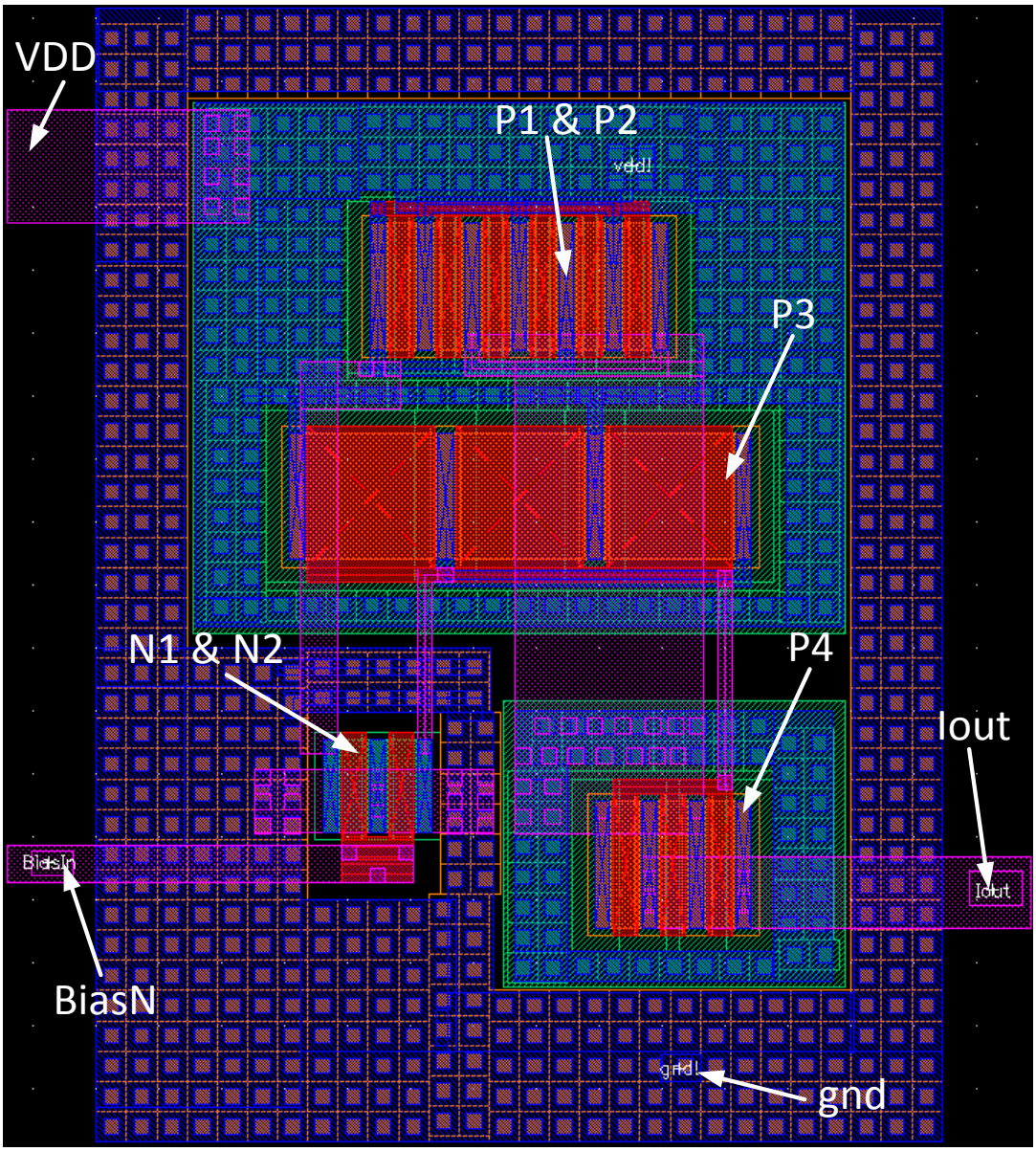


Fig 4.21 Wide-swing current source layout

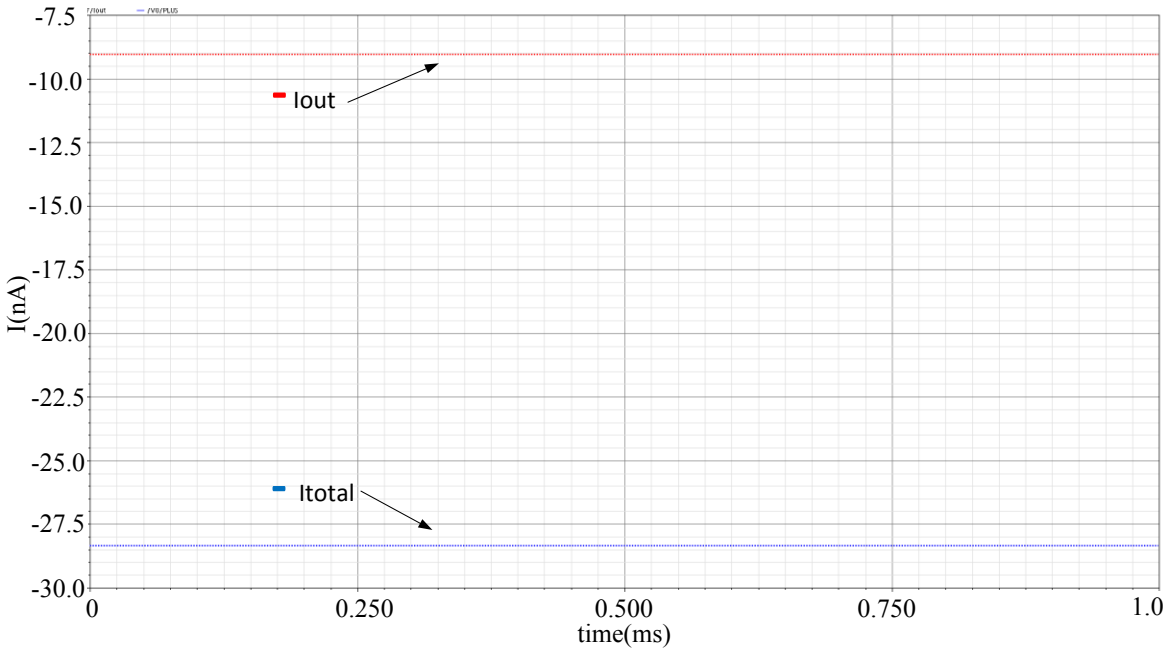


Fig 4.22 Wide-swing current source post-layout output current simulation

4.10 Capacitance to digital converter

The layout of the capacitance to digital converter is shown in Fig. 4.23. Post-layout simulations of test values of C_S = 6.2 pF and 5.8 pF are shown in Fig 4.24 and Fig 4.25 respectively, confirming the functionality of the layout construction. . The layout measures 500 µm x 123.75 µm.

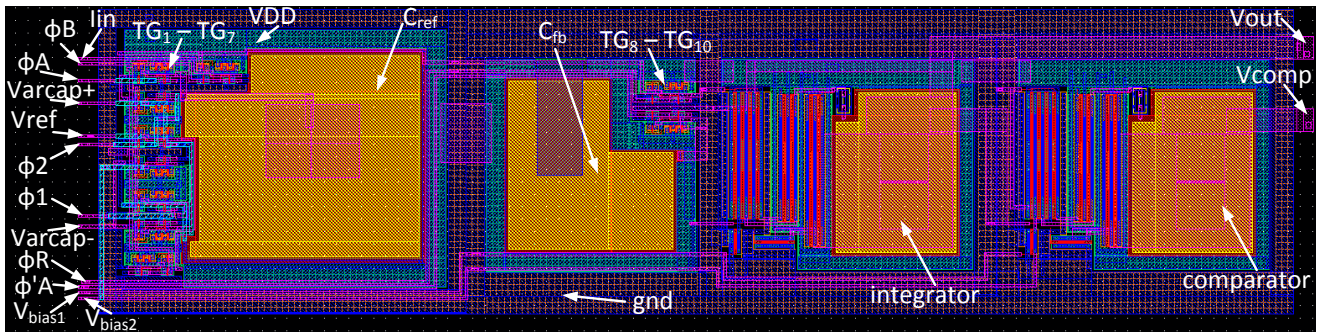


Fig 4.23 Capacitance to digital converter layout

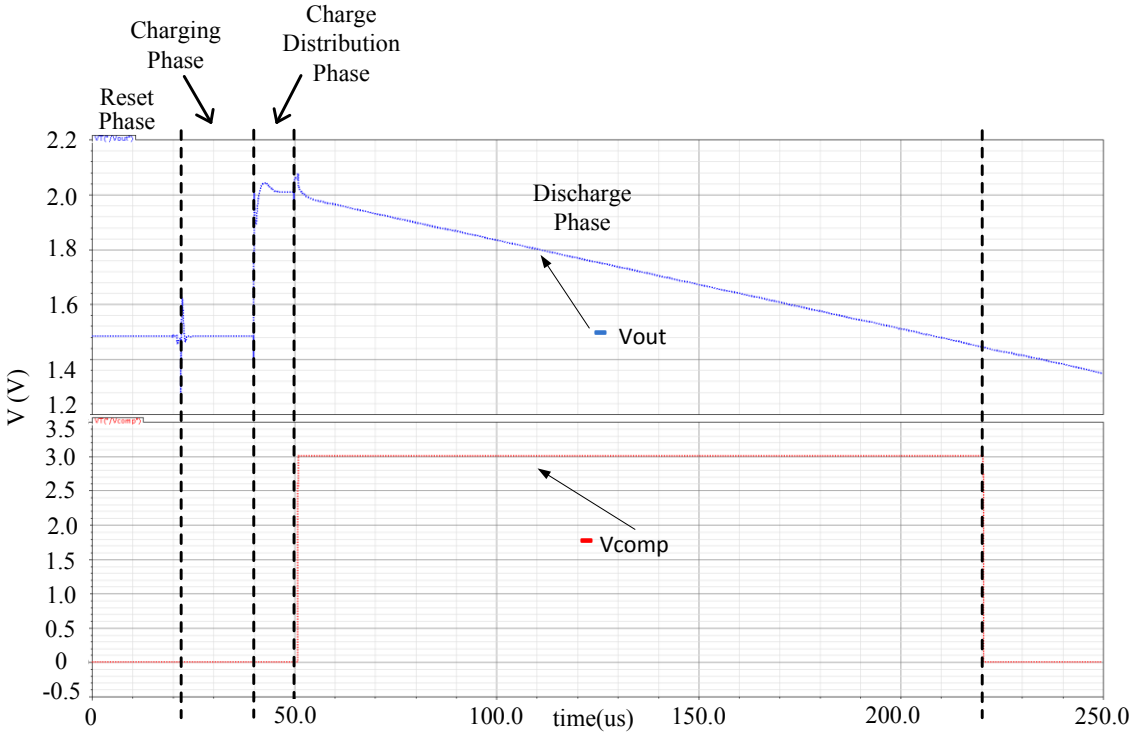


Fig 4.24 Capacitance to digital converter post-layout simulation for C_S = 6.2 pF

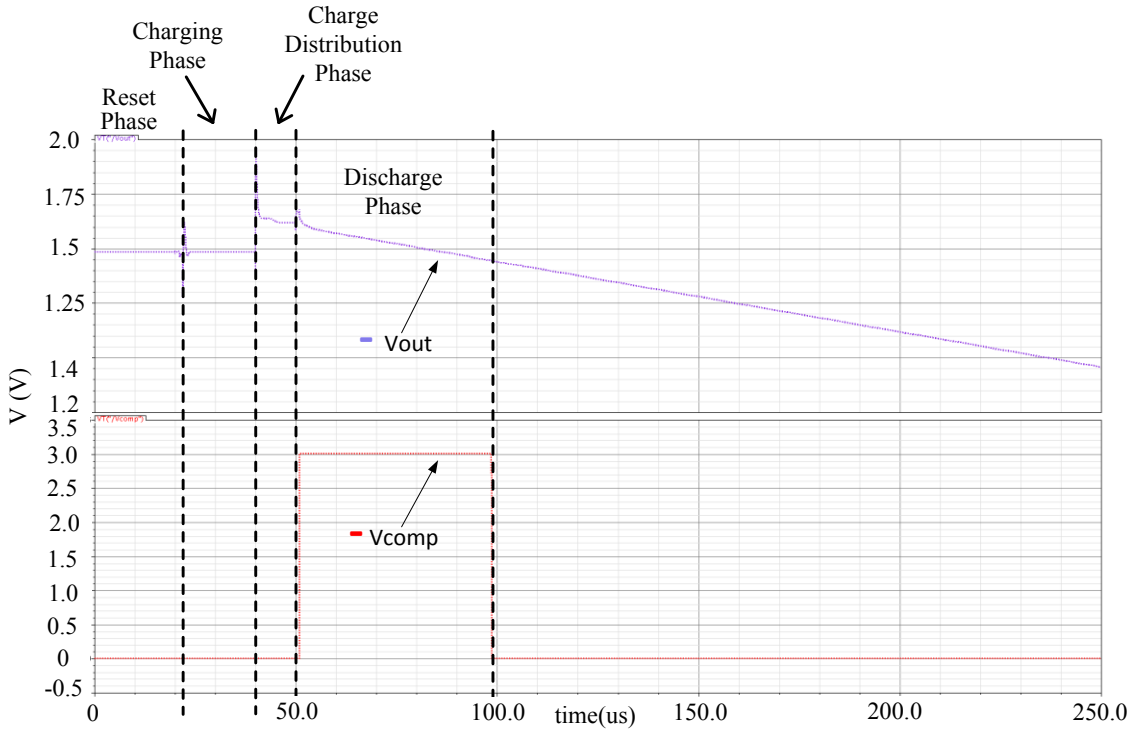


Fig 4.25 Capacitance to digital converter post-layout simulation for C_S = 5.8 pF

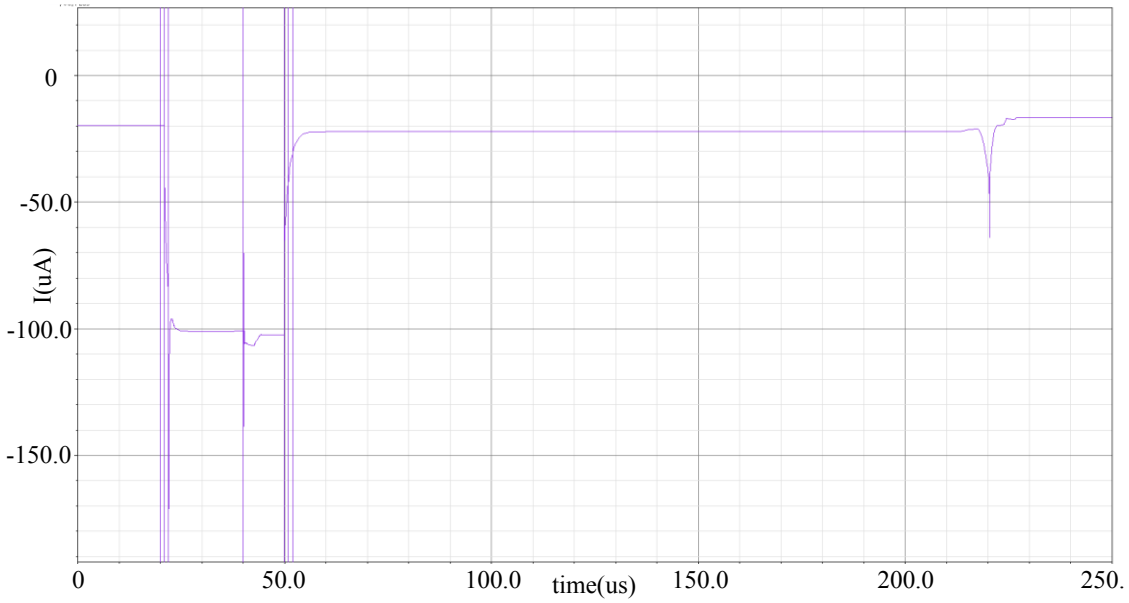


Fig 4.26 Total current consumption of the CDC

The total current consumption of the CDC is shown in Fig 4.26 and noted at 30.1 µA.

Analog Buffer:

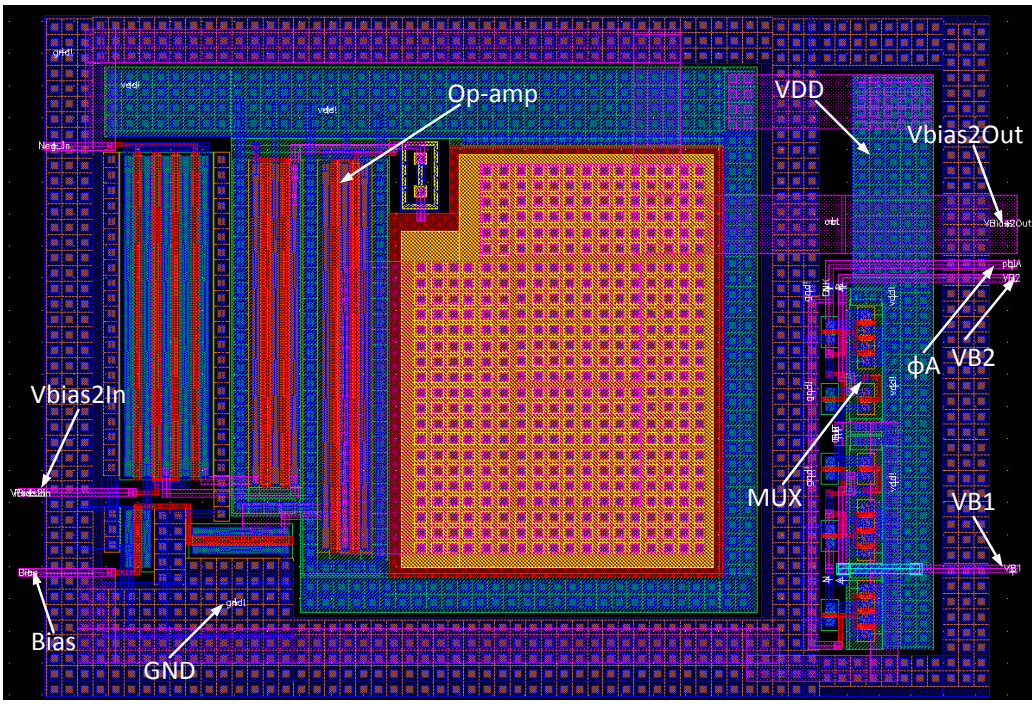


Fig 4.27 Analog buffer layout design

The layout of the analog buffer is shown in Fig. 4.27. The layout measures 154.25 µm x 220.15 µm. The post-layout simulation along with the CDC confirms a functional layout construction. The pin marked Bias is internally connected to the out of the MUX but has also been an external on-chip connection for flexibility in verification during chip testing. The Bias pin may be left un-connected.

Op-amp:

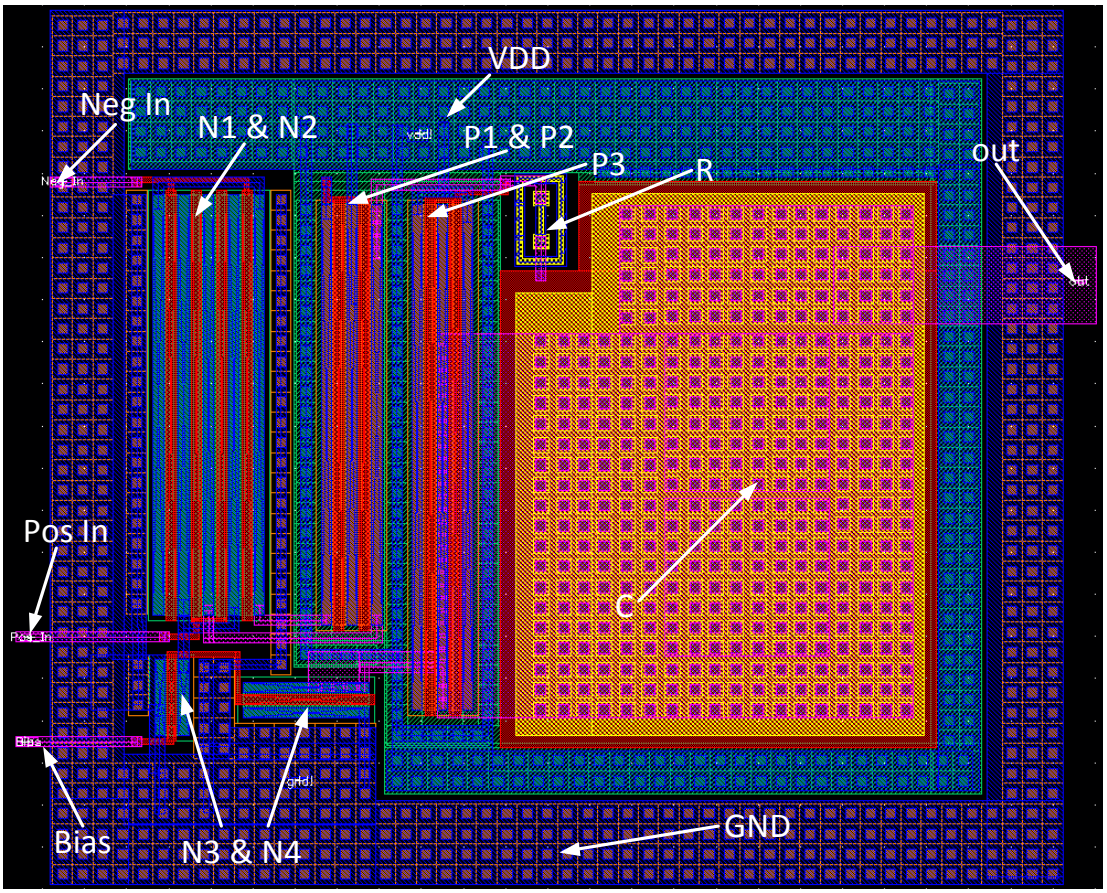


Fig 4.28 Op-amp layout design

The layout of the op-amp is shown in Fig. 4.28. The layout measures 120.45 µm x 145.25 µm. The post layout simulations of the amplified voltage and the gain/stability plots

are shown in Fig 4.29 and Fig 4.30 respectively. Both the plots correspond to the schematic waveforms confirming a functional layout design.

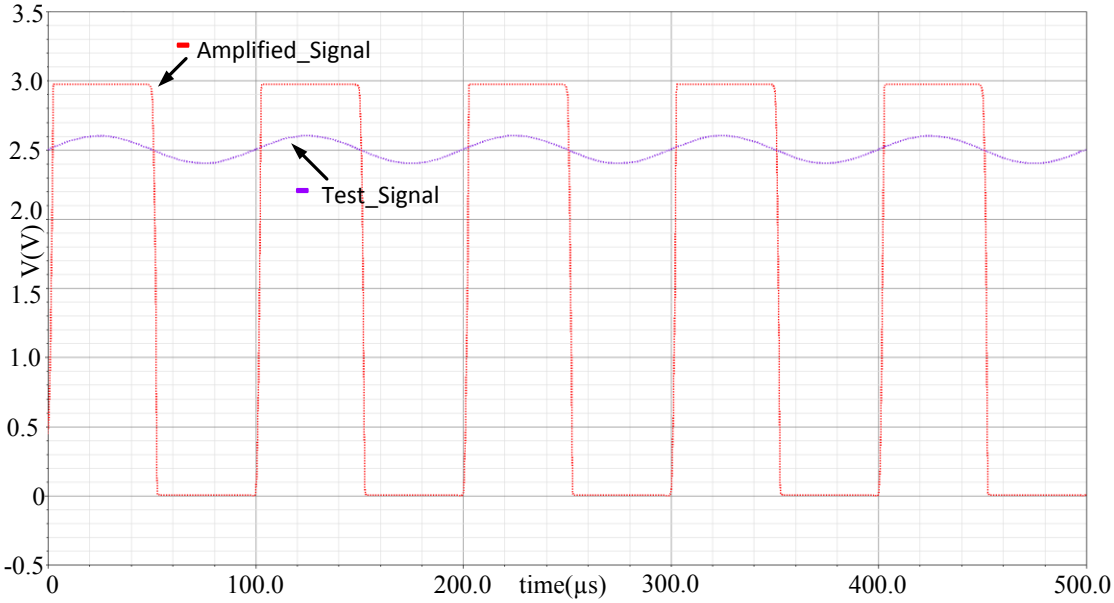


Fig 4.29 Op-amp post-layout amplified signal

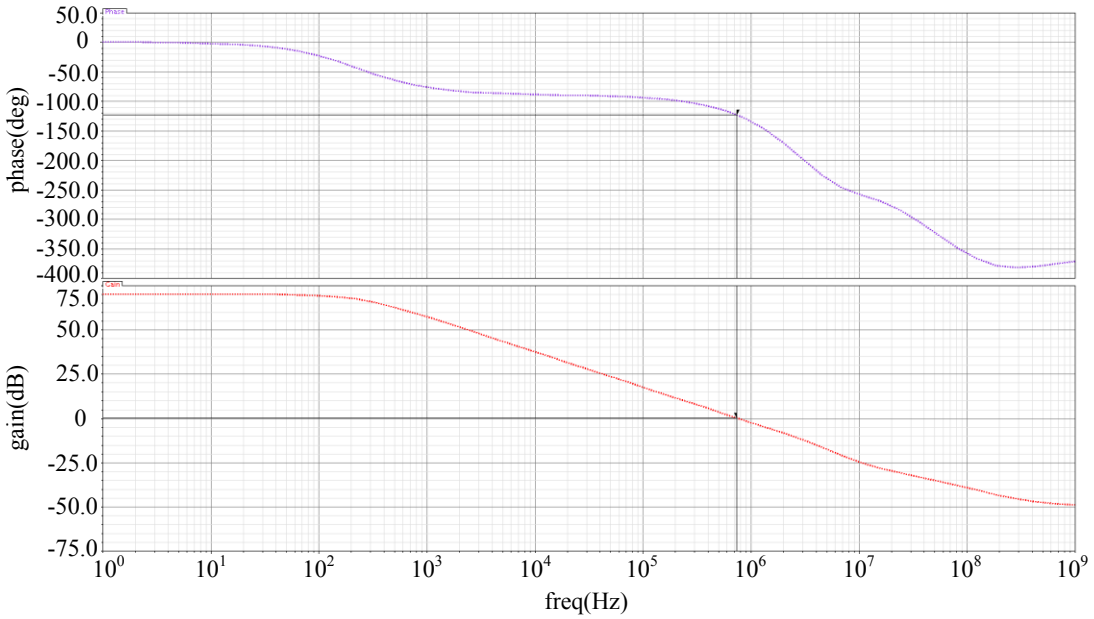


Fig 4.30 Op-amp post-layout gain and stability plot

4.11 Clock Extractor

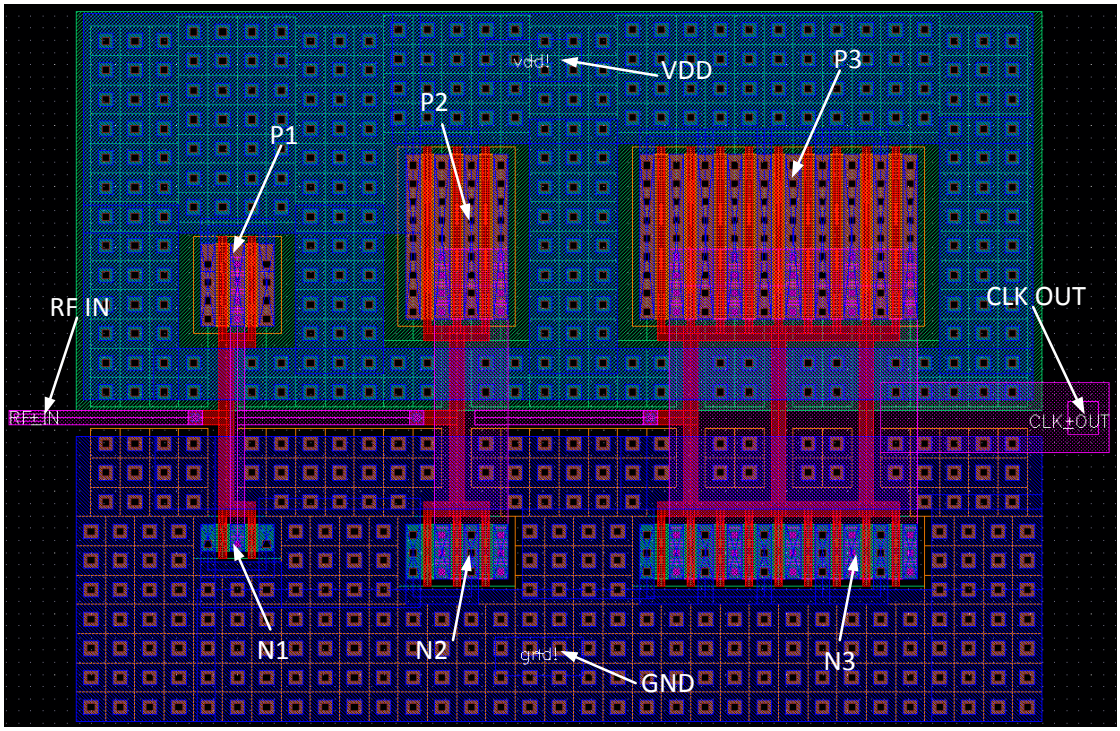


Fig 4.31 Clock extractor layout design

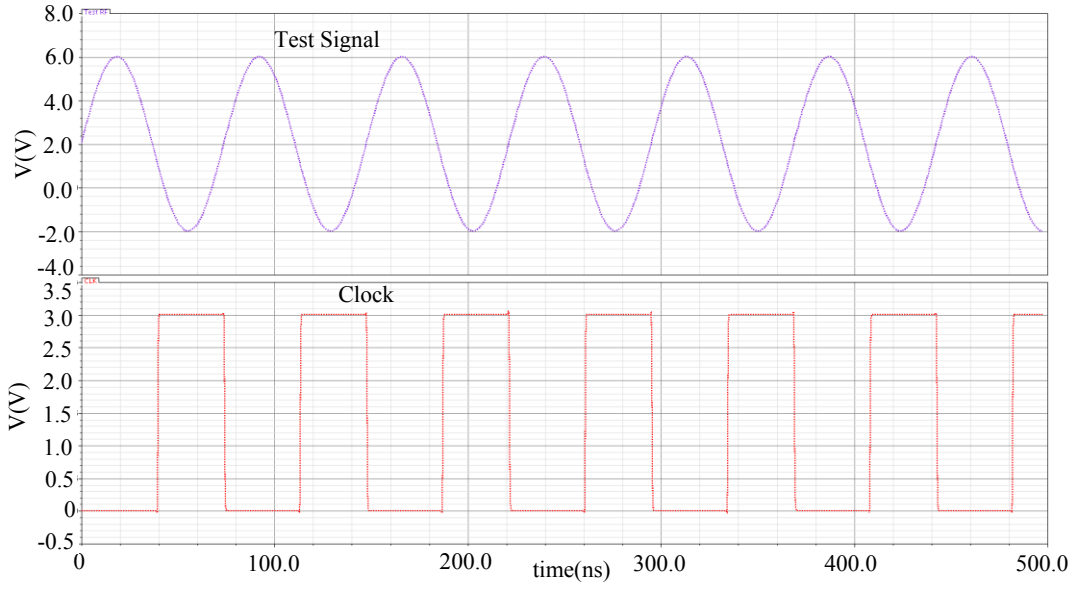


Fig 4.32 Clock extractor post-layout simulation

The layout of the clock extractor is shown in Fig. 4.31. The layout measures 86.25 µm x 65.75 µm. The post layout simulation of the clock extractor is shown in Fig 4.32. The post layout plots correspond to the schematic waveforms confirming a functional layout design.

4.12 Modulator and Demodulator

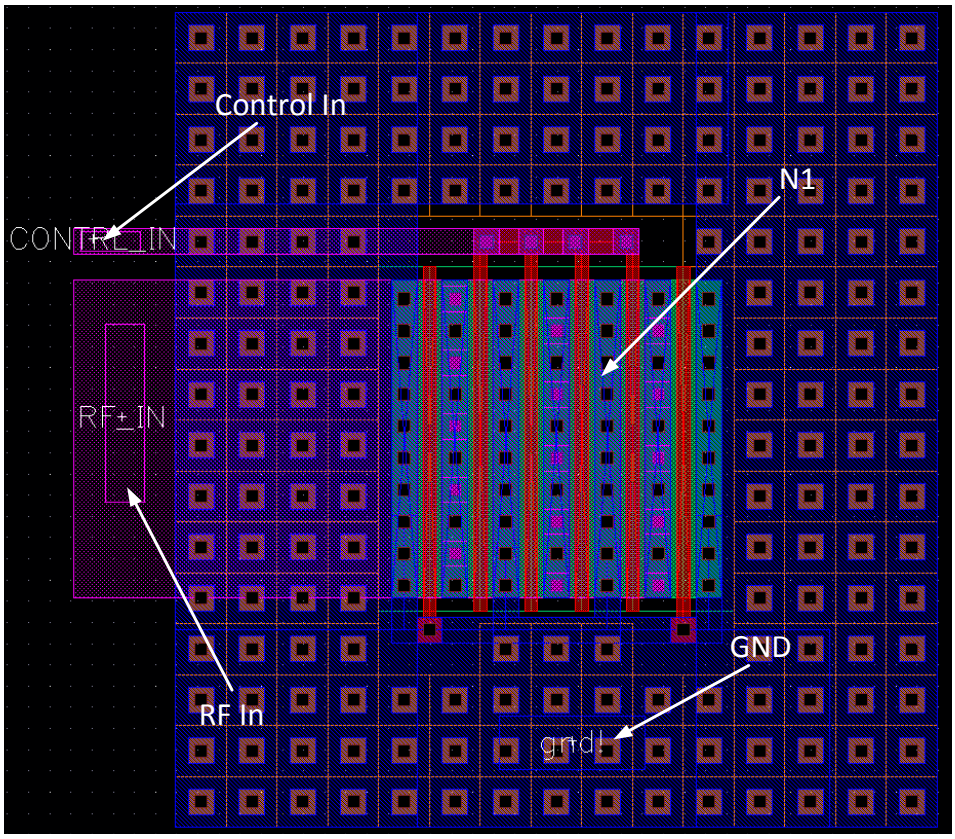


Fig 4.33 Modulator layout design

The modulator layout is shown in Fig 4.33. The layout measures 30.25 µm x 28.5 µm. Post-layout simulation is shown in Fig 4.34 which corresponds to the pre-layout simulation confirming a functional layout design. The demodulator layout is shown in Fig 4.35. The layout measures 355.260 µm x 441.400 µm.

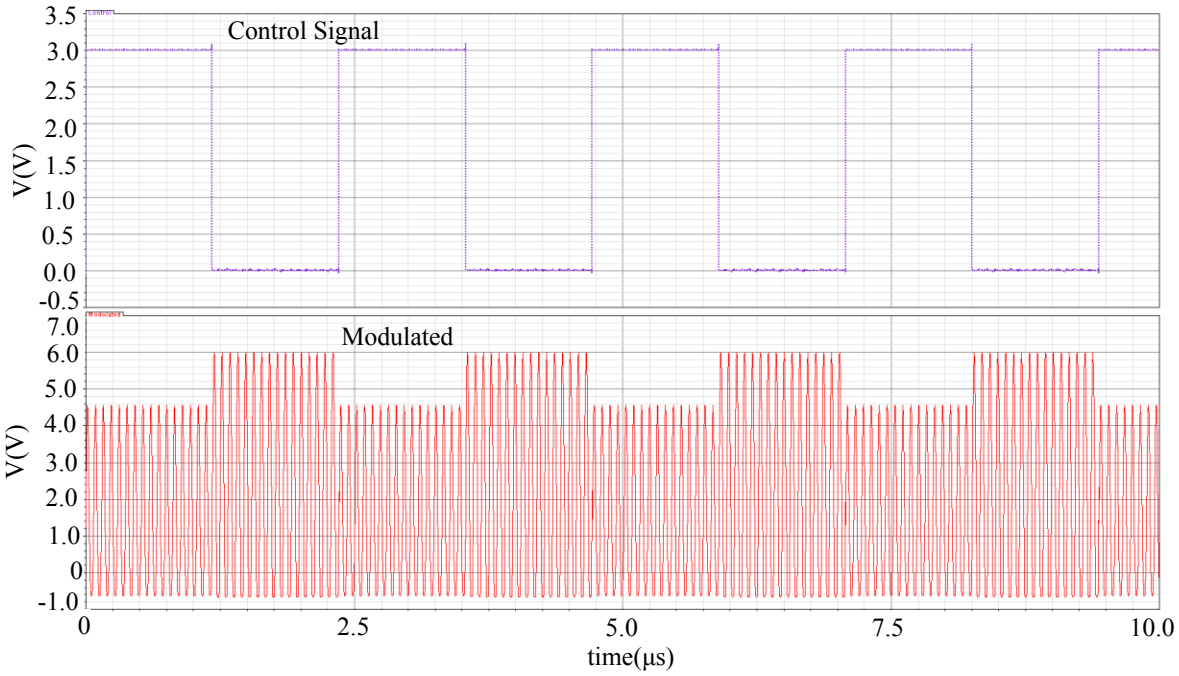


Fig 4.34 Modulator post-layout simulated waveform

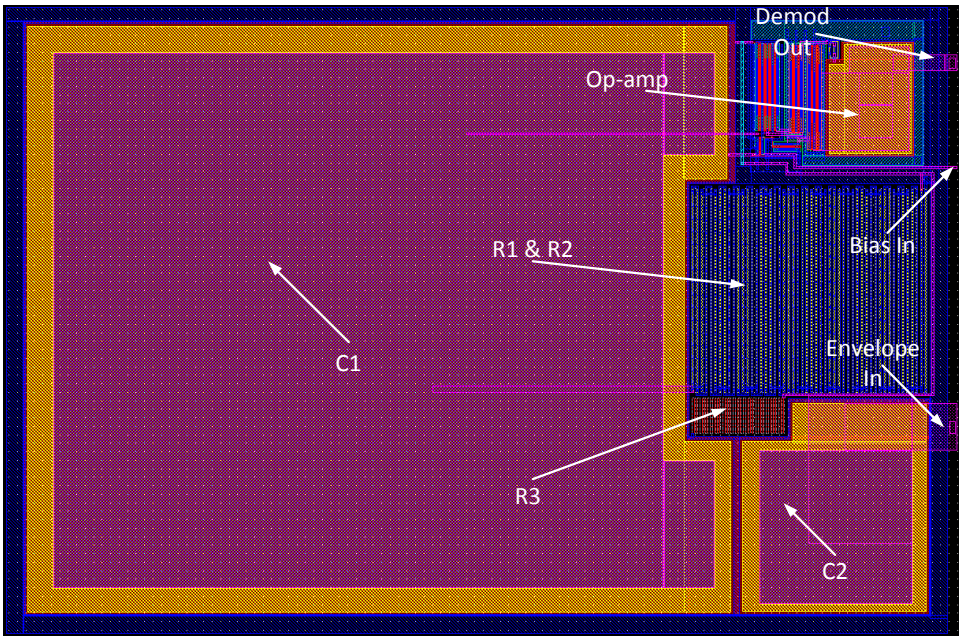


Fig 4.35 De-Modulator layout design

4.13 Final chip layout

The layout of the entire analog core is shown in Fig 4.36. This shows the final chip submission layout. The final layout measures at 3.0 mm x 2.4 mm and was designed on 0.5 µm CMOS technology. An in-detail pin configuration and description is provided in Table 4.1.

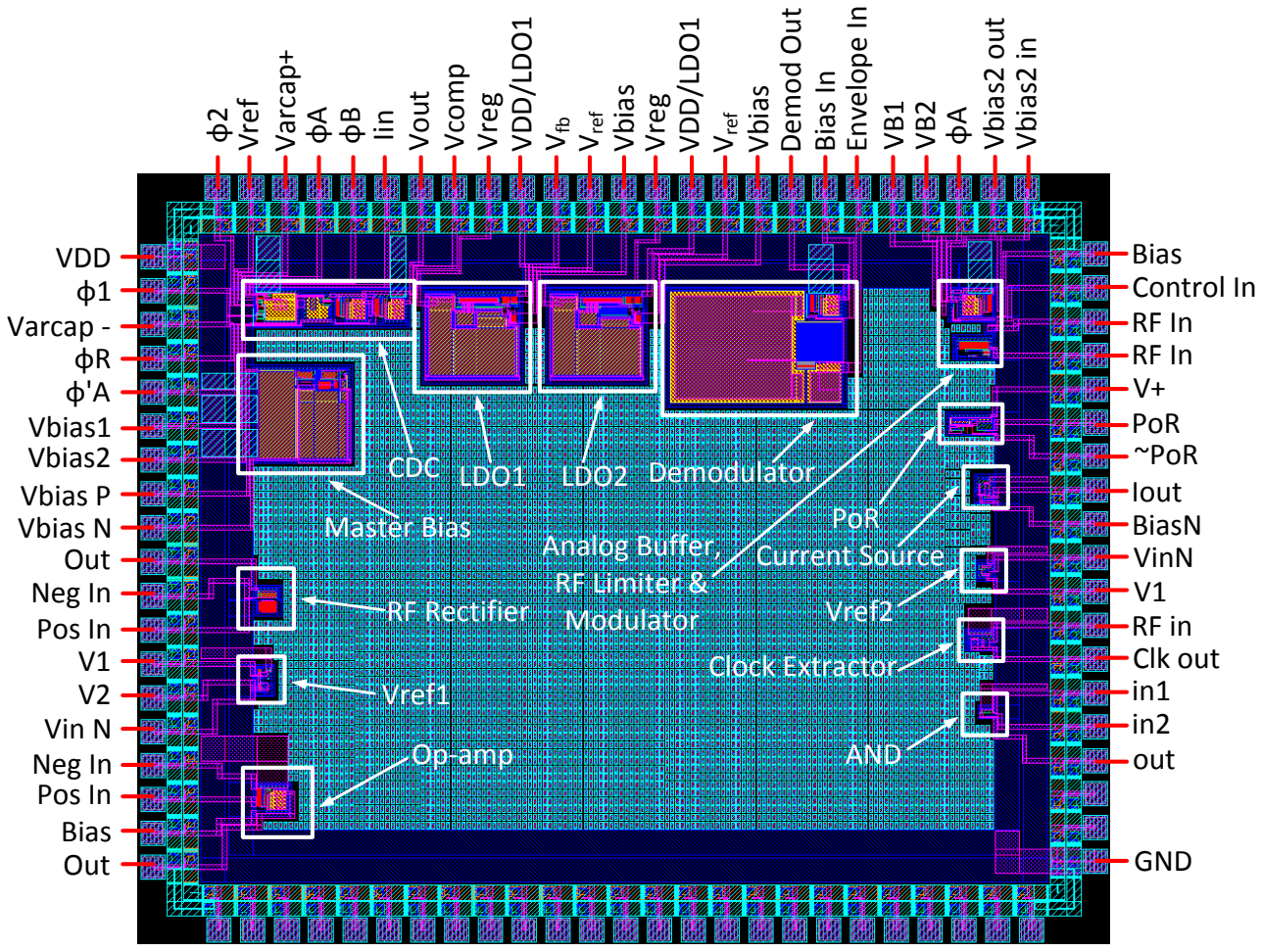


Fig 4.36 Final chip layout of the analog core

Table 4.1 In-detail pin configuration for final chip layout

	Pins	Analog/Digital	Input Range	Connectivity
	VDD	Analog	3 V	in/out
	GND	Analog	0 V	in/out
CDC	ϕA	Digital	0 V-3 V	input
	ϕB	Digital	0 V-3 V	input
	ϕ1	Digital	0 V-3 V	input
	ϕ2	Digital	0 V-3 V	input
	ϕR	Digital	0 V-3 V	input
	ϕ'A	Digital	0 V-3 V	input
	Varcap -	Analog	5.71 pF - 6.2 pF	in/out
	Varcap +	Analog	5.71 pF - 6.2 pF	in/out
	Iin	Analog	10 nA	input
	Vref	Analog	3 V	input
	Vbias1	Analog	750 mV	input
	Vbias2	Analog	1.5 V	input
	Vout	Analog	1.5V - 2 V	output
	Vcomp	Analog	0V - 3V	output
LDO w/o resistor	Vreg	Analog	3V	output
	VDD	Analog	0V - 10V	input
	Vfb	Analog	From resistors	input
	Vref	Analog	2 V	input
	Vbias	Analog	750 mV	input
Fixed LDO	Vreg	Analog	3V	output
	VDD	Analog	0V - 10V	input
	Vref	Analog	2V	input
	Vbias	Analog	750 mv	input
Demod	Demod Out	Analog	0 V- 3 V	output
	Bias In	Analog	1 V	input
	Envelope In	Analog	From Diode	input
Analog Buffer	VB1	Analog	750 mV	input
	VB2	Analog	1 V	input
	ϕA	Digital	0 V - 3 V	input
	Vbias2 Out	Analog	1.5 V	output
	Vbias2 In	Analog	1.5 V	input
	Bias	Analog	750 mV - 1 V	input
Mod	Control In	Analog	0 V- 3 V	input
	RF In	Analog	4 VP-P, 13.56 MHz	in/out
RF Limiter	RF In	Analog	0 V- 30 V, 13.56 MHz	in/out

POR	V+	Analog	0 V- 10 V, 13.56 MHz	input
	PoR	Analog	0V - 3 V	output
	~PoR	Analog	gnd	output
Current Source	Iout	Analog	10 nA	output
	BiasN	Analog	750 mV	input
Clk Extr	RF In	Analog	0 V - 10 V, 13.56 MHz	input
	Clk Out	Analog	0 V - 3 V, 13.56 MHz	output
AND	in 1	Analog	0 V - 3 V	input
	in 2	Analog	0 V - 3 V	input
	out	Analog	0 V - 3 V	output
Master Bias	VbiasP	Analog	2.212 V	output
	VbiasN	Analog	550 mV	output
Vref1	V1	Analog	1.5 V	output
	V2	Analog	750 mV	output
	Vin N	Analog	550 mV	input
Vref2	V1	Analog	1 V	output
	Vin N	Analog	550 mV	input
Rectifier	Neg In	Analog	10 VP-P, 13.56 MHz	input
	Pos In	Analog	10 VP-P, 13.56 MHz	input
	Out	Analog	8 V	output
Op-amp	Neg In	Analog	2 V	input
	Pos In	Analog	2 V, 10 VP-P, 1 KHz	input
	Bias	Analog	750 mV	input
	Out	Analog	0 V - 3 V	output

4.14 Conclusion

The layouts of all the analog blocks were designed and the chip to be submitted was also designed. The following chapter will give concluding remarks on the thesis research work.

CHAPTER 5

CONCLUDING REMARKS AND FUTURE WORKS

5.1 Concluding Remarks

The entire analog core for an implantable RFID-enabled pressure measurement system is designed. The designed analog core includes the power generation block for the system, the clock extractor for the digital core and the pressure sensor data converter. Circuit design constraints of low-power consumption and small form factor were achieved in the implementation of the analog core. A novel low-power analog-to-digital converter (ADC) for the pressure sensor is designed which consumes only 90 μW and has a resolution of 12 buts. This makes the implementation of the entire system suitable for such energy-constrained applications. Cadence Virtuoso 6.1 Analog Design Environment simulators are used to design, test and compare the schematic and post-layout simulations of the components. The final chip layout measured at 3.0 mm x 2.4 mm.

5.2 Future Work

Due to an oversight, the generation of V_{ref} and V_{bias} inputs to the LDO (see Fig 3.1b) requires an LDO output. These signals should have been generated by the master bias circuit. The chip can still be tested by generating a stable 3 V supply from the output of the rectifier using a zener diode.

Post-fabrication chip-testing and verification has to be performed to test chip functionality. The long-term implementation of this thesis will be its integration with the digital core to build the RFID transponder. Also, real time pressure measurement and wireless data transmission will be the ultimate goal of the whole implementation.

REFERENCES

[1] S. Simon, D. K. Moser, and D. Thompson, “Clinical assessment and investigation of patients with suspected heart failure,” in *Caring for the Heart Failure Patient*. Switzerland: Informa Healthcare, 2004, pp. 75–92.

[2] J. B. Young, “The global epidemiology of heart failure,” *Med. Clin. North Amer.*, vol. 88, pp. 1135–1143, 2004.

[3] D. Jakovljevic, V. Salomaa, J. Sivenius, M. Tamminen, C. Sarti, K. Salmi, E. Kaarsalo, V. Narva, P. Immonen-Raiha ,J. Torppa, and J. Tuomilehto *Seasonal variation in the occurrence of stroke in a Finnish adult population*: the FINMONICA Stroke Register. Stroke 1996;27:1774-1779.

[4] K. K. Ho, J. L. Pinsky,W. B. Kannel, and D. Levy, “The epidemiology of heart failure: The Framingham Study,” *J. Amer. Coll. Cardiol.*, vol. 22, pp. 6A–13A, 1993.

[5] V. L. Roger, S. A. Weston, M. M. Redfield, J. P. Hellermann-Homan, J. Killian, B. P.Yawn, and S. J. Jacobsen, “Trends in heart failure incidence and survival in a community-based population,” *J. Amer. Med. Assoc.*, vol. 292, pp. 344–350, Jul. 21, 2004.

[6] M. R. Cowie, D. A. Wood, A. J. S. Coats, S. G. Thompson, V. Suresh, P. A. Poole-Wilson, and G. C. Sutton, “Survival of patients with a new diagnosis of heart failure: A population based study,” *Heart*, vol. 83, pp. 505–510, May 1, 2000.

[7] E.Y. Chow,; A.L. Chlebowski,; S. Chakraborty,; W.J. Chappell,; P.P. Irazoqui,; , "Fully Wireless Implantable Cardiovascular Pressure Monitor Integrated with a Medical Stent," *Biomedical Engineering, IEEE Transactions on* , vol.57, no.6, pp.1487-1496, June 2010 doi: 10.1109/TBME.2010.2041058

[8] Q. Huang; M. Oberle,; , "A 0.5-mW passive telemetry IC for biomedical applications," *Solid-State Circuits, IEEE Journal of* , vol.33, no.7, pp.937-946, Jul 1998 doi: 10.1109/4.701225

[9] C. Sauer,; M. Stanacevic,; G. Cauwenberghs,; N. Thakor,; , "Power harvesting and telemetry in CMOS for implanted devices," *Biomedical Circuits and Systems, 2004 IEEE International Workshop on* , vol., no., pp. S1/8- S1-4, 1-3 Dec. 2004 doi: 10.1109/BIOCAS.2004.1454187

[10] H.Y. Yang,; R. Sarpeshkar,; , "A time-based energy-efficient analog-to-digital converter," *Solid-State Circuits, IEEE Journal of* , vol.40, no.8, pp. 1590- 1601, Aug. 2005 doi: 10.1109/JSSC.2005.852042

[11] B. George,; V.J. Kumar,; , "Switched capacitor triple slope capacitance to digital converter," *Circuits, Devices and Systems, IEE Proceedings* - , vol.153, no.2, pp. 148-152, April 2006

[12] D. Yeager,; F. Zhang; A. Zarrasvand,; N.T. George,; T. Daniel,; B.P. Otis,; , "A 9 μA, Addressable Gen2 Sensor Tag for Biosignal Acquisition," *Solid-State Circuits, IEEE Journal of* , vol.45, no.10, pp.2198-2209, Oct. 2010 doi: 10.1109/JSSC.2010.2063930

[13] P. Vaillancourt,; A. Djemouai,; J.F. Harvey,; M. Sawan,; , "EM radiation behavior upon biological tissues in a radio-frequency power transfer link for a cortical visual implant," *Engineering in Medicine and Biology Society, 1997. Proceedings of the 19th Annual International Conference of the IEEE* , vol.6, no., pp.2499-2502 vol.6, 30 Oct-2 Nov 1997 doi: 10.1109/IEMBS.1997.756835

[14] http://www.microfab.de/downloads/20080109datasheete1.3na4.pdf

[15] K. Fikenzeller, *RFID Handbook, Radio-Frequency Identification Fundamentals and Applications*, 2nd ed. Wiley, 2003.

[16] D. Tandeske, *Pressure Sensors Selection and Application*, 1st ed. Taylor & Francis, Inc.: 1990.

[17] K.R. Lee; K. Kim; Y.K. Kim; H.D. Park; S.W. Choi; W.B. Choi; B.K. Ju; , "Capacitive Absolute Pressure Sensor with Vacuum Cavity Formed by Bonding Silicon to Soiwafer for Upper Air Observations," *Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul. 19th IEEE International Conference on* , vol., no., pp.618-621, 2006 doi: 10.1109/MEMSYS.2006.1627875

[18] P. Gerrish,; E. Herrmann,; L. Tyler,; K. Walsh,; , "Challenges and constraints in designing implantable medical ICs," *Device and Materials Reliability, IEEE Transactions on* , vol.5, no.3, pp. 435- 444, Sept. 2005 doi: 10.1109/TDMR.2005.858914

[19] Jacob R. Baker, *CMOS Circuit Design, Layout and Simulation*, 3rd ed. New York: Wiley, 2010.

[20] J.P. Curty,; N. Joehl,; C. Dehollain,; M.J. Declercq,; , "Remotely powered addressable UHF RFID integrated system," *Solid-State Circuits, IEEE Journal of* , vol.40, no. 11, pp. 2193 - 2202, Nov.2005 doi: 10.1109/JSSC.2005.857352

[21] R.J. Milliken,; J. Silva-Martinez,; E. Sanchez-Sinencio,; , "Full On-Chip CMOS Low-Dropout Voltage Regulator," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.54, no.9, pp.1879-1890, Sept. 2007 doi: 10.1109/TCSI.2007.902615

VITA

Sagnik Kar was born on October 25, 1986, in Kolkata, West Bengal, India. He received a Bachelor of Technology in Electronics and Communication Engineering from S.R.M. University, Chennai, India. He received the Dean's International Computing & Engineering Award (DICE) for the 2009-2011 school years.

Mr. Kar has held various graduate teaching and graduate research assistantship positions in the Department of Computer Science and Electrical Engineering (CSEE) at the University of Missouri- Kansas City (UMKC) from June 2010 to July 2011.

Mr. Kar is a member of the Institute of Electrical and Electronics Engineers (IEEE), Eta Kappa Nu (HKN) - honor society of the IEEE for electrical and computer engineering and of the Honor Society of Phi Kappa Phi (ΦΚΦ). His IEEE conference paper publication is provided below.

Kar, Sagnik; Leon-Salas, Walter D.;, " A Low-Power 12 Bit Capacitance-to-Digital Converter for Capacitive MEMS Pressure Sensor,", *IEEE Sensors Conference: Regular Papers,* October 2011