Unipolar spin diodes and transistors

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Unipolar devices constructed from ferromagnetic semiconducting materials with variable magnetization direction are shown theoretically to behave very similarly to nonmagnetic bipolar devices such as the p-n diode and the bipolar (junction) transistor. Such devices may be applicable for magnetic sensing, nonvolatile memory, and reprogrammable logic. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1348317]

Until recently the emerging field of magnetoelectronics has focused on magnetic metals for conducting components.[1] Multilayer magnetoelectronic devices, such as giant magnetoresistive (GMR)[2] and magnetic tunnel junction (MTJ)[3–5] devices, have revolutionized magnetic sensor technology and hold promise for reprogrammable logic and nonvolatile memory applications. The performance of these devices improves as the spin polarization of the constituent material approaches 100%, and thus there are continuing efforts to find 100% spin-polarized conducting materials.

Doped magnetic semiconductors are a promising direction towards such materials, for the band-width of the occupied carrier states is narrow. For example, for nondegenerate carriers and a spin splitting of 100 meV the spin polarization will be 98% at room temperature. To date high-temperature ($T_{Curie} > 100$ K) ferromagnetic semiconductors such as $Ga_{1-x}Mn_xAs$ are effectively p doped. *Semimagnetic n*-doped semiconductors like BeMnZnSe, however, have already been shown to be almost 100% polarized (in the case of BeMn-ZnSe in a 2 T external field at 30 K).[6] Both resonant tunneling diodes[7] and light-emitting diodes[8] have been demonstrated which incorporate one layer of ferromagnetic semiconductor. It is inevitable that devices incorporating multiple layers of ferromagnetic semiconducting material will be constructed.

Motivated by this possibility, we have investigated the transport properties of specific device geometries based on multilayers of spin-polarized unipolar doped semiconductors. Previous theoretical work in this area includes spin transport in *homogeneous* semiconductors[9,10] and calculations of spin filtering effects in superlattices.[11] Our interest here is on the nonlinear transport properties, particularly the behavior of the *charge* current, of two- and three-layer heterostructures. We focus on two device geometries, which for simplicity we will assume are uniformly n doped (p doped devices behave similarly, but with opposite sign of the charge current). The first, which will be referred to as a spin diode, consists of two layers with antiparallel majority carrier spin polarization and is in many ways similar to the MTJ devices based on metals. The second is a three-layer configuration with alternating majority carrier spin polarization,

which will be referred to as a spin transistor. These devices could function in a similar way to GMR or MTJ devices, in which the resistance of the device changes due to a change in the magnetization direction of one layer. As the parallel configuration (or ''low-resistance state'') would be of higher resistance than that of the GMR or MTJ devices, these devices would match better the typical impedance levels of conventional semiconducting technology.

The aspects of these devices we will emphasize in this letter, however, are the presence of *charge* current gain in the spin transistor and the sensitivity of this gain to magnetic field. Specifically, the I–V characteristics—unlike those of devices based on magnetic metals—are inherently nonlinear, which allows the amplification of spin-polarized charge current. This suggests new modes of operation of these devices in reprogrammable logic, nonvolatile memory, and magnetic sensing.

In our presentation of the current–voltage characteristics of the spin transistor, we will frequently allude to a fundamental analogy between unipolar ferromagnetic semiconductors and nonmagnetic bipolar materials. This analogy is best visualized in the relationship between a spin diode and the traditional p-n diode. Shown in Fig. 1(a) are the band edges of the conduction and valence band for a traditional p-n diode in equilibrium. The quasifermi levels are shown as dashed lines. To assist in exploring the analogy with the spin diode, Fig. 1(b) shows the energies of the elementary carriers in those bands: conduction electrons and valence holes. This unfamiliar diagram is obtained merely by noting that the energy of a hole in the valence band is the negative of the energy of the valence electron (relative to the chemical potential). We introduce Fig. 1(b) in order to point out the similarities with the band edges for the spin diode. Shown in Fig. 1(c) are those band edges, which are also the carrier energies. Just as for the p-n diode, in the unipolar spin diode the majority carriers on one side are the minority carriers on the other side.

A major difference, however, is that the two types of carriers in the p-n diode have an opposite charge, whereas in the spin diode they have the same charge. One implication of this is that in the p-n diode the interface between the layers is a *charge* depletion layer whereas in the spin diode the interface is a *spin* depletion layer. The strong spin–density
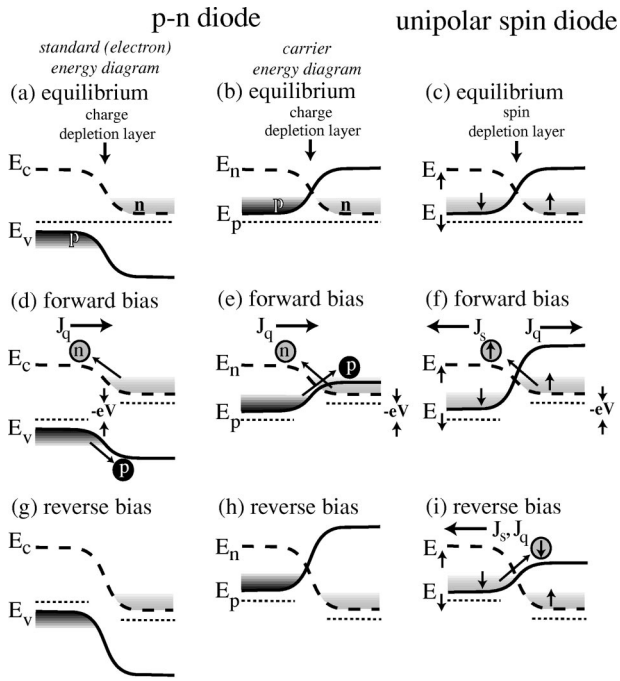
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FIG. 1. Standard and carrier energy diagrams for a traditional p-n diode vs unipolar spin diode under equilibrium conditions (a)–(c), forward bias (d)–(f), and reverse bias (g)–(i).

gradient is maintained by the gradient of a self-consistent exchange field.[12] Another major difference resulting from the charges of the carriers is the way the carrier energies shift under bias.

In the p-n diode under forward bias, the barriers for both valence hole and conduction electron transport across the junction are reduced. As shown in Figs. 1(d) and 1(e) this leads to an increase in the conduction electron current to the left-hand side and the valence hole current to the right-hand side. Because the carriers have an opposite charge, both increases result in an increased charge current to the right-hand side. For the spin diode, only the barrier for spin up electrons moving to the left-hand side is reduced—the barrier for spin down electrons moving to the right-hand side is increased. The charge current is thus directed to the right-hand side and the spin current to the left-hand side. Under reverse bias the barriers for carrier transport are both increased in the p-n diode [Figs. 1(g) and 1(h)], yielding rectification of the charge current. For the spin diode [Fig. 1(i)], one barrier is reduced and the other increased. Thus, the charge current is not rectified but the spin current is. Applying analogous assumptions to the Shockley assumptions for an ideal diode, we find the charge current density J_q and the spin current density J_s depend on the voltage V according to

$$J_q = 2qJ_0 \sinh(qV/kT), \tag{1}$$

$$J_s = 2\hbar J_0 \sinh^2(qV/2kT), \tag{2}$$

where $J_0 = Dn_m/L_m$, q is the electron charge, V is the voltage, k is Boltzmann's constant, T is the temperature, $\hbar$ is the Planck's constant, D is the diffusion constant, n_m is the minority carrier density, and L_m is the minority spin diffusion length. The resulting spin polarization of the current is
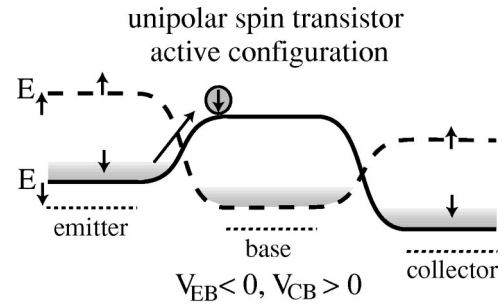
$$P = (2qJ_s/\hbar J_q) = \tanh(qV/2kT). \tag{3}$$

FIG. 2. Carrier energy diagram for the unipolar spin transistor in the normal active configuration.

Thus the spin polarization approaches unity as V gets large, and approaches 0 for small V. The relative directions of the charge and spin currents are shown in Fig. 1 for the cases of forward and reverse bias.

For ease of use as components in integrated circuits, a magnetoelectronic device should allow for magnetic manipulation of the charge current gain—to achieve this we describe the spin transistor, shown in Fig. 2. Analyzing this structure in a similar way to a bipolar nonmagnetic transistor, the collector current density is

$$I_C = -\frac{qJ_0}{\sinh(W/L)}[(e^{-qV_{EB}/kT} - 1) \\ - (e^{-qV_{CB}/kT} - 1)\cosh(W/L)] \\ - qJ_0[e^{qV_{CB}/kT} - 1] \tag{4}$$

and the emitter current is

$$I_E = -\frac{qJ_0}{\sinh(W/L)}[(e^{-qV_{EB}/kT} - 1)\cosh(W/L) \\ - (e^{-qV_{CB}/kT} - 1)] + qJ_0[e^{qV_{EB}/kT} - 1]. \tag{5}$$

The base width is W, the voltage between emitter and base is $V_{EB} < 0$, and the voltage between collector and base is $V_{CB} > 0$. The base current is $I_B = I_E - I_C$. When W/L is small, $I_B \ll I_C$, which is the desired situation for transistor operation (current gain $I_C/I_B \gg 1$).

The ''emitter efficiency'' γ, defined as the ratio of the majority spin–direction charge current $I_{E\downarrow}$ to the total emitter current I_E,[13] is $1 - e^{qV_{EB}/kT}$ and thus very close to one. However, in contrast to bipolar nonmagnetic transistors, the ''collector multiplication factor'' M, defined as the ratio between the full collector current I_C and the majority spin–direction charge current $I_{C\downarrow}$,[13] is given by

$$M = 1 + \sinh(W/L)e^{q[V_{CB} + V_{EB}]/kT}, \tag{6}$$

which is close to 1 only if W/L is small.

Thus, we have shown that it should be possible to program a logical circuit which behaves like a bipolar logical circuit, using a uniformly doped unipolar magnetic material. The ''p''-like regions correspond to regions with the magnetization pointing one way ($\hat{z}$) and the ''n''-like regions correspond to region with the magnetization pointing along $-\hat{z}$. Such logical circuits can include memory circuits, thus indicating that nonvolatile memory can be constructed as well.

We now turn to magnetic sensing applications. For GMR and MTJ devices the sensing is performed by allowing

the magnetization of one layer to rotate easily in the presence of an external field, and observing the resistance change. Of course the spin diode could perform this way as well. The spin transistor, however, can detect magnetic fields sensitively even when the magnetization direction of the semiconductor layers is unchanged.

The effect of an external magnetic field on any section of the spin transistor is principally to shift the minority band edge. If the chemical potential is pinned by the external circuit the majority band edge does not move significantly. Thus the spin transistor is a minority-spin device (in contrast to the ''spin field-effect transistor,'' [14] which is a majority-spin device). The collector and emitter currents in the presence of magnetic fields B_E, B_B, and B_C applied to the emitter, the base, and the collector, respectively, are

$$I_C = -\frac{qJ_0}{\sinh(W/L)}\{(e^{[-qV_{EB}-g\mu B_B]/kT}-1)+\cosh(W/L)\}$$
$$-qJ_0\{e^{[qV_{CB}+g\mu B_C/kT]}-1\}, \tag{7}$$

$$I_E = -\frac{qJ_0}{\sinh(W/L)}\{(e^{[-qV_{EB}-g\mu B_B]/kT}-1)\cosh(W/L)+1\}$$
$$-qJ_0. \tag{8}$$

Here g is the g factor and μ is the magnetic moment of the electron. These currents depend *exponentially* on the magnetic fields applied to the base and the collector, but not on the emitter field B_E. Materials such as BeMnZnSe have g factors close to 1000,[6] thus yielding a change in current of roughly 0.01% per gauss at room temperature, which is still in the *linear* region of the expansion of the exponentials in Eqs. (7) and (8). However materials with still larger g factors may yet be found (typical sensitivity of GMR devices is 1%/gauss). We also note that an electrically isolated magnetic field amplifier can be employed—namely a small magnetic element which is free to rotate in response to the external field, and can produce a larger field at the spin transistor base layer, or the base magnetization itself can be rotated.

We now revisit the Shockley assumptions for an ideal diode. These are (1) the bulk of the voltage drop takes place across the depletion region, (2) the Boltzmann approximation for transport is valid, (3) the minority carrier densities are small compared to majority carrier densities, and (4) no generation currents exist in the depletion layer. Assumption (1) causes the greatest concern. The depletion region in the spin diode is very different than that of the p-n diode. In the p-n diode, the thickness of the charge depletion region is set by the doping levels in the two regions and the band gap of the material. In the spin diode the spin depletion region is probably a Néel wall, and its thickness is set by the ratio between the magnetic anisotropy energy and the magnetic stiffness. For optimal device performance of spin diodes and transistors, the domain wall should be very thin. In this limit, the spin of carriers passing through the domain wall will not precess. When the domain wall is very thick, however, the electron spin will follow adiabatically the direction of the macroscopic magnetization and the device will behave like an ordinary metallic conductor, where the voltage drop is uniformly distributed along the device. In the general case,

there is a finite probability that the electrons emerge from the spin depletion region with their spins flipped. We have analyzed this case and find that, due to the high resistivity of the no-spin–flip channel, the voltage drop still takes place mostly across the spin depletion region, unless the probability of no-spin flip is utterly negligible. The latter case can occur if majority spin orientation carriers from one side of the junction can directly tunnel into the majority spin orientation band of the opposite side, as opposed to being thermally excited above the exchange barrier into the minority spin orientation band. If loss of spin coherence becomes a serious problem, the domain wall can be replaced by a nonmagnetic region, as is currently done in MTJs. In the presence of the nonmagnetic region, the relevant length is the spin coherence length, which can be quite long.

The remaining three assumptions are of less concern. Assumption (2) commonly holds in semiconductor devices so long as the applied voltage is not too large. If the spin splitting in the magnetic regions is sufficiently large compared to the operation temperature then assumption (3) will hold. Assumption (4) relies on the spin coherence time greatly exceeding the transit time through the depletion region (for the spin diode) or the base (for the spin transistor). Measurements of long spin coherence times in semiconductors near room temperature[15,16] indicate this assumption is reasonable.

[1] G. Prinz, Science **282**, 1660 (1998); **283**, 330 (1999).

[2] M. Baibich *et al.*, Phys. Rev. Lett. **61**, 2472 (1988).

[3] M. Johnson, Phys. Rev. Lett. **70**, 2142 (1993); M. Johnson, J. Appl. Phys. **75**, 6714 (1994); J. Daughton, J. Brown, E. Chen, R. Beech, A. Pohm, and W. Kude, IEEE Trans. Magn. **30**, 4608 (1994).

[4] J. Moodera, L. Kinder, T. Wong, and R. Meservey, Phys. Rev. Lett. **74**, 3273 (1995).

[5] A. Fert and S.-F. Lee, Phys. Rev. B **53**, 6554 (1996).

[6] B. König, U. Zehnder, D. R. Yakovlev, W. Ossau, T. Gerhard, M. Keim, A. Waag, and G. Landwehr, Phys. Rev. B **60**, 2653 (1999).

[7] H. Ohno, N. Akiba, F. Matsukura, A. Shen, K. Ohtani, and Y. Ohno, Appl. Phys. Lett. **73**, 363 (1998); H. Ohno, Science **281**, 951 (1998).

[8] Y. Ohno, D. K. Young, B. Beschoten, F. Matsukura, H. Ohno, and D. D. Awschalom, Nature (London) **402**, 790 (1999).

[9] M. E. Flatté and J. M. Byers, Phys. Rev. Lett. **84**, 4220 (2000).

[10] I. D'Amico and G. Vignale (unpublished).

[11] Y. Guo, B.-L. Gu, Z.-Q. Li, J.-Z. Yu, and Y. Kawazoe, J. Appl. Phys. **83**, 4545 (1998); J. C. Egues, Phys. Rev. Lett. **80**, 4578 (1998).

[12] The charge distribution in the spin depletion layer depends on the relative size of the screening length (Thomas–Fermi or Debye) and the width of the domain wall. If the former is much larger than the latter, the situation resembles the ordinary depletion layer in a p-n junction: the charge depleted from the domain wall is balanced by a screening charge over a screening length from the domain wall. This situation is qualitatively depicted in Fig. 1(c). If, on the other hand, the screening length is much shorter than the width of the domain wall, then the domain wall region is essentially neutral.

[13] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), Chap. 3.

[14] S. Datta and B. Das, Appl. Phys. Lett. **56**, 665 (1990).

[15] J. M. Kikkawa, I. P. Smorchkova, N. Samarth, and D. D. Awschalom, Science **277**, 1284 (1997).

[16] Y. Ohno, R. Terauchi, T. Adachi, F. Matsukura, and H. Ohno, Phys. Rev. Lett. **83**, 4196 (1999).