ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

HIGH-SPEED DESIGN OF HIGH-RESOLUTION DACS

Ph.d Thesis

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Department : Electronics and Communications Engineering

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Ph.d Thesis
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YÜKSEK ÇÖZÜNÜRLÜKLÜ SAYISAL-ANALOG DÖNÜŞTÜRÜCÜLERİN YÜKSEK HIZLI TASARIMI

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FOREWORD

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September 2009 Indrit MYDERRIZI

M. Sc.

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ABREVIATIONS

VLSI	: Very Large Scale Integration
DAC	: Digital-to-Analog Converter
ADC	: Analog-to-Digital Converter
CD	: Compact Disc
CMOS	: Complementary Metal Oxide Semiconductor
IC	: Integrated Circuit
DSP	: Digital Signal Processing
HDTV	: High Definition Television
SPICE	: Simulation Program with Integrated Circuits Emphasis
D/A	: Digital/Analog
DR	: Dynamic Range
DNL	: Differential Nonlinearity
INL	: Integral Nonlinearity
DR	: Dynamic Range
SFDR	: Spurious Free Dynamic Range
SNR	: Signal to Noise Ratio
FoM	: Figure of Merit
LSB	: Least Significant Bit
MSB	: Most Significant Bit
LE	: Logical Effort
SRD	: Swing Reduced Driver
VCCS	: Voltage Controlled Current Source
SoC	: System on Chip

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HIGH-SPEED DESIGN OF HIGH-RESOLUTION DACS

SUMMARY

Nowadays DACs have become key elements in many electronic systems. They are used in a large variety of applications ranging from CD players to graphic cards, from wireless communications systems to analytical measurements devices. Since data converters form the bridge between the analog and digital world their efficient implementation is highly desirable. The increase in demand for high speed (several 100MHz) and high resolution (higher than 10-bit) DACs, especially in communication applications forces the use of current-steering DACs.

Most publications made use of the segmentation method for the design and the implementation of high performance current-steering DACs. Although this methodology is advantageous in most of the applications requiring high-speed and high-resolution, it suffers from the prolonged design time, complexity and high cost. Thus, the use of this methodology for some applications is not efficient concerning the time and the cost. To overcome these problems efficient methodologies for the high-speed design of high-resolution DACs are considered. In this thesis, a suitable design methodology and a novel architecture are introduced.

Behavioral modeling is necessary for the design of complex mixed-mode systems like current-steering DACs. Most of the models constructed (mathematical or circuit based) can not give a complete view of the system's behavior. For this reason, models that speed up the design and reflect accurately the behavior of the system prior to transistor level implementation are developed. In this thesis, a SIMULINK® based behavioral model is developed and verified through simulations.

To conclude, the efficiency of the applied methodology and the accuracy of the behavioral model are validated through the implementation of a 12-bit hybrid current-steering DAC in a relatively cheap 0.35μm CMOS process technology. The improvements in the building blocks and the different approaches used are reflected in the respective parts of the layout of the implemented DAC. Post-layout simulations are obtained using CADENCE Custom IC Design Tools and the performance characteristics of the DAC are investigated.

YÜKSEK ÇÖZÜNÜRLÜKLÜ SAYISAL-ANALOG DÖNÜŞTÜRÜCÜLERİN YÜKSEK HIZLI TASARIMI

ÖZET

Günümüzde Sayısal-Analog Dönüştürücüler (SAD) birçok elektronik sistemlerin kilit elemanları olmaktadır. CD oynatıcılarla grafik kartlar, telsiz haberleşme sistemlerle analitik ölçüm cihazları arasında değişen çok çeşitli uygulamalarda kullanılmaktadırlar. Veri dönüştürücüler analog ve sayısal dünyalar arasında bir köprü oluşturdukları için hızlı ve verimli bir şekilde gerçekleştirilmeleri yüksek derecede arzu edilmektedir. Özellikle haberleşme uygulamalarında yüksek hızlı (birkaç 100MHz) ve yüksek çözünürlüklü (10 bitten fazla) SADlar için artan rağbet, akım yönlendirmeli SADların kullanımını mecbur kılmaktadır.

Yayınların çoğunda yüksek performanslı akım yönlendirmeli SADların tasarımında ve gerçekleştirmesinde kesimleme yöntemi kullanılmaktadır. Bu yöntem, yüksek hız ve yüksek çözünürlük gerektiren uygulamaların çoğunda avantajlı olmasına rağmen uzun süreli tasarım zamanı, karmaşıklık ve yüksek maliyet yüzünden değer kaybetmektedir. Bu yüzden, bazı uygulamalar için zaman ve maliyet açısından bu yöntemin kullanılması hızlı ve verimli olmayabilir. Bu problemlerin üstesinden gelmek için yüksek çözünürlüklü SADların yüksek hızlı tasarımını sağlayan hızlı ve verimli yöntemler dikkate alınmaktadır. Bu tezde, uygun bir tasarım yöntemi ve yeni bir yapı önerilmektedir.

Akım yönlendirmeli SADlar gibi karmaşık karma yapılı sistemlerin tasarımı için davranışsal modelın oluşturulması zorunlu olmaktadır. Bu amaçla yapılan modellerin çoğu (matematiksel veya devre tabanlı) sistemin davranışı hakkında istenilen eksiksiz manzarayı vermemektedirler. Bu yüzden, transistor seviyesindeki tasarıma geçmeden önce, tasarımı hızlandırabilen ve sistemin davranışını doğru bir şekilde yansıtabilen modeller geliştirilmektedir. Bu tezde, SIMULINK® kullanılarak bir davranışsal model kurulmakta ve modelin performansı benzetimlerle sınanmaktadır.

Sonuç olarak uygulanan yöntemin verimliliğini ve davranışsal modelin doğruluğunu sınamak için nispeten ucuz olan 0.35µm CMOS proses teknolojisi için tasarlanan bir 12 bitlik melez akım yönlendirmeli SAD kullanılmaktadır. Yapı bloklarında yapılan iyileştirmeler ve kullanılan farklı yöntemler, gerçekleştirilen SAD'ın serimindeki ilgili kısımlarda yer almaktadırlar. CADENCE Geleneksel Tümleşik Devre Tasarım Araçları kullanılarak serim sonrası benzetimleri yapılmaktadır ve SAD'ın performans karakteristikleri incelenmektedir.

1. INTRODUCTION

Nowadays the ever-dropping cost of VLSI circuits allows many analog functions to be done digitally [1]. Thus, many signal processing tasks have been shifted from the analog to the digital domain. However, in order to interface electronic systems with the real world, digital signals have to be translated into physical signals, which requires a conversion into analog signals. Figure 1.1 shows the information conversion cycle between analog and digital domains using data converters.

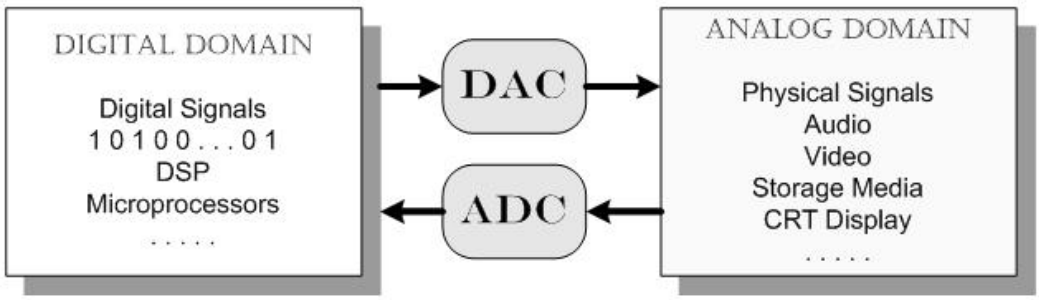

Figure 1.1 : Data converters as interface between the analog and digital domain.

Since data converters form the bridge between the analog and digital world their efficient implementation is also highly desirable. From this point of view, DACs thus have become key elements in many of today's electronic systems. They are used in a large variety of applications ranging from CD players to graphic cards, from wireless communication devices to automotive applications [2]. Since DACs provide an interface between the DSP systems and the outside world; high resolution and fast conversion rate are required. The demand for high-speed, high-resolution DACs has been strongly increased. Applications in the area of video, HDTV and wireless communications need DACs with a resolution of more than 10 bits and a conversion rate up to several hundreds of MHz [3].

Current-steering DACs are widely used, because they satisfy the requirements of high-speed and high-resolution necessary in communication applications. However, due to their numerous features and wide range of application uses, it is very difficult to define and to follow a single way in which current-steering DACs can be specified

and designed [4]. A similar systematic design methodology can be considered during design flow of a predetermined current-steering DAC architecture. Such a methodology is concerned with the entire mixed-signal system and requires a top-down design flow starting with DAC specifications, architectural decisions, cell-level circuit decisions and ending with DAC layout issues both for digital and analog parts of the system [5]. Thus, the selection of the proper methodology and the modeling of the system, prior to transistor level design, are mandatory. The use of DAC modeling tool is helpful to obtain converters having the best performance in terms of speed and accuracy [4]. Through these models (SPICE, Simulink etc. based models), the mixed-signal designs even with large complexity can be easily evaluated [6].

1.1 Purpose of the Thesis

The main objectives of this thesis are summarized as shown in the following sections:

In the past, most publications made use of segmentation for the design and the implementation of high performance DACs. Although this methodology is advantageous in most of the applications requiring high speed and high resolution, it suffers from the prolonged design time, complexity and the high cost. Thus, the use of this methodology for some applications is not efficient concerning the time and the cost. To overcome these problems in this thesis, new methodologies for the high-speed design of high-resolution DACs are considered.

Recent studies have shown that modeling is necessary for the design of complex systems like DACs. Most of the models constructed (mathematical or circuit based) cannot give a full view of the system's behavior. For this reason, models that will speed up the design and will give the complete behavior of the system prior to transistor level implementation are required.

High-speed and high-resolution applications require current-steering DACs. In previous studies, the main building blocks of current-steering DACs are analyzed and used in different implementations [7-25]. Even a saturation point is reached in the design of new blocks and the same building blocks are used in all applications without paying attention to the specs of each specific application [7], [14-16], [22],

[24]. Thus, the design of application dependent new blocks or a tradeoff between available similar blocks according to the specs of the application is necessary for high performance design of a DAC.

In all previous implementations, the main performance measure metrics have been power dissipation, area, supply voltage, dynamic performance etc. parameters. None of these studies have shown the time consumed for the design of the DAC, the degree of simplicity of the building blocks, the suitability of the designed converter with the requirements, the employed staff, and appropriateness of the process technology used with the overall cost i.e. is it necessary to realize a DAC using a 90nm process technology (or more expensive) and a dozen of designers instead of developing methodologies that make possible the realization of a DAC with same specs in a short time and implementation using a cheaper technology like 0.35µm CMOS process technology?

1.2 Background

Since the application field of digital-to-analog converters (DACs) is very widespread, a lot of alternative techniques are used to implement them according to the specifications of each given application. For applications in the area of video or modern communication systems, high-resolution/high-speed DACs with high performance are required. Because of their high-speed and cost effectiveness, CMOS current-steering DACs are ideal candidates for such applications [7].

As a principle, current-steering DACs employ matched current cells arranged in binary weighted or thermometer encoded elements that are steered to the DAC output depending on the digital input code [8]. In binary weighted implementation, one current source per bit is required, and each current source is twice the magnitude of the preceding smaller current source. Besides the advantages like simplicity and relatively smaller area, it suffers from large DNL error and increased dynamic error due to mismatches and large glitch energy. On the other side, in thermometer encoded implementation, the source elements are equally weighted and the switches turn on the number of sources addressed by the thermometer code to generate a particular output. The DNL error and switching dynamic errors are substantially

improved here at a cost of increased complexity, area and power consumption. However, to get the advantages of both implementations, most current-steering DACs are implemented using a segmented architecture [7-9]. Different structures can be derived from these basic architectures and some recent papers have used the idea of connection of subDACs in parallel to regroup the current cells enabling flexibility and smartness for the new architecture without manifesting any evidence of saved area and power efficiency [10], or to reduce the area occupied by the converter without resolving the mismatch problem between subDACs [11].

Conventional high-speed high-resolution CMOS DACs have employed a current-steering architecture with advantage of speed and linearity, while some performances have been degraded due to process variation, current source mismatch, and high glitch energy at outputs [12]. On the other hand, designing high-speed high-resolution data converters is more challenging with lower supply voltages made possible by the current-steering configuration [13].

The current-steering architecture can be implemented by either binary or thermometer coded architecture. To make use of the advantages offered by both architectures segmented architecture is used. Some methods are developed for the proper selection of the percentage of the segmentation between binary weighted and thermometer coded bits of a current-steering DAC [12-14].

It is well known that many kinds of MOSFET matching errors can be improved by using larger devices. So to improve matching between two MOSFET switches, we should make these devices large. Unfortunately, the increased gate capacitance of these larger devices slows down control signals and worsens timing errors [15]. In order to realize a fast settling time, the parasitic capacitance at the output node should be small. The parasitic capacitance at the common source node should also be small to minimize the recovery time of the voltage at this node during the switching transitions. This can be achieved by using small sized transistors for the current source and the current switch. However, short channel devices decrease the output impedance resulting in a degraded linearity [16]. To avoid the prolonged recovery time of the voltage at the common source node caused by the non symmetrical switching of the transistors in the differential switch pair it is necessary to prevent both transistors becoming off at the same time.

One of the most important factors that degrade the dynamic performance of a binary weighted converter is very high glitch energy caused generally by the imperfect synchronization of inputs and nonsymmetrical switch speed in the differential switches [17]. Very low glitch energy can be obtained by synchronizing and adjusting the input signals of the switching transistors of the DAC. This can be done by putting a synchronization circuit and a deglitch driver before switches [18-21]. All these implementations increase the complexity of the digital circuitry inside the DAC. There is insufficient research showing the reduction of the glitch energy by using analog, simple low cost circuits implemented in the DAC architecture.

Due to their numerous features and wide range of application uses, it is very difficult to define and to follow a single way in which DACs can be specified and designed [4]. However a similar systematic design methodology can be considered during design flow of a predetermined current-steering DAC architecture. Such a methodology is concerned with the entire mixed signal system and requires a top-down design flow starting with DAC's specifications, architectural decisions, cell-level circuit decisions and ending with DAC layout issues both for digital and analog parts of the system [5].

For high-speed and high-resolution applications current-steering DAC is the best choice since this configuration best suits those requirements. Although a lot of works and studies have been done, still new and useful improvements in architectures and calibration techniques can be developed. Some recent papers based on the segmented current-steering architectures [14], [22-23] and segmentation techniques [24] have offered attractive solutions for realization of different DACs. Also, calibration techniques [25-28] and proper design methodologies [29] have been developed to reduce various effects that decrease the performance of the DAC.

1.3 Hypothesis

In this thesis, different problems related to the design speed-up of high-resolution current-steering based DACs are addressed. The goal is to overcome these problems through novel solutions. The main problems and possible solutions to be considered here are summarized below.

a) Recent studies have shown that there are some main architectures used in the current-steering based DACs. All the works done are based on these architectures and from a point of view are very similar to each other, although the application fields may be very different. The lack of application related architecture or design methodology leads to new domains for research.

b) The use of standard building blocks in the implementation of a current-steering DAC, even when designed in a proper way, may result in an inefficient device, far away from the required application's specs. This is due to the insufficieny of these standard blocks to take a determinative place in the required tradeoff between speed, area, power consumption, resolution like parameters. Thus, simple, accurate and high performance circuits, capable of replacing low performance blocks can be considered.

c) Prior to transistor level design of the complex systems like DACs, some information about the behavior of the system is very useful. For this reason the behavioral model of the system is required. Unfortunately, the subject of DAC modeling has not got the necessary attention. For this reason, the construction of a universal DAC behavioral model that can speed up the design and gives a complete view of the DAC behavior is aimed. Math based, structural programs like SIMULINK® can be adequate tools for modeling.

d) The possibility of implementing a 12-bit hybrid DAC, using new architecture, methodology and suitable building blocks, in AMS 0.35μm CMOS process technology, achieving good performance, high speed design and small area is intended.

1.4 Overview of the Thesis

The thesis is organized as follows: Chapter 2 provides a short overview of digital-to-analog conversion and the most important performance specifications necessary for the evaluation of a DAC's performance. Chapter 3 covers briefly the most popular

architectures of the DAC and focuses on the current-steering architectures. In this chapter the generalized form of the proposed hybrid architecture to be used in the DAC implementation is introduced. In Chapter 4 the building blocks of the current-steering DACs are given in detail. New different building blocks are presented and their performance is discussed through simulations. Chapter 5 introduces a novel behavioral model developed by using SIMULINK®. Various current-steering DACs are modeled using the standardized blocks of the new model and the behavior of the DACs is investigated through simulations. Chapter 6 applies the architecture, designed blocks and the behavioral model presented in the previous chapters to an implementation of a 12-bit hybrid DAC. Also, the performance and the figure of merit of this work is discussed in this chapter. Finally, in Chapter 7 some conclusions and the main achievements of this thesis are summarized and some recommendations for further research are indicated.

2. DIGITAL TO ANALOG CONVERSION

2.1 Introduction

The purpose of digital to analog conversion is to transform the digital input signal into its corresponding analog output signal. A block diagram of a DAC can be seen in Figure 2.1..

Figure 2.1 : Block diagram of digital to analog converter.

Here, an N-bit digital word is mapped into a single analog signal (voltage or current). The digital signal is a binary coded representation of the analog signal using N bits. The leftmost bit of the digital word is usually called the most significant bit (MSB) and the rightmost bit is called the least significant bit (LSB) [30]. There are many different ways of coding the output signal and some different codes that can be used for 3-bit D/A conversion are shown in Table 2.1.

Table 2.1 : Digital codes used for 3-bit D/A conversion.

Decimal	Binary	Thermometer	Gray
0	000	0000000	000
1	001	0000001	001
2	010	0000011	011
3	011	0000111	010
4	100	0001111	110
5	101	0011111	111
6	110	0111111	101
7	111	1111111	100

2.2 Performance Specifications

Many specifications define a DAC and its performance. Dependent on the application, static and dynamic measures are used to characterize the quality and performance of a DAC. Performance related specifications of the DAC could be classified as general, static and dynamic specs.

2.2.1 General performance specs

2.2.1.1 Resolution

Resolution or the number of bits of a DAC is a term used to describe a minimum voltage or current that a DAC can resolve i.e. the accuracy that the generated analog output is represented in discrete steps.

2.2.1.2 Dynamic range

Dynamic range is defined as the ratio of the output signal's maximum level over the minimum level. For DACs, the dynamic range is related to the resolution of the converter. For example, an N-bit DAC can produce a maximum output of 2^N-1 multiples of LSBs and a minimum value of 1 LSB. Therefore, the dynamic range in decibels (dB) is simply [31]

$$DR = 20\,Log\left(\frac{2^N - 1}{1}\right) \qquad \textbf{(2.1)}$$

2.2.2 Static performance specs

The static behavior of a DAC is described by its transfer characteristics. Finite matching of the components used in the converter's implementation causes static errors. Static specs can be considered as the DAC's distortion performance at low frequencies [30], [32-33] or can be referred as DC specifications [34].

2.2.2.1 Linearity

Static DAC performance is characterized by differential nonlinearity (DNL) and integral nonlinearity (INL). The DNL is a measure of deviation of the actual DAC

step from the ideal step for one LSB i.e. DNL expresses how much the difference in output level between two adjacent codes deviates from the ideal LSB step. The INL is a measure of deviation of the DAC output from the ideal straight line. Ideal straight line can be drawn as a line between the minimum scale and full scale outputs or as a best-fit line to the DAC actual transfer characteristics. INL defines the linearity of the overall transfer curve. Both DNL and INL are measured in the unit of an LSB [30-32], [35]. Nonideal output of a DAC illustrating DNL and INL is shown in Figure 2.2.

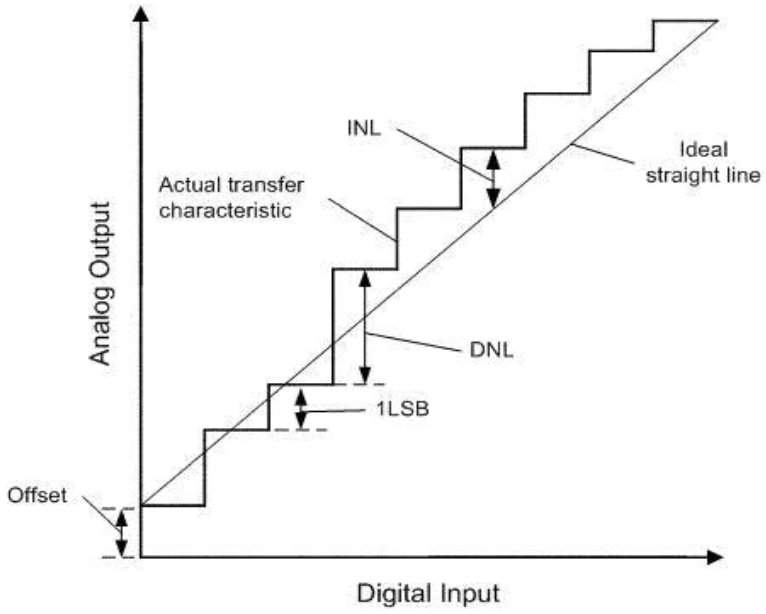

Figure 2.2 : Nonideal transfer characteristic illustrating DNL and INL.

DNL can be given in terms of LSBs with normalized form below,

$$DNL_k^{norm} = \frac{A_{k+1}^{actual} - A_k^{actual} - LSB}{LSB} \tag{2.2}$$

where $A_{k+1}{}^{actual}$ and $A_k{}^{actual}$ are analog outputs corresponding to adjacent codes of the converter. $DNL_k{}^{norm}$ is the differential nonlinearity normalized to LSB step.

INL can be also described as the accumulation of previous DNL errors [11], and can be given in terms of LSBs with the normalized form below,

$$INL_k^{norm} = \frac{A_k^{actual} - A_k^{ideal}}{LSB} = \sum_{j=1}^{k} DNL_j^{norm} \tag{2.3}$$

where A_k^{actual} and A_k^{ideal} are the actual and ideal analog outputs of the converter. INL_k^{norm} is the integral nonlinearity normalized to LSB step.

2.2.2.2 Monotonicity

The ability of the analog output of the DAC to increase/decrease with the increasing/decreasing digital code defines the monotonicity of the converter. The magnitude of DNL and INL determines the monotonicity of the DAC. Thus, for a DAC to be monotonic the following inequalities must be satisfied

$$\begin{aligned} |DNL| &\le 0.5LSB \\ |INL| &\le 1LSB \end{aligned} \qquad \textbf{(2.4)}$$

The relation is sufficient to guarantee the monotonocity, but the converter may be monotonic although this relation is not met [30].

2.2.2.3 Offset

For digital input *D=0* the analog output should be *A=0*. If the analog output is not equal to 0, an offset will be observed. The offset of a DAC is illustrated in Figure 2.2. and can be considered as a shift in the transfer characteristic of the converter.

2.2.2.4 Gain error

If the slope of the best-fit line through the transfer characteristic of a DAC is different from the slope of the best-fit line for the ideal case a gain error occurs. The gain error can be considered as the difference between the actual slope and ideal slope of the transfer characteristics of a DAC [31].

2.2.3 Dynamic performance specs

The dynamic performance of a DAC is determined by signal-dependent errors that occur when the input signals change rapidly. The impact of these signals and frequency dependent dynamic errors is mostly determined by the frequency response and speed of the analog components of the converter, and increases with signal amplitude and frequency. The influence of the dynamic nonlinearities on the distortion performance of the D/A converter can be described by using measures in

both the time and the frequency domain. Thus, dynamic performance specifications are given as a function of frequency, time, or even conversion data rate [30], [32-34].

2.2.3.1 Glitch

Glitch represents the signal dependent error injected from the digital inputs to the analog output during different code transitions in a binary weighted DAC. Because of the unmatched switching time of different bits it can reach its maximum at half scale conversion and for instant time periods false code can appear at the output i.e. for code transition 011…11→100…00 if MSB switches faster than the LSBs the code 11…111 may be present for a short time. In Figure 2.3, typical glitch behavior of a DAC output is illustrated. Glitch error is mainly caused by timing errors (delay between bits in digital part or timing mismatch in analog part) in a DAC. The impact on the output signal is determined by the glitch area (highlighted area) which is defined as the time integral of the analog output value (voltage or current) of the glitch transient and is expressed in pV-s or pA-s.

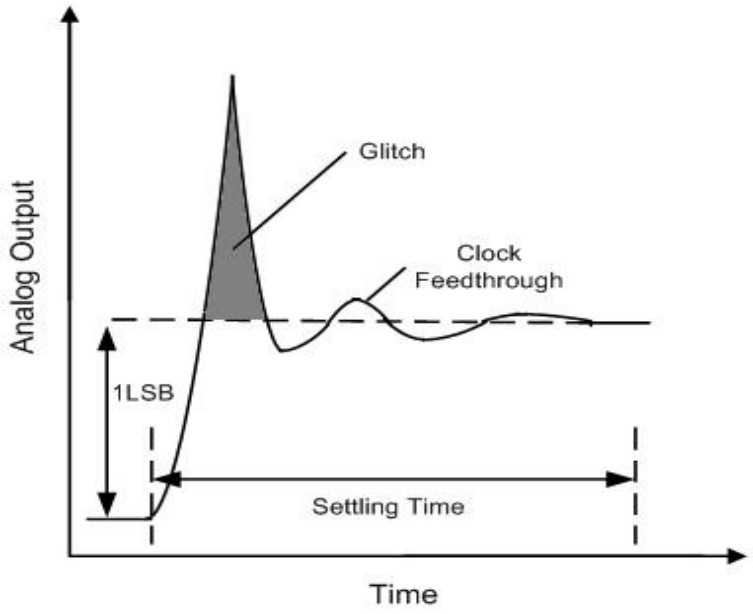

Figure 2.3 : Dynamic errors in a DAC.

2.2.3.2 Settling time

Settling time is the time it takes for the analog output to settle within a certain accuracy of the final value. Settling time determines the speed of the components of the DAC and to avoid the distortion on the analog output signal should be kept as

small as possible. A full-scale transition for a DAC's output illustrating the settling time is shown in Figure 2.3.

2.2.3.3 Feedthrough effects

Feedthrough effects can arise from two main reasons: parasitic capacitive coupling between digital and the analog part or capacitive coupling in switches of the clock. Clock feedthrough is not code dependent and does not introduce any extra noise or distortion in the Nyquist bandwidth. In DAC implementations, clock feedthrough is reduced by reducing the capacitive coupling of the switches to the output i.e. by decreasing the size of the parasitic capacitances of the switches by the means of small-sized switch transistors.

2.2.3.4 Signal-to-noise ratio (SNR)

The signal-to-noise ratio (SNR) is defined as the power ratio of the fundamental signal to the total noise, within a certain frequency band excluding harmonics, at the output when the input is a full-scale digital sinusoidal signal. The SNR of an ideal N-bit DAC is approximated as

$$SNR = 10\log\frac{P_S}{P_N} \cong 6.02N + 1.76(dB) \qquad \textbf{(2.5)}$$

where P_S is the power of the signal and P_N is the power of the total noise in the certain frequency band.

SNR depends on the resolution of the DAC and by definition includes other specifications like linearity, glitch, settling time, noise etc. It must be noted that a lower limit of SNR is dictated by the quantization noise [32].

2.2.3.5 Spurious free dynamic range (SFDR)

The spurious free dynamic range (SFDR) is the ratio between the power of the signal and the power of the largest unwanted distortion component (any harmonic or spurious tone) within a certain frequency band, as shown in Figure 2.4. SFDR is expressed

$$SFDR = 10\log\frac{P_S}{P_{MAX\_DIST}} \tag{2.6}$$

where P_S is the power of the signal and P_{MAX_DIST} is the power of the largest harmonic or spurious tone within the certain frequency band (mostly Nyquist frequency band).

SFDR is measured in dBc unit and shows how many dB below the value of the fundamental frequency is the largest harmonic's (spur's) level.

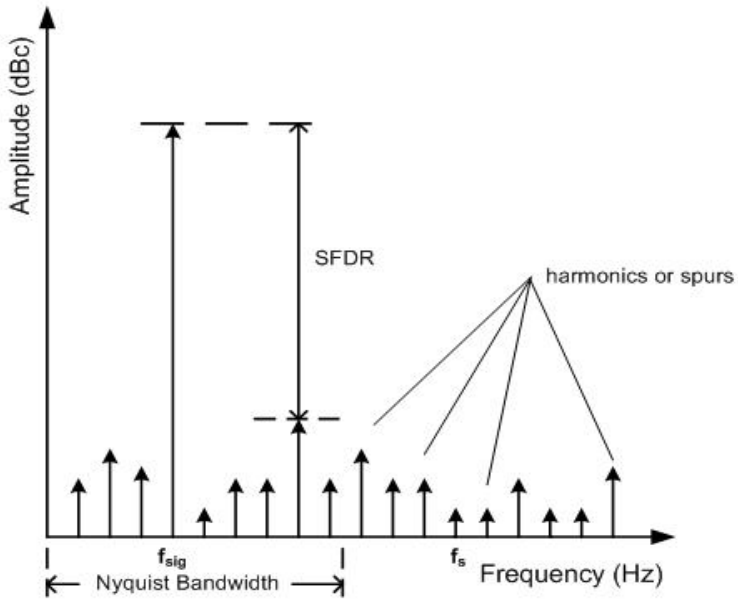

Figure 2.4 : Spurious free dynamic range.

2.2.4 Figure of merit (FoM)

FoM is used to characterize the performance of an implemented device relative to its alternatives. Figures of merit are defined for applications and are based on different performance parameters like resolution, bandwidth and power consumption [32-33]. The FoM used here is based on resolution, input signal frequency, power consumption and area efficiency, and is given by

$$FoM = \frac{2^N \cdot f_{in}}{Power \times Area} \tag{2.7}$$

where N is the resolution and f_{in} is the input signal's frequency for the implemented DAC device.

3. CURRENT-STEERING BASED DAC ARCHITECTURES

3.1 An Overview of DAC Architectures

DAC architectures can be diversified in a very wide range. Resolution, speed, application specifications and the process technology determine the selection of the DAC architecture to be used for a specific design. The most important architectures can be classified in 4 main groups:

- Resistive Network Based Architectures
- Switched-Capacitor Based Architectures
- Algorithmic or Cyclic Architectures
- Current-Steering Based Architectures

Resistive Network Based Architectures: The 2 most distinguished types based on this architecture are resistor string and R-2R ladder networks DACs. Both types use a resistor voltage divider network, connected between two reference voltages, to generate a complete set of voltages [1], [30-37]. The advantages of these architectures are guaranteed monotonicity, good DNL and operation at high speed, while the main drawbacks are; poor INL, matching errors, area and power consumption, code-dependent settling time and distortion. These converters are used in video processing applications where high resolutions are required.

Switched-Capacitor Based Architectures: These architectures are based on the charge redistribution or scaling and use switched capacitor circuits, where the charge stored on a number of binary weighted capacitors (or thermometer-coded capacitors) is used to perform the conversion [30-37]. The advantages of these architectures are simplicity in design and relatively good accuracy, while the main drawbacks are; matching errors, buffer required to drive loads, large transient currents drawn during

switching, and lack of high resolution because of the parasitic capacitances due to the operational amplifier used in the architecture. These converters are mainly used in the implementation of the multiplying DACs (MDACs) part of the algorithmic-pipelined ADCs.

Algorithmic or Cyclic Architectures: The fundamental type based on this architecture is cyclic DAC that uses only a couple of simple components (capacitors, switches, simple op-amps etc.) to perform the conversion. In this type, there is no weight directly associated with a specific bit and a serial input data is used to control the weights [31]. Another type of converter based on this architecture is pipelined DAC which in fact is a version of the cyclic converter, extended to N stages, where each stage performs one bit of the conversion. The signal is passed down through the pipeline and as each stage works on one conversion, the previous stage can begin processing another. Pipelining increases the throughput of the system to the cost of additional hardware and power consumption [30-31]. The advantages of these architectures are compact circuit and low number of circuit components for cyclic DAC and increased throughput of the whole system, after an initial delay for pipelined DAC. While the main drawbacks are; increased conversion time for cyclic DAC, required tradeoff between speed and chip area, converted output with a latency time for pipelined DAC, and required extremely high accuracy of components (op-amp gain etc.) to produce high resolutions for both types.

Current-Steering Architectures: This architecture is based on the current-steering technique and requires precision current sources that are summed in different ways [30-37]. The most important types implemented using these architectures are binary weighted, thermometer coded, segmented and hybrid current-steering DACs. The advantages in common for all types are high-speed operation and high-resolution, while drawbacks are; mismatching and finite output impedance of current sources.

Current-steering architectures are good candidates for high conversion rate and high-resolution applications like wired and wireless communications, and digital audio and video signal processing etc. For this reason, study of these architectures is one of the scopes of this thesis and will be covered with details in the following sections.

3.2 Binary Weighted Current-Steering DAC

An N-bit binary weighted current-steering DAC is shown in Figure. 3.1. Every switch steers a binary weighted current to the output i.e. every steered current value is twice as large as the next less significant bit current value. The switches are controlled by the digital input code, which can be a simple binary number. The converter requires N current sources of different sizes with the size of the largest current source equal to $I_{MSB}=2^{N-1}I_{LSB}$, where I_{MSB} and I_{LSB} are the current outputs steered by the most and less significant bits, respectively. It must be noted that in Figure 3.1 $I=I_{LSB}$.

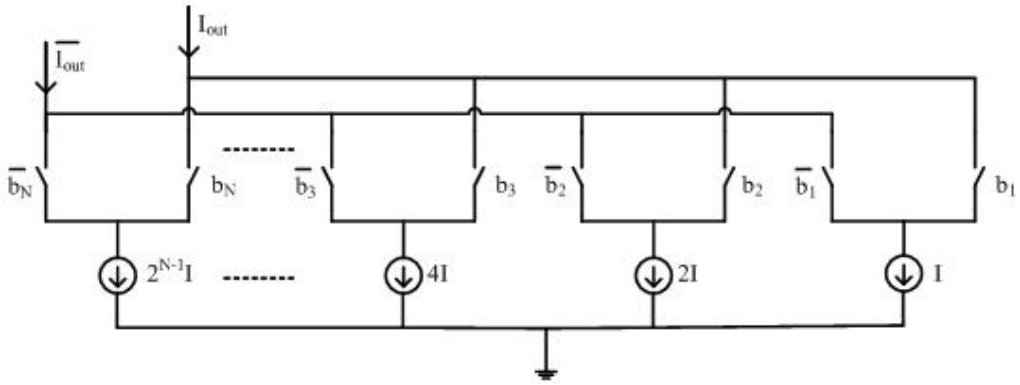

Figure 3.1 : An N-bit binary weighted current-steering DAC.

The output current for the N-bit binary weighted current-steering is given as;

$$I_{out} = I \times \sum_{i=1}^{N} b_i \cdot 2^{i-1} \qquad \textbf{(3.1)}$$

The advantages of the binary weighted current-steering DAC are simplicity, small area and power dissipation. However, in this type of DAC, monotonicity is not guaranteed and it suffers from large DNL and presence of glitches that degrades its dynamic performance [32].

3.3 Thermometer Coded Current-Steering DAC

An N-bit thermometer coded current-steering DAC as shown in Figure 3.2 employs 2^N-1 equal current sources, each having a unit value of current, I. For this reason, the digital input will be in the form of a thermometer code. Further, a thermometer decoder (not shown), which generates the switch control signals, is used to convert

binary inputs into thermometer codes. The analog output current is defined in equation (3.2).

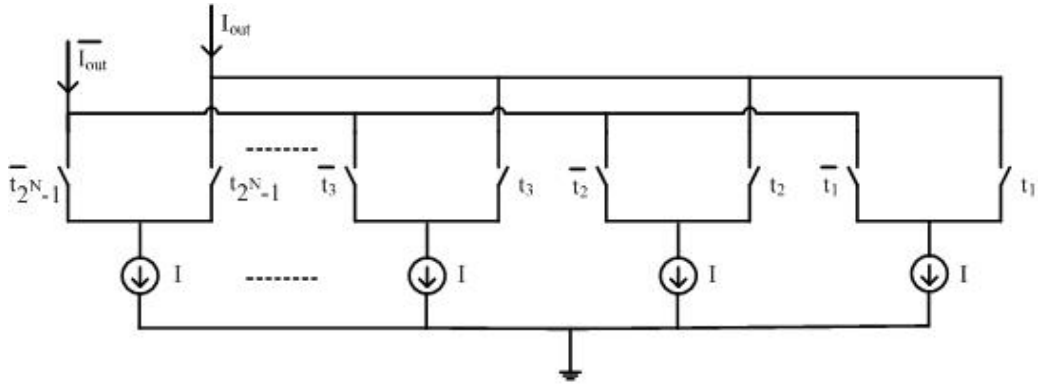

Figure 3.2 : An N-bit thermometer coded current-steering DAC.

$$I_{out} = I \times \sum_{i=1}^{M} t_i \qquad \textbf{(3.2)}$$

where $M=2^N-1$ is the number of thermometer coded bits, t_i $(i=1,....,M)$ are the thermometer coded bits, and I is the unit current.

The advantages of thermometer coded current-steering DAC are, guaranteed monotonicity, good DNL and no glitches i.e. small dynamic switching errors. However, it suffers from the complexity, large area and power consumption increased due to thermometer decoder.

3.4 Segmented Current-Steering DAC

To make use of the advantages offered by both binary weighted and thermometer coded architectures, current-steering DACs are implemented using segmented architecture. Figure 3.3 shows a block diagram of an N-bit segmented current-steering DAC. The N-bit input binary data is segmented into the M least significant bits switching binary weighted current sources and N-M most significant bits are thermometer coded to switch $2^{N-M}-1$ unary current sources. The output current of the DAC is given by;

$$I_{out} = I_{LSB} \sum_{i=1}^{M} b_i \cdot 2^{i-1} + 2^M I_{LSB} \sum_{i=M+1}^{N} b_i \cdot 2^{i-(M+1)} \qquad \textbf{(3.3)}$$

where $b_i 2^{i-1}$ is the decimal number corresponding to i^{th} bit and I_{LSB} is the least significant bit current. The first term corresponds to the output current of the M-bit binary part and the second term corresponds to the output current of the (N-M)-bit thermometer coded part of the segmented DAC.

The thermometer decoder is used to convert *N-M* binary codes into 2^{N-M}*-1* thermometer codes, while dummy decoder is used in the binary weighted part of the segmented DAC to equalize the latency coming from thermometer decoder. Swing reduced drivers (SRDs) are placed before the switches to reduce the clock feedthrough, and to increase the switching speed. All details about the operation and the design of the decoder and swing reduced driver are examined in the next section of this thesis.

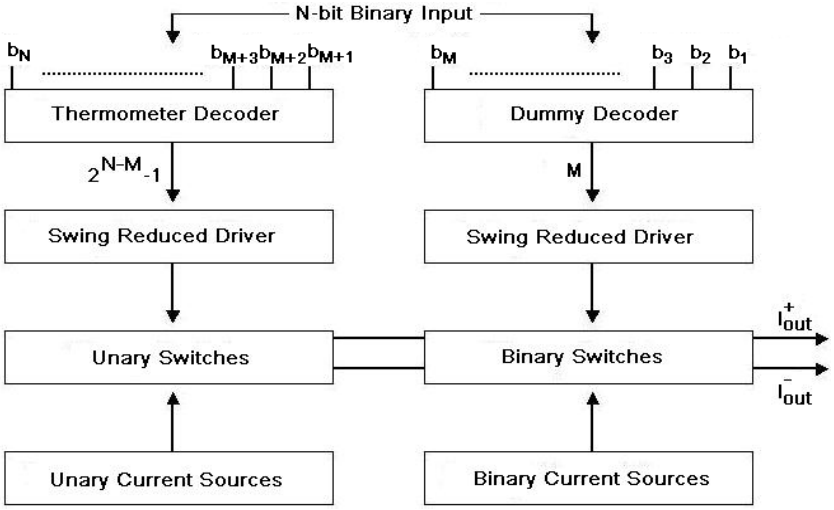

Figure 3.3 : Segmented current-steering DAC.

Determination of the level of the segmentation is of interest to achieve the highest performance for segmented current-steering DAC. Even some methods are developed for the proper selection of the percentage of the segmentation between binary weighted and thermometer-coded bits of a current steering DAC. Based on the area consumption and considering the static performance of the converter, the normalized required area versus percentage of segmentation for a 10-bit current-steering DAC is shown in Figure 3.4 [38].

It must be noted that the required area in Figure 3.4 is normalized to A_{unit} (the minimum area required by the thermometer architecture to obtain *DNL=0.5LSB*).

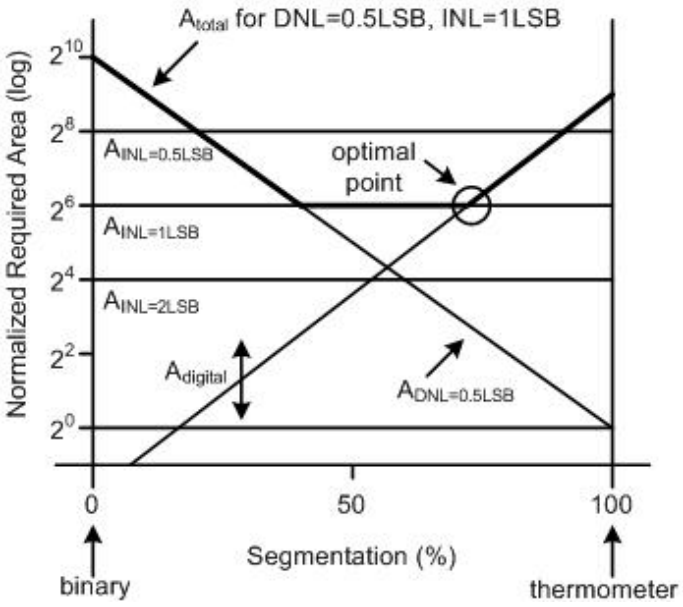

Figure 3.4 : Normalized required area versus percentage of segmentation [38].

A minimal chip area that still guarantees the required static performance (INL and DNL) and has an optimal frequency domain performance (optimal area necessary for the digital circuitry i.e. thermometer decoder) is aimed [32]. The accuracy of such a method is shown in the design of different applications using segmented current-steering DACs [12], [14].

3.5 Hybrid Current-Steering DAC

Different hybrid current-steering DACs can be derived using the basic current-steering converters given in the above sections. Parallel current-steering DACs can be obtained by the connection of subDACs in parallel as in [10], where the current cells are properly regrouped to enable flexibility and smartness for the new converter. But, there is a lack in saved area and the power efficiency for these converters. Another kind of hybrid current-steering DAC based on the parallel connection of non-matched thermometer coded subDACs is given in [11].

3.5.1 Current-mode current-steering DAC

Figure 3.5 shows a block diagram of an N-bit hybrid current-mode current-steering DAC. The architecture consists of M parallel weighted thermometer coded h-bit

subDACs. The current outputs generated at the output of each subDAC are added together to come out with the current output of the parallel DAC.

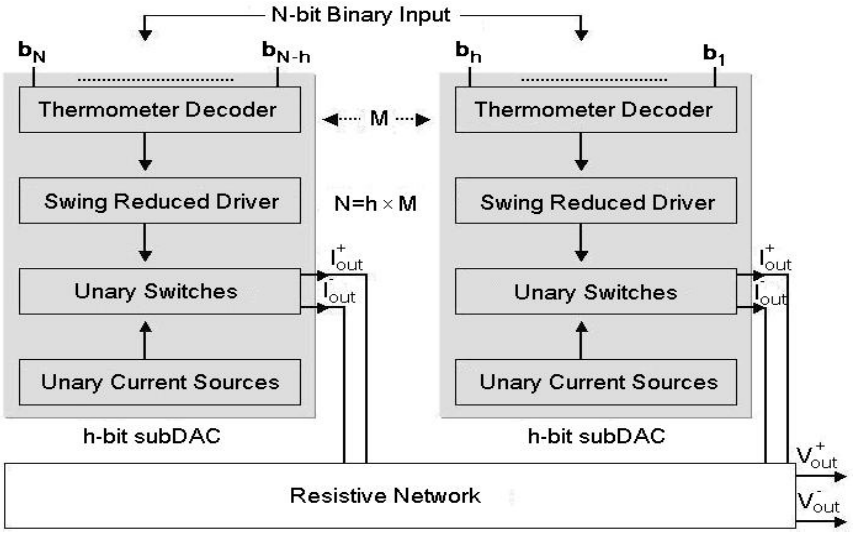

Figure 3.5 : Hybrid current-mode current-steering DAC.

The output current of the DAC is given by;

$$I_{out} = \left(\begin{array}{l} I_{LSB} \sum_{i=1}^{h} b_i \cdot 2^{i-1} + 2^{h} I_{LSB} \sum_{i=h+1}^{2h} b_i \cdot 2^{i-1} + .. \\ ... + 2^{N-h} I_{LSB} \sum_{i=N-h+1}^{N} b_i \cdot 2^{i-1} \end{array} \right) \quad \textbf{(3.4)}$$

where $b_i 2^{i-1}$ is the decimal number corresponding to i^{th} bit and I_{LSB} is the least significant bit current.

The h-bit input binary data of each subDAC are thermometer coded to switch 2^h-1 unary current sources. Note that in practical designs the selection of parallel weighted subDACs, M and the number of bits of each subDAC, h must be maintained within reasonable limits that satisfy the decreased area and simplicity advantages offered by the hybrid architecture.

3.5.2 Voltage-mode current-steering DAC

Figure 3.6 shows a block diagram of an N-bit hybrid voltage-mode current-steering DAC. The proposed architecture consists of M parallel matched thermometer coded h-bit subDACs and a resistive network with weighted resistors connected to V_{DD}. Resistive network is used to scale the output of each identical subDAC according to

the expected N-bit resolution DAC output. Thus, each current output generated at the output of each subDAC is connected through appropriately scaled resistors to conclude in the voltage-mode output of the DAC. Actually, current outputs of subDACs are converted to properly weighted voltages and then are added to each other. The output voltage of the DAC is given by;

$$V_{out} = V_{DD} - \left[\begin{array}{l} R_1 \sum_{i=1}^{h} b(i) I_{LSB} + (R_1 + R_2) \sum_{i=h+1}^{2h} b(i) I_{LSB} + .. \\ + (R_1 + R_2 + ... + R_M) \sum_{i=N-h+1}^{N} b(i) I_{LSB} \end{array} \right] \quad \textbf{(3.5)}$$

where $b(i)$ is the decimal number corresponding to i^{th} binary bit and is equal to $b(i)=2^i*b_i$ and I_{LSB} is the unary current of each matched subDAC. $R_1=R_{unit}$ represents the unit resistor of the network and R_i $(i=2, 3...M)$ are the network resistors weighted with respect to R_{unit} according to the following equation.

$$R_i = 2^{(i-1)h} R_{unit} - \sum_{j=1}^{i-1} R_j \quad \textbf{(3.6)}$$

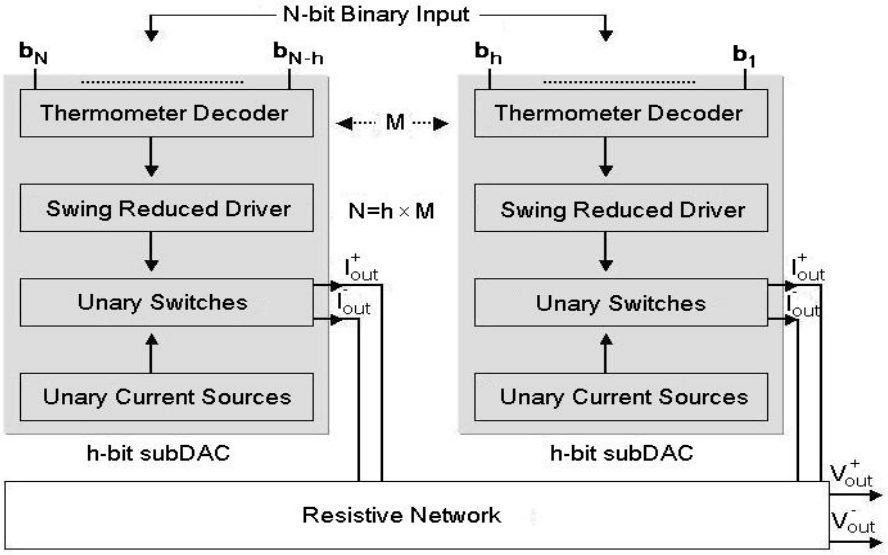

Figure 3.6 : Hybrid voltage-mode current-steering DAC.

The h-bit input binary data of each subDAC are thermometer decoded to switch 2^h-1 unary current sources.

Note that in practical designs the selection of parallel matched subDACs, M and the number of bits of each subDAC, h must be maintained within reasonable limits that

satisfy the decreased area, simplicity and relaxed resistor scaling advantages offered by the hybrid architecture.

4. CURRENT-STEERING DAC BUILDING BLOCKS

4.1 Introduction

Regardless of which architecture is used for the implementation of the current steering DAC the core part of it is current source cell and switches. Mainly, steered current sources based on the differential pair are used. As it can be seen from the architectures given in the previous section the more complex the converter is the more increased is the number of building blocks. Actually, the blocks used in most current-steering DACs are separated into two main groups: analog and digital blocks. Analog blocks include current sources, switches and biasing circuitries, while digital blocks are binary-to-thermometer decoder, swing reduced drivers and latches. A pattern of current-steering DAC building blocks is shown in Figure 4.1.

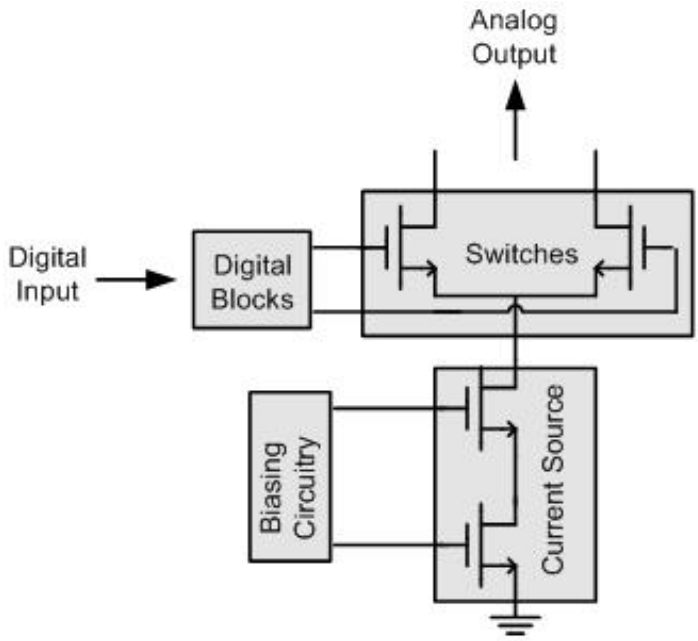

Figure 4.1 : Current-steering DAC building blocks.

4.2 Current Sources

The unit current source to be used in the converter can be constructed in several different ways. The simple or cascode current mirrors are the basis for making unity current sources with MOS transistors. It is worth using current sources with high output resistance to secure linearity but in many situations it is necessary to ensure the best trade-off between speed and accuracy [33]. Since the ideal current source should have infinite output impedance, the cascode transistors are used to increase the output impedance. The finite output resistance strongly affects the linearity of the converter. This is primarily because the output resistance of the converters is signal-dependent [30]. If the output current-summing node of a current-steering array experiences large voltage excursions, then a type of integral nonlinearity arises from the finite output impedance of the current sources. As the output varies between zero and full-scale, different impedances are switched to the output node, thereby introducing variations in the equivalent load resistance and hence nonlinearity in the output voltage [37]. The output impedance of a current-steering DAC is setting a lower limit for the second-order distortion. At low frequencies, it is not much of a factor. The output resistance can be quite high. At higher frequencies, the capacitances gravely reduce the output impedance [39]. It is clear that both linearity and output resistance of current output stage depend on the performance of the current mirrors used and both must be sufficiently high [40]. Some current source topologies suitable for current steering DACs are summarized below. The output resistance performance is evaluated for these current sources.

4.2.1 Simple current source

A simple current source or a basic current mirror is shown in Figure 4.2. Since gate-to-source voltages are equal, for M_1 and M_2 matched transistors and M_2 operating in the saturation region, the same current flows through M_1 and M_2. The output current is equal to the drain currents of the transistors and without considering the channel length modulation is approximately given by

$$I_{out} = I_{bias} = I_{D1} = I_{D2} = \frac{K_n}{2}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2 \qquad \textbf{(4.1)}$$

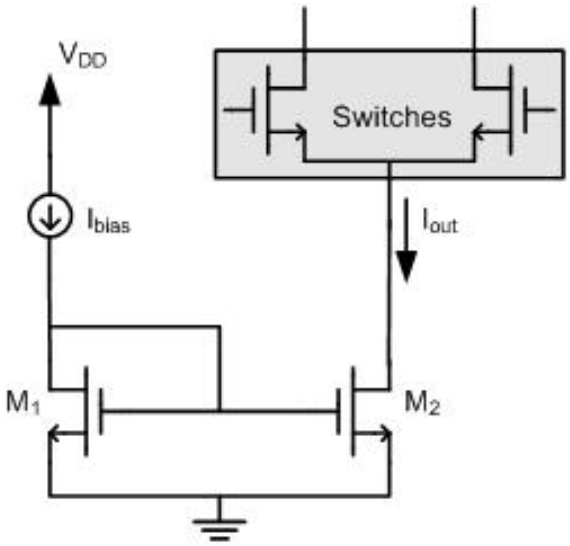

Figure 4.2 : Simple current source.

where V_{GS} is the gate-to-source voltage, W and L are the dimensions of the matched transistors, and K_n and V_{Tn} are the process transconductance parameter and threshold voltage of the NMOS transistor, respectively. $K_n=\mu_n C_{ox}$ where μ_n is the electron mobility and C_{ox} is the gate oxide capacitance per unit area.

The output resistance of the simple current source is approximately equal to the output resistance of the M_2 transistor and is given by

$$R_{\text{oCS}} = r_{o2} \cong \frac{1}{\lambda \cdot I_{out}} \tag{4.2}$$

where λ is the channel length modulation parameter.

It must be noted that the output resistance of the MOS transistors is relatively small and because of this finite output resistance, when the output voltage of the current source varies the output current changes too [41].

4.2.2 Basic cascode current source

To increase the output resistance and the accuracy of the current source cascode configuration is used. A basic cascode current source is shown in Figure 4.3

The output resistance for the cascode current source, when body effect is neglected, is given by

$$R_{\text{oCS}} \approx \left(g_{m4} r_{o4}\right) \cdot r_{o2} \tag{4.3}$$

where g_{m4} and r_{o4} are the transconductance and the output resistance of the M_4 cascode transistor.

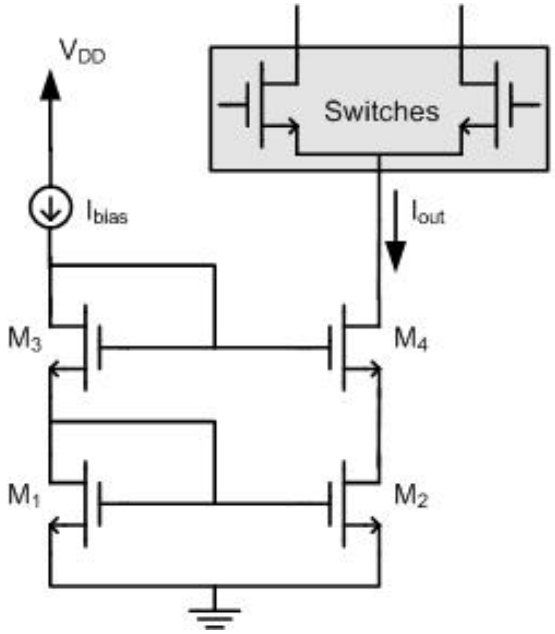

Figure 4.3 : Basic cascode current source.

It is clear that the output resistance is increased by a factor of $g_{m4}r_{o4}$ i.e. output current error is lowered $g_{m4}r_{o4}$ times in expense of a higher minimum supply voltage $2V_{Tn}+V_{DSsat}$ compared with the simple current source.

4.2.3 Low-voltage cascode current source

In practical designs, it is more convenient to use low-voltage cascode current source rather than basic cascode one. Low-voltage cascode current source is shown in Figure 4.4. It can be considered a version of basic cascode operating with lower supply voltage (one threshold voltage less than basic cascode) and preserving the same properties i.e. output resistance is the same [31],[41].

For a proper operation of the low-voltage cascode current source the following conditions must be satisfied

$$V_{bias} - V_{GS3} \rangle V_{GS1} - V_{Tn1} \tag{4.4}$$

$$V_{GS1} \rangle V_{bias} - V_{Tn3} \tag{4.5}$$

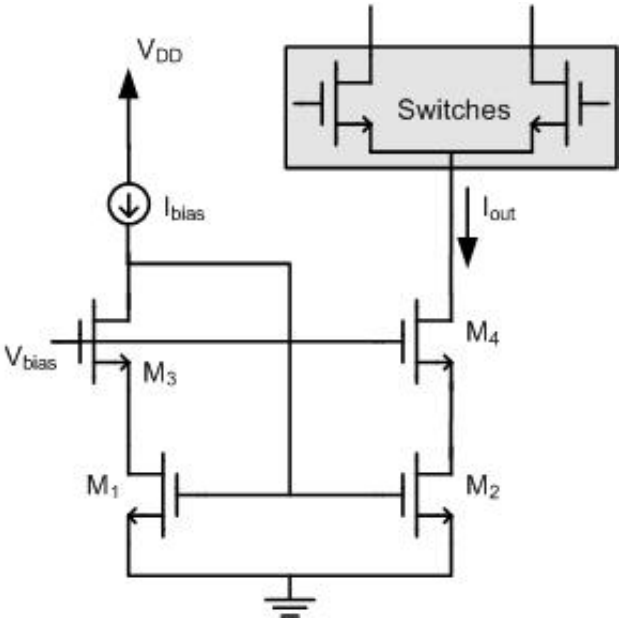

Figure 4.4 : Low-voltage cascode current source.

From (4.4) and (4.5) it is obvious that biasing voltage V_{bias} must be selected within the limits determined by

$$V_{GS1} + V_{Tn3} \rangle V_{bias} \rangle V_{GS1} + V_{GS3} - V_{Tn1} \tag{4.6}$$

4.2.4 Regulated cascode current source

To further increase the output impedance, a negative voltage-voltage feedback amplifier is employed. The amplifier stabilizes output current when output voltage varies [40-42]. Figure 4.5 shows a regulated (active feedback) cascode current source that uses a common-source amplifier. M_3 and M_4 make up the negative feedback loop.

The minimum supply voltage is the same with that of the basic cascode current source $2V_{Tn}+V_{DSsat}$ and the output impedance is given by

$$R_{oCS} \cong A_v \left(g_{m4} r_{o4}\right) \cdot r_{o2} \tag{4.7}$$

where $A_v=g_{m3}r_{o3}$ is the gain of the amplifier.

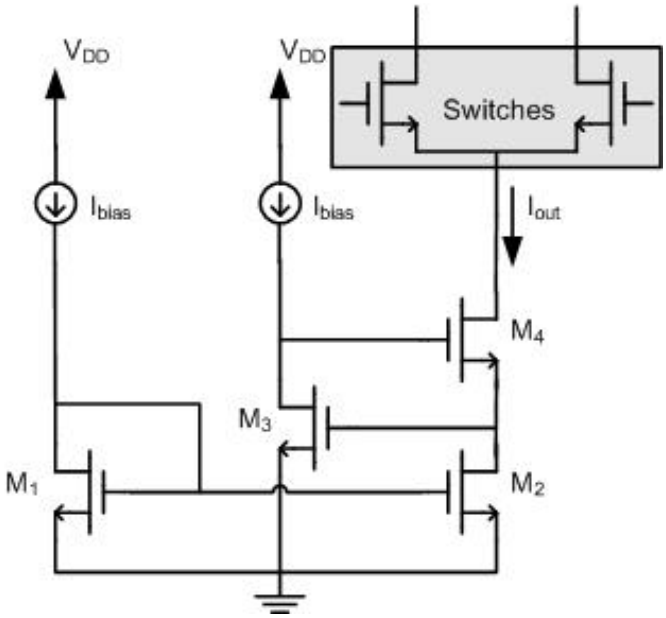

Figure 4.5 : Regulated cascode current source.

4.2.5 Proposed current source

The proposed current source [43] consists of a low-voltage cascode input stage and a feedback amplifier as shown in Figure 4.6. The input (reference) circuitry composed of M_{P1}, M_7, M_{P2}, M_8 and M_1 achieves $V_{DS1} \approx V_{DSsat8}$, as a result of matching, M_7 and M_8, as follows

$$V_{DS1} = V_{GS7} - V_{GS8} = \sqrt{\frac{2 \times 4I_{ref}}{\beta}} - \sqrt{\frac{2 \times I_{ref}}{\beta}} = \sqrt{\frac{2 \times I_{ref}}{\beta}} = V_{GS8} - V_{Tn} = V_{DSsat8} \qquad \textbf{(4.8)}$$

where $\beta = K_n(W/L)$ is the device transconductance parameter.

The property in (4.8) enables low-voltage operation for the proposed current source.

The differential amplifier ($M_5 \equiv M_6$) guaranties the $V_{DS2} = V_{DS1}$ equality to increase the current transfer accuracy ($I_{out} = I_{ref}$ for $M_1 \equiv M_2$), besides enhancing the output impedance [40], [44]. Thus, output voltage swing is maximized. Keeping $V_{DS4} = V_{DS3}$ is also aimed, to minimize the systematic offset of the differential amplifier. This is important in achieving more accurate $V_{DS2} = V_{DS1}$, thus $I_{out} = I_{ref}$ equalities. It is obvious that, $V_{DS4} = V_{GS9} + V_{DS2}$ and $V_{GS7} = V_{GS8} + V_{DS1}$. Considering that, nominally $V_{DS2} = V_{DS1}$ and $I_{out} = I_{ref}$, it is obvious that matching M_8 and M_9 will yield $V_{DS4} = V_{GS7}$. Then, since $V_{DS3} = V_{GS3}$ (M_3 is diode connected), achieving $V_{GS3} = V_{GS7}$ is enough to

satisfy $V_{DS4}=V_{DS3}$. If, for instance, tail current of the differential pair is selected $4I_{ref}$ (i.e. $I_{D3}=2I_{ref}$), then setting $(W/L)_7=2(W/L)_3$ will achieve $V_{DS4}=V_{DS3}$.

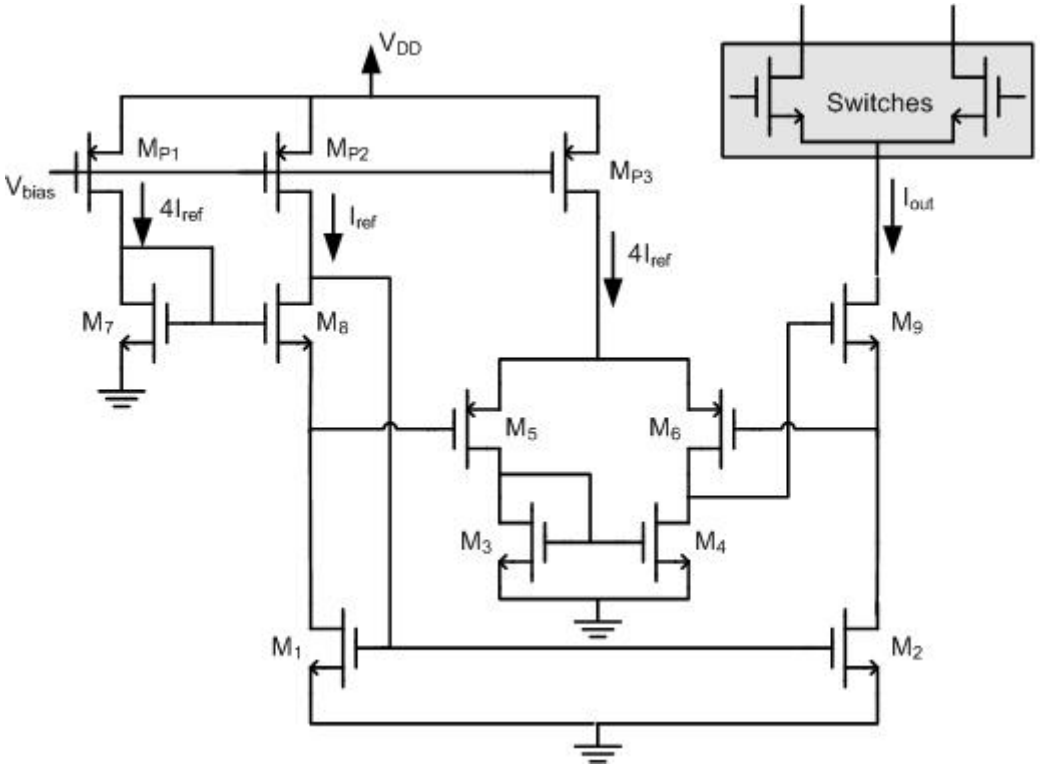

Figure 4.6 : Proposed current source.

It is critical to keep M_5 and M_6 in saturation, because their gate voltages are low and drain voltages are higher. It is obvious that, $V_{DG6}=V_{GS9}$ and this value may be larger than $|V_{Tp6}|$ and drive M_6 in triode region. The same is valid for M_5 (since $V_{D5}=V_{D6}$ as a direct result of achieving $V_{DS4}=V_{DS3}$). To avoid this, the bodies of M_5 and M_6 are deliberately connected to V_{DD}, such that their threshold voltage increases [40]. This slightly degrades the equivalent g_m, but in turn enables operation in saturation region.

The differential gain that is required for the enhancement of the output impedance can be given as

$$A_{vd} = \frac{v_o}{v_{id}} = g_m\left(r_{o4} \| r_{o6}\right) \tag{4.9}$$

where $g_m=g_{m5}=g_{m6}$ is the transconductance of the matched transistors M_5 and M_6, and r_{o4} and r_{o6} are the output resistances of M_4 and M_6, respectively.

The output resistance for the proposed current source can be given by

$$R_{oCS} \approx A_{vd}\left(g_{m9}r_{o9}\right)\cdot r_{o2} \tag{4.10}$$

where A_{vd} is the gain in (4.9), r_{o2} output resistance of M_2 and g_{m9} and r_{o9} transconductance and output resistance of M_9, respectively. For simplicity, body effect is omitted and the source follower gain (from gate to source of M_9) is assumed unity in the calculations above.

All transistors are kept in saturation to achieve high output impedance.

4.2.6 Design of current source

After the selection of the architecture to be used in the converter, the design of the basic building block that is the unit current cell must be performed. The goal of this step is to determine the dimensions of the transistors according to the design constraints of the DAC. The main constraints to be considered are [36]:

- area: must be minimized
- power consumption: must be minimized
- output impedance: must be maximized
- settling time: must be minimized
- glitches: must be minimized
- good matching and performance with a high parametric yield: must be guaranteed

4.2.6.1 Sizing current source transistor

The dimensions of the current source transistor are dependent on the full-scale output current of the DAC and the technology in which the converter will be implemented [32]. The minimum area of current source is determined according to the mismatch equations derived using the standard current deviation and mismatch parameters [45] and is given by

$$\left(WL\right)_{\min} = \frac{1}{2\left(\sigma_{I_{LSB}} / I_{LSB}\right)^2}\left[A_\beta^2 + \frac{4A_{VT}^2}{\left(V_{GS}-V_T\right)_{CS}^2}\right] \tag{4.11}$$

where (σ_{ILSB}/I_{LSB}) is the normalized standard deviation of the unit current source, A_{VT} and A_{β} are technology-dependent parameters that cannot be controlled over and $(V_{GS}-V_T)_{CS}$ is the gate overdrive voltage of the current source. Details on the matching properties of MOS transistors are given in Appendix A. It must be noted that the distance component is extracted and is not shown in equation (4.11). The relative effect on the mismatch due to the distance is only significant for large devices with considerable spacing [45].

Another constraint that determines the size of current source transistor is defined by the full scale current $I_{FS}=I_{LSB}(2^N-1)$ and designs the W/L ratio of the current source as given by

$$\frac{W}{L} = \frac{2I_{FS}}{K_n\left(2^N-1\right)\left(V_{GS}-V_T\right)_{CS}^2} = \frac{2I_{LSB}}{K_n\left(V_{GS}-V_T\right)_{CS}^2} \qquad \textbf{(4.12)}$$

where K_n is the process transconductance parameter of the current source transistor (NMOS in this case), N is the resolution of the DAC and I_{LSB} is the unit current.

From (4.11) and (4.12) it is obvious that extremely tight tolerances on current mismatches will result in very large corresponding devices. Increasing overdrive voltage $V_{ov}=V_{GS}-V_T$ can improve matching, but this uses more power and reduces headroom. Thus, the value for the gate overdrive voltage is determined as a trade-off between the area of the current source transistor and the limit imposed by the fact that all the transistors have to operate in the saturation region for a given supply voltage [32]. L is strongly influenced by output impedance concerns. A small W limits drain capacitance, which affects output impedance modulation.

4.2.6.2 Cascode transistor

The current flowing through the cascode transistor is the same with the current I_{LSB} of the current source. The dimensions of this transistor mainly will be determined by the dynamic performance constraint i.e. output impedance. However, the objective is to find a tradeoff between the required output impedance and a small parasitic drain capacitance with minimum area for the transistor. It must be noted that the gate-length L of the cascode transistor must be larger than the minimal value allowed, since the output resistance of this transistor is directly proportional to this parameter.

4.2.7 Output resistance evaluation

The current sources given in the above sections are sized according to the requirements of a current-steering DAC's current source. Thus, using the unit current cell's specifications given in Table 4.1 and equations (4.11) and (4.12), the dimensions of the current source transistor are determined. In addition, the dimensions of the cascode transistors are derived considering the given constraints discussed above and the current flowing through them.

Table 4.1 : Unit current cell specifications.

Parameter	Symbol	Value
threshold voltage process-related mismatch constant	A_{VT}	9.5 mVμm
transconductance parameter process-related mismatch constant	A_{β}	%0.7 μm
unit current relative standard deviation	σ_I/I	0.35%
current source transistor overdrive voltage	$(V_{GS}-V_T)_{CS}$	0.25V
cascode transistor overdrive voltage	$(V_{GS}-V_T)_{CAS}$	0.3V
supply voltage	V_{DD}	3.3V
unit current	I_{LSB}	5μA

List of the dimensions of the current source and cascode transistors used in the above current sources are given in Table 4.2.

Table 4.2 : Transistors' dimensions.

Tr.	W(μm)	L(μm)
M_1	14.7	15.75
M_2	14.7	15.75
M_3	0.7	1.05
M_4	0.7	1.05
M_8	0.7	1.05
M_9	0.7	1.05

M_1-M_2 are the current source transistors in all given topologies. M_3-M_4 are the cascode transistors of all topologies except the proposed current source whose

cascode transistors are M_8-M_9. The dimensions of the remaining transistors (active feedback amplifier and biasing transistors) are determined considering the relationships given for the proper operation of the respective topology.

Using the calculated transistors' dimensions and the AMS 0.35µm CMOS technology process parameters, the output resistances of the current sources are simulated with SPICE. The simulation results are shown in Figure 4.7.

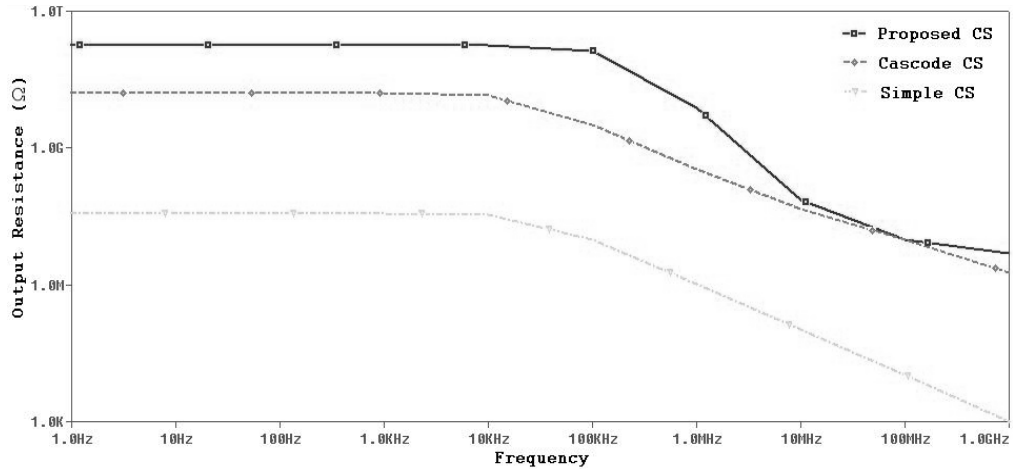

Figure 4.7 : Output resistances of the current sources.

As it can be seen from Figure 4.7, the effect of the cascode and the feedback is obvious in the output resistance value and the bandwidth. Simple current source exhibits a very poor performance even at low frequencies, output resistance is 35.71MΩ, while output resistances for cascode and proposed current source are 15.77GΩ and 174.73GΩ, respectively. The active feedback increases the output resistance and bandwidth (feedback moves the dominant pole at a higher frequency). The increase in this case is mainly determined by the amount of feedback.

4.3 Switches

Switches used in current-steering DACs are implemented with MOS transistors as shown in current cell of Figure 4.8. Realization of switches in CMOS is easy and the switching properties of MOS transistors are good. The use of differential pair switches is necessary to guarantee a continuous flow of current through current source. Thus, the proper design of the differential pair (switches+current source) must be considered separately. In general, the resolution and errors (INL and DNL) in the DAC are determined by the current source. Instantly DNL results from device

mismatches in the current source and can be minimized by increasing the device channel length of the tail transistor. Unfortunately, increasing the device channel length results in increasing parasitic capacitances and consequently, settling time [46]. Thus, the optimization of the device size is required to minimize the problems coming from device mismatch and settling time.

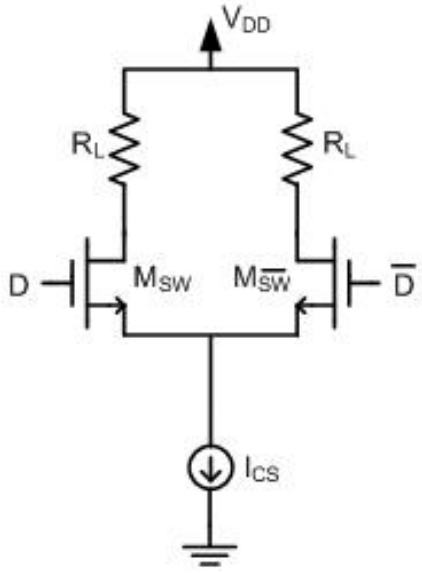

Figure 4.8 : Current cell.

It is well known that many kinds of MOSFET matching errors can be improved by using larger devices. Therefore, to improve matching between two MOSFET switches, we should make these devices large. Unfortunately, the increased gate capacitance of these larger devices slows down control signals and worsens timing errors [15]. In order to realize a fast settling time, the parasitic capacitance at the output node should be small. The parasitic capacitance at the common source node should also be small to minimize the recovery time of the voltage at this node during the switching transitions. This can be achieved by using small-sized transistors for the current source and the current switch. However, short-channel devices decrease the output impedance resulting in a degraded linearity [16]. To avoid the prolonged recovery time of the voltage at the common source node caused by the non-symmetrical switching of the transistors in the differential switch pair it is necessary to prevent both transistors becoming off at the same time.

Using the right switching strategy avoids pushing the transistors into the triode region when the current source is not being used and keeps the transistors in

saturation. To obtain this the current source is not switched off but is routed towards a dummy connection [33].

As it is obvious from all simulations, for the current-steering cell, the output impedance depends on whether the switch transistors are in the saturation or the linear region when they are on. For a given current, this value can be increased by increasing the length of the on switch and source transistor or the width of switches. For a MOS implementation, this implies that the size aspect ratio of the transistors must be large. However, large switches increase clock feedthrough due to the gate capacitances. A tradeoff has to be done. To maximize speed, switches usually employ minimum length and the transistors in the source circuit are sized to provide adequate output impedance [30], [37].

4.3.1 Design of the switches

It is important to have switches that can be synchronized, which means that a small spread of offset voltage is required. An equation that describes the spread of offset voltage in a differential pair as a function of device size is given by

$$\sigma_{Voff} = \frac{A_{VT}}{\sqrt{WL}} \tag{4.13}$$

From (4.13) it can be seen that synchronization would be better with larger switches, since large devices will have better offset matching. Besides this fact, the gate capacitance of a large device increases and for a given gate drive, it will not turn on and off as fast as a small switch. To minimize this effect the size and hence the capacitance of the switches is limited [12], [15].The timing spread Δt_S of a switch depends directly to input capacitance C_{in} as below

$$\Delta t_S = V_{off} \cdot \frac{C_{in}}{I_{LSB}} \tag{4.14}$$

where V_{off} is the offset voltage in the differential pair and I_{LSB} is the drive current.

The combination of equations (4.13) and (4.14) as follows can offer the expected compromises that need to be reached for the size of the switches,

$$\sigma_{\Delta t_S} = A_{VT} C_{OX} \cdot \frac{\sqrt{WL}}{I_{LSB}} \tag{4.15}$$

Finally, considering equation (4.15) it is quiet obvious that although the increase in the size of the switches improves offset matching, it will cause timing mismatch due to larger gate capacitances.

4.3.2 Current cell's output resistance evaluation

It is clear that by addition of the switches, the output resistance of the current cell is increased by a factor $g_m r_o$, where g_m and r_o are the transconductance and the output resistance of the switch turned on, respectively. Actually, the switch turned on behaves like a cascode transistor. For the current cell implemented with the proposed current source the output resistance can be given by

$$R_o \cong g_{mSW}\, r_{oSW}\, R_{oCS} \tag{4.16}$$

where R_{oCS} is the output resistance of the proposed current source given by (4.10).

The output resistance of the steered current cell implemented with the proposed current cell is shown in Figure 4.9. It must be noted that the switches are sized with minimum lengths allowed by the technology $L=0.35\mu m$ and widths $W=0.7\mu m$.

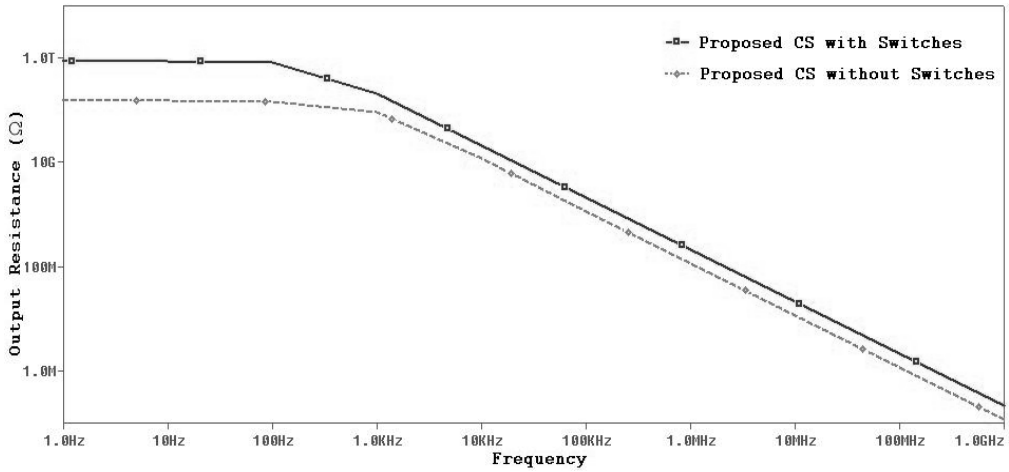

Figure 4.9 : Output resistance of the current cell implemented with the proposed current source.

As it can be seen from Figure 4.9, the cascode effect of the switch turned on is obvious in the output resistance value. The output resistance at low frequencies increases according to (4.16) and equals 882GΩ.

It can be concluded that at low frequencies the output resistance can be designed to be high enough. The reduction of the output impedance at high frequencies introduces distortion. The problems start if the nonlinear current that charges and discharges the parasitic capacitances starts to grow relatively big compared to load current [39]. Since at high frequencies the capacitive part of the output impedance is more effective, only this part will be considered. For the switch turned off only the gate-drain capacitance and the drain voltage dependent drain-bulk capacitance of the MOS switch are effective and the output capacitance is given as [16]

$$C_{off} = C_{gd} + C_{db}(V_D) \tag{4.17}$$

For the switch turned on except the parasitic capacitances given in (4.17) the additional capacitance C_{CM} at common mode will be effective. The overall capacitance in this case is given by

$$C_{on} = C_{gd} + C_{db}(V_D) + C_{CM} \tag{4.18}$$

The capacitance at common mode is determined by the capacitance of the switches, capacitance of the source transistor and their interconnections. Due to the large area of the current source transistor the drain and interconnect capacitances are very large. To reduce these capacitances cascoding, gain boosting techniques are used. Since the size of the current source transistor is fixed following the matching considerations, a small-sized cascode transistor is usually selected to reduce common mode capacitance [15].

The total output impedance of the DAC is strongly affected by the current to be generated. Data dependent output impedance modulation is certainly undesired. To minimize this effect in some applications the switch outputs are buffered with cascode transistors [15].

4.4 Binary-to-Thermometer Decoder

The most important part of the digital circuitry used in the thermometer coded, segmented and hybrid current-steering DACs is binary-to-thermometer decoder. Thermometer decoder can be implemented using different design approaches. Three of them are mostly used [32],

a) *the row and column decoder***.** The combination of the control signals of these 2 decoders determines if the current source is switched to the output or not. Although simple implementation with low power consumption this decoder lacks the flexibility to realize optimal switching schemes.

b) *the VHDL decoder***.** For high resolution DACs, the row and column decoder can be integrated in one block using a VHDL implementation. Although the update rate of the circuit is determined by the performance of the available standard cell library, the major advantage is the high level of automation that can be obtained using this approach.

c) *the custom-made decoder*. For high speed DACs, a custom-made decoder is used. This decoder allows an optimal exploitation of the symmetry by a detailed analysis of the required logic expressions. This results in a number of custom-made standard cells that can be optimized towards a high update rate. This approach gives the designer the opportunity to check the timing constraints on every point within the decoder leading to an improved dynamic behavior of the DAC.

The custom-made decoder approach is adopted in this thesis. The design steps are explicated through the design of a 3-bit binary-to-thermometer decoder to be used in the implementation of a hybrid current-steering DAC. Gate and transistor level design of decoder are given in detail.

4.4.1 Gate level decoder design

The starting point for the gate level design is the extraction of the conversion codes required for 3-bit binary-to-thermometer decoder. Later, all the conversion logic

expressions are realized using logic gates. Table 4.3 gives the 3-bit binary-to-thermometer converted codes together with the conversion expression for each code. *A*, *B*, and *C* denote the binary inputs where *A* is the most significant bit and *C* is the least significant bit. T_i *(i=1....7)* are the converted thermometer outputs.

Table 4.3 : 3-bit binary-to-thermometer conversion codes.

Binary			**Thermometer**						
A	**B**	**C**	**T_7=ABC**	**T_6=AB**	**T_5=A(B+C)**	**T_4=A**	**T_3=A+BC**	**T_2=A+B**	**T_1=A+B+C**
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Figure 4.10 shows the block schematic of the 3-bit binary-to-thermometer decoder.

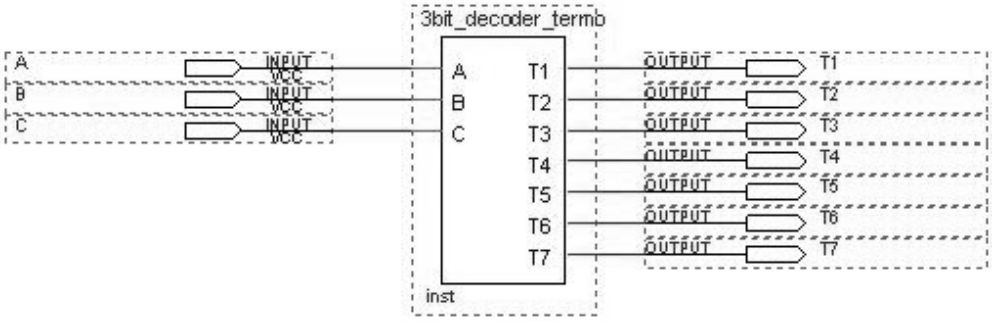

Figure 4.10: Block schematic of the 3-bit binary-to-thermometer decoder.

Binary-to-thermometer conversion codes shown in Table 4.3 are realised using NAND, NOR and NOT gates. These gates are selected for their high-speed operation and simple transistor level implementation compared to other logic gates. The gate level decoder circuit is shown in Figure 4.11.

The designed gate level decoder's operation and speed is simulated using Altera DE2 FPGA. The timing response of the decoder is given in Figure 4.12. It must be noted

that operation speed of the decoder is determined by the components (gates) available in the Altera's libraries.

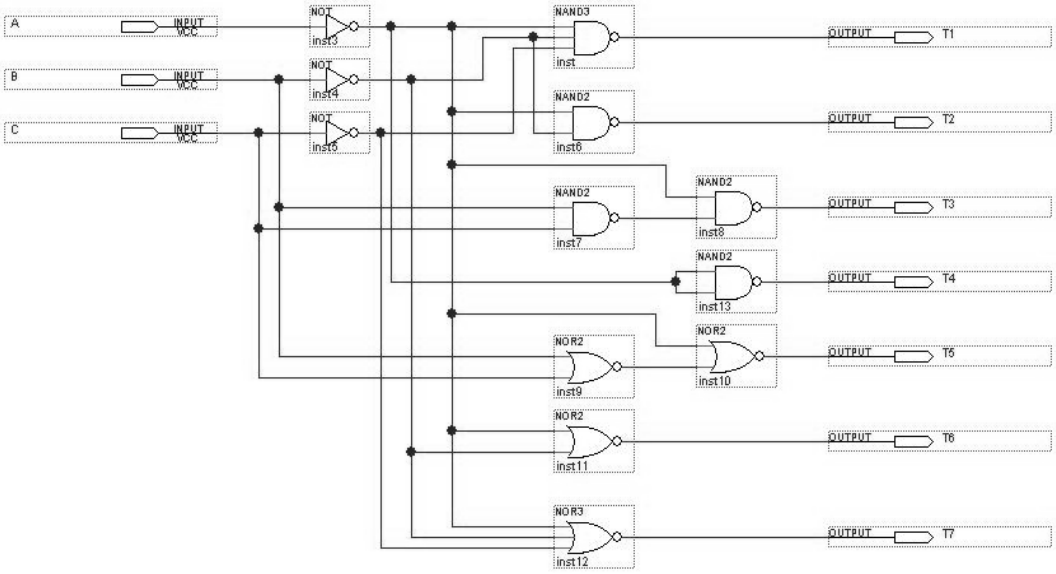

Figure 4.11: Implementation of the decoder with logical gates.

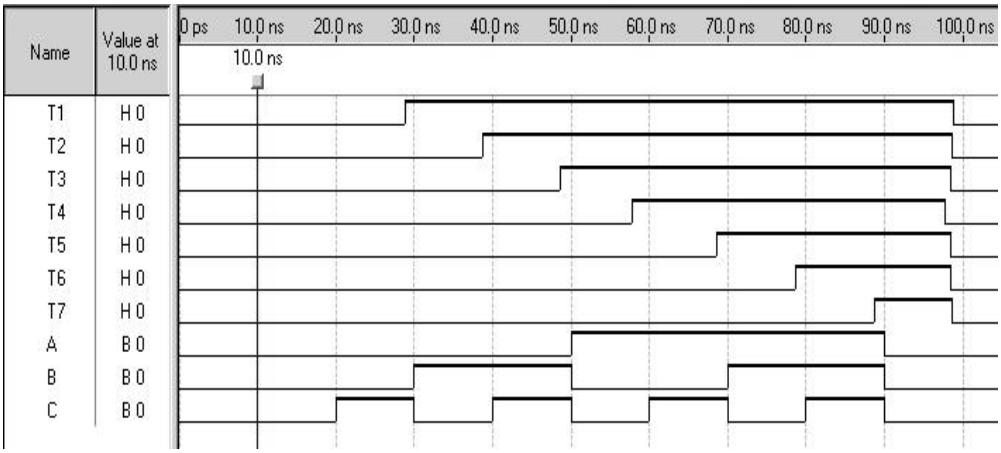

Figure 4.12: Timing response of the 3-bit binary-to-thermometer decoder.

4.4.2 Transistor level design

Binary-to-thermometer decoder is the most important part of the digital circuitry in a current-steering based DAC. Since this circuit is in the input signal's path a high-speed operation is expected. Transistor level design of the decoder is obtained by the implementation of the logic gates functionally tested in the gate level design and by achievement of the timing requirements through the proper gate sizing. However, it must be noted that during the design phase a tradeoff between timing, power and area

is expected. Transistor level implementation is carried out through the design of the complex CMOS logic circuits based on a CMOS reference inverter i.e. all gates consist of pull-up and pull-down networks sized to achieve the same delay as the inverter [47].

3-bit binary-to-thermometer decoder's transistor level circuit based on the gate level design of Figure 4.11 is shown in Figure 4.13.

Each highlighted section represents the circuit performing the respective binary-to-thermometer code conversion, for example by the mean of a 3-input NAND gate T_1 thermometer code is achieved from A, B and C binary codes.

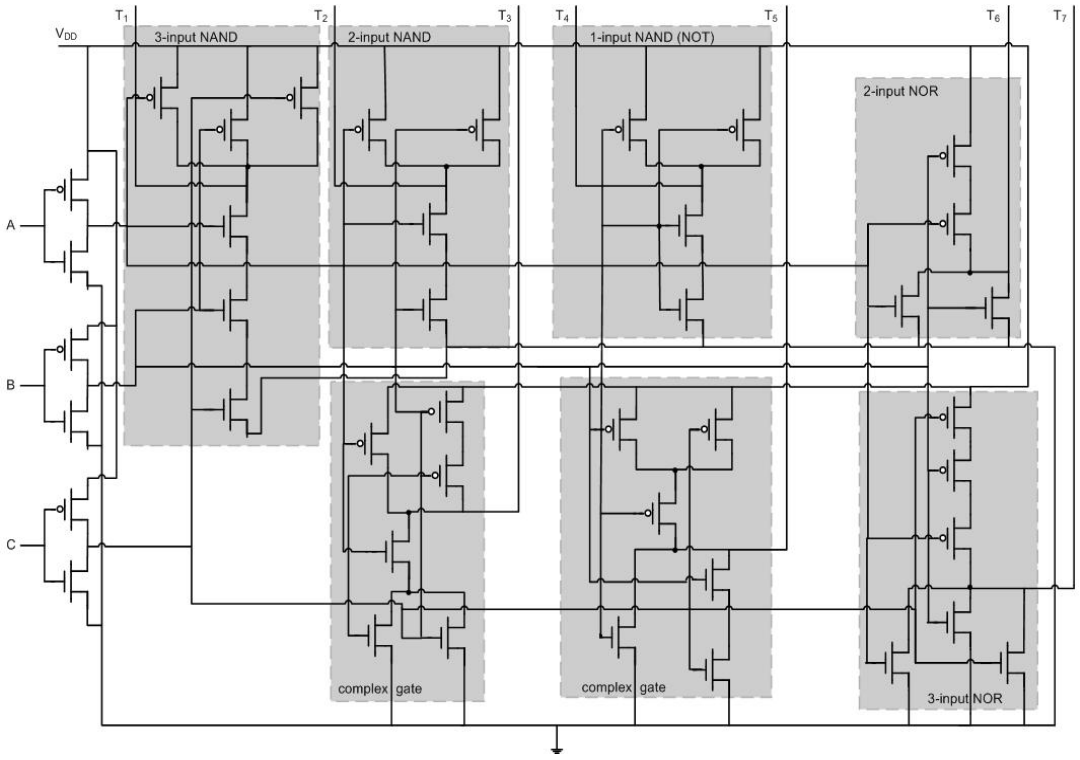

Figure 4.13: Transistor level circuit of the 3-bit binary-to-thermometer decoder.

4.4.3 Sizing gates

Generally, timing requirement determine the device sizes in CMOS logic gates. As mentioned before the sizing of all CMOS logic gates here is based on the sizing of a reference inverter i.e. sizing the transistors for a given gate is based on obtaining the same delay as the reference inverter under worst case operation assuming the same load capacitance is driven. To make the delay calculation simple, the reference inverter is modeled with an effective on-resistance R_{eff}, driving a load capacitance C_L

[48]. From this timing model for the inverter the average propagation delay τ_p, where the 50% point occurs, is given by

$$\tau_p = 0.7 R_{eff} C_L \tag{4.19}$$

where the values of R_{eff} represent the average on-resistances R_N in the pull-down and R_P in the pull-up states. Actual pull-down and pull-up on-resistances depend on the aspect ratios W/L of the devices and equivalent on-resistances of the unit-sized devices. Equivalent on-resistances are related to the technology and are extracted by performing SPICE simulations on unit-sized devices [31], [48]. For calculation purposes the equivalent on-resistances of 0.35µm technology are selected approximately $R_{eqn}=12.5k\Omega$ for unit-sized NMOS and $R_{eqp}=30k\Omega$ unit sized PMOS devices, respectively. Thus, actual on-resistances can be given by

$$R_N = R_{eqn} \times \left(\frac{L}{W}\right)_N \tag{4.20}$$

$$R_P = R_{eqp} \times \left(\frac{L}{W}\right)_P \tag{4.21}$$

It is convenient to design the transistors of the inverter with the minimum length dimension and to deal only with the width. Similarly, the sizing of the other CMOS logic gates is performed. Considering combinations of the connected transistors in the pull-down and the pull-up networks equivalent devices with the same delay characteristics as the reference inverter are derived. For N devices connected in parallel the equivalent aspects ratios are given by

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + ... + \left(\frac{W}{L}\right)_N \tag{4.22}$$

For N devices connected in series the equivalent aspects ratios are given by

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_2 ..... \left(\frac{W}{L}\right)_N}{\left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_3 .. \left(\frac{W}{L}\right)_N + \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3 .. \left(\frac{W}{L}\right)_N + .. + \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_2 .. \left(\frac{W}{L}\right)_{N-1}} \tag{4.23}$$

From (4.19) it can be seen that delay depends on the load capacitance and for a proper sizing of the gates, a good estimation of the effective load capacitance is required. The load capacitance to be considered for the delay calculation in an inverter is given by

$$C_L = C_{self} + C_{fanout} + C_{wire} \quad \textbf{(4.24)}$$

where C_{self} is the sum of the capacitances (gate-to-drain overlap capacitances and bulk-to-drain junction capacitances of NMOS and PMOS transistors) connected to the output, C_{fanout} is the capacitance due to the inputs of subsequent gates (the sum of the input capacitances of the fanouts), and C_{wire} is interconnect capacitance that for short wires (less than a few microns) is negligible [48].

In general, the above gate sizing is sufficient for the design of the 3-bit binary-to-thermometer decoder. However, there exist different approaches such as optimizing gate sizes to minimize delay of a logic path or optimizing paths with logical effort LE, topics that are addressed in detail in [48].

4.5 Synchronization Circuitry

Due to many factors like mismatch in components, differences between logic paths etc., distortion and glitches can be observed at the outputs of a decoder. So that, decoder's output signals are not suitable to drive properly the switched current cells. Furthermore, imperfect synchronization of the control signals at the switches and the current variation due to a drain voltage variation of the current sources, significantly degrades the dynamic performance of the system [7-8]. Consequently, identical and thoroughly well synchronized signals are required to drive the switches. Different circuits are adopted to achieve the required synchronization of the control signals by using static latches before the switching transistors [22] or high-speed latches aimed to reduce the glitch energy [49]. In some papers latch and deglitcher circuit are incorporated in one circuit designed to drive the switches so that the switch transistors are all synchronized during the turn on/off tasks [50-51].

Latches and drivers placed between decoder and switched current cells are implemented in a 3-bit current-steering DAC as shown in Figure 4.14.

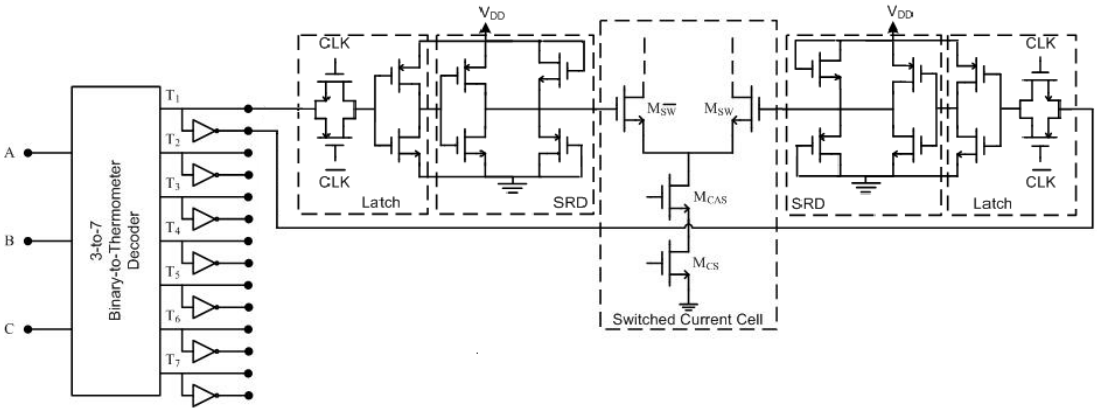

Figure 4.14 : Latch circuit and swing reduced driver in a DAC.

4.5.1 Dynamic latch

The latch used in Figure 4.14 is a dynamic D-latch. The function of the D-latch is to synchronize the external clock. Implementation of the D-latch includes a transmission gate and an inverter. Therefore, circuit requires fewer transistors compared with configurations in [7-8], [22], [49-51]. The block diagram of the dynamic D-latch is shown in Figure 4.15

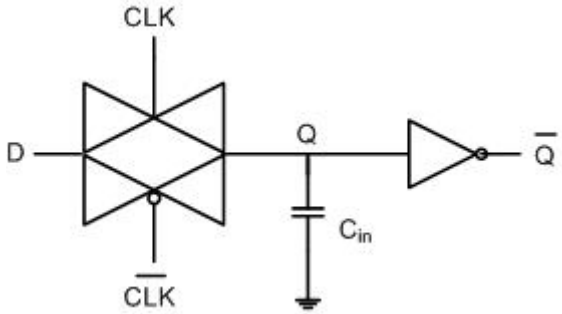

Figure 4.15: Dynamic D-latch.

As in all dynamic latches, the data is stored on gate capacitance of the inverter and the charge is switched in or out with the transmission gate. The complementary transmission gate ensures that storage gate is always strongly driven. The operation of the latch is very simple: when *CLK=0* transmission gate is off and the output is determined by storage node, when *CLK=1* transmission gate is on and inverter output follows *D* input. Thus, latch is transparent when transmission gate is closed.

The delay of the circuit is calculated using the RC model for this circuit [48]. Large signal resistance for CMOS transmission gate can be approximated as below

$$R_{TG} = R_N \| R_P \cong R_{eqn}\left(\frac{L}{W}\right) \quad \textbf{(4.25)}$$

where R_N and R_P are the on-resistances of the NMOS and PMOS devices of the transmission gate, respectively. R_{eqn} is the equivalent on-resistance of the unit-sized NMOS transistor.

The storage capacitance comes primarily from the gate capacitance of the inverter but the output capacitance of the transmission gate, depending on the on or off state of the gate, is also effective. For this reason, the capacitance is denoted as C_{in} in the Figure 4.15. The approximate value of capacitance C_{in} can be calculated using the equation (4.24).

Therefore, for the dynamic D-latch of Figure 4.15 the propagation delay, where the 50% point occurs, is given by

$$\tau_p = 0.7 R_{TG} C_{in} \quad \textbf{(4.26)}$$

Minimum frequency of operation is typically of the order of 1-100kHz so as not to lose data due to reverse-bias leakage current. The most important advantage is that it can be clocked at high frequency since very little delay exists in latch elements.

Although the dynamic storage at node Q may cause problems when operating at low frequencies (data loss occurs), the dynamic D-latch is attractive for its simplicity and high frequency operation. Alternatively, to remove the dynamic storage problem i.e. to obtain low frequency operation without data loss, static latches are used. Static or non-dynamic latches use feedback to restore value. Thus, they are more complex causing the digital circuitry to occupy more area.

4.5.2 Swing reduced driver (SRD)

The use of the MOS transistor as switch causes the coupling of the switching control signal applied on the gate, to the output through effective gate-drain capacitance C_{GD} [52]. The existence of the parasitic gate-drain feedthrough capacitance results in the dynamic performance degradation of the current-steering DAC [7]. It is shown that

the placement of a driver circuit with a reduced swing at the input of the switches reduces the clock feedthrough to the output node [7], [20], [22], [52-53].

The swing reduced driver aims to reduce the swing of the switching control signals applied to the inputs of the switches. Figure 4.16 shows a block diagram of an SRD system. The input swings from V_{IL} (input's low level) to V_{IH} (input's high level) and the SRD drives the input to predefined levels i.e. the output swings from V_{OL} (output's low level) to V_{OH} (output's high level).

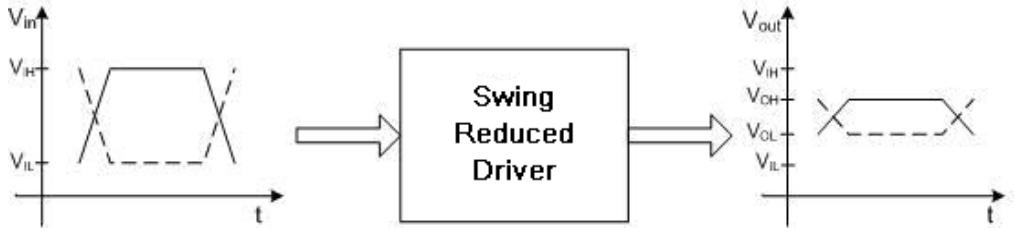

Figure 4.16: SRD block diagram.

Generally, the signals coming from the preceding blocks are digital with a voltage swing varying from ground to the supply voltage level. Hereby, when these signals are applied directly to the switches the switching speed is limited and the power consumption is increased. To address such problems drivers that enable faster switching speed and low power consumption are required.

To illustrate the operation of the SRD block two circuits are investigated. Depending on the output signals obtained, the circuits are denoted as noninverting and inverting SRDs.

4.5.2.1 Noninverting SRD

Noninverting SRD used in [54] is shown in Figure 4.17. The circuit consists of two pMOS transistors M_1 and M_2. Input signal is applied to the gate of M_1 while the gate of M_2 is always grounded. When, the input is at its high level i.e. V_{DD}, M_1 transistor is off. The output's level is the same with input's high level i.e. V_{DD}. When, the input is at its low level V_{IL} i.e. 0, M_1 operates in saturation while M_2 in triode region. The output's level V_{OL} is determined by

$$V_{OL} = V_{SD1} = V_{DD} - V_{SD2} = V_{DD} - R_{ON2} \times I_{D2} \quad \textbf{(4.27)}$$

where R_{ON2} and I_{D2} are the on resistance and the drain current of M_2 pMOS transistor. I_{D2} and R_{ON2}, can be calculated from the equivalent circuit shown in Figure 4.18.

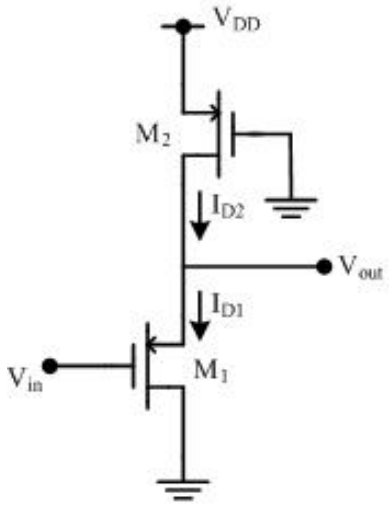

Figure 4.17: Noninverting SRD circuit.

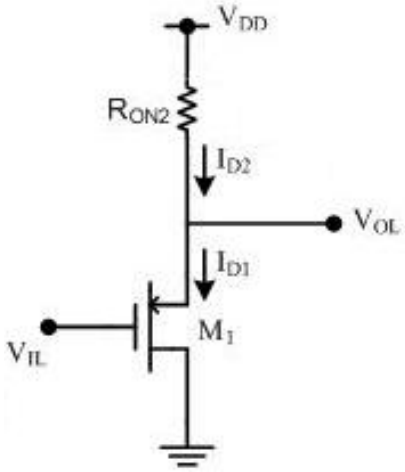

Figure 4.18: Equivalent circuit of noninverting SRD.

$$I_D = \frac{K_p}{2}\left(\frac{W}{L}\right)_1 \left(V_{OL} - V_{IL} - V_{Tp}\right)^2 = K_P \left(\frac{W}{L}\right)_2 \left[\left(V_{DD} - V_{Tp}\right) - \frac{\left(V_{DD} - V_{OL}\right)^2}{2}\right]\left(V_{DD} - V_{OL}\right) \quad \textbf{(4.28)}$$

$$R_{ON2} = \frac{1}{K_p\left(\frac{W}{L}\right)_2 \left(V_{DD} - V_{Tp}\right)} \quad \textbf{(4.29)}$$

where K_p and V_{Tp} are the process transconductance parameter and threshold voltage of pMOS transistor, respectively. *(W/L)* are the aspect ratios of the pMOS transistors.

For a given V_{IL} and an expected V_{OL} the aspect ratios of the transistors are derived from equation (4.28) and are expressed as

$$\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} = \frac{2\left(V_{DD}-V_{Tp}\right)\left(V_{DD}-V_{OL}\right)-\left(V_{DD}-V_{OL}\right)^2}{\left(V_{OL}-V_{IL}-V_{Tp}\right)^2} \qquad \textbf{(4.30)}$$

The transistor dimensions of the circuit in Figure 4.17 are calculated for a given input low level $V_{IL}=0V$ and a yielded output low level $V_{OL}=2.7V$ with minimum lengths as shown in Table 4.4.

Table 4.4 : Transistors' dimensions of noninverting SRD.

Tr.	W(µm)	L(µm)
M_1	1.75	0.35
M_2	2.8	0.35

Using the transistors' dimensions given in Table 4.4 and the AMS 0.35µm CMOS technology process parameters, the noninverting SRD circuit is simulated with SPICE. The simulation results are shown in Figure 4.19.

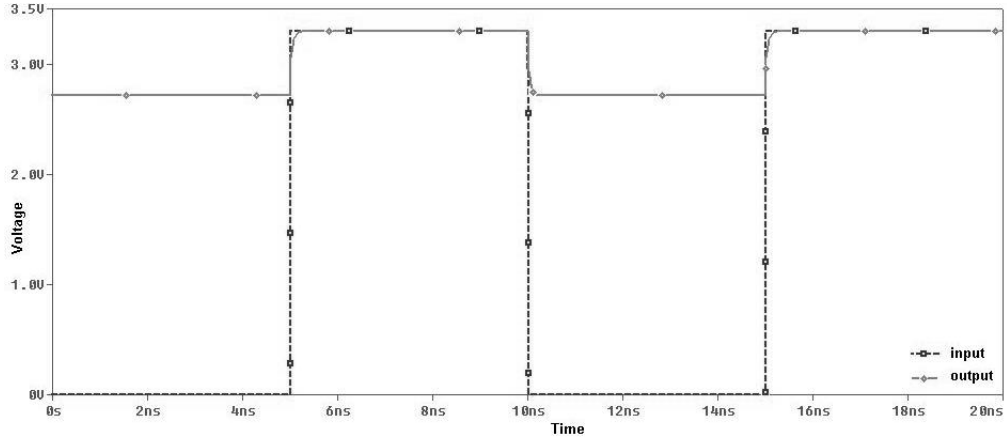

Figure 4.19 : Input and output voltages of noninverting SRD.

In this case, the power dissipation of the circuit is 0.733mW for a drawn current of 0.22mA.

The noninverting SRD has advantages like simplicity in design, low power dissipation, but unfortunately, only the lower level of the switching control signal can be controlled while the higher level is fixed to supply voltage. Thus, it cannot be implemented to the circuits requiring the change of both high and low levels of the switching control signals.

4.5.2.2 Inverting SRD

Inverting SRD circuit proposed in [55] is shown in Figure 4.20. The circuit is very simple and consists of an input applied to the M_1-M_2 inverter pair and an inverted swing reduced output maintained in the desired range by the M_3 nMOS and M_4 pMOS diode-connected transistors.

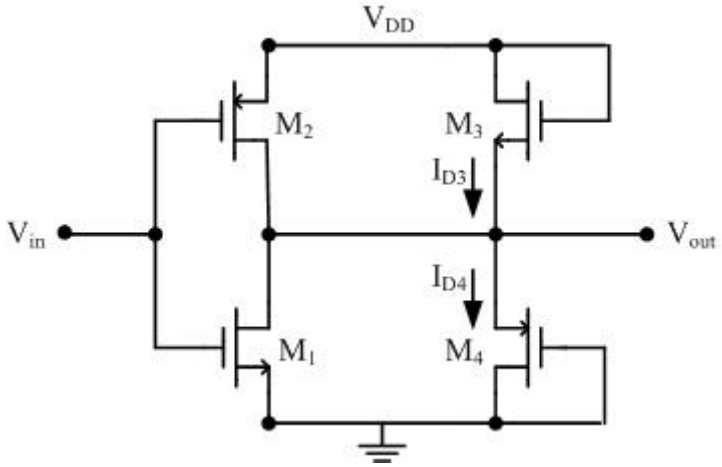

Figure 4.20: Inverting SRD circuit.

The operation of the circuit can be explained as follows: when, the input is at high level V_{IH}, i.e. V_{DD}, M_1 transistor switches on, while M_2 remains off and most of the current flows from supply rail through M_3 and M_1 transistors to ground pulling the output to low level V_{OL}. When, the input is at low level V_{IL}, i.e. *0*, M_2 transistor switches on, while M_1 remains off and most of the current flows from supply rail through M_2 and M_4 transistors to ground pulling the output to high level V_{OH}. The equivalent circuit for the applied high input voltage level V_{IH} is shown in Figure 4.21. M_1 operates in triode region and M_2 is off. The output voltage level for $V_{OL} \geq |V_{Tp}|$ is given by

$$V_{OL} = R_{ON1} \times I_{D1} = R_{ON1} \times \left(I_{D3} - I_{D4}\right) \quad \textbf{(4.31)}$$

where R_{ON1} and I_{D1} are the on resistance and the drain current of M_1 nMOS transistor. I_{D3} and I_{D4} are the currents flowing through M_3 and M_4, respectively. R_{ON1}, I_{D3} and I_{D4} can be calculated from Figure 4.21.

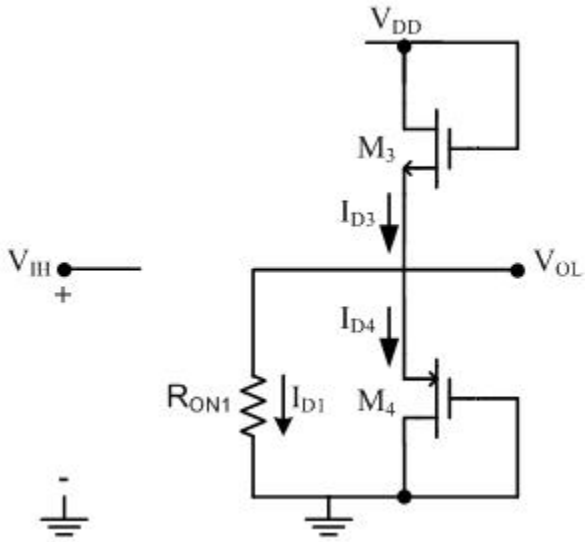

Figure 4.21: Equivalent circuit of inverting SRD for high input level.

$$R_{ON1} = \frac{1}{K_n\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{Tn})} = \frac{1}{K_n\left(\frac{W}{L}\right)_1 (V_{IH} - V_{Tn})} \quad \textbf{(4.32)}$$

$$I_{D3} = \frac{1}{2} K_n \left(\frac{W}{L}\right)_3 (V_{DD} - V_{OL} - V_{Tn})^2 \quad \textbf{(4.33)}$$

$$I_{D4} = \frac{1}{2} K_p \left(\frac{W}{L}\right)_4 (V_{OL} - |V_{Tp}|)^2 \quad \textbf{(4.34)}$$

where K_n, K_p and V_{Tn}, V_{Tp} are the process transconductance parameters and threshold voltages of nMOS and pMOS transistors, respectively. (W/L) are the aspect ratios of the MOS transistors.

For $V_{OL}<|V_{Tp}|$ the above equations are still valid except that $I_{D4}=0$. In this case pMOS M_4 is cut off.

The equivalent circuit for the applied low input voltage level V_{IL} is shown in Figure 4.22. M_1 is off and M_2 operates in the triode region. The output voltage level for $V_{OH} \leq V_{DD}-V_{Tn}$ is given by

$$V_{OH} = V_{DD} - R_{ON2} \times I_{D2} = V_{DD} - R_{ON2} \times (I_{D4} - I_{D3}) \quad \textbf{(4.35)}$$

where R_{ON2} and I_{D2} are the on resistance and the drain current of M_2 pMOS transistor. R_{ON2}, I_{D3} an I_{D4} can be calculated from Figure 4.22.

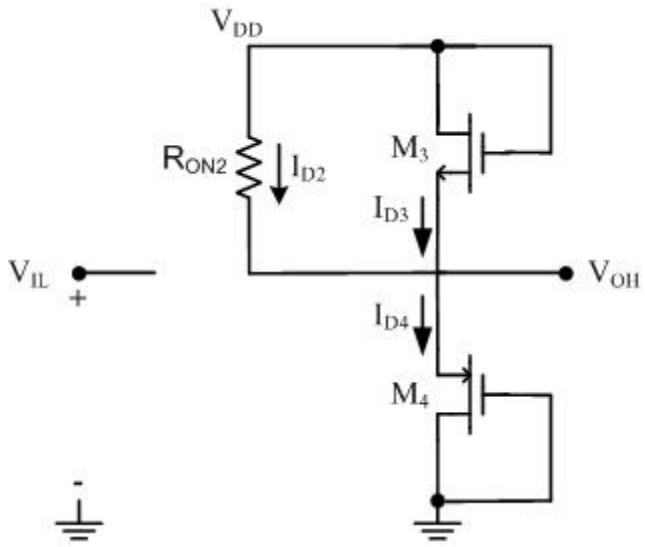

Figure 4.22: Equivalent circuit of inverting SRD for low input level.

$$R_{ON2} = \frac{1}{K_P \left(\frac{W}{L}\right)_2 \left(V_{DD} - V_{IL} - |V_{Tp}|\right)} \quad \textbf{(4.36)}$$

$$I_{D3} = \frac{1}{2} K_n \left(\frac{W}{L}\right)_3 (V_{DD} - V_{OH} - V_{Tn})^2 \quad \textbf{(4.37)}$$

$$I_{D4} = \frac{1}{2} K_p \left(\frac{W}{L}\right)_4 (V_{OH} - |V_{Tp}|)^2 \quad \textbf{(4.38)}$$

For $V_{OH} > V_{DD} - V_{Tn}$ the above equations are still valid except that $I_{D3}=0$. In this case nMOS M_3 is cut off.

Using the equations (4.31) to (4.38) for a given desired voltage swing range i.e. V_{OL} and V_{OH} values, the dimensions of M_3 and M_4 transistors can be found by solving the following system of equations

$$\left(\frac{W}{L}\right)_3 = \frac{\frac{K_p}{K_n}\left(V_{OL} - |V_{Tp}|\right)^2\left(\frac{W}{L}\right)_4}{\left(V_{DD} - V_{OL} - V_{Tn}\right)^2} + \frac{2V_{OL}\left(V_{IH} - V_{Tn}\right)\left(\frac{W}{L}\right)_1}{\left(V_{DD} - V_{OL} - V_{Tn}\right)^2} \quad \textbf{(4.39)}$$

$$\left(\frac{W}{L}\right)_4 = \frac{\frac{K_n}{K_p}\left(V_{DD} - V_{OH} - V_{Tn}\right)^2\left(\frac{W}{L}\right)_3}{\left(V_{OH} - |V_{Tp}|\right)^2} + \frac{2\left(V_{DD} - V_{OH}\right)\left(V_{DD} - V_{IL} - |V_{Tp}|\right)\left(\frac{W}{L}\right)_2}{\left(V_{OH} - |V_{Tp}|\right)^2} \quad \textbf{(4.40)}$$

It is clear that prior to the determination of the M_3 and M_4 transistors' dimensions, the M_1-M_2 inverter is designed considering the performance parameters like propagation delay, current flow and power dissipation.

Using the equations (4.39) and (4.40) for a swing reduction from 3.3V to 400mV, the dimensions of M_1 to M_4 transistors are calculated and summarized in Table 4.5. The desired voltage levels are fixed to $V_{OL}=1.6V$ and $V_{OH}=2V$.

Table 4.5 : Transistors' dimensions of inverting SRD.

Tr.	W(µm)	L(µm)
M_1	0.7	0.35
M_2	2.8	0.35
M_3	5.6	0.35
M_4	9.45	0.35

Figure 4.23 shows the SPICE simulated input-output voltage waveforms of the inverting SRD.

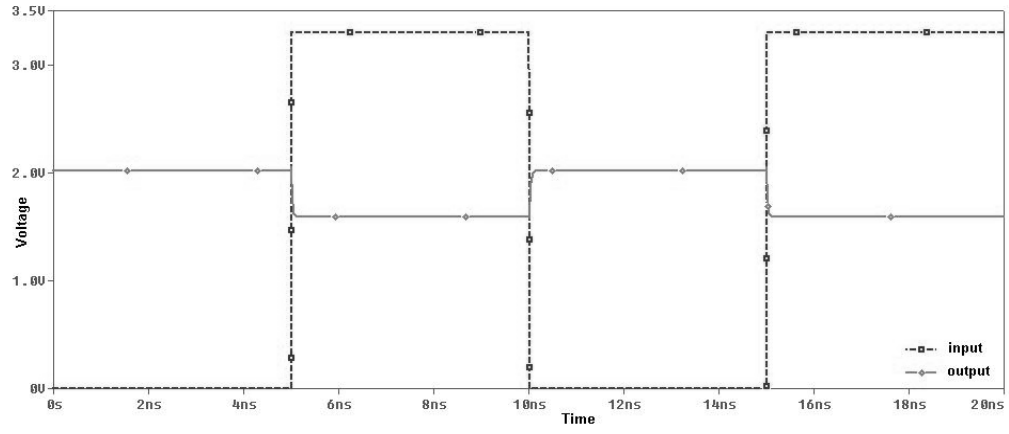

Figure 4.23 : Input and output voltages of inverting SRD.

The power dissipation of the circuit is 1.76mW, mainly caused by the current drawn by the diode-connected transistors.

Despite the static power dissipation, the inverting SRD is useful in some applications where the desired voltage swing range need to be maintained with higher flexibility. By the proper design of the inverting SRD circuit, this can be done easily without compromising the area requirement of the system. Decreased voltage swing reduces the digital signal feedthrough to the output nodes and the large current spikes on the outputs of the switched current cells when used in current-steering DACs.

5. BEHAVIORAL MODEL FOR CURRENT-STEERING DACS

5.1 Introduction

Before proceeding with the transistor level design of the converter it is important to have some knowledge about the behavior of the system and the problems that may occur during the operation of the converter. For this reason, the use of DAC models eases the design and helps on understanding the behavior of each part of the system. Thus, through a good model it is easier to improve the performance of the DAC in terms of speed, accuracy and other parameters according to the required application's specifications.

5.2 SPICE Model

There are numerous ways to implement an ideal DAC in SPICE [6]. The model presented here is based on the operation of the voltage controlled current source (VCCS). In analogy with Figure 4.8, the current cell modeled using the VCCS approach is shown in Figure 5.1.

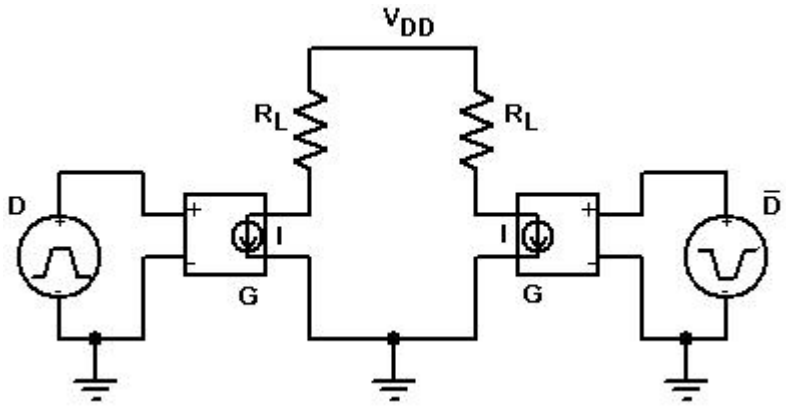

Figure 5.1 : SPICE model of the current cell.

The current of the source is that of the VCCS and is given by

$$I = G \times [V(+) - V(-)] \quad \textbf{(5.1)}$$

where G is transconductance, $V(+)$ and $V(-)$ are the positive and negative controlling nodes.

The applied pulses are the controlling voltages of the VCCSs and represent the digital inputs. When the input is high a current G times the controlling voltage will flow through the current source, otherwise no current flows. Observe that the two VCCSs in Figure 5.1. operate in a complementary way and are controlled with complementary pulse signals. It must be noted the dependent sources may be linear and nonlinear. This is important when nonidealities are added in the model and properties like mismatching are analyzed.

The accuracy of the model is investigated through two implemented models; one 3-bit binary weighted DAC and one 3-bit thermometer coded DAC.

5.2.1 SPICE model for 3-bit binary weighted DAC

The SPICE model for the 3-bit binary weighted DAC is shown in Figure 5.2.

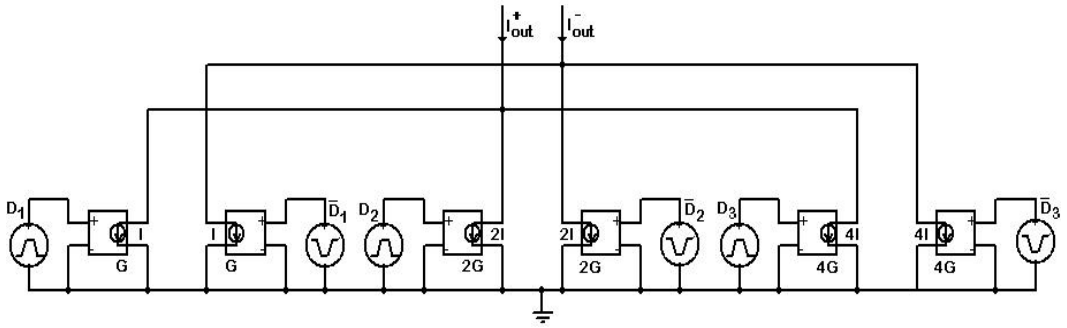

Figure 5.2: SPICE model for 3-bit binary weighted DAC.

Binary weighted property of the converter is obtained by selecting the control voltage amplitude 1V and the transconductances of the VCCSs *G*, *2G* and *4G*, respectively. Thus, for 5µS, 10µS and 20µS transconductances from equation (5.1) 5µA, 10µA and 20µA weighted currents are achieved.

Some nonidealities that affect the performance of the DAC are added to the model. Mismatching between current sources is modeled by randomly changing the value of transconductance G (a percentage of error is added or extracted from the ideal value).

Since, it is known that the dynamic performance of the binary weighted converter is degraded by glitches, by changing the pulse width parameter of the applied pulse sources (equivalent to the asynchronized digital inputs), glitches can be modeled. Simulated 3-bit binary weighted DAC output is shown in Figure 5.3.

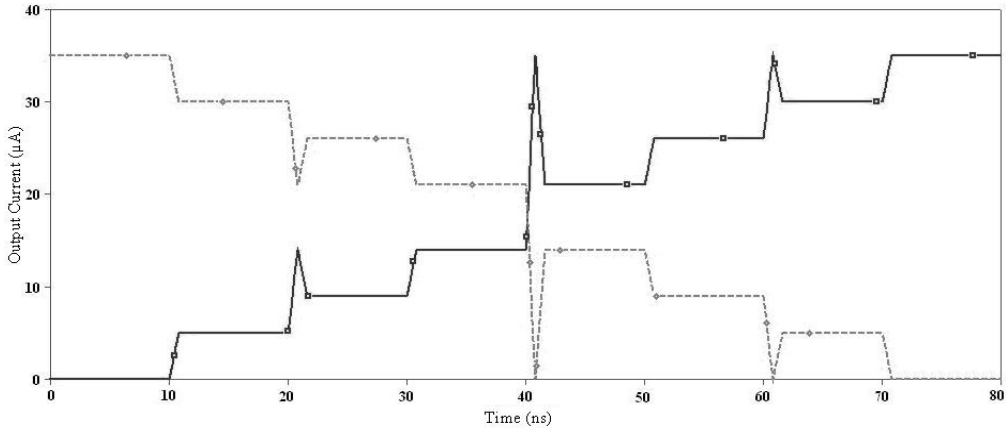

Figure 5.3: 3-bit binary weighted DAC output.

5.2.2 SPICE model for 3-bit thermometer coded DAC

The model is implemented using 7 current cells of Figure 5.1. The SPICE model for the 3-bit thermometer coded DAC is shown in Figure 5.4.

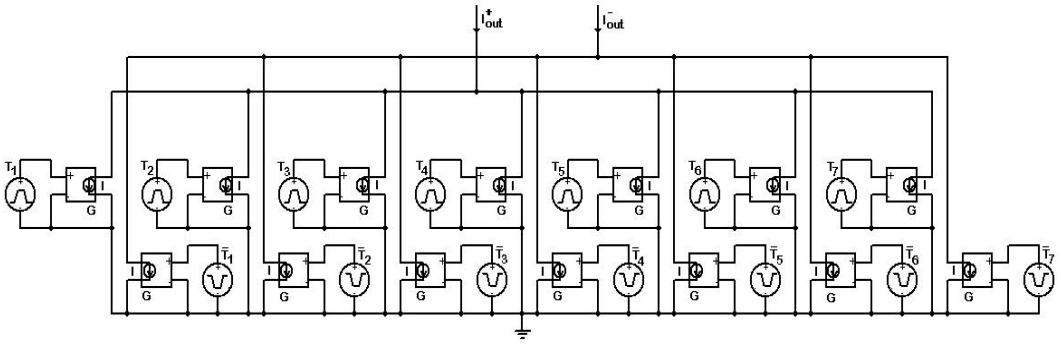

Figure 5.4: SPICE model for 3-bit thermometer coded DAC.

The applied controlling signals correspond to the thermometer coded inputs. Thermometer coded operation of the converter is obtained by selecting the control voltage amplitude 1V and all transconductances of the VCCSs *G*. Thus, for 5μS transconductance from equation (5.1) 5μA unary currents are achieved.

Simulated 3-bit thermometer coded DAC output is shown in Fig.5.5. Unlike the binary weighted DAC model, the change of the pulse widths or the delays of the

pulses do not cause any glitches and the output of the DAC is always free from glitches. Mismatching between current sources is modeled by randomly changing the value of transconductance G (a percentage of error is added or extracted from the ideal value).

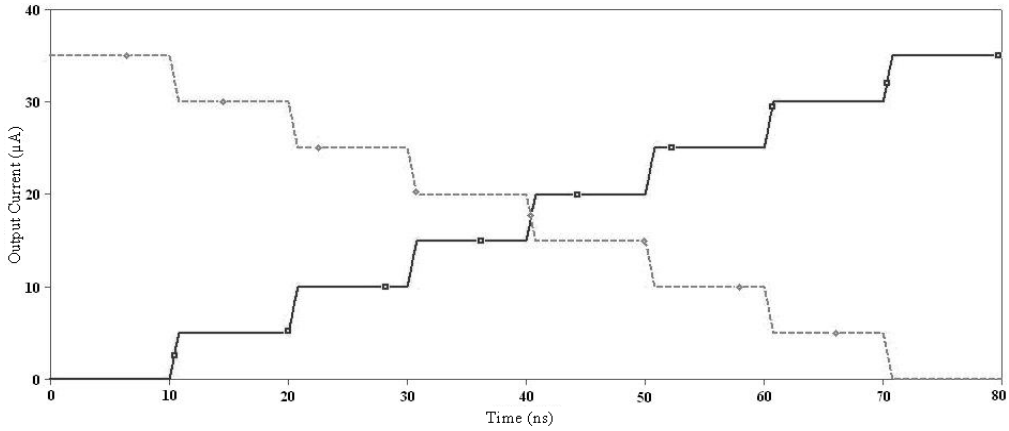

Figure 5.5: 3-bit thermometer coded DAC output.

5.3 SIMULINK® Model

MATLAB®/SIMULINK® models and the mapping of these models to structural VHDL-AMS descriptions have been generated [56]. Although in some developed models the behavioral model and partly the performance are studied [57], the complete behavioral system analysis including the worst case operation is not performed. The parameters like mismatching between current sources, latency and asynchronous operation of the digital components are not investigated through model simulations. The study of the behavioral model considering nonidealities and the evaluation of the static and dynamic performance of the system before the design are very important for an optimal design procedure of the DAC.

A universal behavioral model by using SIMULINK® adopted for current-steering DAC architectures is presented. Each block of the current-steering architecture is modeled in accordance with its function in the DAC system and considering the parameters related to its behavioral performance [58]. The models are validated in different current-steering DAC architectures.

5.3.1 Current source and switch array model

The block modeling the behavior of the current sources and switches is shown in Figure 5.6. The operation of the model is similar to that of the transistor level implementation shown in Figure 4.8. Basically, the switches will be 'on' when the high level of the SRD's output is available and will be 'off' when the low level of the SRD's output is available at the input of the switch. According to these on-off states the source current (binary weighted or unary) or a 0 will be available to the output of the switch.

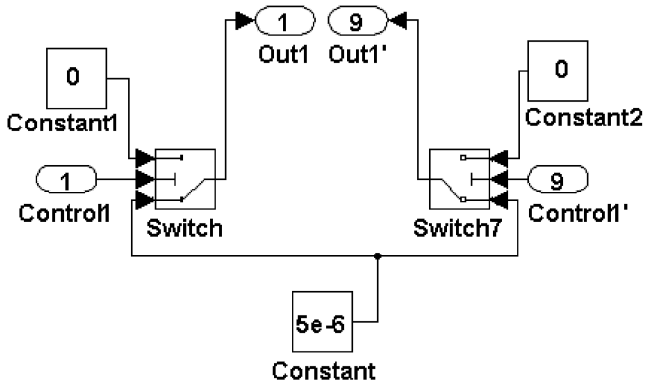

Figure 5.6: Current source and switch array model.

For simplicity the value of the current generated by the source is expressed with a constant, but for a more comprehensive study of the nonidealities of the current sources (mismatching, nonlinearities etc.) equations related with these nonidealities can be entered instead of the constant values.

5.3.2 Swing reduced driver model

As in the real implementation the swing reduced driver aims to reduce the swing of the voltage applied to the gates of the switch transistors. The model developed for this action is shown in Figure 5.7.

The model is based on a conditional block and according to the input's value the output is limited within the predefined values. So if the input's value is higher than 3V, the output is limited to 2.2V and if the input's value is lower than 3V, the output is limited to 1.8V. In this case the SRD is foreseen to achieve a reduction from 0 to 3.3V to 1.8 to 2.2V swing. It is clear that the limits can be changed according to the requirements of the given applications.

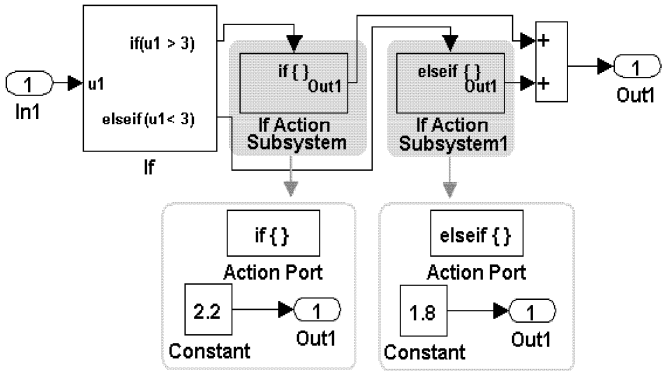

Figure 5.7: Swing reduced driver model.

5.3.3 Binary-to-thermometer decoder model

For DAC applications requiring code conversions as previously mentioned binary-to-thermometer decoders are needed. Since SIMULINK® library includes all the logic gates it is easy to implement a decoder by using SIMULINK®. Similarly to the gate level decoder design using available NOR and NAND gates according to the code conversion functions the binary-to-thermometer decoder model can be implemented. An example of a 4-to-15 decoder model is shown in Figure 5.8.

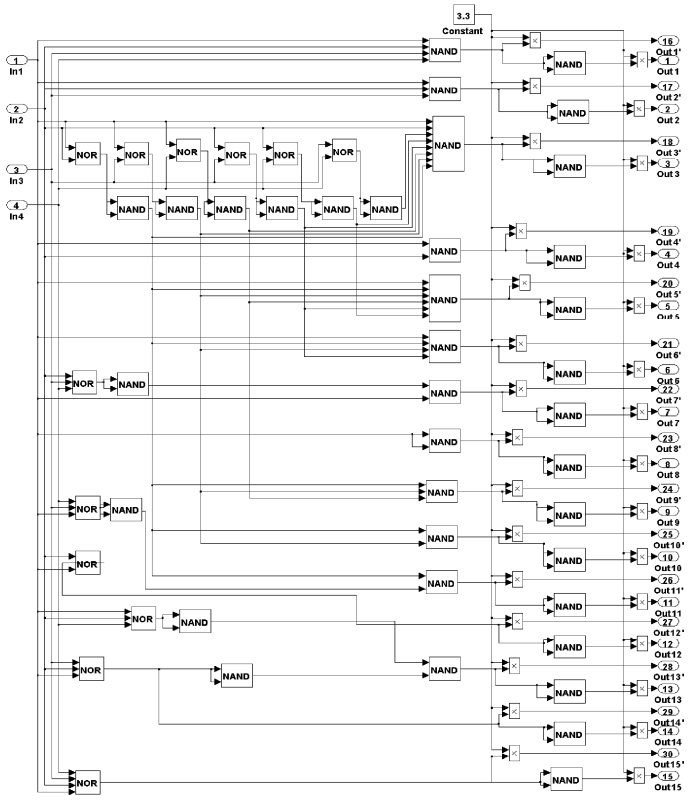

Figure 5.8: 4-to-15 binary-to-thermometer decoder model.

5.3.4 SIMULINK® DAC behavioral models

All current-steering architectures share the same building blocks. Thus, the models constituted for different blocks can be adapted to all implementations. It is convenient to model more complicated architectures since the basic simple architectures are included in them i.e. segmented architecture is modeled using the developed binary and unary subDAC models. The behavioral models of two 12-bit current-steering DACs (segmented and parallel) developed by using SIMULINK® are described. The performance characteristics of the models simulated for the worst case operation scenario of the systems is investigated.

5.3.4.1 12-bit segmented current-steering DAC model

The model for the 12-bit segmented current-steering DAC is based on the architecture given in Figure 3.3 and is shown by the block diagram in Figure. 5.9 [58].. The SIMULINK® model consists of a 12-bit digital data generator, an 8-bit binary weighted subDAC and 4-bit thermometer-coded subDAC subsystems. The system's outputs are obtained by summing up the outputs of both subDACs.

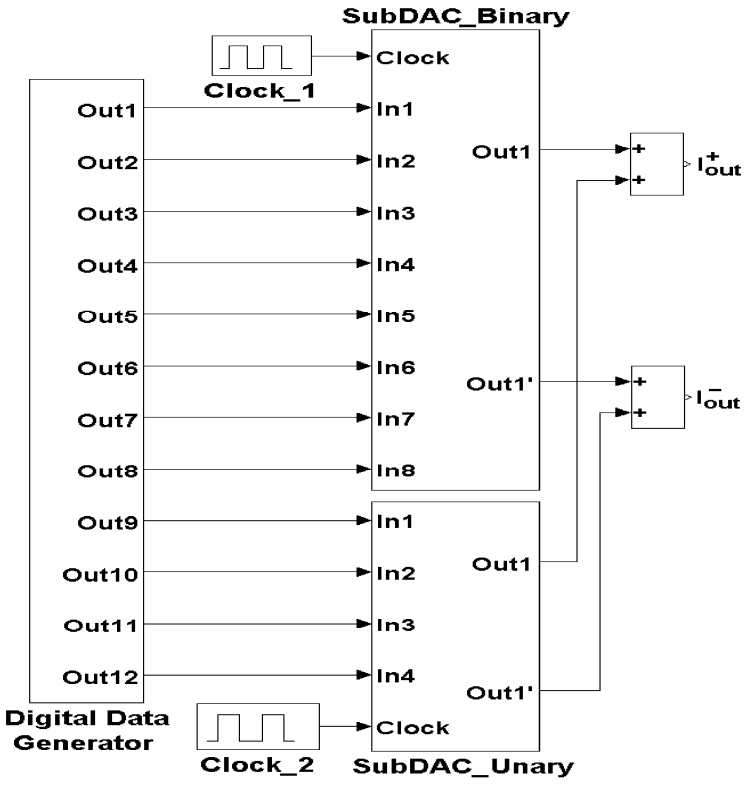

Figure 5.9: SIMULINK® model of the 12-bit segmented current-steering DAC.

The 12-bit input binary data is segmented into the 8 least significant bits switching binary weighted current sources and 4 most significant bits are thermometer decoded to switch 15 unary current sources. 8-bit binary and 4-bit unary subDAC models are shown in Figure 5.10 and Figure 5.11, respectively. 8-bit binary inputs are applied to the input of the binary subDAC and than passed through a dummy decoder (a delay block that equalizes the latency caused by the thermometer decoder in unary subDAC) and SRDs to the binary current source/switch array. The other 4-bit binary inputs are applied to the input of the unary subDAC, where by the mean of a thermometer decoder, are converted to 15 thermometer bits. Later through SRDs are applied to the unary current source/switch array.

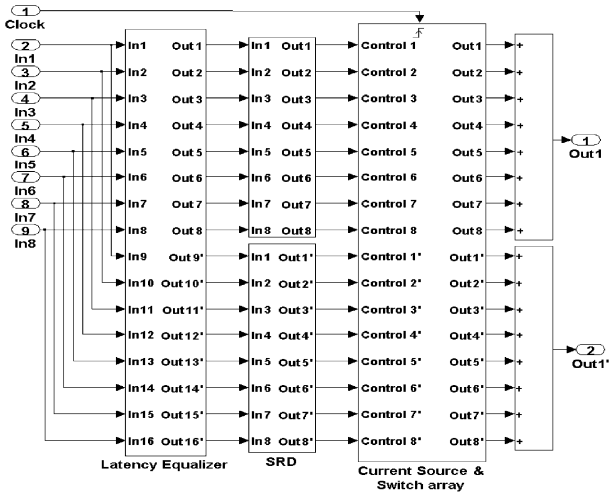

Figure 5.10: 8-bit binary subDAC model.

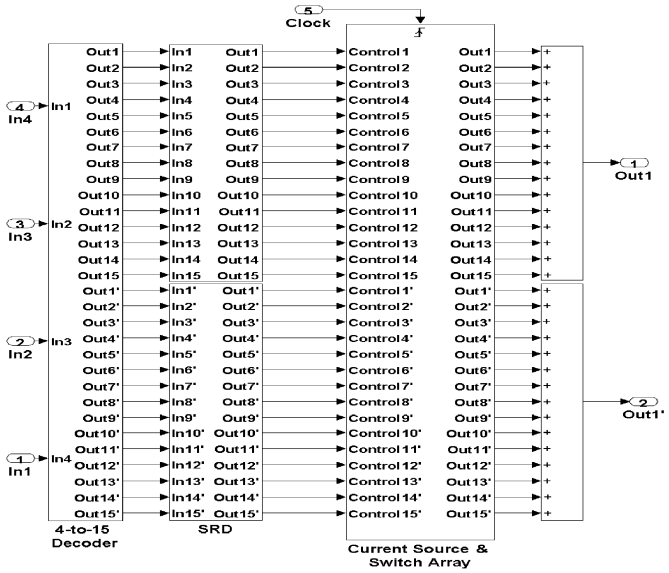

Figure 5.11: 4-bit unary subDAC model.

Each subDAC's model consists of a binary-to-thermometer decoder, swing reduced drivers and a core cell incorporating current sources and switches. 4-bit binary data are decoded into 15 thermometer bits by the mean of a 4-to-15 binary-to-thermometer decoder model constructed using binary-to-thermometer conversion functions. While the 4-to-15 binary-to-thermometer decoder of the unary subDAC is modeled using logical gates the dummy decoder of the binary subDAC is modeled simply by using a delay box reflecting the same latency as that of the binary-to-thermometer decoder. The operation of a current cell can be summarized as follows; the switch turns 'on' and conducts the predefined value of current (in this case 5μA) when the control input is higher than 2V i.e. SRD's output is at its high level (2.2V) and turns 'off' and outputs a '0' when the control input is lower than 2V i.e. SRD's output is at its low level (1.8V). In unary subDAC, there are 15 identical cells while in binary subDAC there are 8 cells with different current values.

Figure 5.12 shows the transfer characteristic of the 12-bit segmented current-steering DAC model simulated for the worst-case operation. The mismatching between current sources is set as 1% error in expected value of each current source. The update rate is 1GS/s.

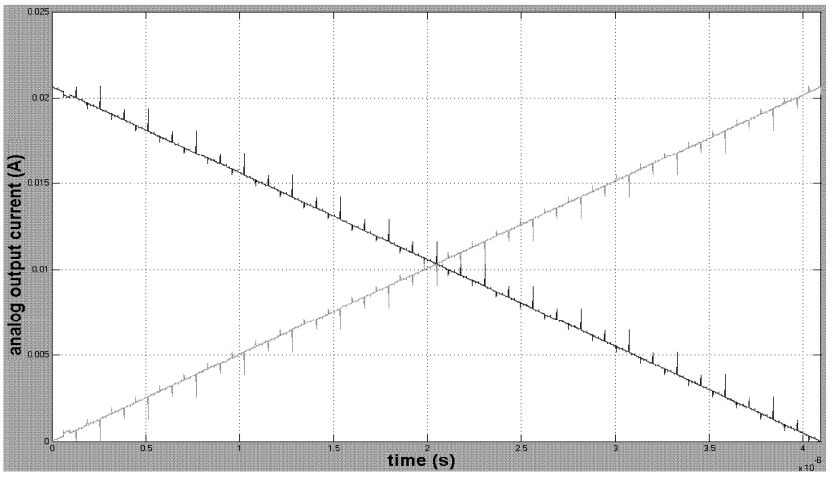

Figure 5.12: Transfer characteristic of 12-bit segmented DAC model.

The static performance analysis of the converter is performed using the developed MATLAB® based algorithm and tool for INL and DNL, given in detail in Appendix B. The INL and DNL for the worst-case operation of the 12-bit segmented current steering DAC are shown in Figure 5.13 and 5.14, respectively. From the simulation results the nonlinearities caused by the mismatching errors excluding the effect of the

glitches that mainly affect the dynamic performance, are calculated as INL smaller than 3.83LSB and DNL smaller than 2.97LSB.

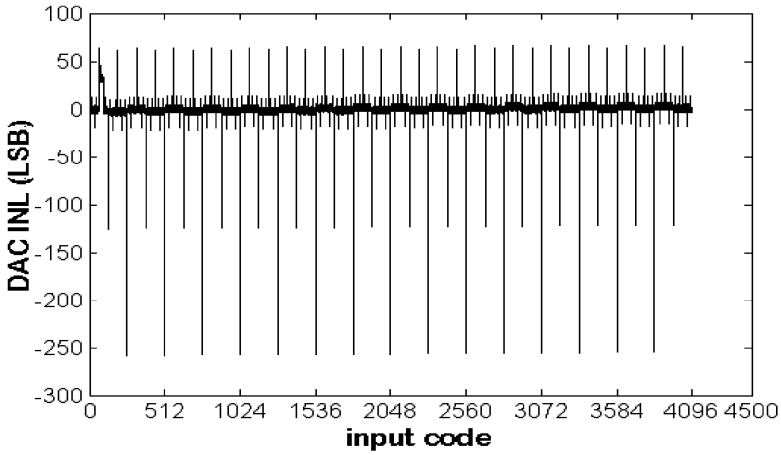

Figure 5.13: Simulated INL for 12-bit segmented DAC model.

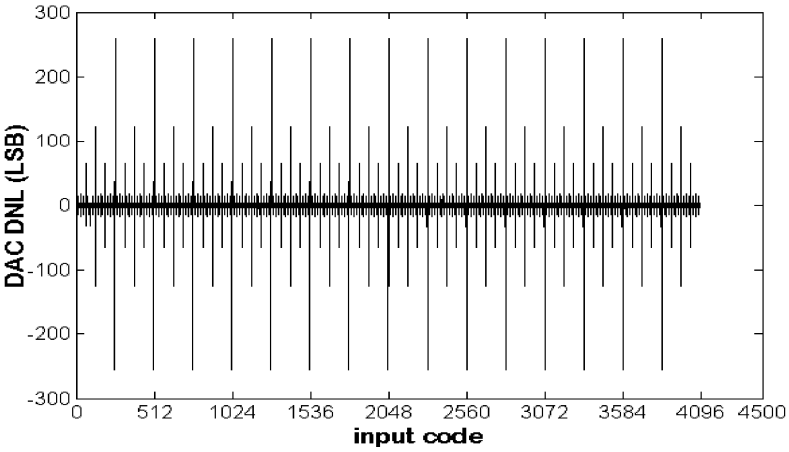

Figure 5.14: Simulated DNL for 12-bit segmented DAC model.

The dynamic performance of the modeled DAC system is simulated by applying digital signals corresponding to sine waves at different frequencies. To feed the inputs of the 12-bit modeled DACs with digital signals a 12-bit digital signal generator is constructed by using blocks of SIMULINK® libraries as shown in Figure 5.15. Digital signal generator consists of three main blocks; a continuous-time analog sine wave, a double to integer and an integer to bit conversion blocks. Actually, the points of the generated continuous-time sine signal are expressed in double numbers. The double to integer conversion block converts these numbers to integer numbers ranging from 0 to 4095 i.e. the point in the sine wave corresponding to 2047.58 double is converted as 2048 integer number. Later the integer numbers are converted

to 12-bit binary numbers. The developed model converts the applied analog signal to 12-bit digital data. If required for further analysis the model can be easily modified to generate modulated digital signals.

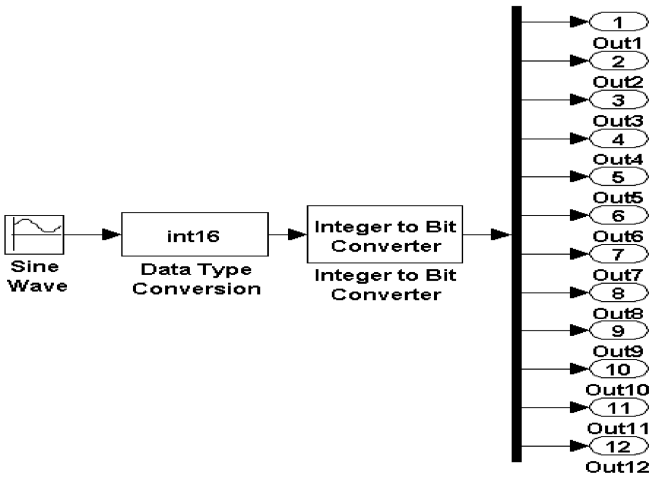

Figure 5.15: 12-bit digital signal generator.

A digital signal corresponding to a sine wave at 50MHz is applied to the inputs of the DAC. Figure 5.16 shows the analog output of the segmented DAC for an update rate of 1GS/s.

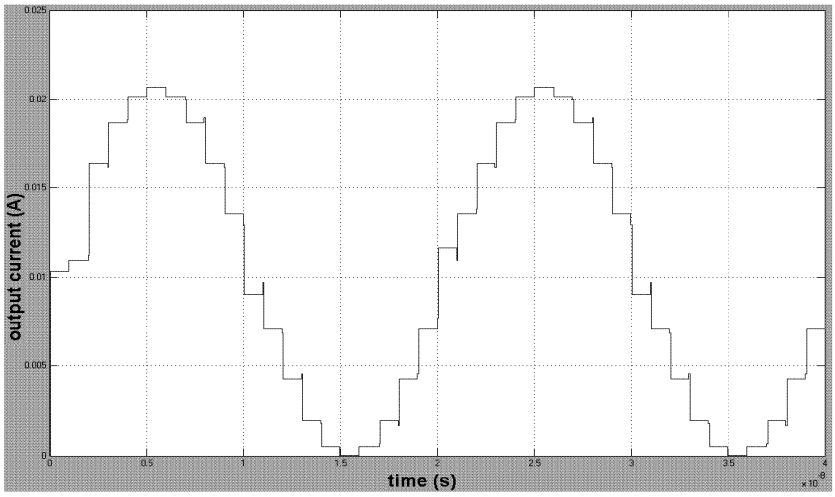

Figure 5.16: Output signal at 50MHz for the segmented DAC.

The overall dynamic range of the DAC is observed through SFDR analysis. The frequency spectrum of the output signal at 50MHz for the segmented DAC model is shown in Figure 5.17. For the simulated worst case operation scenario of the system SFDR of segmented DAC is 33dB.

5.3.4.2 12-bit parallel current-steering DAC model

The model for the 12-bit parallel current-steering DAC is based on the architecture given in Figure 3.5 and is shown by the block diagram in Figure. 5.18. The model consists of a 12-bit digital data generator and four 3-bit weighted unary subDACs. The system's current signal analog output is achieved by summing up subDACs' output currents.

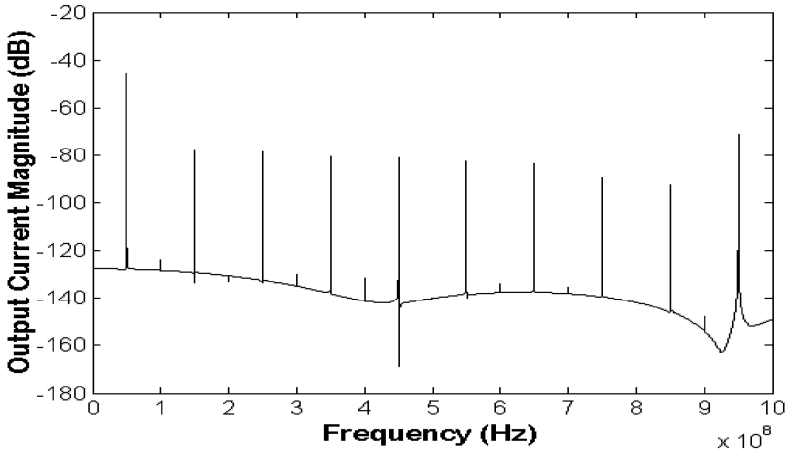

Figure 5.17: Frequency spectrum of the output sine at 50MHz for segmented DAC.

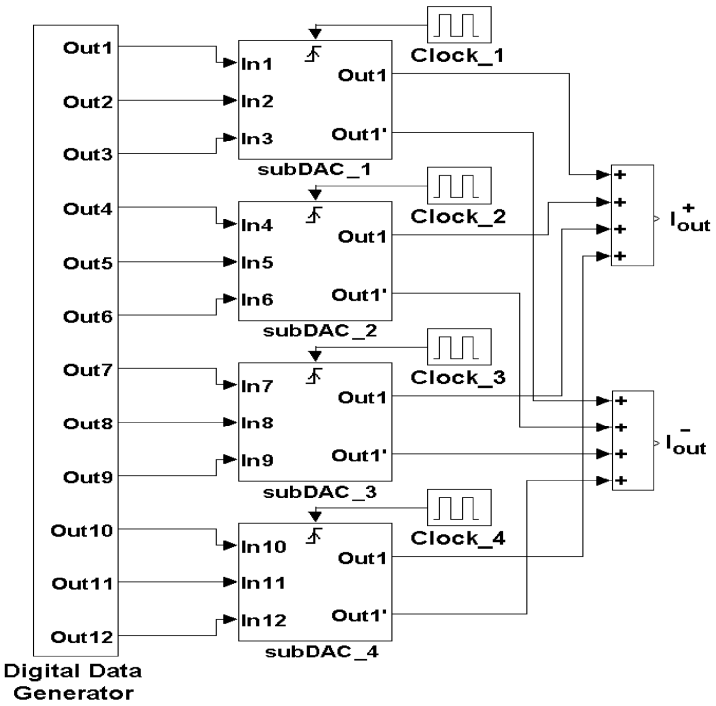

Figure 5.18: SIMULINK® model of the 12-bit parallel current-steering DAC.

The model of the subDAC used is identical with the model of the unary subDAC in

segmented current-steering DAC model shown in Figure 5.11 except the number of the binary inputs, which in this case are 3. Consequently, the constituent parts of the subDAC, binary-to-thermometer decoder, swing reduced driver and current source&switch array are similar and modeled in the same way. It is clear that for each subDAC a 3-to-7 binary-to-thermometer decoder is required to convert the binary input data to thermometer bits.

Figure 5.19 shows the transfer characteristic of 12-bit parallel current-steering DAC model simulated for the worst-case operation. The mismatching between current sources is set as 1% error in expected value of each current source. The update rate is 1GS/s.

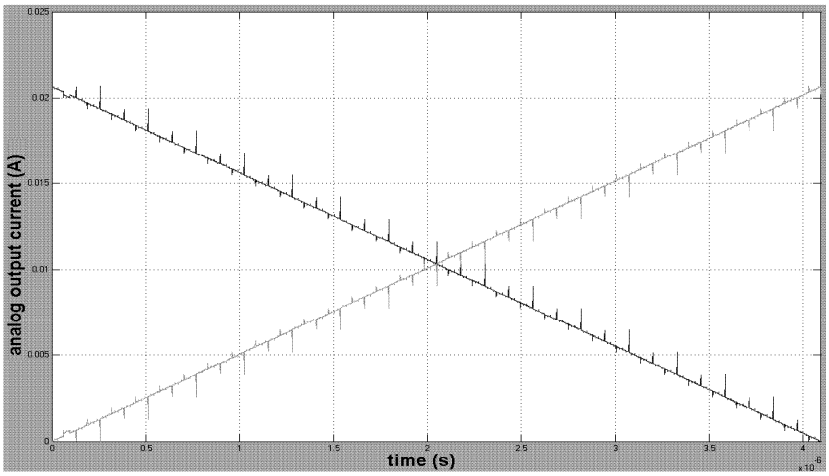

Figure 5.19: Transfer characteristic of 12-bit parallel DAC model.

Static performance of the DAC model is evaluated through simulated INL and DNL. The INL and DNL for the worst-case operation of the 12-bit parallel current steering DAC are shown in Figure 5.20 and 5.21, respectively. Simulation results show that INL is smaller than 2.1LSB and DNL is smaller than 1.13LSB.

A digital signal corresponding to a sine wave at 50MHz is applied to the input of the DAC. Figure 5.22 shows the analog output of the parallel DAC for an update rate of 1GS/s. The frequency spectrum of the output signal at 50MHz is shown in Figure 5.23. It can be seen that the SFDR of parallel DAC is 26dB. It is clear that the reduction of the glitches improves the SFDR of the DACs.

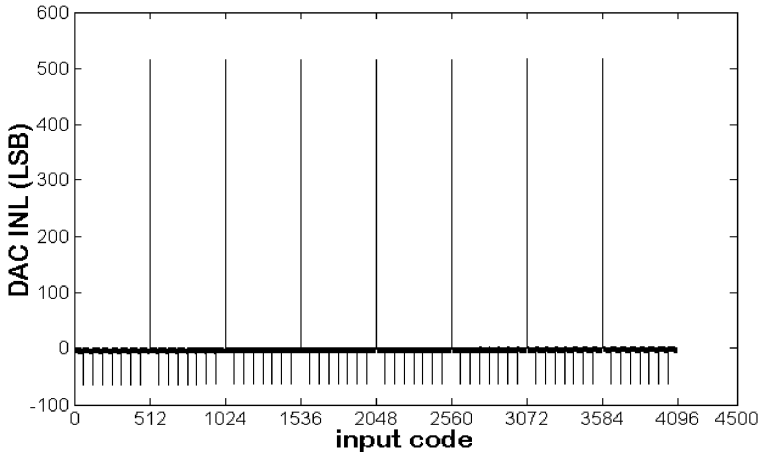

Figure 5.20: Simulated INL for 12-bit parallel DAC model.

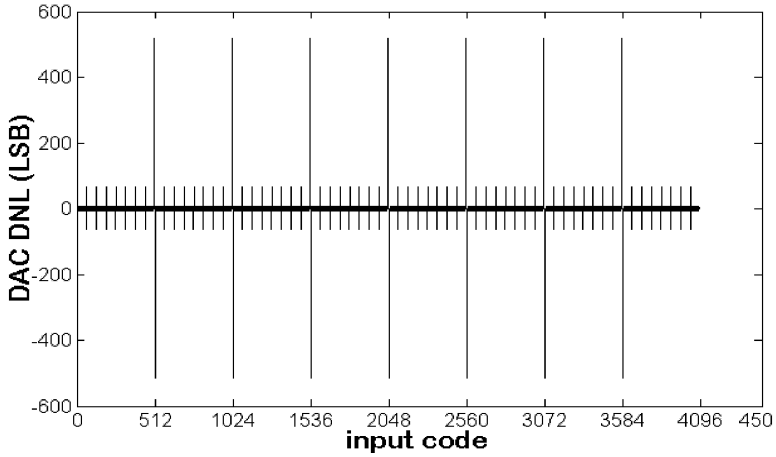

Figure 5.21: Simulated DNL for 12-bit parallel DAC model.

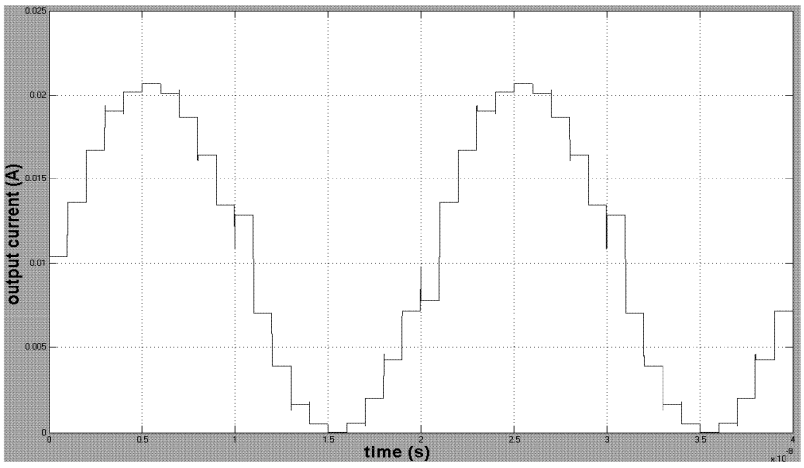

Figure 5.22: Output signal at 50MHz for the parallel DAC.

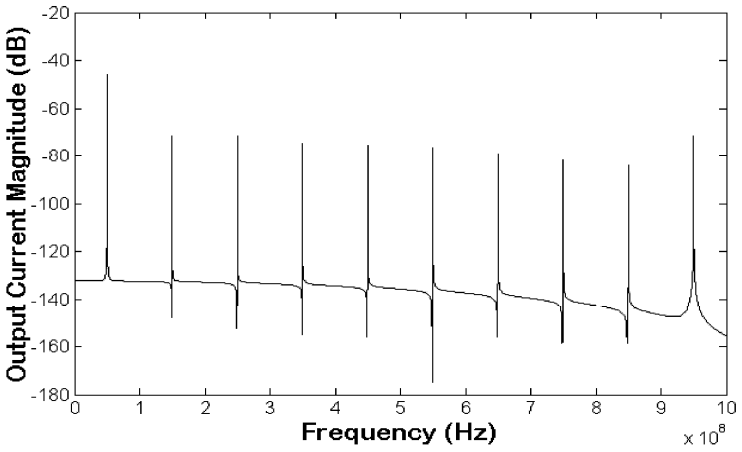

Figure 5.23: Frequency spectrum of the output sine at 50MHz for parallel DAC.

5.3.4.3 Conclusive remarks on SIMULINK® models

The accuracy of the models is verified through performance characteristics' simulations. Each modeled DAC is operated under worst case operation scenario and the static and dynamic performances are observed as in the above sections. The worst case operation for the segmented current-steering DAC is defined as the asynchronous operation of the binary weighted and unary subDACs, mismatching of the current sources in each subDAC, and the different latency of the input signals, while for parallel DAC it is defined as the asynchronous operation of subDACs and mismatching between current sources of different subDACs. The worst case conditions can be established by adjusting the clock signals (asynchronous operation), adding delay in the signals' path (latency), modifying the values of the current sources (mismatching) in blocks of the behavioral models.

A detailed information about the effects of the synchronization, latency and mismatching on the converters' performance can be obtained through the analysis of the behavioral models. The static and dynamic performances of the systems are evaluated using INL, DNL and SFDR parameters. The presented SIMULINK® behavioral model is attractive since it offers a complete view of the converter's nonideal behavior prior to transistor level design. The models enable the high speed design of DAC systems and give hints on the improvements that can be done during the design phase. The modeling methodology can be adapted for every current-steering DAC.

6. IMPLEMENTATION OF A 12-BIT HYBRID DAC WITH THE PROPOSED ARCHITECTURE

In this part of the thesis, the implementation of a 12-bit hybrid DAC with the proposed architecture is performed to illustrate the high-speed design of the high-resolution DACs. Firstly, the decision for the architecture and design methodology is described with the expected advantages and the possible drawbacks. Secondly, the floorplan given in a schematic representation is presented. The behavioral model for the selected architecture and the worst-case operation are analyzed next. Then the design of the building blocks is realized using AMS 0.35µm C35B4C3 (4 metal layers, 2 poly layers and a high resistive layer) CMOS Process, layout issues are discussed and post-layout simulations are performed using Cadence Custom IC Design Tools for each step of the design. Finally, the performance characteristics and the figure of merit of the realized layout are evaluated and conclusions are drawn.

6.1 Architecture and Design Methodology

The selection of architecture is dictated by the process technology, design time, core cell area and other specs related to the application field. Since 0.35µm CMOS process is available for the implementation of the DAC, the use of standard architectures (thermometer or segmented) that satisfies the specs, is design time consuming and core cell area is far from the minimum compared with realizations performed with recent process technologies i.e. core cell area of a DAC implemented using fully thermometer coded or segmented architecture in a 0.35µm CMOS process is much larger than counterparts implemented using the same architectures in a latest CMOS process. Thus, for fixed technology a tradeoff between design time, area, power consumption and other specs has to be done. Actually, design time and occupied area are somewhat affected in the same way, so that a complex architecture requires much more time and occupies a large area. The main spec to be considered here is the required resolution of 12-bit. The architecture most suitable for simple

design of high resolution DAC with minimum area is the hybrid one proposed in section 3.5. Among the two proposed hybrid architectures, the voltage-mode is more attractive since it possesses better matching properties and relatively occupies a smaller area than current-mode.

The general form of the hybrid voltage-mode architecture is previously shown in Figure 3.6. N-bit hybrid voltage-mode current-steering DAC consists of M parallel matched thermometer coded h-bit subDACs and a resistive network with weighted resistors connected to V_{DD}. It must be noted that N, M, h are integer numbers and $N=h*M$. To realize a 12-bit DAC using this architecture there exist 4 possibilities as summarized in Table 6.1.

Table 6.1 : Possible choices for 12-bit hybrid voltage-mode DAC realization.

	Resolution of subDAC (h)	Matched subDACs (M)	No. of resistors
I	6-bit	2	2
II	4-bit	3	3
III	3-bit	4	4
IV	2-bit	6	6

To decide for the best choice parameters like simplicity in design and area must be considered. One of the factors that may degrade the minimum area property is determined by the resistors' size. Using the equation (3.6) and $R_{unit}=100\Omega$ the sizes of the resistors for each choice are calculated as shown in Table 6.2. It must be noted that the value of R_{unit} is determined considering the matching required between resistors and layout area. Thus, decreasing the size of the unit resistor will result in a small area and an increased mismatch, while increasing the size of the unit resistor will result in a large area and a decreased mismatch. Required tradeoff between mismatch and area leads to selection of reasonable values for R_{unit}.

Table 6.2 : Sizes of the resistors of the resistive network of each choice.

	R_1	R_2	R_3	R_4	R_5	R_6
I	100Ω	6.3kΩ	-	-	-	-
II	100Ω	1.5kΩ	24kΩ	-	-	-
III	100Ω	700Ω	5.6kΩ	44.8kΩ	-	-
IV	100Ω	300Ω	1.2kΩ	4.8kΩ	19.2kΩ	76.8kΩ

As it can be seen from Table 6.1 for realisation of choice I two matched 6-bit thermometer coded subDACs are required, violating the simplicity in design condition. Choice IV is not suitable because of the number and the wide range of sizes of the resistors. Thus, the minimum area condition is seriously violated. Choices II and III are close to each other at first glance. But, since choice II requires a 4-to-15 binary-to-thermometer decoder and the number of logic gates increases exponentially for each increased bit, from this point of view choice III is much more advantageous. Besides this fact, choice II requires 90 inverting SRDs of Figure 4.20 (30 SRDs for each subDAC: 15 for thermometer outputs and 15 for complementary outputs), while choice III requires only 56 inverting SRDs. Since inverting SRD dissipates DC power, the power consumption for choice II is higher. The above advantages make choice III attractive for the design and it is selected in expense of a larger area of the resistive networks compared to those of choice II.

The voltage-mode structure selected for the 12-bit hybrid DAC, which avails a voltage signal as its analog output, is shown in Figure 6.1 [59].

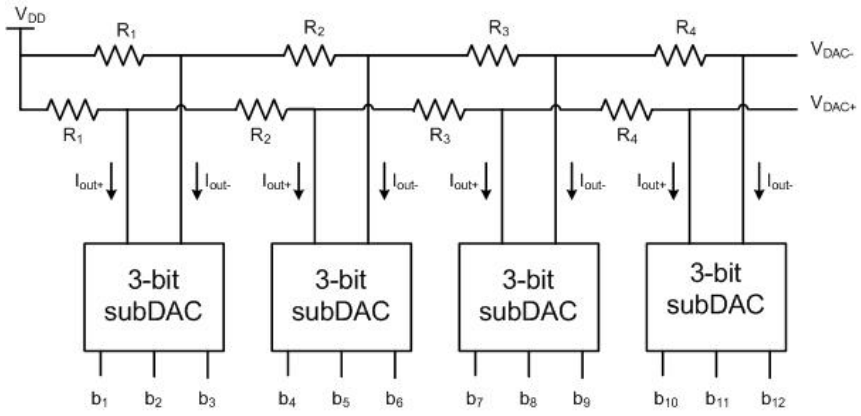

Figure 6.1 : Proposed voltage-mode 12-bit hybrid DAC.

6.2 Floorplan of the Implementation

The floorplan based on a schematic representation of the 12-bit hybrid DAC is shown in Figure 6.2.

The 12 binary inputs are decoded from binary-to-thermometer codes by the means of 4 identical 3-to-7 binary-to-thermometer decoders. Decoding circuitry is placed at the top of the topology. Latches and SRDs are placed immediately before the

switches to reduce the glitches. An external clock is applied to the latches to achieve the required synchronization of the control signals of the switches. Together with the decoders these components constitute the digital part of the system. A global biasing is used to bias the matched current sources. The highlighted sections show the subDACs. The outputs of the subDACs are connected to the resistive networks containing weighted resistors placed at the bottom of the topology. V_{DAC+} and V_{DAC-} are the voltage-mode outputs of the hybrid DAC.

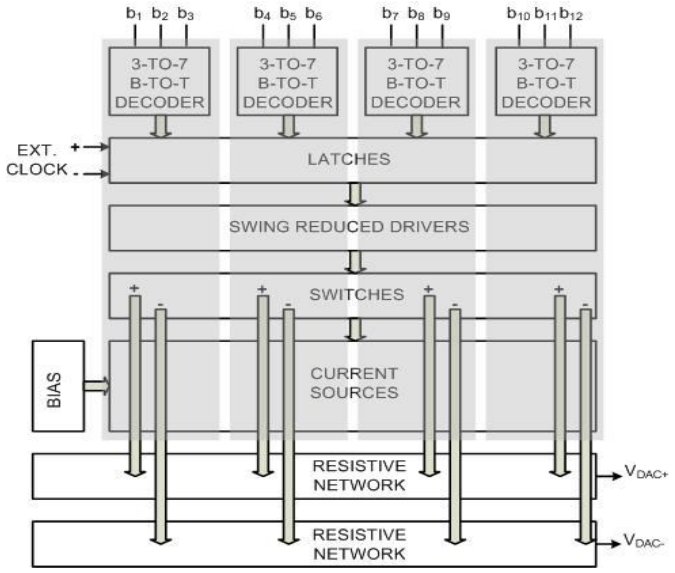

Figure 6.2 : The floorplan of the 12-bit hybrid DAC.

6.3 Behavioral Model and Simulation of the 12-bit Hybrid DAC

The SIMULINK® model of the 12-bit hybrid DAC is shown in Figure 6.3. The model consists of a 12-bit digital data generator, four 3-bit matched unary subDACs and two resistive networks. The voltage signal analog output is achieved by weighting output currents of the subDACs through scaled resistors according to equation (3.6).

The model of the subDAC used is identical to the model of the unary subDAC in segmented current-steering DAC model shown in Figure 5.11 except the number of the binary inputs which in this case is 3. Consequently the constituent parts of the subDAC, binary-to-thermometer decoder, swing reduced driver and current source&switch array are similar and modeled in the same way. It is clear that 3-to-7

binary-to-thermometer decoder is required to convert the binary input data to thermometer bits.

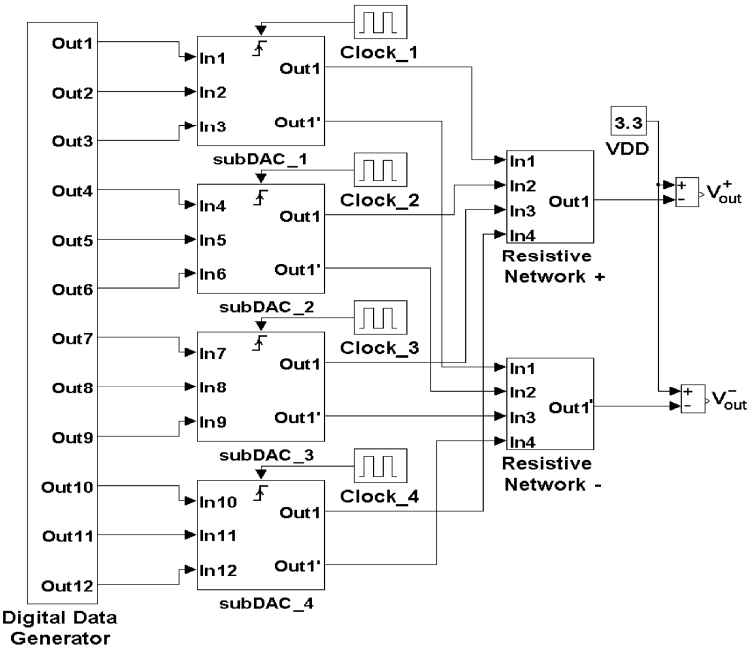

Figure 6.3 : SIMULINK® model of the 12-bit hybrid DAC.

The model for the resistive network is shown in Figure 6.4. It is constructed in such a way that the output corresponds to the term inside parenthesis in (3.5) for N=12. The inputs 1 to 4 are the subDACs' current outputs and the weights from 1 to 4 multiplied by R_{unit}, are the resistors R_1, (R_1+R_2), $(R_1+R_2+R_3)$ and $(R_1+R_2+R_3+R_4)$. Selecting R_{unit}=100Ω and using the equation (3.6) the resistors of choice III shown in Table 6.2, are obtained.

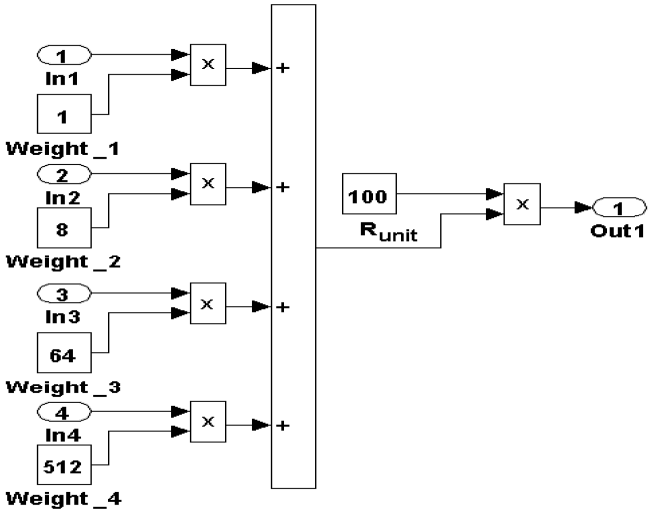

Figure 6.4 : Resistive network model.

The behavioral model of the 12-bit hybrid DAC operated under worst-case operation conditions is simulated and the static and dynamic performance is observed. The worst-case operation for hybrid DAC is defined as the asynchronous operation of subDACs, mismatching between current sources of different subDACs and mismatching of resistors in resistive network. The worst case conditions can be established by adjusting the clock signals, adding delay in the signals' path, modifying the values of the current sources and resistors in models.

To obtain a possible worst-case operation of the hybrid DAC, 1% mismatching is applied to the current sources of the asynchronous subDACs. The transfer characteristic is shown in Figure 6.5. The update rate in this case is 1GS/s.

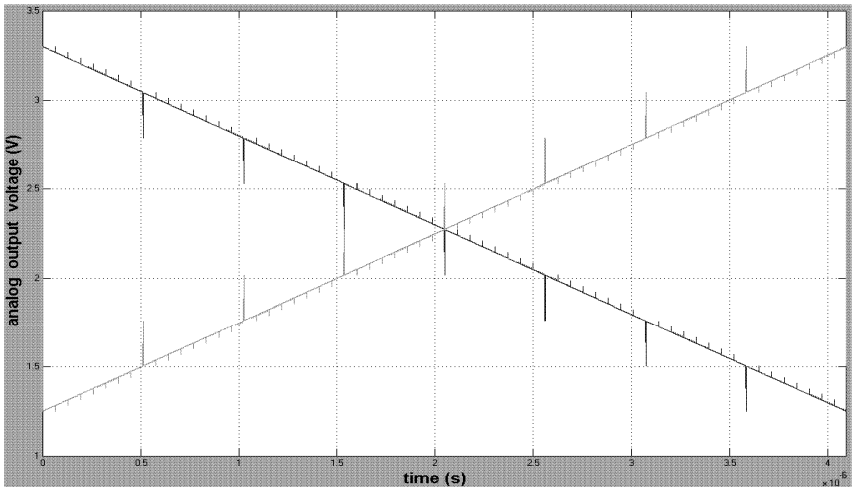

Figure 6.5 : Transfer characteristic of the 12-bit hybrid DAC model.

The INL and DNL for hybrid DAC are shown in Figure 6.6 and Figure 6.7, respectively.

From the simulation results the nonlinearities caused by the mismatching errors excluding the effect of the glitches that mainly affect the dynamic performance are calculated as INL smaller than 1.87LSB and DNL smaller than 1.07LSB.

Figure 6.8 shows the analog output of the hybrid DAC for an update rate of 1GS/s when a digital signal corresponding to a sine wave at 50MHz is applied to the input of the DAC.

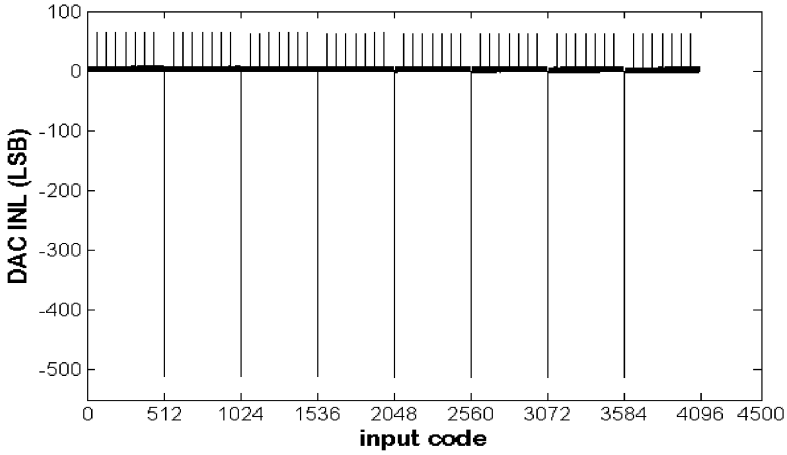

Figure 6.6 : Simulated INL for hybrid DAC model.

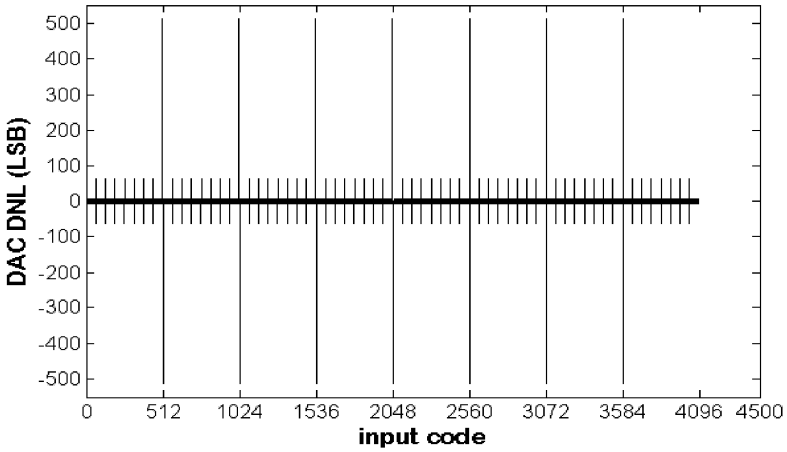

Figure 6.7 : Simulated DNL for hybrid DAC model.

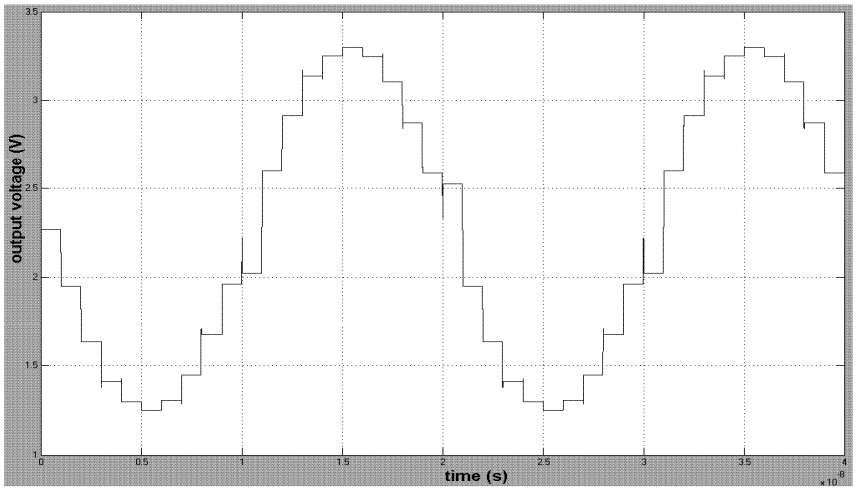

Figure 6.8 : Output sinusoidal signal at 50MHz for hybrid DAC model.

The frequency spectrum of the output signal at 50MHz is shown in Figure 6.9.

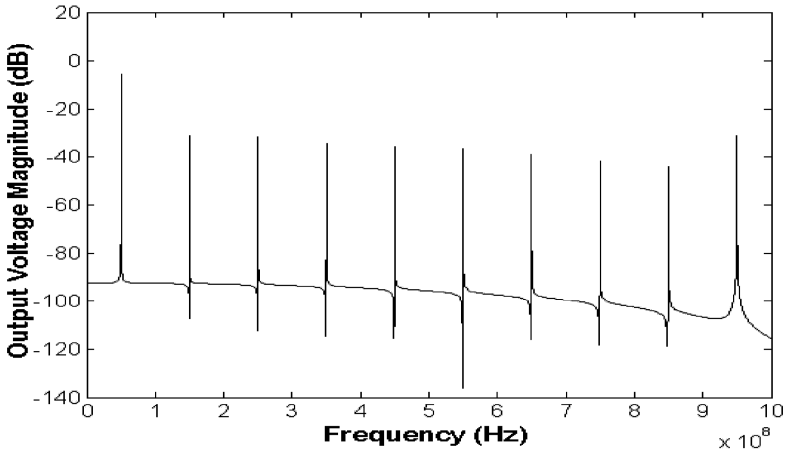

Figure 6.9 : Frequency spectrum of the output sinusoidal signal at 50MHz for hybrid DAC model.

For the simulated worst-case operation, SFDR of hybrid DAC is 26dB.

As it can be seen the model offers a complete view of the hybrid DAC's behavior prior to transistor level design. A detailed information about the effects of the synchronization, latency and mismatching of the components on the DAC's performance is obtained through this analysis.

6.4 Design of the Building Blocks

The circuit schematic illustrating the circuits of the blocks for the hybrid DAC is shown in Figure 6.10.

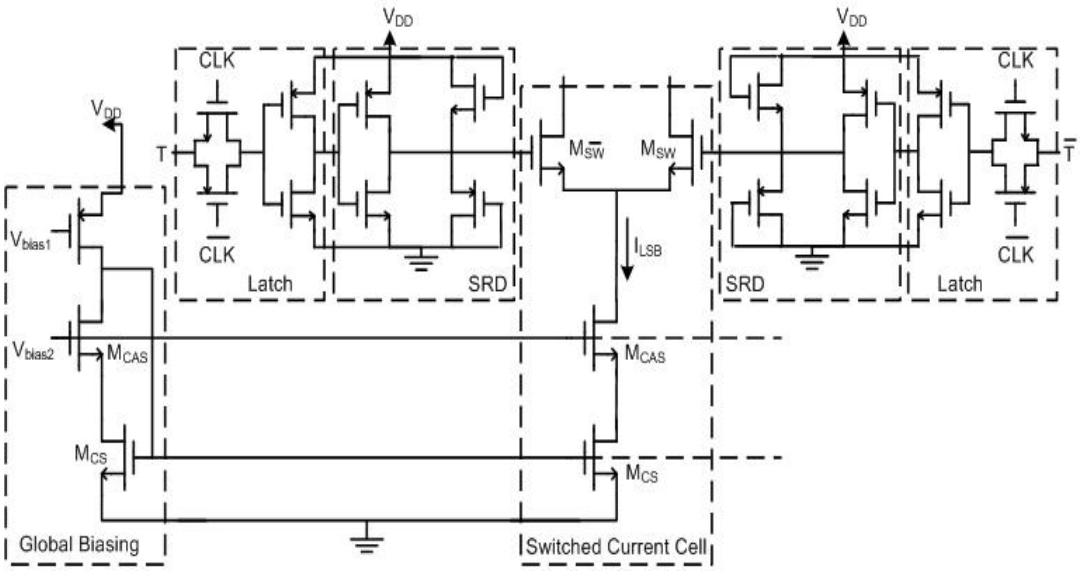

Figure 6.10 : Circuit schematic of the building blocks of hybrid DAC.

6.4.1 Switched current cell

As it can be seen from Figure 6.10 switched current cell consists of a low-voltage cascode current source and switch transistors. The dimensions of the current source, cascode and switch transistors are determined according to the sizing procedure described in chapter 4. In addition, overdrive voltages for transistors are selected considering the analytical expressions derived in [60]. These analytical expressions that depend on circuit and mismatch parameters are used in the design procedure "for the optimum sizing of the current source+cascode+switch current cell topology. All the dimensions of the transistors are calculated using the typical values of the MOS electrical parameters provided by the AMS 0.35µm CMOS C35 Process technology. Table 6.3 gives the typical values of the electrical parameters of MOS transistors.

Table 6.3 : Typical values of electrical parameters of MOS transistors.

Tr. Type	**Process Transconductance Parameter** ($\mu A/V^2$)	**Threshold Voltage** (V)
nMOS	K_n=170	V_{Tn}=0.50
pMOS	K_p=58	V_{Tp}=-0.65

The switched current cell specifications for 12-bit hybrid DAC are given in Table 6.4. It is clear that the required matching is guaranteed by determining the aspect ratios of the current source transistors using equations (4.11) and (4.12).

Table 6.4 : Switched current cell specifications for 12-bit hybrid DAC.

Symbol	**Value**
A_{VT}	9.5 mVµm
A_β	%0.7 µm
σ_I/I	0.25%
$(V_{GS}-V_T)_{CS}$	0.4V
$(V_{GS}-V_T)_{CAS}$	0.25V
$(V_{GS}-V_T)_{SW}$	0.18V
V_{DD}	3.3V
I_{LSB}	5µA
AMS	0.35µm

A global biasing circuit biases all the identical switched current cells in the 12-bit hybrid DAC. V_{bias1} and V_{bias2} are applied externally using DC voltage supplies. $V_{bias1}=2.2V$ is selected to provide $I_{LSB}=5\mu A$ and $V_{bias2}=1.6V$ is selected to satisfy equation (4.6) for the proper biasing of the low-voltage cascode. The dimensions of the cascode transistors are determined by making a tradeoff between the required output impedance and a small parasitic drain capacitance with minimum area for the transistor. To increase the output resistance the gate-length L of the cascode transistor is kept larger than the minimum value allowed by the process (0.35μm for AMS). The calculations of the dimensions for the cascode transistor are performed using the saturation equation of MOS transistor for $I_D=I_{LSB}=5\mu A$. The switch transistors operate in the saturation region and their dimensions are selected small to increase speed and to reduce the timing errors.

Dimensions of the transistors in the switched current cell are given in Table 6.5. In the implementation of the 12-bit hybrid DAC 28 matched cells are used, 7 cells for each subDAC.

Table 6.5 : Dimensions of the switched current cell's transistors.

Tr.	W(μm)	L(μm)
M_{CS}	8.4	22.4
M_{CAS}	1.05	0.7
M_{SW}	0.7	0.35

6.4.2 3-to-7 binary-to-thermometer decoder

Instead of a 12-to-4095 binary-to-thermometer decoder, required for a 12-bit fully thermometer coded DAC, four 3-to-7 binary-to-thermometer decoders are used in the implementation of the 12-bit hybrid DAC. This choice extremely reduces the area and the power consumption of the digital circuitry in the DAC. Since the decoder is in the signal's path the goal is to design a high-speed decoder. For this reason a fully custom-made 3-to-7 binary-to-thermometer decoder, previously shown in Figure 4.13, is used. Conversion codes are that of Table 4.3 and the gates are exactly sized as described in Section 4.4.3.

Decoder's performance is validated through Spectre simulations. It must be noted that the simulations here are aimed to show the operation of the decoder's circuit and are performed with the decoder apart from the other parts of the DAC system. Thus, the load effect and clock feedthrough in the signal is not visible in the output signals. Figure 6.11 and Figure 6.12 show binary inputs and thermometer coded outputs of the 3-to-7 binary- to-thermometer decoder, respectively.

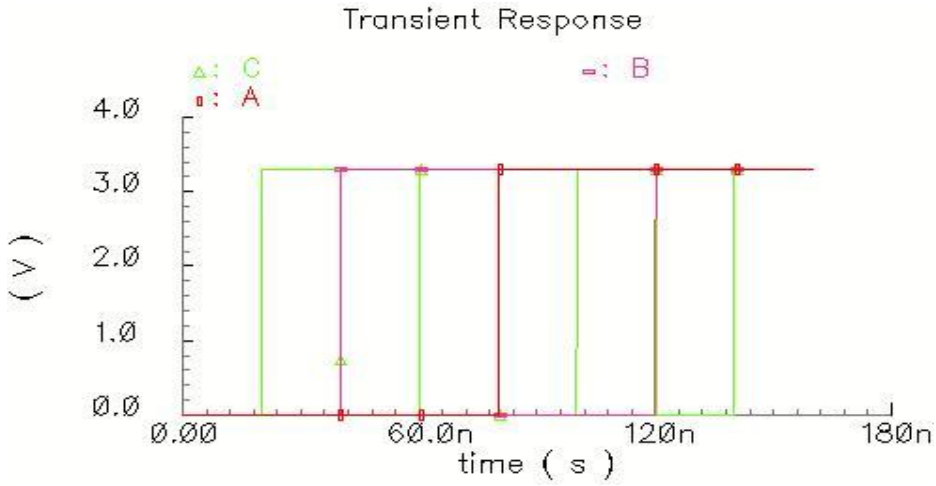

Figure 6.11 : Binary inputs of the 3-to-7 binary-to-thermometer decoder.

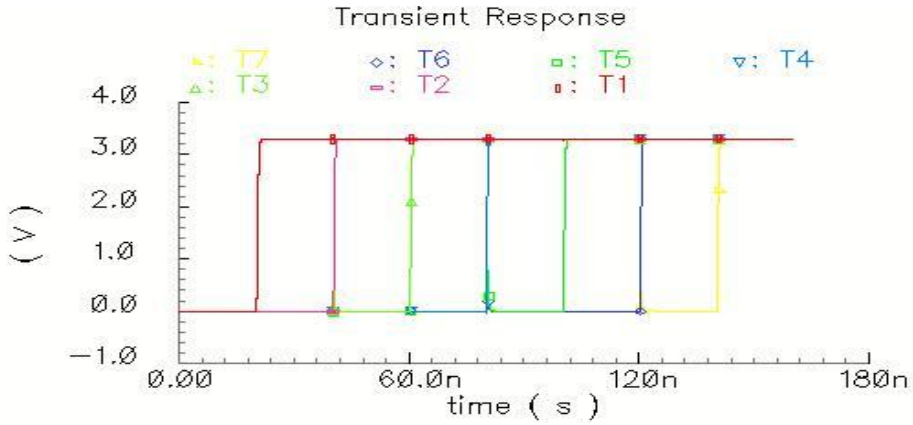

Figure 6.12 : Thermometer outputs of the 3-to-7 binary-to-thermometer decoder.

Operation speed of the decoder is calculated through delay analysis. The longest delay in the output signals limits the speed of the circuit. Practically, it is very hard to equalize all the delays in the design. But, along with the synchronization of signals the delays are somewhat approximated. The longest delay belongs to the T_1 code and is 0.5ns. That means that the designed decoder can operate at high speeds up to 2GHz. Another important parameter is the settling time which is equal to 1.7ns.

6.4.3 Latch and SRD

One of the features of the 12-bit hybrid DAC design is the use of the dynamic latch that has a small delay and by the means of the buffer (inverter) used in the signal's path increases the speed of the system.

The latch is designed using the procedure described in Section 4.5.1. The dimensions of the transmission gate and inverter transistors are determined using equations (4.25) and (4.26) for a propagation delay of *0.1ns* and for a gate capacitance of *50fF*. Table 6.6 shows the dimensions of the transistors in the dynamic latch.

Table 6.6 : Dimensions of the latch's transistors.

	Transmission Gate		**Inverter**	
	NMOS	PMOS	NMOS	PMOS
W(µm)	1.75	4.2	1.75	4.2
L(µm)	0.35	0.35	0.35	0.35

Figure 6.13 shows the output of the latch. As it can be seen the delay required to reach 50% point equals to 0.1ns.

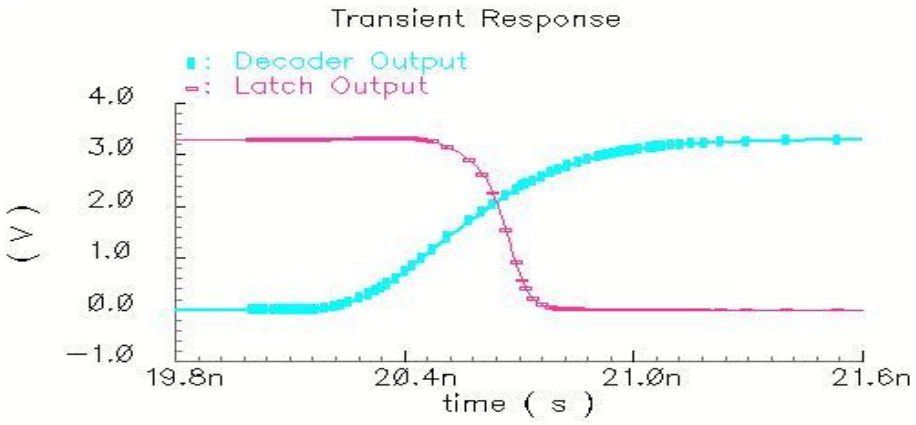

Figure 6.13 : Latch's output.

The inverting SRD circuit proposed in [55] and designed in Section 4.5.2.2 is used in the implementation of the 12-bit hybrid DAC. A tradeoff between area, accuracy, simplicity and power consumption is performed. The benefits of this choice are area, accuracy and simplicity, in expense of a moderate static power consumption. Although, there exist accurate switch drivers [20], they are not suitable for this

design because of their increased number of devices and additional biasing circuits. Thus, the small area feature aimed for 12-bit hybrid DAC is violated. Another reason for the inverting SRD choice is the use of dynamic D-latch in synchronization circuitry. From Figure 6.13 it is clear that the latch itself is an inverting device. Figure 6.14 shows the effect of the SRD in the DAC's implementation. T_1 signal is observed at the output of the decoder, latch and SRD. Through a swing reduction from 3.3V to 400mV the clock feedthrough effect is reduced significantly.

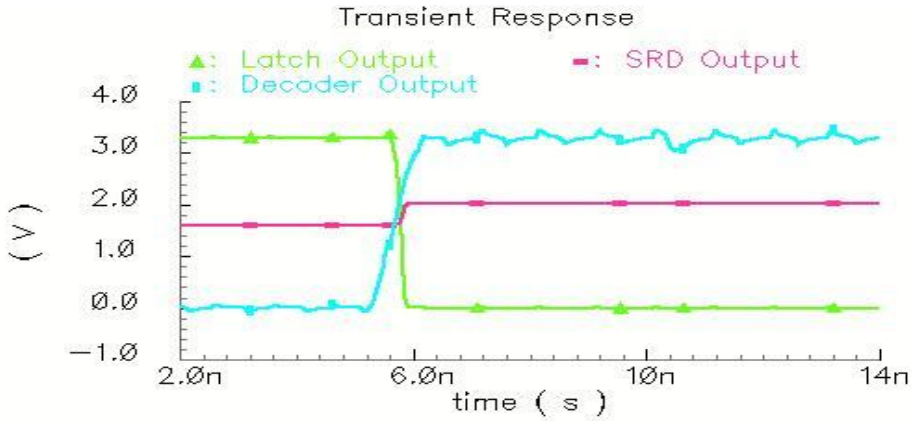

Figure 6.14 : T_1 code decoder, latch and SRD outputs.

Besides the improvement in the digital signal feedthrough to the output nodes, the current spikes on the output signal are vanished too. Figure 6.15 shows the current outputs of a switched current cell with and without SRD circuit.

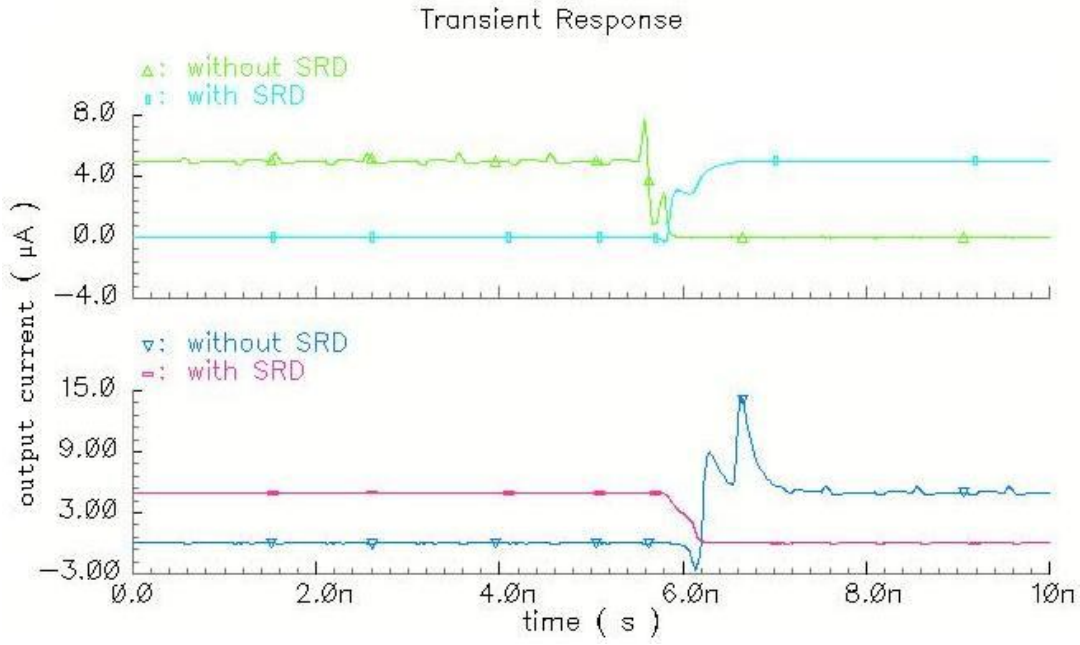

Figure 6.15 : Output current signal of the switched current cell.

It must be noted that the use of the inverting SRD is application dependent. A large number (some hundreds or more) of inverting SRDs used in the system degrades seriously the power consumption requirements. In applications where the small area requirement is dominant and the power consumption of the system itself is very small as in this design a limited number of SRDs can be used.

6.4.4 Layout issues

Prior to layout of the chip a floorplan is required. The floorplan is the outline-only design that shows how all the blocks are interconnected together and how the signals will flow between those blocks [61]. Floorplanning of the layout is dictated by the sub-blocks, their interconnections, wiring and other factors like clock tree connections, external bias etc.

12-bit hybrid DAC consists of 4 matched current-steering subDACs (decoders, latches, SRDs etc.) and 2 identical resistive networks. The floorplan of the layout is shown in Figure 6.16.

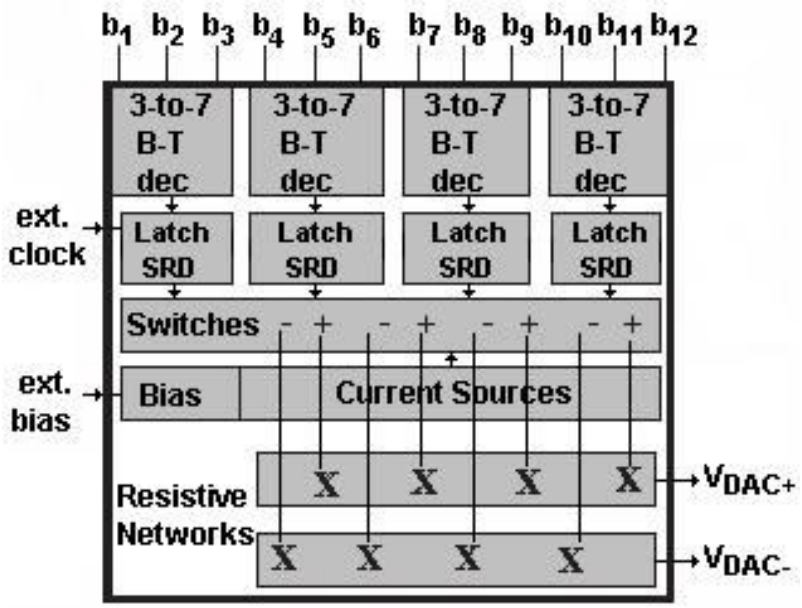

Figure 6.16 : Floorplan of the 12-bit hybrid DAC layout.

The layout is optimized by arranging the blocks according to their functions and the part of the system they belong to (digital or analog). This prevents any possible coupling between digital and analog part of the system. The 3-to-7 binary-to-thermometer decoders followed by latches and SRDs are placed at the top, switches

in the middle and current sources together with the resistive networks at the bottom of the layout. To achieve good matching 28 (7 current sources for each subDAC) current sources plus the reference current source are laid out together. The layout of the devices serving as cascode transistors is done in a similar way. Since switches are included to the digital part of the system they are separated by guard rings from the analog part to eliminate the noise coming from the former. Also, to avoid any noise disturbance the supply rails of digital and analog parts are separated. The layout of the digital circuitry (decoders and synchronization circuitry) is fully custom-made for an optimum area and high update rate. The inputs for the external clock and bias are placed at the left side apart from each other.

The main concern to be considered is the layout of the resistive networks since the resistors increase the occupied area by 30-40% of the existing active area. Fortunately in AMS 0.35µm CMOS C35 process it is possible to lay out resistors using high resistive poly. To achieve the best matching performance the resistors in the resistive network are realized as shown in Figure 6.17. According to the design rules and the guidelines of the process the unit resistor is selected to be 11.2kΩ.

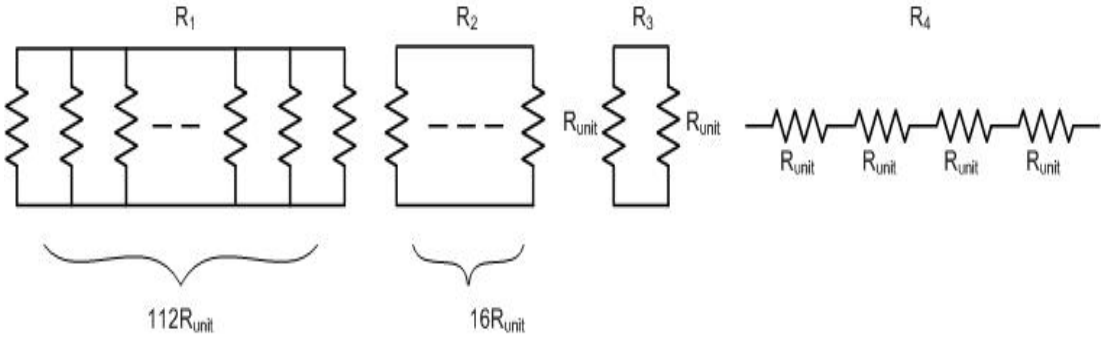

Figure 6.17 : Resistors of the resistive network.

Using AMS 0.35µm C35B4C3 (4 metal layers, 2 poly layers and a high resistive layer) CMOS process technology parameters the layout of the 12-bit hybrid DAC is realized as shown in Figure. 6.18 [59]. As it can be seen the layout is optimized for minimum area.

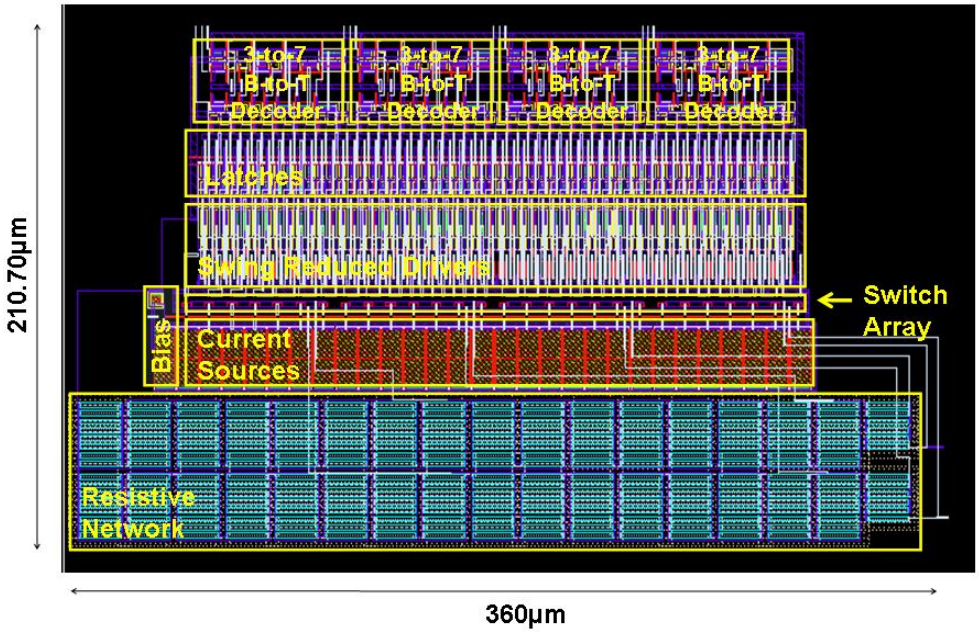

Figure 6.18 : Layout of the 12-bit hybrid DAC.

6.5 Performance Verification

Performance is validated through post-layout simulations using UltraSim. For verification purposes static and dynamic characteristics are investigated. Also, for comparison of this work with recently presented converters, figure of merit is calculated.

6.5.1 Static performance

The transfer characteristic of the 12-bit hybrid DAC is shown in Figure 6.19.

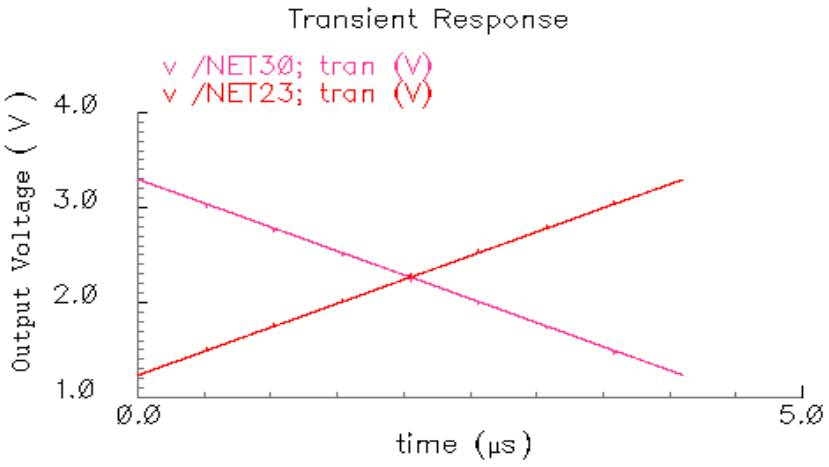

Figure 6.19 : Transfer characteristic of the 12-bit hybrid DAC.

The INL and DNL performance are measured by processing the data gathered from the simulations using the MATLAB codes given in Appendix B. The INL and DNL profiles are shown in Figure 6.20 and Figure 6.21, respectively.

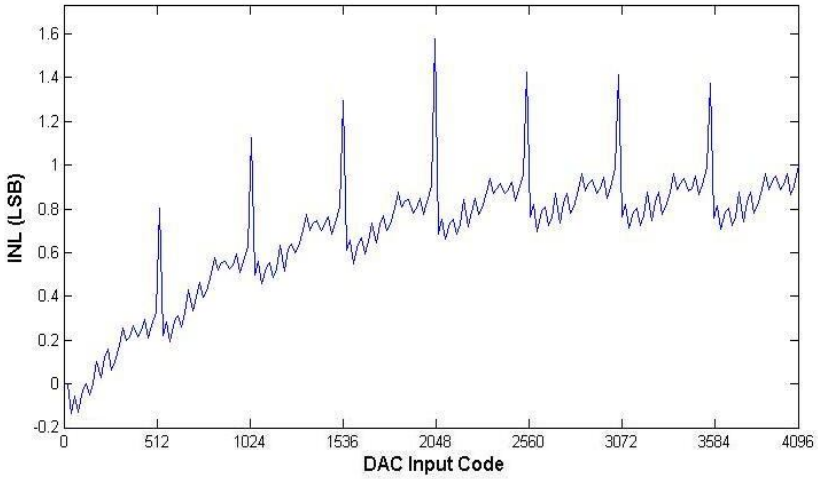

Figure 6.20 : INL performance of the 12-bit hybrid DAC.

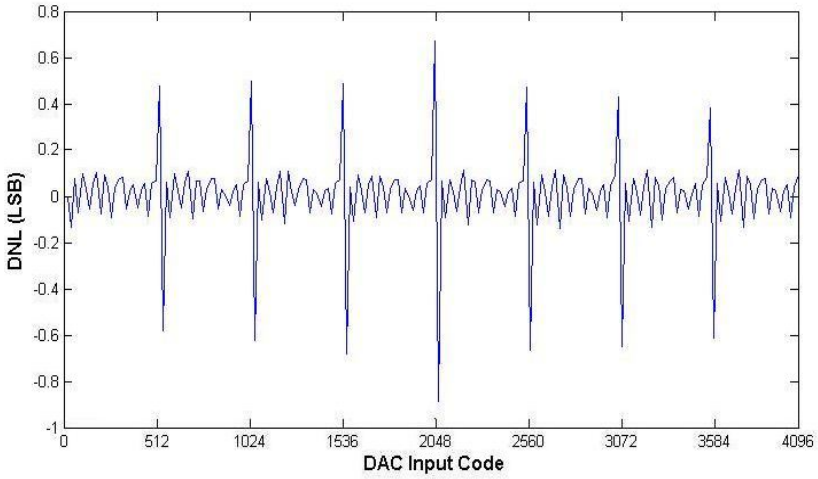

Figure 6.21 : DNL performance of the 12-bit hybrid DAC.

Both INL and DNL figures include the effect of the glitches. Since glitches occurr at high frequencies they can be supressed using low-pass filter at the output of the DAC. Also, their instant occurrence mainly degrades the dynamic performance of the DAC. For this reason in nonlinearity calculations the effect of the glitches is neglected. From Figure 6.20 and Figure 6.21 it can be concluded that INL error is smaller than 0.9LSB and DNL error is smaller than 0.2LSB.

6.5.2 Dynamic performance

The dynamic performance simulations are performed by applying signals to the DAC inputs through an ideal ADC. The details about the testbench and ideal ADC's AHDL code are given in Appendix C.

The settling time of the DAC is simulated by changing the digital inputs of the DAC from all zeros to all ones and vice versa i.e. time necessary for the DAC to settle to its final value after 0 to full scale or full scale to 0 transition. Figure 6.22 shows the settling time calculation for 12-bit hybrid DAC. Both settling times are equal and are calculated to be 14ns to 0.2%.

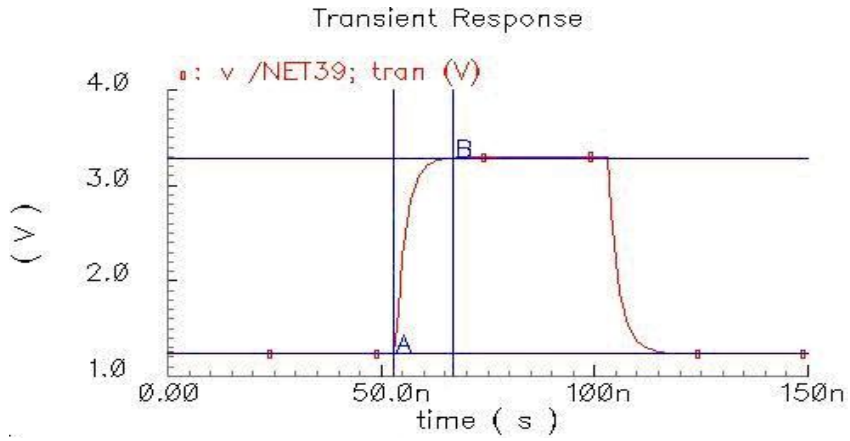

Figure 6.22 : Settling time of the 12-bit hybrid DAC.

Figure 6.23 shows the output of the DAC when a sinusoidal signal at 1MHz is applied to the input of the ideal ADC. The update rate in this case is 200MS/s. It must be noted that the applied sinusoidal signal to the input of the ideal ADC is converted into a digital signal and after that is applied to the DAC's input.

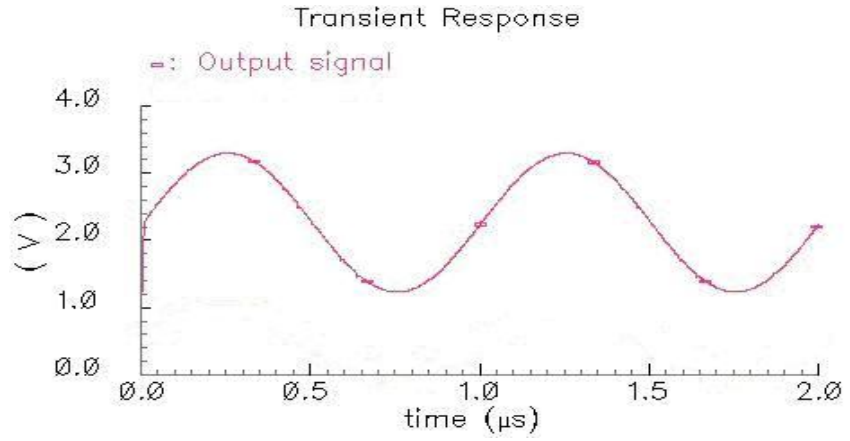

Figure 6.23 : Output signal at 1MHz for an update rate of 200MS/s.

The most important parameter indicating the dynamic performance of the DAC is SFDR. Figure 6.24 shows the SFDR of the DAC as a function of the input signal frequency for fixed update rates, from 100MS/s up to 1GS/s. As can be seen from the figure for a fixed update rate of 200MS/s, SFDR up to 70dB can be obtained for sinusoidal input signal up to 1MHz. Similarly, for a fixed update rate of 100MS/s, SFDR up to 64dB can be obtained for sinusoidal input signal up to 5MHz. Even for a fixed update rate of 1GS/s, a SFDR of 64dB can be obtained for input signal at 500kHz.

The SFDR as a function of the update rate is given in Figure 6.25 for different sinusoidal signals from 100kHz up to 50MHz.

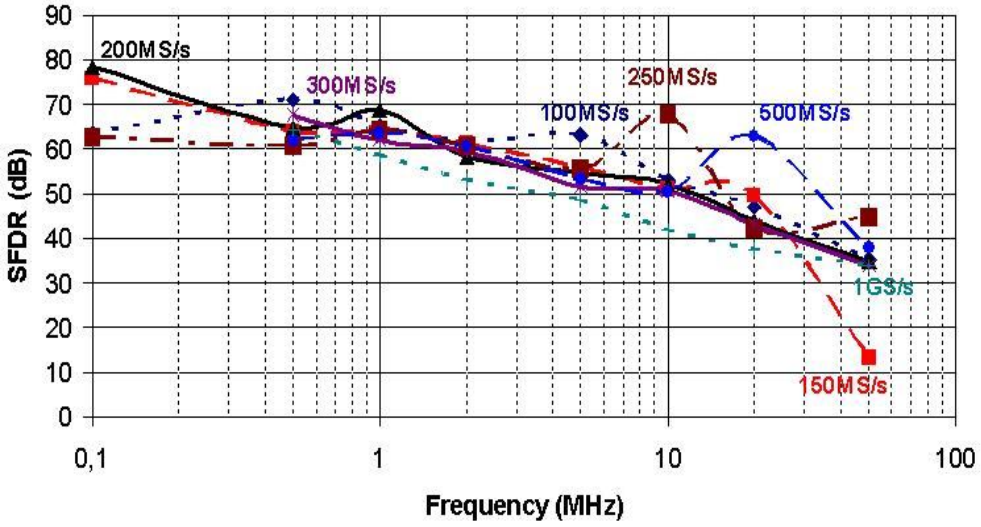

Figure 6.24 : SFDR as a function of the input signal frequency.

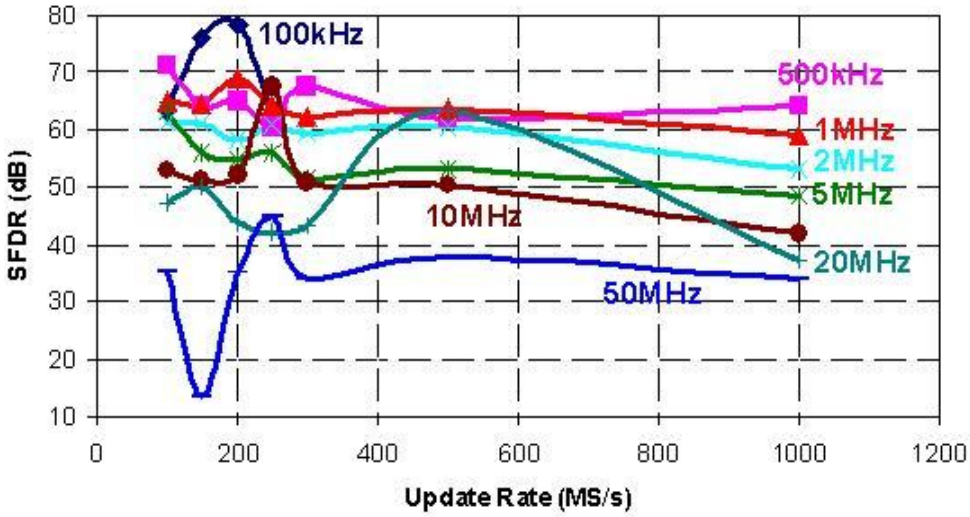

Figure 6.25 : SFDR as a function of the update rate.

The total power consumption of the 12-bit hybrid DAC is 104.4mW. All the simulations performed at different output signal frequencies have shown that power consumption is dominated by the DAC power consumption of the SRDs.

The output compliance voltage in order for DAC to maintain its linearity is approximately 2.05V which is in good agreement with the theoretical value calculated from (3.5) for 12-bit voltage-mode hybrid DAC.

The DAC has been implemented in a AMS 0.35µm CMOS technology and has an active area of only 0.076mm^2. Table 6.7 summarizes the characteristics of the DAC.

Table 6.7 : Performance summary of the 12-bit hybrid DAC.

Resolution	12-bit
Update rate@opt.	200MS/s
INL error	<0.9LSB
DNL error	<0.2LSB
SFDR (500kHz@100MS/s)	71.2dB
SFDR (1MHz@200MS/s)	68dB
SFDR (10MHz@250MS/s)	67.6dB
Settling time	14ns
Voltage compliance	~2.05V
Power consumption	104.4mW
Active area	0.076mm^2
Process	CMOS AMS 0.35µm

6.5.3 Comparison with the state of art

To compare the performance of the implemented 12-bit hybrid DAC with recently presented current-steering based DACs, the figure of merit shown in Section 2.2.4 is used. Performance parameters used are resolution, power consumption, active area and the input signal frequency where the SFDR has dropped with 6dB (1bit) i.e. expected value for the SFDR of a 12-bit DAC is 72dB while for analysis purposes SFDR of 66dB (1-bit loss) is acceptable [32].

Table 6.8 gives an overview of the comparison of this work to recently presented converters, with respect to the figure of merit. The area denoted in the table indicates the active area of the DAC (without bonding pads). The references where the active area of the chip is not available are not included in the FoM table. The update rate indicated in the table is the update rate where the DAC delivers the best SFDR and is not the maximum one. The f_{in} is the input signal frequency where SFDR has its maximal value. The reported power consumption is the maximum one.

According to the results it is clear that the implemented 12-bit hybrid DAC, mainly because of the small active area advantage over other converters, has a higher figure of merit. However, it must be noted that after the fabrication process the fabricated chip test results may be slightly different or may be deviated from the post-layout simulated results. Fabrication related errors are unavoidable and occur as a variation of the parameter values (W and L of the transistors) or as a mismatch between devices.

Table 6.8 : Comparison of FoM for different converters.

Reference	Process (μm)	Resolution (bit)	f_{in} (MHz)	Power (mW)	Area (mm^2)	FoM (MHz/mW*mm^2)
[12]@300MS/s	0.35	12	9	150	3.52	69.82
[15]@350MS/s	0.18	12	125	216	1.13	2097.67
[7]@1GS/s	0.35	10	490	110	0.35	13032.73
[22]@300MS/s	0.5	12	2	320	1.92	13.33
[49]@350MS/s	0.25	10	174	36	0.09	54992.59
[50]@2.704GS/s	0.13	6	520	28	0.76	1563.91
[23]@100MS/s	0.35	12	10	91	4.4	102.30
this work@100MS/s	0.35	12	0.5	104.4	0.076	258.12
this work@200MS/s	0.35	12	1	104.4	0.076	516.24
this work@250MS/s	0.35	12	10	104.4	0.076	5162.40

7. CONCLUSIONS AND RECOMMENDATIONS

This thesis demonstrates that the high-resolution current-steering DAC design can be sped up by selecting proper architecture, behavioral model and design strategy. By using the proposed hybrid architecture in implementation of the DAC, the complexity of the system is decreased, design time is reduced and good performance is achieved. The key point in the design is the required tradeoff between speed, resolution, area and power consumption in a given application. Any improvement performed in any part causes the degradation of another part in the system. Thus, according to the application's specs, the required performance metrics can be obtained in expense of aggravated less important performance metrics.

The efficiency of the applied methodology and the accuracy of the novel behavioral model are validated through the implementation of a 12-bit hybrid current-steering based DAC in a relatively cheap AMS 0.35μm CMOS process technology. Post-layout simulations are obtained using CADENCE Custom IC Design Tools and the performance characteristics of the DAC are investigated. The architecture and design methodology used for the implementation of the DAC offer advantages like design speed up and a small active area. Simulations indicate that the DAC has an accuracy of 12-bit and a static performance of INL and DNL better than 1LSB and 0.25LSB. The DAC operates with update rates up to 1GS/s. However, the best performance is achieved for 200MS/s update rate. At an update rate of 200MS/s the SFDR for signals up to 1MHz is higher than 70dB. Similarly at an update rate of 100MS/s the SFDR is higher than 64dB for signals up to 5MHz. Even for an update rate of 1GS/s the SFDR is higher than 64dB for sinusoidal input signal at 500kHz.

The proposed SDR and the dynamic latch used in the digital circuitry of the hybrid DAC support the small area requirement in expense of a moderate power consumption, mainly caused by the DC power consumption of the SRD.

The performance of the implemented DAC is compared with recently introduced DACs designed for different applications, through Figure of Merit (FoM). The FoM of the implemented hybrid DAC is better than recently presented DACs with different resolutions and implemented using various process technologies.

Thanks to small active area occupation, the implemented hybrid DAC is suitable for system on chip (SoC) applications. The proposed hybrid DAC supporting high update rates with good dynamic performance can be used as an alternative in various applications in industry including video, digital TV, cable modems etc.

In summary, the results obtained in this thesis show that there is still space to be explored and place for innovation in the current-steering DAC design area.

Recommendations for future research in this subject can be categorized in three main groups. Firstly, the power consumption can be further reduced without violating small area advantage. In the existing design this can be done by reducing the number of SRDs. Secondly, the mismatching between current sources and resistors can be improved through layout techniques. This will result in a better linearity and dynamic performance. Thirdly, the developed behavioral model can be extended to become more realistic by adding some nonlinearity properties to the current source and resistor counterparts in the model.

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APPENDICES

APPENDIX A : Mismatch Model
APPENDIX B : MATLAB codes for INL and DNL
APPENDIX C : Dynamic performance simulations' testbench and AHDL code for ideal ADC

APPENDIX A

In this appendix the mismatch between the parameters of equally designed MOS transistors is treated mathematically [45].

The variance of parameter ΔP between two rectangular devices is found to be:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \qquad \textbf{(A.1)}$$

Where A_P is the area proportionality constant for parameter P, while S_P describes the variation of parameter P with spacing. D_x denotes the spacing of both areas *(WL)* of rectangular devices along x axis.

Standard deviations of the threshold voltage V_T and device transconductance parameter β are derived by (A.1) as follows:

$$\sigma^2(V_T) = \frac{A_{VT}^2}{WL} + S_{VT}^2 D_x^2 \qquad \textbf{(A.2)}$$

$$\frac{\sigma^2(\beta)}{\beta^2} \approx \frac{A_\beta^2}{WL} + S_\beta^2 D_x^2 \qquad \textbf{(A.3)}$$

Where A_{VT}, A_β, S_{VT} and S_β are process related constants.

The standard deviation of the current of a MOS transistor pair (two equal designed devices biased in the same conditions) can be calculated using the mismatch data and can be given by

$$\frac{\sigma^2(I_D)}{I_D^2} = \frac{4\sigma^2(V_T)}{(V_{GS} - V_T)^2} + \frac{\sigma^2(\beta)}{\beta^2} \qquad \textbf{(A.4)}$$

APPENDIX B

In this appendix MATLAB codes developed for INL and DNL performance measurement are given below. The codes are based on the equations (2.2) and (2.3).

```
Lb=length(A);
i=1:Lb;
B(i)=A(i,2);
L=length(B);
inl(1)=0;
dnl(1)=0;
LSB=(max (B)-min (B))/L;
for t=2:L;
     inl(t)=(B(t)-(B(1)+(t-1)*LSB))/LSB;                    /* INL best-fit line*/
     dnl(t)=(B(t)-B(t-1)-LSB)/LSB;                          /*DNL*/
end
inl=inl';
dnl=dnl';
figure(1)
X=1:4092;
X=X';
plot(inl)
axis([0 4096 min(inl)*1.1 max(inl)*1.1]);
set(gca,'XTick',0:512:4096)
xlabel('DAC Input Code','FontSize',12,'FontWeight','Bold');
ylabel('INL (LSB)','FontSize',12,'FontWeight','Bold');
figure(2)
plot(dnl)
axis([0 4096 min(dnl)*1.1 max(dnl)*1.1]);
set(gca,'XTick',0:512:4096)
xlabel('DAC Input Code','FontSize',12,'FontWeight','Bold');
```

```
ylabel('DNL (LSB)','FontSize',12,'FontWeight','Bold');
```

APPENDIX C

In this appendix the testbench used for dynamic performance simulations of the DAC and the AHDL code of ideal ADC are given.

Figure C.1 shows the circuit used for generating signals to the DAC under test.

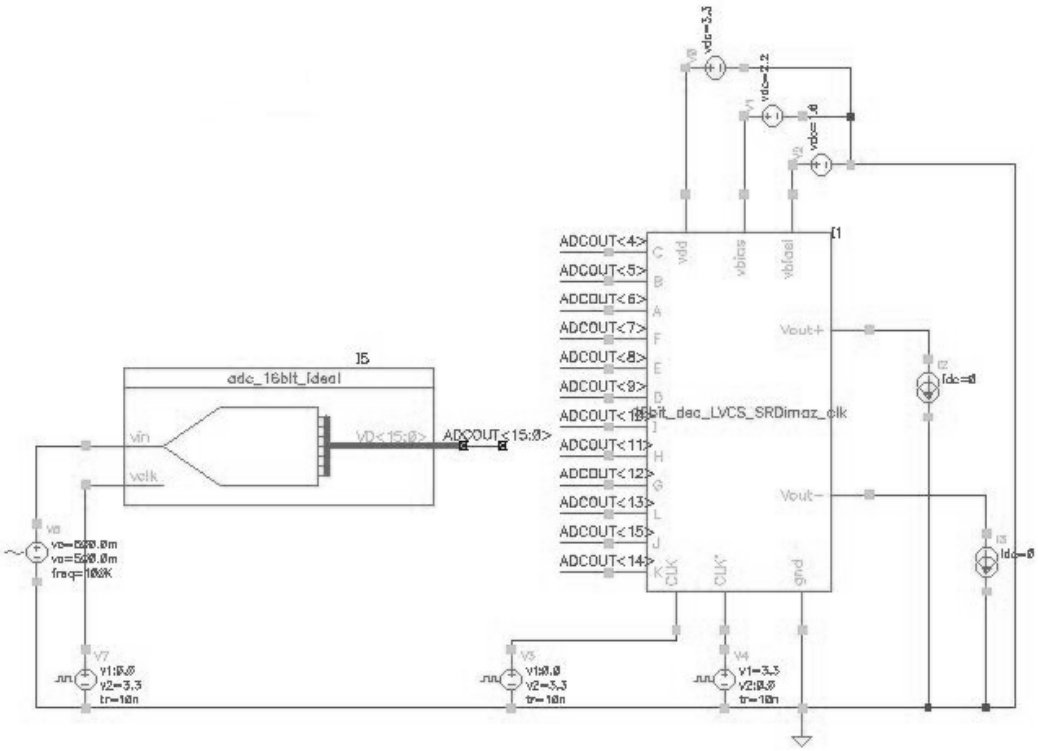

Figure C.1 : Testbench for dynamic performance simulations.

The AHDL code generated in the ITU VLSI Laboratory for the ideal ADC is given below.

```
// $Date: 1995/07/18 02:49:52 $
// $Revision: 1.1 $
//
//
//The sample SpectreHDL library is unsupported and subject to change
//without notice. Future versions of SpectreHDL may not be compatible
//with this library.

//--------------------
```

```
// adc_8bit_ideal
//
// -  Ideal 8 bit analog to digital converter
//
// vin:              [V,A]
// vclk: [V,A]
// vd0..vd7:      data output terminals  [V,A]
//
// INSTANCE parameters
//    tdel, trise, tfall = {usual} [s]
//    vlogic_high = [V]
//    vlogic_low  = [V]
//    vtrans_clk  = clk high to low transition voltage [V]
//    vref        = voltage that voltage is done with respect to [V]
//
// MODEL parameters
//    {none}
//
// This model is ideal in the sense that there is no mismatch modeled.
//

module adc_16bit_ideal(VD, vin, vclk)
  (trise, tfall, tdel, vlogic_high, vlogic_low, vtrans_clk, vref)
node [V, I] vin, vclk;
node [V, I] VD[15:0];
parameter real trise = 100p from (0:inf);
parameter real tfall = 100p from (0:inf);
parameter real tdel = 100p from [0:inf);
parameter real vlogic_high = 3.3;
parameter real vlogic_low  = 0;
parameter real vtrans_clk     = 1.65;
parameter real vref       = 1.0;
{

#define NUM_ADC_BITS     16
  real unconverted;
  real halfref = vref / 2;

  real vd[NUM_ADC_BITS];
  integer i;

  analog {
    if ($threshold(V(vclk) - vtrans_clk, 1.0)) {
      unconverted = V(vin);
      for (i = (NUM_ADC_BITS-1); i >= 0 ; i--) {
        vd[i] = 0;
        if (unconverted > halfref) {
          vd[i] = vlogic_high; unconverted -= halfref;
        } else {
```

```
            vd[i] = vlogic_low;
          }
          unconverted *= 2;
        }
      }
      //
      // assign the outputs
      //
      V(VD[15]) <- $transition( vd[15], tdel, trise, tfall );
      V(VD[14]) <- $transition( vd[14], tdel, trise, tfall );
      V(VD[13]) <- $transition( vd[13], tdel, trise, tfall );
      V(VD[12]) <- $transition( vd[12], tdel, trise, tfall );
      V(VD[11]) <- $transition( vd[11], tdel, trise, tfall );
      V(VD[10]) <- $transition( vd[10], tdel, trise, tfall );
      V(VD[9]) <- $transition( vd[9], tdel, trise, tfall );
      V(VD[8]) <- $transition( vd[8], tdel, trise, tfall );
      V(VD[7]) <- $transition( vd[7], tdel, trise, tfall );
      V(VD[6]) <- $transition( vd[6], tdel, trise, tfall );
      V(VD[5]) <- $transition( vd[5], tdel, trise, tfall );
      V(VD[4]) <- $transition( vd[4], tdel, trise, tfall );
      V(VD[3]) <- $transition( vd[3], tdel, trise, tfall );
      V(VD[2]) <- $transition( vd[2], tdel, trise, tfall );
      V(VD[1]) <- $transition( vd[1], tdel, trise, tfall );
      V(VD[0]) <- $transition( vd[0], tdel, trise, tfall );

#undef NUM_ADC_BITS
    }
}
```

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