ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

NEW POSSIBILITIES IN LOW-VOLTAGE ANALOG CIRCUIT DESIGN USING DTMOS TRANSISTORS

Ph.D. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

DTMOS KULLANAN DÜŞÜK GERİLİMLİ ANALOG DEVRE TASARIMINDA YENİ OLANAKLAR

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EYLÜL 2013

Atilla Uygur, a **Ph.D.** student of ITU **Graduate School of Science Engineering and Technology,** 504062201, successfully defended the **dissertation** entitled "**NEW POSSIBILITIES IN LOW-VOLTAGE ANALOG CIRCUIT DESIGN USING DTMOS TRANSISTORS**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Prof. Dr. Hakan KUNTMAN** Istanbul Technical University	.....
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Date of Submission : 28 June 2013
Date of Defense: 19 September 2013

To my family,

FOREWORD

This dissertation presents dynamic threshold voltage MOS (DTMOS) transistor-based ultra low-voltage, ultra low-power analog circuits. The proposed solutions are used in several circuit applications. The performances of the circuits are verified with simulation results.

I thank my advisor, my mentor Prof. Dr. Hakan Kuntman for his help and guidance throughout the study and throughout my career in my academic life. I acknowledge the help of Prof. Dr. Oğuzhan Çiçekoğlu and Doç. Dr. Nil Tarım for shedding light on several subjects about my study. I am grateful to Dr. Zafer İşcan for his friendship and EEG experiments.

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I hope this study would help researchers working on ultra-low voltage, ultra low-power analog circuits.

June 2013

Atilla UYGUR
(Research Assistant)

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ABBREVIATIONS

BCI	**:** Brain Computer Interface
BiCMOS	**:** Bipolar CMOS
BOX	**:** Buried Oxide
BSIM	**:** Berkeley Short-channel IGFET Model
CCII	**:** Second Generation Current Conveyor
CDTA	**:** Current Differencing Transconductance Amplifier
CMFB	**:** Common Mode Feedback
CMOS	**:** Complementary MOS
DIBL	**:** Drain-Induced Barrier Lowering
DTMOS	**:** Dynamic Threshold Voltage MOS
EEG	**:** Electroencephalogram
EKV	**:** Enz-Krummenacher-Vittoz
FBB	**:** Forward Body Bias
FET	**:** Field Effect Transistor
FinFET	**:** Fin-shaped FET
GBSOI	**:** Grounded Body SOI
GC-LPNP	**:** Gate-Controlled Lateral PNP
IGFET	**:** Insulated Gate FET
MOS	**:** Metal Oxide Semiconductor
OP-AMP	**:** Operational Amplifier
OTA	**:** Operational Transconductance Amplifier
SOI	**:** Silicon On Insulator
SPICE	**:** Simulation Program with Integrated Circuit Emphasis
SR	**:** Slew Rate
SSVEP	**:** Steady State Visually Evoked Potential
THD	**:** Total Harmonic Distortion
UGBW	**:** Unity Gain Bandwidth
VDTA	**:** Voltage Differencing Transconductance Amplifier

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B : Filter bandwidth
C_b : Depletion capacitance
C_{bd} : Body to drain capacitance
C_{bs} : Body to source capacitance
C_{gd} : Gate to drain capacitance
C_{gs} : Gate to source capacitance
C_{ov} : Overlap capacitance
C_{ox} : Oxide capacitance for unit area
D_n : Diffusion constant
f_c : Filter center frequency
f_o : Frequency of a transfer function zero
f_p : Filter pole frequency
g_d : Drain conductance
g_m : Gate transconductance
G_m : Active-block transconductance
g_{mb} : Body transconductance
H_0 : Filter gain factor
I_b : Tail bias current
I_{BJT} : Lateral BJT transistor current in DTMOS transistor
I_c : BJT transistor collector current
I_{CS} : Charge-Sheet model based MOS transistor current
I_d : MOS transistor drain current
I_{d0} : Weak inversion current parameter
i_o : Multiplier output current
k : Boltzmann's constant
l_c : Depletion region width of drain-body junction
L : MOS transistor channel length
L_D : Debye length
l_e : Depletion region width of source-body junction
n : Subthreshold swing coefficient
N_A : Acceptor atom concentration
n_i : Intrinsic carrier concentration
Q_b : Depletion region charge per unit area
Q_c : The charge under the oxide of transistor per unit area
Q_p : Filter quality factor
R_{bd} : Body-drain resistance
R_{body} : Body resistance
R_{bs} : Body-source resistance
R_{de} : Extrinsic parasitic drain resistance
R_{ge} : Extrinsic parasitic gate resistance
r_o : MOS transistor output resistance
R_{se} : Extrinsic parasitic source resistance

$\mathbf{S}$: Subthreshold swing
$\mathbf{T}$: Temperature in Kelvin
$\mathbf{t_{ox}}$: Oxide thickness
$\mathbf{U}$: Electrostatic potential normalized to thermal voltage
$\mathbf{U_d}$: Value of U at drain terminal
$\mathbf{U_f}$: Normalized Fermi level in the bulk
$\mathbf{U_s}$: Value of U at source terminal
$\mathbf{U_{surf}}$: Value of U at surface
$\mathbf{V_B}$: MOS transistor body voltage
$\mathbf{V_{BE}}$: Base emitter voltage
$\mathbf{V_{CE}}$: Collector emitter voltage
$\mathbf{V_D}$: MOS transistor drain voltage
$\mathbf{V_{DB}}$: MOS transistor drain to body voltage
$\mathbf{V_{FB}}$: MOS transistor flat band voltage
$\mathbf{V_G}$: MOS transistor gate voltage
$\mathbf{V_{gap}}$: Bandgap voltage
$\mathbf{V_{GB}}$: MOS transistor gate to body voltage
$\mathbf{V_{GS}}$: MOS transistor gate to source voltage
$\mathbf{V_S}$: MOS transistor source voltage
$\mathbf{V_{SB}}$: MOS transistor body bias voltage
$\mathbf{V_{TH}}$: MOS transistor threshold voltage
$\mathbf{V_{TO}}$: Zero bias MOS transistor threshold voltage
$\mathbf{v_x}$: Multiplier x terminal input voltage
$\mathbf{v_y}$: Multiplier y terminal input voltage
$\mathbf{W}$: MOS transistor channel width
$\mathbf{x_j}$: Depth of drain and source regions
$\mathbf{Z_{bd}}$: Body to drain junction impedance
$\mathbf{Z_{bs}}$: Body to source junction impedance
$\boldsymbol{\gamma}$: Body effect factor
$\boldsymbol{\varepsilon_{si}}$: Permittivity of silicon
$\boldsymbol{\kappa}$: Subthreshold gate coupling coefficient
$\boldsymbol{\mu}$: Effective surface mobility
$\boldsymbol{\mu_n}$: Mobility of electrons
$\boldsymbol{\xi}$: Shift in electron quasi-Fermi level
$\boldsymbol{\phi_{bl}}$: Barrier lowering voltage
$\boldsymbol{\phi_F}$: Fermi potential
$\boldsymbol{\phi_t}$: Thermal voltage
$\boldsymbol{\phi_0}$: Total surface band bending for MOS transistor
$\boldsymbol{\Phi_{GW}}$: Built-in voltage between the gate and well of DTMOS transistor
$\boldsymbol{\Phi_{MS}}$: Work function difference potential
$\boldsymbol{\Psi_s}$: Surface potential
$\boldsymbol{\Psi_{sa}}$: Surface potential when there is no inversion layer
$\boldsymbol{\omega_p}$: Filter angular pole frequency

NEW POSSIBILITIES IN LOW-VOLTAGE ANALOG CIRCUIT DESIGN USING DTMOS TRANSISTORS

SUMMARY

Analog circuit design has evolved significantly during the last years because of continuously decreasing supply voltages of integrated circuits. This situation has brought the necessity of designing low-voltage and low-power analog designs. Conventional circuit techniques have become inefficient with the booming of portable devices. So far, many novel low-power and low-voltage designs have been presented in the literature. It seems that this trend will continue in the future with more performance demanding circuits operating under very stringent power specifications. Thus the need for ultra low-voltage and ultra low power analog circuit designs are inevitable.

Dynamic threshold voltage MOS (DTMOS) transistor has the capability to operate under reduced supply voltage with proper configuration of forward body biasing. Under some limitations, bulk-DTMOS technique can be applied to cheap standard CMOS fabrication process without additional processing steps. Therefore, this study focuses on new possibilities of bulk-DTMOS usage in ultra-low voltage, ultra low-power analog circuits. The results here, can also be applied to silicon on insulator (SOI) DTMOS circuits which is generally the more preferred process technology for DTMOS fabrication because of the reduced parasitics, however, with an increased fabrication cost. Additionally, twin or triple-well process technologies can also be used to increase the performance of the proposed circuits here. Since these process technologies are more expensive than the standard CMOS process, these alternatives are discarded from the scope of this dissertation.

In this study, DTMOS approach to the design of ultra low-voltage and ultra low-power analog circuits, has been successfully applied to the circuits ranging from EEG circuits, speech processing filters in hearing aids, multipliers, analog active building block designs: OTA, OP-AMP, CCII to MOS-only circuits.

The wide range of applications presented here share the common feature of capability to operate under ultra low supply voltage with very low power consumption to meet the requirements of today's power-efficient systems. Proposed circuit solutions are simulated using analog circuit simulator SPICE and MATLAB program is additionally used for some data processing and graphing purposes.

It is found that in designing ultra low-voltage, ultra low power analog circuits, DTMOS approach is a viable alternative due to its inherent characteristic of effective low threshold voltage behaviour under forward body bias. In addition to its conventional usage in digital applications, this approach can also be applied to several analog application subjects with acceptable performance under even ultra low supply voltages.

DTMOS KULLANAN DÜŞÜK GERİLİMLİ ANALOG DEVRE TASARIMINDA YENİ OLANAKLAR

ÖZET

Tümdevrelerin sürekli azalan besleme gerilimleri neticesinde analog devre tasarımı son yıllarda önemli ölçüde değişime uğramıştır. Bu durum düşük gerilimli, düşük güç tüketimli devre tasarımı ihtiyacını doğurmuştur. Taşınabilir cihazların ani artışı sonucu bilinen devre teknikleri günümüzde yetersiz kalmıştır. Özellikle, her geçen gün sayısal devrelerin aynı kırmık üzerinde daha çok sayıda transistor içermesi ve buna bağlı olarak tümdevre yoğunluklarının arttırılması transistor boyutlarda küçülmeye neden olmuştur. Küçülen boyutla birlikte üretilen transistorun düzgün çalışabileceği besleme gerilimleri de düşmeye zorlanmıştır. Bazı özel üretim teknikleri ile bu durum belli ölçüde aşılabilse bile göreceli olarak yüksek gerilim kullanımı, karesel orantılı bir şekilde sayısal devrelerde dinamik güç tüketimini arttırdığından bu yöntem özel uygulamalar haricinde sıklıkla tercih edilen bir yol olmamaktadır.

Bugüne kadar çok sayıda yeni, düşük güç tüketimli, düşük gerilimli sayısal ve analog tasarım literatürde sunulmuştur. Elektronik devrelerdeki küçülmeye paralel olarak bu eğilimin ilerde daha da artarak devam edeceği düşünülebilir. Gelecekte günümüzdeki alternatiflerine göre hem daha fazla performanslı olarak çalışan hem de güç tüketimi bakımından çok daha verimli olan devrelerin yaygın olarak kullanılacağı, bugüne kadar olan sayısal ve analog elektronik devrelerin izlediği süreçle kıyaslandığında net olarak anlaşılır. Bu yüzden çok düşük güç tüketimli ve çok düşük besleme gerilimli devre tasarımlarına olan ihtiyaç, bugün de olduğu gibi gelecekte de kaçınılmaz olarak varlığını devam ettirecektir.

Analog devrelerde besleme gerilimleri düştükçe transistorların çalışma şartları zorlanmakta hatta bazı durumlarda hiç çalışamamaktadırlar. Ayrıca, her ne kadar düşük besleme gerilimleri güç tüketimini düşürse de bu durum analog devrelerde önemli ölçüde performans kayıplarına neden olmaktadır. Bu sorunun aşılması için analog devre tasarımında yeni yaklaşımların bulunmasına ihtiyaç vardır. Bu nedenle bu konu üzerine hem sistem hem devre hem de eleman temelli yapılan çalışmalar günümüz analog devre tasarımı araştırmalarında çok önemli bir yer edinmiş olup bundan sonra da yoğunlaşarak önemini sürdürmeye devam edecektir.

Dinamik eşik gerilimli MOS (DTMOS) transistor, ileri yönde gövde kutuplaması belirli şartlara bağlı olarak doğru şekilde yapıldığında, düşük besleme gerilimlerinde yüksek başarımlı olarak çalışabilmektedir. DTMOS transistor MOS tekniğinde gövdenin geçide bağlanması sonucu elde edilen ve gövde kaynak jonksiyonunun ileri yönde kutuplanması durumunda düşük gerilimli olarak işlev görme prensibine göre çalışan bir eleman olmaktadır. Bu durum MOS teknolojisinde transistorun eşik gerilimi seviyesinin matematiksel ifadesinin gövde kaynak gerilimine bağlı olarak değişmesinden kaynaklanmaktadır. Buna göre bir DTMOS gövde kaynak gerilimi değişiminde, geçidi gövdesine bağlı olduğu için dinamik bir karakteristiğe sahip bir eleman olarak algılanılabilir. Ayrıca normal MOS transistora göre daha yüksek geçiş

iletkenliği göstermesinden dolayı daha düşük besleme gerilimlerinde daha yüksek akım akıtarak günümüzün düşük güç tüketimli, düşük gerilimli analog devreleri için de kullanışlı bir eleman olmaktadır. Literatürde ilk olarak sayısal devrelerde düşük besleme gerilimlerinde güç tasarrufu sağlarken aynı zamanda da kaçak akımının düşük olması nedeniyle önerilmiştir. Bir diğer taraftan da düşük besleme gerilimli analog devrelerde yüksek geçiş iletkenliği göstermesi sonucu devrelerin performansını arttırmakta ve düşük besleme gerilimli analog devre tasarımları için de uygun olmaktadır.

Bu transistora ait bir diğer özellik de eşik altında çalıştırıldığında DTMOS transistorun ideale çok yakın bir eşik altı salınımı göstermesidir. Normal bir MOS transistora göre eşik altı çalışmada sahip olduğu bu karakteristik sayesinde DTMOS transistor, eşik altında çalışan çok düşük güç tüketimli devre tasarımları için de uygun bir eleman olarak karşımıza çıkmaktadır.

Belirli kısıtlamalar altında, DTMOS tekniği fazladan üretim adımı gerektirmeden ucuz standart CMOS üretim sürecine uygulanabilmektedir. Bu yüzden, bu çalışmada çok düşük gerilimli, çok düşük güç tüketimli tasarımlarda standart CMOS proseslerde üretilebilecek DTMOS ele alınmış ve bu yaklaşıma bağlı olarak DTMOS kullanımında yeni olanaklar üzerine yoğunlaşılmıştır. Burada elde edilen sonuçlar DTMOS üretiminde daha düşük parazitikleri nedeniyle daha çok tercih edilen yalıtkan üzeri silikon (SOI) DTMOS devrelere de uygulanabilmekte fakat bu proses kullanıldığında elde edilen devrelerin üretim maliyeti artmaktadır. Ek olarak çift ya da üçlü kuyulu üretim teknolojileri kullanılarak burada önerilen devrelerin performansı arttırılabilir. Bu üretim teknolojileri, standart CMOS prosese göre daha pahalı olduğundan bu çalışmanın kapsamı dışında tutulmuştur.

DTMOS transistorun çalışmasında ortaya çıkabilecek en büyük sakınca, kutuplama gerilimleri aşırı olduğunda ileri yönde kutuplanan kaynak gövde, savak gövde jonksiyonlarının diyot gerilimi seviyesini geçerek çok yüksek akımlar akıtması ve transistorun çalışma prensibini bozması olmaktadır. Bunun engellenebilmesi için önerilebilecek ilk yöntem, bu jonksiyonlar üzerine düşen gerilimi sınırlandırmak olmaktadır. Bu konuda yapılan çalışmalarda yaklaşık olarak 0.4V~0.5V civarındaki seçilen ileri yönde kutuplanmış pn jonksiyon gerilim seviyelerinin transistorun normal çalışma karakteristiğini etkilemediği bulunmuştur. Bu şartlar altında standart MOS transistor için kullanılan kompakt BSIM, EKV gibi yaygın modeller ile uzun kanallı DTMOS transistorlar modellenebilmekte ve devre tasarımlarında iyi bir yaklaşıklıkla kullanılabilmektedir. Bu nedenle bu çalışmada DTMOS transistorlar uzun kanallı seçilmiş olup modellemelerinde de devre tasarımlarında yaygın olarak kullanılan ve pek çok devre simülatörü tarafından yaygın bir şekilde desteklenen endüstri standardı BSIM kullanılmıştır.

Bu çalışmada DTMOS temelli çok düşük besleme gerilimlerinde çalışan çok düşük güç tüketimli devreler önerilmiş ve bu önerilen devrelerin analog devre tasarımının çeşitli uygulama alanlarında başarıyla uygulanabileceği gösterilmiştir. Tasarlanan devreler arasında OTA, OP-AMP, CCII gibi yaygın olarak kullanılan analog aktif yapı blokları, çarpıcı devresi, yüksek frekanslı uygulamalarda etkinliği gösterilmiş sadece-MOS yapılar gibi devreler bulunmaktadır.

Bu çalışmada tasarlanan devrelerin başarımı çeşitli uygulama devreleriyle gösterilmiştir. Yapılan uygulamalar arasında kablosuz EEG cihazlarında kullanılabilecek filtre yapıları, DTMOS tekniği kullanılarak gerçekleştirilen sadece MOS devresine ait üçüncü dereceden Butterworth karakteristiği veren bir yüksek frekans filtresi ve analog duyma cihazlarında kullanılmaya müsait, ses işareti işleye-

bilen çok düşük güç tüketimli ve çok düşük besleme gerilimli devreler bulunmaktadır.

Burada sunulan çok çeşitli uygulama alanlarının ortak olarak paylaştıkları gücü verimli kullanma özelliğine ek olarak, düşük besleme gerilimlerinde analog devrelerin karşılaştığı sorunlara yeni ve kompakt çözümler getirmektedirler. Önerilen devrelerin başarımlarını göstermek amacıyla SPICE analog devre tasarım programı ile benzetimleri yapılmış ek olarak veri işlenmesi ve grafiklerde de MATLAB programından faydalanılmıştır.

İleri yönde gövde kutuplamaya bağlı olarak DTMOS transistorun yapısından kaynaklanan, efektif olarak düşük eşik gerilimli çalışma özelliği nedeniyle, çok düşük güç tüketimli ve çok düşük gerilimli devrelerde DTMOS yaklaşımının geçerli bir alternatif olduğu bu çalışmayla gösterilmiştir. Sayısal devrelerde bilinen uygulamalarına ek olarak DTMOS yaklaşımı geniş bir alanda çeşitlilik gösteren analog devre yapılarında da çok düşük besleme gerilimlerinde bile kabul edilebilir bir performansla kullanılabileceği bulunmuştur.

1. INTRODUCTION

The demand for portable applications has continuously increased during the last years. The usage of smart phones, tablet computers, netbooks and several other wireless devices has grown dramatically which brings about the requirement for more advanced power-aware design techniques.

The trend of improving the power efficiency of CMOS circuits has first lead to reduced supply voltage levels of digital circuits for lower power consumption which is proportional to the square of the used supply voltage. Therefore, this approach has also arisen the necessity to design analog circuits that are capable of operating under very low supply voltage levels of digital circuitry in the same chip. Sharing very low supply voltages with digital circuits, however, severely limits the performance of analog circuits.

Until now, generally in digital circuits, decreasing supply voltage levels for transistors having thinner gate oxides has been utilized as a solution to lower the power consumption and increasing chip density by laying out more transistors on a smaller chip area. However, further decreasing the channel lengths has created leakage current problems. Moreover, threshold voltages cannot be kept below certain limits to minimize the leakages in the chip.

There is a strong need for new ideas and perspectives to analog circuit design to meet the requirements of modern highly power-efficient electronic devices. Conventional analog circuits suffer from very low supply voltages of digital circuits and relatively high threshold voltage levels to prevent large leakage currents in standard CMOS process technology [1-2].

As a solution to the problems of conventional circuits, DTMOS, dynamic threshold voltage MOS, was presented by Assederaghi et al. in [3-4] which operates as a low-leakage as well as low-voltage, low-power device for digital circuits.

1.1 DTMOS Transistor

In 1994, DTMOS transistor was proposed by Assederaghi et al, in their pioneering paper [4] for silicon on insulator (SOI) process technology. Although the idea goes back to earlier dates [5], this paper best describes the device and the underlying reasons of the operation. As shown in Figure 1.1 the idea is to connect the gate and body of a transistor to dynamically change its threshold voltage by utilizing the relation in (1.1) where ϕ_0 is the total surface band bending, γ body effect factor, V_{TO} is the zero bias threshold voltage. The equation is written for a long channel n-MOS transistor where drain-induced barrier lowering (DIBL) effect is neglected.

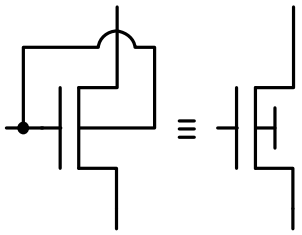


Figure 1.1 : DTMOS transistor and its commonly used circuit symbol.

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right) \tag{1.1}$$

and zero bias threshold voltage V_{TO} is defined by

$$V_{TO} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0} \tag{1.2}$$

V_{FB} is the flat band voltage and γ is the body effect factor. It is given by

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \tag{1.3}$$

N_A is the substrate doping, ε_{si} represents dielectric permittivity of silicon, C_{ox} is the oxide capacitance for unit area. ϕ_0 in (1.1) is usually considered equal to two times of Fermi potential, $2\phi_F$, for simplicity. However, to obtain more accurate approximations, this should be calculated as in (1.4) where α is an experimental fitting parameter and ϕ_t is the thermal voltage [6-7].

$$\phi_0 = 2\phi_F + \alpha\phi_t \tag{1.4}$$

For conventional n-MOS operation V_{SB} value is either zero or positive whereas in DTMOS operation this value might become negative, however, the equation in (1.1)

is still applicable for not too large negative values provided that the junction currents are negligibly small [6-7].

The DTMOS configuration does not require any additional processing steps in fabrication and it is made as shown in Figure 1.2 for a SOI process by connecting the gate and the body of the transistor using a metal contact.

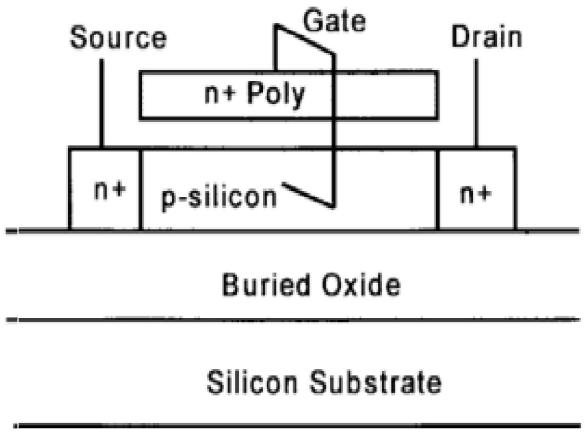


Figure 1.2 : SOI NMOS transistor connected in DTMOS configuration [4].

From Figure 1.2, it is seen that there is a lateral bipolar transistor consisting of two source body and drain body junctions which might latch up and cause very high body currents. This should be strictly kept under control for correct mechanism of the device. The possibility of very high forward biased source body and drain body diode currents is the main problem of such a connection. For this reason, as recommended in the original paper [4], DTMOS with its plain structure is not usable for supply voltages over 0.6V. Although it is possible to use it with an addition of an extra limiter transistor, this will almost double chip area for digital circuits and increases parasitic effects. Additionally, the operation of all chip components strongly depends on those limiter transistors which decrease robust operation performance and failure-safety because any high on diode currents totally disrupts transistor operation. For those reasons throughout this study supply voltages are chosen low enough (0.4V~0.5V) to limit forward biased diode currents. It is practically shown in circuit realizations that forward biased diode currents do not effect much the operation of the transistor or the overall circuit if the supply voltages, in other words, forward body biases are close to 0.4V~0.5V [8-9]. The main reason is that the mobile carrier concentrations for supply voltages in 0.4V~0.5V range do

not reach high levels in modern highly doped substrates leading to source body, drain body junctions with high turn-on voltages [6].

DTMOS transistor, under the same V_{GS} voltage behaves as a high-transconductance MOSFET. In Figure 1.3, it is depicted that a p-type DTMOS conducts more current than a regular MOSFET when V_{DS} kept at -0.1V constant voltage while V_{GS} is swept from -0.4V to 0V. The reason behind this mechanism is the threshold voltage reduction due to the positive source body voltage. Additionally, due to the forward biasing, vertical electric field in the channel decreases which improves carrier mobility and increases current drive [3].

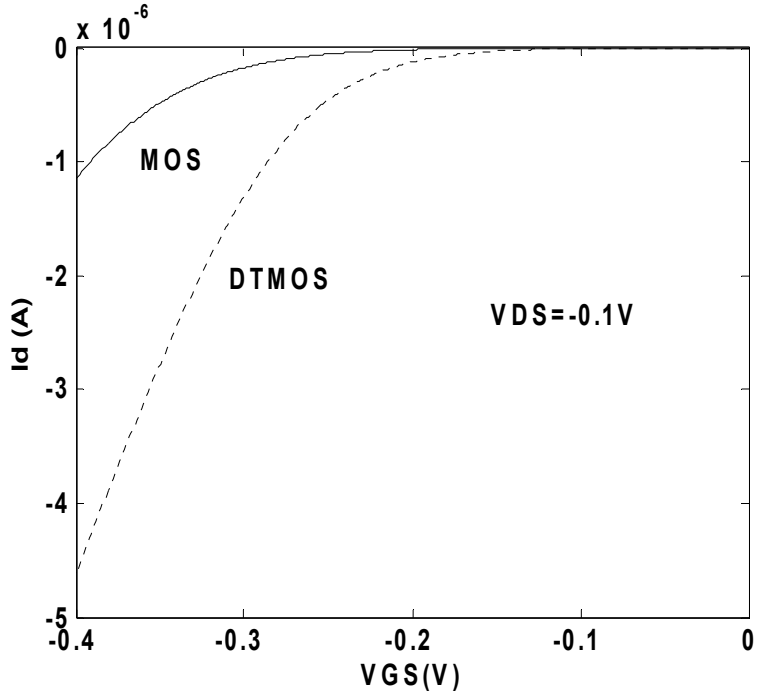


Figure 1.3 : The current change of DTMOS and MOS transistors versus V_{GS}.

The phenomenon makes DTMOS transistor a promising element in low voltage circuits where higher currents can be obtained in comparison to conventional MOS transistors.

Subthreshold mode of operation of CMOS circuit is usually the preferred method for power-saving circuits if the high frequency operation is not needed. This is mostly the chosen mode of operation throughout this study where ultra low voltage, ultra low power designs are generally focused.

In this operation mode, current flow is due to the diffusion current and the current relation becomes no longer proportional to square root of the applied voltage but

exponential as described by a rough model in equation (1.5) where n and I_{d0} can be experimentally determined [10-11]. Differentiating (1.5) gives transconductance in weak inversion as in (1.6) which shows an important result that the transconductance in weak inversion is directly proportional to the current which is similar to bipolar transistor characteristic. The reason is the current mechanism in both is caused mainly by diffusion. In weak inversion, another important point that should be mentioned is that the transconductance to current ratio is the highest in this mode of operation [12].

$$I_d = \frac{W}{L} I_{d0} e^{qV_{GS}/nkT} \tag{1.5}$$

$$g_m = \frac{q}{nkT} I_d \tag{1.6}$$

Weak inversion and strong inversion models can be compared graphically as in Figure 1.4. The slope in this figure is called as subthreshold slope which determines how well a transistor turns off according to the decrease in V_{GS} for digital circuits. The inverse of this is the subthreshold swing (1.7) which is a very important parameter showing the amount of V_{GS} that should be decreased for the weak inversion current to reduce one order of magnitude [6]. Subthreshold swing can be approximately calculated by the equation in (1.8).

$$S = \left(\frac{\partial \log I_d}{\partial V_{GS}} \right)^{-1} \tag{1.7}$$

$$S = 2.3 \frac{nkT}{q} \tag{1.8}$$

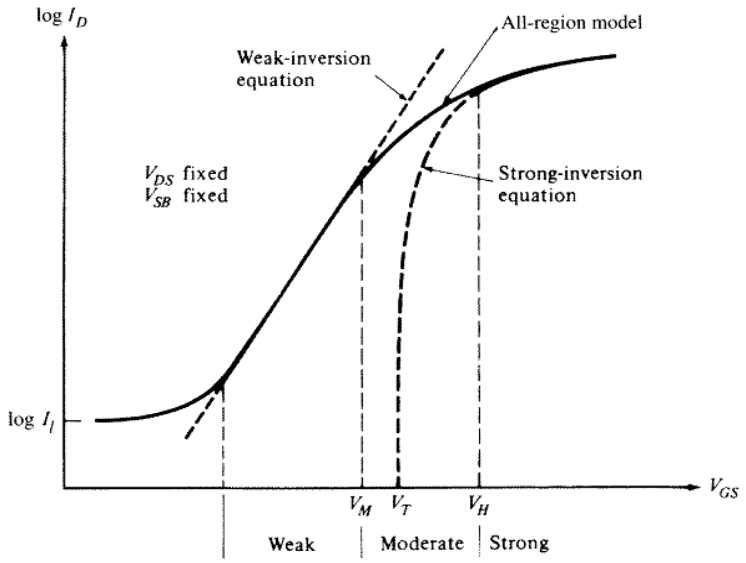


Figure 1.4 : Graphical comparison of weak and strong inversion models [6].

The subthreshold swing equation in (1.8) is just an approximation and it gives roughly 60mV/dec value for the ideal case when n is equal to unity. The real value for MOS transistors deviates from the approximation and it can be defined more accurately in a body referenced model as [6]

$$I_d = \frac{W}{L} I' \left(e^{-V_{SB}/\phi_t} - e^{-V_{DB}/\phi_t} \right) \tag{1.9}$$

and *I'* is defined by

$$I' = \mu \frac{\sqrt{2q\varepsilon_{si}N_A}}{2\sqrt{\psi_{sa}(V_{GB})}} \phi_t^2 e^{[\Psi_{sa}(V_{GB})-2\phi_F]/\phi_t} \tag{1.10}$$

In (1.10), we made an assumption that surface potential $\Psi_s \cong \Psi_{sa}$ which is the surface potential when there is no inversion layer and it is described by the equation in (1.11).

$$\psi_{sa}(V_{GB}) = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}} \right)^2 \tag{1.11}$$

Surface potential satisfies the following equation in (1.12) where Q_c is the charge under the oxide of the transistor per unit area and is a function of surface potential. With the absence of inversion layer this charge consists of only depletion region

charge per unit area Q_b. This charge is related with the depletion capacitance according to equation (1.13).

$$V_{GB} = V_{FB} + \psi_s - \frac{Q_c(\psi_s)}{C_{ox}} \tag{1.12}$$

$$C_b = -\frac{dQ_b}{d\psi_s} \tag{1.13}$$

In equation (1.8) parameter n shows the inverse of the change of surface potential with respect to V_{GB} voltage. This parameter can be defined using (1.12) and (1.13) by the capacitances in (1.14) where the capacitance coming from interface traps are neglected and C_b shows the depletion region capacitance for unit area.

$$n = \left(\frac{\partial \Psi_s}{\partial V_{GB}} \right)^{-1} = 1 + \frac{C_b}{C_{ox}} \tag{1.14}$$

So equation (1.8), subthreshold swing for a MOS transistor, can be rewritten as

$$S = 2.3 \frac{kT}{q} \left(1 + \frac{C_b}{C_{ox}} \right) \tag{1.15}$$

For a DTMOS transistor, since gate to body is connected, the equation in (1.14) becomes equal to unity which means that the equation (1.8) transforms to the ideal case shown in (1.16), however it should be pointed out that the equation in (1.8) is an approximation. Nevertheless, this result is also verified experimentally for long channel DTMOS transistors with channel lengths greater than 0.4μm showing nearly 60mV/dec subthreshold swing [13].

$$S = 2.3 \frac{kT}{q} \tag{1.16}$$

That means DTMOS transistors with high on-off ratio has better drivability than a regular MOS transistor under low voltage operation, which makes them suitable devices for low power, low voltage operations, where transistors are usually operating in weak inversion region. Figure 1.5 shows the subthreshold characteristics of a regular MOS and a DTMOS device fabricated in SOI process.

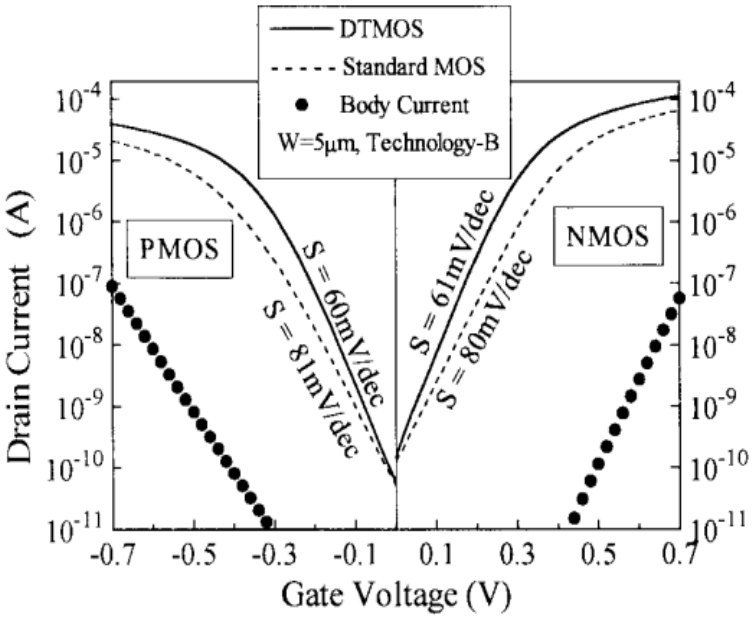


Figure 1.5 : The subthreshold swings of MOS and DTMOS transistors [3].

1.2 Model of DTMOS Transistor

In the design of analog circuits, correct modeling of semiconductor devices plays a crucially important role for the accuracy of simulations. Therefore, a critical question might arise that if the conventional MOSFET models are sufficient for proper modelling of the operation the DTMOS transistor. Actually, mostly used MOSFET models such as BSIM, EKV were developed under the assumption that the channel is free of mobile carriers, which is the total depletion approximation. However, for a DTMOS transistor, this is not true because there are mobile carriers and total depletion approximation is not valid now. Additionally, vertical forward biased drain body and source body junction currents add another dimension and this might require two dimensional device models. However, these complicated modeling efforts are not necessary if the supply voltage is kept below 0.4V~0.5V voltage levels and the channel length of the device is not chosen very small to prevent short channel effects. According to both mathematical analyses and real life experiments, conventional models are still applicable to DTMOS transistor with good accuracy to model the device and the related circuits provided that the mentioned specifications exist [7, 14]. Therefore, we have mainly used 0.4V supply voltage for DTMOS designs and transistors with minimum channel lengths 2μm in our designs to be in agreement with results and compact models experimentally proven in [15].

Although there are some bulk-based DTMOS modeling efforts [16-17], silicon on insulator (SOI) technology is the usually preferred process technology for fabrication of DTMOS transistors. In SOI technology, due to the isolation of body using an insulating buried oxide (BOX) layer, the parasitics become reduced [18]. As shown in Figure 1.6, the parasitic junction capacitances of a bulk MOS device become MOS capacitor in SOI technology where the parasitics are smaller comparing to its bulk alternative [19]. Therefore, modelling efforts in the literature have focused more on SOI DTMOS devices. Nevertheless, results from these studies, in some degree, can also be applied to bulk DTMOS with taking account the increased parasitics of their bulk counterparts.

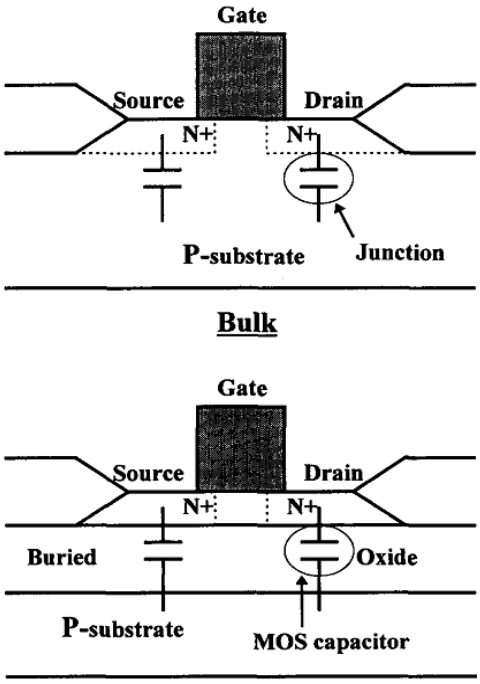


Figure 1.6 : SOI and bulk technology parasitic capacitances [18].

There are different approaches in the literature to model the device. In some of early studies, a similar idea to DTMOS approach was realized as a gate-controlled lateral bipolar transistor (GC-LPNP) with four electrodes that are collector, base, emitter and gate [20]. The transistor in this study was fabricated using BiCMOS process technology as a bulk lateral pnp transistor parallel with a surface p-MOSFET. Then the total collector current of the device becomes the total BJT and MOSFET currents as in (1.17). In DTMOS operation, for very low supply voltages in the range 0.4V the base current (body current of MOS) becomes so small that it can be neglected comparing to the MOS current. This approximation can be verified by measurement

results from [16] where V_{gb}=0 is considered for DTMOS operation as depicted in Figure 1.7.

$$I_c = I_{c(lateral\ pnp)} + I_{d(pmos)} \tag{1.17}$$

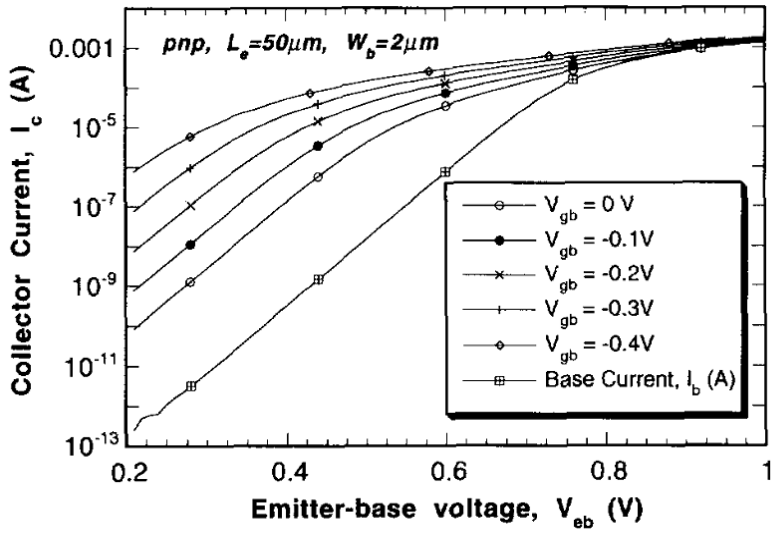


Figure 1.7 : Collector and base current for gated lateral bipolar transistor [16].

Similar idea to the work in [20] was also applied to an earlier study [5] as voltage controlled bipolar device in a SOI process where the performance increase was attributed to the bipolar transistor's current added over the MOS current, however, main reason was the threshold decrease as shown later by Assederaghi et al in their paper [3]. In addition to past studies, DTMOS operation principal has also been studied in newer, advanced devices, triple-gate FinFETs [21].

Another past study was explained in [22] which pointed out the current increase due to the forward biased source-substrate junction and tried to model the threshold decrease of bipolar induced breakdown mechanics in MOSFETs. However, this study lacks sufficient physical interpretations and utilized several empirical parameters.

Later, the modeling ideas of gated-lateral BJTs in [20] were explicitly applied to DTMOS transistor in the study [23] where the authors used a modified Pao-Sah model. Here we skip the details of the model not to lose the integrity of the subject except the resulting current definition in (1.18).

$$I_d = qD_n L_D n_i \frac{W}{L} \int_{U_S}^{U_D} \int_{U_j}^{U_{surf}} \frac{e^{U-\xi-U_f} - e^{-\xi-U_f}}{F(U,\xi,U_f)} dU\, d\xi + qD_n n_{p0} \frac{W}{L} x_j \left(e^{-U_S} - e^{-U_D}\right) \tag{1.18}$$

where n_i is the intrinsic carrier concentration and ξ is the shift in electron quasi-Fermi level. U shows electrostatic potential normalized to kT/q. D_n is the diffusion constant. U_{surf} is the value of U at x=0 , U_D and U_S show voltage values of drain and source to the bulk in units of kT/q. U_f is the Fermi level in the bulk. x_j is the depth of drain and source regions in the bulk. U_j is potential at x_j. $F(U,\xi,U_f)$ is the function of normalized electric field which is found by the solution from Poisson equation. L_D is the Debye length in and it is defined by

$$L_D = \sqrt{kT\varepsilon_{si}/2q^2 n_i} \tag{1.19}$$

The first term in equation (1.18) represents the current from conventional charge sheet model of MOS and second term comes from the lateral BJT current. Therefore, (1.18) can be rewritten as (1.20). Identical result (1.17) was proposed by [20] after real measurement results. The drain current of the model in (1.18) is given in Figure 1.8 where Joarder curve represents the model in [16]. It is necessary to note that this model does not include short-channel effects so it is valid for long channel DTMOS devices.

$$I_d = I_{CS} + I_{BJT} \tag{1.20}$$

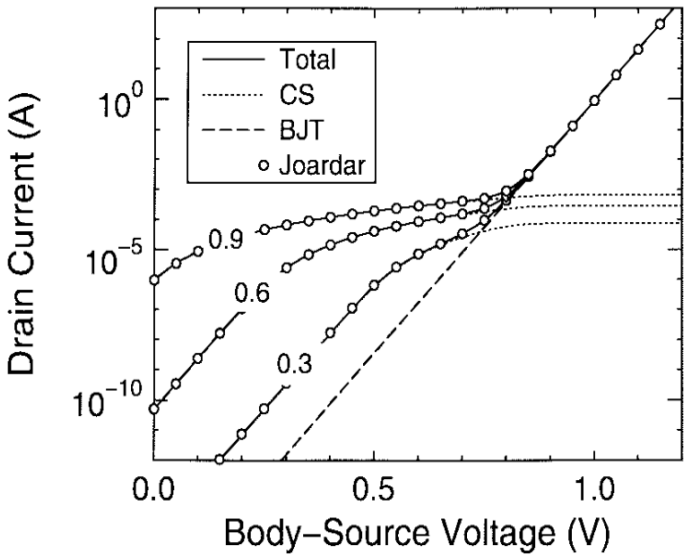


Figure 1.8 : Drain current to body-source voltage for three values of V_{GD} [23].

A comprehensive study for SOI DTMOS transistors including both short channel effects and two dimensional Poisson equation was proposed in [24]. This model is the improved version of [25] which adds support for short channel DTMOS

transistors. Since the model equations and its derivation require much space, here we have preferred to give just the subthreshold current relation (1.21). This is the mostly-used operation region of transistors in the proposed circuits in this dissertation.

$$I_d = -\frac{q\mu W \phi_t n_i \exp\left(\frac{\Psi_{s\min} - \phi_F + V_{BE}}{\phi_t}\right)}{L - l_e - l_c}\left[\frac{\phi_t}{\overline{E}_s}\left(1 - \exp\left(-\frac{V_{CE}}{\phi_t}\right)\right)\right] \qquad \textbf{(1.21)}$$

$\Psi_{s\,min}$ shows minimum surface potential, ϕ_F is the bulk Fermi potential. l_e and l_c are the depletion region width of the source-body and drain body junctions. $\overline{E}_s$ shows the average surface electric field which is roughly calculated by (1.22). Others have their usual meaning.

$$\overline{E}_s = \frac{E_{se} + E_{sc}}{2} = \frac{C_{ox}}{\varepsilon_{si}}\left(V_{GB} - V_{FB} - \frac{1}{2}\left(\Psi_{se} + \Psi_{sc}\right)\right) \qquad \textbf{(1.22)}$$

In (1.22), Ψ_{se} and Ψ_{sc} show the surface potential at the depletion region edge of source-body and drain-body junctions respectively. Similarly, E_{se} and E_{sc} are the electric fields at the source and the drain. To investigate the validity of this model, simulations and real measurements were done in [24]. Figure 1.9 shows the drain current according to gate voltage for SOI DTMOS device. Simulated data comes from device simulator PISCES and circles show the model which is in close agreement with simulations.

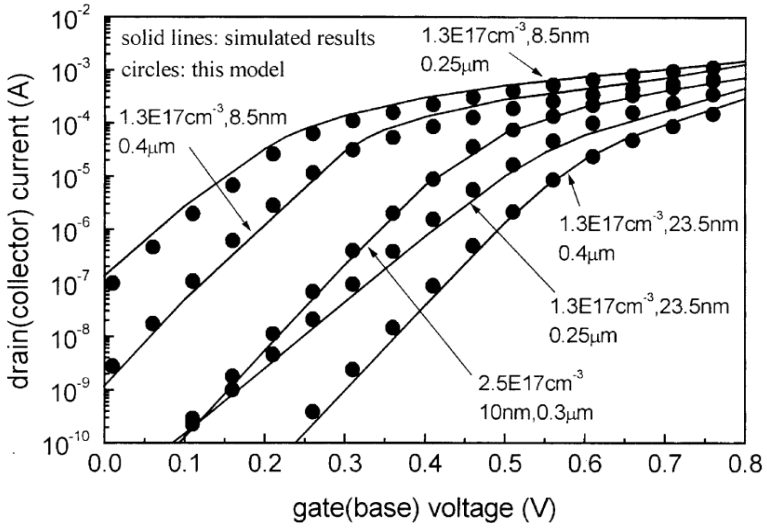


Figure 1.9 : Drain current to gate voltage for different device parameters [24].

Figure 1.10 shows the comparison of the model with real measurements of DTMOS transistor fabricated in SOI process with a channel length 0.4μm.

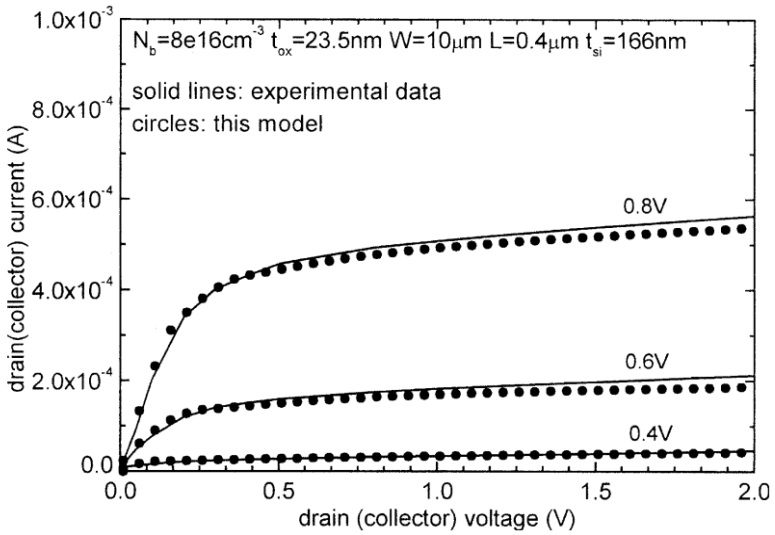


Figure 1.10 : Drain current to drain voltage for measurements and the model [24].

Models presented so far are taking into account several features of DTMOS for better modeling and accurate simulation. However, some of those models require the consumption of much computer resources when large circuits are built with several transistors. Moreover, the models should be added to simulators such as SPICE for simulation of circuits. Fortunately, available compact models such as EKV, BSIM are still valid under some limitations which were mentioned at start of this section. Validity of EKV model for SOI DTMOS transistors is shown in [26]. Without modifying the EKV model [27] it can be used just connecting body and gate of a transistor if the device has long channel and supply voltage is lower than 0.5V. Therefore, current relation of this model can be used which is given by (1.23).

$$I_d = 2n\mu_n C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 \times \left[\left(\ln\left[1+\exp\left(\frac{V_P - V_S}{2kT/q}\right)\right]\right)^2 - \left(\ln\left[1+\exp\left(\frac{V_P - V_D}{2kT/q}\right)\right]\right)^2\right] \quad \textbf{(1.23)}$$

where

$$V_P = \frac{V_G - V_{TH}}{n} \quad \textbf{(1.24)}$$

$$n = \frac{1}{1 - \dfrac{\gamma}{2\sqrt{V_G - V_{TO} + \left(\dfrac{\gamma}{2} + \sqrt{2\phi_F}\right)^2}}} \tag{1.25}$$

with γ representing body effect factor as defined by

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \tag{1.26}$$

$$V_{TH} = V_{TO} - \gamma\sqrt{2\phi_F} + \gamma\sqrt{2\phi_F - V_B} + 3\frac{kT}{q} \tag{1.27}$$

$$V_{TO} = \Phi_{MS} + 2\phi_F + \frac{\sqrt{4q\varepsilon_{si}N_A\phi_F}}{C_{ox}} \tag{1.28}$$

Φ_{MS} in (1.28) shows work function difference potential and setting V_B equal to V_S or V_G in (1.27), the model can be used for DTMOS devices without any other modification [26].

Some of the measurement results from [26] are given in the following figures comparing the operation of DTMOS and normal grounded body SOI (GBSOI) devices. Figure 1.11 shows the output characteristic from measurements of a DTMOS transistor having 2μm channel length. In the figures, star (*) symbols represent the measurements and solid lines show EKV model. As it is seen from Figure 1.11, under 0.5V gate bias, the model and measurements are in close agreement. In Figure 1.12, subthreshold swings of DTMOS and normal MOS have been depicted where V_D is biased at 0.1V. Under 0.3V, DTMOS shows close to ideal 60mV/dec subthreshold swing and almost under 0.4V has better swing value than normal MOS transistor. From this figure, it can be figured out that, for gaining ideal subthreshold swing, biasing of DTMOS gate should not exceed 0.3V.

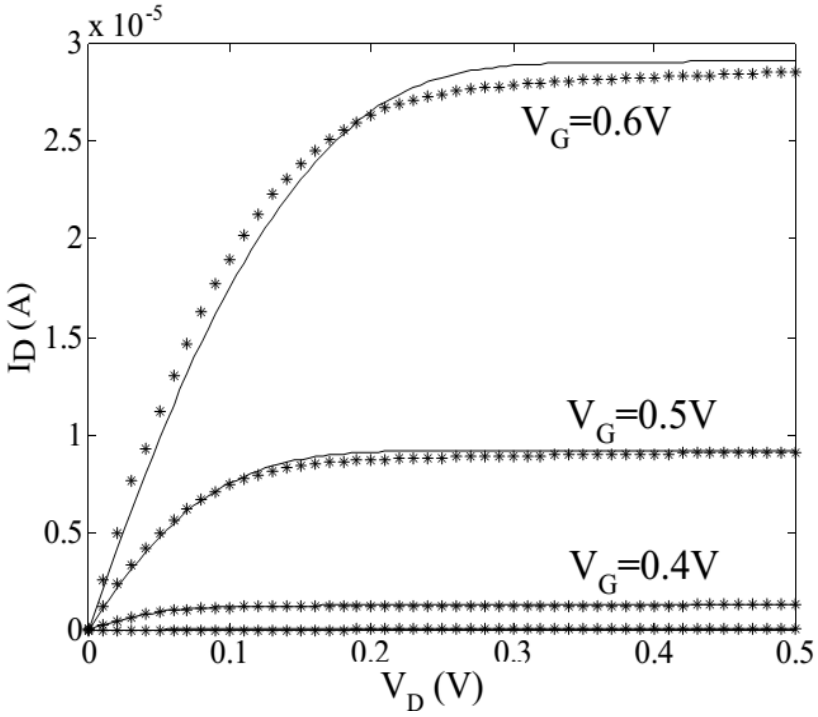


Figure 1.11 : Comparison of GBSOI and DTMOS output characteristics [26].

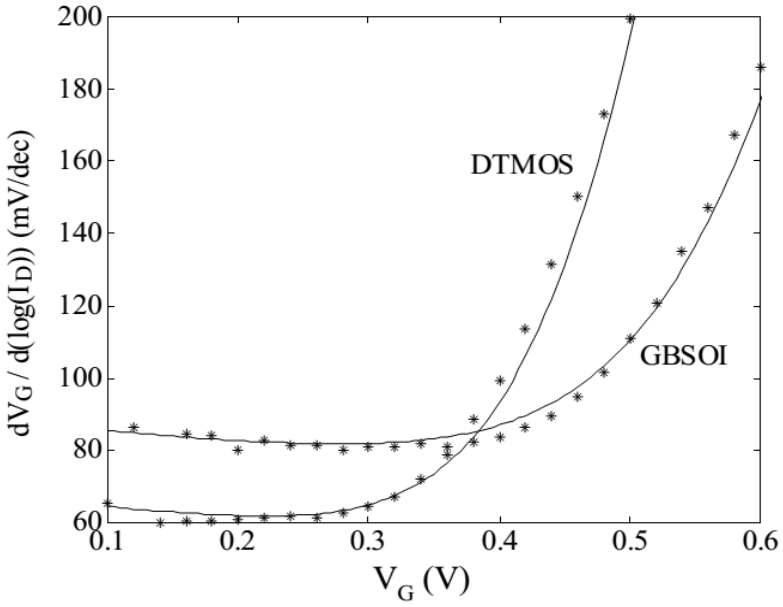


Figure 1.12 : Subthreshold swings of GBSOI and DTMOS transistors [26].

Similar to the above work, the validity of BSIM and BSIMSOI models was also investigated. It was found that, similar to EKV model, BSIM models even with total depletion approximation can be used for DTMOS transistors as verified by experiment results for long channel DTMOS transistors [7,14,28]. The same supply voltage limitation in the range of 0.4V~0.5V applies to BSIM models too. The

temperature characteristics of DTMOS were also investigated experimentally in [7] where the same 0.4V~0.5V forward bias limit manifests itself in Figure 1.13.

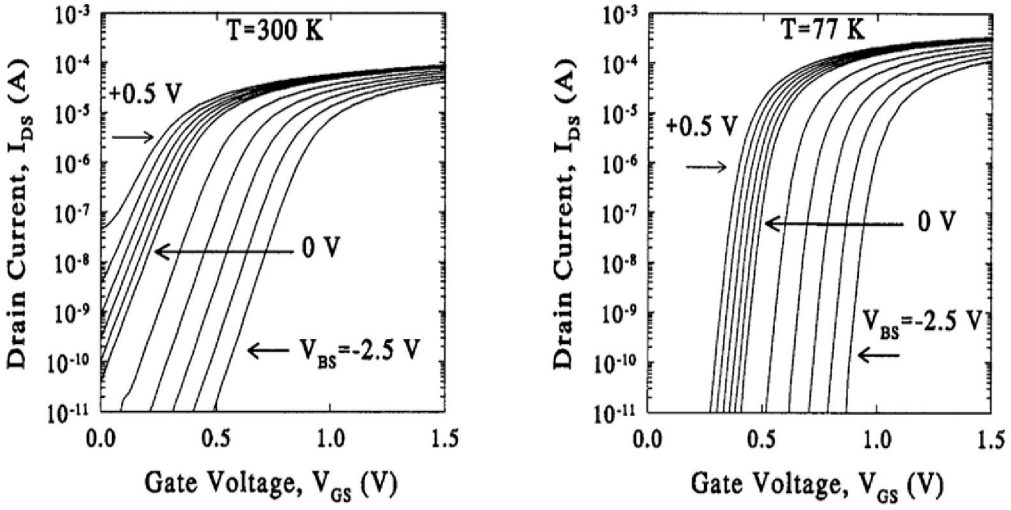


Figure 1.13 : Temperature characteristic of n-MOS 2µm DTMOS transistor [7].

Here, after a brief introduction of Y-parameters, we finally add a DTMOS transistor small signal equivalent circuit for a wide frequency band analysis from [29] to fully characterize the device with its Y-parameters. These parameters are often used for RF applications. For more information on RF characteristics of DTMOS transistor, references [30-32] can be read. For a general linear two-port network as shown in Figure 1.14, Y-parameters are defined as in (1.29).

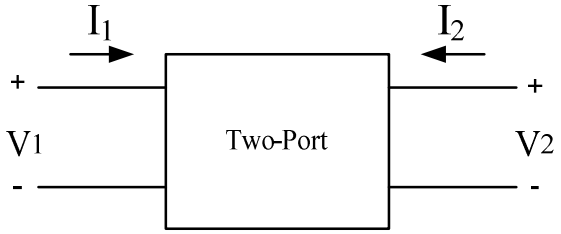
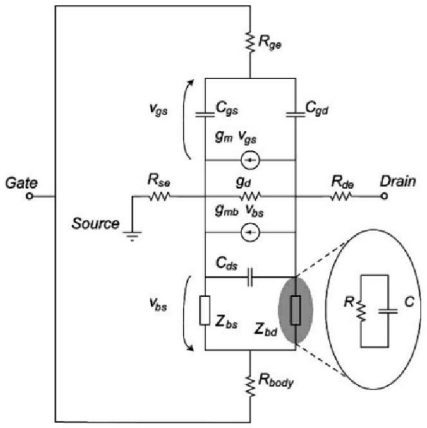


Figure 1.14 : General linear two-port network.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{1.29}$$

The model proposed by Dehan et al [29] with extracted model parameters is given in Figure 1.15 which was confirmed experimentally for a 0.25µm SOI DTMOS device in a frequency range from 100kHz to 4GHz.



Channel elements

g_m (mS)	g_d (mS)	C_{ds} (fF)	C_{gs} (fF)	C_{gd} (fF)
14.1	0.6	3.5	62	20

Body elements

g_{mb} (mS)	C_{bs} (fF)	R_{bs} (Ω)	C_{bd} (fF)	R_{bd} (Ω)
4.7	42.3	7000	10.3	∞

Resistances

R_{ge} (Ω)	R_{de} (Ω)	R_{se} (Ω)	R_{body} (Ω)
13	3	3	2900

Figure 1.15 : DTMOS small signal equivalent circuit [29].

In the model, complex impedances Z_{BS} and Z_{BD} model the source body and drain body junctions. g_d is the drain conductance, R_{se} , R_{de} and R_{ge} are the extrinsic parasitic source, drain and gate resistances respectively. In DTMOS transistors, gate and body are connected by a body resistance where R_{body} models this resistance. It is important to note that this resistance might have significantly large values for bulk-DTMOS and results in high RC delays if it appears on the signal path [14] which, however trading off the cost, can be solved by intervening standard CMOS process such as using the techniques in [33-34].

Y-parameters of the model in Figure 1.15 are given below [29].

$$Y_{11} = j\omega\left(C_{gs}+C_{gd}\right)+\left(R_{body}+\frac{Z_{bs}Z_{bd}}{Z_{bs}+Z_{bd}}\right)^{-1} \tag{1.30}$$

$$Y_{12} = -j\omega C_{gd}-\left(\frac{Z_{bs}}{Z_{bd}R_{body}+Z_{bs}R_{body}+Z_{bs}Z_{bd}}\right) \tag{1.31}$$

$$Y_{21} = g_m - j\omega C_{gd}+g_{mb}Z_{bs}\left(\frac{Z_{bd}-\left(1/g_{mb}\right)}{Z_{bd}R_{body}+Z_{bs}R_{body}+Z_{bs}Z_{bd}}\right) \tag{1.32}$$

$$Y_{22} = g_d + j\omega\left(C_{gd}+C_{gs}\right)+g_{mb}Z_{bs}\left(\frac{Z_{body}+\frac{1}{g_{mb}}\left(1+\frac{R_{body}}{Z_{bs}}\right)}{Z_{bd}R_{body}+Z_{bs}R_{body}+Z_{bs}Z_{bd}}\right) \tag{1.33}$$

Figure 1.16 illustrates the transconductance and output conductance of DTMOS and MOS transistors which shows the validity of the model for a wide frequency band. The degradations of DTMOS characteristics such as dynamic modulation of body by gate is generally caused by the high value of R_{body} resistance which can be reduced by using double body contacts or increasing the number of fingers of transistors [29].

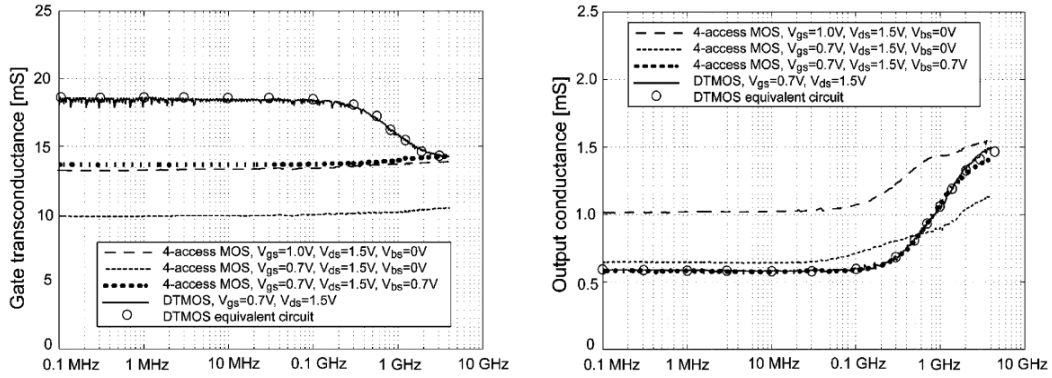


Figure 1.16 : Transconductance and conductance of DTMOS and MOS [29].

Consequently, it is important to summarize the modeling efforts explained in this section. It is shown in the literature that compact EKV, BSIM models are still valid for less than 0.4V~0.5V forward biased source body, drain body junctions even those models assume the total depletion approximation. Under these voltage levels, free carriers in the channel are so small in numbers that their effects can be safely neglected in the operation of long channel DTMOS devices. One last point to be mentioned in this section is the noise characteristics of DTMOS transistors. Unfortunately, there are not generally accepted, comprehensive noise analyses and models that are experimentally proven for DTMOS transistors. Nevertheless, interested readers may refer to the references [35-37] for further insights on the subject.

1.3 Some DTMOS-based Circuits Available in the Literature

DTMOS transistor was initially proposed for digital circuits which has the ability to work under low supply voltages with its low on-state threshold voltage and simultaneously, it is capable of operating with low leakage currents because of its high off-state threshold voltage value due to its dynamic operation principal as explained in [3-4]. Similar to DTMOS transistors, forward body biasing technique (FBB) uses the same idea of reducing threshold voltage by applying DC bias to the

body of a MOS transistor [38]. This type of operation was practiced in analog applications to increase current of the transistor due to reduction in the threshold voltage under ultra low supply voltage by connecting the bulk of transistors to fixed voltage levels with controlling the maximum forward body bias. In this study, FBB method is also expressed as in the concept of DTMOS technique.

As a difference to DTMOS transistors, in DTMOS technique, gate and body connection is not necessary so the transistor can be freely used as a four terminal device which is favored in some analog and digital applications [39-43]. Figure 1.17 illustrates these two types of design strategies of DTMOS approach. Although, we have made a distinction here, these two terms are sometimes used interchangeably in the literature. Furthermore, both of these strategies can sometimes be used in a single design such as, in the design of an ultra low-voltage OTA circuit where twin-well process technology are used to reach the bodies of both PMOS and NMOS transistors [44].

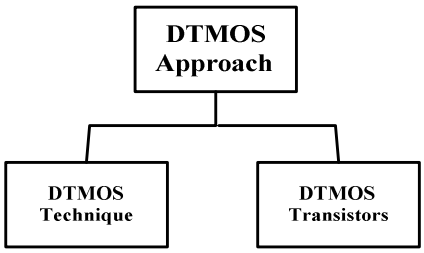


Figure 1.17 : DTMOS design strategy.

DTMOS technique was used to realize a common mode feedback circuit (CMFB) for a folded cascode amplifier in [39-41] which is shown in Figure 1.18 with the circuit part that is realizing the CMFB circuit.

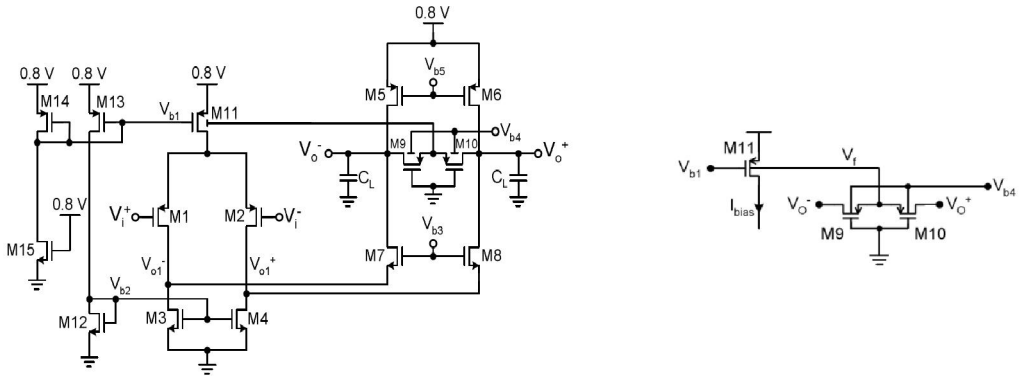


Figure 1.18 : Folded cascode amplifier using DTMOS technique [39-41].

In the circuit in Figure 1.18, to compensate the voltage variations over M11, a feedback is applied to its body by M9 and M10 which sense the common mode voltage and behaves as big two resistors. Figure 1.19 shows the effectiveness of the CMFB circuit utilizing DTMOS technique.

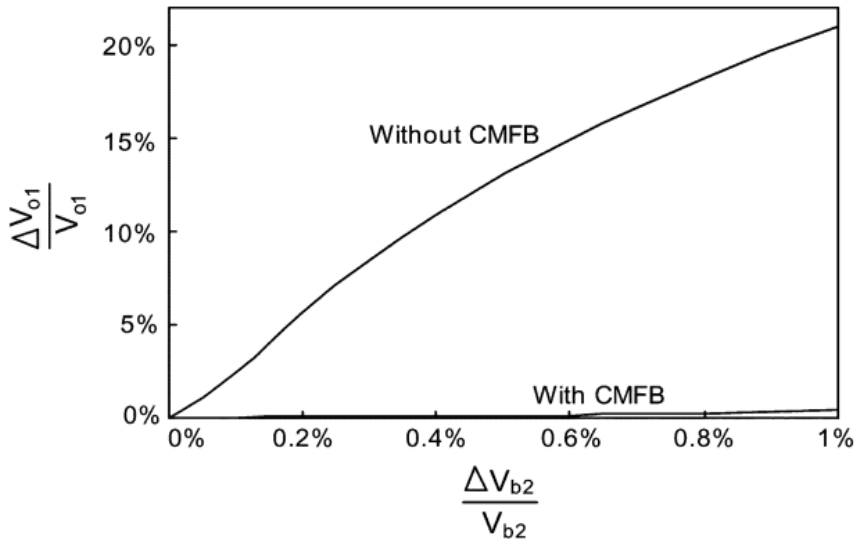


Figure 1.19 : The CMFB circuit effectiveness [39].

Another circuit with DTMOS technique was proposed in [45]. The designed OTA circuit operates under 0.5V supply voltage with a 61dB dynamic range at 1% THD consuming 0.6mW and it was used as the active element in a fifth-order Chebyshev filter. However, to reach the bodies of both PMOS and NMOS transistors in the circuit, an expensive triple-well fabrication process was used.

DTMOS approach, either as DTMOS transistors or DTMOS technique is utilized in digital circuits [46-49]. Since the scope of this study does not include digital circuits, we have just preferred to give them as references except the inverters in [48] as an example of DTMOS usage in digital circuitry. The DTMOS inverters are depicted in Figure 1.20 where the first one uses additional auxiliary transistors to reduce the input load of the inverter to increase overall performance of the inverter, second inverter in the figure is the classical DTMOS inverter proposed by Assederaghi et al [3-4].

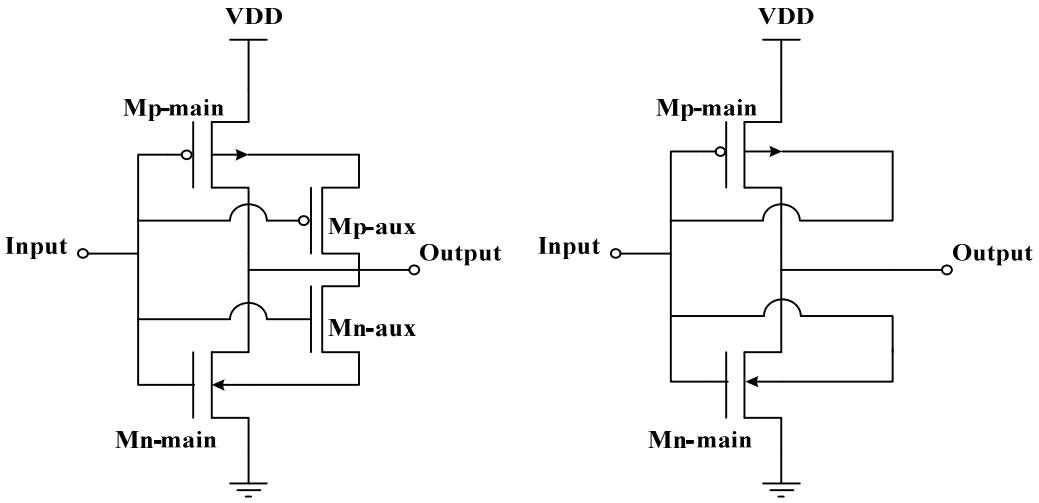


Figure 1.20 : DTMOS inverters [48].

The measured delays of the inverter with auxiliary transistors and normal CMOS inverter are compared in Figure 1.21. It is seen that DTMOS inverter has less delay than its CMOS counterpart due to its higher current drive.

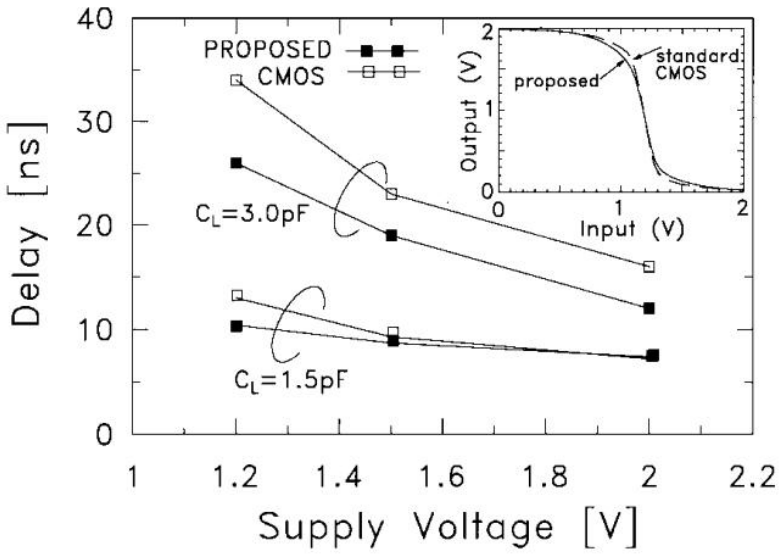


Figure 1.21 : Delay comparison of DTMOS and MOS inverters [48].

Conventional bandgap references are limited by almost 1.25V bandgap of silicon for low-voltage operation [50]. Therefore, low power reference designs have become an active research topic. Low-power bandgap reference design is another DTMOS application area. Some studies about this topic can be found in [51-54] where diodes realized by DTMOS transistors behave virtually as low bandgap devices. Similar to bandgap references, by using DTMOS transistors, a precision temperature sensor was also proposed in [55].

Figure 1.22 shows a DTMOS-based bandgap reference with 0.65V reference voltage from [51] where diode connected PMOS transistors are used in DTMOS configuration utilizing their virtually lower bandgap reference characteristic as given in (1.34). The shaded area in Figure 1.22 shows a low-voltage current mirror similar to the design in [56].

$$V_{gap,DTMOS(apparent)} = V_{gap} - \phi_{bl} \tag{1.34}$$

where ϕ_{bl} is the barrier lowering voltage [51] and given by (1.35).

$$\phi_{bl} = \frac{\Phi_{GW}.C_{ox}}{C_{ox} + C_b(\phi_{bl})} \tag{1.35}$$

Φ_{GW} shows the built-in voltage between the gate and well of DTMOS transistor and C_b is the depletion capacitance. For a standard 0.35μm CMOS p-type DTMOS device in [51] apparent bandgap voltage extrapolated to 0K is about 0.6V significantly less than normal bipolar transistors and silicon diodes having 1.2V bandgap.

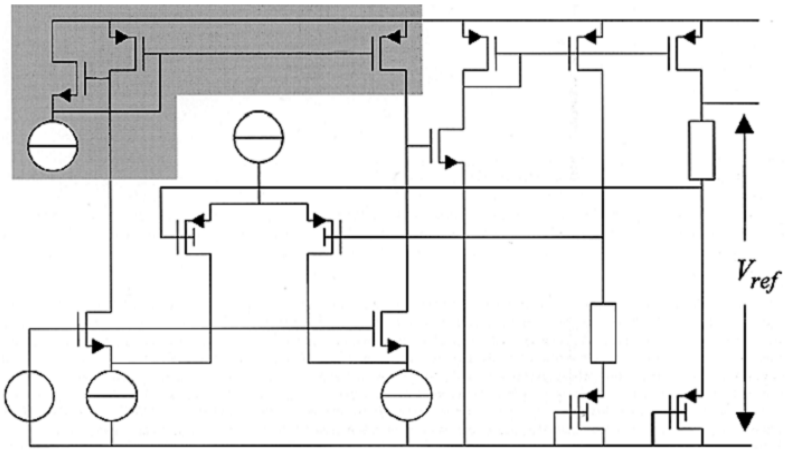


Figure 1.22 : Low-voltage DTMOS bandgap reference [51].

1.4 Motivation for This Study

DTMOS transistor having unique features is a very suitable device for ultra low power ultra low voltage circuits. However, because of its modelling difficulties and subtle operation dynamics, this device has not been fully appreciated in the literature. The need for low-voltage designs has been continuously growing where the requirements of the today's and even future circuits can be met by this device

successfully. Especially, its ideal subthreshold swing feature leads to efficient subthreshold circuits capable of operating even under 0.5V supply voltage whenever ultra low power consumption is necessary such as biomedical operations. A few examples can be given as wireless EEG or hearing aid applications where operation frequency and speed is not the main design specification but power consumption is the top priority. Interestingly, there are very few studies on DTMOS-based circuits for aforementioned applications in the literature.

Consequently, in this study, we have tried to connect this missing link and showed even using standard bulk CMOS technologies such circuits can be realized under ultra low supply voltage of 0.5V with consuming power ranging in nanowatt levels. Furthermore, in DTMOS technique, freely available bulk terminal can be used for original circuit solutions by adjusting biasing of the transistor. That idea can be used for tuning in different applications such as MOS-only filters.

2. DTMOS OTA DESIGN

This section summarizes a DTMOS-based OTA design and its application to EEG data processing. An OTA circuit in Figure 2.1 was designed using PMOS DTMOS transistors. For the validity of our MOSFET models, we have used minimum channel lengths as 2µm long and the supply voltage is chosen ±0.2V for safe operation that prevents excess currents from forward biased junctions which may violate BSIM model we have used.

2.1 DTMOS OTA Circuit

The proposed ultra low voltage low power OTA circuit is depicted in Figure 2.1 where transistor M1-M5 are chosen as DTMOS transistors since the process is n-well so only PMOS transistors can be connected as DTMOS.

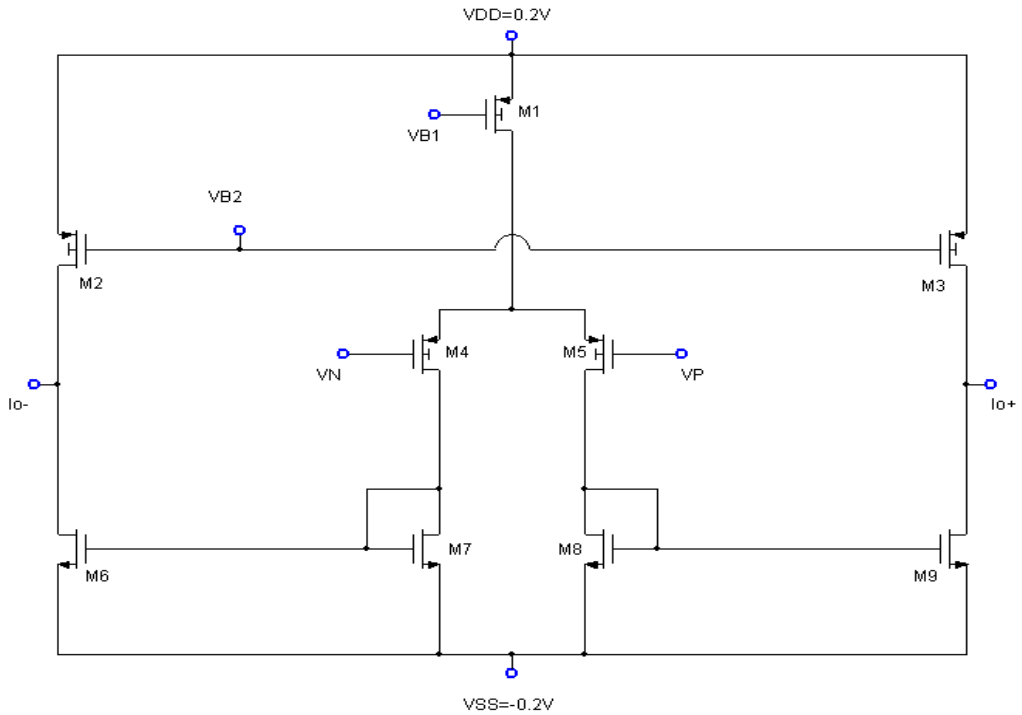


Figure 2.1 : DTMOS-based ultra low voltage OTA [57].

All the transistor channel lengths are chosen 2µm while maximum transistor width does not exceed 300µm. The dimensions of the transistors in Table 2.1 are obtained for a tail current of 2.65nA in the designed circuit.

Table 2.1 : Transistor dimensions.

Transistor	Channel Width (W)	Channel Length (L)
M1, M2, M3	5 µm	2 µm
M4, M5	300 µm	2 µm
M7, M8	50 µm	5 µm
M6, M9	100 µm	5 µm

In SPICE simulations, the circuit consumes only 3.18nW power. Biasing voltages V_{B1} and V_{B2} were chosen as reference potential. That eliminates the necessity to form separate biasing voltage circuits. As it is seen from voltage transfer characteristic in Figure 2.2, when the circuit is supplied by a symmetric ±0.2V supply voltage, its input voltage swings between -120mV and 60mV. Under this biasing conditions, it shows a transconductance of 54nA/V which can be defined as in (2.1).

$$G_m = \frac{g_{m5,m4}}{g_{m8,m7}} g_{m9,m6} \qquad \textbf{(2.1)}$$

The 3dB-bandwidth of this transconductance was found as 3.3kHz. Although this frequency bandwidth for the transconductance seems less for some application, it was quiet sufficient for the filter circuit used in real EEG data processing. For the proposed circuit, the performance summary was tabulated in Table 2.2.

Table 2.2 : OTA performance summary.

Technology	TSMC 0.18µm
Supply voltage	±0.2V
Power consumption	3.18nW
Transconductance	54nA/V
Tail current	2.65nA
Transconductance 3dB-frequency	3.3kHz
Input resistance@1kHz	213MΩ
Output resistance@1kHz	762MΩ

The voltage transfer characteristic of the proposed circuit is shown in Figure 2.2. The circuit operated without following error, fairly close to the negative supply rail but misses more than half of the positive rail. This might be improved by employing rail to rail input stages [58]. However, this requires both constant transconductance circuitry and a twin-well process for NMOS DTMOS generation. Ordinary NMOS usage in this circuit topology is limited by 0.4V ultra low-voltage supply rail.

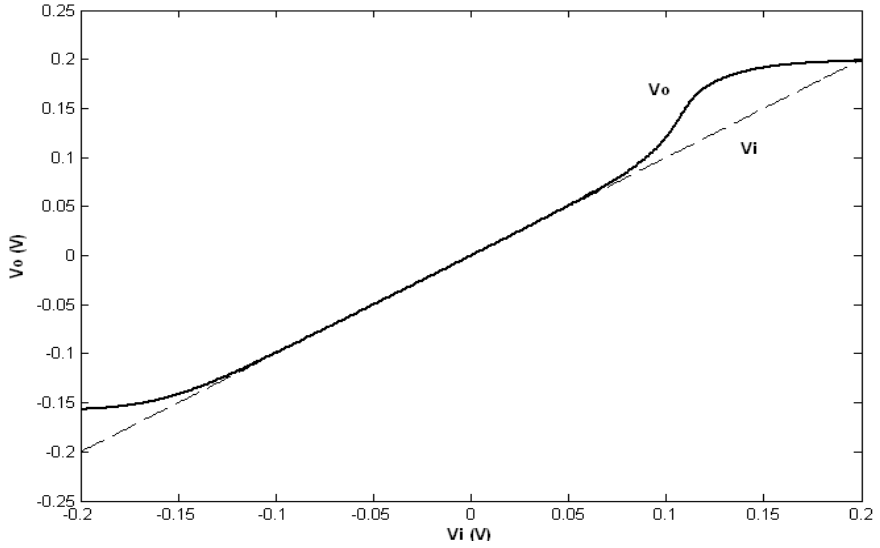


Figure 2.2 : DTMOS-based OTA voltage transfer characteristic [57].

In Figure 2.3, the transconductance of the OTA is drawn against frequency, which has the value of 54nA/V, when V_{B1} biasing voltage is connected to the reference.

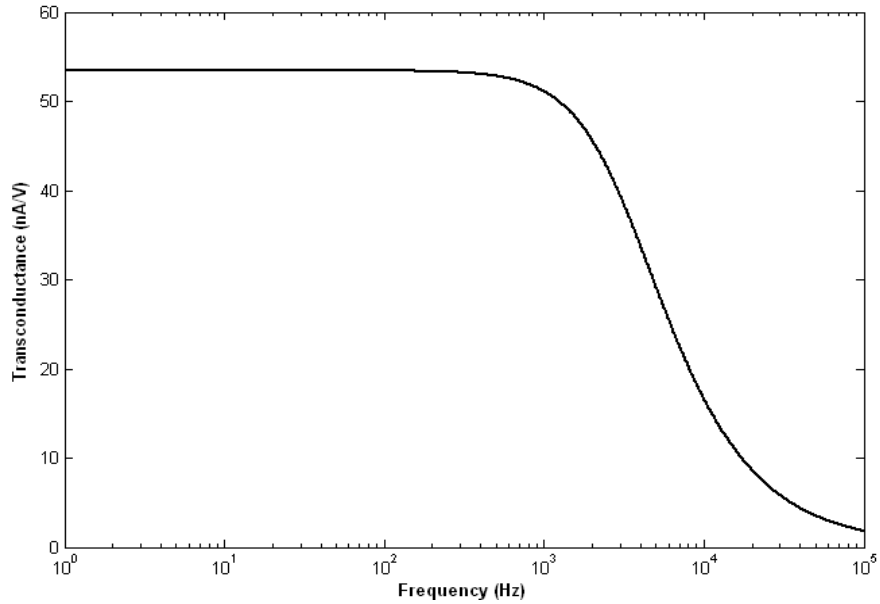


Figure 2.3 : DTMOS-based OTA transconductance characteristic [57].

The transconductance value can be adjusted by either changing the adjusting voltage value or, in some degree, changing the dimension of M1 transistor for different applications but this value for the EEG data filtering circuit was sufficient.

2.2 OTA-based Band-pass Filter

The proposed OTA circuit was used in a band-pass configuration in Figure 2.4 to filter real EEG measurements by connecting low-pass and high-pass filter biquads from [59-60] to maximize pass-band flatness which is necessary when EEG signals are considered. In the design, BSIM3v3.2 TSMC 0.18 µm process parameters are used to model the transistors with passive element values C_1=348pF C_2=174pF C_3=3040pF C_4=1520pF and W/L ratios of Table 2.1 were used for the EEG filter application.

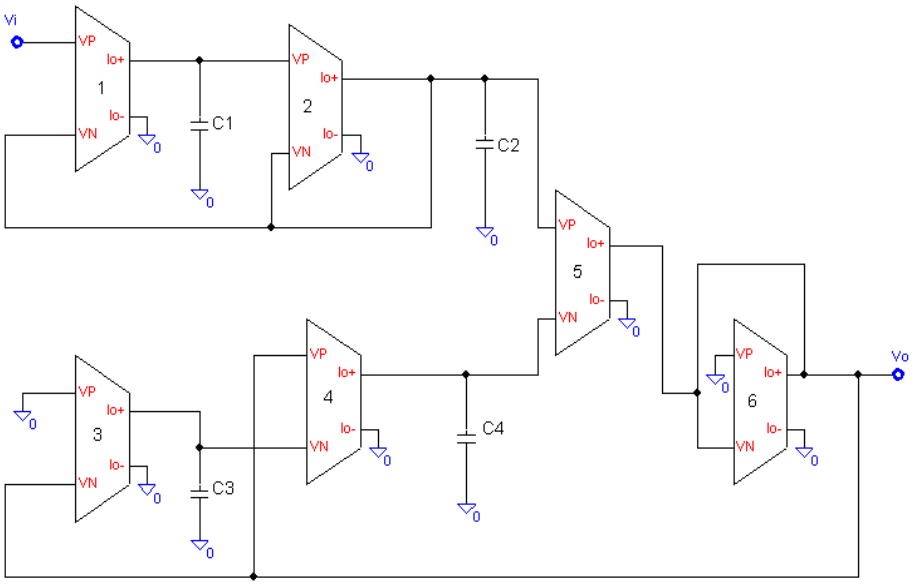


Figure 2.4 : OTA-C band-pass filter [57,59-60].

The transfer function of the filter in Figure 2.4 is given in (2.2) and design equations are given in (2.3).

$$\frac{V_o}{V_i} = \frac{\omega_{p1}^2}{s^2 + \frac{\omega_{p1}}{Q_{p1}} s + \omega_{p1}^2} \frac{s^2}{s^2 + \frac{\omega_{p2}}{Q_{p2}} s + \omega_{p2}^2} \qquad \textbf{(2.2)}$$

$$C_1 = \frac{G_{m1}}{Q_{p1}\omega_{p1}} \quad C_2 = \frac{G_{m2}Q_{p1}}{\omega_{p1}}$$
$$C_3 = \frac{G_{m3}}{Q_{p2}\omega_{p2}} \quad C_4 = \frac{G_{m4}Q_{p2}}{\omega_{p2}} \qquad \textbf{(2.3)}$$
$$G_{m5} = G_{m6}$$

The simulated and ideal filter responses are in close agreement from 0dB to -40dB amplitude. Flatness can be seen at the pass band from Figure 2.5. Instead of using high-pass and low-pass filters to get this flat pass band response, two band-pass filters can be used together with proper tuning.

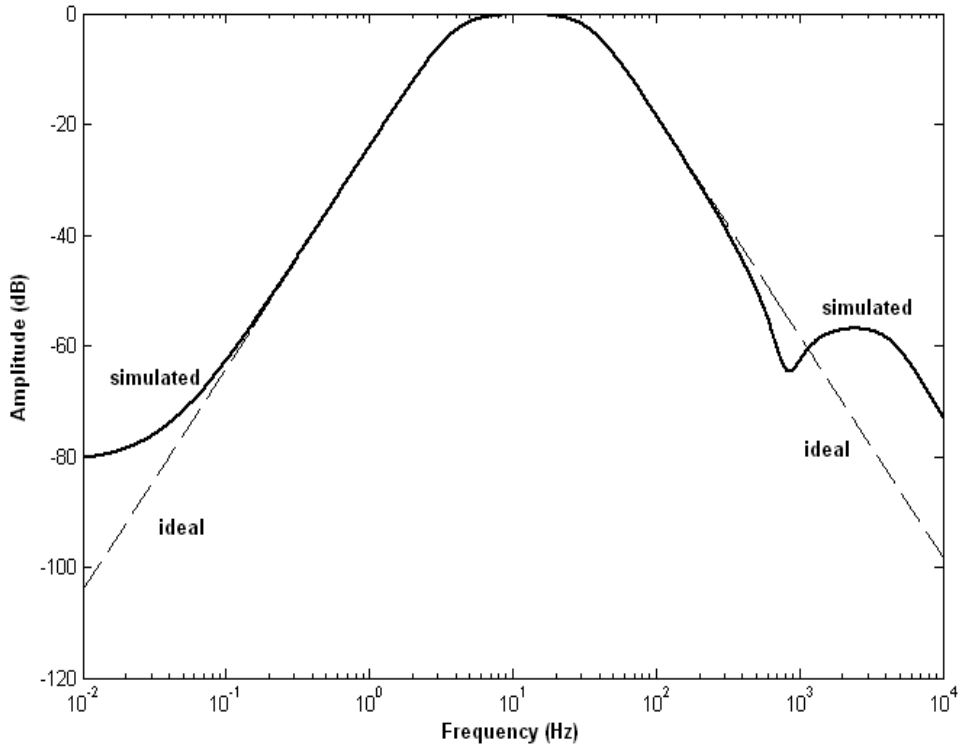


Figure 2.5 : The simulated and ideal responses of OTA-C band-pass filter[57].

After 1kHz, actual filter response deviates from the ideal one which is induced by the limited bandwidth of the OTA used in the filter. This can be increased by adjusting W/L ratios of the transistors and biasing voltages but we actually do not favour high currents to increase the bandwidth when very low frequency EEG signals are processed in the circuit because this will unnecessarily increase the power consumption.

Figure 2.6 shows the total harmonic distortion against input peak to peak voltage signal where it can be seen that THD value becomes less than 9% for all the common mode range.

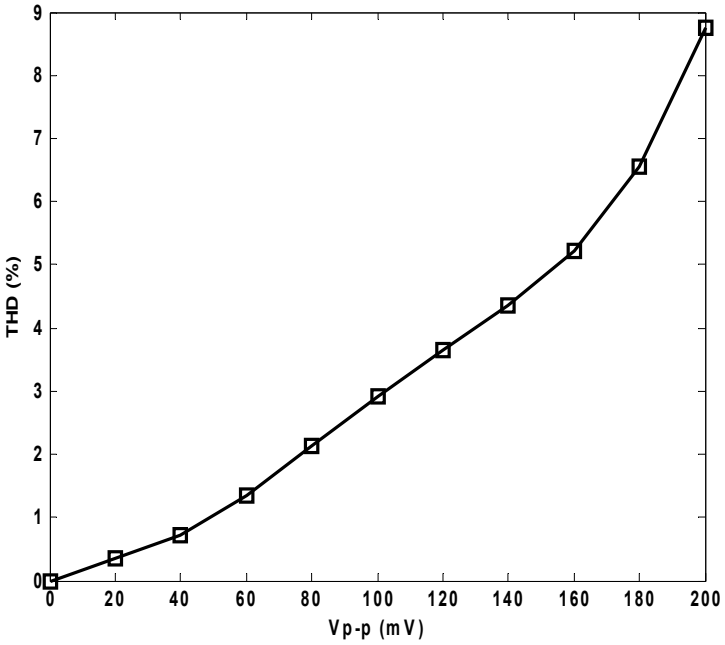


Figure 2.6 : OTA-C band-pass total harmonic distortion[57].

2.3 EEG Application using OTA Element

The band-pass filter circuit in Figure 2.3 was used to filter out unwanted signals from real EEG data measurements of the author's brain [61]. Resulting input and output signals are depicted in Figure 2.7 where the bold lines represent output signal which is clear of high and very low frequency signal. The band-pass filter circuit is composed of high-pass filter having 4Hz pole frequency and low-pass filter having 35Hz pole frequency to process the EEG data that carries the frequency information of steady state visually evoked potential (SSVEP). This information is extracted from the EEG of the subject after s/he is stimulated visually. SSVEP is used in human-brain interface studies which is an active research topic in biomedical engineering.

The importance of the proposed design is that the DTMOS transistors are first used in EEG data processing. It was shown in the proposed circuit that DTMOS transistors are suitable elements for ultra low voltage and ultra low power applications where the signal frequencies are not high such as the EEG data signals in this study.

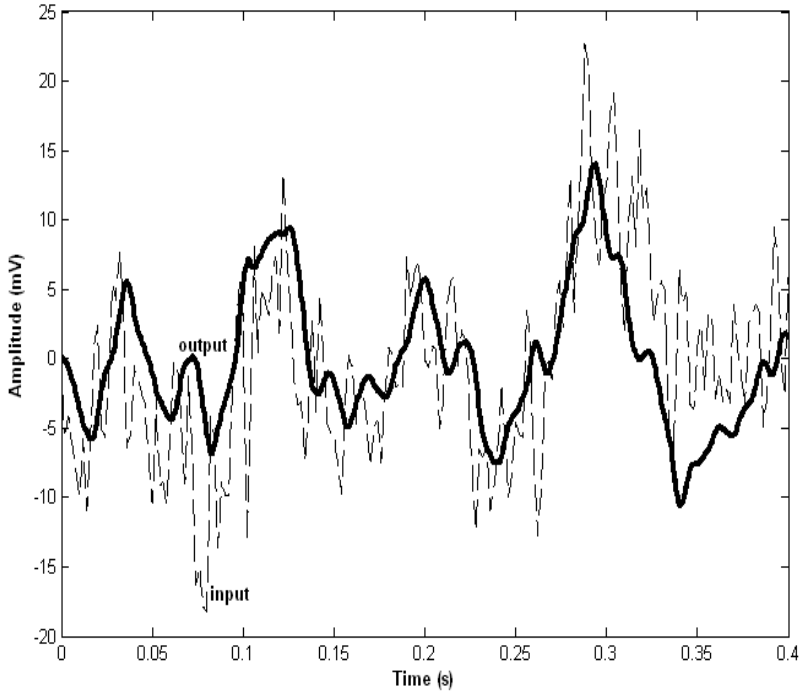


Figure 2.7 : The input and output responses of the filter for EEG signal [57].

3. DTMOS VDTA DESIGN

Voltage differencing transconductance amplifier (VDTA) is a recently proposed active element [62]. It has voltage inputs, an alternative to current differencing transconductance amplifier (CDTA) where the inputs are currents [63]. These voltage inputs result in new useful propositions for conventional circuits of analog signal processing [64]. The circuit symbol of VDTA is given in Figure 3.1 and its definition relations are shown in matrix form in (3.1).

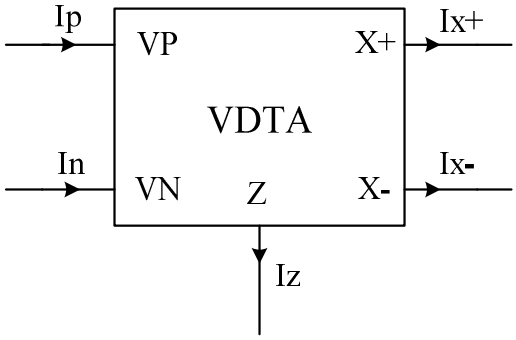


Figure 3.1 : VDTA circuit symbol.

$$\begin{bmatrix} Iz \\ Ix+ \\ Ix- \\ Ip \\ In \end{bmatrix} = \begin{bmatrix} G_{m1} & -G_{m2} & 0 & 0 & 0 \\ 0 & 0 & G_{m2} & 0 & 0 \\ 0 & 0 & -G_{m2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_{Z} \\ V_{X+} \\ V_{X-} \end{bmatrix} \quad \textbf{(3.1)}$$

The voltage difference of input terminals is multiplied by a transconductance of G_{m1} which then becomes the I_Z current. This current flows over the impedance at the Z terminal forming the voltage at Z terminal. This voltage is then multiplied by positive and negative $\pm G_{m2}$ transconductances to form the output $\pm I_X$ currents.

3.1 DTMOS VDTA Circuit

The proposed DTMOS-based ultra low-voltage, ultra low-power VDTA circuit is illustrated in Figure 3.2. VDTA element can be generated by connecting two OTA circuits in a cascaded fashion. The transistors from M1 to M9 constitute the first OTA and the transistors from M10 to M18 constitute the second OTA where the transistors from M1 to M5 are DTMOS and similarly in the second part, the transistors from M10 to M14 are DTMOS. These DTMOS transistors having ideal subthreshold swing efficiently use the available voltage headroom under the ultra low supply voltage of ±0.2V.

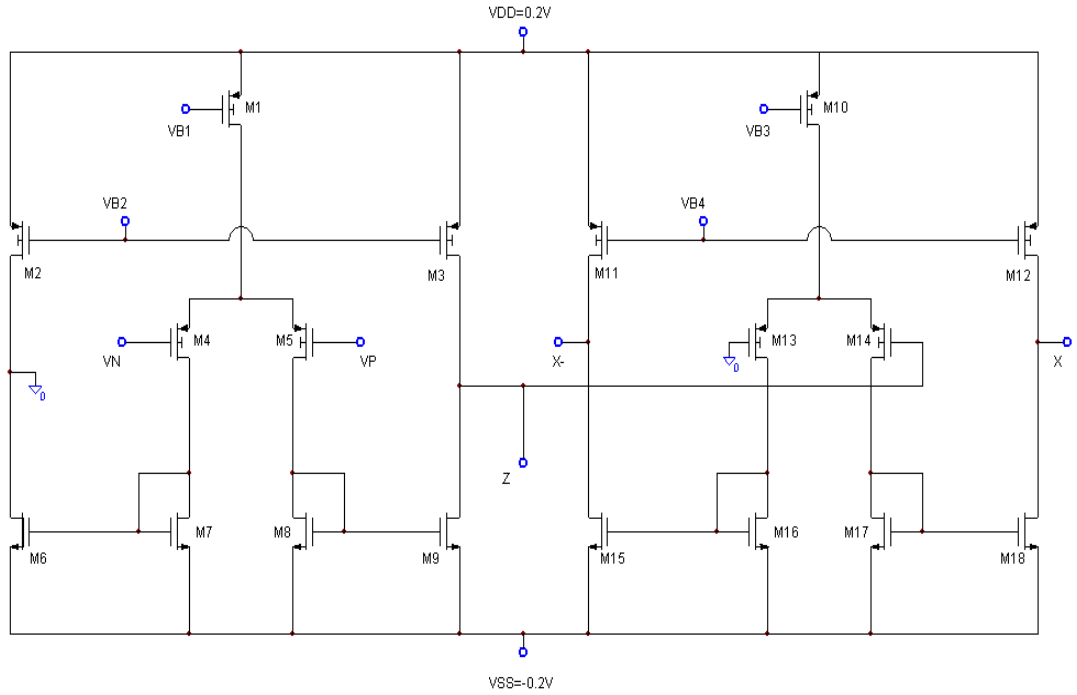


Figure 3.2 : The proposed VDTA circuit [65].

In an n-well standard CMOS process, PMOS transistors can only be connected as DTMOS transistors whereas NMOS transistors share a common well in an n-well process and their body terminals cannot be connected to their gates to generate NMOS DTMOS transistors. One possibility is to use expensive triple-well processes with deep n-wells to produce NMOS transistors with their own wells. The cost restriction limits the overall performance of the proposed circuit where most of the voltage headroom is consumed over the NMOS transistors. As a result, strong inversion operation and high frequency applications are not possible using this circuit where the transistors are biased in weak inversion. In this mode of operation, MOS

transistor's drain current is given by (3.2), transconductance by (3.3) and the transconductance resulting from body effect by (3.4) as described in [66]. Active-block transconductance G_m is given in (3.5). The parameters in (3.2), (3.3), (3.4) and (3.5) have their usual meanings.

$$I_d = I_s\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad \textbf{(3.2)}$$

$$g_m = q\frac{I_D}{nkT} \quad \textbf{(3.3)}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_F - V_{SB}}}g_m \quad \textbf{(3.4)}$$

$$G_{m1} = \frac{g_{m5}}{g_{m8}}g_{m9} = G_{m2} = \frac{g_{m14}}{g_{m17}}g_{18} \quad \textbf{(3.5)}$$

Using TSMC 0.18µm BSIM3v3.2 process parameters, PSPICE gives VDTA transconductances $G_{m1} = G_{m2} = 54$nA/V for the proposed circuit. Tail bias current flowing over both M1 and M10 transistors is 2.65nA when the transistor dimensions in Table 3.1 are used in the design. In Figure 3.3, voltage transfer characteristic of the VDTA circuit is shown. While obtaining this characteristic, VDTA was connected in a feedback configuration and the Z terminal was loaded with a 1nF capacitor, which is a typical load value for the operating frequency.

Table 3.1 : Transistor dimensions of the proposed VDTA circuit.

Transistors	Width	Length
M1, M2, M3, M10, M11, M12	5µm	2 µm
M4, M5, M13, M14	300 µm	2 µm
M7, M8, M16, M17	50 µm	5 µm
M6, M9, M15, M18	100 µm	5 µm

It is found from the figure that input voltage swing range is between -170mV to 60mV under ±200mV supply voltages.

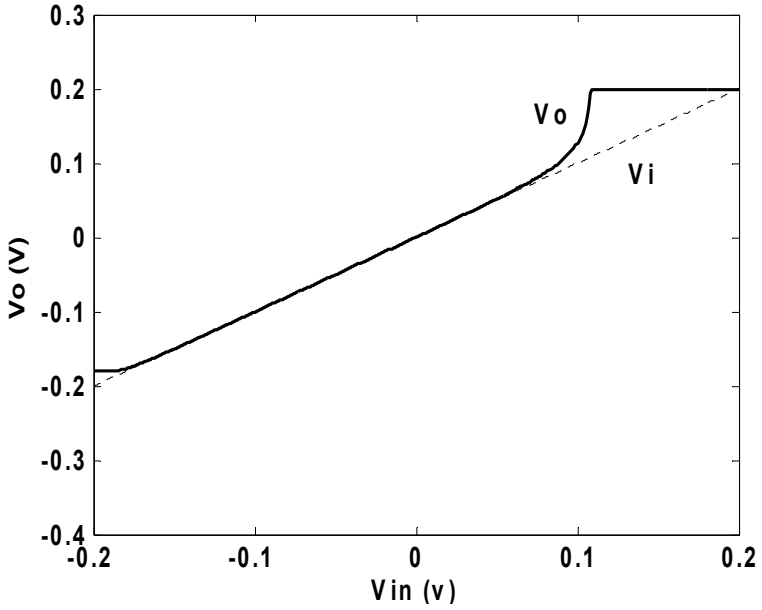


Figure 3.3 : Voltage transfer characteristic of the proposed VDTA circuit [65].

VDTA transconductance $G_m=G_{m1}=G_{m2}$ is depicted in Figure 3.4 where it is found approximately as 54nA/V with a 3dB bandwidth of 3.3 kHz.

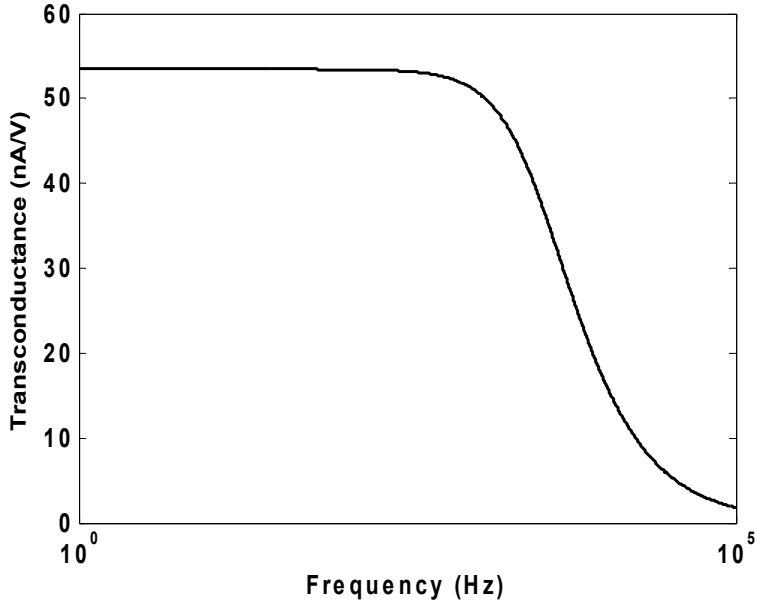


Figure 3.4 : Transconductance characteristic of the proposed VDTA circuit [65].

Performance summary of the proposed VDTA is tabulated in Table 3.2.

Table 3.2 : VDTA Performance summary.

Technology	TSMC 0.18μm
Supply Voltage	±0.2V
Input Voltage Range	-170mV - 60mV
Power Consumption	5.96nW
Transconductances (G_{m1}=G_{m2})	54nA/V
Transconductance 3dB Frequency	3.3kHz
Input Resistance @300Hz	628MΩ
Output Resistance@300Hz	1.85GΩ

From the Table 3.2, it can be seen that the input range of this element is larger than the OTA design in section 2 which can be attributed to the inherent feedback in VDTA element. Total power consumption of the proposed VDTA circuit is just 5.96nW which is a very suitable value for ultra low-power operation. One last thing to note about this VDTA circuit is that there are four biasing voltages as seen from Figure 3.2. For our application, we have found that using the reference voltage level for them is possible. Grounding the biasing voltages as V_{B1}=V_{B2}=V_{B3}=V_{B4}=0V has prevented the necessity of additional circuitry.

3.2 VDTA-based Band-pass Filter

The VDTA-based band-pass filters in [64] are used in this study. The fourth-order band-pass filter employing proposed VDTAs is shown in Figure 3.5.

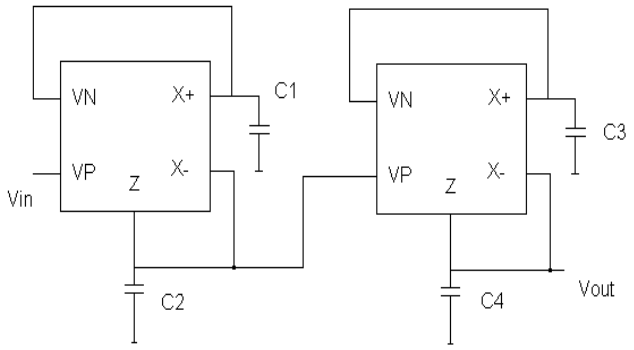


Figure 3.5 : VDTA-based double-tuned band-pass filter circuit [64].

The double-tuned circuit is comprised of two band-pass filters which are tuned using two different pole frequencies. The transfer function of the filter in Figure 3.5 is given in (3.6).

$$\frac{V_{out}}{V_{in}} = H_0 \frac{\frac{\omega_{p1}}{Q_{p1}} s}{s^2 + \frac{\omega_{p1}}{Q_{p1}} s + \omega_{p1}^2} \frac{\frac{\omega_{p2}}{Q_{p2}} s}{s^2 + \frac{\omega_{p2}}{Q_{p2}} s + \omega_{p2}^2} \tag{3.6}$$

where H_0 is the gain factor. Natural frequencies $\omega_{p1,2}$ and quality factors $Q_{p1,2}$ of the filter are determined according to the relations in (3.7) and (3.8).

$$\omega_{p1,2} = \sqrt{\frac{G_{m1,3} G_{m2,4}}{C_{1,3} C_{2,4}}} \tag{3.7}$$

$$Q_{p1,2} = \sqrt{\frac{C_{2,4} G_{m1,3}}{C_{1,3} G_{m2,4}}} \tag{3.8}$$

The non-ideal effects coming from the CMOS VDTA circuit such as parasitic capacitances and conductances modify the natural frequency and quality factor definitions as described in [64]. Parasitic capacitances appear at VP, VN inputs and Z terminal. Additionally, parasitic conductances occur at X_+, X_- and Z terminals.

The filter circuit was used in processing real EEG data measurements. For our EEG application, the requirement was a fourth order band-pass filter with a pass-band between 4Hz and 35Hz. For the double tuned filter, we have used the pole frequency relations in [67] where B is the bandwidth and f_0 is the center frequency. The EEG filter parameters, B=31Hz, f_c=19.5Hz and $Q_{p1}=Q_{p2}=1$ were chosen. The pole frequencies are f_{p1}=30.45Hz and f_{p2}=8.54Hz.

$$f_{p1} = \frac{\omega_{p1}}{2\pi} = f_c + \frac{B}{2}\sin\left(45^0\right) \tag{3.9}$$

$$f_{p2} = \frac{\omega_{p2}}{2\pi} = f_c - \frac{B}{2}\sin\left(45^0\right) \tag{3.10}$$

To realize these pole frequencies, VDTA transconductances and capacitor values were determined according to the relations in (3.7) and (3.8) which give $C_1=C_2$=1.006nF, $C_3=C_4$=0.282nF when VDTA transconductances

$G_{m1}=G_{m2}=G_{m3}=G_{m4}=54nA/V$ are chosen. Since relatively large capacitors are needed they should be connected to the filtering circuit externally.

Double-tuned band-pass filter using the circuit in Figure 3.2 was simulated using PSPICE program with above calculated passive element values. Ideal and simulated frequency responses of the filter are shown in Figure 3.6.

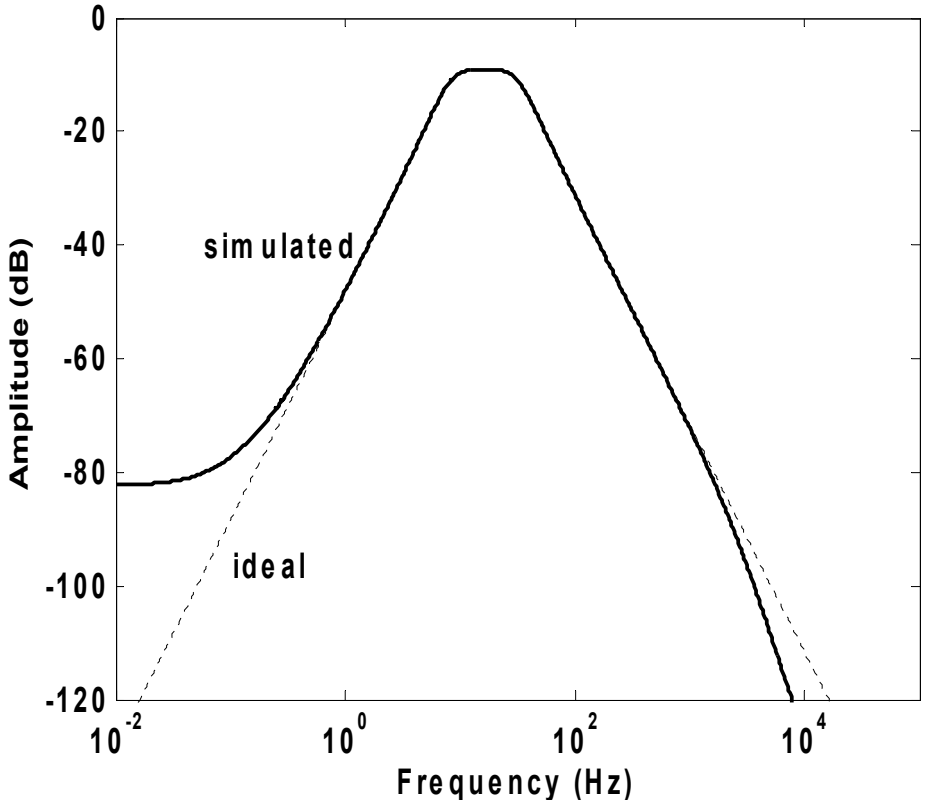


Figure 3.6 : Ideal and simulated frequency responses of the filter circuit [65].

The deviation from the ideal one, after a few kHz frequencies, is caused by the proposed VDTA's bandwidth which is limited to a few kHz range because the transistors in the active circuit operate in weak inversion. Actually, there is a trade-off between bandwidth and power consumption. High biasing currents bring higher bandwidth at the expense of high power consumption. Fortunately, for our EEG data filtering application, our active block's bandwidth was sufficient and did not lead to any problems.

In order to investigate the time domain response of the double-tuned VDTA-based band-pass filter, an input sine wave with a frequency of 20Hz and peak to peak amplitude of 100mV is applied and the corresponding response in Figure 3.7 is obtained. The decrease in the amplitude is actually the characteristic of the double-

tuned filter design because two different intersections of the two band-pass filters to obtain double-tuned response cause an expected decrease in the amplitude which can be increased by an additional circuitry if necessary.

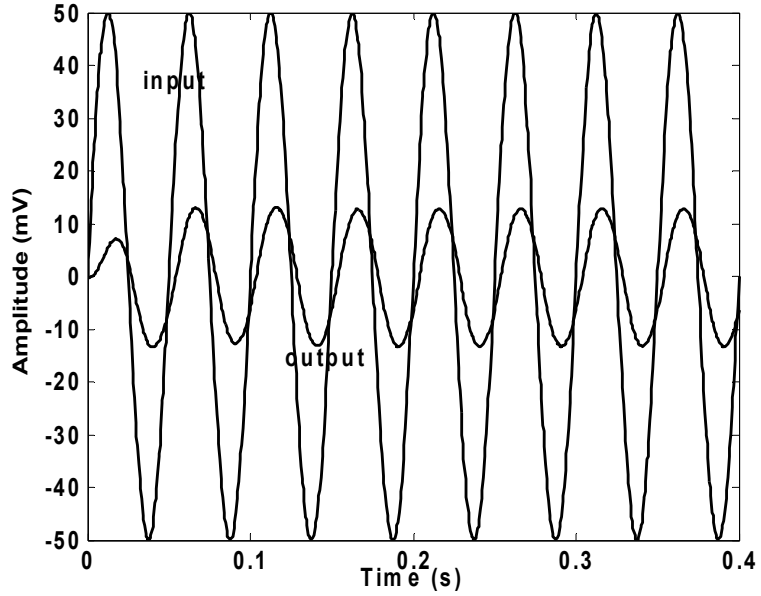


Figure 3.7 : Sinusoidal response of the filter for 20Hz, 100mV (p-p) signal [65].

Temperature is an important factor for very low frequency filters with large time constants. Therefore, it is necessary to analyze the change of pole frequencies with respect to the change in temperature [68].We have changed the temperature from 0°C to 75°C. Resulting amplitude characteristic is depicted in Figure 3.8.

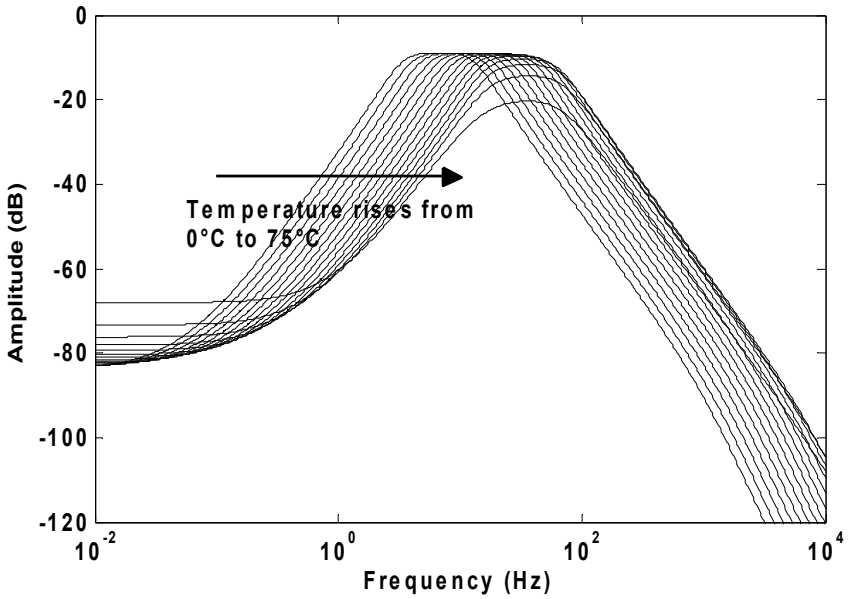


Figure 3.8 : Filter pole frequency change with temperature [65].

From Figure 3.8, it can be seen that the temperature drift of the center frequency is quite significant. This decreases signal amplitudes because of the drifted stop-band of the filter. Nevertheless, the filter can be used under conditions or in environments requiring high temperature change, if a compensation method is utilized to keep the center frequency in limits.

One solution to resolve this problem is explained in [68]. Another solution might be off-chip tuning of pole frequencies of the filter. In Figure 3.9, the response of the filter to a 20Hz sinusoidal input signal has been given for the temperature range from 27°C to 40°C. This limited range is chosen in the figure to prevent amplitude losses due to pass-band drift.

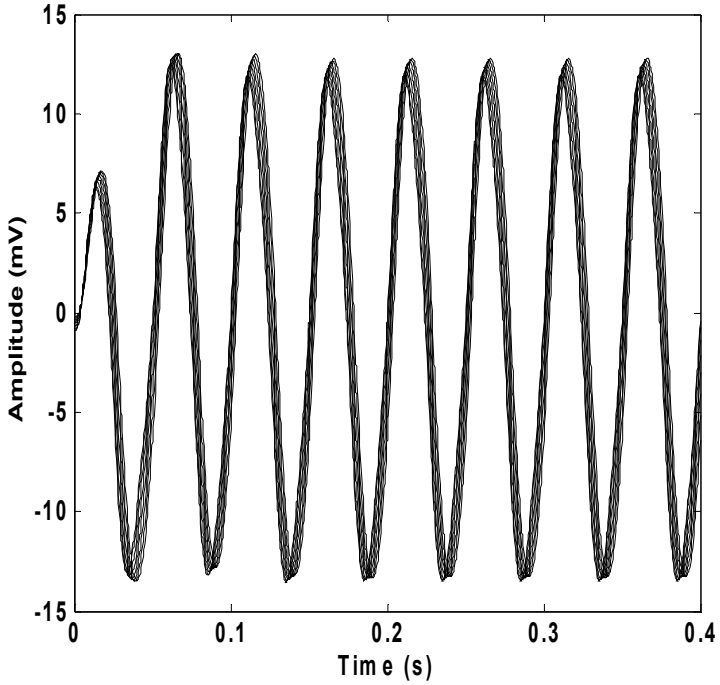


Figure 3.9 : Filter response to input signal for the change in temperature [65].

THD of the proposed filter was calculated with PSPICE and the related results was depicted in Figure 3.10 where the total harmonic distortion of the filter is less than %2 for inputs not exceeding 100mV peak to peak voltage.

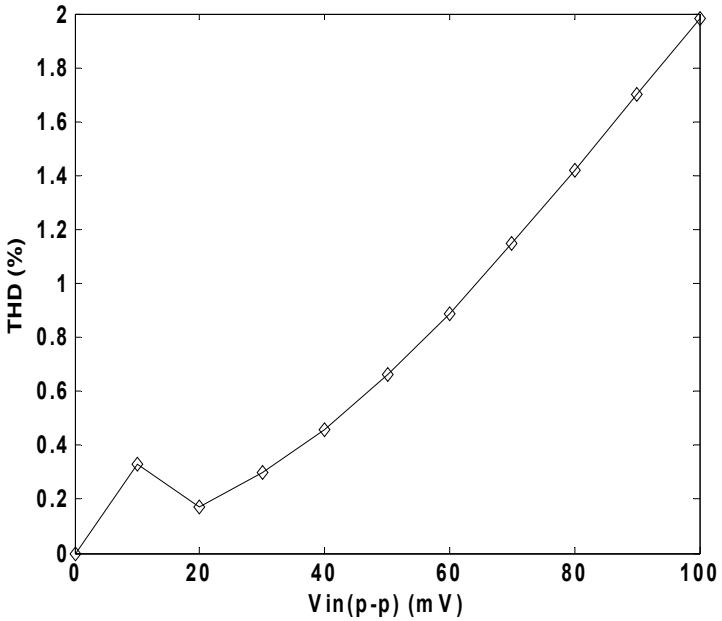


Figure 3.10 : Output THD of the filter with respect to input voltage [65].

Monte-Carlo simulations are performed with the help of PSPICE program to show the effects of process variations (W, L, t_{ox}, V_{TO}) on the filter amplitude characteristic. From Figure 3.11, it is seen that most of the cases the variations are in specific limits, however, there are some cases where deviations are significant. This is caused by the susceptibility of the circuit to process deviations which mainly affect the biasing under ultra low supply voltage with ultra low biasing currents. These biasing currents can be increased but this trades off power consumption performance of the filter.

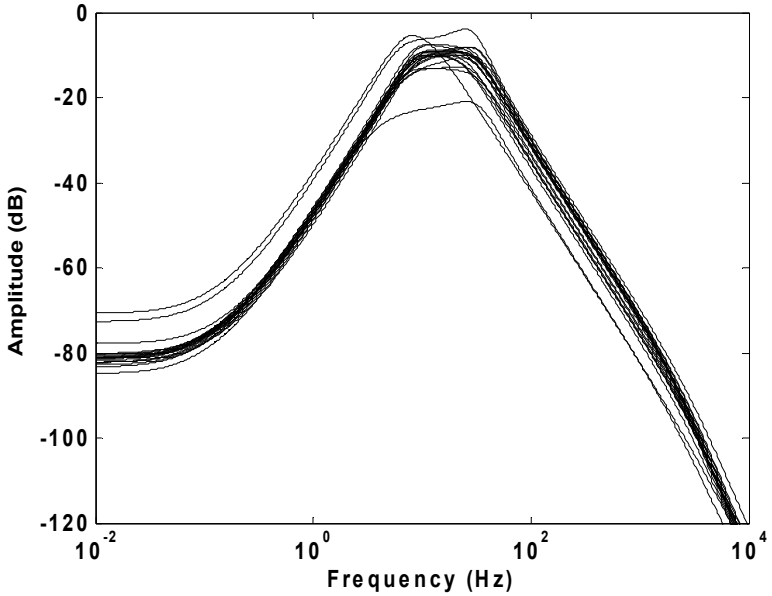


Figure 3.11 : Monte-Carlo simulations for the amplitude of the filter [65].

The noise is an another important parameter in EEG signal processing where the signal voltage levels are so weak that the desired signal components might be lost in the measuring process if noisy equipment is used. To investigate the noise performance of the VDTA filter, PSPICE simulations are performed in the frequency range of interest. Over a 500Hz bandwidth rms noise voltage was found as 22.9μV which is a significantly high value for EEG signal processing applications. This can be resolved by using, in the preceding stages, an instrumentation amplifier which has characteristically low noise level.

3.3 EEG Application using VDTA Element

In order to further investigate the characteristics of the proposed band-pass filter, real measurements from an SSVEP (Steady State Visual Evoked Potential)-based BCI (brain computer interface) EEG experiment were used with the help of MATLAB program.

SSVEP dominantly appears in the visual cortex of the brain and it is the result of a person's attention on flickering lights [61]. It is measured by using EEG methods. Constant frequency signals visually stimulate a person and this affects the person's EEG signal at the same frequency which can be used as a mean to brain computer interaction which is currently an active research topic.

EEG measurement setup and the data in [61] were used for applying input signal data to our filter. The experiment setup is shown in Figure 3.12. EEG signal is sensed via electrodes connected to the scalp. These signals are then fed into an amplifier system specialized on EEG data recordings. Amplified signal data are then transferred to computer for further processing.

The part of the experiment we used for filtering is comprised of computer recordings of the EEG signals of the subjects while they are looking at four red circles at the four the corners of the computer monitor flickering at four different constant frequencies (4.60Hz, 6.43Hz, 8.03Hz, and 10.70Hz). Applied input data is taken from the OZ channel of the connected 16 electrodes. This channel is more sensitive to the visual stimulations.

The EEG data was taken for 30s with a sampling frequency of 500Hz generating 15000 data points [61]. For simplicity, in our filter application, we have just used the

recordings for two seconds with 1001 data points from OZ channel recordings of the subject's visual attention on the left red circle that is flickering on the monitor with a constant frequency of 10.70Hz.

Figure 3.12 : EEG measurements setup [61,65].

Filter input and output signals are illustrated in Figure 3.13. For figure clarity, only the data of first 0.4s is shown in the figure and the output signal is multiplied by a factor of filter gain loss to compensate the decrease in amplitude. Input data signal amplitudes are also multiplied by a factor to manage to use them properly as inputs to the filter.

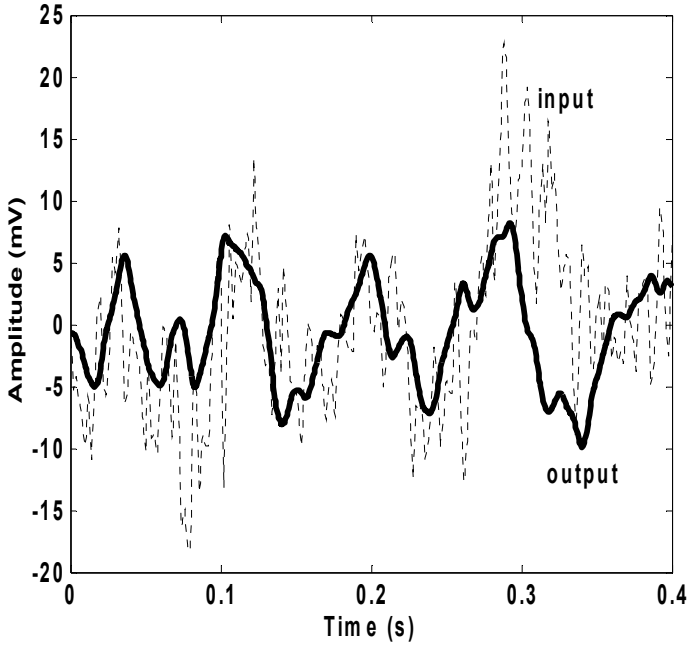


Figure 3.13 : Time response of the filter output to EEG data for 0.4s [65].

In Figure 3.14 and Figure 3.15, pre-filter and post-filter frequency spectrums of our EEG signal are depicted respectively.

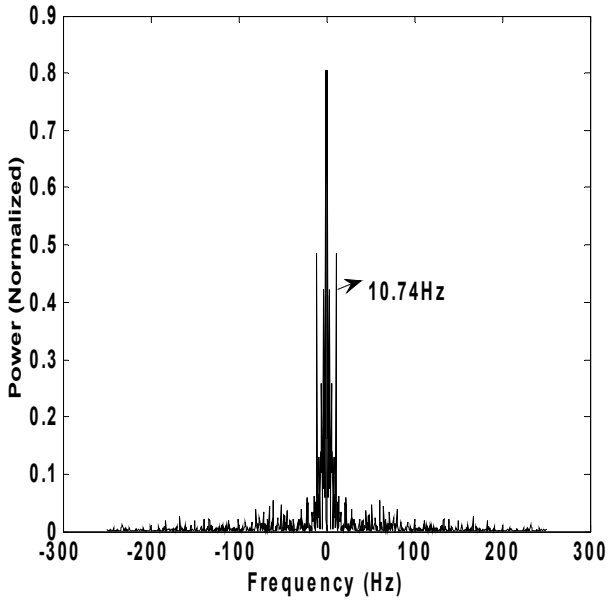


Figure 3.14 : Pre-filter frequency spectrum of the EEG data [65].

As shown in the figures, unwanted frequency harmonics are successfully filtered out from the signal by the VDTA filter and the main frequency component of 10.74Hz is become clearer at the filter output. That is almost the same frequency of the applied visual stimulation signal to the subject.

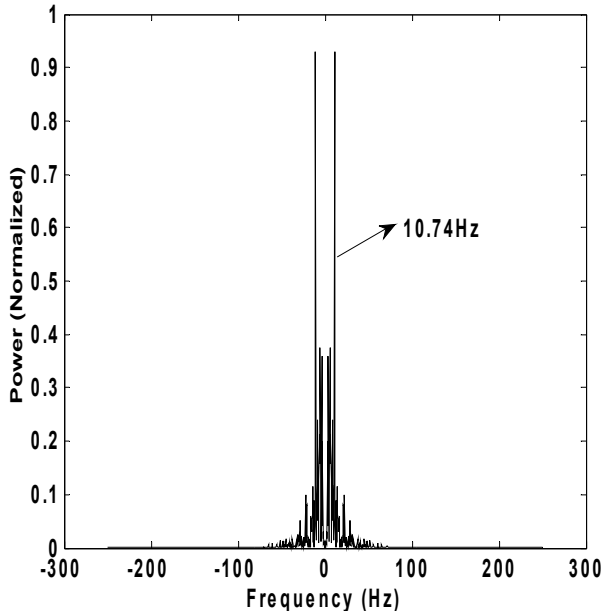


Figure 3.15 : Post-filter frequency spectrum of the EEG data [65].

Pre-filter and post-filter frequency spectrums show the validity of SSVEP study where the subject's brain reacts to the applied flickering light by producing EEG signal at the same frequency of the flickering. That phenomenon is used in brain computer interface applications.

3.4 Comparison of the Filter with Available Literature

Performance summary of the filter circuit in this work and comparison of other published low power filter circuits with a Figure of Merit (FoM) [71], which is described in (3.11), are given in Table 3.3. From the results, it is seen that, DTMOS-based VDTA filter in this work, with a FoM better than [69], [70] and worse than [71] achieves a moderate performance among the filters in Table 3.3. However, it is important to note that the proposed DTMOS-based filter circuit is capable of working under significantly lower supply voltage of ±0.2V than its alternatives and consumes the least power.

$$FoM = \frac{P \times VDD}{n \times f_c \times DR} \tag{3.11}$$

Table 3.3 : Performance summary and comparison of the VDTA filter [65].

Filter	[69]	[70]	[71]	This work
Supply (V)	0.9	2.8	1	±0.2
Power (nW)	262k	230	14.4	12.7
DR (dB)	52	67.5	55	63.7
f_c. (Hz)	1.12k	141	732	19.5
Order, (n)	6	4	4	4
THD (%)	1	5	1	2
FoM (10^{-13})	6632	169	0.89	10.2

To summarize the work in this section, it can be concluded that a DTMOS-based VDTA circuit was proposed. The circuit is capable of working under an ultra low supply voltage ±0.2V and only consuming 5.96nW. DTMOS transistors are used to efficiently exploit shrank voltage headroom. For very low power consumption, the transistors were used in weak inversion where DTMOS transistors are very suitable to this mode of operation due to their well subthreshold slope characteristic.

Using the proposed VDTA circuit, a band-pass filter was designed for EEG data processing. The circuit was used in a fourth order double-tuned pass-band filter. The filter consists of two VDTA cells and two externally connected capacitors. According to PSPICE simulations, both VDTA and the double-tuned filter have performed well. The filter was successfully used to filter out unwanted frequency components of an SSVEP based BCI system's amplifier outputs. Although, in measurements, there was amplifying and filtering integrated in the measurement hardware, there was still a need for additional filtering which is usually done by digital filtering via software. Instead of digital filtering approach, the proposed filter was utilized to investigate its performance in a practical application. It is found that both PSPICE and MATLAB results are in close agreement with theory. The proposed DTMOS-based VDTA circuit is suitable for ultra low-power, ultra low-voltage analog signal processing applications.

4. DTMOS OP-AMP AND MULTIPLIER DESIGNS

In this section, an ultra low voltage ultra low power DTMOS OP-AMP and DTMOS multiplier circuit is described. Those elements are operating in subthreshold region and they are designed for a possible memristor application. Ultra low voltage operation was the main design specification. Therefore, similar to previous designs, only 0.4V supply voltage was used in the designs. These designs here, after some modification in their biasing, were used in the generation of an ultra low voltage memristor element.

4.1 OTA-based DTMOS OP-AMP Design

The designed subthreshold DTMOS OP-AMP is composed of the DTMOS-based OTA [57] and a simple inverter output stage. The topology is very compact and having only 11 MOS transistors. The OP-AMP circuit is shown in Figure 4.1.

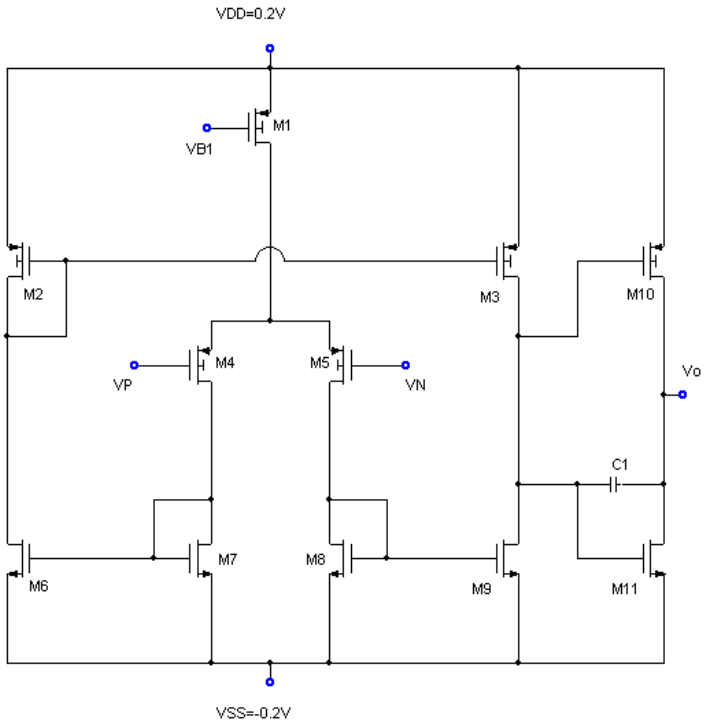


Figure 4.1 : DTMOS-based OP-AMP.

In the circuit in Figure 4.1, M1-M5 and M10 transistors are DTMOS transistors. M1 transistor supplies the biasing current of M4 and M5. M6-M7 and M8-M9 are the current mirror pairs. V_{B1} is the biasing voltage which can be changed to adjust the biasing current of the first OTA stage which mainly determines the performance of the OP-AMP.

Transistor dimensions of the proposed OP-AMP circuit are given in Table 4.1.

Table 4.1 : Transistor dimensions of the proposed OP-AMP.

Transistor	Width	Length
M1, M2, M3	5µm	2µm
M4, M5	300µm	2µm
M7, M8	50µm	5µm
M6, M9	100µm	5µm
M10, M11	400µm	2µm

In the circuit, drain of the M9 transistor is the output of the initial DTMOS OTA stage which has high output impedance where the voltage signal is weak if low resistive loads are connected to the output. However, this node sees the gates of M10 and M11 which are very high impedance inputs. Thus, voltage signal is transferred to the output where M10 and M11 increase load driving capability but the output stage is still incapable of driving low resistive loads and overall circuit behaves a kind of high output impedance circuit. This problem can be solved by applying additional negative feedback, however, this would require more circuitry which increases power consumption. In our application, using the available ultra low-voltage ultra low-power DTMOS OTA stage in [57] for the circuit in Figure 4.1, it was sufficient in our memristor emulating circuit when there is high resistive load connection at the output. C_1 is the Miller compensation capacitor. Choosing 8pF was sufficient for the stability and this value has given 63° phase margin and close to 20kHz unity gain bandwidth when V_{B1} biasing voltage was set to -0.1V. Transistors were operated in the subthreshold region of operation since, in this mode of operation, DTMOS transistors operate with an ideal subthreshold swing of 60mV/dec.

Figure 4.2 shows the voltage transfer characteristic of the operational amplifier when the OP-AMP is loaded with a 100kΩ resistor in an open loop configuration.

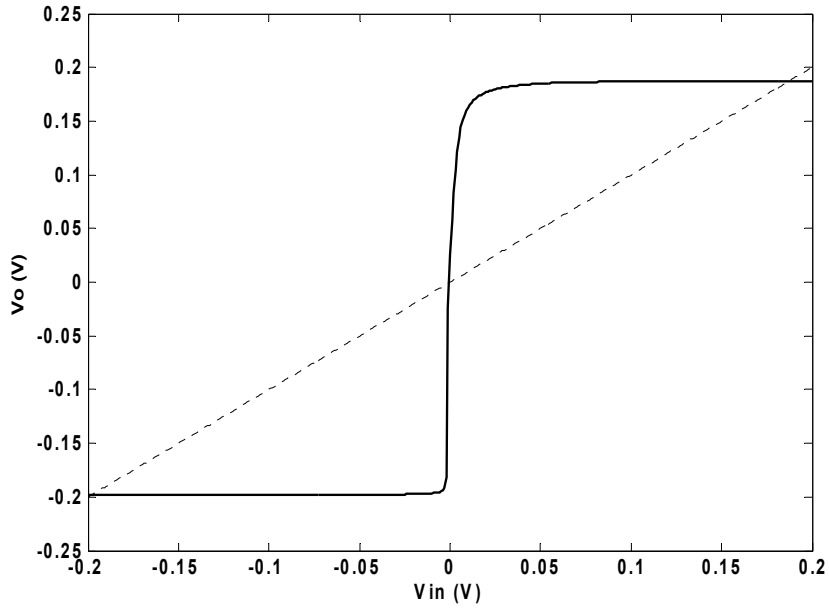


Figure 4.2 : Voltage transfer characteristic of the open-looped OP-AMP.

Input voltage range is depicted in Figure 4.3 when the output is unloaded and the OP-AMP is connected in a unity gain feedback configuration.

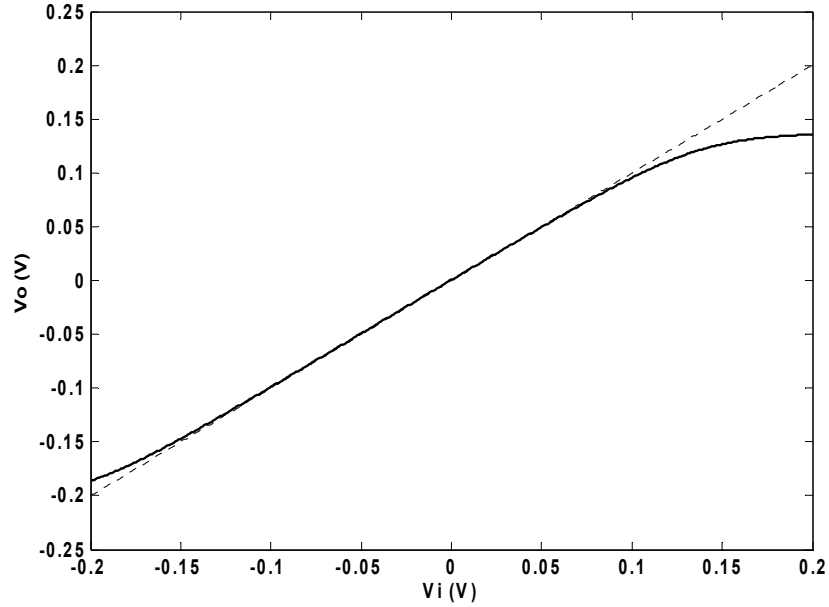


Figure 4.3 : Voltage transfer characteristic of the closed-looped OP-AMP.

AC response of the proposed OP-AMP is illustrated in Figure 4.4 where the OP-AMP is loaded with a 100kΩ resistor in open loop configuration and having 20kHz Unity gain bandwidth (UGBW).

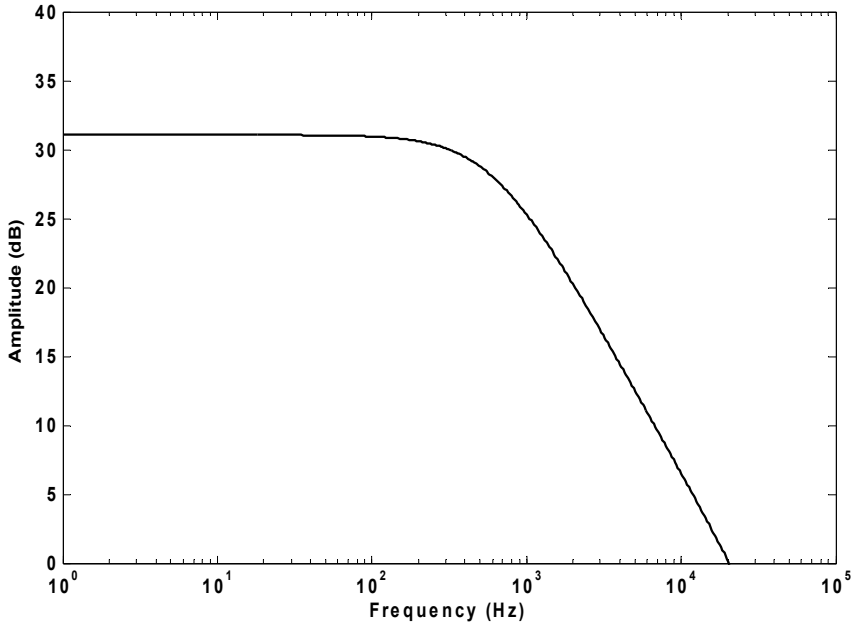


Figure 4.4 : AC characteristic of the OP-AMP.

Sinusoidal response in Figure 4.5 is obtained when the OP-AMP is connected in unloaded unity gain feedback configuration. The input signal is 200mV peak to peak, 1kHz sinus signal.

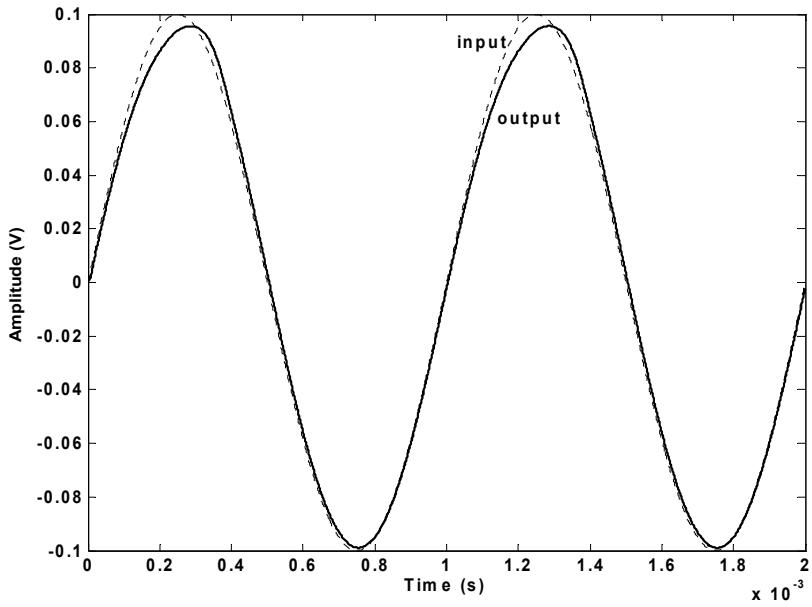


Figure 4.5 : The response of the OP-AMP to sinusoidal input signal.

Figure 4.6 shows the step response of the OP-AMP for a 100mV step input at 1kHz when it is connected as unloaded in a unity gain feedback configuration. Slew Rate (SR) was found as 7V/ms.

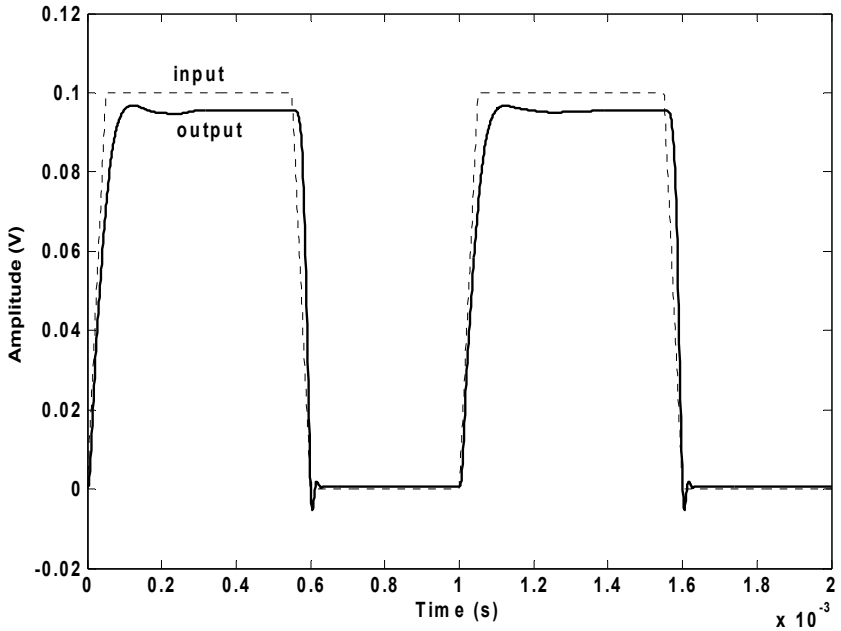


Figure 4.6 : Step response of the OP-AMP.

To further investigate the OP-AMP characteristics, it is used in a Sallen and Key topology. Figure 4.7 is obtained where a zero is effective on the transfer function however, this did not cause any problems in the memristor application.

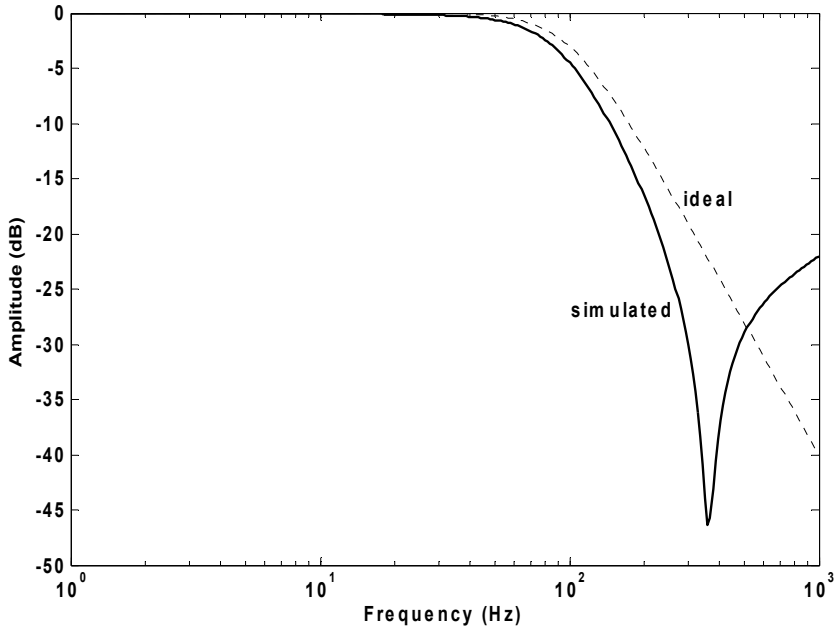


Figure 4.7 : Ideal and simulated responses of a Sallen and Key filter.

Some of the performance metrics of the proposed DTMOS-based OP-AMP are tabulated in Table 4.2.

Table 4.2 : Performance summary of the proposed OP-AMP.

Technology	TSMC 0.18μm
Supply Voltage	±0.2V
Input Voltage Range	-140mV - 80mV
Power Consumption	160nW
Slew Rate (SR)	7V/ms
Unity Gain Bandwidth (UGBW)	20kHz
Phase Margin	67°
Compensation Capacitor	8pF

4.2 DTMOS Multiplier Design

A DTMOS-based four-quadrant multiplier circuit was proposed based on the subthreshold multiplier idea in [72]. Ultra low voltage ultra low power DTMOS multiplier circuit is shown in Figure 4.8. The circuit was supplied by ±0.2V symmetrical power supply. All transistors are operating in the subthreshold region. For ultra low voltage operation, M5-M7 DTMOS transistor were used. To pick up the output current, M8-M9 and M10-M11 current mirror transistors were employed. The overall circuit is consist of only 11 transistors as depicted in the figure. V_{B1} is chosen as the ground reference potential. It is seen from the simulation results, as expected, circuit operates a four-quadrant multiplier circuit. There is slight nonlinearity at X terminal which limits input voltage range.

The circuit consumes just 1.7nW under 0.4V supply voltage and capable of operating in the range of 4kHz which was sufficient for the low frequency memristor application circuit.

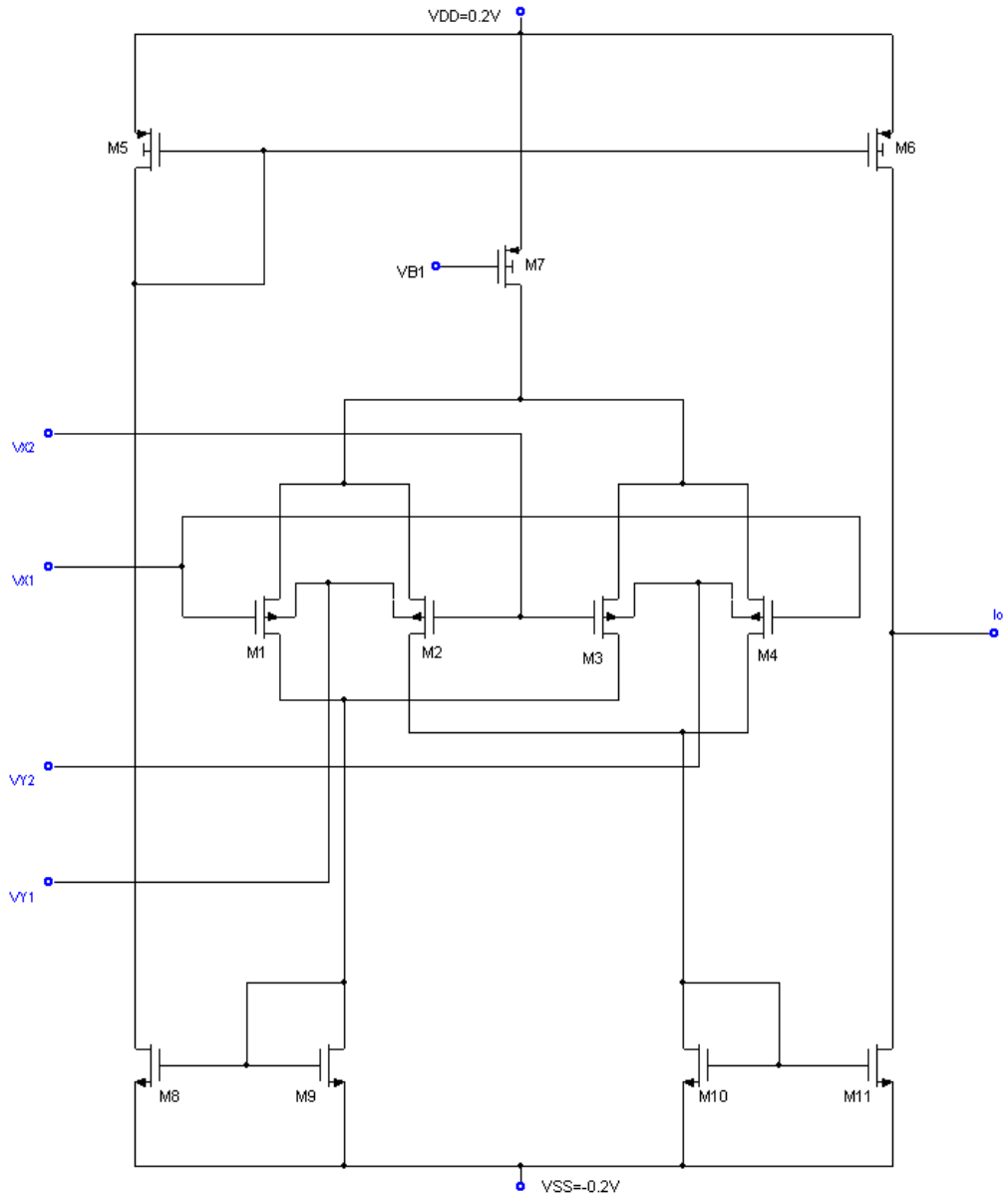


Figure 4.8 : DTMOS-based four-quadrant subthreshold multiplier.

Body terminals of M1-M4 are used for applying the input signal so the circuit can be also thought as a bulk-driven multiplier with additional DTMOS transistors. In fact, the structure is based on classical Gilbert multiplier and gives Gilbert-like multiplication coefficient. Output current can be approximated as

$$i_o = \frac{I_b \kappa (1-\kappa)}{4\phi_t^2} v_x v_y \qquad \textbf{(4.1)}$$

where κ is subthreshold gate-coupling coefficient, ϕ_t is the thermal voltage and I_b is the biasing current flowing over M7 transistor.

Transistor dimensions of the circuit is given in Table 4.3.

Table 4.3 : Transistor dimensions of the proposed multiplier.

Transistor	Width	Length
M1, M2, M3, M4	50µm	2µm
M5, M6	30µm	5µm
M7	4µm	2µm
M8, M9, M10, M11	50µm	5µm

The performance of the proposed DTMOS-based multiplier is investigated by SPICE program and resulting simulations including input voltage ranges, frequency behavior and a modulator application are illustrated in the figures from Figure 4.9 to Figure 4.13, where in Figure 4.13, the frequency of one input has been chosen forty times larger than the other input.

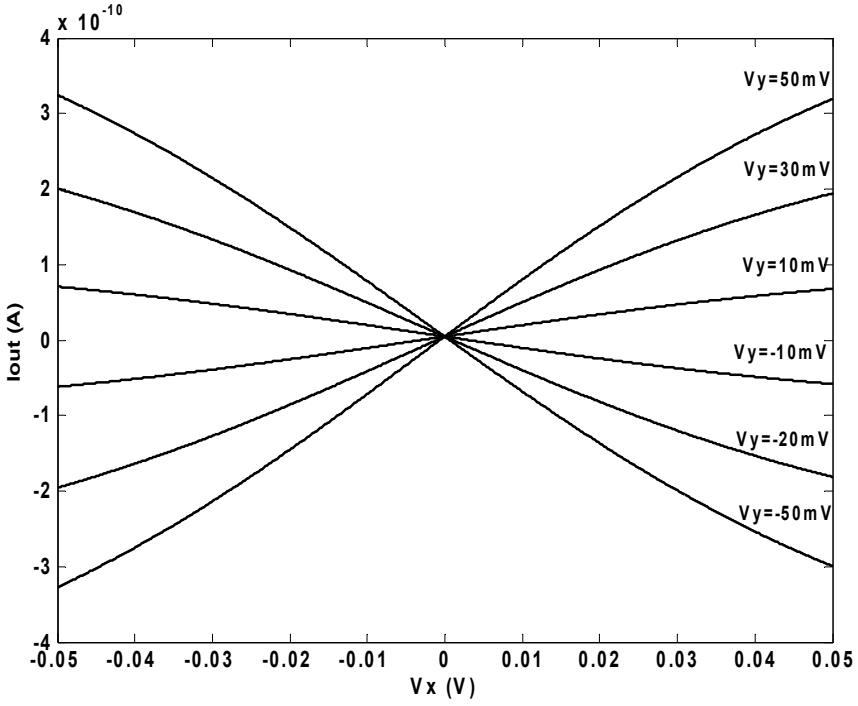


Figure 4.9 : DC characteristics (X terminal) of the proposed multiplier circuit.

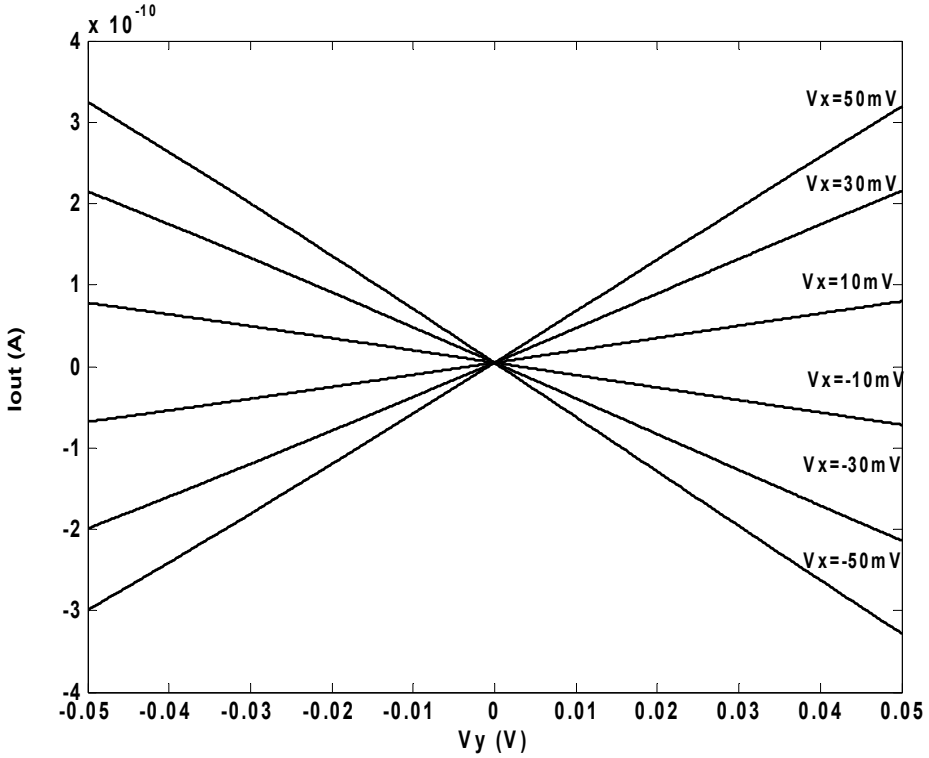


Figure 4.10 : DC characteristics (Y terminal) of the proposed multiplier circuit.

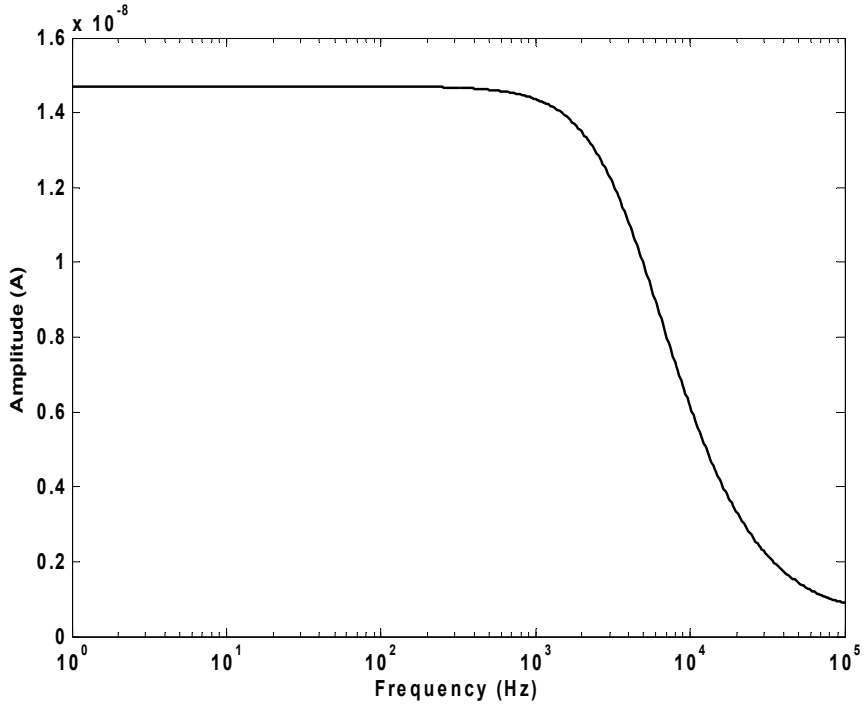


Figure 4.11 : AC characteristic (X terminal) of the proposed multiplier circuit.

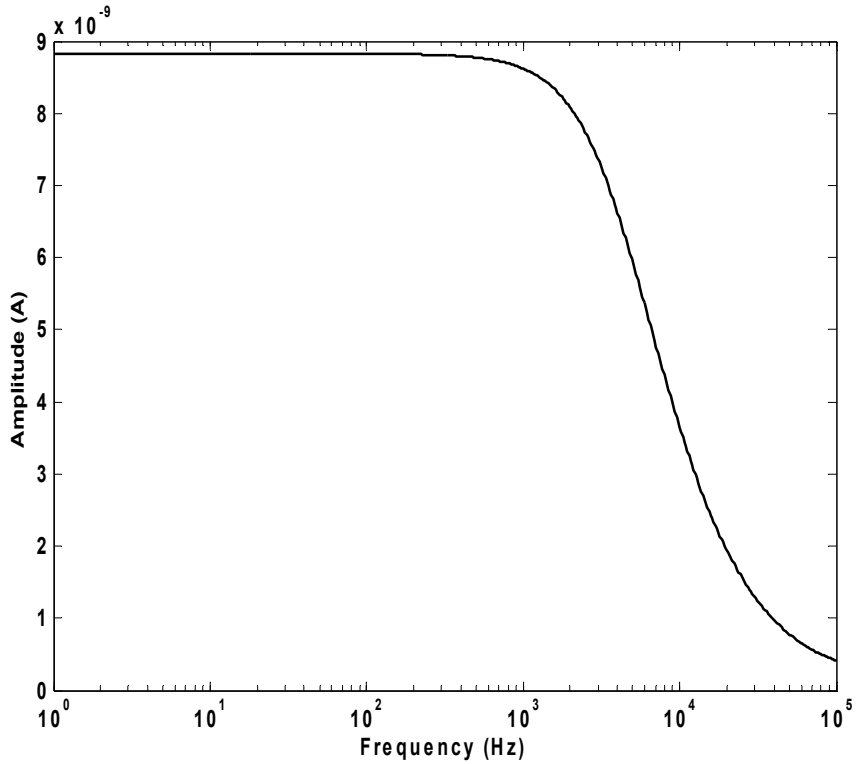


Figure 4.12 : AC characteristic (Y terminal) of the proposed multiplier circuit.

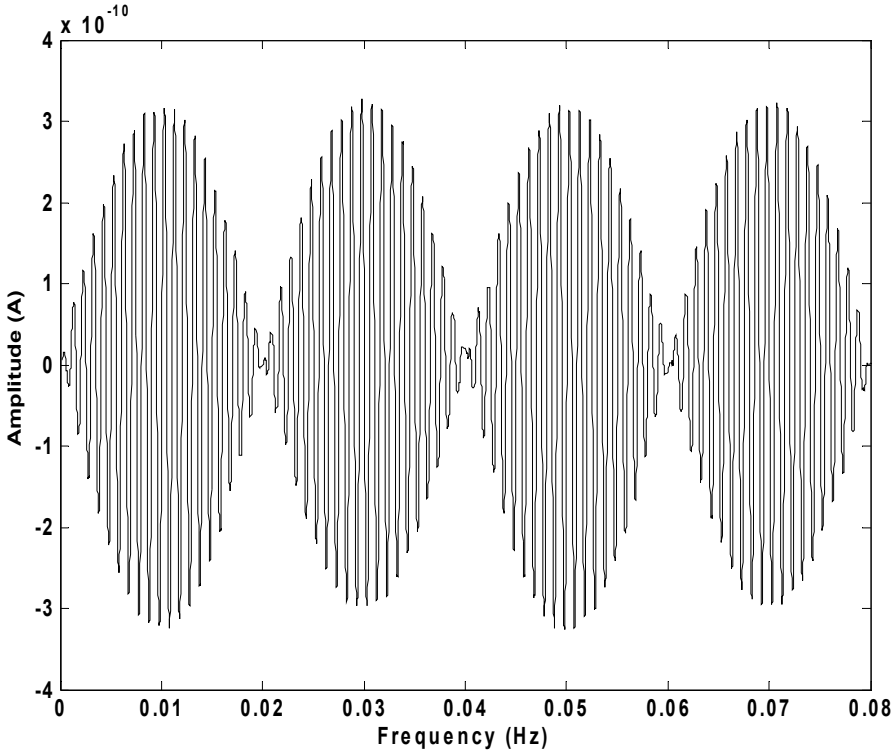


Figure 4.13 : Multiplier response to sinusoidal input for two different frequencies.

4.3 Memristor Application using Op-Amp and Multiplier

The proposed OP-AMP and multiplier circuits here were successfully applied to an ultra low-voltage ultra low power memristor circuit. Since memristor circuit operates in low frequencies, the limited bandwidth of the design did not cause problems. In order to stay in the scope of this study, we do not give the details of the memristor design here.

5. DTMOS CCII DESIGN

In this section, a DTMOS-based ultra low voltage, ultra low power second generation current conveyor has been proposed. The circuit is used in a second order band-pass filter topology which is then applied to an analog hearing aid scheme, as the part of the filter bank within the overall system.

5.1 DTMOS CCII Circuit

Current conveyor circuit is one of most important active blocks of current-mode approach. It is possible to find three different generations of this basic block where the second generation current conveyor (CCII) is the mostly used one. They have attracted much attention with the increasing importance of low power and low voltage circuits [73].

A DTMOS-based CCII circuit is proposed in this study. The transistors are all operating in the subthreshold region. The input stage has been formed by a pseudo-differential low voltage amplifier consisting of M1-M4. The output stage is the class AB stage from [73] with the modification of DTMOS transistor usage for ultra-low voltage operation. M1-M2 and M5,M7 are the PMOS DTMOS transistors. There is feedback in the topology including M6 transistor which helps to decrease the resistance at the X input terminal which should be zero ideally. However, this is very difficult to achieve under subthreshold mode of operation where transistor transconductances are significantly low which severely affects the resistance seen at the X terminal.

The overall circuit is shown in Figure 5.1 where it can be seen that it consists of just eight transistors, thus, the topology is very compact which is a good thing for minimizing the parasitics and low power consumption. The circuit consumes just 214nW while enabling close to MHz range operation.

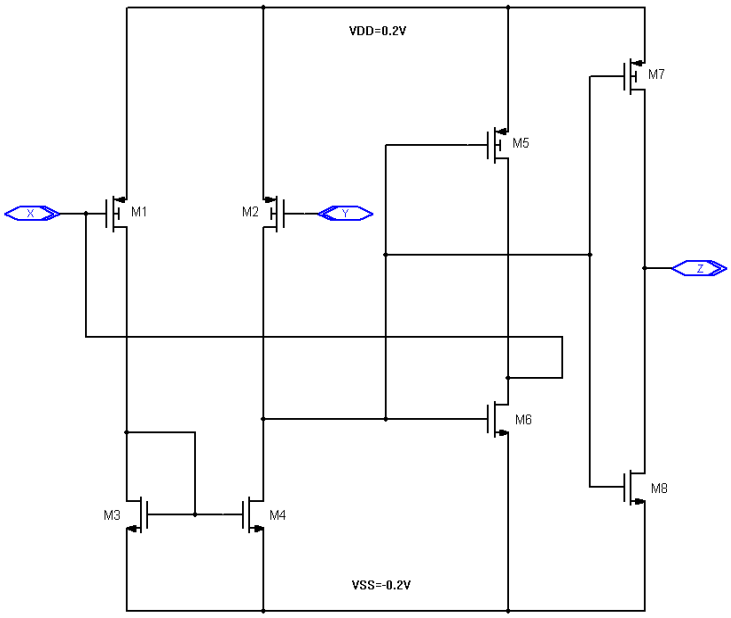


Figure 5.1 : The proposed DTMOS-based subthreshold CCII circuit.

The dimensions of the transistor in the Figure 5.1 are tabulated in Table 5.1. The minimum channel lengths used for DTMOS transistors are 2µm for the support of the model as explained at the introduction section.

Table 5.1 : Transistor dimensions of the proposed CCII.

Transistor	Width	Length
M1, M2	300µm	2µm
M3, M4	50µm	2µm
M5	300µm	2µm
M6	320µm	0.4µm
M7	300µm	2µm
M8	320µm	0.4µm

From Table 5.1, it can be concluded that relatively large transistors are used in the design. They were chosen for correct operation of the circuit under ultra low supply voltage and this is generally the expected case for any MOS circuits operating in the subthreshold region where transistor dimensions have been chosen large to enable targeted current flow under low voltage operation. The circuit was simulated by SPICE. Figure 5.2 shows the input range where the V_X voltage follows V_Y voltage.

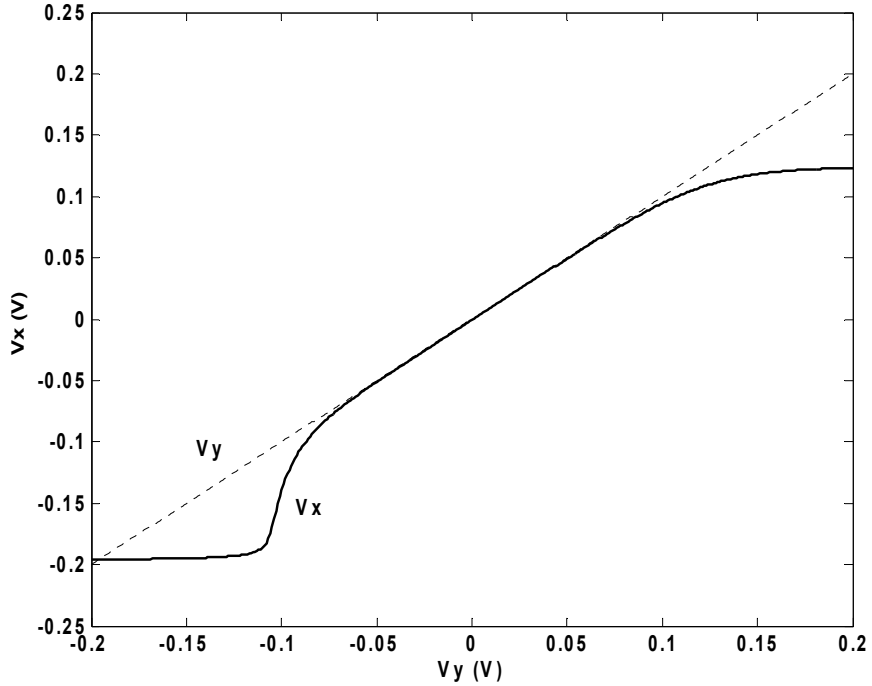


Figure 5.2 : The change of V_X voltage versus V_Y voltage.

In Figure 5.3, the following error of V_X voltage to V_Y voltage is shown where it can be said that input voltage range is ±60mV with small error.

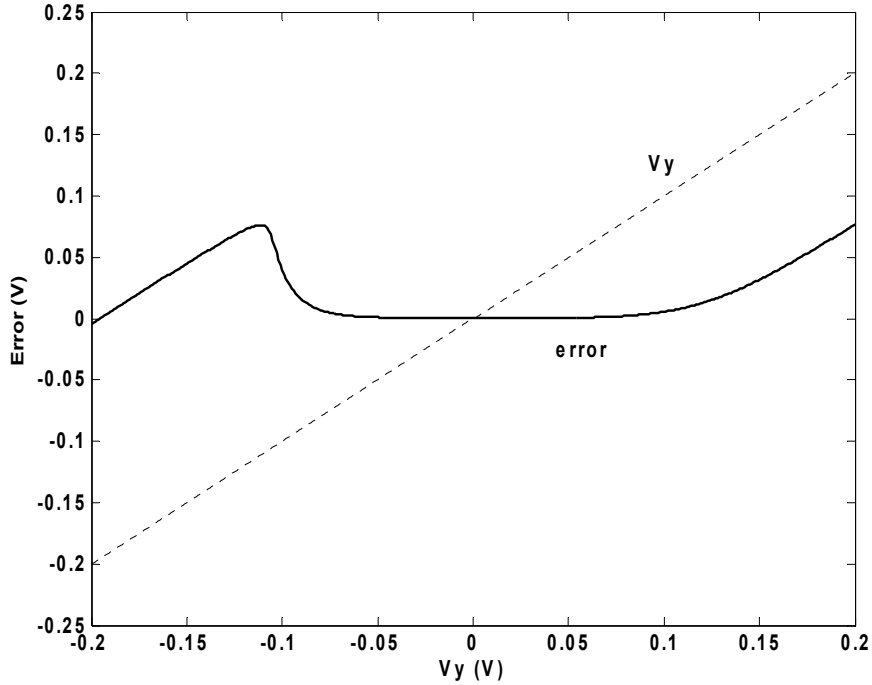


Figure 5.3 : The change of error versus V_Y voltage.

Figure 5.4 depicts the sinusoidal responses obtained by 100mV peak to peak input V_X and V_Y input voltages.

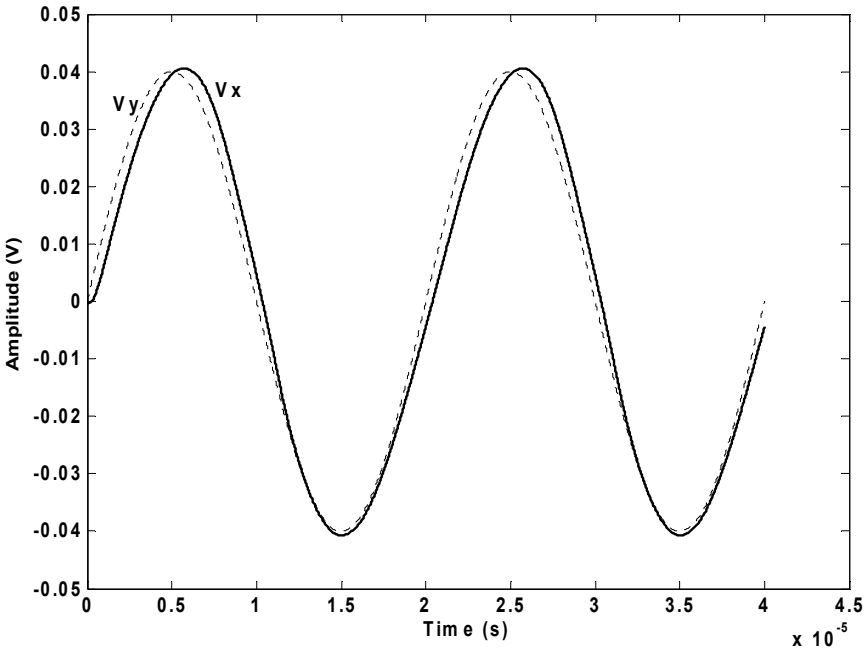


Figure 5.4 : The sinusoidal response of V_X and V_Y voltage.

Figure 5.5 illustrates the voltage change of both V_Z and V_X versus V_Y voltage when both Z and X terminals are loaded with 100kΩ resistances.

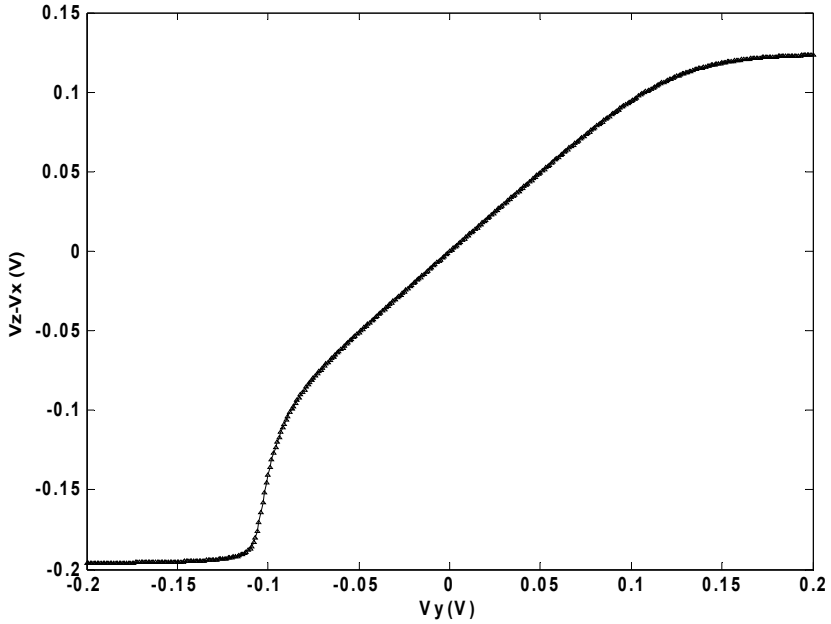


Figure 5.5 : The change of V_Z and V_X versus V_Y voltage.

In Figure 5.6, sinusoidal response of both V_Z and V_X are shown where they are very close in value and AC response of V_X and V_Z has been given in Figure 5.7.

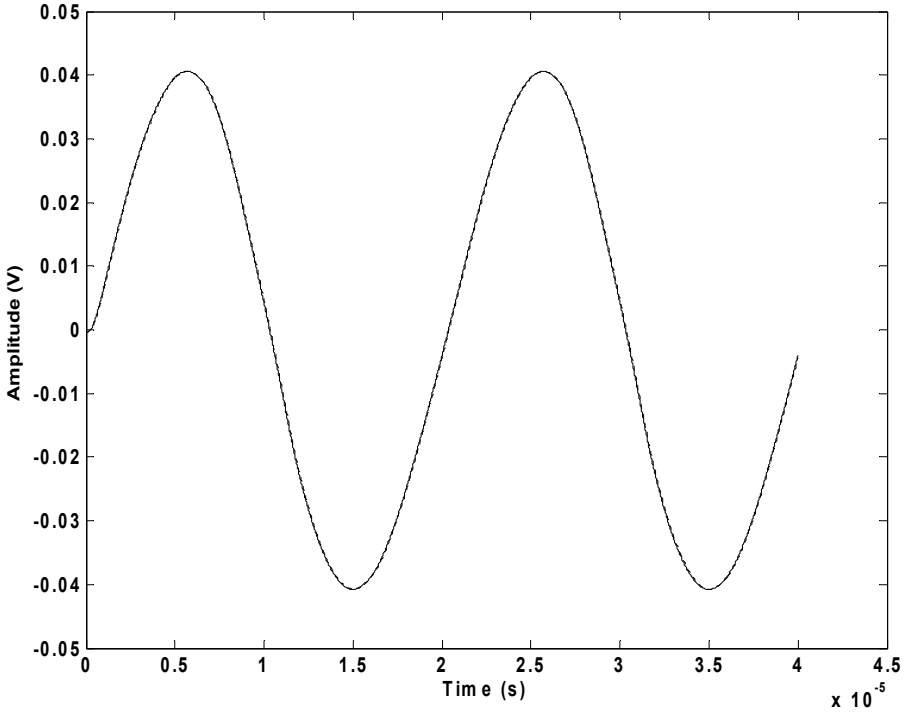


Figure 5.6 : The sinusoidal response of V_X and V_Z voltage.

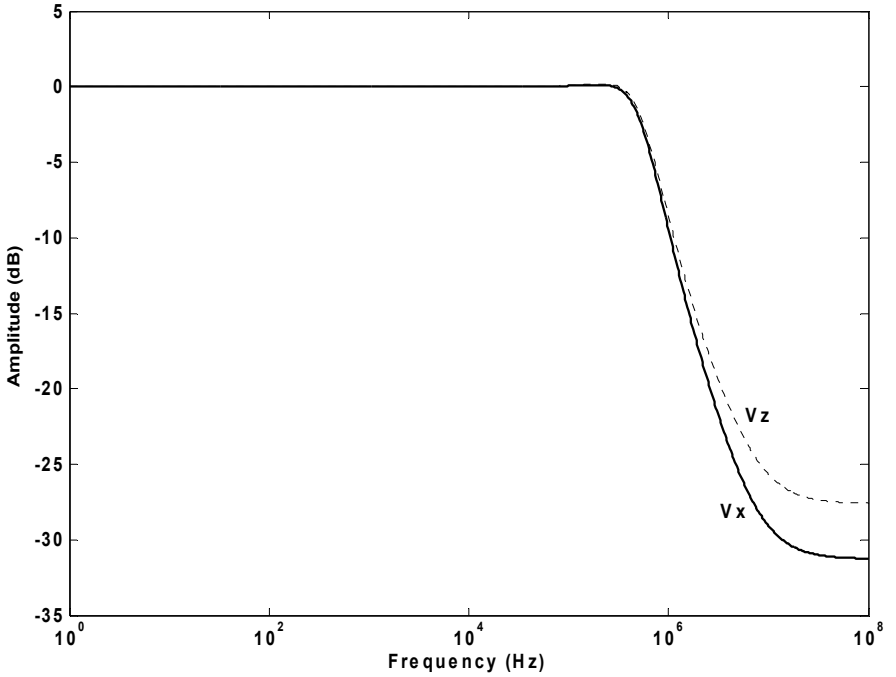


Figure 5.7 : AC response of V_X and V_Z versus frequency.

Some of the simulations results and the performance summary of the proposed CCII are tabulated in Table 5.2.

Table 5.2 : Performance summary of the proposed CCII.

Technology	TSMC 0.18μm
Supply Voltage	±0.2V
Input Voltage Range (V_X-V_Y)	-60mV - +60mV
3dB Bandwidth (V_X,V_Z)	600kHz
Power Consumption	210nW
V_Y resistance@1kHz	11.8MΩ
V_X resistance@1kHz	964Ω
V_Z resistance@1kHz	2MΩ

5.2 CCII-based Band-pass Filter for Speech Processing

The proposed DTMOS-based subthreshold current conveyor was used in a band-pass filter which was proposed by the reference [74]. That filter configuration is shown in Figure 5.8. The reason for choosing a band-pass filter type is that in analog hearing aid systems, there are analog filter banks that consist of band-pass filters [75]. Those filters should be capable of operating at sound frequencies with very little power consumption to save the life of battery as long as possible. The filter circuit employing the proposed CCII was simulated by SPICE program and the Figure 5.9 was obtained when the passive element values of C_1=628pF C_2=628pF, R_1=100kΩ R_2=100kΩ are used.

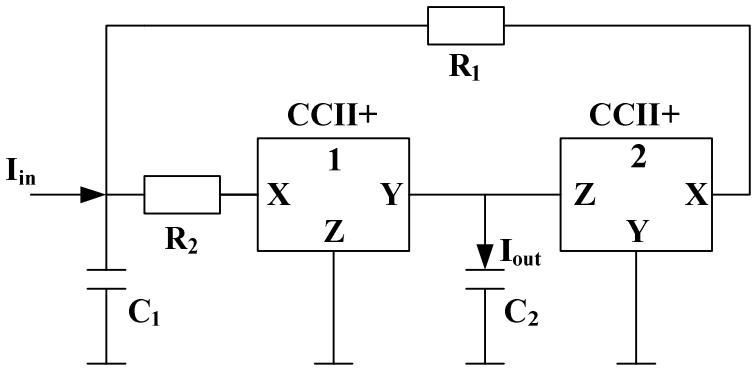


Figure 5.8 : CCII based band-pass filter [74].

The pole frequency and quality factor of the filter was given in (5.1) which was adjusted to show that the circuit behaves close to the ideal response throughout all the sound frequency range and give an example that the filter might be employed in hearing aid filter banks.

$$\omega_p = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad Q_p = \frac{\sqrt{R_1 R_2}}{R_1 + R_2}\sqrt{\frac{C_1}{C_2}} \qquad \textbf{(5.1)}$$

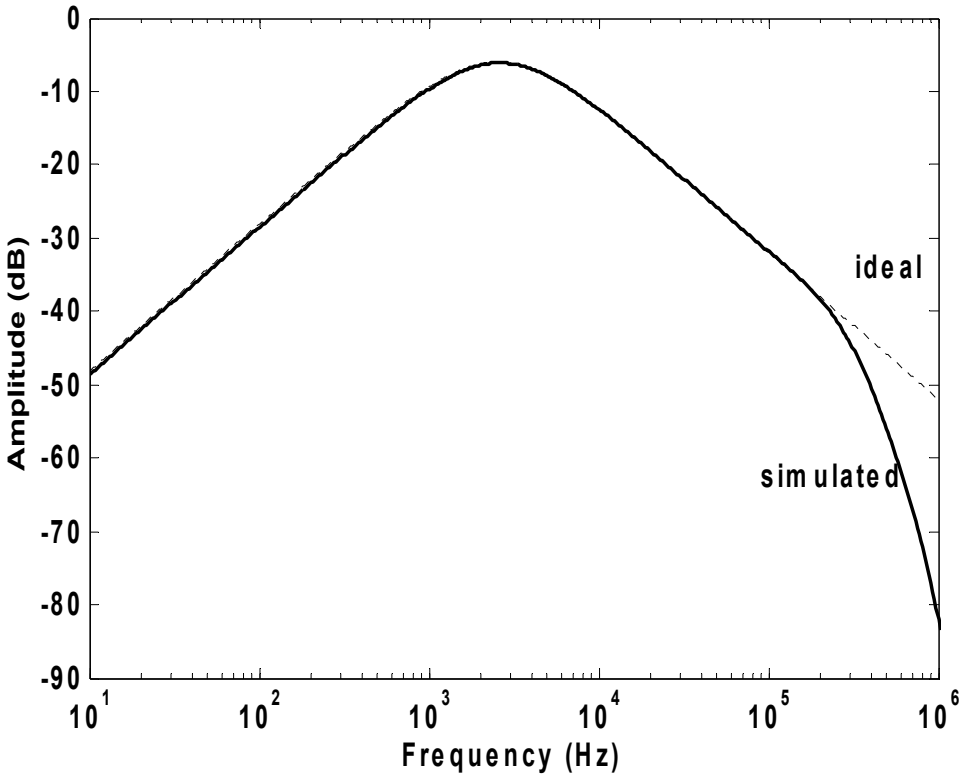


Figure 5.9 : CCII based band-pass filter frequency response.

To further investigate the characteristic of the filter, real human speech signal is applied to SPICE, then ideal and simulated filter responses are compared. Figure 5.10 shows author's speech signal while saying the word "DTMOS".

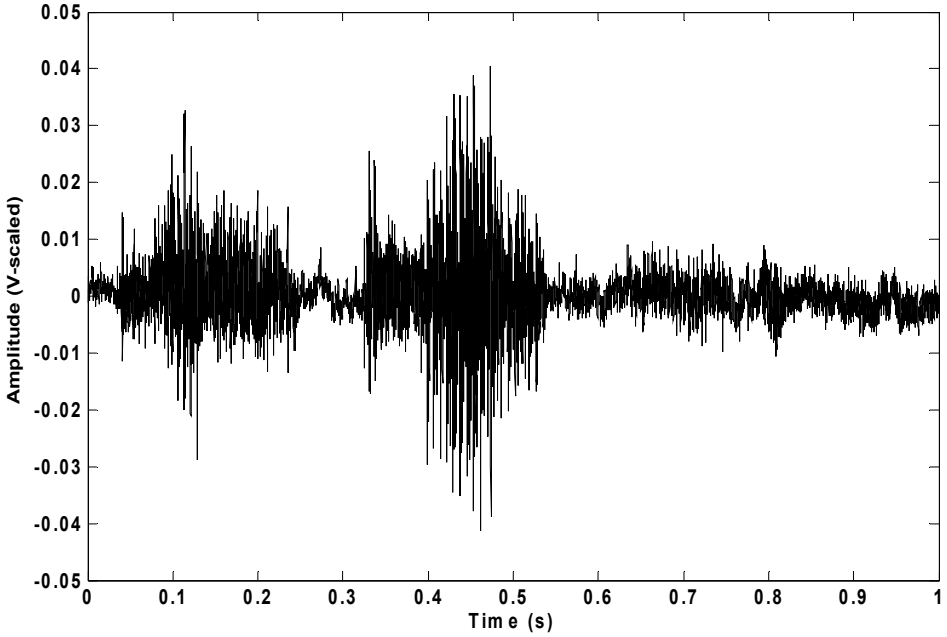


Figure 5.10 : Input speech signal.

For clarity, only some portions of the filter output for ideal and simulated cases have been shown in Figure 5.11 where simulated response is very close to ideal one.

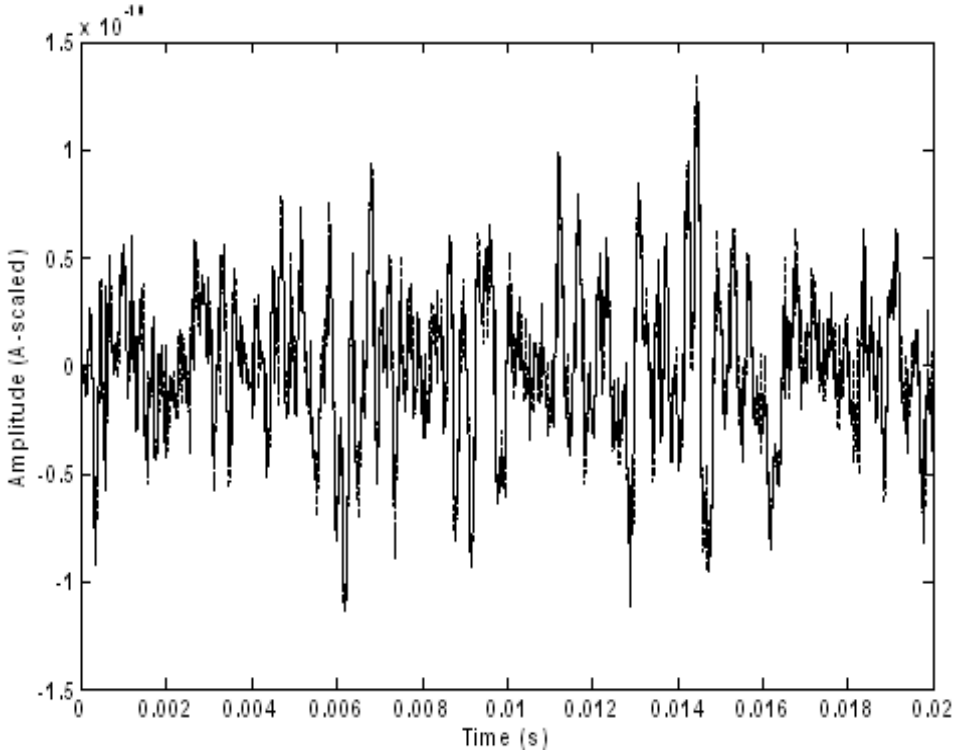


Figure 5.11 : Output ideal and simulated speech signals.

6. MOS-ONLY CIRCUIT WITH DTMOS TUNING

In the literature, there has been an increasing amount of interest on MOS-only circuit design because of its advantageous features [76-80]. MOS-only circuits both eliminate the necessity of connection of additional passive elements and complex circuits requiring high number of transistors. Therefore, high frequency operation is an inherent feature of this design methodology.

6.1 MOS-Only Method

MOS-only method is a very promising approach for analog signal processing applications. Recently, a third-order current-mode high frequency Butterworth low-pass filter has been proposed with using OTAs in g_m-C configuration. The filter cut-off frequency was 200MHz with a power consumption of 16.77mW. However, this topology requires relatively high number of transistors to realize the OTA elements and additional passive capacitances [81].

Instead of conventional g_m-C technique as exemplified in the study [81], it is possible to get similar results with employing less number of transistors, without using additional passive elements and significantly lower power consumption when MOS-only technique is used in the design of third-order current-mode high frequency Butterworth low-pass filters.

In this study, a third order Butterworth current-mode filter is presented using three MOS transistors. Our approach of utilizing the parasitic capacitances of MOS transistors regards gate-to-source capacitances (C_{gs}) as useful, whereas other parasitic capacitances such as drain-to-gate capacitances (C_{gd}) are considered as parasitic. Therefore, the proposed circuits make use of the gate-to-source capacitances and the effect of the other parasitic capacitances is desired to be minimized. The fact that the gate-to-source capacitance of a MOS transistor is usually higher than the other parasitic capacitances is the reason behind this methodology.

We have analyzed the effect of additional transistors to overall transfer function for picking up the output current. Therefore, we have also proposed an enhanced version of MOS-only third order Butterworth filter with an available output current for usage in succeeding stages. A straightforward technique has been utilized to pick up the currents flowing over the MOS transistors by adding additional MOS transistors for this purpose. Their effects on the Butterworth transfer function are also analyzed and an improved version of MOS-only circuit including the effects of these additional transistors is investigated. Moreover, suppressing the effects of non-idealities caused by biasing or other parasitic capacitances, a tuning methodology based on external tuning and Dynamic Threshold MOS (DTMOS) transistor technique is developed. In this tuning technique, bulk terminals of MOS transistors are used to adjust the biasing point of the circuit by changing the threshold voltages of the MOS transistors. This gives the designers more flexibility than conventional tuning methods and allows low voltage operation when several transistors are stacked over each other.

6.2 MOS-Only Third Order Low-pass Butterworth Filter

The proposed MOS-only filter circuit is shown in Figure 6.1. M2 and M3 are NMOS transistors and M1 is chosen as PMOS. Input current signal is applied to the source terminal of M1 transistor while the output signal is flowing over the drain of M2.

AC model of the proposed MOS-only circuit is depicted in Figure 6.2 where only gate to source capacitances and transconductances of MOS transistors are added to the model for simplicity. When the gate-to-source parasitic capacitances are taken into consideration, but the gate-to-drain capacitances not, then the transfer function of this circuit is given as

$$\frac{i_{out}}{i_{in}} = \frac{g_{m1}g_{m2}g_{m3}}{(g_{m1}+sC_{gs1})(s^2C_{gs3}C_{gs2}+sC_{gs3}g_{m2}+g_{m2}g_{m3})} \qquad \textbf{(6.1)}$$

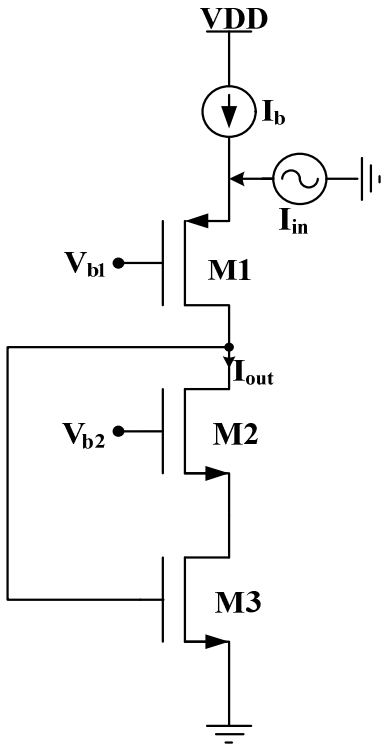


Figure 6.1 : The proposed MOS-only circuit.

The equation (6.1) can be rewritten as

$$\frac{i_{out}}{i_{in}} = \frac{1}{s^3 \frac{C_{gs1}C_{gs2}C_{gs3}}{g_{m1}g_{m2}g_{m3}} + s^2\left(\frac{C_{gs1}C_{gs3}}{g_{m1}g_{m3}} + \frac{C_{gs2}C_{gs3}}{g_{m2}g_{m3}}\right) + s\left(\frac{C_{gs1}}{g_{m1}} + \frac{C_{gs3}}{g_{m3}}\right) + 1} \tag{6.2}$$

The equation in (6.2) becomes a third order low-pass Butterworth filter transfer function when following equalities are satisfied. Thus, under the conditions in (6.3), it is possible to get a third order Butterworth filter only using three MOS transistors when the biasing transistors are neglected.

$$\frac{g_{m1}}{C_{gs1}} = \frac{g_{m2}}{C_{gs2}} = \frac{g_{m3}}{C_{gs3}} \tag{6.3}$$

In this technique, gate to drain capacitances of MOS transistors become undesired parasitic capacitances which deteriorate the ideal transfer function in (6.2). When their affects are added to the transfer function, it becomes

$$\frac{i_{out}}{i_{in}} = \frac{g_{m1}g_{m2}(g_{m3} - sC_{gd3})}{(g_1 + sC_{gs1}).\Delta} \tag{6.4}$$

where

$$\Delta = s^2(C_{gs2}C_{gs3} + C_{gs2}C_{gd1} + C_{gs2}C_{gd2} + C_{gs2}C_{gd3} + C_{gs3}C_{gd3} + C_{gd3}C_{gd1} + C_{gd3}C_{gd2}) + s(g_{m3}C_{gd3} + g_{m2}C_{gs3} + g_{m2}C_{gd1} + g_{m2}C_{gd2}) + g_{m2}g_{m3} \quad \textbf{(6.5)}$$

When gate to drain capacitances are neglected, the equation reduces to its definition in (6.2) as expected. The numerator of the non-ideal transfer function in (6.4) shows that there is a right hand plane zero at

$$f_o = \frac{g_{m3}}{2\pi C_{gd3}} \quad \textbf{(6.6)}$$

This right hand plane zero adds more phase shift to the Bode plot of the circuit and might be a problem for the stability of the circuit unless it is moved to very high frequencies. This is the chosen method in our design to alleviate its effect by properly adjusting the biasing and transistor aspect ratios which affect the value of parasitic gate to drain capacitances. Additional elements might be added to the circuit to move the zero to the left half plane or even to cancel the poles. However, this is not a robust solution and does not guarantee the pole zero cancelation whenever any variation occurs in the circuit such as process variations, temperature, etc. Moreover, the realization of these elements leads to additional parasitics.

$$f_{3dB_{ideal}} = \frac{g_m}{2\pi C_{gs}} \quad \textbf{(6.7)}$$

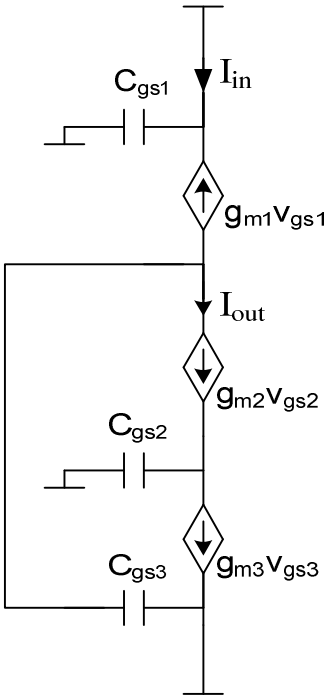


Figure 6.2 : The AC model of the proposed MOS-only circuit.

The equality of ideal 3dB pole frequency in (6.7) shows that cut-off frequency is proportional to the transconductances and gate to source capacitances of transistors. High frequency operation is possible when C_{gs} capacitances and transconductances are adjusted accordingly since the topology requires very small number of transistors contrary to a realization based on active analog building blocks such as op-amps, OTAs, etc. It is useful to note that the transconductance of a MOS transistor, as given in (6.8), is proportional to its width length ratio which also affects gate to source capacitance (6.9), so the designer should be careful while adjusting their values to determine the circuits both biasing and operation frequency for proper operation. In (6.9), gate source capacitance is given when the transistor is in saturation mode of operation where C_{ov} is the overlap capacitance and C_{ox} is the oxide capacitance.

$$g_m = \sqrt{2kI_d \frac{W}{L}} \tag{6.8}$$

$$C_{gs} = WLC_{ov} + \frac{2}{3}WLC_{ox} \tag{6.9}$$

6.3 Improved MOS-Only Circuit

One thing should be resolved for the circuit in Figure 6.1 is that the output current is flowing over the transistor M2. This current should be picked by a mechanism which does not affect the overall Butterworth transfer function. This method additionally should consider proper biasing of overall circuit and it should not deteriorate the frequency behavior of the circuit when high frequency operation is required. Furthermore, parasitics from the additional circuitry should be kept to a minimum. Considering aforementioned specifications, the improved circuit is shown as in Figure 6.3.

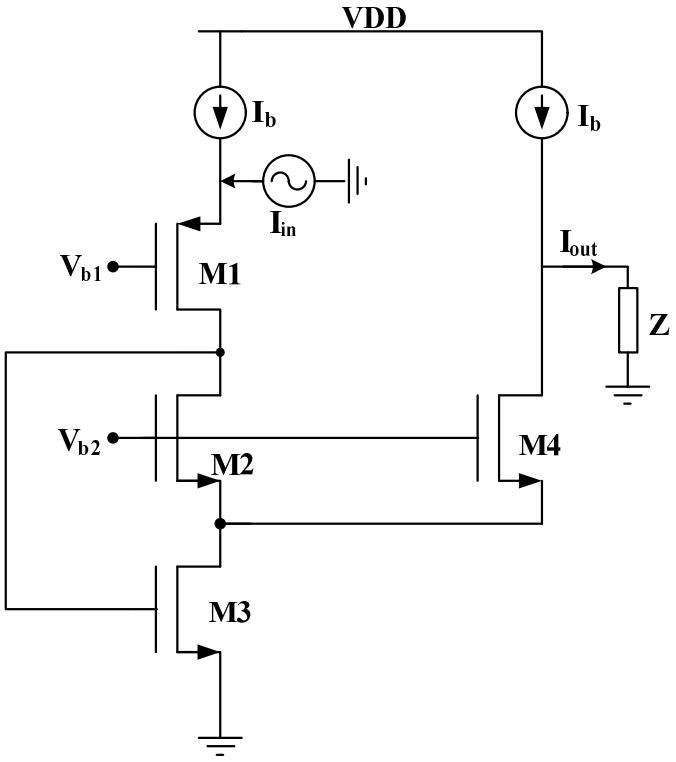


Figure 6.3 : The proposed overall MOS-only circuit.

The transfer function of the improved MOS-only circuit can be given as in (6.10) when its AC model in Figure 6.4 is analyzed. The circuit in Figure 6.3 satisfies third order Butterworth transfer function with new design equalities given in (6.14).

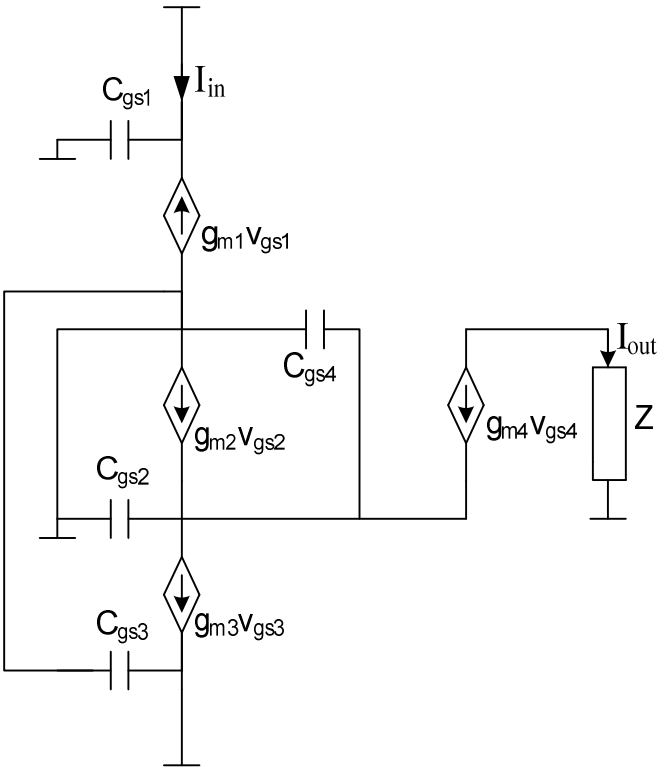


Figure 6.4 : The AC model of the improved MOS-only circuit.

$$\frac{i_{out}}{i_{in}} = -\frac{g_{m1}g_{m3}g_{m4}}{(g_{m1}+sC_{gs1})[s^2C_{gs3}C_T + sC_{gs3}g_{m4}(a+1) + ag_{m4}g_{m3}]} \qquad \textbf{(6.10)}$$

In equation (6.10), C_T shows the total equivalent gate to source capacitance between the gate and source of M2 and M4 transistors which is equal to $C_{gs2}//C_{gs4}$. The coefficient *a,* is defined by the ratio of the transconductances of M2 transistor to M4 transistor. Under the same biasing conditions and same transistor dimensions, these two capacitances become approximately same. Additionally, when M2 and M4 transconductances are chosen equal, these two variables, C_T and *a* become

$$C_T = 2C_{gs2} \quad , \quad g_{m2} = g_{m4} \Rightarrow a = 1 \qquad \textbf{(6.11)}$$

After substituting these values into (6.10), transfer function becomes

$$\frac{i_{out}}{i_{in}} = -\frac{g_{m1}g_{m2}g_{m3}}{(g_{m1}+sC_{gs1})[s^2 2C_{gs2}C_{gs3} + s2C_{gs3}g_{m2} + g_{m2}g_{m3}]} \qquad \textbf{(6.12)}$$

which can be rewritten as

$$\frac{i_{out}}{i_{in}} = -\frac{1}{s^3 \frac{2C_{gs1}C_{gs2}C_{gs3}}{g_{m1}g_{m2}g_{m3}} + s^2\left(\frac{2C_{gs1}C_{gs3}}{g_{m1}g_{m3}} + \frac{2C_{gs2}C_{gs3}}{g_{m2}g_{m3}}\right) + s\left(\frac{C_{gs1}}{g_{m1}} + \frac{2C_{gs3}}{g_{m3}}\right) + 1} \quad \textbf{(6.13)}$$

To get a third order Butterworth response, new design equalities should be chosen as in (6.14)

$$\frac{g_{m1}}{C_{gs1}} = \frac{g_{m2}}{C_{gs2}} = \frac{2g_{m3}}{C_{gs3}}, \quad g_{m2} = g_{m4}, \quad C_{gs2} = C_{gs4} \quad \textbf{(6.14)}$$

when parasitic Cgd capacitances are taken into consideration, non-ideal transfer function becomes

$$\frac{i_{out}}{i_{in}} = \frac{-g_{m1}g_{m2}(g_{m3} - sC_{gd3})}{(g_1 + sC_{gs1})(1 + sC_{gd4}Z).\Phi} \quad \textbf{(6.15)}$$

where Z is the load impedance and Φ is given as

$$\Phi = [s^2(2C_{gs3}C_{gs2} + 2C_{gd1}C_{gs2} + 2C_{gd2}C_{gs2} + C_{gd3}(C_{gs3} + C_{gd1} + C_{gd2} + 2C_{gs2})) + s(2C_{gs3}g_{m2} + 2C_{gd1}g_{m2} + 2C_{gd2}g_{m2} + C_{gd3}(g_{m2} + g_{m3})) + g_{m2}g_{m3}] \quad \textbf{(6.16)}$$

6.4 Overall MOS-Only Filter Circuit with DTMOS Tuning

As it is seen from the non-ideal transfer function in (6.15), there is an additional pole coming from the gate to drain capacitance of M4 transistor and the Z load impedance. Usually the gate to drain capacitances significantly is lower than gate to source capacitances. When their effects are neglected, that is $C_{gd} << C_{gs}$, the transfer function in (6.15) reduces to the ideal function. However, another important point to be pointed out that the current sources in circuits are not ideal. Thus, their gate to source capacitances will also affect the circuit. Similarly, the effects coming from transistors forming biasing voltages should also be considered but adding all the secondary effects in hand calculations become tediously complicated. Therefore following complete circuit in Figure 6.5 is formed for further investigations in simulations with real current sources and biasing voltages.

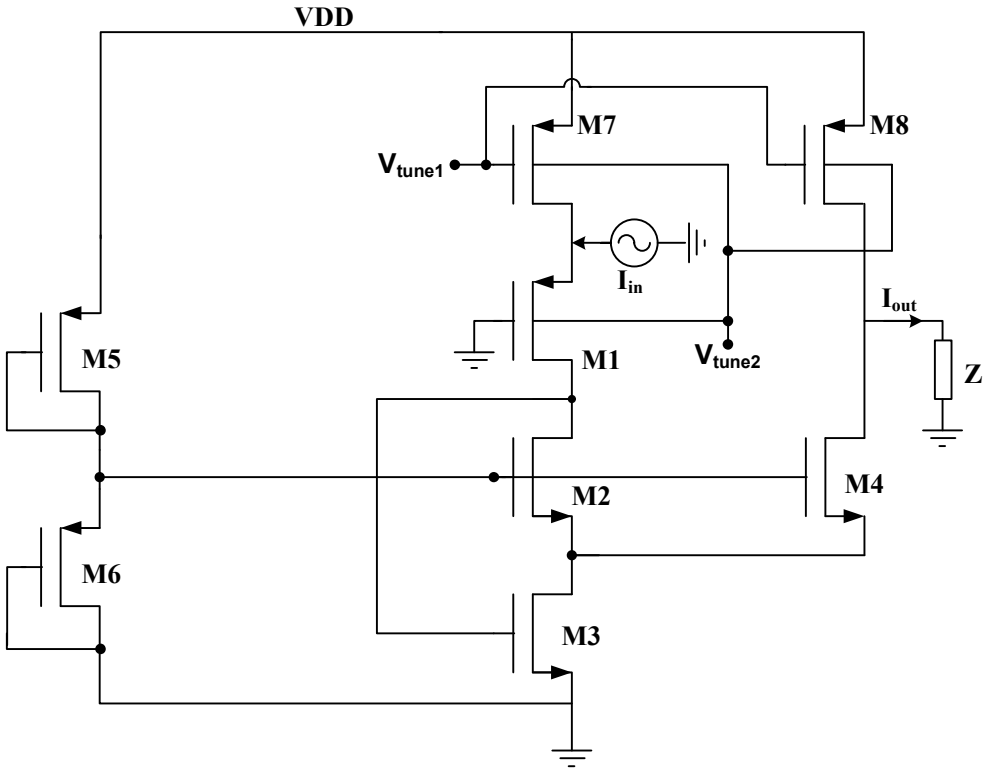


Figure 6.5 : The complete MOS-only circuit with DTMOS tuning technique.

In Figure 6.5, M5 and M6 transistors are diode connected transistors to generate desired biasing voltage at the gate of M2 transistor. M7 and M8 are current sources supplying biasing current over the core MOS-only circuit part. V_{tune1} and V_{tune2} are off-chip tuning voltages. These are used to compensate the change of the circuit's center frequency due to non-idealities. However, in the topology, four MOS transistors are stacked over which limits the biasing options of designer because of the supply voltage limits of modern low power analog circuits. For proper tuning in the circuit, DTMOS technique based on additional off-chip tuning voltage is utilized.

In simulations, TSMC 0.18µm n-well process technology parameters are used in SPICE program to model the transistors. V_{tune1} voltage is set to 0.6V while the maximum forward body bias of PMOS transistors M1, M7, M8 is 0.4V to employ DTMOS technique in off-chip tuning methodology.

The power consumption of the circuit is 0.69mW when I_b biasing currents are set to 186.5µA after DTMOS tuning. The ideal cut-off frequency of the filter is found as 228MHz.

The ideal and simulated responses of proposed third order Butterworth MOS-only filter are given in Figure 6.6 when the output is loaded with a 10pF capacitor which

is a typical load for the operating frequency. Figure 6.7 shows the sinusoidal response of the ideal and the simulated responses at 100MHz. Ideal and simulated responses are opposite in phase but direction of the output current is taken inside in order to compare the ideal and simulated characteristics more closely. There is small magnitude loss at the simulated characteristic which is a result of the biasing conditions. These conditions are closely related with the filter results especially when high frequency operation is an aimed specification.

To investigate the effects of process variations (W, L, V_{TO}, t_{ox}) on the proposed circuit, Monte Carlo simulations are additionally performed by using SPICE program and resulting magnitude and sinusoidal response figures are shown in Figure 6.8 and Figure 6.9 respectively.

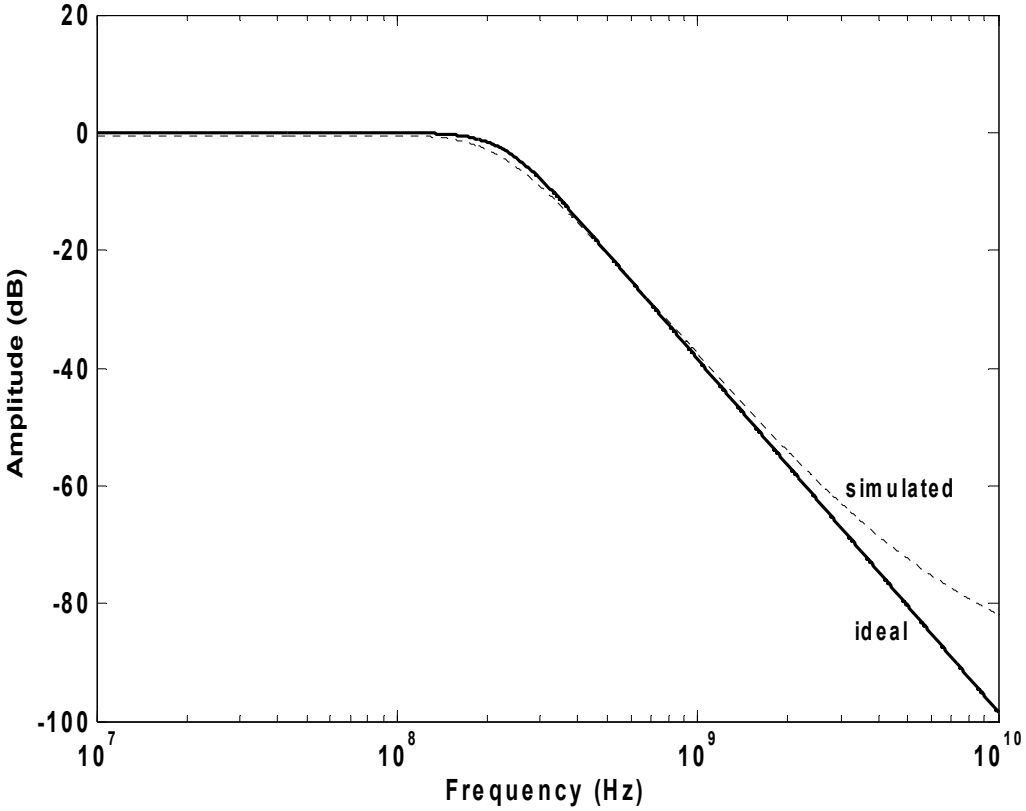


Figure 6.6 : Ideal and simulated filter magnitude response.

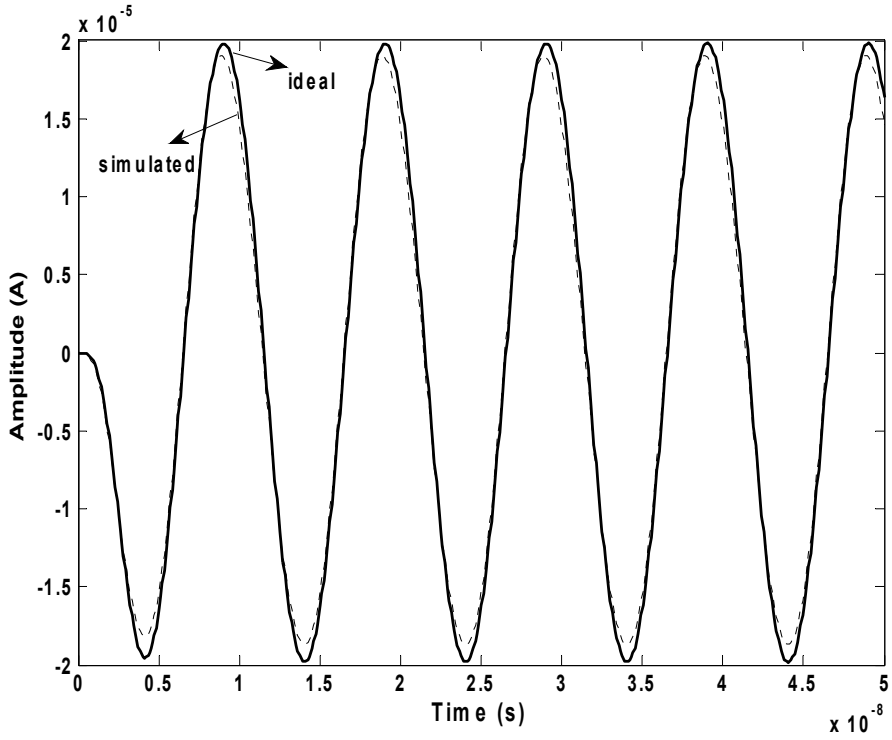


Figure 6.7 : Ideal and simulated filter sinusoidal responses at 100MHz.

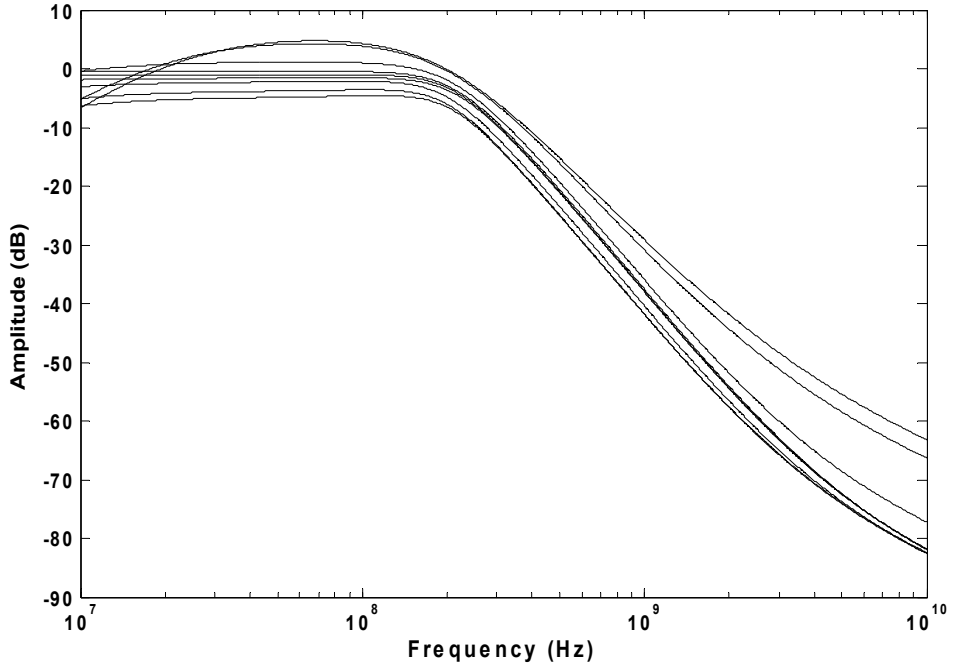


Figure 6.8 : Monte Carlo simulation for the magnitude response.

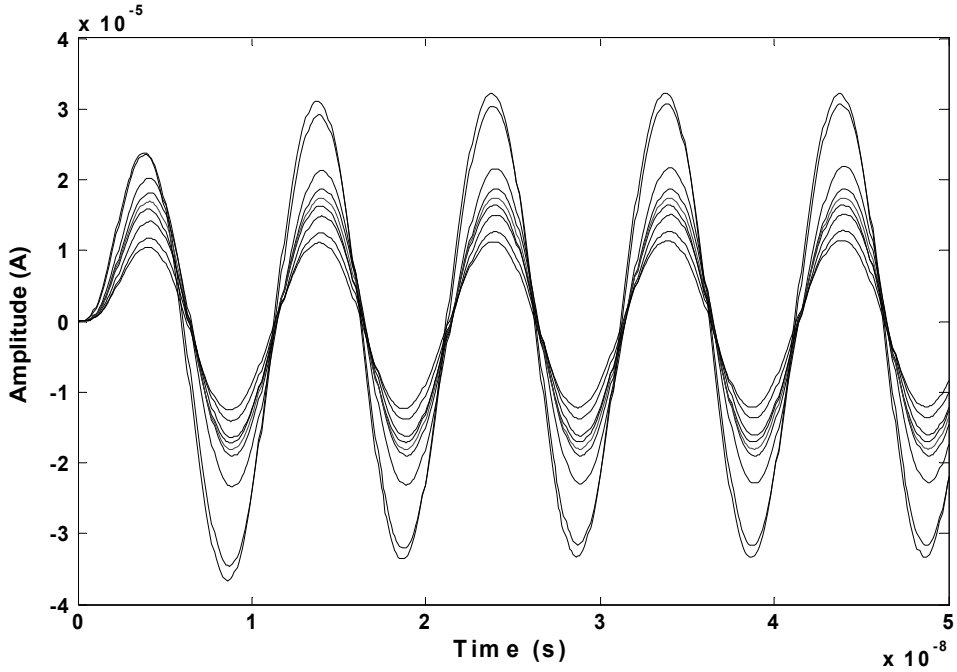


Figure 6.9 : Monte Carlo simulation for the sinusoidal response.

From Monte Carlo simulations, it is seen that there are some situations where variations are relatively high but usually the variations are in acceptable limits.

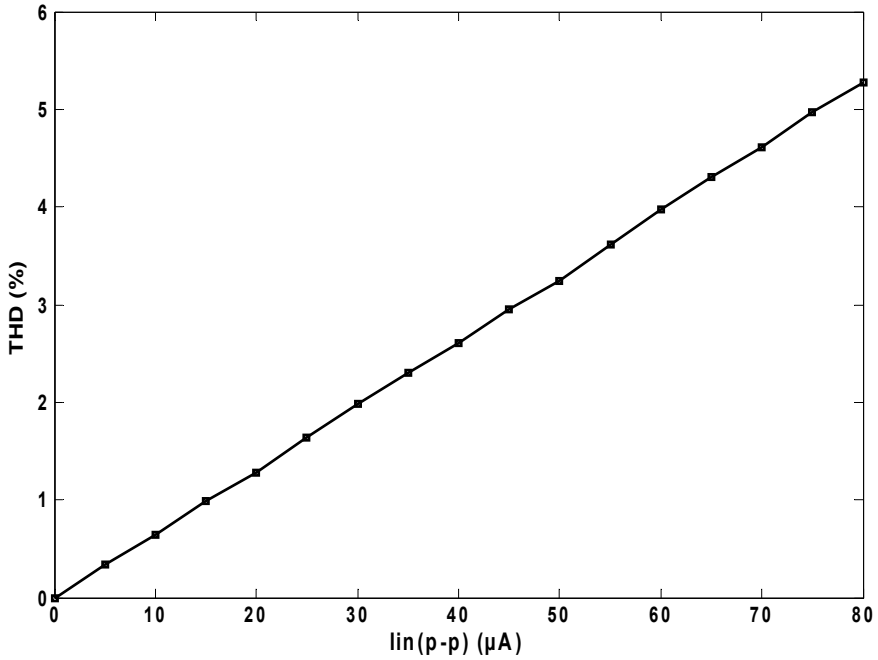


Figure 6.10 : Total harmonic distortion of the proposed filter.

Total harmonic distortion of the circuit is illustrated in Figure 6.10 which shows the THD for a peak to peak input current signal at 100MHz.

The dimensions of the transistors in Figure 6.5 are tabulated in Table 6.1.

Table 6.1 : Transistor dimensions.

Transistors	**Width (µm)**	**Length (µm)**
M1	30	1.5
M2, M4	168	2
M3	238	1.4
M5	4	4
M6, M7, M8	20	2

7. CONCLUSION

In conclusion, DTMOS-based active building blocks have been designed in this study. The designs are mainly focused on ultra low power consumption due to the usage of ultra low supply voltage of even less than 0.5V, which leads the transistors to operate in subthreshold region where DTMOS transistors having ideal subthreshold swings.

DTMOS-based OTA, VDTA, OP-AMP, multiplier, CCII are some of the active blocks that are designed in this study for ultra low power applications. The channel lengths of all DTMOS transistors were chosen 2μm to be in agreement of the models used here and to prevent short channel effects.

Additionally, a third order low-pass Butterworth filter for high frequency applications are proposed in this study. MOS-only technique has been used to get a filter circuit with small number of transistors, low power consumption and requiring no additional passive elements. To alleviate the deviation from ideal case caused by parasitics, A DTMOS technique-based tuning methodology has been developed. Results show that the proposed circuit is capable of operation at high frequencies with consuming low power.

The performance of all proposed circuits are confirmed with SPICE program with detailed simulations. Theoretical calculations are found in good agreement with simulation results.

7.1 Results and Importance of the Study

This study, as far as the author's knowledge, first applies the DTMOS approach to EEG processing successfully where the operation frequency is low so limited bandwidths due to subthreshold operation, no longer become a problems. Such circuits proposed here are required designs, especially, for wireless EEG devices. Additionally, the performance of the proposed designs here have been investigated by real life measurements practically by various signal processing ways.

DTMOS transistor with its unique qualifications becomes a very suitable device for low-power, especially subthreshold designs. In addition to its several interesting features, bulk terminal plays the role of a second gate and increases the control over the channel. Bulk terminal can also be used as the fourth terminal of the transistor which leads to interesting applications as in the proposed MOS-only filter circuit where it increases the tuning range. Actually, the DTMOS tuning in third order Butterworth filter, not only increases the tuning range but also it enables the circuit to flow high currents by decreasing the threshold voltage of PMOS transistors and leads to a unique biasing scheme for the cascode stage.

Another important result, to be finally mentioned here for the presented dissertation study is that all of the proposed active building blocks lead to both compact and ultra low power consuming circuits which can be applied to numerous application subjects in low power analog circuits.

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List of Publications:

[1] **Uygur, A., Kuntman, H**. (2007). Seventh order elliptic video filter with 0.1dB pass band ripple employed CMOS CDTAs. *International Journal of Electronics and Communications AEÜ*, *61*, 320-328.

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PUBLICATIONS/PRESENTATIONS ON THE THESIS

[1] **Uygur, A., Kuntman, H**. (2013). 0.4V OTA design using DTMOS transistors for EEG data processing, *IEEE 21th Signal Processing and Communications Applications Conference (SIU)*, Girne, TRNC, 1-4.

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