ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN EXAMPLES FOR SECOND GENERATION CURRENT CONTROLLED CURRENT CONVEYORS AND THEIR APPLICATIONS IN 28nm PROCESS

M.Sc. THESIS

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Electronics Engineering Programme

Thesis Advisor: Prof. Dr. Hakan KUNTMAN

JANUARY 2013

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

28 nm PROSESİNDE ÖRNEK İKİNCİ KUŞAK AKIM KONTROLLÜ AKIM TAŞIYICI YAPILARI TASARIMI VE UYGULAMALARI

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To my beloved family,

FOREWORD

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ABBREVIATIONS

CCII	**:** Second Generation Current Conveyor
CCCII	**:** Second Generation Current Controlled Current Conveyor
GPS	**:** Global Positioning System
GNSS	**:** Global Navigation Satellite System
ADC	**:** Analog to Digital Converter
DAC	**:** Digital to Analog Converter
FHSS	**:** Frequency Hopping Spread Spectrum
LNA	**:** Low Noise Amplifier
DRC	**:** Design Rule Check
LVS	**:** Layout vs Schematic
PLS	**:** Post-Layout Simulation

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DESIGN EXAMPLES FOR SECOND GENERATION CURRENT CONTROLLED CURRENT CONVEYORS AND THEIR APPLICATIONS IN 28nm PROCESS

SUMMARY

Intensified and complex communication needs of the society and the need for connectivity in every moment causes increasing interest in encrypted and cognitive communication techniques. Since the circuits used in encrypted and cognitive communication systems have some advantages over standard circuits such as, agility and configurability, it is aimed in this study to provide circuits with lower power consumption and higher bandwidths to be used in encrypted, cognitive and multi-standard communication systems. For this purpose and also with respect to their well-known current-mode operation advantages it is decided to use CCCII structure to build candidate applications for multi-protocol supporting topologies. STMicroelectronics` 28nm CMOS process is used in this study to increase the effectiveness of current mode implementations with a high end process. Applications to be implemented in this study are selected as a universal filter application and a frequency agile, configurable filter application for global positioning systems.

In this project, the initial period was started with feasibility phase to define needs of available communication standards and available circuit solutions currently in use. For this reason, literature search mainly focused on multi-protocol systems, cognitive and encrypted communications and so on. After a wise literature search main goals for the design activities and specification like constraints defined for the sake of the design process.

Following the literature search phase, previously provided CCCII structures and their behaviors were investigated deeply and available CCCII topologies checked for the consistency for possible multi standard application. After this research phase, two main topologies decided to be implemented with respect to performance and also design kit related constraints. Translinear CCCII topology and the balanced differential pair based CCCII structure were the selected design structures to be implemented.

Design of CCCII structures started with the mathematical definitions of behaviors expected from the designs. Firstly, translinear CCCII circuit designed with the mentioned process design kit and all main characteristics obtained accordingly and appropriately matching with the theoretical expressions. After that, corner simulations ran for the designed circuit to check its behaviors under various conditions of temperature and scattering of bias voltages and currents. Following the design of translinear CCCII circuit, balanced differential pair based CCCII structure designed and it`s also checked for consistency and behavior correctness. Corner simulations ran for balanced differential pair based CCCII and the results observed clearly for all corner cases.

As the next phase, applications of the designed CCCII circuits realized and exercised. An universal filter application with different filter frequency responses selected for translinear CCCII circuit and realized. All frequency responses observed with simulations and expressions detailed. A frequency agile configurable filter application is selected for the balanced differential pair based CCCII circuit. Possible era to implement this filter is selected as an industrial GPS filter structure and specifications for the filter are defined with respect to this. Realization of the filter done and behaviors checked for the designed frequency agile configurable filter structure.

As an important step in this thesis, layout and post-layout simulation phases also done for the designed CCCII structures. All steps were done according to the steps provided by the design kit provider and all mandatory recommended rule sets were satisfied for the processes. Post layout simulations and characteristics were obtained for the extracted netlists of the designed circuits and comments given for the behaviors.

In the last part of the study, recommendations and points to be kept in mind for this thesis reported and possible future implementations listed.

28nm PROSESİNDE ÖRNEK İKİNCİ KUŞAK AKIM KONTROLLÜ AKIM TAŞIYICI YAPILARI TASARIMI VE UYGULAMALARI

ÖZET

Çoklu içerik ve format yapısına dayanan, yoğunlaşan ve karmaşıklaşan haberleşme ihtiyacı günümüzde yeni haberleşme standartlarına ve uygulamalarına olan ilgiyi arttırmaktadır. Şifrelenmiş ve bilişsel haberleşme teknikleri sunmuş oldukları hızlı frekans cevabı ve kurgulanabilirlik gibi kilit rol oynayan özellikleri nedeniyle standart yapılara göre avantajları bulunan ve bu özelliklerin gelişimine ihtiyaç duyan yapılardır. Bu çalışmada, düşük güç tüketimi ve yüksek frekanslarda çalışma gibi günümüz için önem arzeden hedeflere ulaşılabilmesi amacıyla akım modlu devrelerden yararlanılarak şifrelenmiş ve bilişsel haberleşme sistemlerinde kullanılabilecek kurgulanabilir, çoklu frekans desteği olan ve hızlı frekans cevabı olan devre yapılarının önerilmesi amaçlanmıştır. Bu amaçla devre tasarımları ve benzetimleri sırasında tasarım kütüphanesi olarak STMicroelectronics 28nm prosesinden yararlanılmıştır. Yapılan tüm bu çalışma 28nm prosesinde gerçeklenmiş olması ve endüstriyel uygulamaları hedef alan yapısı nedeniyle önemlidir. Ayrıca, kullanılan prosese ait farklı özelliklerdeki elemanların farklı devre yapılarında kullanılması ile bu prosese ait davranışların anlaşılması ve bilinen devre yapılarındaki davranışlarının gözlenmesi sağlanmıştır.

Yapılan bu çalışmada öncelikle bilişsel ve şifreli haberleşme standartlarının detayları, gereksinimleri ve uygulanmış ve uygulanmakta olan devre çözümleri belirlenmiş olup yapılacak çalışmada dikkat edilecek hususlar ve hedefler büyük bir titizlikle belirlenmiştir. Yapılan inceleme ve literatür taramaları esnasında da tasarlanılacak devre yapıları için uygun uygulama alanları araştırmanın önemli noktalarından biri olmuştur. Bilişsel ve şifreli haberleşme sistemleri günümüzde özellikle askeri alanlarda önem arzeden haberleşme biçimlerini kapsamaktadır. Bu durumdaki temel unsur bu tarz yapıların sunduğu yüksek güvenilirlik ve performans ile açıklanabilir. Toplum ve bireylerin kullanmakta olduğu uygulamalar açısından düşünüldüğünde ise, uygulamalarını yavaş yavaş görmeye başladığımız bu haberleşme biçimleri taşınan içeriğin önem arzettiği durumlarda ve sistem performansının vazgeçilemez olduğu uygulamalarda dikkat çekmektedir. Günümüzde gittikçe artan bilgiye erişime bağlı kalma isteğiyle beraber kişinin güncel hayatında da bu tarz uygulamaların önemi ve görülme sıklığı artmaktadır. Burada ortaya çıkan önemli unsur, standartların belirlenmesinde olduğu kadar bu standartları destekleyebilen devre yapılarının tasarımıdır. Günümüzde kullanımda olan yapılarda çoklu standart desteği ve benzeri başlıklar ayrık devre tasarım ve modelleriyle giderilmekte olup kullanılan devrelerin yapısal büyüklük ve karmaşıklığını arttırmaktadır. Bu açıdan akademik ve endüstriyel olarak gittikçe önem arzeden ve hedeflenen konu, çoklu standart desteğini çok geniş frekans aralıklarında destekleyebilen haberleşme devrelerinin tasarlanmasıdır.

Endüstri ve akademik çevrelerin ihtiyaç duyduğu çoklu haberleşme standardı desteği ve geniş çalışma bantları için devre tasarımı bu çalışmanın temel çıkış noktasını oluşturmaktadır. Tasarlanması planlanan yapı, endüstriyel olarak problem arz eden haberleşme standardlarına örnek çözüm önerme amacıyla kurgulanmıştır.

Çoklu standart desteği ve yüksek çalışma frekans aralığının sağlanabilmesi açısından akım modlu devrelere duyulan ihtiyaç açıktır. Akım modlu devrelerin seçiminde, bu devrelerin gerilim modlu eşlenik devrelere göre kolay tasarımı, yüksek çalışma bandı aralıkları, geniş doğrusal çalışma bölgeleri gibi özellikleri sahip olması önemli seçim parametrelerini oluşturmuştur. Bu açıdan bu çalışmada akım modlu devre yapılarından olan ikinci kuşak akım kontrollü akım taşıyıcı yapılarından yararlanılması planlanmıştır.

İkinci kuşak akım kontrollü akım taşıyıcı yapılarının incelenmesine bu yapıların ortak olarak sağladığı temel karakteristiklerin incelenmesiyle başlanmıştır. Devrelere ait matematiksel ifadeler ve devre davranışları teorik olarak incelenmiştir. Bu yapıların devre tasarımının temel noktası olarak seçilmesindeki ana unsurlardan biri de bu devrelerin sağlamış olduğu terminal direnç davranışları ile tamamiyle aktif ayarlanabilir devre yapılarına olanak sağlamasıdır. İncelemenin ardından, örnek olarak alınan yapılardan öncelikle translineer ikinci kuşak akım kontrollü akım taşıyıcı yapısının kendine özgü davranışı incelenmiş ve tamamen CMOS yapılarla gerçeklenecek bir yapının sergileyeceği davranışlar matematiksel olarak incelenmiştir. Yapılan incelemenin ardından gerek kullanılan tasarım kütüphanesinin getirdiği kısıtlar nedeniyle gerekse performans incelemesi nedeniyle dengelenmiş ihtiyaç duyulacağı göz önüne alınarak farksal giriş devresi tabanlı tamamen CMOS CCCII yapısının incelemesine yer verilmiştir. Bu yapının da ortak CCCII davranışlarının üzerine sahip olduğu devreye özgü davranışlara ait ifadeler dikkatle incelenmiş ve hedeflenen davranış hakkında bilgi sahibi olunmuştur.

Tasarlanması planlanan yapıların incelemesinin tamamlanmasının ardından devrelerin 28nm CMOS kütüphanesi ile tasarımına geçilmiştir. Öncelikle translineer CCCII devresinin tasarımı yüksek geçit kalınlığına sahip yüksek eşik gerilimli transistörler kullanılarak yapılmış ve temel karakteristikleri yapılan benzetimler yardımıyla gözlenmiştir. Elde edilen karakteristiklerin incelenen devreye ait matematiksel ifadelerle eşlendiği gözlenmiş ve tasarımın başarısı gözlenmiştir. Yapılan bu benzetimlerin ardında endüstriyel uygulamalarda çok önemli bir yer arz eden farklı durum senaryoları (corner) kullanılan tasarım kütüphanesinin belirlediği ölçülerde incelenmiştir. Bu durumda incelemede farklı sıcaklık, besleme gerilimi ve kutuplama akım sapmalarının devre üzerinde göstereceği etkiler kütüphane değişkenlerinin sapmalarına bağlı olarak devre davranışları üzerinde incelenmiştir. Translineer devrenin tasarımının ardından dengelenmiş farksal giriş tabanlı CCCII yapısının tasarımı proses tarafından öncelikli olarak sağlanan transistör yapıları ile gerçeklenmiş ve temel karakteristikleri yapılan benzetimler yardımıyla incelenmiştir. Elde edilen davranışların incelenen devreye ait matematiksel ifadelerle bağdaştığı bu devre için de gözlendikten sonra devreye ait farklı durum senaryolarına ait benzetimler gerçekleştirilmiştir. Yapılan bu benzetimlere ait inceleme ve sonuçlara çalışma içerisinde detaylı biçimde yer verilmiştir.

Kullanılacak olan devre yapılarının tasarımlarının ardından devrelere ait uygulamaların seçilmesine ve gerçeklenmesine geçilmiştir. Uygulamaların seçilmesi esnasında belirtildiği gibi endüstriyel uygulamalarda konuyla ilgili karşılaşılan problemler esas alınmış ve çözüm önerisi sağlanması amaçlanmıştır. Translineer

CCCII yapının uygulaması olarak çoklu frekans cevabı destekleyen genel süzgeç yapısı seçilmiştir. Tasarlanan süzgeç yapısının davranışları ve çıkışlarında farklı süzgeç davranışlarına ait band geçiren, alçak geçiren, yüksek geçiren süzgeç karakteristileri gözlenmiştir. Elde edilen davranışların incelemesi sonucunda yapılan süzgeç devresine ait matematiksel ifadelerle karakteristiklerin örtüştüğü gözlenmiştir.

Tasarımı yapılan dengelenmiş farksal giriş devresi tabanlı CCCII yapısının uygulaması olarak literatürde önerilen kurgulanabilir, frekans atik süzgeç yapısı seçilmiştir. Tasarlanacak uygulamanın özellikle endüstriyel uygulamalarda öneminin yüksek olmasından dolayı tasarım sürecinde devrenin global yer belirleme sistemlerinin farklı protokollerini destekleyen bir yapıya çözüm olarak sunulması hedeflenmiştir. Bu hedefle devre tasarımı endüstriyel spesifikasyonlara uygun frekans aralıklarını destekleyecek şekilde tasarlanmış, yapının oluşturulmasından önce yapının dayandığı temel mantık ve ilkelerden bahsedilmiştir. Daha sonra tasarımı yapılan devreye ait benzetimler gerçekleştirilmiş ve devrenin belirlenen hedef standart protokollere uygun çalışıp çalışmadığı gözlenmiştir. Yapılan bu tasarım uygulaması sonucunda da bilişsel sistemlere olan benzerliğiyle önem arz eden küresel yer belirleme sistemlerine dair yeni çözüm hedefleyen yapının çalışması sınanmıştır.

Endüstriyel uygulamalarda tasarımın gerçeklenmesi açısından serim çiziminin önemi çok büyüktür. Serim çizimi devrenin kırmık üzerine gerçekleneceği materyallerin belirlendiği önemli bir adımdır. Bu açıdan, serim ve serim sonrası benzetimler devrenin fikir ve tasarımının gerçek dünyaya uyarlanması için en kilit adım olarak düşünülebilir. Tüm bu nedenler göz önünde bulundurularak, gerek endüstriyel önemi gerekse kullanılan 28nm kütüphanesine ait gerekli bilgi birikimin elde edilmesi amacıyla tasarlanan CCCII yapılarına ait serim çizimleri ve serim sonrası benzetimleri bu çalışma içerisinde yapılmıştır. Serim çizimlerinin yapılması sırasında kullanılan tasarım kütüphanesinin yeni ve endüstriyel anlamda yerleşikliğinin az olması nedeniyle bazı problemlerle karşılaşılmış olsa da sorunlar çözülerek serim ve serim sonrası adımların gerçeklenmesi tamamlanmıştır.

Serim sırasında ve serim sonrası benzetimlerde tasarım kütüphanesi tarafından önerilen tüm testler ve benzetim setleri uygulanmıştır. Profesyonel bir endüstriyel uygulamada gerçekleştirilen tüm adımlar aynı titizlik ve sırayla gerçeklenmiş ve gözlenmiştir. Bu çalışmalara ek olarak, serim çizimi yapılan CCCII yapılarına ait davranışların serim öncesi ve serim sonrası karşılaştırmaları özenle yapılmış ve elde edilen sonuçlar bu çalışmanın içerisinde yorumlanmıştır.

Çalışma içerisinde yer alan tüm adımlarda tasarımı yapılan devrelere ait devre çizimleri, elde edilen sonuçların grafiksel gösterimleri gibi önemli unsurlar büyük bir titizlikle verilmiş, bu şekilde yürütülen çalışmanın adım ve sonuçlarının grafikler yardımıyla ön plana çıkarılması ve doğruluğunun gösterilmesi amaçlanmıştır.

Çalışmanın son kısmında yapılan tüm araştırmalar ve devre tasarımı, serim çizimleri ve benzetimlerle ilgili sonuçlar özet şeklinde incelenmiş ve ilerleyen aşamalarda devre üzerinde ne gibi iyileştirmelerin yapılabileceği ve ne gibi uygulama alanlarının seçilebileceği gibi öngörülerde bulunulmuştur. Yapılmış olan bu çalışma özellikle kullanılmış olan tasarım kütüphanesinde yapılan ilk literatür çalışması olması ve endüstriyel uygulamalara alternatif devre çözümü sunması nedeniyle önemlidir.

1. INTRODUCTION

Intensified and complex communication needs cause increasing interest in encrypted and cognitive communication techniques [1]. As there is a growing interest in implementing multi-standard structures, it is well known that the ease of realization and flexibility are not compatible for the designs supporting such communication techniques. Circuits used in encrypted and cognitive communication systems have some advantages over standard circuits such as, agility and configurability [1]. In addition to this, current mode circuits are commonly known with their larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry and low power consumption [2]. The objective of this thesis is to provide circuits, with lower power consumption and higher bandwidth with the aid of current mode circuits, to be used in encrypted and cognitive communication systems.

1.1 Background

Over the past decades, the continuous and fast growing use of digital communication, mobile, computer and network systems has aroused communication data security issue concerns where some type of data cryptography is required. Furthermore, telecommunications have become an important part of society in this period, in economics as well in terms of technological advances. The convergences of various communication technologies increase the necessity for more powerful, multi-channel and multi-functional terminals. This led to several new technologies such as software radio and cognitive radio [3].

Encouraged by developments in technological part, the explosion of applications in areas such as voice, data transmission and multimedia has therefore contributed to different corresponding standards [4]. The handling of various standards was firstly achieved by specific structures dependent on the standard, which increased the number of circuits in the systems supporting multi-functional interfaces. In that period, the trend was to handle unique transmission standards with dedicated device structures. This trend has now changed due to increased complexity and number of

communication standards. Communication devices and circuits should currently be able to support multi standards at the same time. These constraints led to investigation of circuits supporting multi-standards with quick frequency response, wide bandwidth operation, low power consumption and configurability easiness.

In recent years, the emphasis on current mode circuits has been increased due to the advantages of improvements of semiconductor technologies and supremacy of current mode circuits over voltage mode circuits such as higher operation frequencies and low power consumption. In parallel to this, a three terminal device named "second-generation current-conveyor" (CCII) becomes one of the most preferred devices in realizing current-mode circuits mainly because it is the counterpart of an operational amplifier in current-mode circuits [5]; besides, it has high slew-rate, wide bandwidth and large dynamic-range. Afterwards, the next generation circuitry named current-controlled current-conveyor (CCCII) fulfills the weaknesses of CCII on configurability and tunability which makes current-mode circuits one step further than voltage-mode devices in circuit designs.

With the widespread advances in communication standards and increasing complexity, multi-standard supporting agile and configurable circuit structures becomes a hot point to be investigated in both academic and industrial eras [6 – 9]. Through various pioneering designs, many frequency agile filters supporting multi-standards have shown up in both literature and in industrial applications. Design of a frequency agile, multi-standard supporting, fully active structures to be used in system on chips will be the main topic of this project.

1.2 Previous Work

The importance of circuits for multi-standards has resulted in lots of literature on the subject. Researches on the topic both describe the most important design constraints to support multi-standards and multi-functionality. Main stream followed by the most of the researches depend on a dedicated circuit design with parameters and values. As it can easily be considered, it`s not the optimistic solution for the issue.

Despite the numerous published documents in the area, there is lack of information on configurable design applications to support this kind of multi communication standards simultaneously.

To achieve a fully active solution for multi standard circuit implementations, multi standard definitions and constraints in the literature investigated deeply [10 - 13]. It is decided to provide a global positioning system application in fully active configuration and a universal filter implementation as it was studied in many researches [14, 15]. As a fully active analog component CCCII structures investigated to have optimum topology for this project [16 -21]. Balanced differential pair based CCCII structure and translinear CCCII structures are selected for implementations due to constraints and limitations encountered during the use of design kit [17, 22, and 23].

A valuable research done by Fabre and Lakys provides how the problem of multi standard support will be solved with the help of current mode, fully active circuit topologies. Basically, a feedback loop realized by active element CCCII is used to meet functional requirements. By implementing more feedback paths on the circuit, it is shown that the frequency agile configurability is possible for more operation frequencies.

Another valuable research done by Liu and Xi provides how the universal filter implementation will be done more efficiently with the help of available current mode, fully active circuit topologies [24]. By implementing such a universal filter, it is shown that the multi type filter responses will be obtained easily with current mode topologies as previously presented in the literature [25].

1.3 Motivation

With advances in communication technologies, it becomes a bottleneck to support multi functionality without sacrificing any power or area in mobile electronics. Improvements in semiconductor process nodes have shown a great support to meet such limitations until now. It is fully observable that an extra effort needs to be put on design side to balance the pressure on process side.

Current problems and limitations will be addressed regarding the improvements on both design and process sides. The process used in this work is STMicroelectronics` 28nm CMOS process which is a cutting edge technology has not been commonly used in industrial products yet. This process will provide area and power improvements to this project easily when compared to other implemented circuits.

In this project, it is aimed to use Fabre`s frequency agile, configurable structure with this process node by making necessary changes to improve behavior of the circuit. Application is chosen as global positioning systems since they are a bunch of different standards provided and supported by different nations or associations with names: GLONASS, GPS, GALILEO and BEIDOU.

It is also aimed to use Liu`s universal filter structure as an alternative solution to currently available industrial universal filter topologies with the advantages of 28nm design process.

1.4 Outline of Thesis

This thesis presents design of a balanced differential pair based CCCII design and translinear CCCII design at 28nm process node and their possible applications in a system on chip current mode, fully active, frequency agile and configurable filter design for global positioning systems and in a universal filter implementation. Chapter 1 gives the background and main motivation behind the design and reviews the related literature. Chapter 2 discusses the encrypted and cognitive communication standards and possible application constraints. Chapter 3 presents CCCII circuit characteristics and design of translinear CCCII circuit and balanced differential pair based CCCII circuit with simulations of the designs. Chapter 4 gives the details for the design of universal filter with translinear CCCII circuit. Design of frequency agile, configurable filter is discussed and definitions of important parameters are given in Chapter 5. Layout and post-layout simulations are detailed in Chapter 6. Chapter 7 concludes the thesis and provides future directions to this work.

2. ENCRYPTED AND COGNITIVE COMMUNICATIONS

2.1 Software Defined Radio

Software defined radio, or SDR, is a transmission-reception system whose characteristics (frequency, bandwidth, modulation, etc.) are controlled and can be chosen using computer tools [6, 7]. A software radio is a multi-band radio capable of supporting multiple air interfaces and protocols through the use of wideband antennas, RF conversion, analog to digital converters (ADCs) and DACs [8].

Software defined radio consists of hardware parts for execution of communication over air interface and the software part to sense, control and model the communication standard in an abstract level. Our focus will be more on the hardware part for multi-band communication in this project.

Such a circuit to receive or transmit data in software defined radio structure needs to support controllable structure depending on the communication protocol models in software part. This kind of circuit topology is called reconfigurable.

An effective software radio, both in hardware and in software, thus must make it possible to cover common communication frequency range (800MHz – 6 GHz) in a continuous way and with a same performance as those required by the already existing standards [9].

Various approaches are currently used to realize software defined radio functionality. According to Mitola [10], the best way is digitizing the totality of the spectrum received by the antenna. After then, the signal will be processed. Indeed, such structure to overcome the complexity of processing is not feasible with the current state of the art structures. So, this approach is not the optimal solution to be considered. Alternatively, the receiver part will include parallel structures dedicated to different protocols of air interfaces and various standards. In this way, this solution results in high number of elements so size, cost and power consumption will increase. The most widespread approach currently used for software defined radio is

using reconfigurable elements. This approach makes it possible to adapt to any standard of radio communication [9].

2.1.1 Cognitive radio

Cognitive radio refers to wireless architectures in which a communication system does not operate in a fixed assigned band, but rather searches and finds an appropriate band in which to operate [11]. It will be considered as the most elaborate level of software radio. The cognitive radio, built on software defined radio, is defined as an intelligent wireless communication system that is aware of its environment and uses the methodology of understanding-by-building to learn from the environment and adapt to statistical variations in the input stimuli, with two primary objectives in mind; highly reliable communication whenever and wherever needed, efficient utilization of the radio spectrum [12].

Cognitive radio needs to adapt its behavior according to the external environments situation at the communication period according to the needs of the user. Decision parts responsibility is fully on software part and software part will drive the hardware part to be configured accordingly.

An example for the dynamic use of the spectrum shown in Figure 2.1 consists of transmitting and receiving in the areas of spectrum which are not used at one given time by other users [9].

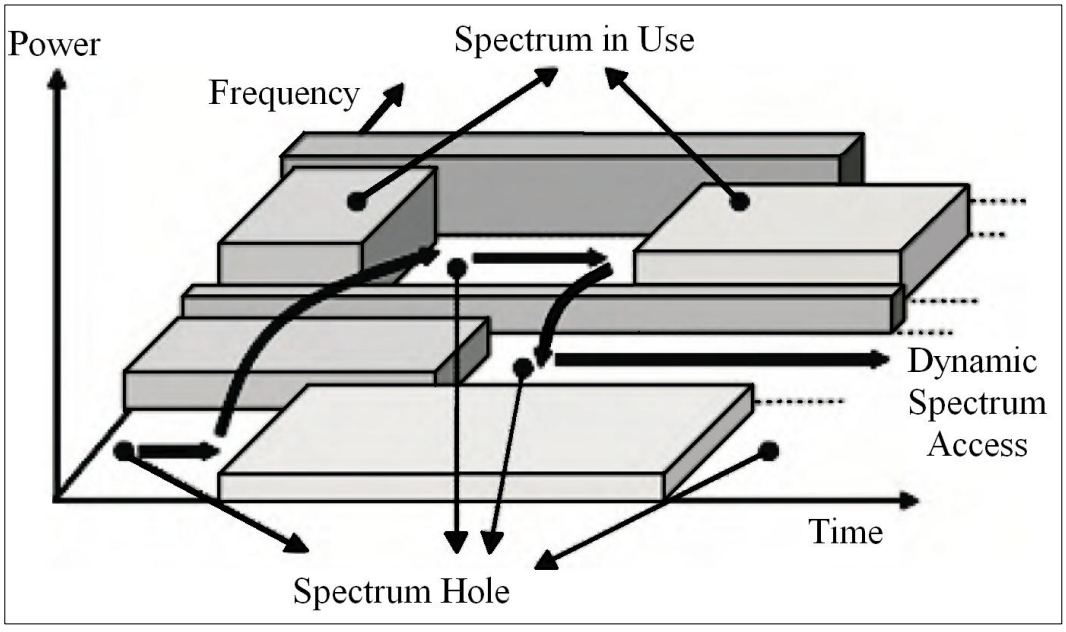

Figure 2.1 : Dynamic access to the spectrum of telecommunications [9].

2.2 Frequency Hopping Spread Spectrum

Encryption is the process of transforming information by using an algorithm to make it unreadable to anyone except those possessing special knowledge, named as key. Encrypted communications have long been used by militaries and governments to facilitate secret communication. Encrypted communications are safe communications for which various techniques of encodings are applied with the basic aim of preventing unauthorized signal reception or making it incomprehensible to undesirable receivers. Various encryption techniques are used to make this communications not exploitable by an unauthorized receiver [9].

The frequency hopping spread spectrum technique (FHSS) spreads data over wider bandwidth than the necessary one. Signal broadcasting done over seemingly random series of frequencies and receiver hops between frequencies in synchronous with the transmitter [13]. This technique was first introduced with an aim of making military communications safe [9]. When FHSS used for broadcasting signals, eavesdroppers hear unintelligible blips only and jamming on one frequency affects only a few bits.

An example for the frequency hopping spread spectrum shown in Figure 2.2 gives diagrams for channel configuration and channel use during transmission.

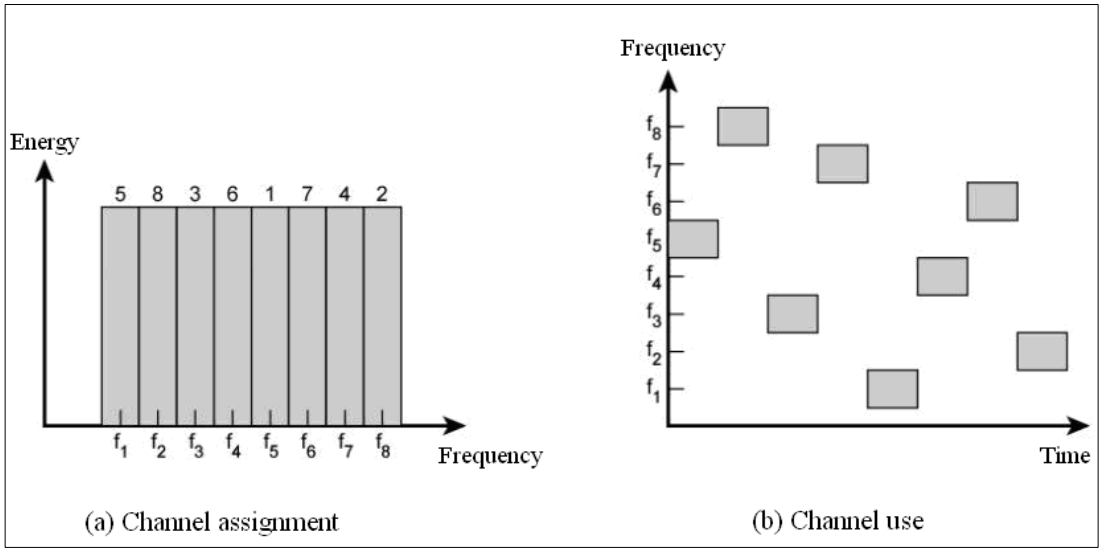

Figure 2.2 : Frequency hopping spread spectrum example [13].

2.3 Global Positioning as an Example Communication System

Since the Global Position System (GPS) was first launched by U.S. government and widely used in civilian applications, many countries have engaged in developing

their own Global Navigation Satellite Systems (GNSS). Currently, in addition to GPS, three others exist including GLONASS from Russia, Galileo from Europe and Compass/Beidou from China. Possible increase in satellite amounts in coming years will bring the opportunities for interoperation between different constellations of global positioning systems. So, a receiver structure compatible with all constellation signals is favorable, especially for the next generation GNSS applications [14].

For the biggest possible versatility of future global navigation systems, including GPS, GLONASS, Beidou and Galileo, the modular RF architecture and software defined radio concept will be chosen [15]. This is also an important research topic currently under investigation by many academic and industrial partners.

As the software defined radio concept is far further, the design of the RF front end part becomes a key technology for such receivers which handle different constellations.

2.4 Common Problems for Realizing Encrypted and Cognitive Communication Circuits

Through the evolution of wireless receivers, the direction continued from inflexible but easily realizable architectures to entirely flexible but not easily realizable architectures for multichannel communications. Under these circumstances, ease of realization always depends on the availability of reconfigurable structures to be used in receiver systems. Such architectures require reconfigurable analog elements: LNA, local oscillators, mixers and filters [9]. It is not a big deal to find reconfigurable LNA and local oscillator structures but, implementation of integrated and easily reconfigurable RF filters on a wide frequency range is a more delicate task [9].

As we search the software defined radio and cognitive radio part, the software part comprises functions that allow an optimal reconfiguration. It is easy to handle different communication protocols simultaneously with the aid of a multifunctional software structure. On the other hand, if we look at the RF front-end part of the software defined radio and cognitive radio structures, it is visible that we need to perform analog functionality with reconfigurable components to handle multi protocol communications. By the way, realization of integrated and reconfigurable RF filters is not an easy thing to do.

All in all, when we check the current implementations and possible future topologies for the multi-functional, multi-protocol communications, it is obvious that the design of the integrated and reconfigurable RF filters is the most critical part to be investigated.

3. DESIGN OF CCCII

Nowadays, current mode circuits have been receiving significant attention in analog circuit design. A useful function block for high frequency current mode applications is a current conveyor. The current conveyor is a three terminal device performing many useful analog signal processing functions when the device is connected with other electronic elements in specific circuit configurations.

The first generation current conveyor (CCI) was proposed by Smith and Sedra in 1968 [16] and the more versatile second generation current conveyor (CCII) was introduced by the same two authors in 1970 [17], as an evolved version of their first generation conveyor. In 1996 were introduced current controlled conveyors that are an evolution of previous CCII [18, 19]. The introduction of the second-generation current controlled current conveyor (CCCII) responded the main drawback in lacking of electronically tunable feature of CCII by utilizing the parasitic floating intrinsic terminal resistance at port X [18, 19], which can be tuned electronically by adjusting the bias current.

3.1 The Principle of CCCII

Classically, the core of CCCII is simply the mixed translinear-loop, which is implemented originally in BJT and later in MOSFET. Translinear structure will be satisfied with different circuit topologies. So, our aim in this section is to give the principle of CCCII.

The operation of CCCII± can be described by the following equation [19]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \qquad \textbf{(3.1)}$$

The current output at port Z(i_z) that is conveyed from the input current at port X(i_x) is

expressed as [19]:

$$i_x = \pm i_z = \pm \frac{v_x - v_y}{R_x} \tag{3.2}$$

As it can be easily derived from the formulas, the CCCII based applications can be realized resistor-free and tunable by utilizing terminal resistance R_x as the adjustable circuit's parameters.

The ideal equivalent circuit of CCCII is displayed in Figure 3.1 for better understanding.

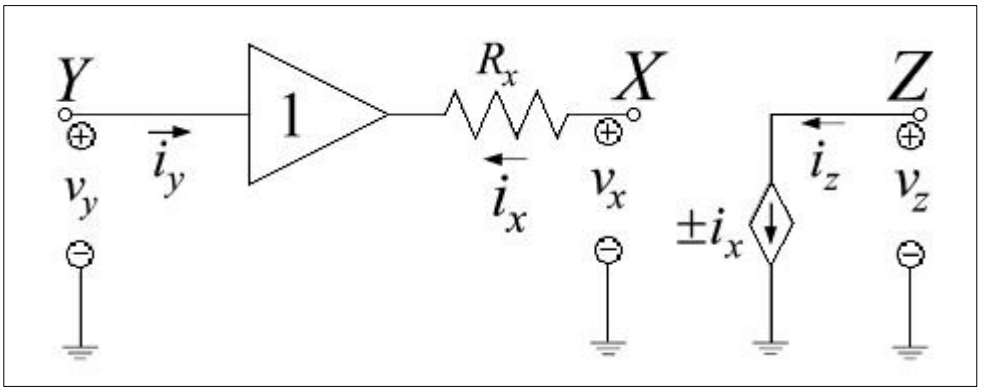

Figure 3.1 : Ideal equivalent circuit of CCCII [20].

The practical equivalent circuit of CCCII due to transistor non-idealities is given in Figure 3.2.

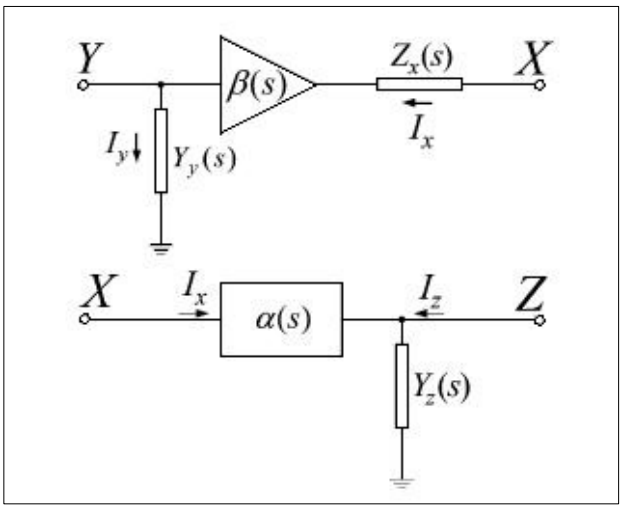

Figure 3.2 : Approximate practical equivalent circuit of CCCII [20].

The approximated practical equivalent CCCII due to imperfect transistor behavior and non-idealities will be formulated with formula 3.3 [21] where parasitic admittances at port Y and Z are $Y_y(s)$ and $Y_z(s)$, current and voltage gain are $\alpha(s)$ and $\beta(s)$, frequency dependent terminal resistance is $Z_x(s)$.

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} Y_y(s) & 0 & 0 \\ \beta(s) & Z_x(s) & 0 \\ 0 & \pm\alpha(s) & Y_z(s) \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad \textbf{(3.3)}$$

3.2 CCCII Topography Used in Fabre's Circuit

The schematic implementation of the second generation controlled conveyor which is used by Fabre and his team is shown in Figure 3.4. It uses the mixed translinear loop of Figure 3.3. Two current mirror implementations allow the mixed loop to be dc biased by the bias current I_0. The general matrix relationship written for the second generation current conveyor will also be valid for the circuit topology used by the team.

A negative current transferring version of the current conveyor will be obtained easily, by only adding two cross coupled current mirrors in order to reverse the sign of the current $i_z(t)$ [19].

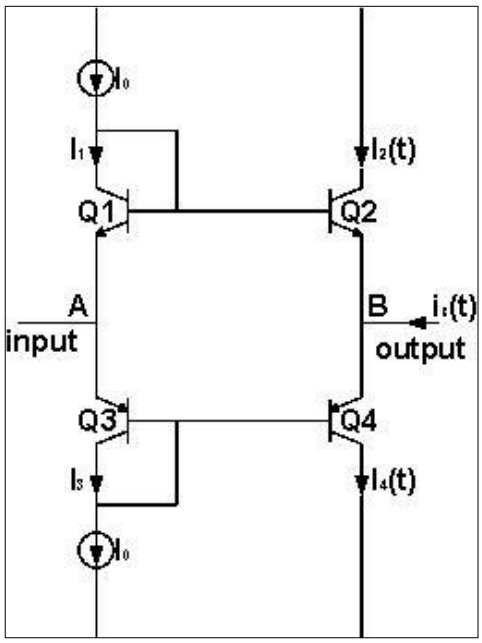

Figure 3.3 : Schematic from of the mixed translinear loop [19].

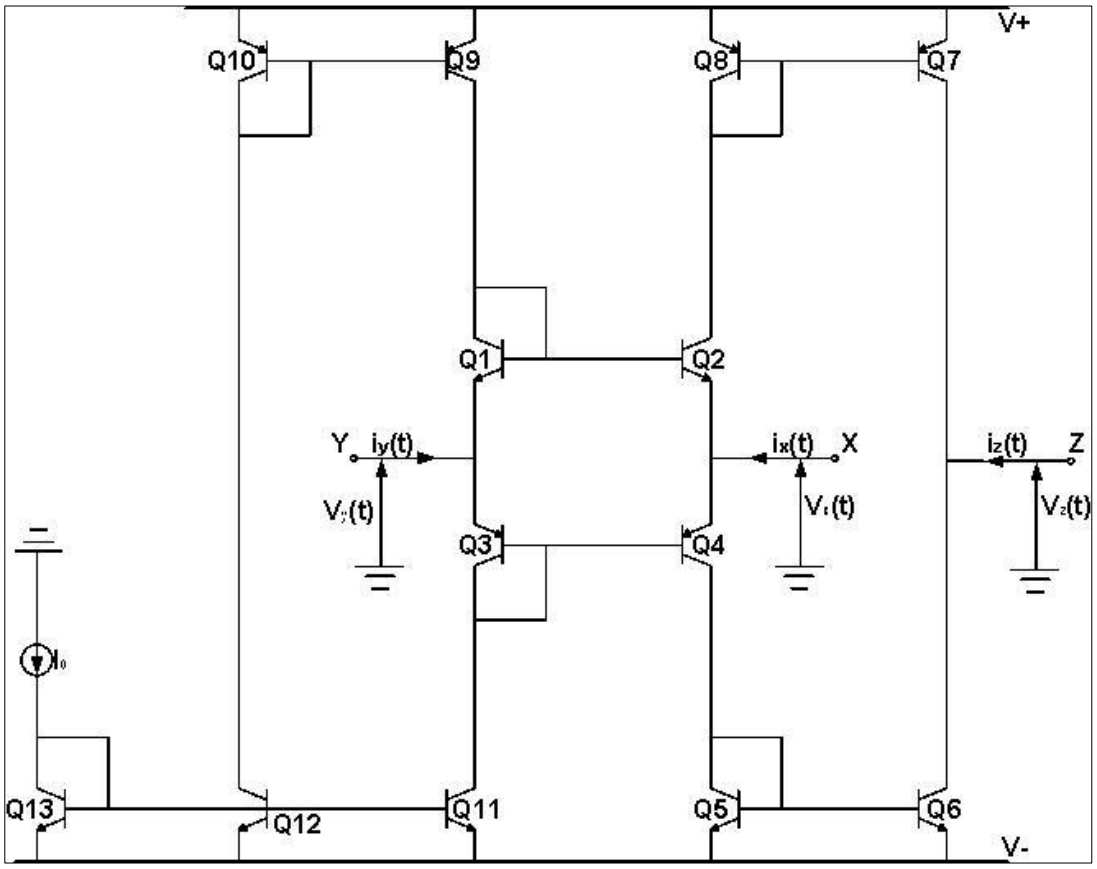

Figure 3.4 : Schematic implementation of CCCII used by Fabre [19].

The mixed translinear loop, shown in Figure 3.3 and placed in CCCII circuit in Figure 3.4 contains two PNP`s and two NPN`s transistors. The behavior is characterized by the translinear relationship between the collector currents of the transistors and this relationship shows that the output small signal resistance of the equivalent voltage follower, is equal to [19]:

$$R_x = V_T / 2I_0 \tag{3.4}$$

Briefly, the resistance will be able to be controllable by adjusting on the bias current of the loop. As a basic modes of operation of the circuit, when the port Y of the non inverting CCCII is grounded and the port X constitutes the input port of the circuit, the output current is then given by [19]:

$$I_{out}(t) = \frac{2I_0}{V_T} V_{in}(t) = \frac{1}{R_x} V_{in}(t) \tag{3.5}$$

It is clear from the given formula that the value of output current is controllable by the bias current.

3.3 Design of Fully CMOS Translinear CCCII Circuit

The translinear CCCII circuit is implemented with the bulk CMOS process in the initial feasibility period and the implementation did not satisfy operation conditions due to low supply voltages supported by regular process transistors. Afterwards, the circuit is designed with STMicroelectronics 28nm 28A GO2 CMOS process which supports ±0.90V supply voltages. This process has specific gate oxide materials and thickness to support higher supply voltages for different operations. This 1.8V supply voltage is the upper limit allowed for the operation in this CMOS process provided by STMicroelectronics.

The designed mixed translinear fully CMOS CCCII structure is displayed in Figure 3.5.

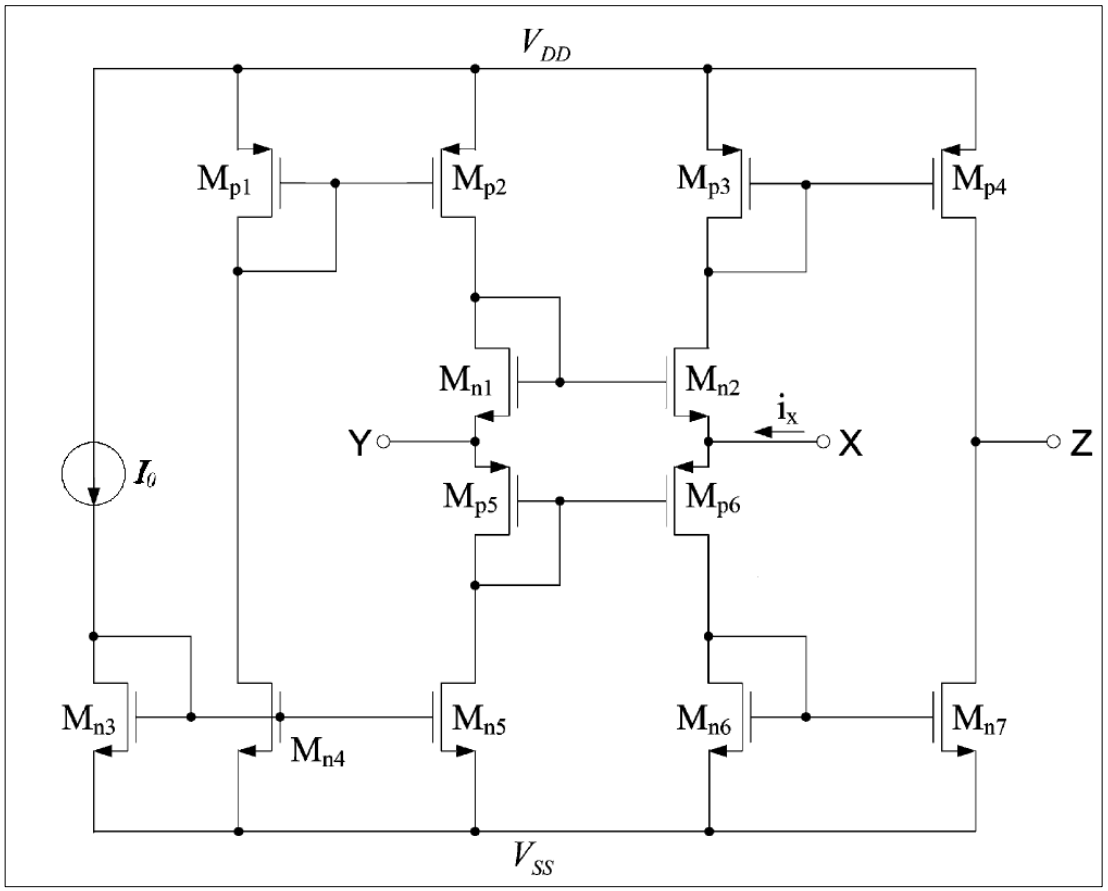

Figure 3.5 : Fully CMOS translinear CCCII circuit.

MOSFETs W/L ratios are listed in Table 3.1 based on common channel length 600nm. This length is chosen because minimum allowed channel length for GO2 process is 150nm.

Table 3.1 : Transistor ratios of translinear CCCII.

Transistor	W/L Ratio
M_{p1}-M_{p4}	15
M_{p5}-M_{p6}	30
M_{n1}-M_{n2}	10
M_{n3}-M_{n7}	5

3.3.1 Main characteristics of designed CCCII circuit

In order to verify the translinear CMOS CCCII architecture that is explored in previous section, Spectre simulator is used. It is a part of the Cadence package. Design kit of the STMicroelectronics 28nm GO2 process was used. Different simulation setups were used for different behavior analysis.

The translinear CCCII circuit`s characteristic of R_x relating to 10µA bias-current is presented in Fig. 3.6. Its frequency-dependence can be clearly seen from the following figure.

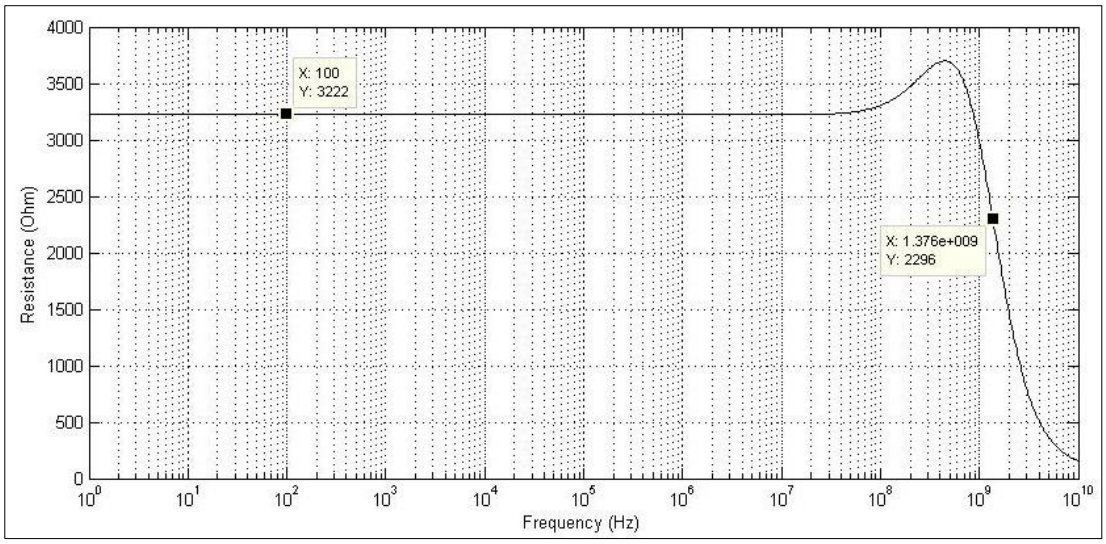

Figure 3.6 : R_x based on I_0=10µA.

Observing Figure 3.6, the resistance value seen on port x remains flat up to 1.37GHz frequency values. This operating frequency will be efficient for many application areas.

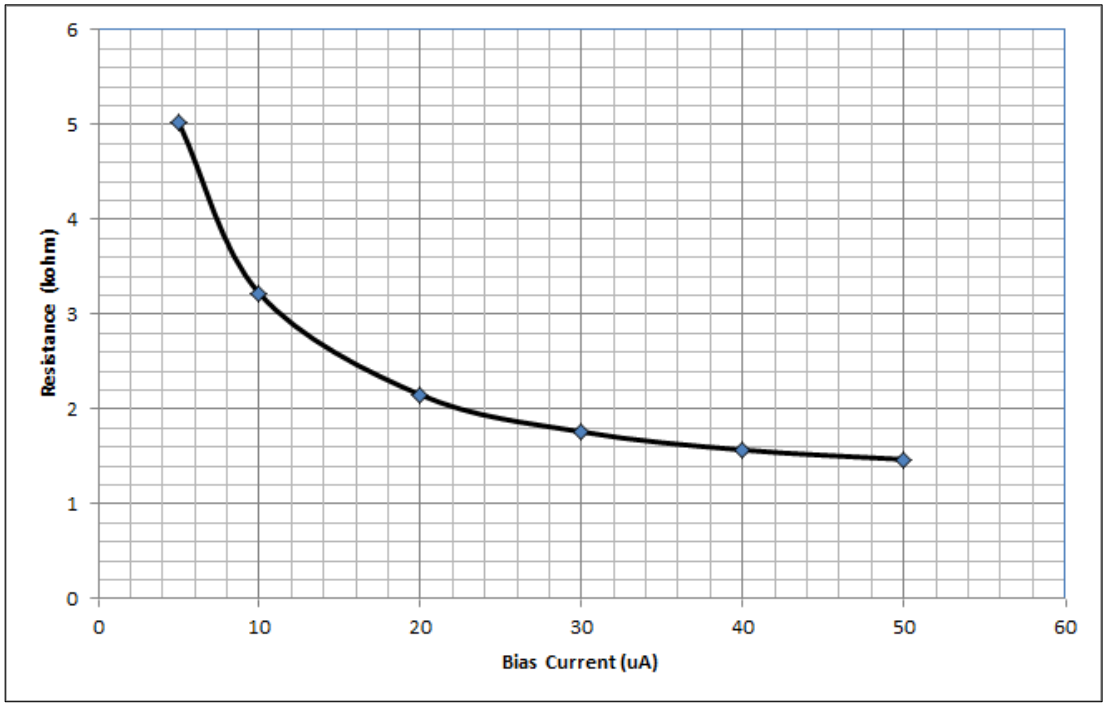

Figure 3.7 : Rx vs bias current.

Figure 3.7 emphasizes the bias current and resistance value at port x relationship with respect to different bias current values. The behavior is clear that when bias current increases, resistance value at port x decreases. This behavior is also compatible with the given equations.

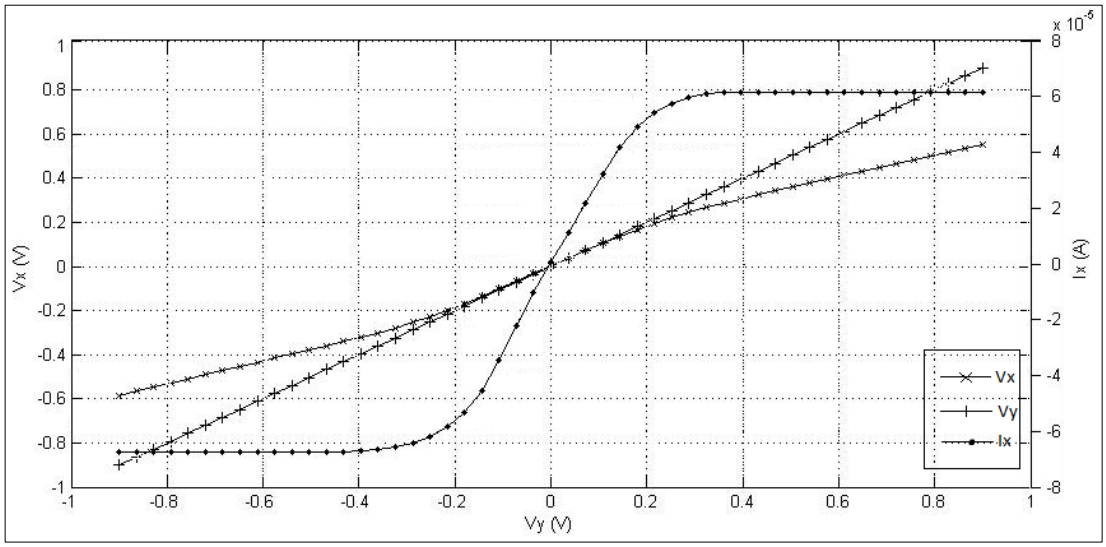

Figure 3.8 : The voltage transfer and voltage-current characteristics of translinear CCCII.

In Figure 3.8, the voltage transfer characteristics of the translinear CCCII structure are plotted. Additionally, the V-I characteristic of the input voltage versus the input

current at port X is given in the same figure. This behavior verifies the current-voltage and voltage-voltage following behaviors given by the equations.

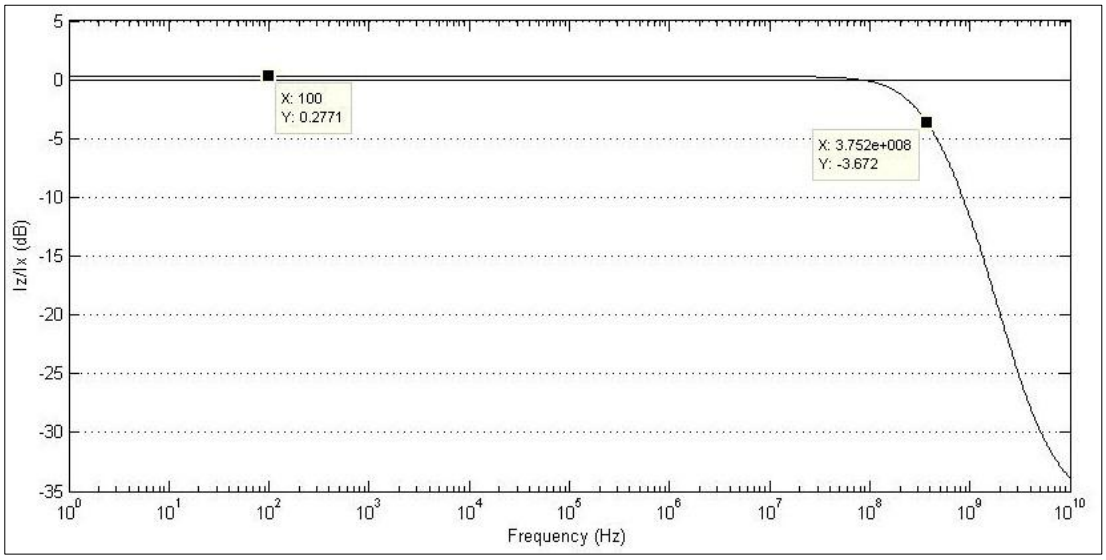

Figure 3.9 : The small-signal characteristic of the current transfer gain.

The small-signal current transfer gain characteristic of the designed translinear CCCII circuit is plotted in Figure 3.9. The 3-dB bandwidth of current gain for 10µA bias-current can be approximately read as 375 MHz.

At given bias current conditions, the frequency characteristics of the designed circuit in operation can be assumed to be dominated by terminal resistance bandwidth. This can be also referred as open loop bandwidth of the circuit.

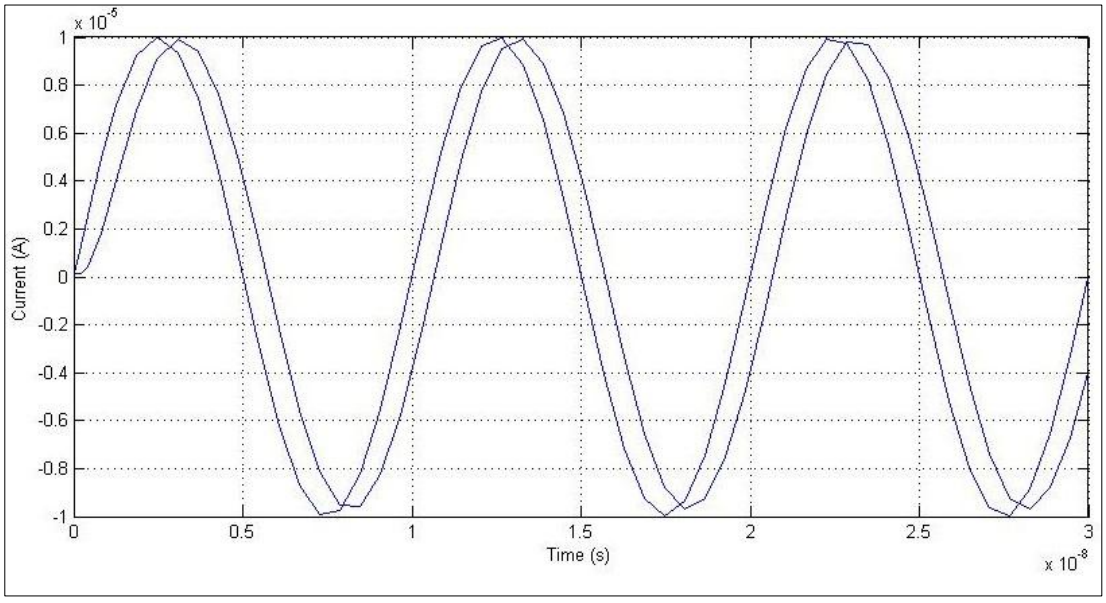

Figure 3.10 : Transient current transfer characteristic between ports X and Z.

The transient current follow between port Z and X is shown in Figure 3.10 for 100MHz, 10µA amplitude signal input.

In parallel to all characteristics, power consumption of the circuit is observed as 17.54µW.

Briefly, after observing main large and small signal behaviors of the designed translinear CCCII circuit, it is very visible that the designed structure is suitable for high frequency applications with the advantages of high end process node of 28nm.

3.3.2 Corner simulation characteristics of designed translinear CCCII circuit

In modern circuit design, as it was before, investigation of the circuit behavior with respect to design itself and additional variables is very important to prevent unwanted behaviors before mass production. For the sake of design behavior, parasitic variables of the process and additionally defined variables such as, working temperature, voltage and current changes are tested over the circuit and their effects on the performance observed during verification period.

Corner simulation for the designed translinear CCCII circuit is executed to see circuit behavior under industrial working case specifications. These cases are commonly used scattering examinations of supply voltage, bias signals and environmental variations in addition to process related changes. In the simulations, in addition to the default process variables scattering, temperature max-min variables defined as -40˚C and 110˚C, bias current scattering factor is defined as %25, which leads to 7.5µA and 12.5µA for a 10µA bias current and finally supply voltage scattering factor is defined as ±0.85V and ±0.95V for a ±0.9V supply voltage.

As an important point to mention, the rule sets defined for the corner case simulations will be improved with additional parameters and restrictions of the standards.

Figure 3.11 shows the resistance behavior seen at port x over frequency with respect to all defined corner cases. The resistance value seen on port x takes the maximum value 10.02kΩ that remains flat up to 3.10GHz for 7.5µA bias current, ±0.85V supply voltage, 110˚C temperature and 3.94kΩ that remains flat up to 7.53GHz for 12.5µA bias current, ±0.95V supply voltage, -40˚C temperature.

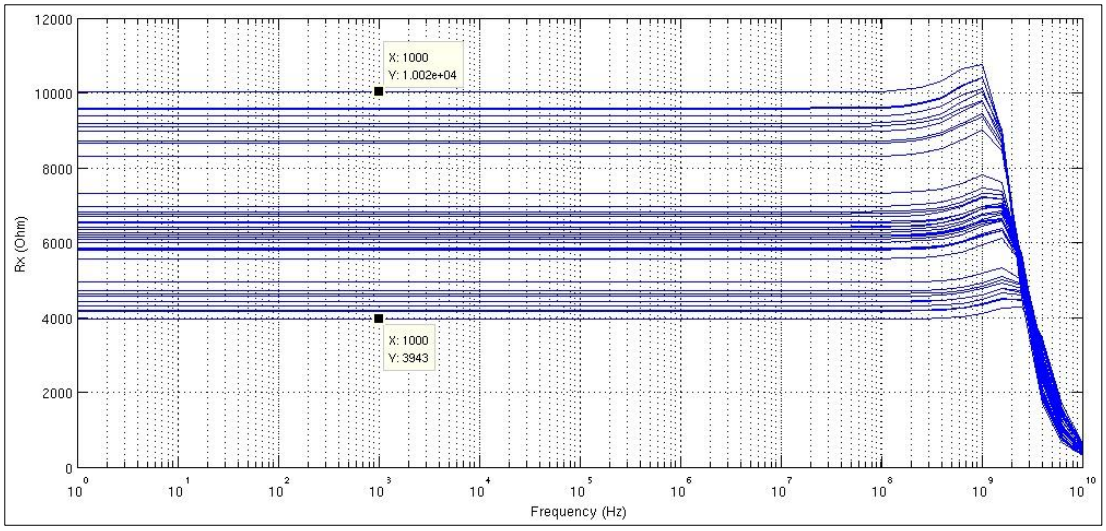

Figure 3.11 : R_x of translinear CCCII based on 72 different corners.

The large signal characteristics of the designed translinear CCCII structure are simulated again for 72 different corners to observe and review the behavior of the circuit. In Figure 3.12, the voltage transfer characteristics are plotted.

As it is seen in Figure 3.12, maximum dynamic range linearity is observed for 12.5µA bias current, ±0.95V supply voltage, 110˚C temperature and minimum dynamic range linearity is observed for 7.5µA bias current, ±0.85V supply voltage, -40˚C temperature.

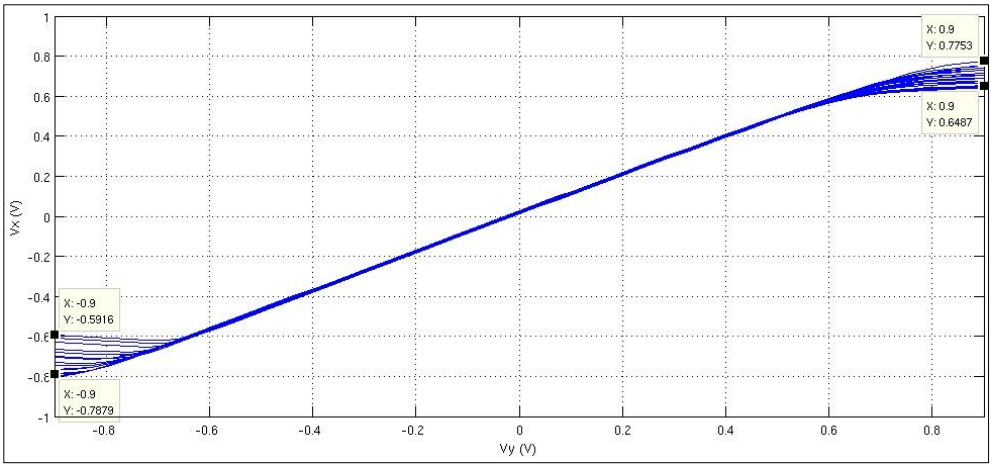

Figure 3.12 : The voltage transfer characteristics of translinear CCCII for corner analysis.

Observing Figure 3.12, maximum offset voltage seen at port x for zero input voltage is 28.43mV for operating conditions 7.5µA bias current, ±0.95V supply voltage,

110˚C temperature and minimum offset voltage seen at port x for zero input voltage is 11.2mV for 7.5µA bias current, ±0.85V supply voltage, -40˚C temperature.

The characteristic of the input voltage versus the input current at port X is shown in Figure 3.13 for the mentioned corner cases. Maximum offset current flowing through port x is observed as 5.14µA for operating conditions at 12.5µA bias current, ±0.95V supply voltage, 110˚C temperature. Minimum offset current flowing through port x is observed as 1.54uA for operating conditions at 7.5µA bias current, ±0.85V supply voltage, -40˚C temperature.

As an additional investigation, operating condition that allows maximum current flow at port x will be observed as 12.5µA bias current, ±0.95V supply voltage, -40˚C temperature. At this operating condition maximum current observed at positive supply is 26.24µA and at negative supply 14.82µA. In the meantime, operating condition that allows minimum current flow at port x will be observed as 7.5µA bias current, ±0.85V supply voltage, -40˚C temperature. At this operating condition maximum current observed at positive supply is 12.46µA and at negative supply 7.70µA.

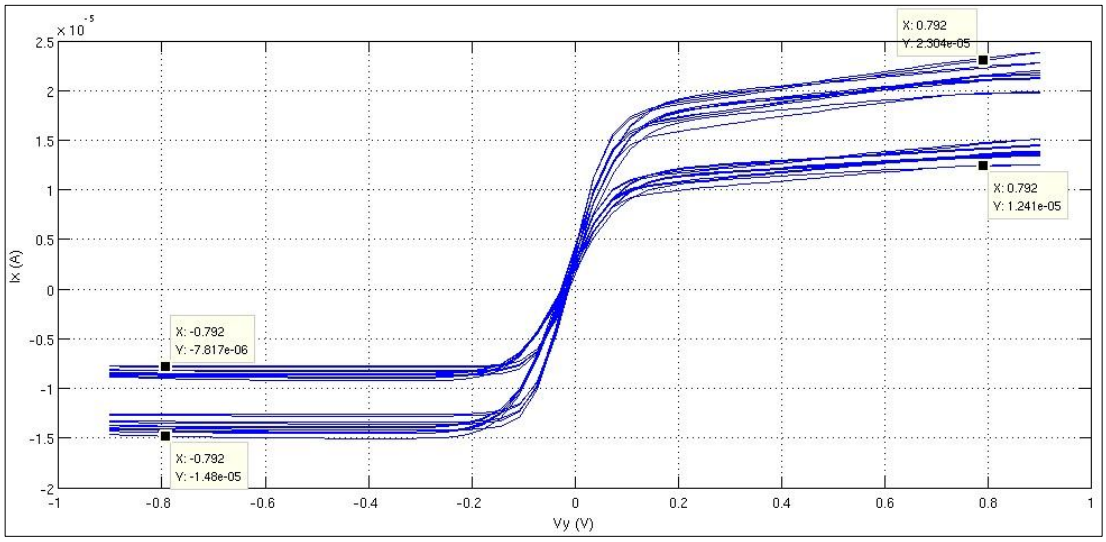

Figure 3.13 : The voltage current (Vy-Ix) characteristics of translinear CCCII for corner analysis.

The small-signal current transfer gain characteristic of the designed translinear CCCII circuit is plotted in Figure 3.14 for the mentioned corner cases. As it can easily be seen from the graph, low frequency operation is less affected by the corner cases and high frequency operation or bandwidth is affected more.

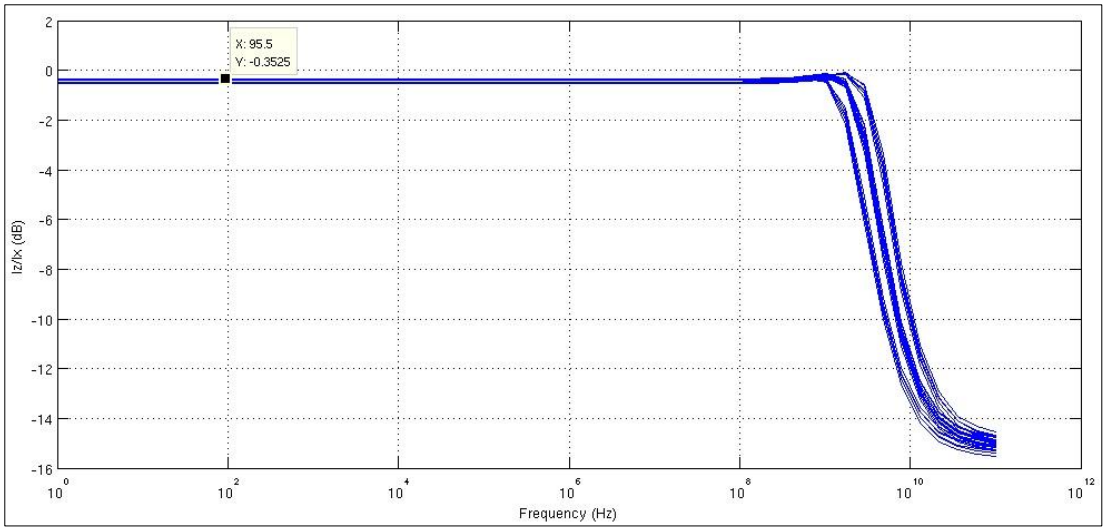

Figure 3.14 : The frequency current (Iz/Ix) characteristics of CCCII for corner analysis.

Maximum value observed for current transfer ratio is -346mdB for 7.5µA bias current, ±0.95V supply voltage, -40˚C temperature and minimum value observed for current transfer ratio is -598mdB for 7.5µA bias current, ±0.85V supply voltage, 110˚C temperature. Moreover, the 3-dB bandwidth of current gain for different cases can be approximately read as maximum 5.34GHz for 12.5µA bias current, ±0.95V supply voltage, -40˚C temperature and it is read as minimum 2.15GHz for 7.5µA bias current, ±0.85V supply voltage, 110˚C temperature.

3.4 Balanced Differential Pair Based CCCII Circuit

During the initial feasibility phase of the design, different circuit topologies are investigated in details. In the implementation phase, it is seen that the supply voltages of 28nm process will limit the maximum number of elements to be placed rail-to-rail. Especially, default transistors` saturation voltage level scaling is not at the expected level when compared to supply voltage scaling. According to this, common topologies suffer from unsatisfied operation conditions and that leads us to find and use a topology which satisfies our limitations.

The balanced differential pair based CCCII circuit is the improved version of unbalanced modified differential pair CCCII circuit [22]. The asymmetric dynamic range property of the previous circuit is reduced with this balanced structure by adding a dedicated Y-Branch for producing output as the structure in Figure 3.15, which is also operated as CCCII+ [22].

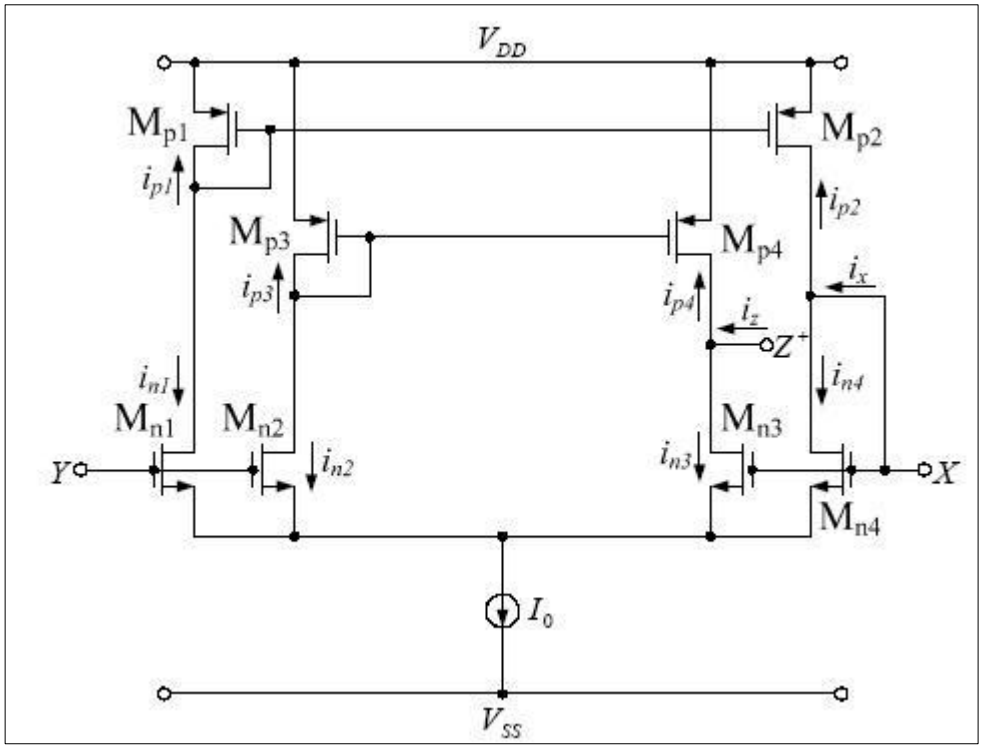

Figure 3.15 : Balanced differential-pair CMOS CCCII+ [22].

The current-relationship between port X and Z of the balanced differential-pair CCCII can be expressed as [22]:

$$i_x = i_{p2} + i_{n4} \cong i_{p4} + i_{n3} \cong i_z \tag{3.6}$$

The output resistance of any Z-port of the balanced differential-pair CCCII is simply characterized based on the attached MOSFETs as [22]:

$$r_o = 1/(g_{ds}^{PMOS} + g_{ds}^{NMOS}) \tag{3.7}$$

The terminal resistance (r_x) is still dependent on the transconductance of NMOS differential-pair (g_{md}), which can be expressed as [22, 23]:

$$R_x = (v_x - v_y)/i_x \cong \left|1/g_{md}\right| \cong 1/\sqrt{\mu_n C_{ox}\frac{W_n}{L_n} I_o} \tag{3.8}$$

Lastly, in the balanced differential-pair structure, as $V_x >> V_y$, M_{n1} and M_{n2} are virtually off, while nearly conduct whole bias-current when $V_x << V_y$. Therefore $I_X^{\max}$ and $I_X^{\min}$ can be approximated to equation **3.9** [22]:

$$I_x^{max} \cong \left| I_x^{min} \right| \cong \frac{I_0}{2} \quad \textbf{(3.9)}$$

Therefore, the estimation of symmetrical dynamic-range of the balanced structure is [22]:

$$|V_{XY}| \leq \sqrt{I_o / (\mu_n C_{ox} \frac{W}{L})} \quad \textbf{(3.10)}$$

From the given equations of the circuit, it seems feasible for the implementation.

3.5 Design of Balanced Differential Pair Based CCCII

The balanced differential-pair CCCII structure is realized as stated in literature [22], with two Z+ output ports to provide design flexibility in frequency agile filter implementation. It is also possible to add inverted outputs or more non-inverting outputs under some constraints [22].

The circuit is designed with STMicroelectronics 28nm CMOS process default transistors, ±0.5V supply voltages and simulations are held by Spectre. Minimum length of the transistors used in the design is selected as 120nm, which is 4 times of the minimum allowed value 30nm, to increase finite output resistance values.

The designed balanced differential-pair MOSFET CCCII structure is displayed in Figure 3.16. As it was previously mentioned, structure consists of the transistors M1, M4, M11 and M12 is added to obtain second Z output from the basic structure. The mentioned transistors are also configured with the related aspect ratios to prevent any inconsistency between two Z output ports.

MOSFETs W/L ratios are listed in Table 3.2 based on common channel length 120nm.

Table 3.2 : Transistor ratios of balanced differential pair based CCCII.

Transistor	W/L Ratio
M_1-M_6	20
M_7-M_{10}	30
M_{11}-M_{16}	50

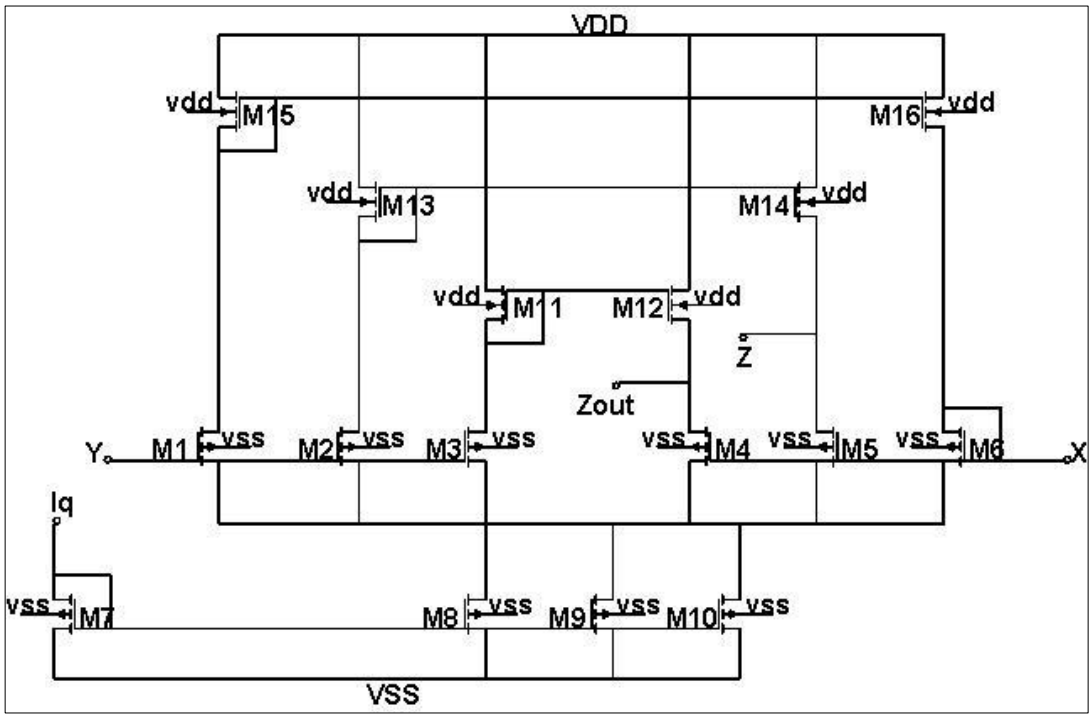

Figure 3.16 : Designed balanced differential-pair CCCII structure with two Z ports.

3.5.1 Main characteristics of designed CCCII circuit

In a general CCCII structure, many specifications are considered when describing its overall performance. Since the thesis is mainly concerned with the frequency agile filter implementation of the balanced differential pair CCCII structure, important properties will be covered.

In order to verify the balanced differential pair based CCCII architecture that is explored in previous section, Spectre simulator is used. It is a part of the Cadence package. Design kit of the STMicroelectronics 28nm process was used with default defined GO1 transistors. Every simulation characteristic is observed with the dedicated simulation setups of the designed circuit.

The characteristic of R_x relating to 10µA bias-current is presented in Fig. 3.17. Its frequency-dependence can be easily approximated by a model having one real zero and a pair of complex poles.

Observing Figure 3.17, the resistance value seen on port x remains flat up to 1.45GHz frequency values, which is very efficient for our application range.

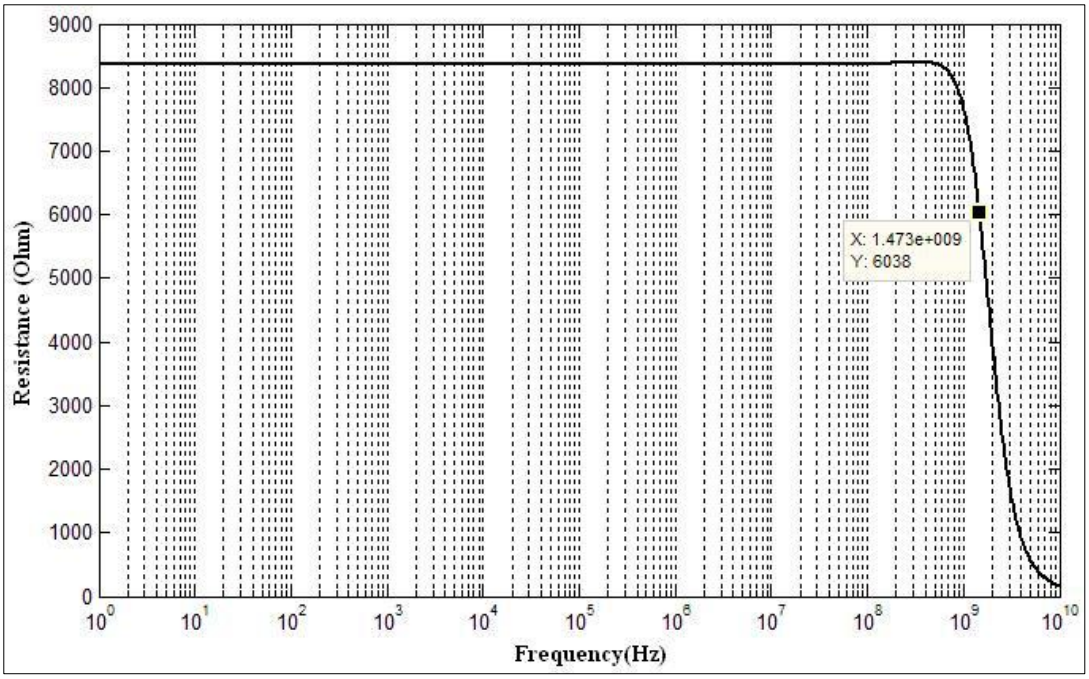

Figure 3.17 : R_x based on I_0=10µA.

The large signal characteristics are simulated again at 10µA bias-current to prove the compatibility of the used balanced differential pair based structure and the CCCII theorem.

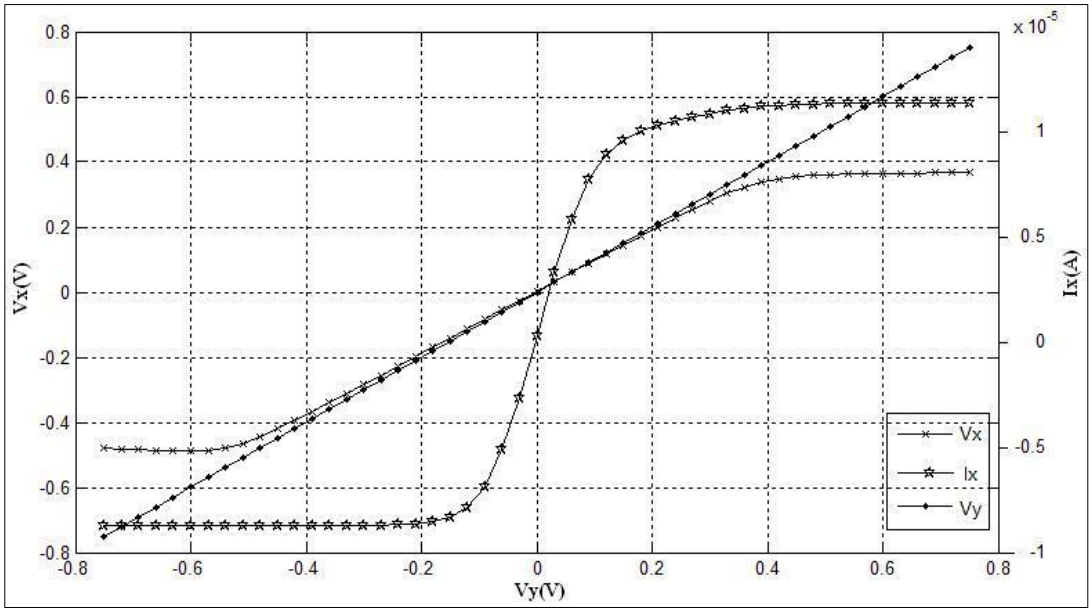

Figure 3.18 : The voltage transfer and voltage-current characteristics of CCCII.

In Figure 3.18, the voltage transfer characteristics are plotted, which is showing the exact voltage following performance of Y and X. Additionally, the V-I characteristic of the input voltage versus the input current at port X is revealed in the same figure.

This behavior verifies the approximated balanced dynamic range and very low offset voltage.

The small-signal current transfer gain characteristic of the designed CCCII circuit is plotted in Figure 3.19. The 3-dB bandwidth of current gain for 10µA bias-current can be approximately read as 1.85GHz.

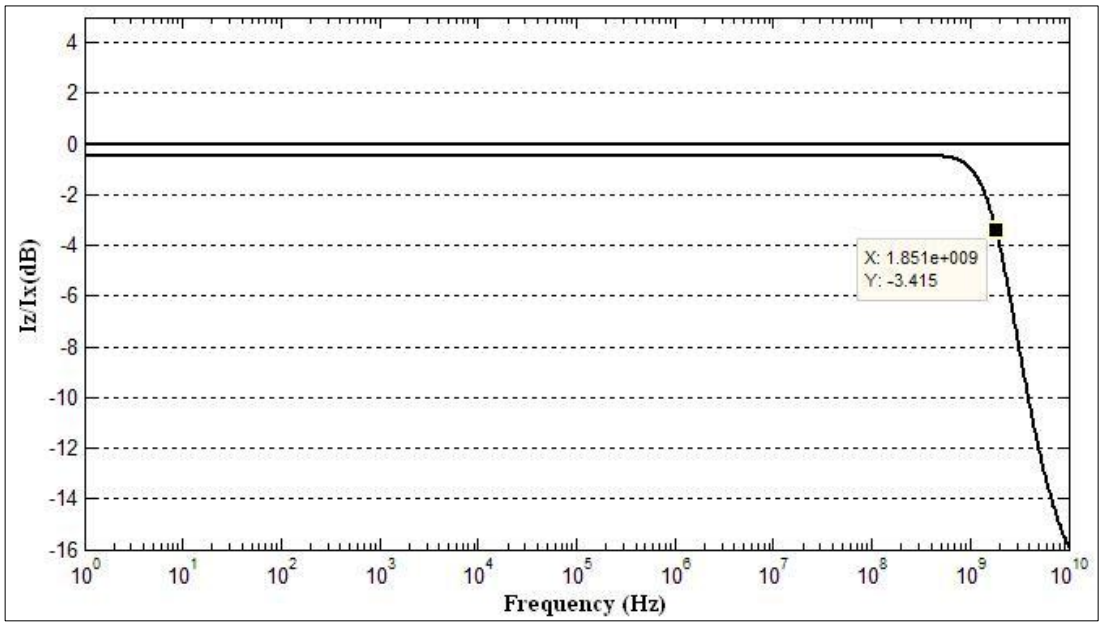

Figure 3.19 : The small-signal characteristic of the current transfer gain.

At corresponding bias current, the frequency characteristics of the designed circuit in operation can be assumed to be dominated by terminal resistance bandwidth. This can be also referred as open loop bandwidth of the circuit.

The transient current follow between port Z and X is shown in Figure 3.20 for 500MHz signal input.

As it can be observed easily, current transfer behavior of the circuit is satisfactory up to high frequency values.

In parallel to all characteristics, power consumption of the circuit is observed as 34.08µW.

All in all, after observing main large and small signal behaviors of the designed CCCII circuit, it is very clear that it is suitable for high frequency applications with the advantages of high end process node of 28nm.

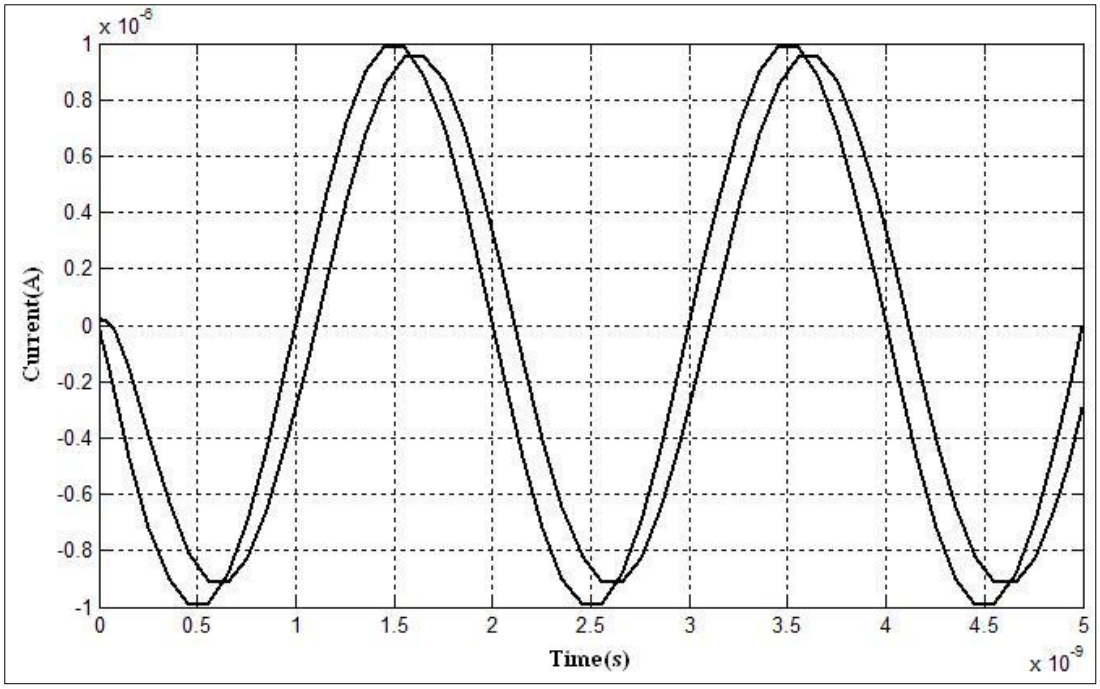

Figure 3.20 : Transient current transfer characteristic between ports X and Z.

3.5.2 Corner simulation characteristics of designed CCCII circuit

Corner simulation for the designed CCCII circuit is also executed to see circuit behavior under industrial standards. To do this, in addition the default process variables scattering, temperature max-min variables defined as -40˚C and 110˚C, bias current scattering factor is defined as %25, which leads to 7.5µA and 12.5µA for a 10µA bias current and finally supply voltage scattering factor is defined as %10, which leads to ±0.45V and ±0.55V for a ±0.5V supply voltage.

In order to verify the balanced differential pair based CCCII architecture that is explored in previous sections, 72 different corners are obtained with the 8 different corners defined over temperature, supply voltage and bias current. Other 9 variables are related to rcmax and rcmin scatterings with respect to process variables.

The characteristics of R_x relating to corner analysis results are presented in Fig. 3.21.

Observing Figure 3.21, the resistance value seen on port x takes the maximum value 13.14kΩ that remains flat up to 2.10GHz for 7.5µA bias current, ±0.45V supply voltage, 110˚C temperature and 5.35kΩ that remains flat up to 5.10GHz for 12.5µA bias current, ±0.55V supply voltage, -40˚C temperature.

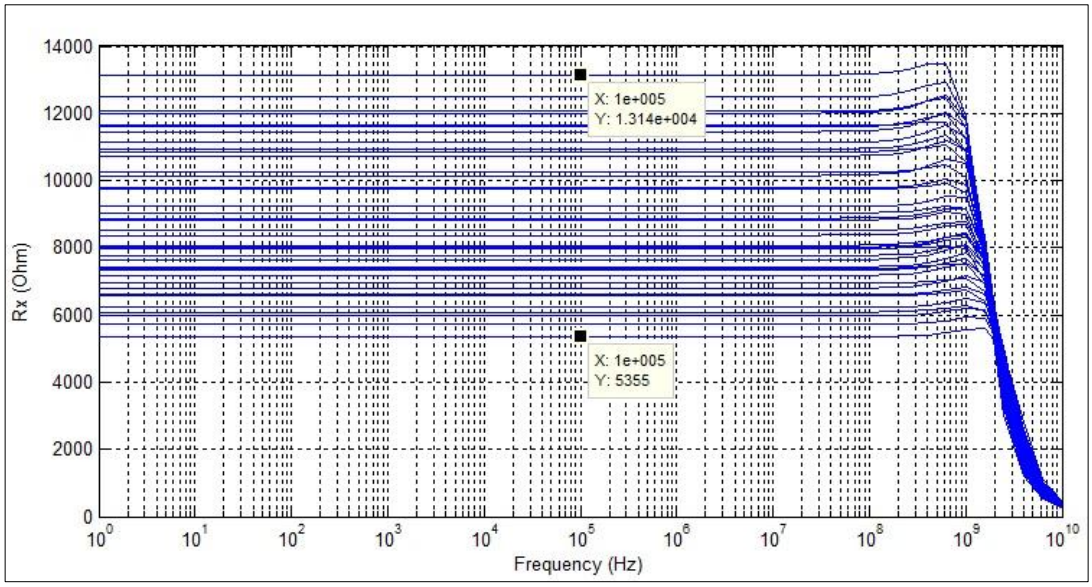

Figure 3.21 : R_x based on 72 different corners.

The large signal characteristics of the designed balanced differential based CCCII structure are simulated again for 72 different corners to observe and review the behavior of the circuit.

In Figure 3.22, the voltage transfer characteristics are plotted, which is showing the exact voltage following performance of Y and X for corners.

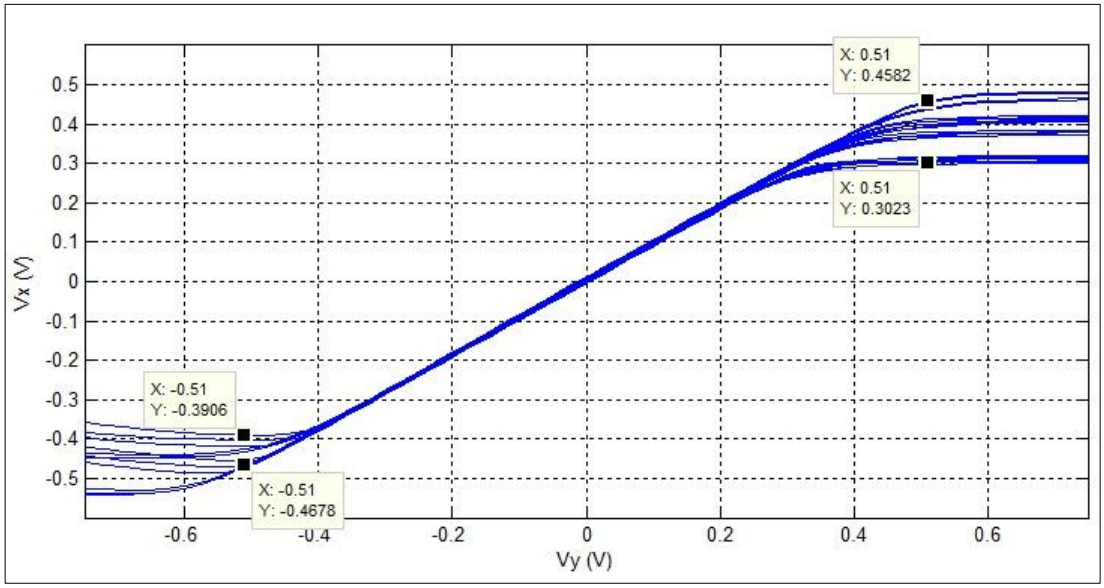

Figure 3.22 : The voltage transfer characteristics of CCCII for corner analysis.

This figure verifies the approximated balanced dynamic range and very low offset voltage for different cases.

Maximum dynamic range linearity is observed for 12.5µA bias current, ±0.55V supply voltage, 110˚C temperature and minimum dynamic range linearity is observed for 7.5µA bias current, ±0.45V supply voltage, -40˚C temperature.

Observing Figure 3.22, maximum offset voltage seen at port x for zero input voltage is 13.6mV for operating conditions 7.5µA bias current, ±0.55V supply voltage, 110˚C temperature and minimum offset voltage seen at port x for zero input voltage is 177µV for 12.5µA bias current, ±0.45V supply voltage, -40˚C temperature.

The characteristic of the input voltage versus the input current at port X is revealed in Figure 3.23 for the emphasized corner cases. Maximum offset current flowing through port x is observed as 1.8µA for operating conditions at 12.5µA bias current, ±0.55V supply voltage, 110˚C temperature. Minimum offset current flowing through port x is observed as 24nA for operating conditions at 12.5µA bias current, ±0.45V supply voltage, -40˚C temperature.

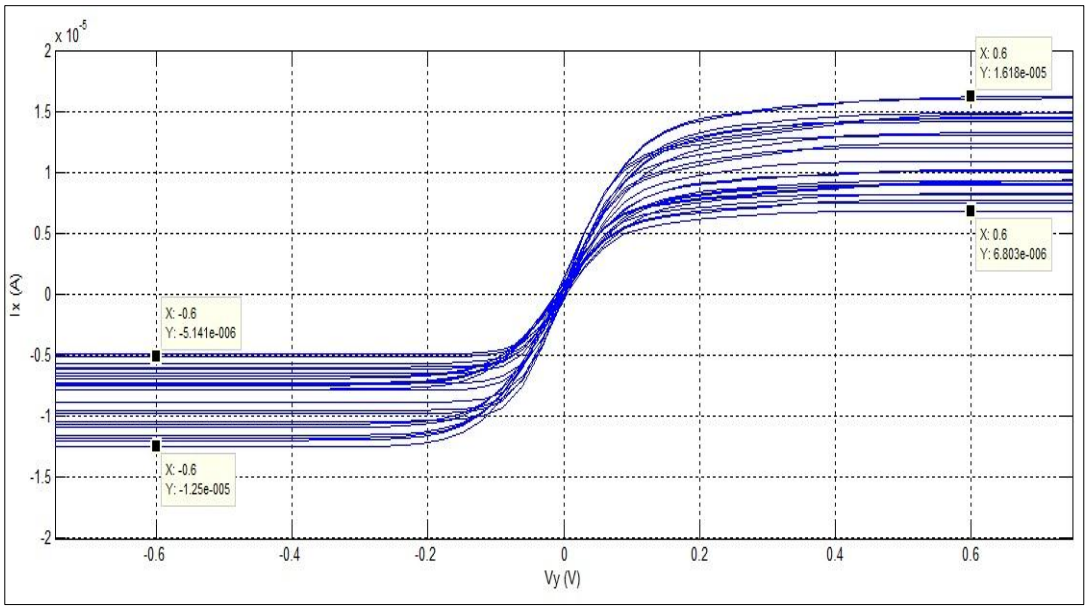

Figure 3.23 : The voltage current (Vy-Ix) characteristics of CCCII for corner analysis.

As an additional investigation, operating condition that allows maximum current flow at port x will be observed as 12.5µA bias current, ±0.55V supply voltage, 110˚C temperature. At this operating condition maximum current observed at positive supply is 17.46µA and at negative supply 13.42µA. In the meantime, operating condition that allows minimum current flow at port x will be observed as 7.5µA bias

current, ±0.45V supply voltage, -40˚C temperature. At this operating condition maximum current observed at positive supply is 6.79µA and at negative supply 4.89µA.

The small-signal current transfer gain characteristic of the designed CCCII circuit is plotted in Figure 3.24 for the mentioned corner cases. Maximum value observed for current transfer ratio is -368mdB for 7.5µA bias current, ±0.55V supply voltage, -40˚C temperature and minimum value observed for current transfer ratio is -668mdB for 7.5µA bias current, ±0.45V supply voltage, 110˚C temperature. Additionally, the 3-dB bandwidth of current gain for different cases can be approximately read as maximum 3.75GHz for 12.5µA bias current, ±0.55V supply voltage, -40˚C temperature and it is read as minimum 1.51GHz for 7.5µA bias current, ±0.45V supply voltage, 110˚C temperature.

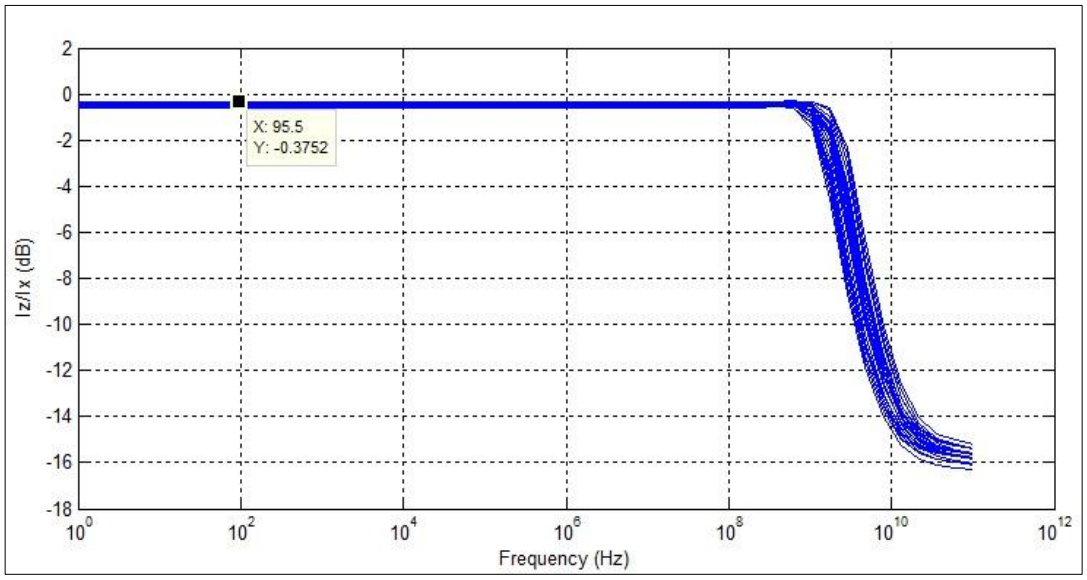

Figure 3.24 : The frequency current (Iz/Ix) characteristics of CCCII for corner analysis.

4. UNIVERSAL FILTER APPLICATION

In this section, the design and implementation of a universal filter with translinear dual output CCCII will be discussed in details. This application is selected for the designed CCCII structure to demonstrate current mode operation of the circuit effectively. In addition to this, the designed second order universal filter will be suitable in a wide range of IC technologies because of the absence of external resistors, its electronically adjustable behaviors and smaller number of active and passive elements used in the design.

The designed filter will provide compactness for different types of filters in a single structure, that makes the circuit a great alternative to currently used bigger, passive and multi element designs.

4.1 Design of Filter

In this study, it is targeted to provide a universal filter implementation for multi type filtering responses to be used as a compact alternative to available passive filter structures. In this part of the study, implementation of the universal filter will be discussed in details.

The universal filter used in this study is based on the proposed structure by Xi and the team [24]. The concept and the theory of the designed circuit will be shortly described in th following paragraphs to obtain mentioned universal filter.

The schematic representation of the implemented new universal filter with single-input, triple-output emloying only four elements is presented in Figure 4.1 [24].

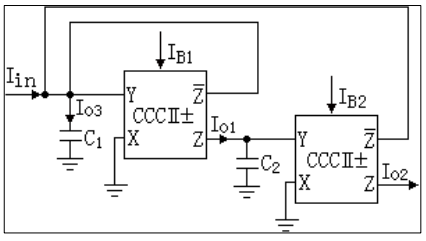

Figure 4.1 : Current-mode universal filter [24].

As it can be easily derived from the given figure, the filter contains only two capacitances as passive elements and does not require any additional any passive resistance.

Node equations are the starting points to extract characteristic of the designed filter. This structure can be characterized by the following expressions [24]:

$$\frac{I_{in} - I_{o1} - I_{o2}}{C_1 s} - I_{o1} R_{x1} = 0 \qquad \textbf{(4.1)}$$

$$\frac{I_{o1}}{C_2 s} - I_{o2} R_{x2} = 0 \qquad \textbf{(4.2)}$$

From the given expressions, bandpass, lowpass and highpass filter response functions of this circuit will be given as follows [24]:

$$F_{BP}(s) = \frac{I_{o1}}{I_{in}} = \frac{R_{x2} C_2 s}{R_{x1} C_1 R_{x2} C_2 s^2 + R_{x2} C_2 s + 1} \qquad \textbf{(4.3)}$$

$$F_{LP}(s) = \frac{I_{o2}}{I_{in}} = \frac{1}{R_{x1} C_1 R_{x2} C_2 s^2 + R_{x2} C_2 s + 1} \qquad \textbf{(4.2)}$$

$$F_{HP}(s) = \frac{I_{o3}}{I_{in}} = \frac{R_{x1} C_1 R_{x2} C_2 s^2}{R_{x1} C_1 R_{x2} C_2 s^2 + R_{x2} C_2 s + 1} \qquad \textbf{(4.3)}$$

The designed universal filter structure also produces band reject and all pass filter responses simultaneously with the other responses as given in the following equations [24]:

$$F_{BR}(s) = \frac{I_{o2} + I_{o3}}{I_{in}} = \frac{R_{x1} C_1 R_{x2} C_2 s^2 + 1}{R_{x1} C_1 R_{x2} C_2 s^2 + R_{x2} C_2 s + 1} \qquad \textbf{(4.4)}$$

$$F_{AP}(s) = \frac{-I_{o1} + I_{o2} + I_{o3}}{I_{in}} = \frac{R_{x1}C_1R_{x2}C_2s^2 - R_{x2}C_2s + 1}{R_{x1}C_1R_{x2}C_2s^2 + R_{x2}C_2s + 1} \quad \textbf{(4.5)}$$

For the designed universal filter topology, the natural frequency and the quality factor equations can be given as [24]:

$$\varpi_0 = \frac{1}{\sqrt{R_{x1}C_1R_{x2}C_2}} \quad \textbf{(4.6)}$$

$$Q = \sqrt{\frac{R_{x1}C_1}{R_{x2}C_2}} \quad \textbf{(4.7)}$$

The implemented design will satisfy and provide the functionality of the given expressions **4.1** to **4.7**. It is aimed in this thesis to provide an example application case for translinear CCCII usage.

4.1.1 Second order universal filter design

In this part of the thesis, second order universal filter design steps will be covered and detailed. Since the structure needs dual output CCCII structures as shown in Figure 4.1, an adapted version of the CCCII with dual outputs is designed as shown in Figure 4.2.

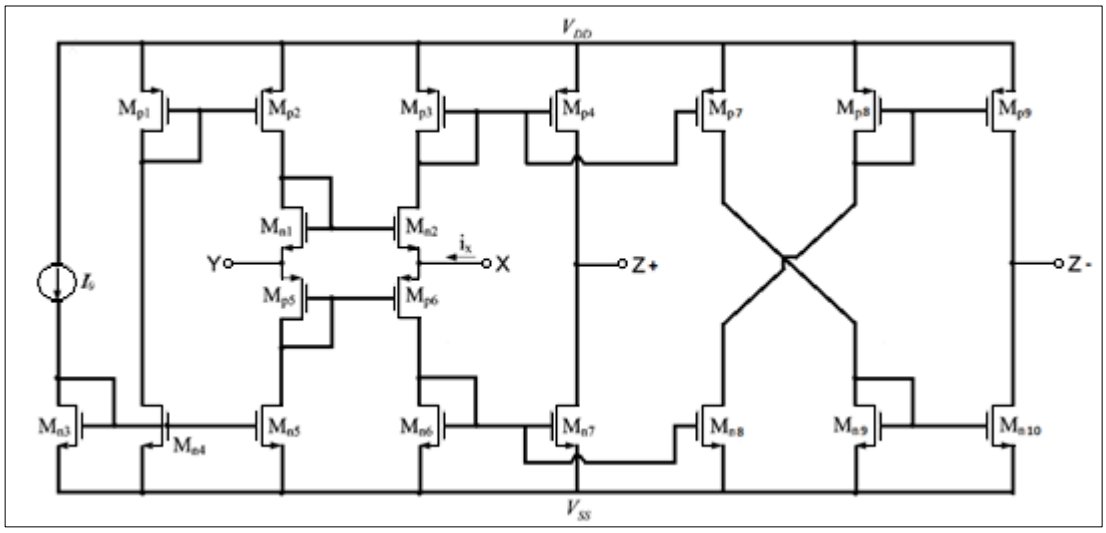

Figure 4.2 : Dual output CMOS CCCII structure.

In the designed structure, aspect ratios of the MOSFETs used in the additional part are same as the ratios of the mirrored transistors.

As it is investigated in previous section, implemented filter produces bandpass, lowpass, highpass, band reject and all pass responses simultaneously with respect to given expressions.

The main important advantage of the filter is that it provides universal filter behavior with triple output by employing only four elements and not any additional passive resistance.

4.1.1.1 Main characteristics

The universal filter structure in Figure 4.1 is implemented in the 28 nm CMOS GO2 technology from STMicroelectronics same as the translinear CCCII and dual output CCCII circuit. The CCCII structure shown in Figure 4.2 was used and the filter circuit is biased under ±0.9V which is the original supply voltage supported by GO2 process. Common bias current for two dual output translinear CCCII circuits is chosen as 10µA.

The validity of the designed universal filter is verified using Spectre environment. For these simulations, capacitance values are selected to have square shaped capacitances for matching issues, as 3.96pF. Figures given in the following paragraphs show different filter responses observed simultaneously at different ports of the filter.

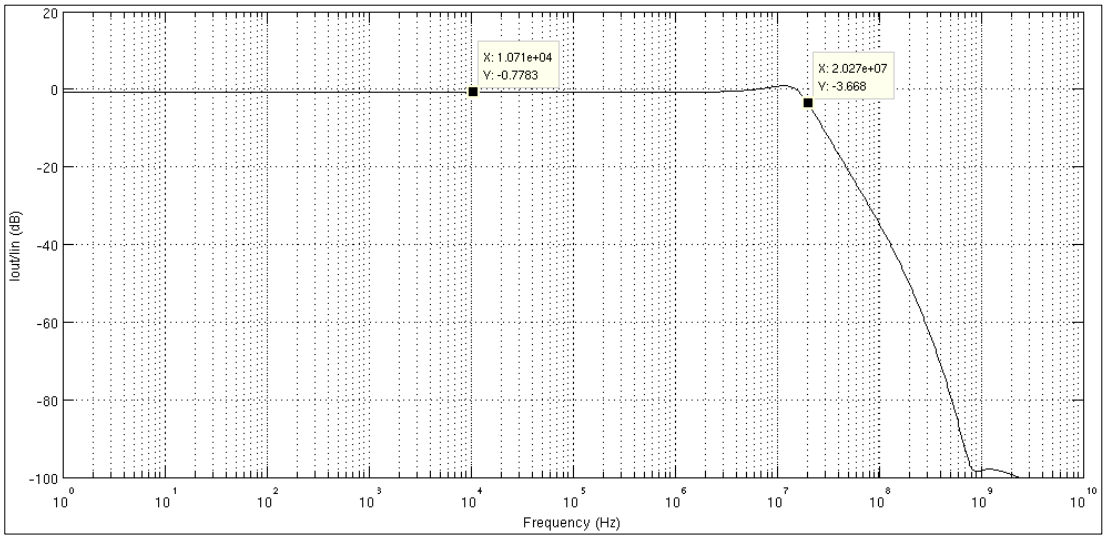

Figure 4.3 : Lowpass frequency response of second order universal filter.

From the given figure, it is clear that the frequency response of the filter is lowpass and its gain in pass band is nearly 0.93. Observed behavior is not perfect but will be used efficiently for filtering purposes with adjustments.

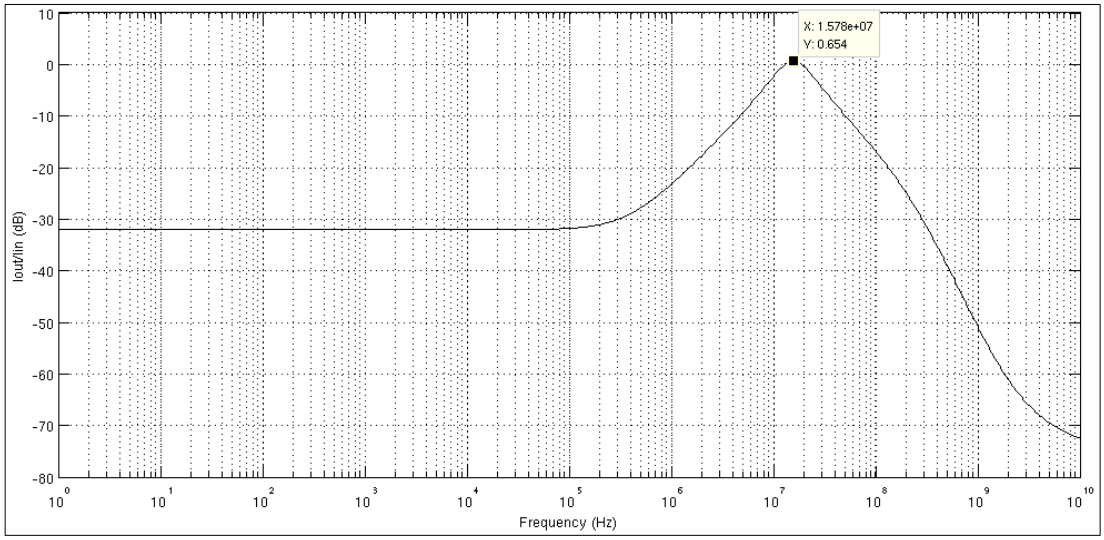

Figure 4.4 : Bandpass frequency response of second order universal filter.

Figure given above demonstrates a bandpass behavior which is obtained simultaneously from the implemented filter output. Its pass band gain is nearly 1.07 and filtering bands are appropriate for second order filtering.

As an other investigation, implemented filter also provides highpass frequency response which is shown in the following figure. Again, passband gain of the filter is efficient enough to be used for dedicated purposes.

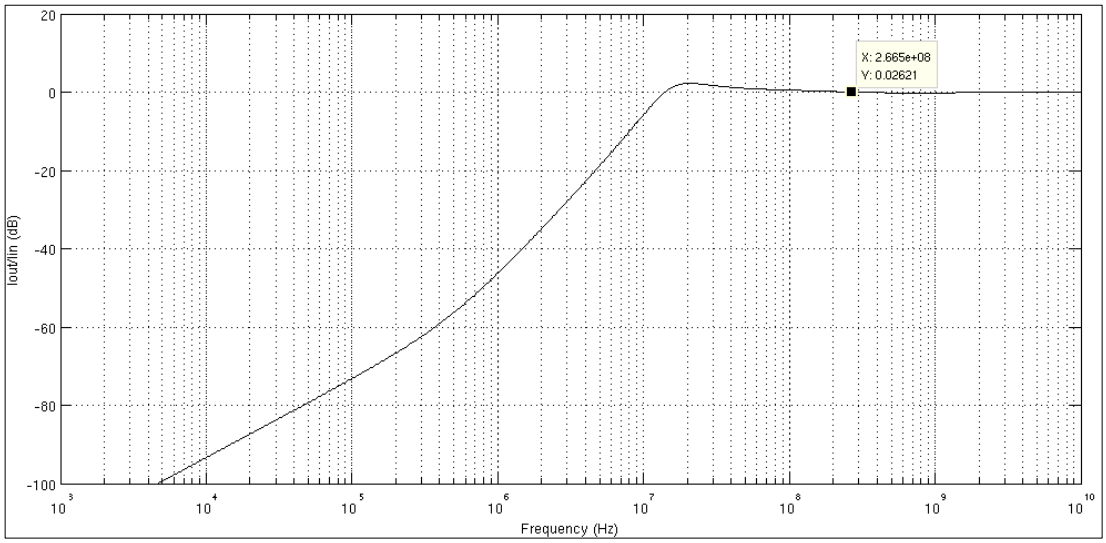

Figure 4.5 : Highpass frequency response of second order universal filter.

As it is stated in the definition section for the universal filter, it is important to notice that, filter provides simultaneous compact frequency responses for different types of filters. Three main filter responses shown and allpass and notch filter responses will also be obtained from the node operation combinations of the mentioned main responses.

5. FREQUENCY AGILE FILTER APPLICATION

In this part of the thesis, the design and implementation of the frequency agile filter will be discussed in details. Before focusing on the design, some specific properties` definitions will be given to prevent any misunderstanding of these advantageous behaviors.

The range of adjustment of the center frequency f_0 of the filters is defined in several ways by various researchers and authors. Among all, one definition is very clear and easy to use as a step for further declarations [9]. By supposing that the center frequency f_0 is adjustable between two values noted $f_{0\min}$ and $f_{0\max}$, we will call n the ratio [25]:

$$\frac{f_{0\max}}{f_{0\min}} = n \qquad \textbf{(5.1)}$$

The convention "n:1" is also often used to denote expression (**5.1**). In order to express the range of adjustment of frequency f_0 appropriately, it is also necessary to provide the frequency value of $f_{0\min}$ and $f_{0\max}$ [9]. For instance, two adjustable filters that have a range n:1 are not equivalent if the values of $f_{0\min}$ are different (100MHz and 1GHz, for example).

5.1 Tunability, Reconfigurability and Agility

The concepts of tunability and reconfigurability, especially in filter design, are very often used interchangeably in the literature [9]. With respect to this, it is very necessary to build a definition for the concept of reconfigurability and tunability. A tunable filter can be defined as a filter whose tuning of f_0 is carried out only very close to f_0 and its prior aim is to compensate drifts related to thermal, technological and etc parameters. On the other hand, in a reconfigurable filter, the tuning of the f_0

frequency is expected to be carried out over a very wide range of frequency when compared to a tunable filter [3].

To overcome the problem of using definitions interchangeably, a stable definition is provided by Fabre and his team. According to this definition, a tunable filter is a filter for which the tuning range is lower than 2:1; i.e. $f_{0\max} < 2f_{0\min}$ and a reconfigurable filter is a filter for which the tuning range is higher than 2:1, which leads to $f_{0\max} > 2f_{0\min}$ [3]. It's also important to note down that to be completely reconfigurable, a filter must have an adjustable quality factor [3].

Apart from the definitions of reconfigurable and tunable, it is also necessary to define agility concept. Agility will be defined as the property of hopping between two consecutive frequencies f_1 and f_2 very quickly during the transmission of the signal, without any prevention on the signal processing [3]. According to this, a frequency agile filter will be a reconfigurable filter with the property of agility. Such a filter is perfect candidate to be used in cognitive radio and encrypted communication systems.

5.2 Design of Filter

It's aimed in this thesis to provide a new application solution for multi band communication systems, especially global positioning. To realize the possibility, a frequency agile structure is extremely needed to quickly reply to the needs of five bands containing global positioning systems, GPS, Glonass, Galileo, Beidou, GNSS. In this part of the thesis, frequency agile filter implementation will be discussed in details.

The implementation of the frequency agile filter is based on the proposed structure by Fabre and the team [4]. In the following paragraphs, the theory making use of voltage mode circuits and current mode circuits will be briefly given to obtain the agile filters.

The structure is mainly based on a classical second order filter structure with two different outputs at least: band-pass and low-pass [3]. Figure 5.1 shows the classical voltage mode second order filter circuit with two outputs. This cell is called as class

0 filter which is the basic element for the implementation of a frequency agile filter [9].

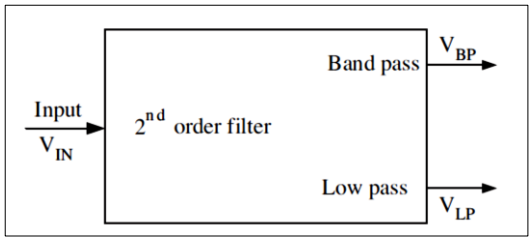

Figure 5.1 : Basic second order filter including two different outputs [4].

The input voltage of the filter is V_{in}, its band pass and low pass outputs are V_{BP} and V_{LP}. Transfer functions for the two outputs are [4]:

$$F_{BP}(s) = \frac{V_{BP}}{V_{IN}}(s) = \frac{a's}{1 + as + bs^2} \tag{5.2}$$

$$F_{LP}(s) = \frac{V_{LP}}{V_{IN}}(s) = \frac{d'}{1 + as + bs^2} \tag{5.3}$$

The values of the constants a, b, a` and d` allow us to determine the characteristic parameters of the filter. In these equations, a and b are real positive constants to ensure stability of the filter and we also suppose that a` and d` are real positive constants [4].

Table 5.1 summarizes the characteristics of the starting filter shown in Figure 5.1.

Table 5.1 : Characteristic parameters of the filter in figure 5.1.

	Basic Circuit
Center frequency	$f_0 = \frac{1}{2\pi\sqrt{b}}$
Q-factor	$Q = \frac{\sqrt{b}}{a}$
BP Gain	$G_{BP} = \frac{a`}{a}$
BP: -3dB Bandwidth	$\Delta f = \frac{a}{2\pi b}$
LP Gain	$G_{LP} = d`$

As a reminder for the equations given for the basic filter, generally the gains of the two outputs will be greater than or equal to unity, i.e. a`≥a and d`≥1.

Figure 5.2 shows the new second order frequency agile filter circuit obtained from the basic cell given by Figure 5.1. It is called by the team as class 1 frequency agile filter [9]. The main difference of this implementation with respect to the basic design is the amplification of the low pass output with an adjustable gain A and its addition to the input voltage of the previous filter structure.

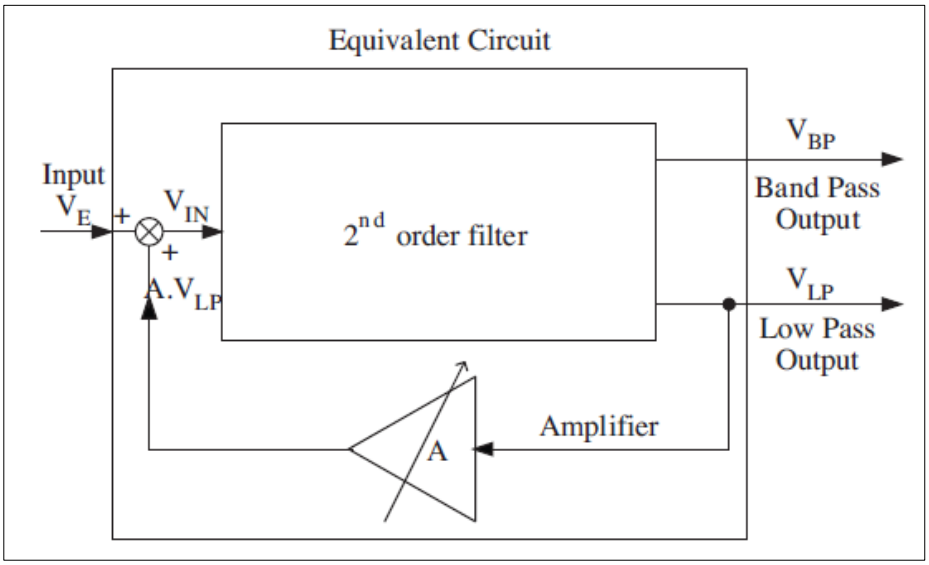

Figure 5.2 : Frequency agile filter made from the basic cell [9].

The new input voltage of the filter is then V_E and the circuit includes the same two outputs: V_{BP} and V_{LP}.

Figure 5.3 shows the necessary modifications of the (n-1) class agile filter block.

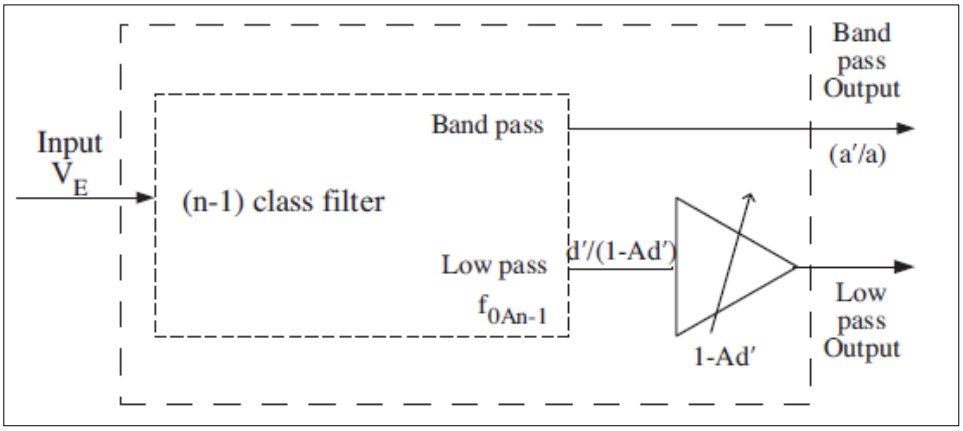

Figure 5.3 : Necessary modifications of the (n-1)th class agile block [9].

The input signal of the new circuit is now given by the formula $V_E = V_{IN} - AV_{LP}$. Its corresponding tranfer function for the band pass output is then:

$$F_{BP}(s) = \frac{V_{BP}}{V_E}(s) = \frac{\frac{a's}{(1-Ad`)}}{1+\frac{as}{(1-Ad`)}+\frac{bs^2}{(1-Ad`)}} \qquad \textbf{(5.4)}$$

$$F_{LP}(s) = \frac{V_{LP}}{V_E}(s) = \frac{\frac{d'}{(1-Ad`)}}{1+\frac{as}{(1-Ad`)}+\frac{bs^2}{(1-Ad`)}} \qquad \textbf{(5.5)}$$

Table 5.2 summarizes the characteristics of the agile filter shown in Figure 5.2 and 5.3.

Transfer functions of the agile filter indicates that the new circuit will be stable provided that (1-Ad`) remains positive according to the Routh-Hurwitz criterion.

Table 5.2 : Characteristic parameters of the frequency agile filter.

	Basic Circuit
Center frequency	$f_0 = \sqrt{(1-Ad`)}\,\frac{1}{2\pi\sqrt{b}}$
Q-factor	$Q = \sqrt{(1-Ad`)}\,\frac{\sqrt{b}}{a}$
BP Gain	$G_{BP} = \frac{a`}{a}$
BP: -3dB Bandwidth	$\Delta f = \frac{a}{2\pi b}$
LP Gain	$G_{LP} = \frac{d`}{(1-Ad`)}$

5.2.1 Class 2 frequency agile filter design

In this study, an agile filter at the class 2 for negative values of A is chosen for implementation. Since the gain of the amplifier is negative, $1-Ad'>1 \Rightarrow A<0$, the

center frequency f_{0An} of the circuit shown in Figure 5.4 is greater than the center frequency f_0 of the starting filter.

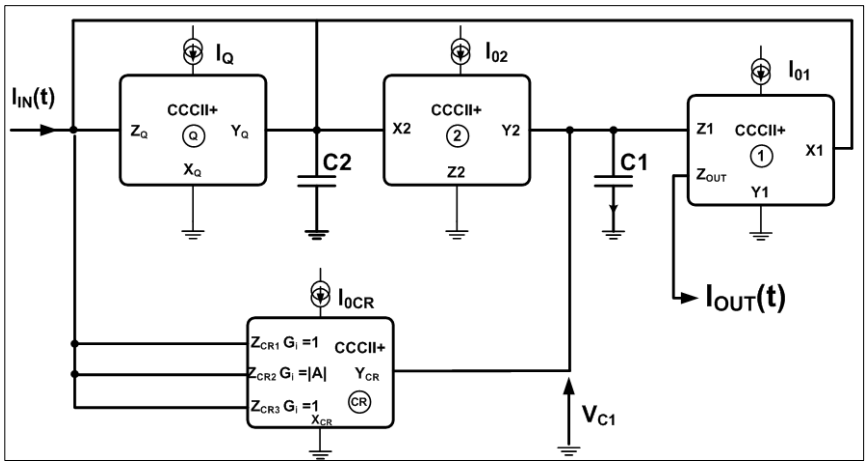

Figure 5.4 : Class 2 frequency agile filter with A<0 [4].

The different feedbacks will be possibly achieved by single or multi current conveyors(CR) at feedback line. Figure 5.5 shows the corresponding agile filter at the class 2 with multiple feedback current conveyors.

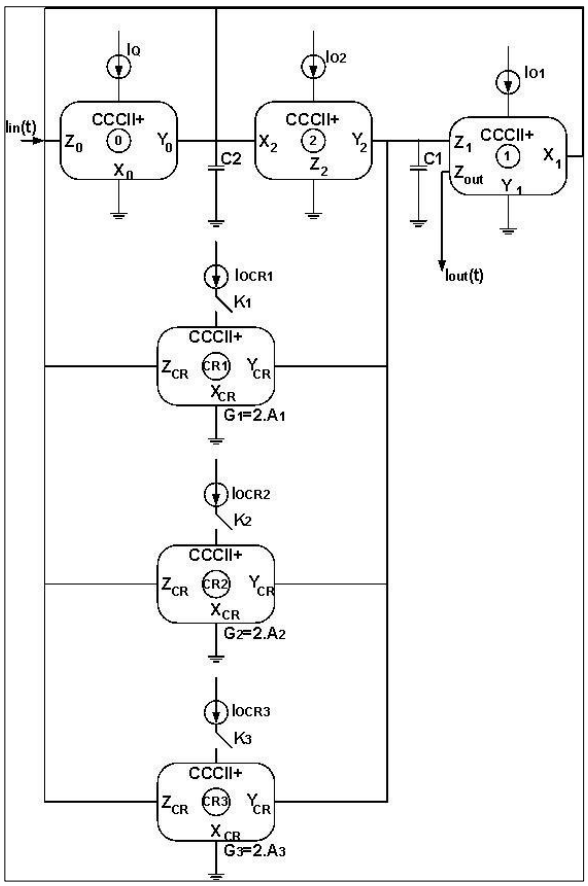

Figure 5.5 : Class 2 frequency agile filter with A<0 and multiple feedback CR.

Note that no more passive elements added to have agile filter for different center frequencies. The band pass output remains the same and the center frequency for any feedback will be:

$$f_{0An} = (1 - A) f_0 \tag{5.6}$$

One important advantage of the filter is, the output current is obtained at high impedance so, various elementary cells of Figure 5.5 can be connected in cascade without any need for any additional stage.

5.2.1.1 Main characteristics

The frequency agile filter structure in Figure 5.5 is implemented in the 28 nm CMOS technology from STMicroelectronics same as the CCCII circuit.

The CCCII structure investigated in section 3 was used and the filter circuit is biased under ±0.5V. Adjustment current I_Q is used to adjust center frequency gain of the circuit at 0dB. Common bias current for all implemented CCCII circuits is chosen as 10µA.

Frequency agile filter is exercised with different feedback values and Figure 5.6 to Figure 5.11 show different frequency responses obtained for the filter varying the position of the switches K_1 to K_3.

From the given figures, it is clear that the behavior is band pass and obtained response is the main frequency characteristic to be adjusted by the feedback paths.

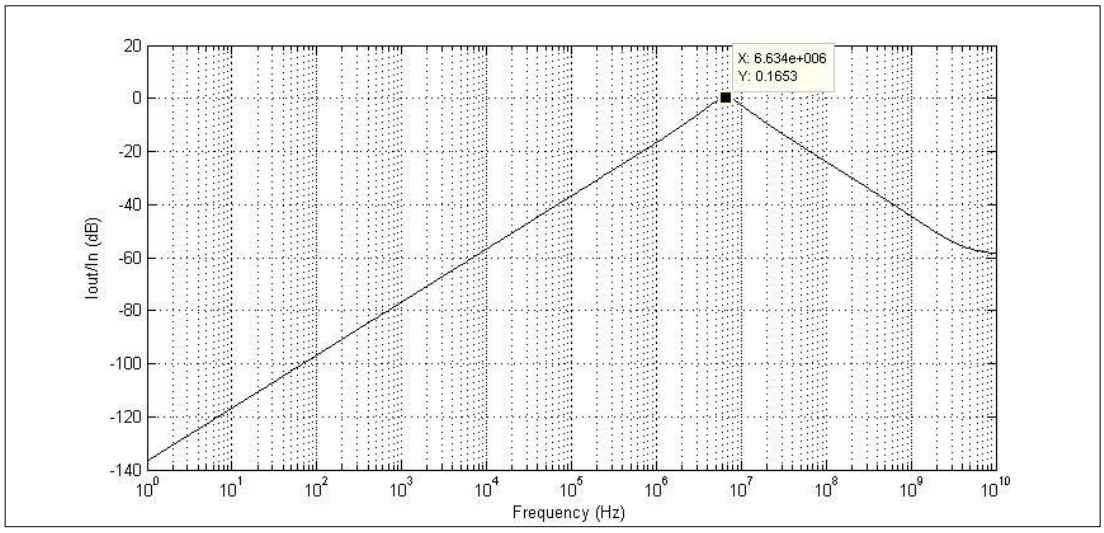

Figure 5.6 : Frequency response of class 2 filter without feedback.

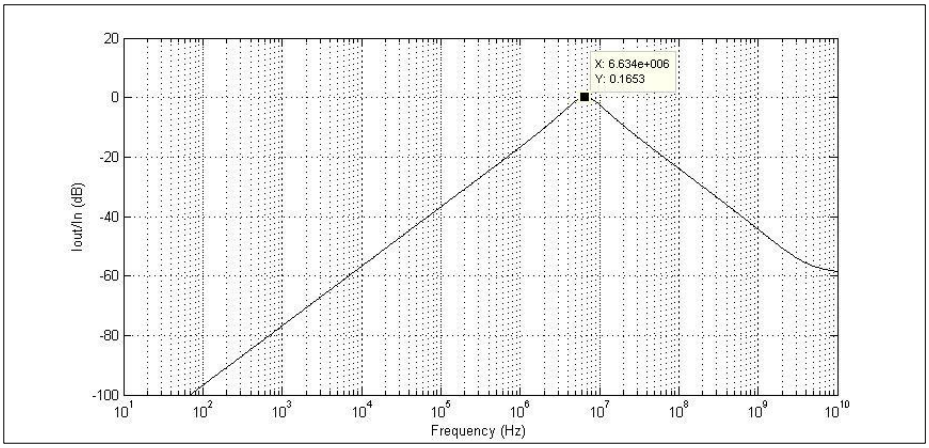

Figure 5.7 : A closer look to frequency response of class 2 filter without feedback.

Figure 5.8 and Figure 5.9 show feedback applied class 2 frequency agile filter frequency response. Feedbacks are applied with same currents in this case which made the feedback paths three times the same feedback.

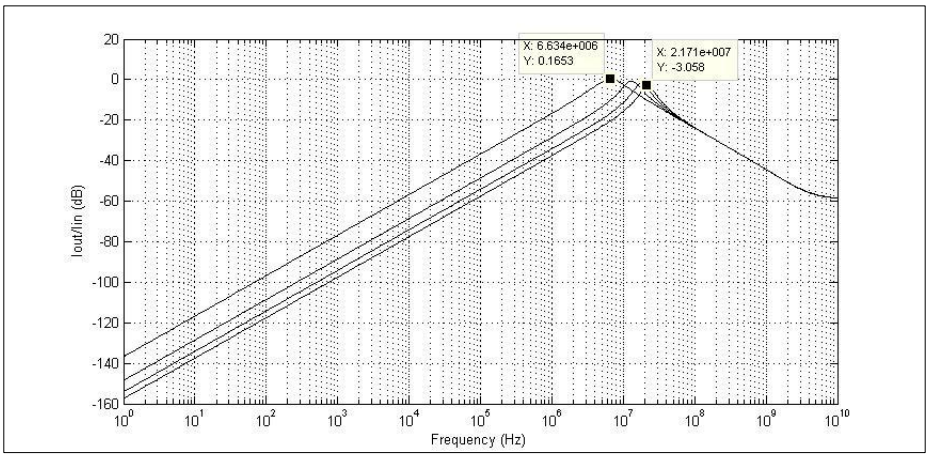

Figure 5.8 : Frequency response of class 2 filter with three times the same feedback.

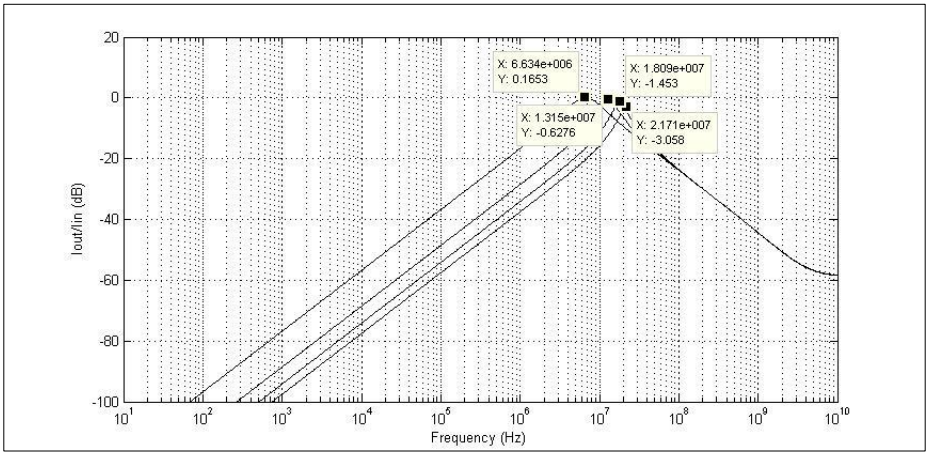

Figure 5.9 : A closer look to frequency response of class 2 filter with three times the same feedback.

Figure 5.10 and Figure 5.11 show feedback applied class 2 frequency agile filter frequency response with dedicated current feedbacks. Feedbacks are applied with different currents in this case which made the feedback paths dedicated.

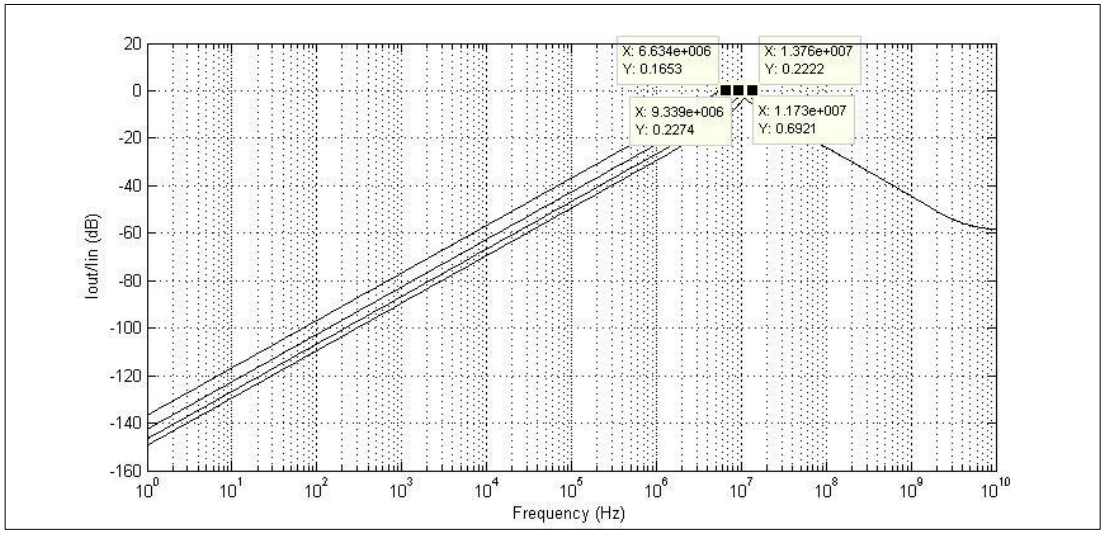

Figure 5.10 : Frequency response of class 2 filter with dedicated current feedbacks.

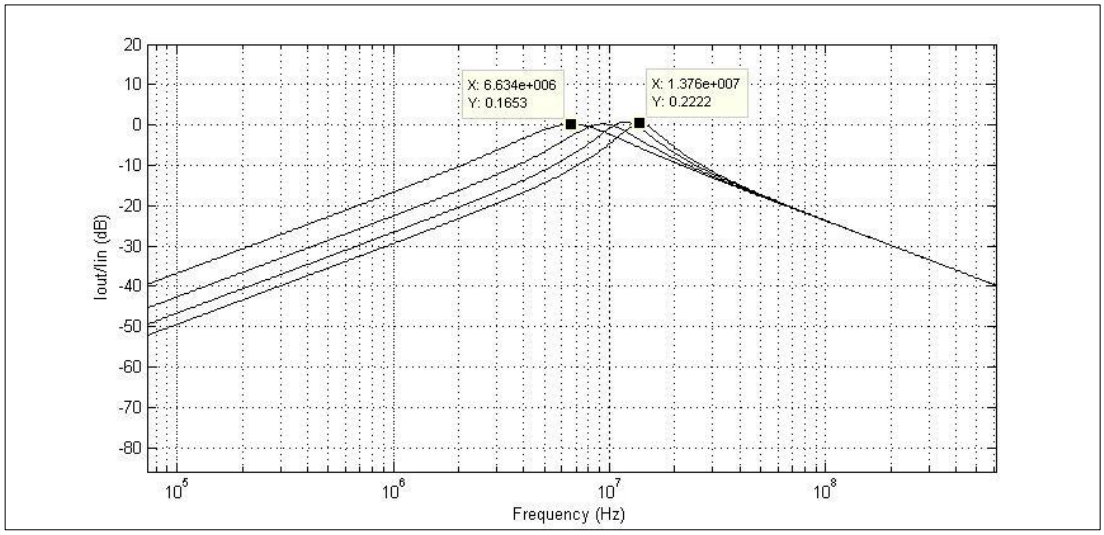

Figure 5.11 : A closer look to frequency response of class 2 filter with dedicated current feedbacks.

From the given figures, it is clear that the class 2 frequency agile filter response is obtained successfully for four different center frequencies. The best approach in this implementation is the structure obtained with dedicated current feedback paths. This is the more realistic structure to be implemented in an integrated circuit.

From the given investigations and the results obtained, it is clear that the structure is easily to implement and configure according to the needs of standard specifications.

5.2.2 Fourth order class 2 frequency agile filter design

In this study, a 4th order agile filter at the class 2 for negative values of A is chosen for implementation. This implementation is selected to provide an alternative solution to an industrial global positioning system filter which fully passive and currently in use.

The theoretical implementation in Figure 5.4 and practical implementation in Figure 5.5 is the main element of the designed filter. Cascaded connected class 2 filter topology is used for having a more compact and configurable structure which is also easy to adapt for various orders of filters. Implemented structure in block schema is shown in Figure 5.12. Each block in the figure represents the main block which is investigated deeply in previous section.

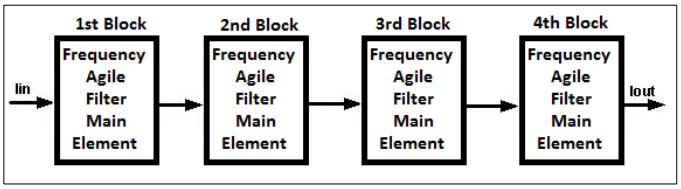

Figure 5.12 : Block schema of 4th order class 2 frequency agile filter.

Note that the filter consist of 4 cascaded main elements and all given formulas for the main structure are still valid, only order of filter increased with the given implementation. Moreover, no more passive elements added to have agile filter for different center frequencies again. The band pass output remains the same and the center frequency for any feedback will be as given in formula 5.6.

5.2.2.1 Main characteristics

The 4th order class 2 frequency agile filter structure in Figure 5.12 is implemented in the 28 nm CMOS technology from STMicroelectronics same as the CCCII circuit. The balanced differential pair based CCCII structure investigated in section 3 was used and the filter circuit is biased under ±0.5V. Adjustment current I_Q is used to adjust center frequency gain of the circuit at 0dB. Common bias current for all implemented CCCII circuits is chosen as 10µA.

4th order class 2 frequency agile filter is exercised with different feedback values and Figure 5.13 shows 4th order frequency responses obtained for the filter varying the position of the switches K_1 to K_3 with different feedback current values.

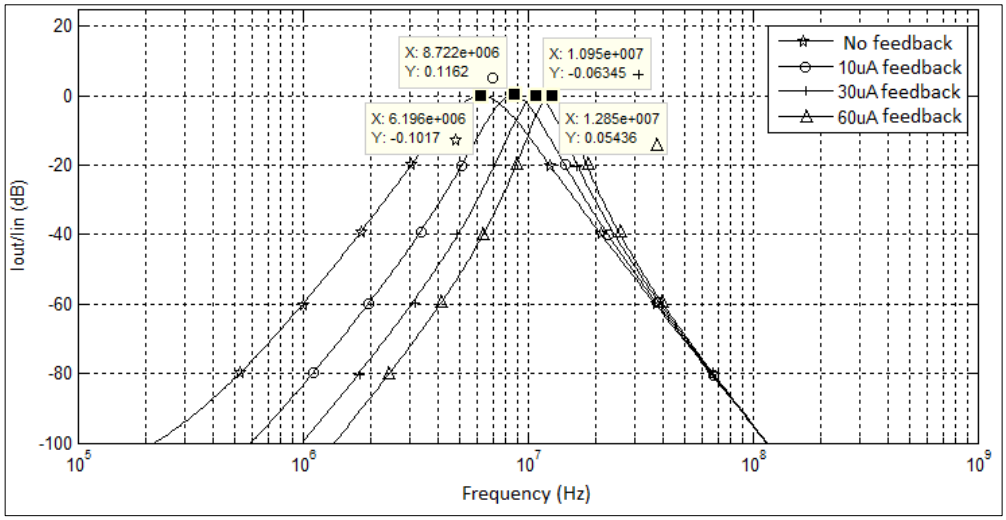

Figure 5.13 : A closer look to frequency response of 4th order class 2 filter with dedicated current feedbacks.

In the designed filter structure, four different band pass filter behaviors obtained for dedicated center frequencies as; 6.17MHz for feedback line off, 8.60MHz for 10µA feedback, 10.9MHz for 30µA feedback and 12.8MHz for 60µA feedback applied. For these cases, gain adjustment current is found as; 13.5µA, 14.4µA, 15.7µA and 17.3µA in order. It is clear that with the implemented circuit, frequency values between these values are easily achievable and it is also possible to support very high frequency responses by choosing feedback current value greater.

From the given figure, it is clear that the 4th order class 2 frequency agile filter response is obtained successfully for four different center frequencies. Implemented circuit structure is the more realistic implementation for integrated circuit design with dedicated current feedback paths.

6. LAYOUT AND POST-LAYOUT SIMULATIONS

The last and the most important step for any design activity is the layout drawing of the designed circuit in industrial processes. In this study, since the used one is an industrially available design kit library, it is also planned to implement layout drawing and post-layout simulations within the flow. From expressions to reality, all steps executed with respect to rule sets provided by the design kit provider company. As the first step after schematic design, layouts of the designed circuits` are draw by Layout XL tool. It`s important to note some points since this design kit is not a well-known or experienced one. During layout drawing, automatic poly layer routing needs to be disabled for the used transistors. Additionally, pin labeling should be done with labeling layers which is very new to other design kit users. Lastly, since it`s an encountered problem, automatic gate distance should be disabled since layout extraction will provide non-matching transistor gate layers in the layout. After layout drawing step, design rule checking done on the layout with Calibre DRC tool with full recommended rule sets. Next step through the flow is layout versus schematic (LVS) comparison. LVS comparison ran again with Calibre tool to see if there is any problem or mismatch between the schematic design and layout. The last step of the flow is extraction of the layout. Extraction of the circuit layout is executed with Mentor Graphics` toolset with name Calibre PEX, PVE. Extraction executed with full resistor and capacitance extraction and with respect to rule sets provided.

Extracted view is the last view of the design which is close to real implementation with different layers. For the sake of the circuit implementations, all recommended rule sets checked by the tools during each step.

6.1 Layout of The Translinear CCCII

Layout of the translinear CCCII structure is drew with respect to all mentioned items in previous sections. The transistors used in this design are bulk CMOS process transistors with specially doped gate oxide layer properties. These transistors are collected under the name of GO2 by the provider STMicroelectronics.

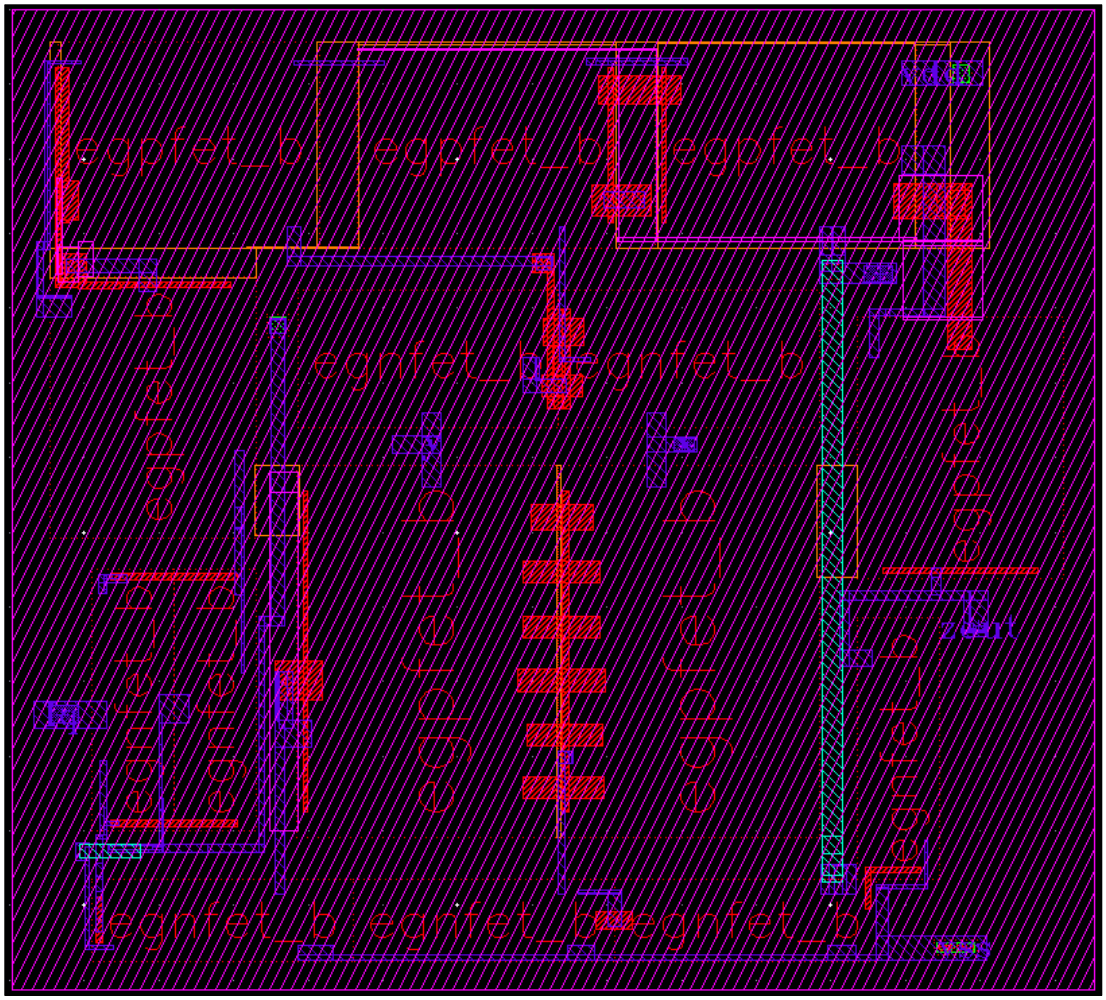

Figure 6.1 : Layout of the tranlinear CCCII(1).

From the given layout Figures 6.1 and 6.2 of the design, it is clear to demonstrate that the metal 2 layer is the upper layer in this circuit. Most of the connections and nets realized with metal 1 layer in the layout. Total area of the designed circuit is 13.12µm x 14.50µm.

6.1.1 Post-Layout simulations

After extraction of the translinear CCCII circuit, to test the realized structure behavior, post-layout simulations executed with the aid of Spectre tool. In these verification test runs calibre views of the extracted layouts are used.

The translinear CCCII circuit is biased with ±90V bias voltages and 10µA bias current is used same as the schematic verification tests to compare the extraction results.

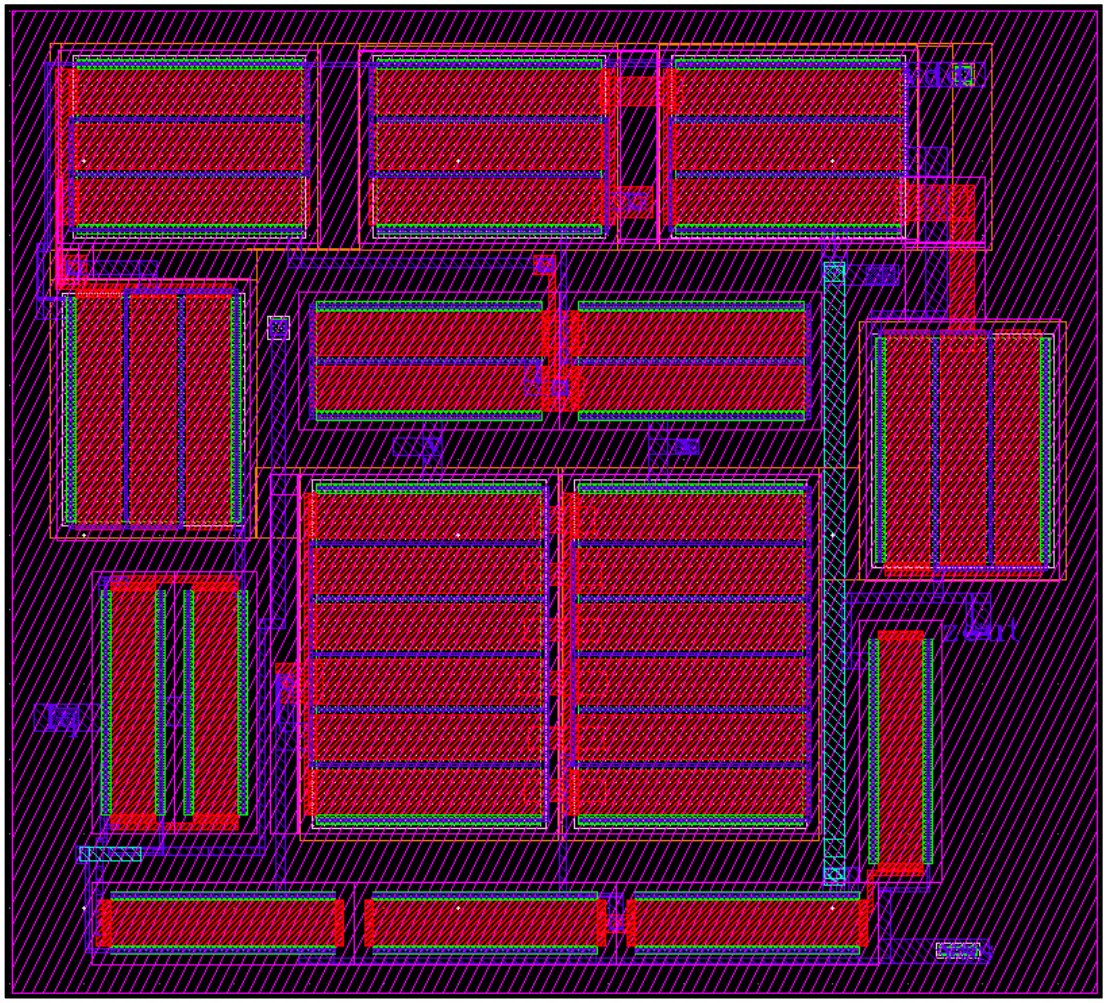

Figure 6.2 : Layout of the translinear CCCII(2).

The translinear CCCII circuit`s characteristic of Rx resistance related to the given bias current is shown in Figure 6.3. It`s frequency dependence is easy to obtain.

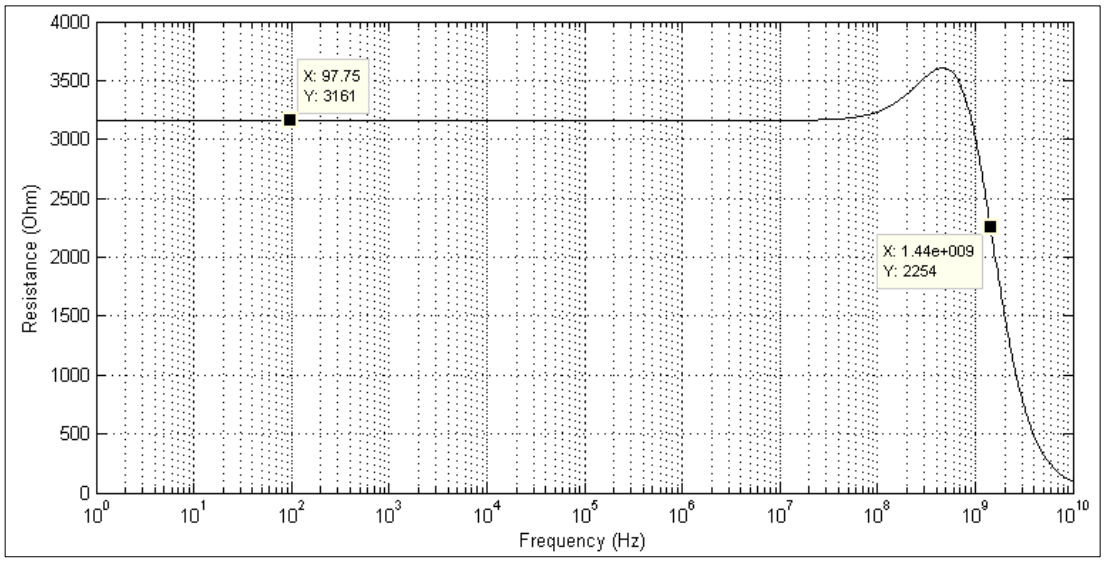

Figure 6.3 : R_x based on I_0=10µA.

It`s clear from the given figure and the behavior obtained by schematic verification that resistance value drop from 3.222kΩ to 3.161kΩ which is negligible and the frequency range increased 70MHz.

Figure 6.4 demonstrates the voltage transfer characteristics of the translinear CCCII structure. Moreover, the V-I characteristic of the input voltage versus the input current at port X is given in the same figure. When compared with the pre-layout version, voltage follow range decreased and current relationship is very slightly affected.

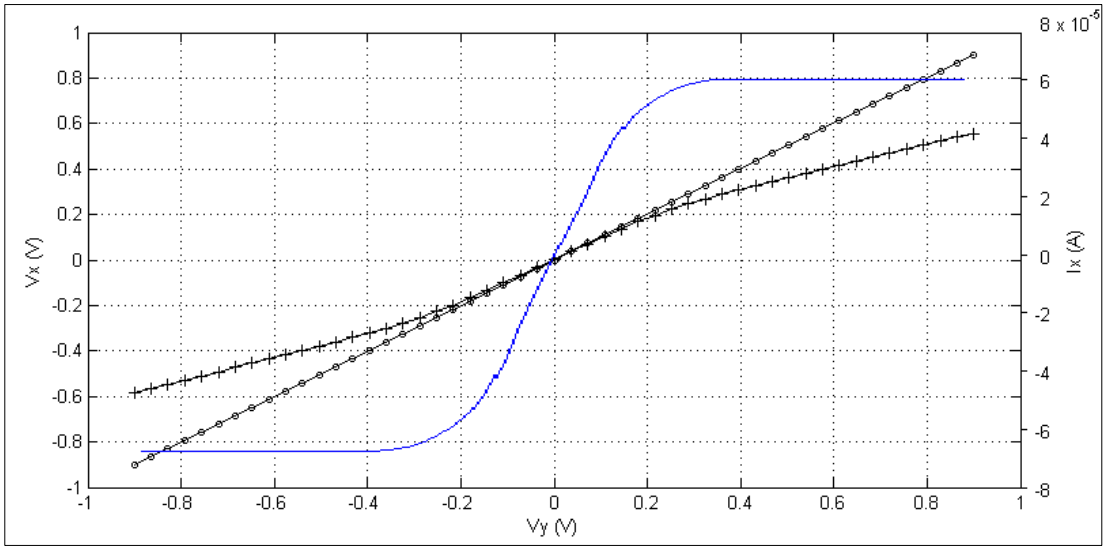

Figure 6.4 : The voltage transfer and current-voltage characteristics of translinear CCCII.

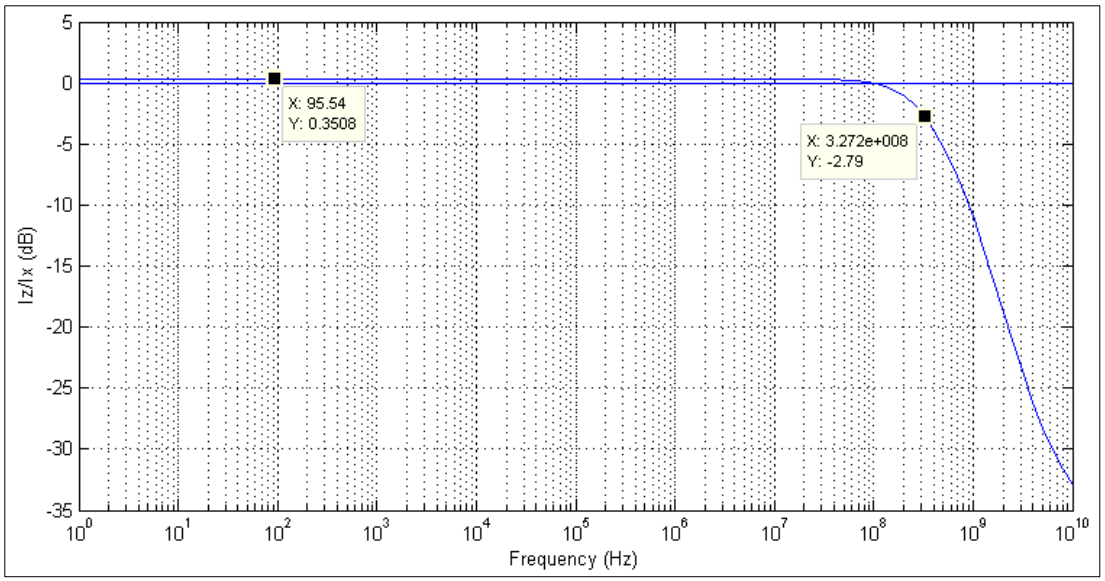

Figure 6.5 : The small-signal characteristic of the current transfer gain.

The small signal current transfer gain characteristic of the designed translinear CCCII circuit is plotted in Figure 6.5. The 3-dB bandwidth of current gain for 10µA bias current can be approximately read as 327MHz which is 50MHz lower than the schematic version.

Shortly, after checking the post layout behaviors of the translinear CCCII structure, it is still suitable for high frequency applications with the advantages of its high end process.

6.2 Layout of The Balanced Differential Pair Based CCCII

Layout of the balanced differential pair based CCCII structure is drew with respect to all mentioned items in previous section. The transistors used in this design are bulk CMOS process transistors with low threshold properties. Although, various transistor types are provided with the design kit with super low threshold voltage values, they are not realizable and not allowed to be used for production. These transistors are collected under the name of GO1 by the provider STMicroelectronics.

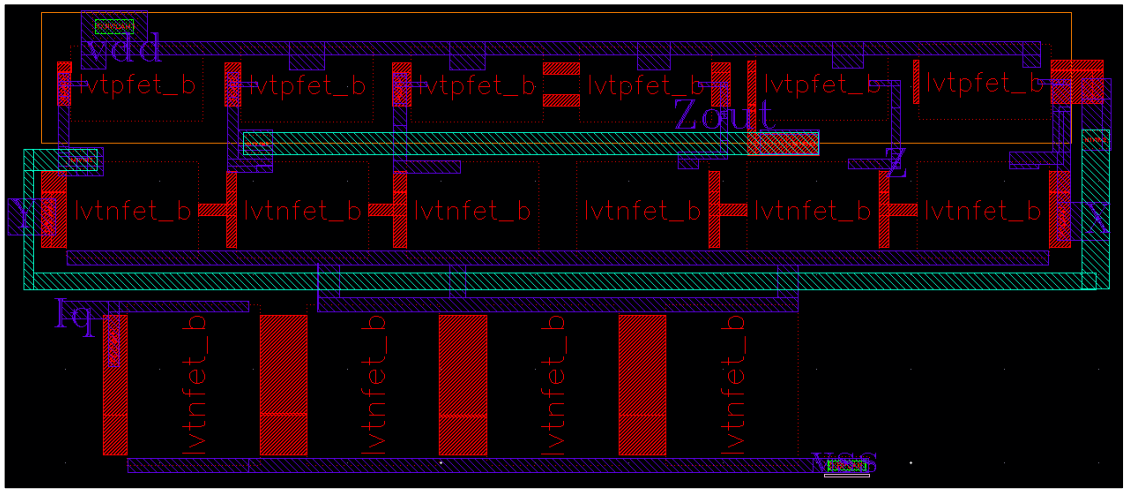

Figure 6.6 : Layout of the balanced differential pair based CCCII(1).

Different snapshots for the layout of the design given with Figures 6.6 and 6.7. From the given layout figures of the design, it is clear to state that the metal 2 layer is again the upper layer in this circuit.

It is visible from the given figures that metal layer 2 is the upper layer used in this design. Since the design kit library provides eight more metal layers, it enables the design of complex circuits. Total area of the designed circuit is 4.9µm x 11.75 µm, which is very small in dimensions.

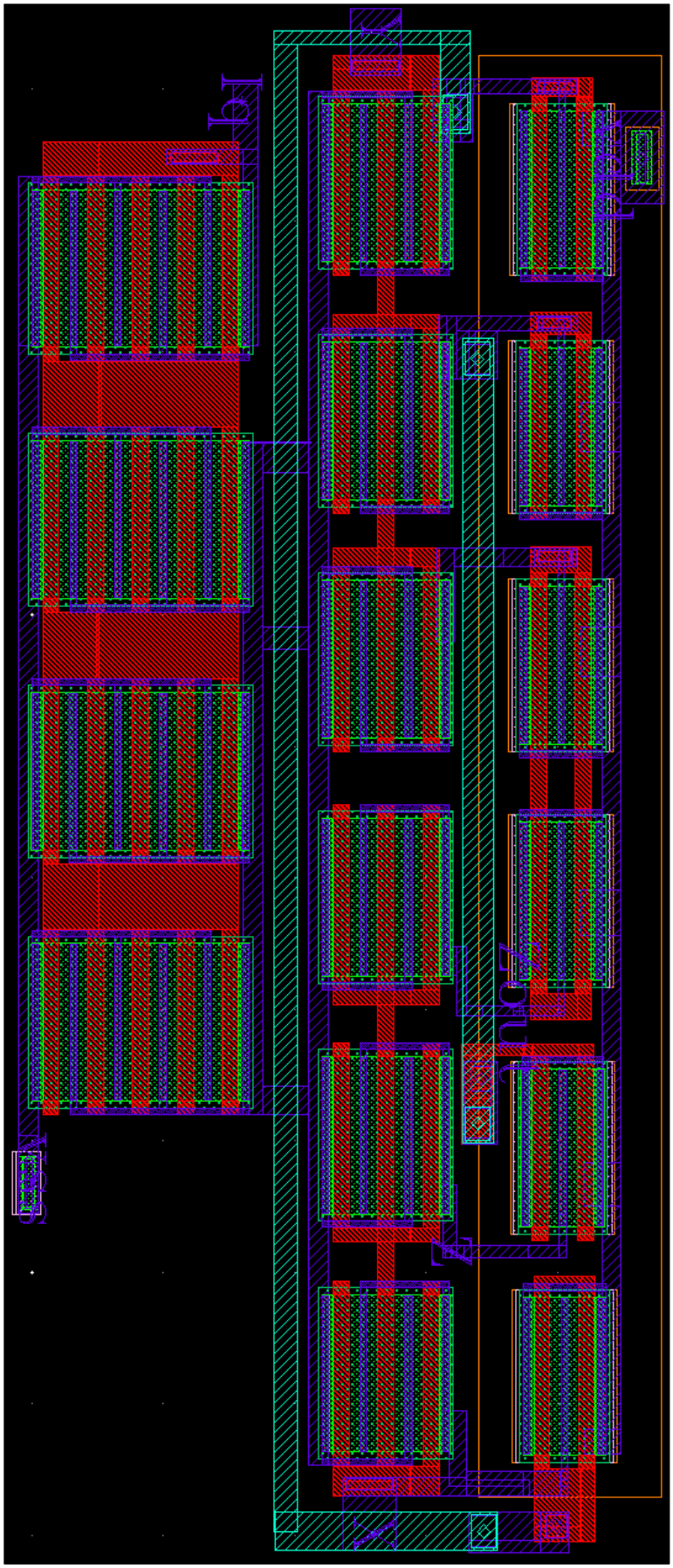

Figure 6.7 : Layout of the balanced differential pair based CCCII(2).

6.2.1 Post-Layout simulations

Following the extraction of the balanced differential pair based CCCII circuit, to test the realized structure behavior, post-layout simulations executed with the aid of Spectre tool. In these verification test runs Calibre views of the extracted layouts are used.

The balanced differential pair based CCCII circuit is biased with ±50V bias voltages and 10µA bias current is used same as the schematic verification tests to compare the extraction results.

The characteristic of R_x relating to 10µA bias current is presented in Figure 6.8. Observing the figure, the resistance value decreases very little and frequency range decreases 30MHz when compared with the pre layout simulations.

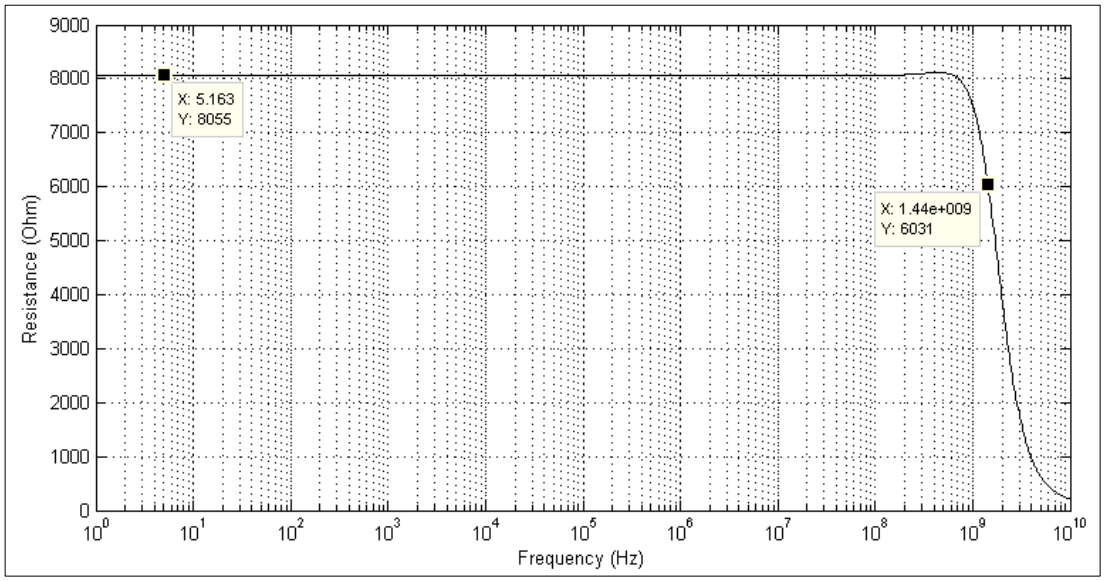

Figure 6.8 : R_x based on I_0=10µA.

In Figure 6.9, the voltage transfer characteristics are plotted. The figure again shows an efficient voltage following performance of ports X and Y. In addition to this, the voltage current characteristic of the input voltage versus input current at port X is revealed in the same figure as previously.

The given behavior in Figure 6.9 is again efficient and very little effected after the layout extraction steps. This behavior also proves that the layout steps for the designed structure are executed well and effectively.

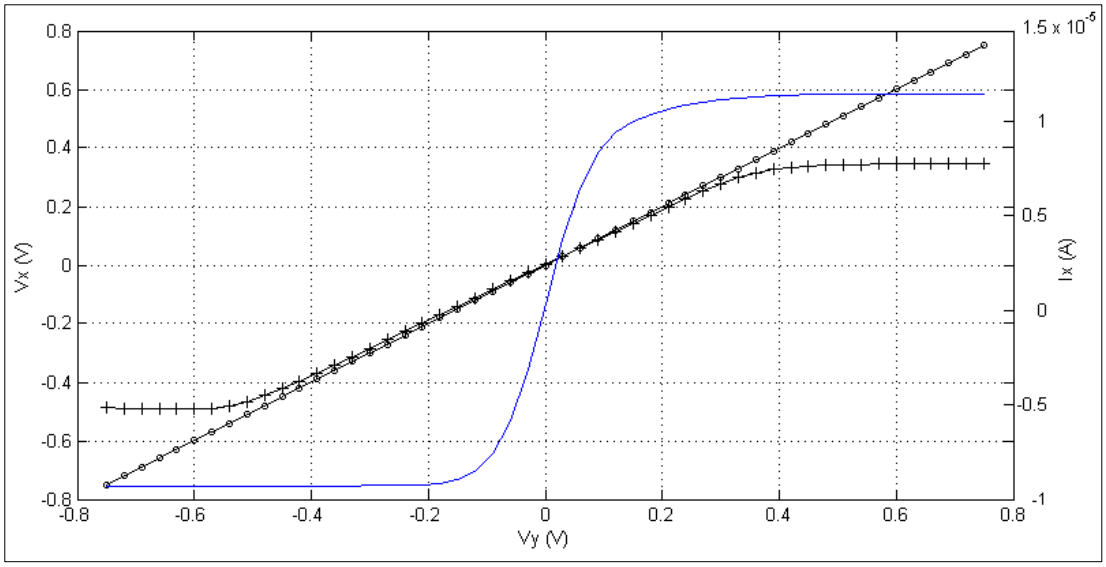

Figure 6.9 : The voltage transfer and voltage-current characteristics of CCCII.

At corresponding bias current, as stated before, the frequency characteristic of the designed circuit operation can be assumed to be dominated by the terminal resistance bandwidth. This can be called as open loop bandwidth of the circuit.

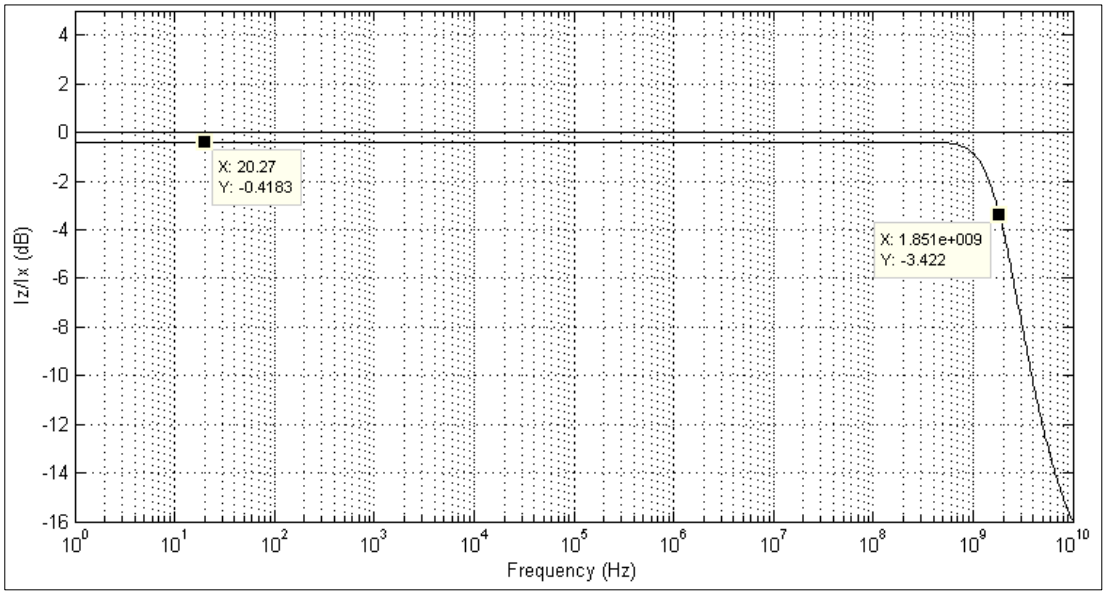

Figure 6.10 : The small-signal characteristic of the current transfer gain.

The small-signal characteristic of the current transfer gain of the designed CCCII is plotted in Figure 6.10. The 3-dB bandwidth of current gain for 10µA bias current can be approximately read as 1.85GHz which is very close to pre-layout version. Gain value decreases very little when compared to previous simulation. This post-layout simulation also shows that the layout steps for the designed structure is held carefully and effectively.

To sum up, after observing all characteristics same as the pre-layout version of the simulations, it is very clear that the extracted version is suitable for the application in high frequency ranges.

7. CONCLUSIONS AND RECOMMENDATIONS

In this thesis two design examples of current controlled current conveyors and their applications in 28nm STMicroelectronics design kit were presented.

The idea of providing fully active, configurable alternative solutions to current complex communication standards was the main goal of this project. In parallel to increasing complexity of communication standards and related circuit design creates the need for compact solutions. To overcome this problem, wiser and easy adapting environments and circuits need to be provided.

In this study, the investigation started with defining the common needs of encrypted and cognitive communication standards. Following to this, available solutions and possible implementations were checked for feasibility of the work to be done. Later on, two example CCCII structures were investigated with their theoretical expressions and their design implementations done in 28nm design kit. The design simulations held with the Cadence environment and behaviors of the designed circuits tested with respect to theory. Corner simulations were also checked to see circuit behaviors under different environment variables which were defined by the industrial standards. Observed behaviors emphasize that the designed CCCII structures were effective candidates to our application cases.

In the application phase, a frequency agile configurable filter application was realized for the balanced differential pair based CCCII circuit and a universal filter implementation was designed for the translinear CCCII structure. The designed filter behaviors were also checked with simulations and the matching between theory and implementation was exercised.

Layout realization and extraction was the last step of making our idea to real CMOS implementation. Layout drawing and extractions done with respect to design kit standards for GO1 and GO2 processes and the extracted netlists were created for post-layout simulations.

In the last part of the study, extracted netlists for both current controlled current conveyors were tested with post-layout simulations and behaviors were investigated for both schematic implementation and our constraints for the design at the beginning.

All in all, the design of the circuits, simulations and layout, post-layout steps were done in line with the industrial standards. All obtained data and results provide that the design of both CCCII circuits and their applications provide great performance in 28nm process and this show that the designs done in this thesis are high end alternatives to currently used structures. Our frequency agile filter application is a great alternative to industrially in use multi standard, complex GPS filters. The designed universal filter is also an effective candidate for wide application areas.

7.1 Future Work

One possible subject for the future work is to optimize the circuits and applications with respect to design specifications currently used in available products since every product has its own behavioral implementations.

Another possible subject is to implement all these work in FDSOI process since its getting an increasing attention for the future of industry. This kind of implementation will bring the advantages of FDSOI over bulk process such as power consumption and etc.

The implemented circuits and topologies can also be improved for specific cases and application areas.

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- Berna A., **Armagan E.,** Aygin S., Topcu S., and Arun S., An IP-XACT Deployment Case: IZARN IP. *IP-SOC 2010,* November 30, 2010 Grenoble, France.
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- **Armagan E.,** and Kuntman H., Design of Balanced Differential Pair Based CCCII Circuit and Configurable Frequency Agile Filter Application in 28nm Process. *ELECO 2012,* November 30, 2012 Bursa, Turkey.
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