İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

DESIGN OF A 2.4 GHz LOW POWER LC VCO IN UMC 0.18u TECHNOLOGY

M.Sc. Thesis by

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Programme: **Electronics Engineering**

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2.4 GHz DÜŞÜK GÜÇLÜ LC VCO TASARIMI

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CONTENTS

ABBREVIATIONS

RF	: Radio Frequency
IC	: Integrated Circuit
LO	: Local Oscillator
VCO	: Voltage Controlled Oscillator
MOS	: Metal Oxide Semiconductor
NMOS	: N- Type Metal Oxide Semiconductor
CMOS	: Complementary Metal Oxide Semiconductor
PMOS	: P-Type Metal Oxide Semiconductor
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
AM	: Amplitude Modulation
PM	: Phase Modulation
FM	: Frequency Modulation
AC	: Alternative Current
DC	: Direct Current
IMOS	: Inversion Mode Metal Oxide Semiconductor
AMOS	: Accumulation Mode Metal Oxide Semiconductor
PVT	: Process Voltage Temperature
LTV	: Linear Time Variant
LTI	: Linear Time Invariant
PA	: Power Amplifier
PLL	: Phase Locked Loop
Q	: Quality Factor
ISF	: Impulse Sensitivity Function
CAD	: Computer Aided Design
PSS	: Periodic Steady State
SCA	: Switched Capacitor Array

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LIST OF SYMBOLS

t	**:** Time
f	**:** Frequency
π	**:** Pi constant
Ω	**:** Ohm
γ	**:** Thermal Noise Coefficient
F	**:** Phase Noise Fitting Parameter
G_m	**:** Large Signal Transistor Transconductance
g_m	**:** Small Signal Transistor Transconductance
W	**:** Width
L	**:** Length
V_{dd}	**:** Supply Voltage
Q	**:** Quality Factor
g_l	**:** Conductance Loss

2.4 GHz DÜŞÜK GÜÇLÜ LC VCO TASARIMI

ÖZET

Bu tez çalışmasında, Bluetooth standardında çalışabilen çeşitli gerilim kontrollü LC osilatör devreleri UMC 0.18u prosesinde tasarlanmıştır. Bluetooth uygulamalarının düşük güç gereksinimi göze alınarak çalışmanın ikinci hedefi düşük güçlü devre çözümleri olarak belirlenmiştir. İlaveten, PLL'e tam uygunluk sağlanması amacıyla dışarıdan devreye bağlanacak olan gerilim değerlerinin toprakta ya da besleme gerilimine eşit olması sağlanmıştır.

Çalışmada ilk olarak temel osilasyon teorisi anlatılmıştır. Sağlanan bu altyapının üzerine entegre osilatörler anlatılmış, özellikle RF entegre osilatörleri olarak sıkça kullanılan negatif Gm ve Colpitts osilatör yapılarının detaylı analizleri yapılmıştır. Bunun yanı sıra birbirlerine olan üstünlükleri ve eksiklikleri de belirtilmiştir.

İkinci olarak, GKO faz gürültüsü ele alınmıştır. Faz gürültüsü ve alıcı-vericiler üzerindeki etkileri üzerinde kısaca durulmuş ve bundan sonra iki faz gürültüsü modelinin çıkarımı, altında yatan temel prensiplerle birlikte adım adım anlatılmıştır. Bu faz gürültüsü ifadeleri üzerine yorumlar yapılarak tasarım kısmında gürültünün kaynakları hakkında temel bir bakış açısı edinilmesi amaçlanmıştır. Bölümün son kısmında çapraz bağlı bir LC GKO devresindeki her elemanın sebep olduğu faz gürültüsü analiz edilmiştir. 'Pasif ya da aktif elemanların gürültüleri nasıl faz gürültüsüne dönüşür?' ya da 'Hangi mekanizmalar faz gürültüsüne sebep olur?' gibi soruların cevapları her faktörün sebep olduğu faz gürültüsünün nasıl düşürülebileceği anlatılarak verilmiştir.

Üçüncü olarak, entegre devrelerde kullanılan varaktör ve endüktans çeşitleri anlatılmıştır. Endüktansın fiziksel modelinde bulunan elemanlar kısaca açıklanmış ve darbant modelinin dönüşüm ifadeleri verilmiştir. Bu eşitlikler sayesinde endüktansın kalite faktörü veya iletkenlik kaybı gibi önemli parametrelerinin yazılan Matlab koduyla elde edilmesi sağlanmıştır.

Tasarım kısmında başlangıç noktası olarak 3 temel çapraz bağlı osilatör yapısının faz gürültüsü performansları düşük güç tüketimi göz önüne alınarak karşılaştırılmıştır. Bundan sonra en uygun osilatör seçilmiş ve yüksek *figure of merit* sağlaması amacıyla optimize edilmiştir. Optimizasyonda amaç faz gürültüsü mekanizmalarının etkisini azaltmaktır. Bu sebeple, varaktör yapısı üzerindeki AM-PM dönüşümünün en aza indirilmesi amacıyla frekans ayarlamasının kaba ve ince ayar olmak üzere ikili olması kararlaştırılmıştır. Kaba ayar devresi 4 bitlik sayısal kontrollü varaktör yapısı olarak tasarlanmıştır. Devrenin fizibilitesini göz önünde bulundurarak kontrol bitlerine uygulanacak gerilim değerlerinin toprakta olması ya da beslemeye bağlanması farz edilmiştir. Bunu sağlamak amacıyla çeşitli tranzistörler denenmiş ve sadece düşük eşik gerilimli PMOS tranzistörün uygulanabileceği görülmüştür. İnce ayar devresi olarak kapasite bağlı diyot varaktör devresi seçilmiş ve rezonatörü yüklemeyecek şekilde tasarlanmıştır. Aynı şekilde diyotun maksimum kontrol

gerilimi de besleme gerilimine eşit tutulmuştur. Sonuç olarak verilen faz gürültüsü sınır değerlerinin en kötü durumda bile 5dBc/Hz aşağısında değerler elde edilmiştir. Bu devreye ilaveten daha düşük gerilimlerde çalışabilen yine çapraz bağlı topolojisine dayanan çeşitli GKO'ların tasarımı yapılmıştır. Çok düşük gerilim değerlerinde IMOS varaktörün sayısal kontrolu imkansız olduğundan 4 bitlik farksal anahtarlamalı kapasite dizisi tasarlanmıştır. Simulasyonlar neticesinde birçok devrenin Bluetooth standardını filtre görevi üstlenen bir endüktans ile sağladığı görülmüştür. Sonuç olarak düşük gerilimli çözümler istenilen faz gürültüsü değerlerini geniş bir alan kaybıyla ödeyerek kazanmıştır. Tasarım bölümünün son kısmında üç değişik farksal Colpitts devrelerinin akım değerleri diğerler devrelerle aynı tutularak tasarlanmasına çalışılmıştır fakat sadece Gm yükseltilmiş Colpitts devresinin salınıma başlatılabildiği gözlemlenmiştir. Bu devrenim faz gürültüsü performansının tasarlanan ilk çapraz bağlı devreden daha düşük olduğu görülmüştür.

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DESIGN OF A 2.4 GHZ LOW POWER LC VCO IN UMC 0.18u TECHNOLOGY

SUMMARY

In this work, several LC oscillators were designed to meet the specifications of Bluetooth standard in UMC 0.18u technology. Taking into account that low power consumption is demanded for Bluetooth applications, another target of the work was decided to focus on low power circuit implementations. Also, to provide a full integration to a PLL, the external voltages applied to the oscillator were kept below or equal to supply voltage as much as possible.

Firstly, basic oscillation theory including the feedback system approach and two single-port view was explained. After attaining fundamental knowledge on oscillators, three IC oscillator types; the ring, the negative Gm and the Colpitts oscillator were described. Since mostly preferred RF IC VCOs are the cross-coupled and the Colpitts oscillators, they were analyzed in details and their superiorities and drawbacks were given.

Secondly, the specification that makes the oscillator design crucial, the oscillator phase noise, was focused on. After a brief definition of the phase noise and its effect on RF transceivers, the expressions of two phase noise models were obtained via a step by step transformation methodology, also, by explaining the underlying approaches; LTV and LTI. The phase noise expressions were commented to provide practical conclusions so that the phase noise sources in the designed oscillators could be understood. This topic ended with a very detailed and useful analysis of the phase noise sources in a cross-coupled LC VCO. The questions such as "how the noise of the active and passive devices is translated to phase noise?" and "which mechanisms cause the phase noise?" were answered through giving the techniques to reduce the phase noise produced by each factor.

Thirdly, the varactor and the inductor types employed in IC process were discussed. The elements in the physical model of the inductor were described briefly and its narrowband model conversion equations were expressed. With the aid of these equations, the physical model of the inductor in UMC 0.18um design kit was converted via a Matlab code in order to obtain the important parameters such as the conductance loss and the quality factor.

As a starting point to the design section, three basic cross-coupled LC oscillators were compared due to low power consumption. After choosing the most suitable topology, the oscillator was optimized by minimizing the effect of the phase noise generating mechanisms to achieve a high figure of merit circuit. For this reason, the AM-PM conversion, which degrades the phase noise at least 10dBc/Hz when only an IMOS varactor is employed, was reduced by recognizing the frequency tuning in two ways; the fine and the coarse tuning. In the coarse tuning circuitry, a 4 bits digitally controlled varactor structure was designed. Considering the feasibility of the circuit, the voltage values applied to control bits were assumed to be ground and supply

voltage for on or off state of varactors. To accomplish that, low-V_{th} PMOS transistor was selected after examining the possibility of several MOS transistors. In fine tuning circuitry, a capacitor coupled diode varactor topology was properly implemented without degrading the quality factor of the tank and again the maximum value was kept equal to supply voltage for high integration. As a result, the phase noise requirement was attained with a 5dBc/Hz phase noise margin for the worst case. In addition to the oscillator described above, several LC voltage controlled oscillators based on cross-coupled topology were designed in order to lower the power consumption as well as to satisfy the phase noise specification. To make a fair comparison, in most cases, their bias current was kept the same. It was not possible to digitally control an IMOS varactor in an ultra low voltage range (from ground to <1V), therefore the digital control topology was replaced with a 4 bits binary weighted differential SCA array to be able to apply the supply voltage as the digital control voltage. After the phase noise simulations, most of the circuits met the phase noise requirement of the Bluetooth standard with the use of a filtering inductor. In the last part of the design section, three differential Colpitts structure were targeted to design with respect to the same current, but only Gm boosted Colpitts topology achieved to start-up the oscillation. However, this topology had a worse phase noise performance compared to the first oscillator design.

1. INTRODUCTION

1.1 Motivation behind the Work

As the time passes, people are taking a closer interest on the technological developments in communication systems. They demand more and different features at a reasonable cost. For instance, while purchasing a cell phone, they seek for not only a good camera resolution, high purity mp3 sound and a variety of menu options, but also a stylish design -mostly slim and compact design- and a long lasting battery. This increasing pressure for lower power, higher integration and lower cost in the mobile communication market drives the industry to on-chip solutions and CMOS technology. Among different fabrication technologies such as GaAs and SiGe, CMOS provides high integration levels, mixed analog/digital compatibility, capability for low voltage operation, mature fabrication technology, successful scaling characteristics, and the combination of complementary MOSFETs yielding low power CMOS circuits. For these reasons, in a transceiver the baseband blocks such as high speed ADC/DAC, DSPs and memories are mostly manufactured in CMOS technology and this constrains RF blocks to be also implemented in the same technology. However, the integration between them is an important issue because RF blocks generally need external passive components such as front-end SAW filters to accomplish their mission which is to carry the desired signal from the antenna to the baseband blocks with a minimum loss in the receiver path and to generate high purity signals with high efficiency in the transmitting path. Bringing the signal off-chip and then on-chip again complicates the transceiver design because proper matching at the output and input terminals is required. This also increases the power consumption of the transceiver because it takes more power to drive an off-chip load than to keep the signal completely on the same integrated circuit. Generally, taking the signal off and then on-chip results in signal power loss accompanied by an undesirable increase in noise figure. Taking these drawbacks into account, a fully integrated RF front-end and surely an RF transceiver is desirable despite the fact that passive IC devices have poorer quality factor than their discrete counterparts.

Indirect frequency synthesis techniques based on a phase-locked-loop (PLL) are preferred to generate programmable carriers and RF frequencies that many communications applications require. In a PLL structure as depicted in Fig. 1.1, a less accurate RF oscillator whose frequency can be controlled with a control signal is embedded in a feedback loop and its output frequency is locked to an accurate low frequency reference. In general, this control signal is a DC voltage and so the RF oscillator is called a voltage controlled oscillator (VCO). Hence, a VCO generates the local oscillator (LO) signal to upconvert the input baseband signal and to downconvert the RF signal. In addition to the frequency translation duty, they are also used in clock recovery circuits. Despite being researched continually, it is still a bottleneck and one of the most critical and challenging parts of a transceiver due to some severe parameters that will be explained below.

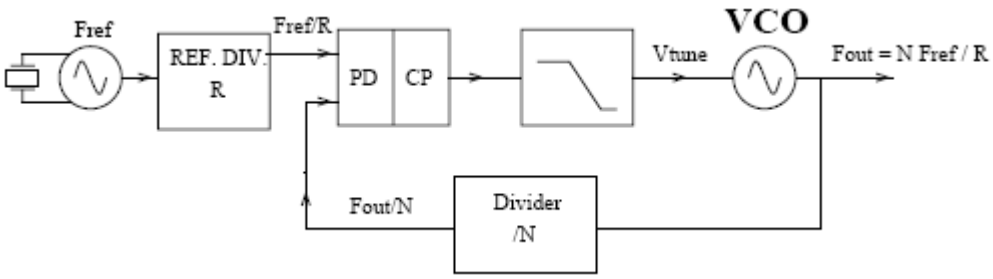


Figure 1.1: A phase locked loop with a voltage controlled oscillator (VCO), frequency divider, phase detector (PD), charge pump (CP) and lead-lag loop filter; the VCO's output frequency Fout is set to a multiple of the reference oscillators frequency Fref depending on the divider ratios (N & R).

1.2 VCO Spec-sheet

In each VCO design, several requirements must be fulfilled regarding the application of interest such as GSM, ZigBee or other communication protocols. These specifications are composed of the following entries:

Center Frequency: is the oscillation frequency of the VCO where the control voltage takes its center value. It is denoted in [Hz] and its angular frequency equivalent is in [rad/s]. The application determines its value.

Tuning Range: is the interval of output frequencies where the VCO operates over the whole range of the control voltage. Due to process variations, the tuning range provided by the application is generally increased by %20.

Tuning Sensitivity: is the variation in output frequency per unit change in the control voltage, typically expressed in [Hz/V]. VCOs usually have a nonlinear relationship between the control voltage and the oscillation frequency so that several values are quoted or min/max boundaries are given.

Power Consumption: specifies the DC power used up by the oscillator. In some applications, power dissipation has a vital importance among all specifications.

Spectral Purity: can be specified depending on the application, in the time domain in terms of jitter or in the frequency domain in terms of phase noise or carrier/noise ratio. The factors affecting the purity of the LO output waveforms will be discussed in chapter 3.

Load Pulling: quantifies the sensitivity of the output frequency to changes in its output load. In some applications the output load of the VCO is switched while the VCO must remain at the same frequency to avoid frequency errors.

Supply Pulling: defines the sensitivity of the output frequency to changes in the power supply voltage and is expressed in [Hz/V]. The power up or down of other circuits in a transceiver can generate abrupt changes in the power supply voltage so the VCO frequency can shift up or down.

Output Power: is the power delivered to a specified load by the VCO. A low change in output power with respect to different control voltage values is desirable.

Harmonic suppression: specifies the ratio of the harmonics of the output signal to the fundamental wave voltage in [dBc].

Among these specifications, low phase noise, low power dissipation and large tuning requirements are usually the dominant terms and the trade-off between them makes the VCO design challenging.

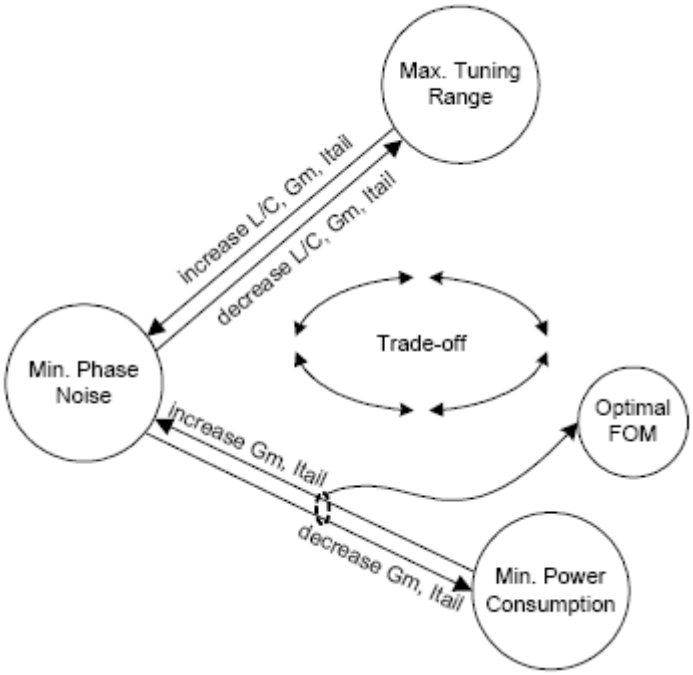


Figure 1.2: Trade-off between crucial VCO specifications [1]

1.3 The Design Specifications of the Proposed VCO

In this project, a VCO is intended for Bluetooth application. Bluetooth is a wireless communication technology using short-range radio links to connect portable and/or fixed electronic devices. Its key features are robustness, low complexity, low power and low cost. Designed to operate in noisy frequency environments, the Bluetooth radio uses a fast acknowledgement and frequency hopping scheme to make the link robust. Bluetooth radio modules operate in the unlicensed industrial, scientific and medical (ISM) band at 2.4GHz to 2.485GHz and the signal hops among 79 frequencies at 1MHz intervals to a new frequency after transmitting or receiving a packet. The ISM band is available and unlicensed in most countries.

Table 1.1: Phase noise specification values for Bluetooth

Offset	50kHz	3MHz	Noise floor
Max. phase noise [dBc/Hz]	-84	-123	-145

The phase noise specification is provided by Nokia as depicted in Table 1.1. Since it is not stringent, the VCO is proposed to consume as low power as possible. Taking process variations into account, the targeted frequency range is between 2.2GHz and 2.7GHz with a center frequency of 2.45GHz.

2. OSCILLATOR BASICS

In this chapter, basic oscillation theory including the feedback system approach and two single-port view is explained. Three IC oscillator types; the ring, the negative Gm and the Colpitts oscillator are described. Since mostly preferred RF IC VCOs are the cross-coupled and the Colpitts oscillators, they are analyzed in details and their superiorities and drawbacks are given.

2.1 Oscillator as a Feedback System

An oscillator can be modeled as a feedback circuit. The overall transfer function of the feedback network depicted in Fig. 2.1 is expressed as

$$G(jw) = \frac{Y(jw)}{H(jw)} = \frac{H(jw)}{1 - H(jw)} \quad \textbf{(2.1)}$$

At a frequency of ω_o, if $H(j\omega_o)=1$ where the closed loop gain goes to infinity, the system causes its own noise to grow and generates a periodic signal. The oscillation reaches its steady state when $H(j\omega_o)$ is purely imaginary [2]. In practice, the small-signal loop gain must have a value of at least two to guarantee the oscillation start up because this value is reduced and equals to one as the amplitude increases due to the nonlinearity of the active device. Therefore, two conditions must be met for steady oscillations at ω_o:

$$|H(j\omega_o) = 1| \quad \textbf{(2.2a)}$$

$$arg(H(j\omega_o)) = 0° \quad \textbf{(2.2b)}$$

The latter expression can be modified to a value of 180° for a negative feedback system. These expressions are called Barkhausen's criteria. However, for some cases Barkhausen's criteria is necessary but not sufficient. For instance, if the phase shift at dc level is zero, even though the loop gain is enough to start oscillation, the output voltage goes to supply voltage or zero rather than oscillate. A cascade amplifier

which contains two single common-source stage transistors with a feedback from the drain of the second transistor to the gate of the first one is a good example of this case. The output latches because overall phase shift is also 360° at zero frequency.

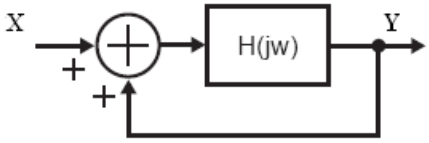


Figure 2.1: Feedback model of an oscillator

Today, there are many topologies used to realize oscillation feedback systems answering the two conditions mentioned above. In general, ring oscillators and LC oscillators are commonly preferred in RF IC oscillator design.

2.2 Ring Oscillators

Ring oscillators comprise N amplifiers with an odd number of inversions connected in a feedback loop. Each amplifier stage acts as an inverter and total delay of each inverter cell determines the large-signal oscillation frequency below:

$$f_o = \frac{1}{2\,N\,t_d} \qquad \textbf{(2.3)}$$

The number of stages (N) is mainly chosen due to the power dissipation and the phase-noise performance. There are two main topologies for the ring-oscillator: the differential and the single-ended one (Fig. 2.2).

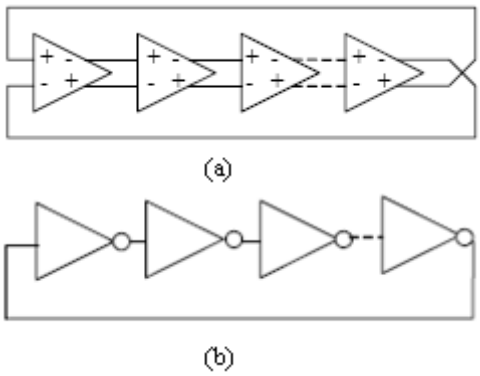


Figure 2.2: Ring oscillator implementation; (a) differential topology, (b) single-ended topology

In single-ended topology Barkhausen criteria is always fulfilled since the inverter cells have high small-signal gain. The single-ended topology has to be implemented

with an odd number of cells because each delay cell has a large-signal phase shift of 180°. The current is only consumed during transitions of the inverters. This constant current generated by the transistor when “on” charges and discharges the intrinsic capacitances of transistors; therefore, it defines the delay time of each cell, so the higher current leads to a faster transition and higher oscillation frequency. It is possible to control the frequency with voltage sources by adding two transistors as shown in Fig. 2.3. This type of delay cell is called current-starved inverter.

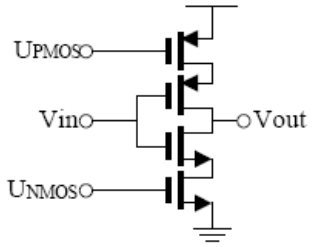


Figure 2.3: Current starved inverter

The differential topology is composed of a load and an NMOS differential pair (Fig 2.4). The delay in the cell is set by the charge in each node and the current through the load. As load devices, resistors can be used for fixed frequency or PMOS transistors can be employed to make the oscillator tunable with external voltages. PMOS load can be implemented as symmetric or cross-coupled.

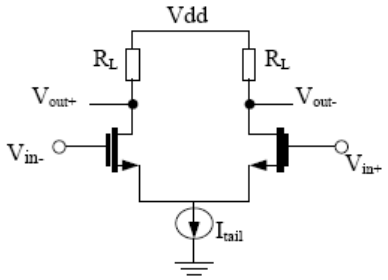


Figure 2.4: Differential cell with symmetric load

The differential ring oscillator has $N(1+V_{char}/(R_L*I_{tail}))$ times higher phase-noise level than the single-ended ring oscillator with equal power dissipation, frequency and number of stages [3]. The single-ended topology dissipates less power than the differential topology and therefore has a better phase noise for a given power dissipation since phase noise is inversely proportional to power consumption. In digital circuits differential ring oscillators are often preferred because they have much better common noise rejection of substrate-coupled noise [3]. They also have

lower noise injection into other circuits on the same chip [3]. A quadratic signal can only be obtained by using differential topology since even number of cells can be implemented.

Non-use of passive devices in ring oscillators is both advantageous and disadvantageous. The only usage of active devices makes ring oscillator easy to integrate. Furthermore, an inductor occupies a substantial amount of area in an IC oscillator. Its absence will result in less chip area. On the other hand, an inductor with a capacitor forms a band pass filter that causes the phase noise to reduce in an oscillator. As a result, ring oscillators exhibit poor phase noise performance compared to LC oscillators. They are usually used as clock recovery for serial data communications and on chip clock distribution.

2.3 LC Oscillators

LC oscillators comprise a resonator tank. There are mainly two LC oscillator type: Negative Gm and Colpitts oscillator. In this section, these two types are analyzed and compared.

2.3.1 LC Tank

In VCO designs, LC network is widely used because of its filtering capability. The network, also called parallel resonator circuit, is composed of the parallel combination of an inductor and a capacitor. The loss of the network is compensated by an active device. The main contributors of loss in the tank are the series resistances of the passive devices. The parasitic resistances can be converted to their parallel equivalent since RF oscillators operate over a narrow band of frequencies (Fig. 2.5).

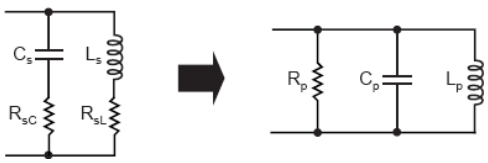


Figure 2.5: Conversion of the series resistances of an LC tank into a parallel resistance

Each term in the above figure can be expressed as

$$C_p \approx C_s \quad \textbf{(2.4)}$$

$$C_p \approx L_s \tag{2.5}$$

$$R_p = R_{pL} \,//\, R_{pC} \approx R_{sC} \,//\, Q_{sL}^2 R_{sL} \quad (Q_{sC} \gg 1 \,\&\, Q_{sL} \gg 1) \tag{2.6}$$

where Q_L *and* Q_C are the quality factors of the inductor and the capacitor respectively. The quality factor of the inductor is lower than that of the capacitor even if diode or MOS varactors are used so the dominant term for R_p is the former part of the Equation 2.6. Also, the filtering capability of the resonator is defined by the quality factor of the inductor. The overall quality factor of the resonator is expressed as below:

$$Q_{tank} = Q_L \,//\, Q_C \tag{2.7}$$

However, for some cases, the varactors with very poor quality factor which is close to that of the inductor can be obtained, that causes a drop in the quality factor of the tank.

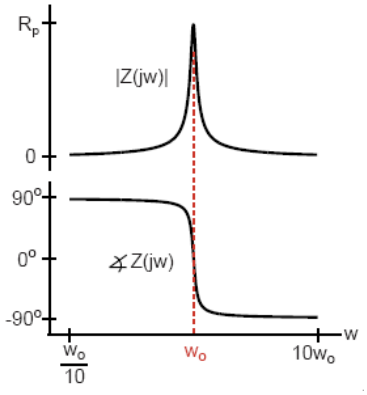


Figure 2.6: Magnitude and phase spectrum of an LC tank

The magnitude and phase characteristics of an LC parallel network are shown above. At resonance the network is purely real, in other words, behaves like a resistor. The resonant frequency is written as $\omega_o = 1/\sqrt{LC}$.

2.3.2 One-port View of an LC Oscillator

One-port view or sometimes called negative Gm approach handles the oscillator as the connection of two one-port networks (Fig. 2.7). It is especially convenient for intuitive analysis of LC oscillators.

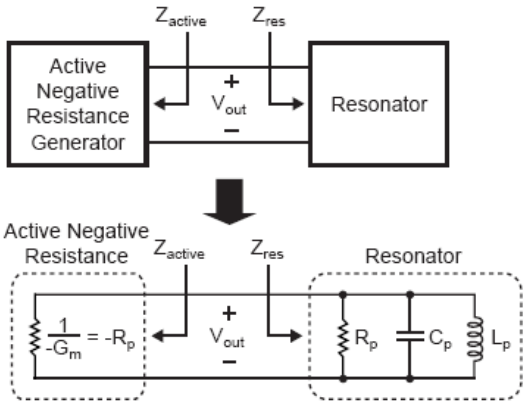


Figure 2.7: One-port view of an LC oscillator

Remembering from Fig. 2.5, the resonator circuit with the series resistive loss of each passive element can be converted to the parallel equivalent for narrow band applications. At each cycle the dissipation of some amount of stored tank's energy in R_p prevents stable oscillation. However, an active negative resistance generator that is equal to $-R_p$, compensates the loss of the tank, therefore, creates a lossless resonator whose parallel resistance is infinite at resonant frequency. In other words, the energy lost in R_p is regenerated by the active circuit in every cycle. That condition is met with the equation below:

$$\frac{1}{G_m} = R_p \tag{2.7}$$

Here, G_m is defined as the large signal transconductance of the active device when the oscillator is in steady-state.

2.3.3 Cross-Coupled LC Oscillator

From the point of the negative Gm approach, the loss in the tank must be compensated for steady-state oscillation. In a cross-coupled topology, the transistor pair behaves like an active negative resistance generator. To guarantee oscillation start-up, negative resistance is chosen at least two times more than the parallel loss. Two advantages of this topology are the simple design and the differential implementation. There are three sorts of this topology: NMOS, PMOS and CMOS cross-coupled. Each of these types can be designed with either a current source of top-biased, bottom-biased or self biasing.

2.3.3.1 NMOS Cross-Coupled LC Oscillator

Fig 2.8 depicts a bottom-biased NMOS cross-coupled LC oscillator including the losses in the tanks. It contains an NMOS differential pair and two equivalent tanks with series and parallel resistive losses, respectively.

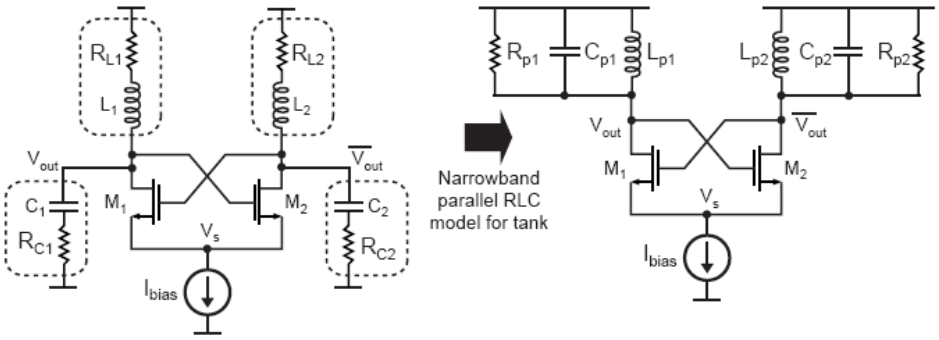


Figure 2.8: Bottom biased NMOS cross-coupled LC oscillator with series losses and parallel losses

For the simplicity of the analysis, the circuit is split into two equal parts and it is assumed that the common-mode node is AC grounded so that the source of the transistor V_s is biased to zero. In reality, this assumption is not definitely valid due to the finite output resistance of the current source. Differential implementation enables two output voltages to have the same output swing with a phase difference of 180° so the gate of the left side transistor can be expressed as $-V_{out}$, then the resistance seen from V_{out} to ground through this transistor is equal to $V_{out}/I_{d1}=V_{out}/-G_mV_{out}$, or simply $-1/G_{m1}$.

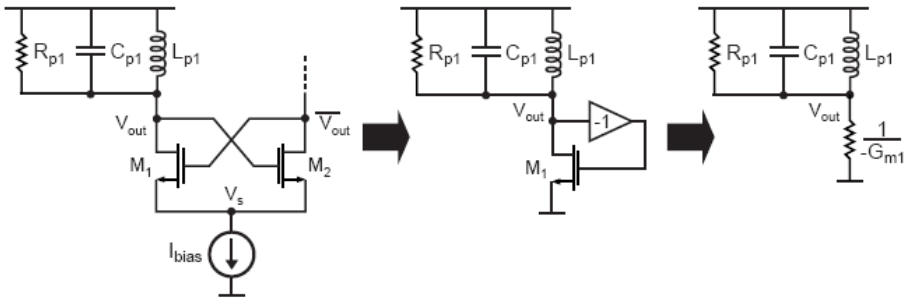


Figure 2.9: Analysis of an NMOS cross-coupled LC oscillator

Hence, if two tanks are equal, by merging them one can get the results; $L_p=2L_{p1}$, $C_p = C_{p1}/2$, $R_p =2R_{p1}$ and also negative resistances in parallel conclude to $-2/G_{m1}$. The equation 2.7 can be rewritten as

$$\frac{1}{G_{m1}} = R_{p1} \tag{2.8}$$

for an NMOS cross-coupled LC oscillator in steady state. The oscillator must have a greater small-signal loop gain of α than unity in order to grow its own noise and usually the minimum value of this gain α_{min} is chosen as at least two. Hence the start-up condition is met if

$$\frac{1}{g_{m1}} \geq \alpha_{min} R_{p1} \tag{2.9}$$

It is interesting to investigate the relationship between the large-signal gain G_{m1} and the small-signal gain g_{m1}. The small-signal gain which is α_{min} times greater than G_{m1} leads the circuit's own noise to grow. As the oscillation grows, the small signal gain of the transistor will degrade and stabilize at G_{m1} due to the nonlinearity of the active device. The nonlinear behavior can be understood by observing the transistor's operation in triode region and in cut-off. While the transistor enters cut-off region, the swing of the positive output wave under bias voltage is clipped. Secondly, the large signal transconductance of an NMOS transistor in linear region is equal to $\mu_n C_{ox}(W/L)V_{ds}$, , in other words, it is directly proportional to drain voltage. In the NMOS cross-coupled LC oscillator depicted in Fig. 2.9, since the gate and the drain voltages have a phase difference of π, an increment of ΔV at V_{g1} will bring on V_{d1} or V_{g2} to decrease by the same amount as a result of the nature of the differential oscillation. If ΔV is high enough, the transistor M_1 to enters into linear region corresponding to Vx in Fig 2.10. At this point g_{m1} starts to degrade because the instant voltage of the negative output waveform becomes one threshold voltage greater than that of positive output waveform where $2\Delta V \geq V_{th}$. When this output reaches to its maxima, the loop gain stabilizes at unity.

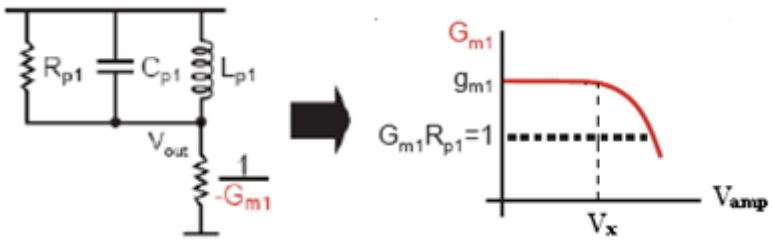


Figure 2.10: Output voltage saturation

Since the output waveforms are symmetric, each NMOS transistor conducts only in half cycle so the characteristic of current can be illustrated as a square wave for each one [4]. By the Fourier series expansion, all the frequency components of the current can be obtained as depicted in Fig. 2.11. At zero frequency or DC, the value of the current corresponds to the mean value of the square waveform in time domain. The current at the fundamental frequency (1/T) of the double-sided spectrum is expressed $(1/\pi)I_{bias}$. DC and other harmonics of the current is filtered by the LC tank so the amplitude of the output waveforms is expressed as

$$v_o = \frac{2}{\pi} I_{bias} R_p \tag{2.10}$$

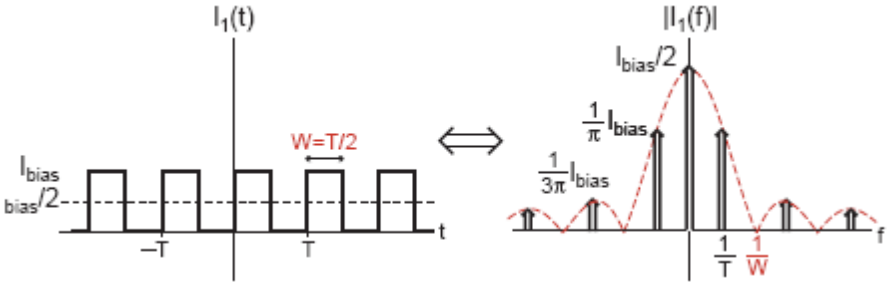


Figure 2.11: Current waveform of a switching transistor in NMOS cross-coupled LC oscillator in time and frequency domain

2.3.3.2 CMOS Cross-Coupled LC Oscillator

CMOS cross-coupled LC oscillator comprises a PMOS differential pair additional to NMOS-only structure. This type enables the implementation of only one inductance. In this case, the inductor is driven differentially resulting in a higher quality factor than a single ended one. For the symmetry of the outputs, the parallel resistance of the tank seen from both sides must have equal values. Otherwise, the phase noise of the circuit increases. To prevent this, if the inductor provided in the design is nonsymmetrical, two inductances in series must be chosen instead.

This topology provides twice higher output voltage since the current is reused in PMOS pair. During the rise of V_{out}, M_2 eventually enters into triode and M_1 goes to cut-off region and also PMOS transistors behave similarly, but conversely. M_4 conducts and M_2 goes off. Therefore, the current drawn from the bias transistors flows through M_3 then through the LC tank and lastly through the M_2 to the ground so in each half cycle, the current flows on both of two parallel loss resistances of the

tank. Hence, the output waveform is doubled compared to NMOS cross-coupled topology. According to Leeson's formula, this rise corresponds to an improvement on the phase noise at a maximum value of 6dBc/Hz.

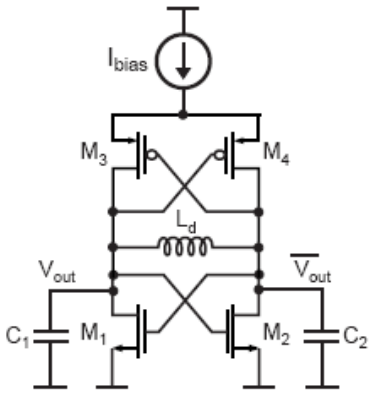


Figure 2.12: Top biased CMOS cross-coupled LC oscillator

The PMOS switching pair also generates a negative resistance of $2/Gm_3$ and this resistance is added to negative NMOS resistance in series. Therefore, in steady state, the CMOS structure attains a negative resistance of $(-2/G_{m1}-2/G_{m3})$. In order to generate symmetrical outputs, the transconductance of PMOS and NMOS transistors must be equal so the overall negative resistance equals to $-4/Gm_1$. Recalling the negative resistance value obtained or the NMOS cross-coupled topology the addition of PMOS pair relaxes the start-up condition by a factor of two for a given bias current.

Furthermore, the PMOS and NMOS transistors having equal transconductance result in a more symmetric waveform than in NMOS cross-coupled topology. This improvement on rise and fall time symmetry reduces the upconversion of the transistor's flicker noise to close-in frequencies [3]. Consequently, this topology achieves a better $1/f^3$ phase noise performance than an NMOS topology. According to [5], the phase noise in $1/f^2$ is also reduced in this topology although the PMOS pair also adds thermal noise which is the main source of the phase noise in this region. This behavior is attributed to a smaller noise coefficient γ because of a smaller DC voltage drop across the channels.

The main drawback of this topology is the output swing limitation. In an NMOS cross-coupled topology with an NMOS bias transistor, the output is biased at V_{dd} and taking the voltage headroom of the bias transistor into account, the maximum voltage swing at each output waveform is $(V_{dd}-V_{od})$. In a CMOS cross-coupled topology with

PMOS or NMOS bias transistor, the maximum output swing reduces to $(V_{dd}-V_{od})/2$. However, the output voltage biased at the supply voltage makes the oscillator very susceptible to the fluctuations at the supply voltage.

In CMOS topology, the addition of the PMOS transistor contributes a considerable parasitic capacitance added to the capacitor in the tank. Depending on the bias current, the ratio of PMOS to NMOS transistor dimensions may be as high as four times to equalize transconductance of the complementary transistors. Even though transconductance requirement is reduced in CMOS topology, the total intrinsic capacitance may constitute a significant part of the total capacitor of the tank. Therefore, the decline in the value of the tunable capacitor will constrain the tuning range of the oscillator.

2.3.4 Colpitts Oscillator

The Colpitts type is a good example of one transistor LC oscillator category. Recalling the two-port network model in Fig 3.1, one transistor whose drain is connected to an LC tank can be fed back to gate or source. Since the tank has no phase difference between its voltage and current at resonant frequency, the signal must return to the source of the transistor to accomplish a phase shift of zero in total. Hence, one transistor oscillator is realized. However, a direct feedback from the drain to the source leads to two severe problems. Firstly, the impedance seen from the source ($1/g_m$) significantly degrades the quality factor of the tank. This impedance combines with the parallel loss resistance of the tank in parallel. The total parallel loss of the tank decreases and gets lower than $1/g_m$ because this resistive load of the transistor is smaller than the loss of the tank. Consequently, the loaded quality factor of the tank degrades as the total parallel loss drops. Secondly, the loop gain $1/g_mR_{ploaded}$ falls below unity showing that the start-up condition cannot be met thereby making the network impossible to oscillate. To cope with these two issues, an impedance transformer can be added to the network. One solution of transforming the impedance to a higher value is via the usage of a capacitive or inductive divider. If the tank is employed with a capacitive divider, the circuit is called a Colpitts oscillator; whereas the circuit including an inductive divider is called a Hartley oscillator. In IC technology, it is much more practical to design Colpitts type rather than Hartley to get rid of the implementation of one inductance more.

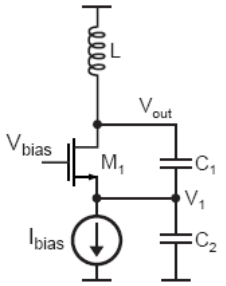


Figure 2.13: Single ended Colpitts oscillator

Fig 2.13 shows the basic structure of a Colpitts oscillator. The parallel resonant tank comprises L and the parallel combination of C_1 and C_2. The loop circuit is realized with a common gate stage and the capacitors.

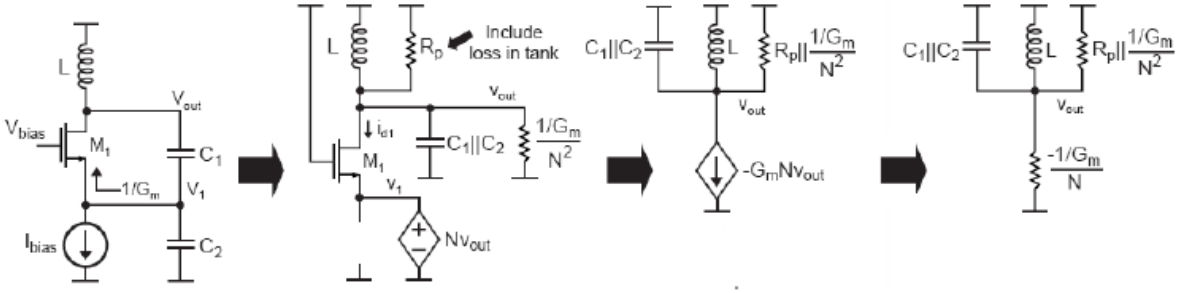


Figure 2.14: Negative Gm Analysis of Colpitts oscillator

Fig. 2.14 illustrates this transformation step by step. In a lossless step down transformer with a ratio of 1:N, the parallel resistance increases by $1/N^2$ and in a Colpitts oscillator the capacitive divider has a ratio of

$$N = \frac{C_1}{C_1 + C_2} \qquad \textbf{(2.10)}$$

Here, for the simplicity of calculations it is assumed the impedances of the capacitors are less than the source impedance $1/g_m$ so the voltage ratio is determined only by the capacitors. The capacitive divider transforms the parallel resistance of the source impedance to $(1+C_1/C_2)^2/g_m$. This impedance in parallel with R_p defines the total parallel resistance of the tank. Besides, the relationship between the source (or the input) voltage NV_{out} and the drain current can be resulted to $-G_mNV_{out}$ as the expression of output current, therefore, the output impedance is converted to a negative resistor: $-1/G_mN$.

On the other hand, the addition of capacitive divider concludes to a higher g_m value in order to meet oscillation start-up condition. Firstly, assuming parallel loss resistance of the tank is higher than the drain impedance of the resistance, R_{eq} is now equal to R_p. Secondly, according to [3], the ratio N is chosen as 1/5 for the best noise performance. In these cases, from one-port view of oscillators we obtain the below equation:

$$R_p = \frac{1/G_m}{N} = \frac{1/G_m}{5} \tag{2.11}$$

in steady-state oscillation. In other words, assuming the start-up loop gain as 2, g_m must be at least 2N times more than $1/R_p$ to achieve sustained oscillation. This is an important drawback in oscillator design. The transistor width must be increased to get a higher G_m value for a constant bias current. This leads to higher transistor thermal noise and lower tuning range because of greater parasitic capacitances.

The differential output can be provided by combining two identical single-ended oscillators as shown in Fig 2.15. If the circuit is perfectly matched, both sides carry out of phase signals of equal amount. In this case, source to ground capacitor shared by two sides behaves like a virtual ground since the differential signals cancel each other at that midpoint. The differential operation is guaranteed unless this midpoint is connected to the ground [6]. Compared with the single ended topology the power consumption is doubled if the device values are kept.

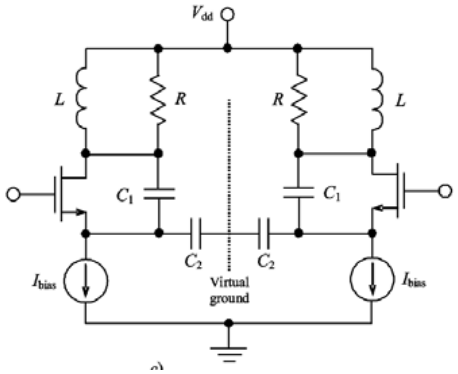


Figure 2.15: Differential Colpitts oscillator

Because of the push-pull operation of the transistors, DC current is drawn from current sources only during a half period from current sources so they can be replaced with one current source which is able to switch the current after each half period. This can be accomplished with a pair of cross-coupled NMOS transistors.

This structure shown in Fig. 2.16 provides a synchronized current switching from one side to another, and also negative resistance generated by the cross-coupled pair relaxes the oscillation start up condition.

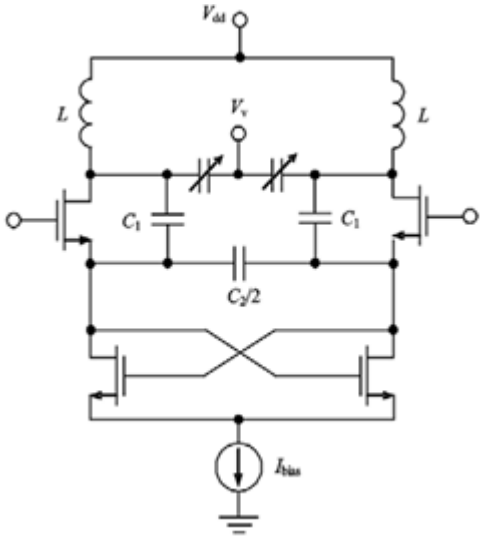


Figure 2.16: Current shifting differential Colpitts Oscillator [6]

Similar to the above oscillator, the circuit in Fig 2.17 can also be implemented to eliminate the tough start-up condition of a conventional differential Colpitts oscillator. The idea comes from a floating gate voltage. One way to raise G_m is to increase the voltage between gate and source. Instead of an AC grounded gate, the signal as the inverted voltage of the source can be applied to the gate of the transistor. If one replica of one transistor is added and the gate terminals of these blocks are coupled crosswise, G_m requirement will be relaxed. In this new differential Colpitts topology, negative conductance is increased by a factor of $(2+C_2/C_1)$ or 1+A where A is called G_m boosting factor of the proposed Colpitts oscillator [7]. Two current sources can be combined using two transistor added in cascade way. Their gates are connected to the outputs of the oscillator in order to relax voltage headroom requirements.

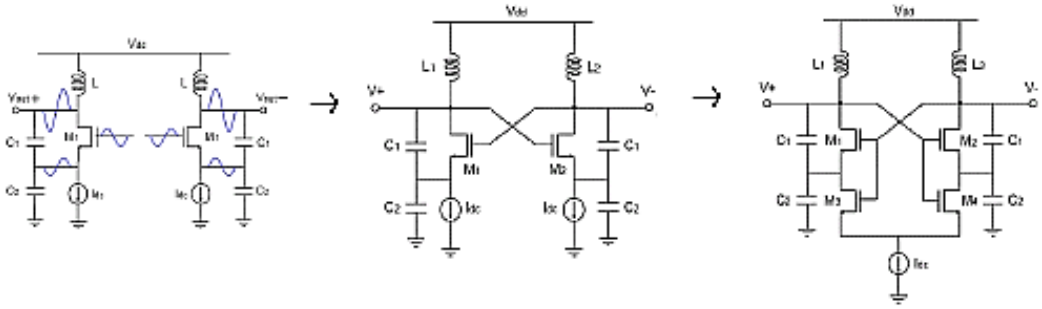


Figure 2.17: Gm Boosted differential Colpitts oscillator [7]

3. OSCILLATOR NOISE

In this chapter, the oscillator phase noise is focused on. After a brief definition of the phase noise and its effect on RF transceivers, the expressions of two phase noise models are obtained via a step by step transformation methodology, also, by explaining the underlying approaches; LTV and LTI. The phase noise expressions are commented to provide practical conclusions. This topic ends with a very detailed and useful analysis of the phase noise sources in a cross-coupled LC VCO.

3.1 General Definition

There are two kinds of noise classes affecting the response of a voltage controlled oscillator. The extrinsic noise is generated by the other blocks that are working with VCO such as the loop filter producing the control voltage of a VCO and the frequency divider in a PLL. The intrinsic noise is created by the physical structure and the process dependency of the active and passive devices in the oscillator. The noise injected from both types may disturb both the frequency and the amplitude of the output signal. The noise in the amplitude is generally negligible because the non-linearity characteristic of the active device stabilizes the amplitude's noise. The phase noise, on the other hand, is essentially a random deviation in frequency which can also be viewed as a random variation in the zero crossing points of the time-dependent oscillator waveform. It is also one of the main determinants on the VCO specifications. In time domain, phase noise is defined as jitter. Fig 3.1 shows the phase noise and its correspondence in time domain.

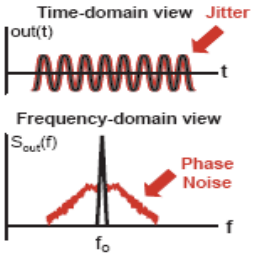


Figure 3.1: Phase noise in time and frequency domain

Let $x(t) = A\cos[\omega_o t + \varphi_n(t)]$ where A is the noiseless oscillator amplitude, ω_o is the oscillation frequency, $\varphi_n(t)$is the phase noise, $x(t)$ is the sinusoidal oscillator output signal. $x(t)$ can be extracted as $A[\cos(\omega_o t)\cos(\varphi_n(t)) - \sin(\omega_o t)\sin(\varphi_n(t))]$ and for very small values of $|\varphi_n(t)|$, $x(t) \approx A\cos(\omega_o t) - A\varphi_n(t)$ since $\cos(\varphi_n(t)) \approx \cos(0) = 1$ and $\sin(\varphi_n(t)) \approx \sin(0) = \varphi_n(t)$. Therefore, the spectrum of phase noise is translated to the oscillation frequency. However, the tank in the oscillator can filter the out of band signals only to some degree. Its filtering capability increases as the signals move farther from the oscillation frequency ω_o. Consequently, the phase noise around the oscillation frequency is shaped like skirts in the frequency domain (Fig. 3.2).

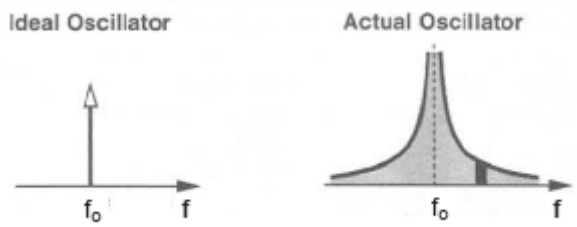


Figure 3.2: Spectrums of output waveforms of an ideal and a real oscillator

To measure the phase noise, the noise at a distance or an offset of Δω away from the carrier frequency integrated over a 1Hz bandwidth is defined. The ratio of this noise power to the carrier power in logarithmic scale gives the phase noise at Δω offset.

$$L(\Delta\omega) = 10\log\left(\frac{P_{tone}(\Delta\omega, 1Hz)}{P_{carrier}}\right) \quad \textbf{(3.1)}$$

where $P_{tone}(\Delta\omega, 1Hz)$ represents the unity bandwidth noise power at $\Delta\omega$ and $P_{carrrier}$ is the power of the carrier. $L(\Delta\omega)$ denoted by dBc/Hz simply points out how many dB this noise power is below the carrier power.

3.2 Impact of Phase Noise on Transceiver Architectures

In a front-end part of a transceiver, the signal delivered from the antenna is downconverted to a lower intermediate frequency without any change in shape by the local oscillator. In the presence of a strong interferer standing close to the desired signal, the local oscillator downconverts both. The phase noise skirts of the LO modulates onto the strong interferer and this cause the overlapping of two signals at IF as depicted in Fig. 3.3, thereby, this reduces the signal-to noise ratio (SNR) of the desired signal at IF. This effect is also called the reciprocal mixing.

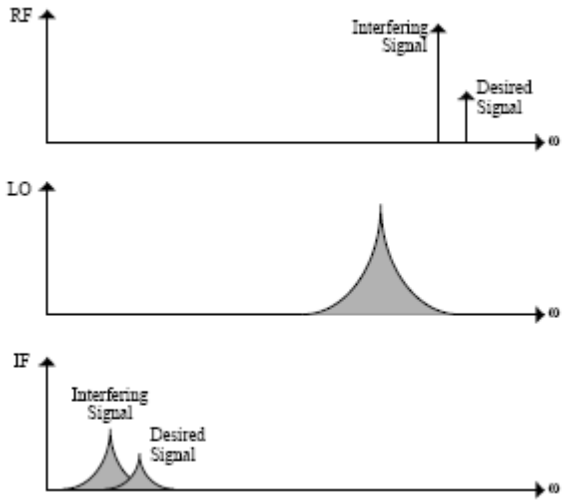


Figure 3.3: Effect of phase noise in receivers

In the transmitter part, the phenomenon is quite similar. A strong interferer modulated by the local oscillator attains a widening spectrum as the offset increases since it is amplified by the PA. Its skirts extend over the desired signal in the receiver part and corrupt it. This effect also causes an extravagant consumption of out of band energy.

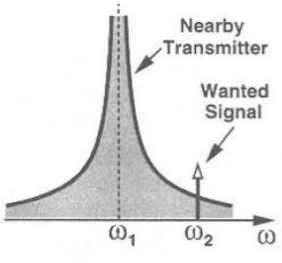


Figure 3.4: Effect of phase noise in transmitters

3.3 Phase Noise Models

In literature, there exist two phase noise models depending on different system approaches for oscillators.

3.3.1 Leeson's Phase Noise Model

Considering one-port view of an oscillator, the intrinsic noise sources can be put in two categories; the noise of the resonator and the noise of the active negative resistance generator. The loss of the passive elements in the tank falls into the first category. The thermal and the flicker noise of the active device are the main sources

of the latter category. However, only the thermal noise of the active part is attributed to this category since it is assumed as a negative resistance in the model of two one-port.

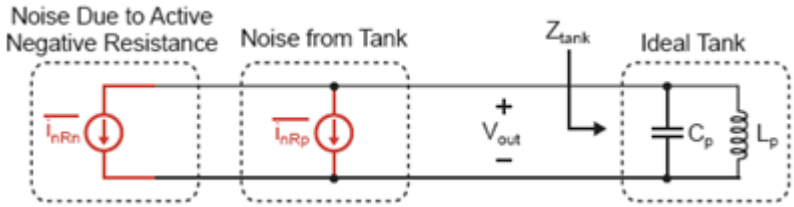


Figure 3.5: One-port view of LC oscillator with noise sources

The one port view of an LC oscillator with noise sources can be illustrated as in Fig. 3.5 to determine how these categories affect the phase noise of the oscillator. Here, the tank is realized as an ideal one because the loss of the tank is compensated by the active circuitry.

The input impedance of the tank at the frequency ω is simply expressed as

$$Z(\omega) = \frac{j\omega L_p}{1 - \omega^2 j\omega L_p C_p} \tag{3.2}$$

The above expression can be rewritten for the frequency $\omega = \omega_o + \Delta\omega$ where ω_o, the oscillation frequency is equal to $1/\sqrt{L_p C_p}$ and $\Delta\omega$ is the offset frequency

$$Z(\Delta\omega) = \frac{j(\omega_o + \Delta\omega)L_p}{1 - (\omega_o + \Delta\omega)^2 j\omega L_p C_p} \tag{3.3}$$

After the expansion of the square term in the denominator part, we get

$$Z(\Delta\omega) = \frac{j(\omega_o + \Delta\omega)L_p}{1 - {\omega_o}^2 L_p C_p - 2\Delta\omega\left(\omega_o L_p C_p\right) - \Delta\omega^2 L_p C_p} \tag{3.4}$$

Since $1 - {\omega_o}^2 L_p C_p = 0$ and $\Delta\omega^2 L_p C_p$ is negligible, the expression can be simplified to

$$Z(\Delta\omega) \approx \frac{j(\omega_o + \Delta\omega)L_p}{-2\Delta\omega\left(\omega_o L_p C_p\right)} \tag{3.5}$$

Taking into account that $\omega_o \gg \Delta\omega$, the numerator part of the expression can be simplified to

$$Z(\Delta\omega) \approx -\frac{j}{2}\frac{1}{C_p}\left(\frac{\omega_o}{\Delta\omega}\right) \tag{3.6}$$

The quality factor of the tank due to the parallel resistance R_p is equal to $\omega_o R_p C_p$ so we can parameterize the ideal tank impedance in terms of Q of the actual tank as

$$Z(\Delta\omega) \approx -\frac{j}{2}\frac{R_p}{Q}\left(\frac{\omega_o}{\Delta\omega}\right) \tag{3.7}$$

By squaring both sides we reach the expression below in terms of $\Delta\omega$ away from center frequency;

$$|Z_{tank}(\Delta\omega)|^2 \approx \left(\frac{R_p}{2Q}\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3.8}$$

At this point, it is possible to derive an expression for the total output noise with respect to offset frequency

$$\frac{\overline{v_{out}^2}}{\Delta\omega} = \left(\frac{\overline{i_{nRp}^2}}{\Delta\omega} + \frac{\overline{i_{nRn}^2}}{\Delta\omega}\right)|Z_{tank}(\Delta\omega)|^2 \tag{3.9}$$

The above expression includes both the amplitude and phase noise of the oscillator. After arranging the expression we get,

$$\frac{\overline{v_{out}^2}}{\Delta\omega} = \frac{\overline{i_{nRp}^2}}{\Delta\omega}\left(1 + \frac{\overline{i_{nRn}^2}}{\Delta\omega}\Big/\frac{\overline{i_{nRp}^2}}{\Delta\omega}\right)|Z_{tank}(\Delta\omega)|^2 \tag{3.10}$$

The term in large brackets called *F(Δω)* is defined by

$$\mathrm{F}(\Delta\omega) = \left(1 + \frac{\overline{i_{nRn}^2}}{\Delta\omega}\Big/\frac{\overline{i_{nRp}^2}}{\Delta\omega}\right) = \frac{\text{total noise in tank at } \Delta\omega}{\text{noise in tank due to tank loss at } \Delta\omega} \tag{3.11}$$

Since $i_{nRp}^2/\Delta\omega$ equals to $4kT/R_p$ for the single-sided spectrum, the output noise spectrum density due to tank loss is

$$\frac{\overline{v_{out}^2}}{\Delta\omega} = \frac{\overline{i_{nRp}^2}}{\Delta\omega} \mathrm{F}(\Delta\omega)|Z_{tank}(\Delta\omega)|^2 = 4kT\mathrm{F}(\Delta\omega)R_p\left(\frac{1}{2Q}\frac{\omega_o}{\Delta\omega}\right)^2 \quad \textbf{(3.12)}$$

According to equipartition theorem, if the output signal is a sinusoidal wave, the noise impact splits equally into amplitude and phase [8].

$$\left.\frac{\overline{v_{out}^2}}{\Delta\omega}\right|_{PHASE} = 2kTF(\Delta\omega)R_p\left(\frac{1}{2Q}\frac{\omega_o}{\Delta\omega}\right)^2 \quad \textbf{(3.13)}$$

From the above equation, the phase noise is expressed as:

$$L(\omega) = 10\log\left(S_{noise}(\Delta\omega)/P_{sig}\right) = 10\log\left(\frac{1}{R_p}\left.\frac{\overline{v_{out}^2}}{\Delta\omega}\right|_{PHASE}\Big/P_{sig}\right) \quad \textbf{(3.14)}$$

$$L(\omega) = 10log\left(\frac{2kTF(\Delta\omega)}{P_{sig}}\left(\frac{1}{2Q}\frac{\omega_o}{\Delta\omega}\right)\right)^2 \quad \textbf{(3.15)}$$

The two noise contributors have the same phase noise spectral density since they have equal absolute resistance values. Hence, $\mathrm{F}(\Delta\omega) = 2$ and the system's phase noise is defined by

$$L(\omega) = 10log\left(\frac{4kT}{P_{sig}}\left(\frac{1}{2Q}\frac{\omega_o}{\Delta\omega}\right)\right)^2 \quad \textbf{(3.16)}$$

The above equation corresponds to -20dBc/Hz change of phase noise per decade. In reality, this is not completely true because the noise of the active negative resistance generator is more sophisticated. In the derivation of the equation, since switching transistors are modeled as resistors, they only generate thermal noise. However, recalling a cross-coupled topology, firstly, the flicker noise of all transistors must also be considered. Secondly, the noise of the bias transistor is modulated on to the output voltage. Thirdly, the noise is influenced during switching operation of cross-coupled transistors. Fourthly, and last, these transistors while operating in triode region may have low output impedance and therefore, result in a drop-off on the quality factor of the tank.

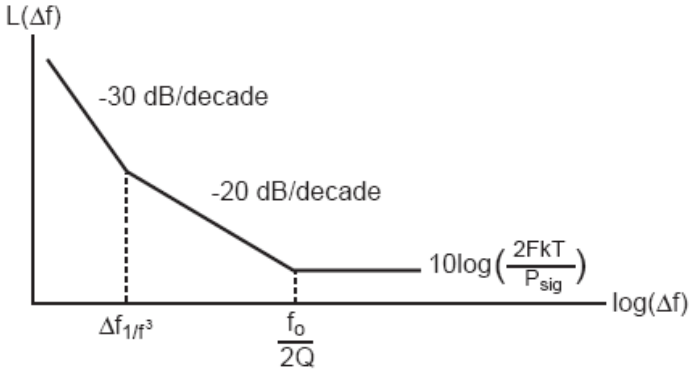


Figure 3.6: Phase noise spectrum of an actual oscillator

The phase noise spectrum of an actual oscillator is shown above. At low offset frequencies, the phase noise degrades -30 dB/decade. Then, for a wide range of offset frequency, the slope is fixed to -20 dB/decade. At a very high offset, the noise floor forms and the slope flattens.

Leeson proposes a semi-emprical formula of the phase noise satisfying both the basic phase noise equation 3.16 and the characteristic of the phase noise spectrum of an oscillator. He assumes that F(Δω) is independent of frequency and describes F as an empirically-determined parameter.

$$L(\omega) = 10log\left(\frac{2kTF}{P_{sig}}\left(1+\left(\frac{1}{2Q}\frac{\omega_o}{\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right) \quad \textbf{(3.17)}$$

where $\Delta\omega_{1/f^3}$ is the boundary frequency between $1/f^2$ and $1/f^3$ regions. It is assumed that this parameter is equal to noise corner frequency of the device.

Examining (3.17), it is indicated that the phase noise is inversely proportional to the average power dissipated in the tank resistance and second order of the quality factor. Therefore, the phase noise performance can be improved by increasing the oscillation voltage amplitude and choosing higher Q inductors among possible alternatives.

3.3.2 Lee and Hajimiri's Phase Noise Model

It is clear that the Lesson's model does not reveal the impact of all noise sources on phase because this model is based on empirical fitting parameters such as F and $\Delta\omega_{1/f^3}$. In general, $\Delta\omega_{1/f^3}$ is not equal to 1/f corner frequency, thus it should be measured before calculating the phase noise. Furthermore, in the case of more than

one active device contributing 1/f noise, no information is mentioned about whose 1/f corner frequency will determine $\Delta\omega_{1/f^3}$. Also, according to Leeson's formula higher Q values lead to a better phase noise performance, but boosting Q of the tank increases F factor as well [9]. As a result of these drawbacks, Leeson's phase noise equation needs to be revisited. Lee and Hajimiri first observed the impulse response of an ideal oscillator in order to model the noise of an oscillator (Fig. 3.7).

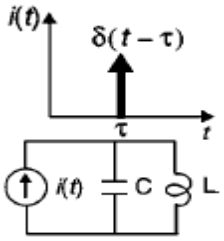


Figure 3.7: Ideal LC oscillator stimulated by a current pulse

Fig. 3.8 shows how an impulse of current affects the response of a lossless resonator at different times. If an impulse is injected at the peak of the signal, it only causes a change in the amplitude with an amount of $\Delta V=\Delta Q/C$ where ΔQ denotes the total charge variation across the resonator; no variation in phase. On the other hand, if an impulse is injected at the zero crossing of the signal, there occurs an influence only in the phase, not in the amplitude. The injection of current pulse during any other time period impacts the amplitude of the output signal and also shifts the zero crossing point of the oscillation. The amount of phase disturbance for a given injected impulse depends on the time in which when the injection occurs; an oscillator is therefore a periodically time-varying (LTV) system [9]. It is also linear since the amount of amplitude disturbance depends on the amplitude of the impulse current [10].

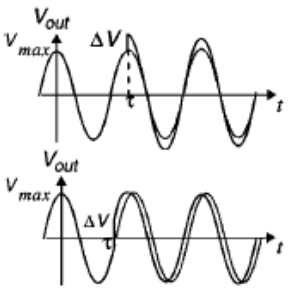


Figure 3.8: Impulse effects on a sinusoidal output waveform

As mentioned earlier, the amplitude variations are generally ignored because the gain control mechanism of the oscillator, as a result of nonlinearity, alleviates them over time as depicted in Fig. 3.9.

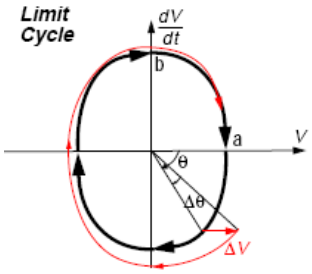


Figure 3.9: Damping of amplitude variation in one oscillation cycle

Therefore, according to this theory, for a minimal phase noise, any noise impulse must coincide in time with the peaks of the output voltage.

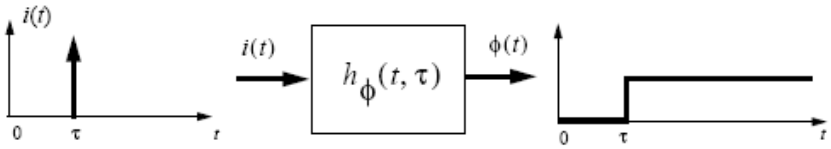


Figure 3.10: Characteristic of an impulse response in time domain

Fig 3.10 depicts the impulse response in time domain. Since an impulse produces a step change in phase, the phase impulse response of the oscillator can be expressed as

$$h_\varphi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \qquad \textbf{(3.18)}$$

where u(t) is the unit function. Γ(x) is called impulse sensitivity function (ISF). It is an amplitude and frequency independent, dimensionless function periodic in 2π. It describes how much phase change occurs from applying an impulse at time: t=T·x/2π. It is roughly equal to the derivative of the output voltage waveform as seen in Fig 3.11 illustrating the ISF function of an LC oscillator.

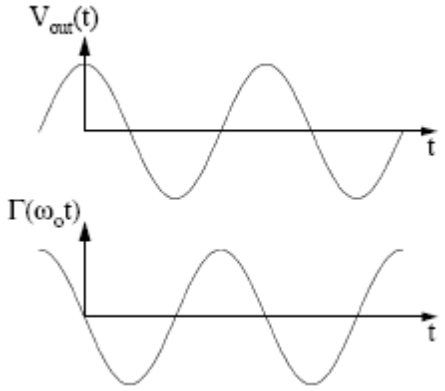


Figure 3.11: ISF function of an LC oscillator

As a result, the amplitude of the ISF function marks where the output of the oscillator is most sensitive to the noise current injected into the tank causing phase noise.

The phase noise of a noise current input can be computed by using superposition integral because of its linearity property.

$$\varphi(t) = \int_{-\infty}^{\infty} h_{\varphi}(t,\tau) i(\tau) d(\tau) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau) i(\tau) d(\tau) \qquad \textbf{(3.19)}$$

This computation is illustrated with the aid of the equivalent block diagram shown in Fig. 3.12.

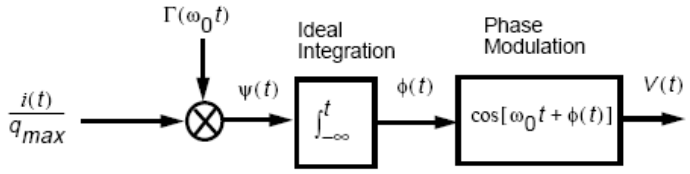


Figure 3.12: Block diagram describing the response of a current impulse on output wave

Since periodic functions can be extracted as a Fourier series, we can rewrite ISF function as

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \qquad \textbf{(3.20)}$$

where all of the coefficients are real and θ_n is the excess phase of the nth harmonic. Here, θ_n will be ignored for the rest of the calculations because it is assumed that

noise components are uncorrelated [9]. As a result, after ISF decomposition phase is defined as

$$\varphi(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d(\tau) + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau + \theta_n)\, d(\tau)\right] \quad \textbf{(3.21)}$$

The expression above can be visualized as below similarly to Fig 3.13.

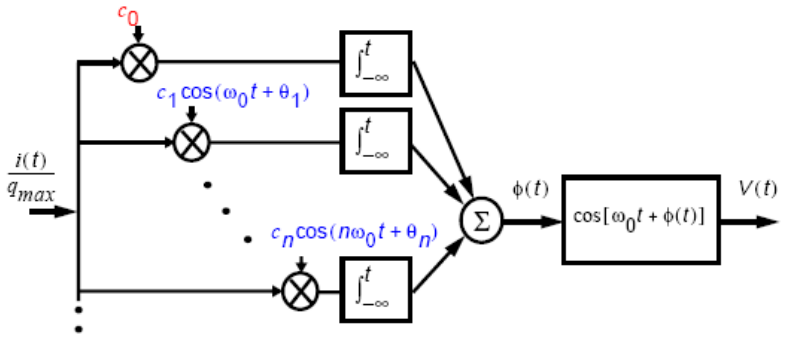


Figure 3.13: Block diagram of ISF decomposition

Consequently, this model shows that any noise current injected to an oscillator produces phase noise components at different frequencies depending on the coefficients of ISF. This behavior is illustrated in Fig. 3.14.

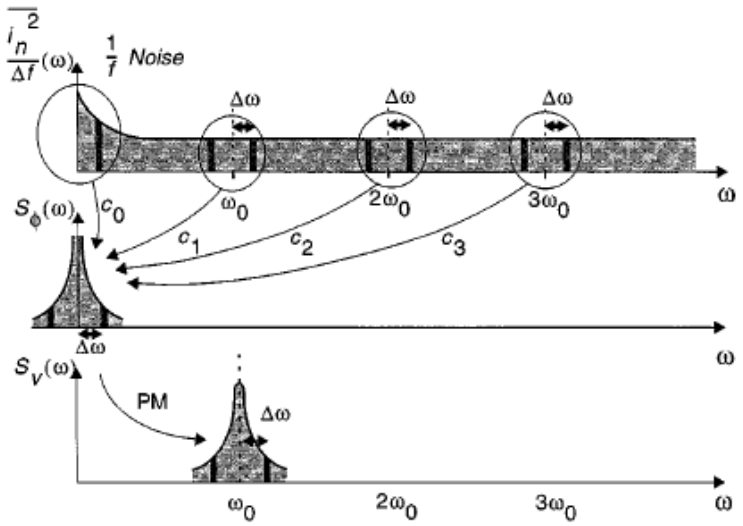


Figure 3.14: Evolution of current noise into phase noise

The flicker noise of the active devices weighted by ω_0 is upconverted to $1/f^3$ noise and sets around carrier. The noise close to oscillation frequency is also present and weighted by c_1. The phase noise in $1/f^2$ region comes from downconverted thermal noise at some harmonic frequencies. For instance, noise around $2\omega_0$ is

downconverted depending on c_2, noise around $3\omega_0$ is downconverted depending on c_3, and so on...

The phase noise expression of this model in $1/f^2$ region is given below:

$$L(\Delta\omega) = 10log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{i_n^2/\Delta f}{4\Delta\omega^2}\right) \quad \textbf{(3.22)}$$

where i_n is the noise current magnitude, Δf is the noise bandwidth, $\omega_{1/f}$ is the 1/f noise corner frequency of the device, $\Delta\omega$ is the offset from the carrier frequency, q_{max} is the maximum charge on the capacitors in the resonator, and Γ_{rms} is the rms value of the ISF.

An expression of the phase noise in $1/f^3$ region can be derived if it is assumed that the noise current coming from flicker noise is defined as below:

$$\overline{i_{n,1/f}^2} = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega} \quad \textbf{(3.23)}$$

Since the DC value of ISF function is equal to c_0, the phase noise in $1/f^3$ region is obtained as follows by combining the equations (3.22) and (3.23):

$$L(\Delta\omega) = 10log\left(\frac{c_0^2}{q_{max}^2}\frac{i_n^2/\Delta f}{8\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right) \quad \textbf{(3.24)}$$

By equalizing (3.22) to (3.24), the corner frequency of $1/f^3$ region is given as:

$$\Delta\omega_{1/f^3} = \omega_{1/f}\frac{c_0^2}{4\Gamma_{rms}^2} = \omega_{1/f}\left(\frac{\Gamma_{dc}}{\Gamma_{rms}}\right)^2 \quad \textbf{(3.25)}$$

Consequently, the phase noise of an oscillator at all offsets can be reduced by decreasing the coefficients of the ISF since $\sum_{n=0}^{\infty} c_n^2 = 2\Gamma_{rms}^2$. Equation (3.25) shows that lowering the dc value of ISF narrows the $1/f^3$ region in the phase noise spectrum. In an LC oscillator, this is accomplished by making the oscillator waveforms symmetrical with respect to rise and fall times. Moreover, this model discloses that the phase noise reduces if the energy of the LC tank is replenished by the active device when the output wave is at its maximum value.

3.3.3 F-parameter Extraction

Rael and Abidi investigated the physical processes of all noise sources generating phase noise in a differential LC oscillator in [11]. They attribute these sources' mathematical expressions into the semi-empirical fitting parameter F:

$$F = \underbrace{1}_{resonator} + \underbrace{\frac{2\gamma R_p I_{bias}}{\pi V_0}}_{switching\ pair} + \underbrace{\gamma \frac{4}{9} g_{d0,bias} R_p}_{bias\ transistor} \quad \textbf{(3.26)}$$

If an oscillator operates in current-limited region, the second term simplifies to 2γ and the phase noise which is inversely proportional to V_0^2 reduces as the bias current increases. However in voltage-limited region where the output voltage amplitude is limited by the supply voltage, V_0 remains the same whereas bias current increases so F starts to increase and, hence the phase noise degrades proportionally to I_{bias}. The best phase performance is met when the switching pair is biased between these regimes [11, 12].

3.4 Phase Noise Sources in Cross-Coupled LC-VCO

In this section a more detailed analysis of phase noise sources is explained. Differently from section 3.2.2, the tank generated noise will not be inspected in detail, and several phase noise mechanisms in the switching pair and the bias transistor will be the center of attention.

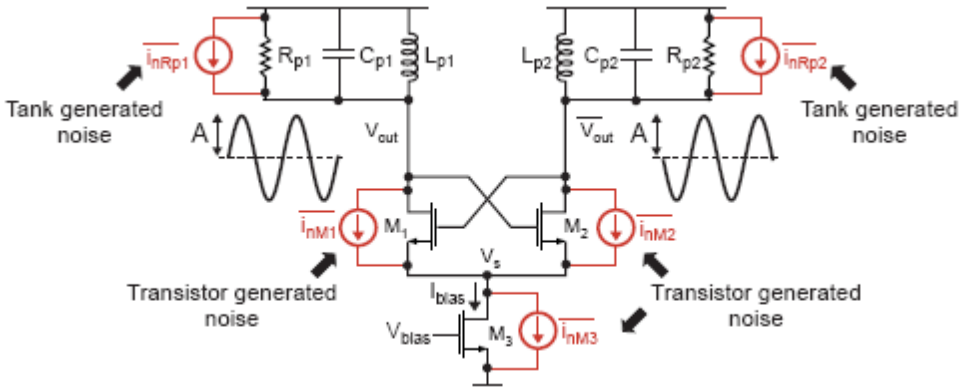


Figure 3.15: Noise generators in a cross-coupled LC VCO

3.4.1 Transistor Generated Noise

As mentioned in Hajimiri and Lee's phase noise model, the phase noise is generated not only from high frequencies but also from low frequency noise of the active device. For this reason, it is favorable to start this section by explaining all noise sources in a MOSFET device.

3.4.1.1 MOSFET Noise Sources

The noise sources in a MOSFET are categorized as the intrinsic and extrinsic noise sources. All noise sources can be modeled in a lumped network model as depicted in Fig 3.16. The extrinsic noise comes from the parasitic resistances of the terminal connections of the device and the metal to semiconductor junctions found at the contacts at these terminals. The intrinsic noise can also be divided into two subcategories; thermal noise and flicker noise…

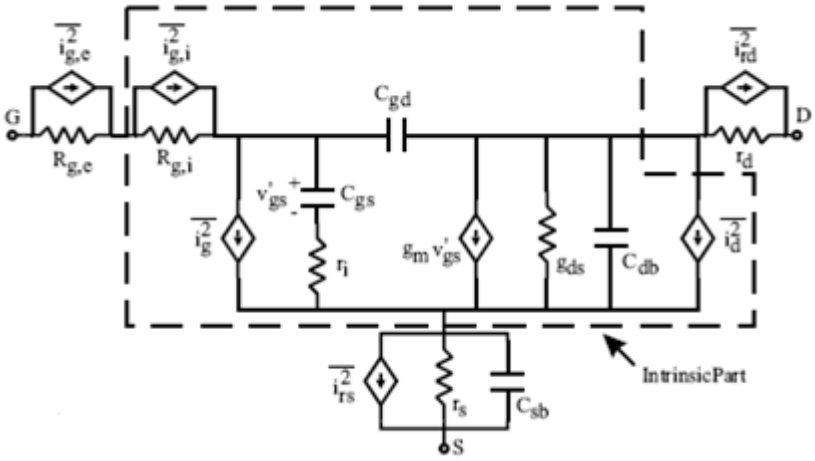


Figure 3.16: Lumped noise model of a MOSFET

Thermal Noise

The intrinsic thermal noise arises from three important sources. The first source is the gate resistance noise. The resistance of the gate material, given by $Rg=(W\times R_{\square})/(N\times L)$, where $R_{\square}$ is the sheet resistance of the gate material and N is the number of fingers, contributes to the thermal noise presence in the device. The value of the lumped resistor of the distributed gate material shown at the gate of the MOSFET in Fig. 3.16 can be reduced due to proper layout techniques. When the gate is only connected from one end, $R_{g,i} = R_g/3$. However, if the gate is folded or is connected by both sides, this leads to a decrease in $R_{g,i}$ by a factor of 4 [2]. In terms

of the equivalent gate resistance and the transistor's dimensions, the gate resistance noise is given by,

$$\overline{v_{g,i}^2} = 4kTR_{g,i}\,\Delta f \quad \textbf{(3.27)}$$

where *k* is Boltzmann's constant and *T* is the temperature in Kelvin. Note that the gate resistance noise is proportional to the width, inversely proportional to the length of the device, and scales in inverse proportion to the number of fingers used in the transistor layout.

The second source of thermal noise in a MOSFET is the thermal channel noise. It is composed of drain channel noise, $\overline{i_d^2}$ and induced gate noise, $\overline{i_g^2}$. The drain channel noise is generated by the carriers in the channel region and represented as a noise current. It is the most significant contributor to thermal noise in a MOSFET. Assuming that MOSFET operates in saturation region, the drain channel noise is approximately given by

$$\overline{i_d^2} = 4kT\gamma\, g_{do}\,\Delta f \quad \textbf{(3.28)}$$

where γ is a bias dependent parameter and g_{do} is the zero drain voltage conductance of the channel. Generally, in the expression above g_m is referred to g_{do} since long channel devices with zero drain to source voltage exhibit equal values in saturation. The factor γ is an increasing function of V_{DS}, but a value of 2/3 is often used for long-channel devices. This coefficient has a greater value for short channel devices.

The induced gate noise is a weak noise current at the gate terminal produced by the coupling of the fluctuations in the channel with the transistor gate via the oxide capacitance. The approximation for this noise type made by Van der Ziel is given as

$$\overline{i_d^2} = 4kT\beta\frac{(\omega C_{gs})^2}{k_{gs}}\Delta f \quad \textbf{(3.29)}$$

where β is a bias-dependent parameter typically greater than or equal to 4/3. The factor $1/k_{gs}$ arises from a first-order expansion that gives k_{gs} = 5 for long channel devices. Interestingly, the induced gate noise is proportional to the square of the frequency. Clearly, this expression cannot hold as the frequency becomes extremely large.

Fig 3.17 illustrates these two channel noise mechanisms. Since they have the same physical noise sources; the carriers in the channel, the channel drain noise and the induced gate noise are correlated.

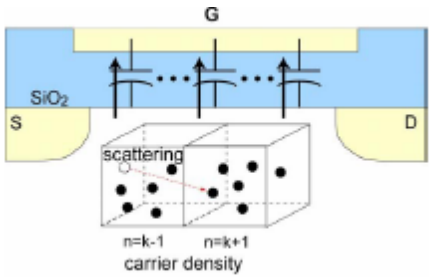


Figure 3.17: Illustration of channel drain noise and induced gate noise

Flicker Noise

The noise spectral density exhibits an increasing shape as the frequency decreases. This excess noise level, different from thermal noise, starts from a corner frequency of approximately between 100 kHz and several MHz for MOSFETs. It is also called 1/f noise due to inverse relationship to frequency.

There are two dominant theories on the origins of 1/f-noise in MOSFETs. First, the carrier density fluctuation theory manifest that the random trapping and release of charges by the oxide traps near the Si-SiO2 interface beneath the gate is the reason of the flicker noise. The channel surface potential fluctuates because of this charge fluctuation; therefore the channel carrier density is in turn modulated by the channel surface potential fluctuation. According to this theory, the flicker noise is independent of the gate bias voltage and the noise power is proportional to the interface trap density. The second major theory, called the mobility fluctuation theory, betrays the origin of the flicker noise as the fluctuation in bulk mobility based on Hooge's empirical relation for the spectral density of flicker noise in a homogenous medium. However, this theory reveals that 1/f noise is dependent upon the gate bias voltage. The fig 3.3 illustrates the trap/detrap of charges and the fluctuation of the mobility in red and blue colors, respectively.

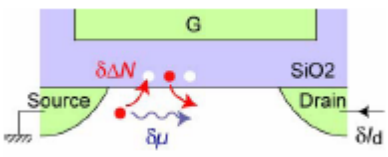


Figure 3.18: Sources of flicker noise

The most known equation of flicker noise of a MOS transistor in saturation is given as;

$$\overline{i_f^2} = K_f \frac{g_m^2}{C_{ox}^2 WL} \frac{\Delta f}{f^{\propto}} \quad \textbf{(3.30)}$$

for the flicker-noise current. The value of α is typically close to unity, and K_f is in general a bias-dependent parameter, on the order of 10–14 C/m2 for PMOS devices and 10–15 C/m2 for NMOS devices.

3.4.1.2 AM-PM Conversion Mechanisms

In this subsection the conversion mechanism of amplitude modulation into phase modulation will be discussed. This conversion mainly takes place in the switching pair and the varactor.

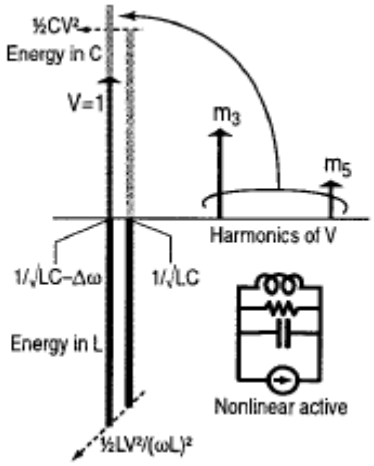


Figure 3.19: Impact of output harmonics on reactive power of an LC tank

The switching pair in the oscillator drives the LC tank not only with the fundamental waveform but also with its harmonics because of the nonlinearity behavior of the transistors. In steady state, these harmonics flowing into the capacitor of the tank which has lower impedance create an imbalance in the tank since the reactive powers of the inductor and the capacitor must be equal in resonance. In order to stabilize, the inductor increases its reactive power by shifting down the oscillation frequency because the energy stored in the inductor is defined as $0.5LV^2/(\omega L)^2$ [13]. Consequently, any change in the output waveform also reflects to its harmonics and will result in frequency deviations so the phase noise will arise.

The fundamental voltage and its harmonics across the tank are proportional to:

$$Fundamental\ voltage\ \propto \frac{IQ}{\omega_o C} \quad \textbf{(3.31a)}$$

$$nth\ Harmonic\ voltage\ \propto \frac{1}{n}\frac{I}{n\omega_o C} \quad \textbf{(3.31b)}$$

Here, (3.31) shows that the harmonics is a function of bias current. The sensitivity of oscillation frequency with respect to bias current causes an indirect FM due to flicker noise in bias transistor [11]. The other mechanism of indirect FM is the characteristics of the intrinsic capacitances of the active devices at RF. These capacitances which are collected at the drain terminal of the tail transistor appear like a negative capacitor across the resonator and the current flowing on this negative capacitor is commutated by the differential pair [14]. The flicker noise in differential pair modulates the duty cycle of this commutation thus shifting up the oscillation frequency [11].

One solution to decrease the AM-PM conversion across the switching pair is to increase the quality factor of the resonator so the harmonics can be suppressed more effectively since the ratio of fundamental voltage to nth harmonic voltage is $1/n^2Q$ as presented at (3.31).

Another solution is to increase the linear range of the switching pair. This can be accomplished by increasing the overdrive voltage of these transistors so that the harmonic distortion reduces or by decreasing the intrinsic device capacitances since at high frequencies these capacitances get effective and increase the harmonic distortion.

The second mechanism of AM-PM conversion occurs with the usage of nonlinear devices in the varactor structure. The varactor enables the oscillation frequency shift with a control voltage. However, the varactors such as diode and MOSCAP realized in a VCO have nonlinear characteristics so any dc variation at the control voltage will lead to deviations in the oscillation frequency, thereby generating phase noise at the output.

The effective capacitance value also depends on the output amplitude. The large AC signal on either node causes the varactor to take different capacitance values at each

instance of time leading to phase noise. This plays an important role in phase fluctuations especially if the varactor has high gain. For example, in the presence of a diode varactor, during a certain period of time the large signal amplitude can force the diode to enter the forward-bias region where the characteristic of the varactor sharpens abruptly and its quality factor degrades remarkably after the transition from reverse-bias region, resulting in a significant variation on the effective capacitance. For this reason, this situation should be considered in diode varactor design and the operation of the varactor in forward-region must be avoided. Furthermore, the reverse bias voltage must increase as much as possible because the nonlinearity reduces as the reverse control voltage of the diode varactor increases. In the presence of an inversion mode MOS varactor, for the first and the third cases in Fig. 3.20, no AM-PM conversion occurs, however if the control voltage is applied to any transition point between the maximum and the minimum values of the varactor, the amplitude variations modulate the effective capacitance and FM modulation occurs. This conversion reaches its maxima when the control voltage is biased on the mid-point of the transition. AM-PM conversion can be reduced by using switched capacitor arrays in tuner structure or reducing the C_{max}/C_{min} ratio of the varactor.

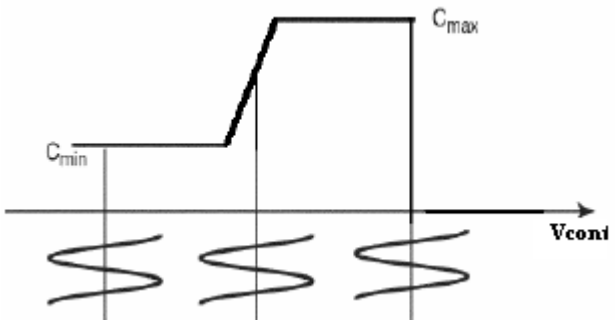


Figure 3.20: Different control voltages applied to IMOS varactor with AC component

3.4.1.3 Bias Generated Noise

In bias circuit, there exist two noise sources causing the phase noise at the output of the oscillators; the low frequency flicker noise and the high frequency thermal noise of the bias transistor. Due to the switching operation of the cross-coupled pair, these transistors act as mixers and upconvert the flicker noise component of the bias transistor at ω_n to two sidebands at ω_o-ω_n and ω_o+ω_n. Since these two frequencies lay at an equal distance from the fundamental frequency, their phase components cancel each other so only AM noise is produced. However, AM noise is converted into PM

noise through the mechanisms mentioned in the previous subsection (called indirect FM). Secondly, the high frequency noise around $2\omega_o+\omega_n$ is downconverted to a single side band, close to oscillation frequency and also is upconverted to $3\omega_o+\omega_n$ where the LC tank bandpass characteristic rejects the noise around 3rd harmonics so only downconversion is considered. As explained in the LTV model of phase, any injected noise in passband is composed of both AM and PM components. In spite of the fact that AM noise is suppressed in a duty cycle (Fig. 3.9), it is again indirectly converted to PM noise via the nonlinear devices in the feedback loop. In order to reduce the flicker noise of the bias transistor, its dimension must be increased while keeping the W/L ratio equal. In this case, the bandwidth of the bias transistor also reduces, hence, attenuates the high frequency bias noise. If this is not sufficient to block high frequency noise around second harmonic, a shunt capacitor can be connected to bias transistor so that it creates a low impedance path at $2\omega_o$. However, in the presence of a bottom biasing transistor, this can cause the switching transistor exhibit low impedance to the tank, therefore this loads the resonator and degrades the quality factor of the tank. As a solution to this issue, an inductor can be connected to between switching pair and bias transistor, providing high impedance on this path.

3.4.1.4 Noise in the Switching Pair

The noise in the switching pair can be modeled as depicted in Fig 3.21. At low frequencies where the flicker noise is the dominant contributor of the transistor noise, low impedance is seen from the drain terminal through inductor. Assuming this impedance as short, the flicker noise current source of the switching transistors can be placed in parallel with the bias noise current source [11]. The same upconversion mechanism accounts for the switching transistors. Here, the point must not be overlooked is that the upconversion mechanism of the flicker noise of all transistors in the circuit depends on the linearity of the switching transistor so reducing the width of the switching transistors is a good option, this will, however, leads to a higher 1/f noise magnitude in the switching pair. The designer must take into account this trade-off.

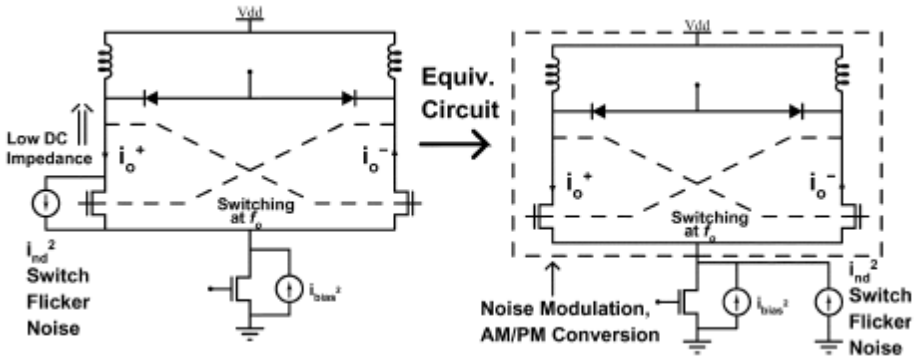


Figure 3.21: Upconversion of flicker noise in switching pair

The main source of the phase noise in $1/f^2$ region is the thermal noise of the switching transistors. As mentioned in section 3.3.3, the main contributor of thermal noise in a MOSFET is the drain current thermal noise which is proportional to the transconductance of the long-channel in saturation so a decrease in transistor width results in a reduction at a rate of square root. However, this case may vary for short-channel devices due to the effects of velocity saturation. As devices are reduced in size, the electric field typically increases and the carriers in the channel have an increased velocity. However at high horizontal fields there is no longer a linear relation between the electric field and the velocity. The velocity gradually saturates until it reaches to the saturation velocity at a critical electric field E_C. When the overdrive voltage approaches the product of LE_C, the equality of the transconductance to the output conductance does not hold, therefore, thermal noise gets proportional to transistor width since $g_{d0} = \mu_{eff} C_{ox}(W/L)(V_{gs} - V_{th})$. Also, the expression for the transconductance equals to $WC_{ox}\upsilon_{sat}$. Consequently, the thermal noise of the short-channel MOSFETs increases more rapidly, however at the same amount of reduction in gm for higher values of the overdrive voltage.

3.4.2 Tank Generated Noise

This subject is discussed in subsection 3.3.1 where all other noise sources in the oscillator are described as a negative resistance thermal noise. These two noise sources are correlated with a parameter of F(Δω) in equation 3.11. If we neglect the noise due to the active negative resistance generator, F(Δω)=1 and we reach the same result that Rael and Abidi obtained for the resonator noise in (3.26). Hence, the noise generated by the loss of passive components in the tank is expressed, similar to (3.16), as

$$L(\omega) = 10log\left(\frac{2kT}{P_{sig}}\left(\frac{1}{2Q}\frac{\omega_o}{\Delta\omega}\right)\right)^2 \quad \textbf{(3.32)}$$

4. IC INDUCTORS

This chapter gives information about two widely used inductor types in RF IC VCO design.

4.1 Bond Wire Inductors

Bond wire inductors are realized by a wire connection between a die and the package. The parasitic inductance of the wire is approximately 1 nH/mm. They have a low series resistance so that high Q inductors (Q>40) can be obtained. Their main superiority is to have a very small die area which is a considerable design constraint of today. However, they have poor tolerance in value (> ± 20%) since it is off-chip.

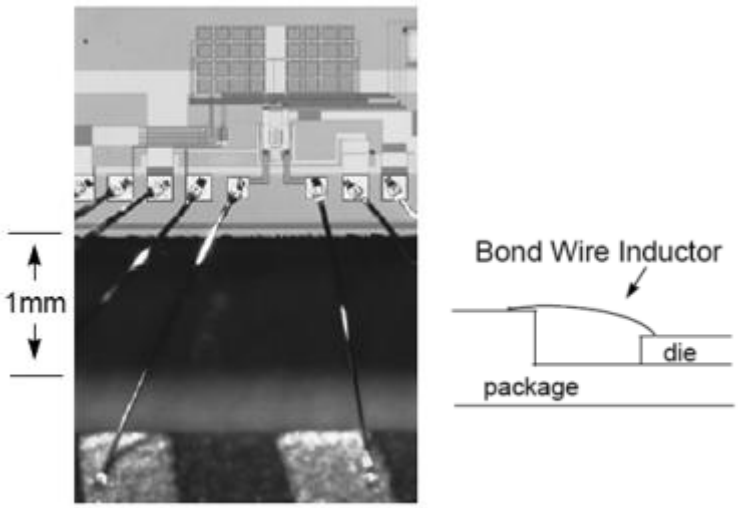


Figure 4.1: Die photo and cross-sectional view of a bond wire inductor

4.2 On-chip Inductors

On-chip inductors are widely used in LC VCO structures although they have lower and moderate Q value (between 4 and 10) than bond wire inductors because they are completely integrated and, especially, have high tolerance (< ± 10%). Their main drawback is that they are bulky and usually occupy more area than the sum of other devices in the layout.

4.2.1 On-chip Inductor Types

On-chip inductors are usually implemented by spiral structures fabricated on top metal layers. Top metals have less resistivity per area so their loss is low, resulting in a higher Q value. As shown in Fig. 4.2, there are several kinds of spiral inductors. The most common topology of an on-chip inductor is the spiral square inductance (Fig. 4.2a). In order to obtain higher Q values, hexagonal and octagonal shaped (Fig. 4.2b) spiral inductors are preferred. However, the designer should also consider the available structures presented by design kit if an inductor CAD program such as ASETEC is not used for inductor design. For instance, UMC 0.18u RF design kit only offers a circular spiral inductor which has almost the same structure in Fig. 4.2c. In Fig. 4.2d,e,f, the fully symmetric inductor is realized by joining coupled microstrips to another with respect to a symmetry axis using a number of cross-over and cross-under connections. When driven differentially, the voltages on adjacent conducting strips have 180° phase difference, however, current flows in the same direction along each adjacent conductor. This reinforces the magnetic field produced by the parallel groups of conductors and increases the overall inductance per unit area [15].

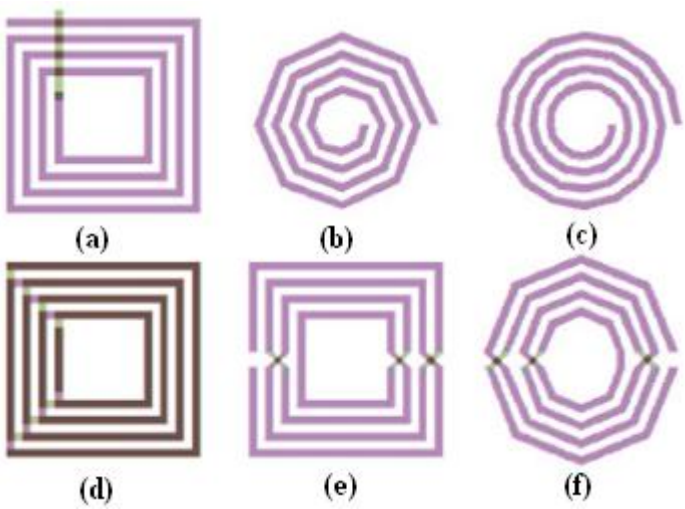


Figure 4.2 Different types of inductors (a) square spiral with cross-under, (b) octagonal spiral, (c) circular spiral, (d) multi-layer series-joined square spiral, (e) symmetric center-tapped square spiral, (f) symmetric center-tapped octagonal spiral.

4.2.2 Modeling of on-chip inductor

The parameters of an inductor are extracted from the physical structure. However, the narrowband model is also useful especially for the easiness of the calculations

4.2.2.1 Physical Model

A spiral inductor which is rich in electromagnetic phenomenon can be modeled by a lumped element model since the geometrical dimensions of these devices are small compared to the wavelength. The simplest model which accurately predicts the behavior of on-chip inductors is shown in Fig. 4.3.

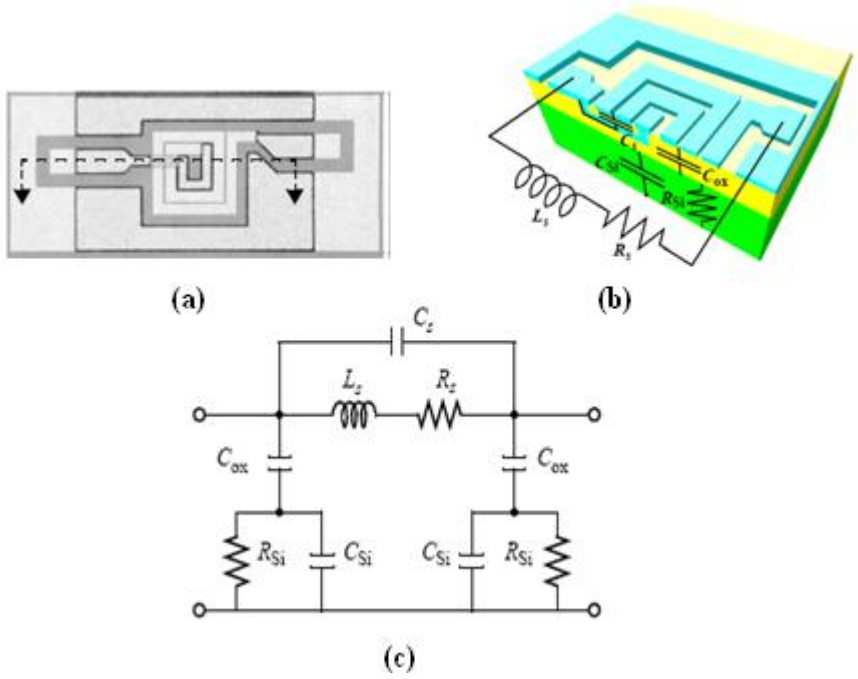


Figure 4.3: (a) Top view, (b) cut-away view, and (c) the physical model of an on-chip spiral inductor

The elements used in this model are described briefly below:

Series Inductance (L_s): The inductance of the spiral and underpass is represented by the series inductance. L_s consists of the self inductance, positive mutual inductance, and negative mutual inductance.

Series Resistance: R_s models the metal resistance loss of spiral turns due to the formation of eddy current. The eddy effect, which Faraday's law leads to is, appears when a conductor is exposed to time-varying electromagnetic fields [16]. Eddy currents manifest themselves as skin and proximity effects [17]. Both effects tend to re-distribute the current and result in a reduction in the effective cross-sectional area through which the current can flow. Thus, R_s will increase as the operating frequency of the inductor increases [18].

Series Capacitance: The series capacitance models the parasitic capacitive coupling of two ports of the inductor. There are two reasons generating this capacitance; the

crosstalk between adjacent turns and the overlap capacitance between the spiral and underpass. The crosstalk capacitance can be reduced by increasing the spacing between turns. Moreover, since the adjacent turns are almost equipotential, the effect of the crosstalk capacitance can be neglected [17]. The effect of overlap capacitance is more significant because of the larger potential difference between the spiral and the underpass [19].

Substrate Parasitics: The effect of substrate on MOS structures is generally modeled by a three-element network comprised of C_{ox}, R_{si} and C_{si} . C_{ox} represents the oxide capacitance. R_{si}, the substrate resistance, models the effect of the silicon conductivity which is predominately determined by the majority carrier concentration. C_{si}, the substrate capacitance, characterizes the high-frequency capacitive effects occurring in the semiconductor.

4.2.2.2 Narrowband Inductance Model

Physical lumped model can be translated to a narrowband model by series to parallel and parallel to series conversions respectively. The new model is essential for the easiness of calculations. The circled sub-circuits in Fig. 4.4 are equivalent to each other at the oscillation frequency of the VCO.

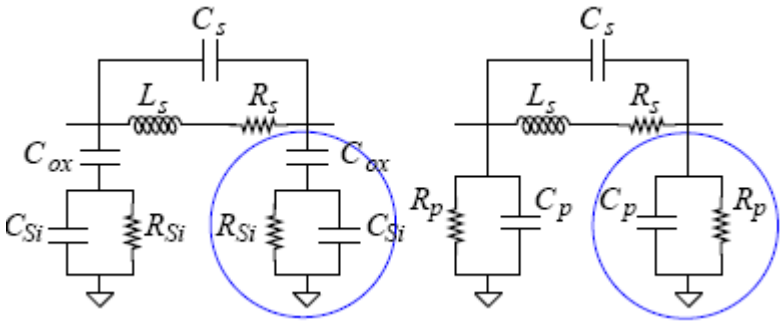


Figure 4.4: Physical model of an on-chip spiral inductor and its parallel equivalent network

The equations for conversion are expressed below:

$$C_{p_{1,2}} = C_{ox}\frac{1+\omega^2 R_{si_{1,2}}^2 C_{si_{1,2}}\left(C_{si_{1,2}}+C_{ox_{1,2}}\right)}{1+\left(\omega R_{si_{1,2}}\left(C_{si_{1,2}}+C_{ox_{1,2}}\right)\right)^2} \quad \textbf{(4.1)}$$

$$R_{p_{1,2}} = \frac{1+\omega^2 R_{si_{1,2}}\left(C_{si_{1,2}}+C_{ox_{1,2}}\right)}{\omega^2 R_{si_{1,2}}^2 C_{ox_{1,2}}^2} \quad \textbf{(4.2)}$$

After connecting one port to ground we can derive an expression of the conductance loss of the inductor:

$$g_L = \frac{R_s}{(\omega L)^2} + \frac{1}{R_{p_{1,2}}} \quad \textbf{(4.3)}$$

If the left (right) port is grounded, $R_{p1,2}$ is equal to R_{p2} (R_{p1}). The quality factor of the inductor can be modeled as

$$Q_L = \frac{|B_p|}{G_p} = \frac{1/g_L}{\omega L} \quad \textbf{(4.4)}$$

It is possible to increase the quality factor of an inductor by driving differently. In this case, the conductance of the inductor reduces since $R_{p1,2}$ is now equal to (R_{p1}+R_{p2}).

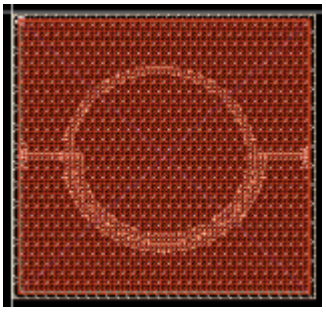


Figure 4.5: Layout of inductor in UMC 0.18u design kit

The inductor in the design kit of UMC 0.18u technology is determined by three parameters: width, diameter and number of turns…The minimum realizable inductor is 0.6nH with a diameter of 136um and a turn number of 1.5. Table 4.1 presents some specifications of several inductor values measured in RF-Spectre at 2.4GHz.

Table 4.1: Specifications of several inductor values at 2.4GHz

Inductance [nH]	Quality Factor	Conductance loss [mS]	Diameter [um]	Number of Turns	Width [um]
3	9.51	2.2	231.72	2.5	19
2.5	9.35	2.7	197.02	2.5	19
2.0	8.78	3.6	161.06	2.5	19
1	6.08	5.0	202.34	1.5	19

5. VARACTORS

Two kinds of varactors: diode and MOS varactors are described in this chapter. The implementation of the switched capacitor arrays as varactors is also explained.

5.1 Diode varactors

A diode varactor is comprised of a reverse- biased p^+ /n junction in an n-well. The capacitance value is controlled by the reverse voltage. The expression below describes the behavior of varactor with respect to control voltage.

$$C_j = A_j \frac{\varepsilon}{x_{dep}} = \frac{C_{j0}}{\left(1 - \frac{V_j}{\varphi_0}\right)^n} \tag{5.1}$$

where φ_o is the junction potential, V_j is the reverse voltage and C_{j0} is the gate capacitance when V_j is zero and n whose value is usually between 0.3 and 0.4 is a fitting parameter depending on doping profile. From the above formula, a positive increment in reverse bias voltage requires an increment of growth of the depletion region width. Since charge must flow to the edge of the depletion region, the structure acts like parallel plate capacitors for small voltage perturbations.

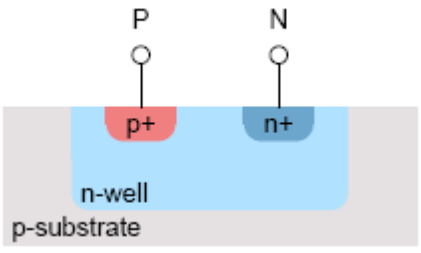


Figure 5.1: Cross-sectional area of a diode varactor

Diode varactors generally are not appropriate for course tuning varactor implementations. As the technology scales down, the maximum supply voltage and, the maximum available control voltage decrease. Typically, the achievable frequency tuning range of tanks, in which diode varactors are used, is less than ±10% of the center value, if a control voltage smaller than 2V is applied. This is, however, not

enough to compensate for the capacitance and inductance variations with respect to their nominal values [20]. Moreover, diode varactors usually have low quality factor; less than 20 [4, 21]. On the contrary, the RF diode varactor in UMC 0.18u tech exhibits a reasonable quality factor value as depicted in Fig 5.2. Hence, diode varactors are only preferable for fine tuning of frequency because of their low gain.

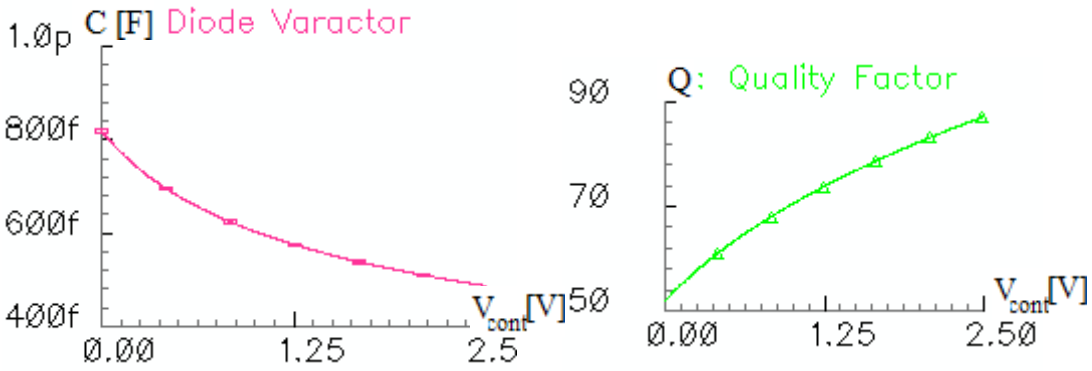


Figure 5.2: Voltage-capacitance characteristics and quality factor of RF diode varactor in UMC 0.18u design library

5.2 MOS Varactors

5.2.1 General Concept of MOS Varactors

A MOS varactor can easily be implemented by connecting drain, source, and bulk terminals (D=S=B) together. The capacitance value of this structure depends on the voltage between gate and bulk nodes.

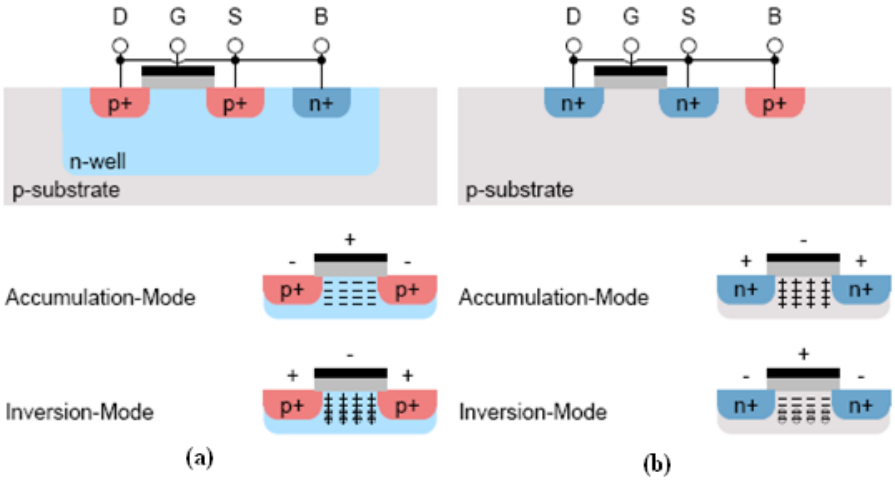


Figure 5.3: Cross-sections and definitions of accumulation and inversion mode of (a) PMOS and (b) NMOS varactor

This structure, shown in the previous page, forms 5 different operating regions. An example of this MOS varactor type is simulated using a standard 1.8V NMOS transistor from UMC 0.18u design kit. A port applying 0.5V AC signal without DC offset to gate terminal is used to run the s-parameter analysis and the bulk voltage is swept from -1.8V to 1.8V. For $V_{bg}<-V_{th}$, the varactor operates in the strong inversion region that capacitor acts as a transistor. On the other hand, for some positive values of bulk to gate voltage, for example more than 0.5V in our analysis, the capacitor operates in the accumulation mode, where the potential at the interface between gate oxide and semiconductor is high enough to allow holes to move freely and to accumulate them under the gate oxide. In both regions, the value of capacitance C_{var} is equal to $C_{ox}=A\varepsilon_{ox}/t_{ox}$ where *A* denotes to the transistor channel area (W·L) and t_{ox} is the oxide thickness. In between these, three more regions are placed on the NMOS capacitance-drain voltage plot; the weak and the moderate inversions, and the depletion region. In these regions the number of holes under the gate decreases, thus, causes the capacitance of the MOS to lessen. The varactor capacitance is now approximated to C_{ox} in series with the parallel of capacitances C_b and C_i. The modulation of the depletion region under gate oxide is the origin of C_b and C_i is generated by the variation of the number of holes at the gate oxide interface [22]. The MOS transistor operates at the depletion region if C_b dominates whereas it works at the moderate inversion if C_i outweighs. In the lack of a dominant capacitance, the device employs in the weak inversion region.

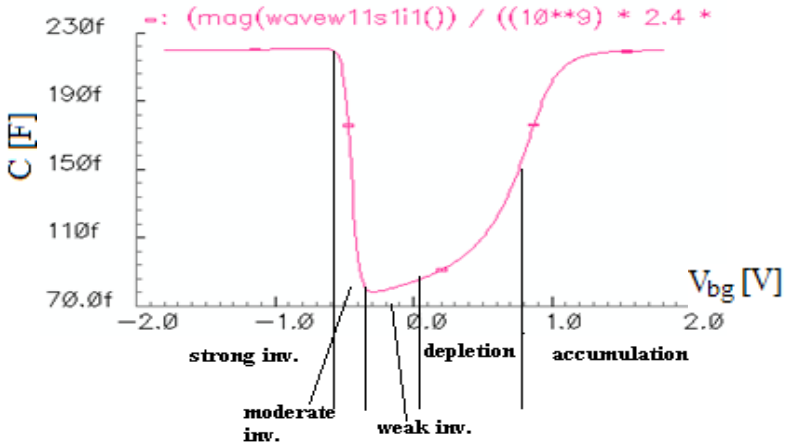


Figure 5.4: Operating modes of NMOS varactor in UMC 0.18u design library

5.2.2 Inversion Mode MOS Varactors

The voltage swing on the gate terminal accounts for the simultaneous variations at the small signal capacitance and if high enough, it brings about the MOS to operate in the accumulation region for some instant while biased in the depletion or strong inversion region and vice versa. Therefore, the dependency of the average value of the MOS varactor to the control voltage degrades. To overcome this, an inversion only mode varactor can be implemented. In the presence of a PMOS transistor, if the bulk is connected to highest possible potential instead of connecting to drain and source terminals, the MOS varactor only operates at inversion mode. In addition, an inversion mode NMOS varactor can also be realized by connecting its bulk to the lowest dc-voltage possible in the circuit. Compared to (D=B=S) MOS varactor, a more monotonic function of C_{var} is obtained since the average value of the MOS varactor over a period is less effected by the voltage swing at the gate terminal. Furthermore, in IMOS varactors, as the voltage swing increases the transition between the depletion and the inversion mode regions gets smoother wheras C_{vmax}/C_{vmin} does not change so the range of the control voltage widens. However, a rise on the voltage swing diminishes C_{vmax}/C_{vmin} ratio in (D=S=B) MOS varactors [21].

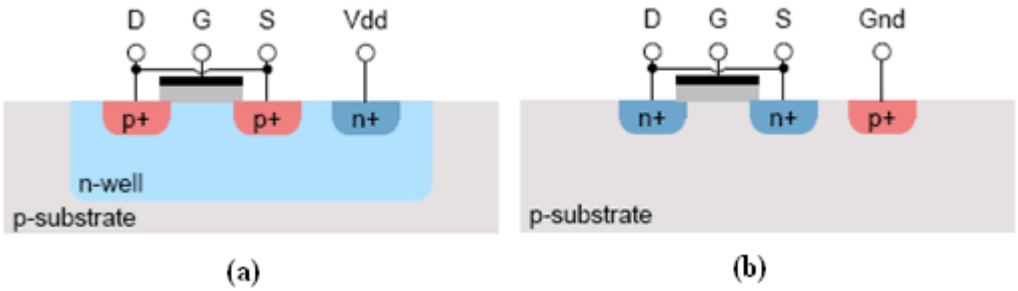


Figure 5.5: Cross-sections of an inversion mode (a) PMOS and (b) NMOS varactor

There exist a trade-off between the quality factor and the ratio C_{vmax}/C_{vmin} of a varactor due to the channel length of the device. The quality factor of an IMOS varactor, defined as $1/R_s\omega C$, enhances with a decreasing length since the less channel length, the less series resistance of capacitor. On the other hand, this leads to a decrease in C_{vmax}/C_{vmin} because this ratio is directly proportional to channel length. A low quality factor of the varactor can degrade the quality factor of the tank resulting in a worse phase noise performance whereas a smaller C_{vmax}/C_{vmin} means a lower tuning range. An s-parameter analysis is run by keeping the product of WL equal for

different transistor dimensions. The result shown in Fig. 5.7 is consistent with the above statement for C_{vmax}/C_{vmin}. Unfortunately, no meaningful value is obtained for quality factor because of the inaccurate modeling of the gate resistance.

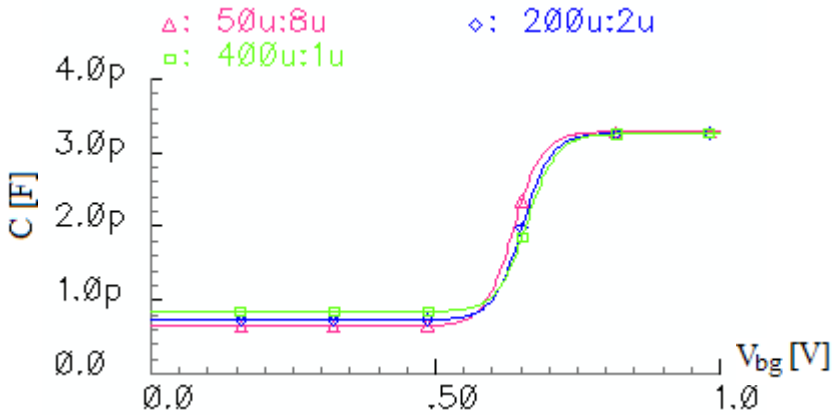


Figure 5.6: Variation of C_{vmax}/C_{vmin} with respect to channel length in IMOS varactors

5.2.3 Accumulation Mode MOS Varactors

An alternative to inversion mode MOS varactor, this varactor type is realized by replacing the D–S diffusions (p^+ -doped) from the PMOS device with the bulk contacts (n^+) as shown in Fig. 5.6. The transistor operates only in the depletion region and accumulation mode. In this physical structure, the parasitic n-well resistance of the device is minimized due to higher mobility of electrons as mobile charge carriers so the quality factor of the varactor will increase. Quality factor of this capacitor type is proportional to L^{-2} when the device is operating in the accumulation region [23], and to L^{-1} in the depletion region [20]. However, this type of MOS varactor does not exist in UMC 0.18u library.

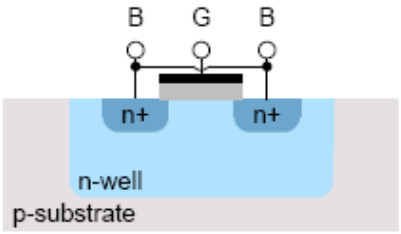


Figure 5.7: Cross-section of an accumulation mode PMOS varactor

5.3 Switched Capacitor Array Varactor

MOS switch banks can be used as varactors in VCO designs to coarsely or discretely tune the frequency. Fig 5.8 depicts the basic equivalent circuit for the "on" and "off" states of the switch.

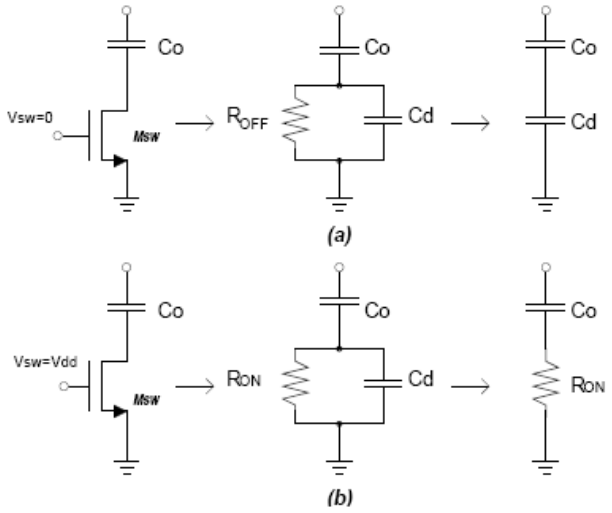


Figure 5.8: NMOS as a RF switch

C_d is the total parasitic capacitance of the switch which is equal to $W_{sw}C_{dd}$ where C_{dd} is the parasitic capacitance per micron and W_{sw} is the width of the MOSFET. During off-state, the quality factor is quite high and proportional to $Wsw/\omega_o C_o$ [24]. However, when the MOSFET is on, the switch-on resistance loads the capacitor and degrades the quality factor which is equal to $1/\omega_o C_o R_{ON}$. Since R_{ON} is inversely proportional to W/L, width of switch must be high enough in order not to degrade the quality factor of the tank. On the other hand, since an increase on the transistor width will add more parasitic off-capacitance C_{dd}, this can cause to limit the tuning range. Consequently, selection of minimum length transistor is better and the widths must be optimized for sufficient tuning range.

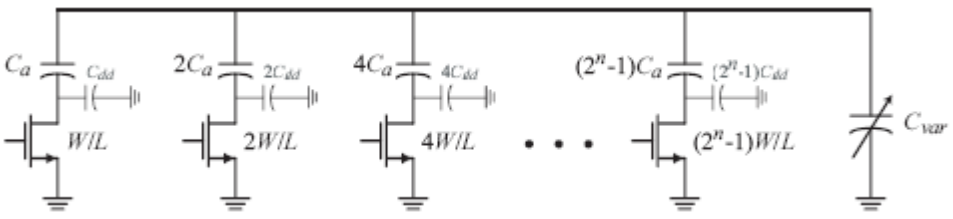


Figure 5.9: Varactor implementation of switched capacitor array

It is also possible to switch two capacitances with only one single transistor in a differential way as shown in Fig 5.10. In this case, the quality factor of the switch increases by a factor of two because only half of the R_{ON} is added to each capacitor when the device is on [24].

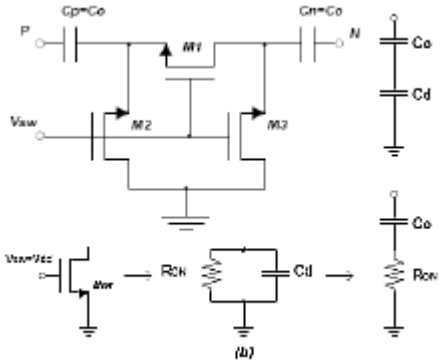


Figure 5.10: Differential Switch

The bottom transistors M_2 and M_3 bias the switch in order to guarantee the on-state of the structure. Since there is no dc current through these NMOS transistors, so, they do not add significant noise to the circuit [25]. Their dimensions must be kept minimum sized to lower the effect of parasitic capacitances.

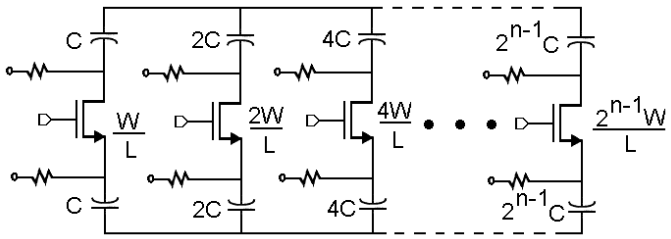


Figure 5.11: Circuit schematic of the differential SCA [26]

6. VCO DESIGN

In this chapter, three basic cross-coupled LC oscillators were compared due to low power consumption. After choosing the most suitable topology, the oscillator was optimized by minimizing the effect of the phase noise generating mechanisms to achieve a high figure of merit circuit. In addition to this, several LC voltage controlled oscillators based on cross-coupled topology were designed in order to lower the power consumption as well as to satisfy the phase noise specification. To make a fair comparison, in most cases, their bias current was kept the same. In the last part of the design section, three differential Colpitts structure were targeted to design with respect to the same current.

6.1 Comparison of Three Cross-coupled Topologies

The widely used cross-coupled LC topology is selected and as a starting point to VCO design, three versions of this topology: NMOS, PMOS and CMOS cross-coupled LC VCOs are compared due to the phase noise specification.

6.1.1 A Simple Comparison

The main target of this study is to make a fair comparison among three topologies by supplying equal power and using the same inductor of UMC 0.18u library. The inductor has a value of 2nH and its quality factor is around 8.8 at 2.4GHz. The conductance loss of the inductor is 3.6mS. The supply voltage is set to 2V. An ideal current source, whose value is chosen 2.5mA in order to guarantee that all circuits are operating in current- limited regime, is used. As mentioned earlier, the CMOS cross-coupled topology has twice greater output swing so if the current-limited regime is provided in this topology, other topologies will be assured to work in this regime since equal current and inductor values are accommodated. Remembering that the output voltage swing for the CMOS cross-coupled topology is a function of the bias current and the loss of inductor, and it is expressed as $4I_{bias}/\pi g_{l;}$ sufficient output voltage headroom is derived in most part of the simulations except high W/L

ratios. The active devices used for three topologies are the standard 1.8V PMOS and NMOS transistors in the design kit. This voltage value indicates that for the MOS transistor $|V_{DS}|$, $|V_{GS}|$ and $|V_{BS}|$ voltages should not exceed 1.8 with a 10% tolerance. An ideal capacitor is used and its value is calculated to make all circuits oscillate at around 2.4GHz. For the easiness of comparison, it is kept constant. To start-up oscillation, an initial condition of 1V is assigned to ideal capacitors. In CMOS cross-coupled topology, the transconductances of NMOS and PMOS transistors are kept the same. For the applied 2.5mA current, the best ratio around 2.6 is obtained after simulating the transistors in DC analysis by sweeping their widths. Equal g_m leads to lower phase noise since more symmetrical waveform is acquired. Fig. 6.1 shows the schematics of three topologies. The method of the comparison is based on sweeping widths and lengths of the transistors in parametric PSS analysis and plotting their phase noise spectrums for some offsets via phase noise analysis.

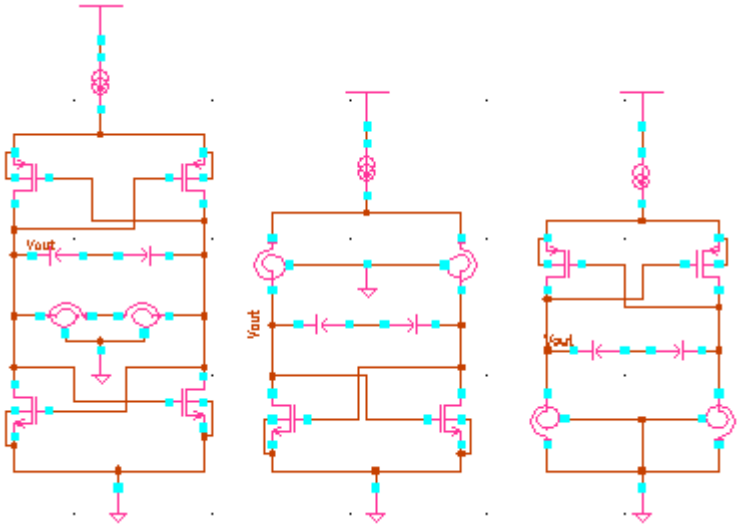


Figure 6.1: Schematics of three cross-coupled topologies

However, there exist some drawbacks in this comparison. First, the usage of ideal current source leads to error. The transistors on both sides always try to flow half amount of the bias current. For some cases, this may cause a negative voltage drop on bias current source. For instance, in CMOS cross-coupled topology if the W/L ratio is low enough, the transistor gate to source voltage will be able to have a greater value than $V_{DD}/2$. In reality, the designer must consider the voltage headroom of the bias transistor. Moreover, the noise coming from the bias circuitry must be taken into account; this is the main disadvantage of this comparison method. Second, the

oscillation start-up condition disagrees in practice and in simulation. In simulation, the oscillation starts at a less loop gain compared to a practical design. Therefore, higher points where the oscillation starts must be considered. Third case is the use of an ideal and constant capacitance. The ideal capacitance is lossless and has an infinite quality factor, but in practice especially if a varactor is used, the quality factor may be less enough, that cause the quality factor of the tank to decrease. However, this can be negligible since all topologies will suffer at the same amount. Moreover, since dimensions of the transistors are swept, their total intrinsic parasitic capacitance changes, therefore, the oscillation frequency shifts. Especially in CMOS and PMOS cross-coupled topologies, the frequency can vary remarkably because of the low mobility of PMOS transistors. Recalling the Leeson's phase noise formula, as the frequency increases, the phase noise of the circuit rises.

Despite these drawbacks, this comparison is able to give a rough insight on the phase noise performance of three topologies. After PSS analysis, the phase noise results are depicted in Fig. 6.2 and Fig 6.3 for 50 kHz and 1 MHz offset frequencies, respectively. It is observed that the graphs are too complicated to reveal brief comments on phase noise performance.

However, a simple comparison of three topologies considering the W_p/W_n ratio and start-up condition can be done. The dimensions of NMOS transistor giving a small-signal gain of two for NMOS topology is 25/0.18. Choosing its length as 0.24um, its width gets the value of 32um. For PMOS structure, the size of the PMOS transistors corresponds to 94um/0.24um and the dimension of NMOS in CMOS topology reduces to a value of 25um/0.24um. From these reference points at a cost of a small oscillation frequency shift but at the same loop gain, for low offset frequencies, PMOS achieves the best phase noise performance and NMOS topology exhibits the worst. This rank is not surprising since high transistor widths leads to low flicker noise. At 1MHz offset, CMOS cross-coupled topology achieves the best phase noise performance, the other topologies has likely phase noise spectrum and approximately 4dBc/Hz above from CMOS pair. The reason is that at high offsets the effect of flicker noise upconversion reduces and the dominant region is mostly $1/f^2$ region. All in all, the results of the comparison reveal that a more complicated and realistic circuit implementation is needed especially for low offsets.

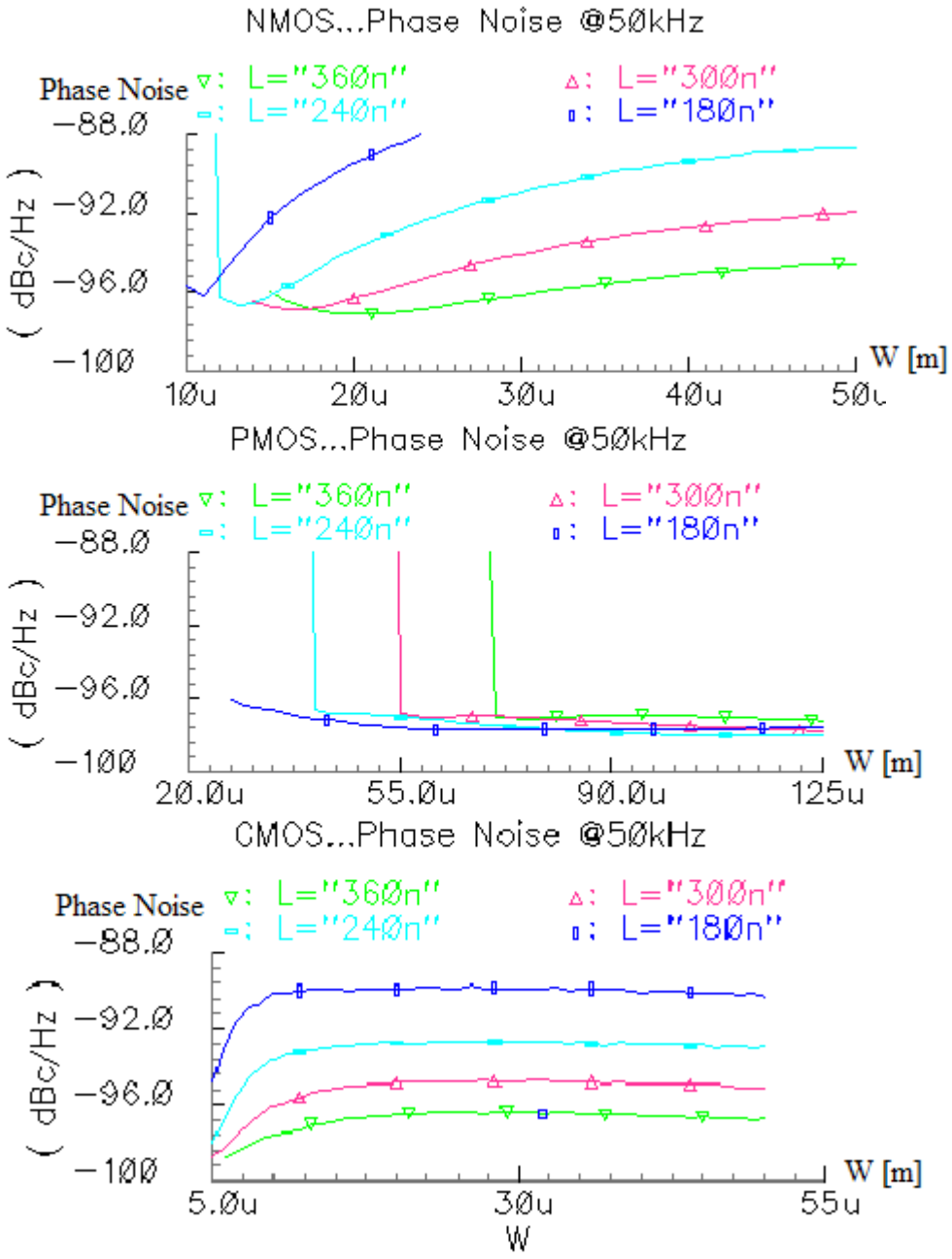


Figure 6.2: Phase Noises of three topologies at 50kHz offset

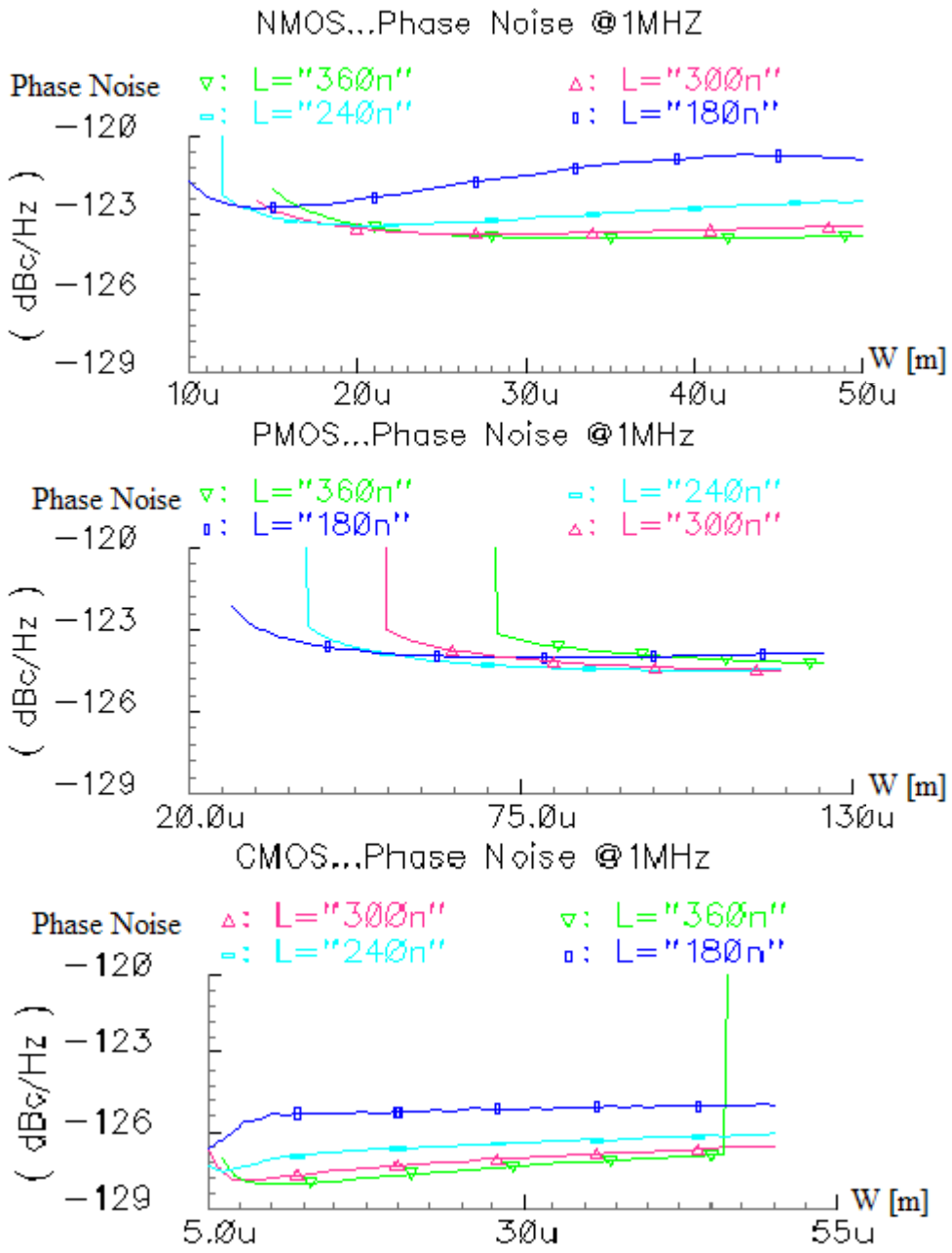


Figure 6.3: Phase Noises of three topologies at 1 MHz offset

6.1.2 A More Detailed Comparative Study

6.1.2.1 Design Methodology

Different versions of three cross-coupled LC VCO topologies are designed. In all simulations, at least 400mV output swing is achieved by an equal bias current around 2mA and a constant inductor providing equal conductance loss used in the previous comparison. The power supply voltage is set to 1.5V. The phase noise characteristics are obtained using an ideal capacitor pair which determines the oscillation frequency at 2.45GHz for all oscillator circuits in this section. The minimum transistor width

providing sufficient small signal loop gain which is at least two in most cases is chosen. The minimum length is preferred for switching transistors to reduce parasitic capacitances and to see the potential tuning range of all oscillators. The reference transistor in the bias circuitry is designed to have a very low overdrive voltage because of the low supply voltage and 0.5 mA current. The mirror ratio is selected 4 for better matching.

6.1.2.2 CMOS Cross-Coupled LC VCO

As a starting point, the CMOS cross-coupled LC oscillator with NMOS bias circuitry depicted in Fig. 6.4 is designed. For a supply voltage of 1.5V, if W/L ratios of the switching transistors are assigned to meet the minimum loop gain value of 2, their gate to source voltage attains a high value so the voltage headroom of the bias transistor is dropped off, therefore, this situation prevents the current of 2mA to flow. Here, the V_{gs} of the bias transistor is around 0.58V and it demands a V_{ds} value of at least 400mV.

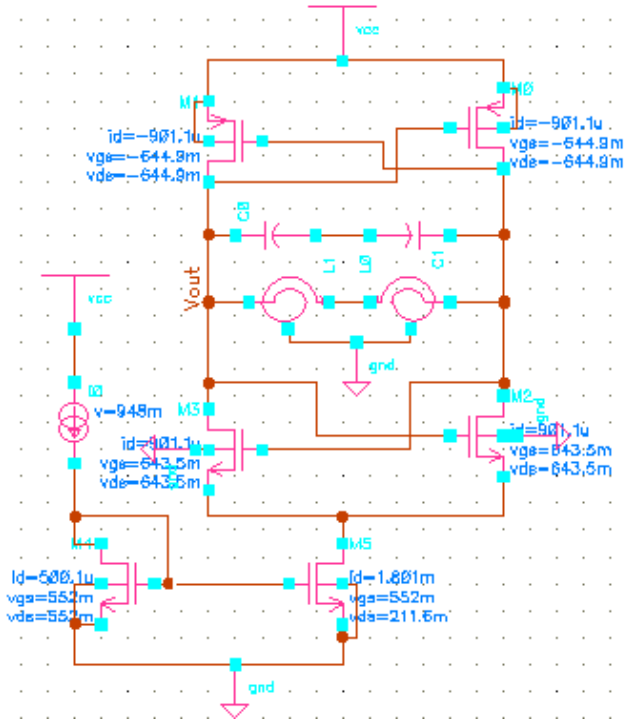


Figure 6.4: CMOS cross-coupled LC oscillator with NMOS bias circuitry

There are two possibilities to cope with this situation. Firstly, W/L ratio of the switching pair can be rise up. This will relax the voltage drop on the bias transistor and let it flow the current with respect to reference current since V_{gs} of the switching

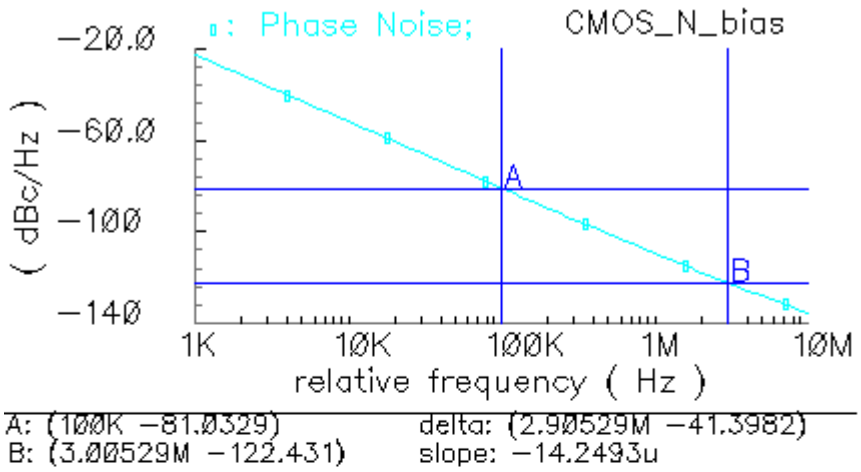
pair reduces. However, the parasitic capacitances also increase resulting in a narrower tuning range. Secondly, the supply voltage may be increased so the voltage drop on the bias transistor again can allow this current amount. Only the former solution is implemented since equal power consumption is targeted in comparison. The widths of the minimum length NMOS and PMOS transistors are increased to more than 100um and 2.7x100um respectively, but since the threshold voltage of the transistors are around 500mV, sufficient overdrive voltage on the bias transistor cannot be obtained. Consequently, for these values of supply voltage and bias current it is impossible to pull that amount of current from bias circuitry in CMOS topology.

Table 6.1: CMOS Cross-Coupled LC Oscillator device dimensions

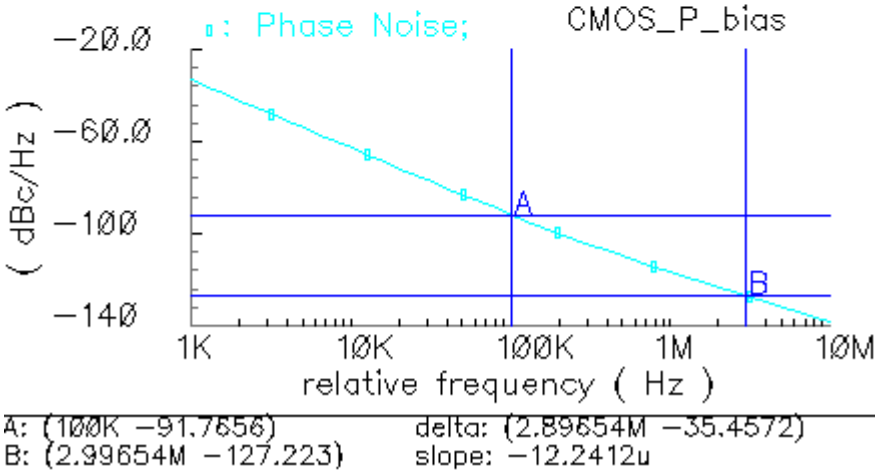
CMOS Topology	PMOS			NMOS			Ref. current		Cap.
	W[m]	L[m]	NF	W[m]	L[m]	NF	W[m]	L[m]	[F]
NMOS bias	130u	0.18u	29	45u	0.18u	10	100u	0.5u	0.49p
PMOS bias	130u	0.18u	29	45u	0.18u	10	200u	0.5u	0.49p
Self bias	54u	0.18u	15	17u	0.18u	5	-	-	1.58p

Nevertheless, a simulation of the circuit with NMOS/PMOS widths of 45um/130um is run and also keeping the same dimensions of the switching pair a PMOS bias circuitry version of this topology is designed. The bias values of all transistors are given in Fig. 6.1 for the NMOS bias circuitry. Although the bias transistor operates in saturation region, it suffers from low drain to source voltage drop, therefore flows around 1.8mA that is less than expected.

Since transistor dimensions are quite large as mentioned in Table 6.1, their parasitic capacitances composes the dominant part of overall capacitor and a low value of tank capacitor around 0.49pF ensures the oscillation at the frequency of interest. Consequently, the tuning range specification cannot be met for current source biased CMOS VCOs.



(a)



(b)

Figure 6.5: Phase noise spectrum of CMOS topology with (a) NMOS and (b) PMOS bias circuitry

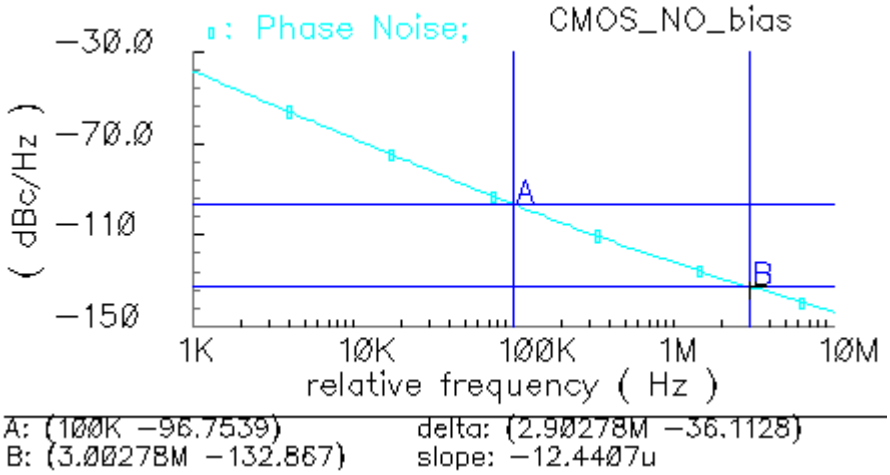


Figure 6.6: Phase noise spectrum of self biased CMOS topology

In order to deal with narrow tuning range and constraint on bias condition, a self biasing CMOS cross-coupled topology can be preferred. By sweeping the width of the transistors, an appropriate W/L ratio enabling a current flow of 2 mA is acquired. For these transistor dimensions, the loop gain is around three.

6.1.2.3 NMOS Cross-Coupled LC VCO

Two NMOS cross-coupled oscillators are designed with bottom and top bias. The dimensions are given at Table 6.2. Since the biasing condition is relaxed in this topology, the dimensions of the bias transistors are reduced by a factor of 0.5 and also constant capacitor is increased to make the circuit to oscillate at the center frequency.

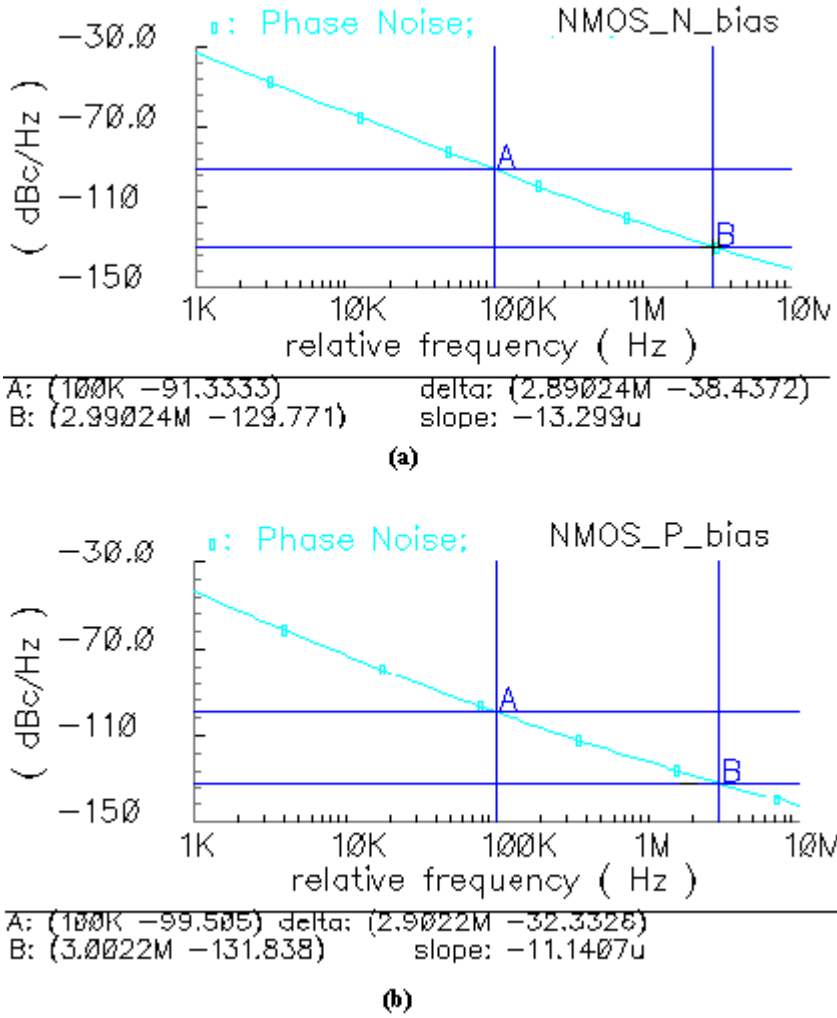


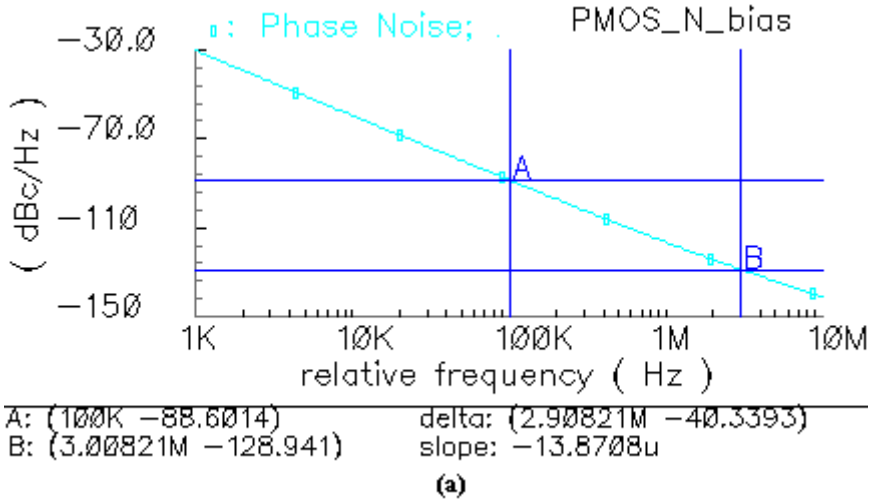
Figure 6.7: Phase noise spectrum of NMOS topology with (a) NMOS and (b) PMOS bias circuitry

Table 6.2: NMOS Cross-Coupled LC Oscillator device dimensions

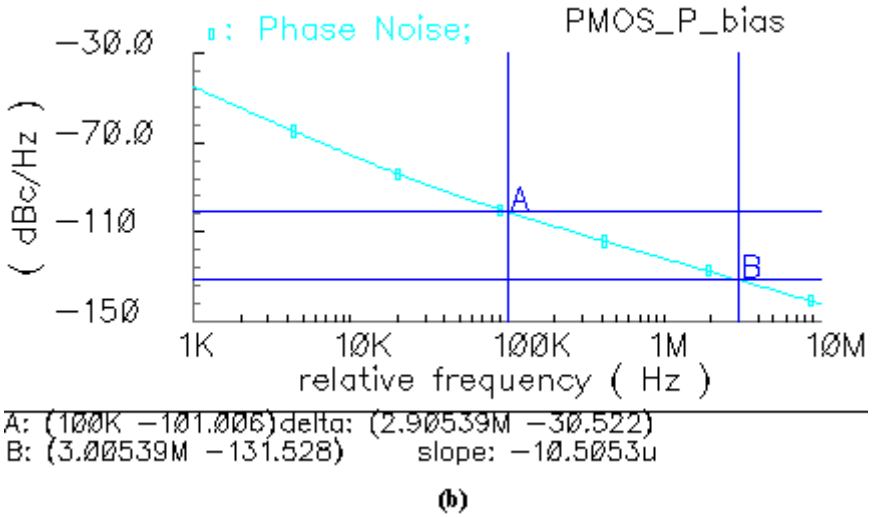
NMOS Topology	NMOS			Ref. current		Cap.
	W[m]	L[m]	NF	W[m]	L[m]	[F]
NMOS bias	25u	0.18u	10	50u	500n	1.96p
PMOS bias	25u	0.18u	10	100u	500n	1.96p

6.1.2.4 PMOS Cross-Coupled LC VCO

Similarly to the previous subsection, PMOS topology is implemented by using NMOS or PMOS transistors in bias circuitry. Table 6.3 shows the dimensions of all transistors used in circuits and phase noise spectrums are depicted in Fig. 6.8.



(a)



(b)

Figure 6.8: Phase noise spectrum of PMOS topology with (a) NMOS and (b) PMOS bias circuitry

Table 6.3: PMOS cross-coupled LC oscillator device dimensions

PMOS Topology	PMOS			Ref. current		Cap.
	W[m]	L[m]	NF	W[m]	L[m]	[F]
NMOS bias	67u	0.18u	10	50u	500n	1.82p
PMOS bias	67u	0.18u	10	100u	500n	1.82p

6.1.3 On the selection of the convenient topology

Firstly, in general, CMOS topology exhibits best noise performance among three topologies [27]. However, in our comparison the limitation on the supply voltage caused it to present the worst phase noise values at all offsets. In this topology, to overcome the biasing constraint, the overdrive voltage of the transistors is reduced by increasing their W/L ratio so the transconductance is increased excessively. This leaded to an increment on the thermal noise of the switching pair. Furthermore, the harmonic distortion of the output circuit is increased because of the poor linearity of the switching transistors. Secondly, reducing the gate to source voltage also caused the oscillator to work on the voltage limited regime. For instance, in the top biased topology, the output waveform is clipped by the ground. After eliminating bias transistor, the phase noise is improved and achieves the best phase noise performance at high offsets and a close performance at low offsets, but this circuit is more sensitive to PVT variations than other circuits employed with a bias current and also it is not suitable for lower voltage applications

Table 6.4: Performance comparison of all designed circuits in this section

Topology	Phase Noise [dBc/Hz] @100kHz	@3MHz	Power Consumption Vdd	Ibias
CMOS_Nbias	-81	-122.4	1.5V	1.8mA
CMOS_Pbias	91.8	-127.2	1.5V	1.84mA
CMOS_NO_bias	-96.7	-132.8	1.5V	2mA
NMOS_Nbias	-91.3	-129.7	1.5V	2.04mA
NMOS_Pbias	-99.5	-131.8	1.5V	2mA
PMOS_Nbias	-88.6	-128.9	1.5V	2.05mA
PMOS_P bias	-101.0	-131.5	1.5V	2.00mA

Secondly, in all topologies, the circuits with the bias circuitry in which PMOS transistors are employed have lower phase noise values compared to their bottom biased counterparts. At 100kHz offset, the improvement is around 10dBc/Hz. This

enhancement reduces but still continues at high offsets. Although PMOS bias transistor has twice value in width than NMOS bias transistor, this phase improvement is high enough not to be related to this difference. Hence, we can mention that in UMC 0.18u library PMOS transistor has less flicker noise than its complementary. It is preferable to select top-biasing circuitry in oscillator design.

Thirdly, comparing two single cross-coupled oscillators equipped with PMOS bias transistor, PMOS cross-coupled topology attains a slightly better phase noise at low offset whereas two topologies have almost the same performance at high offsets.

All in all, the most worthy circuit is the PMOS cross-coupled topology with PMOS bias circuitry. However, in this case the output transistor is biased at ground node and it gets very susceptible to variations on ground. If we consider that in a transceiver architecture PLL works with digital circuits such as baseband signal processors on the same substrate, the performance of this circuit is tend to degrade in practice. The top-biased oscillator is more immune to substrate noise because the current source is placed in an n-well, rather than in the substrate [28]. Therefore, NMOS cross-coupled topology with PMOS bias circuitry is picked out.

6.2 Design of the Chosen Topology

The simulation results in the previous subsection clarify that the phase noise specification is easily met for a power consumption of 3mW so firstly the current is reduced to 1.2mA and the power supply voltage is set to 1.4V which achieves enough overdrive voltage with a reasonable dimension for PMOS bias transistor and sufficient gate to source voltage in the switching pair to have a small-signal loop gain of two. Secondly, digitally controlled coarse tuning MOS capacitors are added and a fine tuning diode varactor circuitry is also implemented.

6.2.1 Inductor Selection

The inductor in the UMC 0.18u library is a spiral circular inductor. Firstly, to see the effects of dissymmetry, an s-parameter analysis is run in RF-Spectre by connecting the left side or right side of the inductor to the ground with the aid of the assumption that the midpoint of two inductors in series is AC grounded. Additional to this, a Matlab code is written in order to verify the results. This code utilizes the physical model parameters obtained from Hspice model datasheet supplied by the

manufacturer and then these parameters are converted to parallel equivalent model parameters. After that, the prominent specifications of an inductor such as quality factor, resistive loss, self resonant frequency with respect to which side is grounded is calculated in this code. One can get all these results only by entering the parameters of the inductor; the width, the diameter and the number of turns, and the operating frequency. The results of the simulation and the calculation are compared in Table 6.5 for the inductor of 2nH at a frequency of 2.4GHz.

Table 6.5: Inductor parameter comparison

Induct [nH][1]	Quality Factor			Inductance Loss [mS]		Self-resonant Frequency [GHz]		Dia-meter [um]	Wid. [um]
	RF Sp.	Matl	max@GHz[2]	RF-Sp.	Matl.	RF-Sp.	Matl.		
2 *(l)*	6.73	7	10,3@6,1	4.74	4.74	21.3	17.1	161.44	10
2 *(l)*	8.11	8.42	10,3@4,7	3.93	3.93	17.6	14.7	162.44	15
2 *(l)*	8.89	9.26	10,5@ 4	3.58	3.58	15.3	13.5	161.06	19
2 *(r)*	8.78	9.19	10@ 4	3.6	3.6	14.5	12.6	161.06	19
2 *(r)*	8.08	8.43	10@4,5	3.93	3.93	16.4	13.8	162.44	15
2 *(r)*	6.75	7.03	10,2@ 5,8	4.71	4.71	19.7	16.2	161.44	10

[1] *(l)* and *(r)* notifications refer to left side grounded and right side grounded, respectively.
[2] max value of inductor is obtained via RF Spectre analysis

The results are perfectly matched for inductance loss. The Matlab code has an error of 4% and around 20% in the cases of quality factor and self resonant frequency calculation, respectively. All in all, the Matlab code is reliable and simplifies the calculations of the determinant parameters of the inductor for the frequency of interest. Up to the value of 4nH, the self-resonant frequency is far enough not to degrade oscillator phase noise performance.

Secondly, several values of the inductor are simulated to see their phase noise performance. The interval where all inductors have a quality factor value of at least 8.8 is kept between 2nH and 3.2nH. In simulations, the purposed topology is kept with the exception of the use of varactors; an ideal capacitor is used instead. The resonant frequency is always set at 2.45GHz. As a result, the best phase noise is achieved when the inductor is 2.5nH. This value also provides enough tuning range which is targeted between 2.2GHz-2.7GHz. This inductor has a loss of 3.2mS at 2.2GHz and 2.2mS at 2.7GHz and has a quality factor of 9.4 at around center frequency.

6.2.2 Bias Circuitry Design

In low voltage design of NMOS-only or PMOS-only cross-coupled LC VCO, the dimension of the reference transistor has an impact on determining supply voltage. The current of the bias transistor depends on its drain to source voltage in saturation, V_{ds} must be kept high enough to flow the demanded amount of current. In general, its value must be close to V_{gs} in bias transistor for UMC 0.18u CMOS technology. For this oscillator topology, V_{ds} of the bias transistor is equal to V_{supply}-(V_{gs}-V_{th}). In our design, the switching pair has a transconductance value of 6.56mS that is around twice greater than the highest value of inductor loss which is 3.2mS at 2.7GHz. Since V_{gs} is around 610mV, the dimension of the reference transistor must be chosen such that its V_{gs} value is around 790mV. This is achieved when W/L=30um/180nm. The trade-off caused by mirror ratio is described as "the higher mirror ratio, the less power consumption and the worse transistor matching…" It is selected to be 4 in order to attain a current of 1.2mA that drives the oscillator where the reference transistor flow 300uA.

After that, keeping the ratios of transistor dimensions and mirror equal, the size of the bias transistors is increased to see their effect on phase noise in Fig 3.3 since one of the main contributor of the phase noise in $1/f^3$ region is the upconvertion of the flicker noise of bias transistors in our topology.

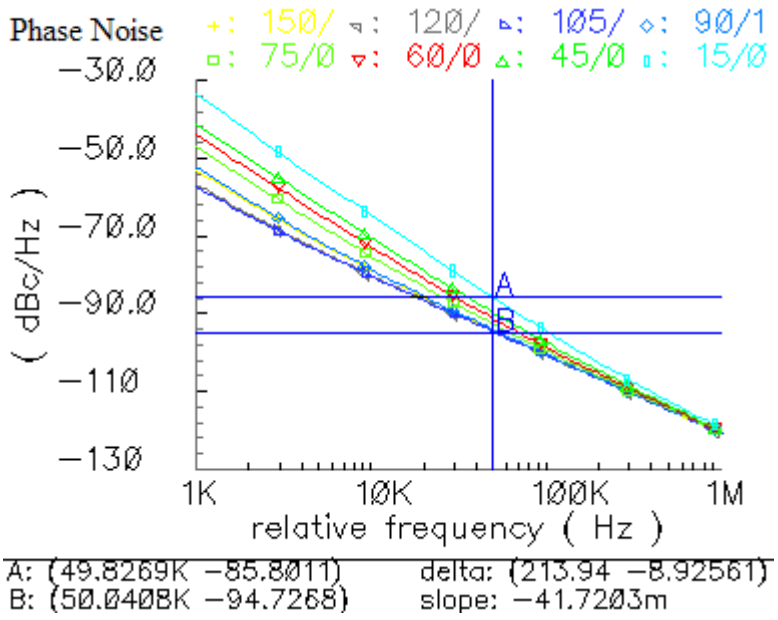


Figure 6.9: Effect of bias transistor dimension on phase noise performance

In $1/f^3$ region, the phase noise decreases as the dimension of the bias transistor increases up to 105um/1.26um. After this point the phase noise starts to rise, one reason of this behavior is the growing thermal noise of the transistor. This optimum value results a 9dBc/Hz improvement at 50kHz offset. For lower offset frequencies, improvement on phase noise increases. For example, the difference is around 17dBc/Hz at 10kHz offset.

6.2.3 Tuning Circuitry Design

In the previous section, the phase noise simulation with a IMOS varactor is also done. It is remarked that the addition of the PMOS varactor instead of an ideal capacitor results the phase noise to increase at least 10dBc/Hz at low and high offset frequencies in all topologies. The main contributor of this rise is the nonlinearity characteristics of the inversion mode PMOS varactor. To reduce this effect, the gain and the nonlinearity of the varactor must be decreased so that AM-PM conversion on the varactor diminishes. For this reason, a 4 bits binary weighted MOS varactor structure is designed for coarse tuning. Firstly, the C_{max}/C_{min} ratio of standard NMOS and PMOS, low-V_{th} NMOS and PMOS and zero-V_{th} NMOS transistors are observed while implemented as varactors. All transistors have the same dimensions.

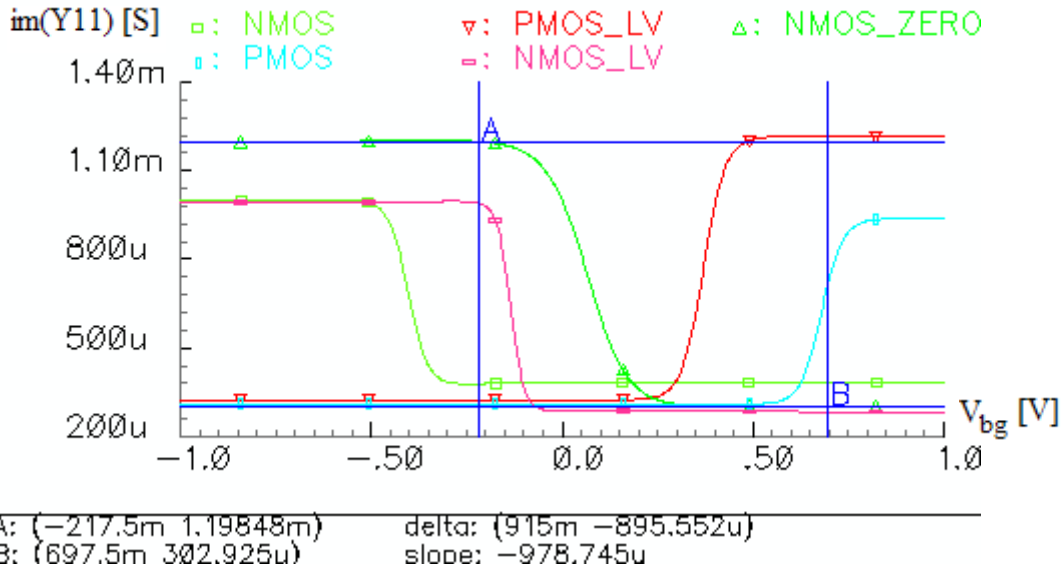


Figure 6.10: Y11 imS: C_{max}/C_{min} ratio of several IMOS varactors in UMC 0.18u library

The highest ratio which is around 4 is attained when NMOS zero-V_{th} transistor is employed and also PMOS low-V_{th} transistor implementation has close varactor gain ratio.

Secondly, one target in the project is the non-use of any external voltages having a different value than the supply voltage except the fine tuning voltage so the digital control voltage value of a bit must be set at the supply voltage and at the ground. To see the characteristics of these five types of coarse tuning implementations, they are simulated in the proposed topology. The output voltage of the oscillator is biased at 460mV and has a peak to peak value of around 500mV. The drain voltage of one MOSCAP is swept while others are biased at a high enough voltage to keep their values constant. The aim of this simulation is to decide which implementation can be chosen with respect to a given bias current in order to guarantee that the MOSCAPs operate at their maxima or minima when the supply voltage or zero voltage (grounding) is applied. The results given at Table 1 shows that zero V_{th} NMOS or low V_{th} PMOS capacitor can be preferred for the supply voltage of our interest with respect to a bias gate voltage of between 400mV-700mV.

Table 6.6: Guaranteed operating points of several MOSCAPs for a 0.5V swing

Transistor Type	Max. lower value	Min. upper value
NMOS	Vg - 0.87 V	Vg - 0.13 V
PMOS	Vg + 0.18 V	Vg + 0.84 V
Low Vth NMOS	Vg - 0.6 V	Vg + 0.14 V
Low Vth PMOS	Vg - 0.32 V	Vg + 0.6 V
Zero Vth NMOS	Vg - 0.5 V	Vg + 0.5 V

However, these results are not definitely accurate for different values of output amplitudes because as the amplitude grows, the characteristic of the varactor widens and gets smoother so in each design, the varactor control voltages must be checked. As seen in Fig. 6.11, the control voltage determination is so severe that an improper value can lead to a significant degradation on phase noise at low offsets.

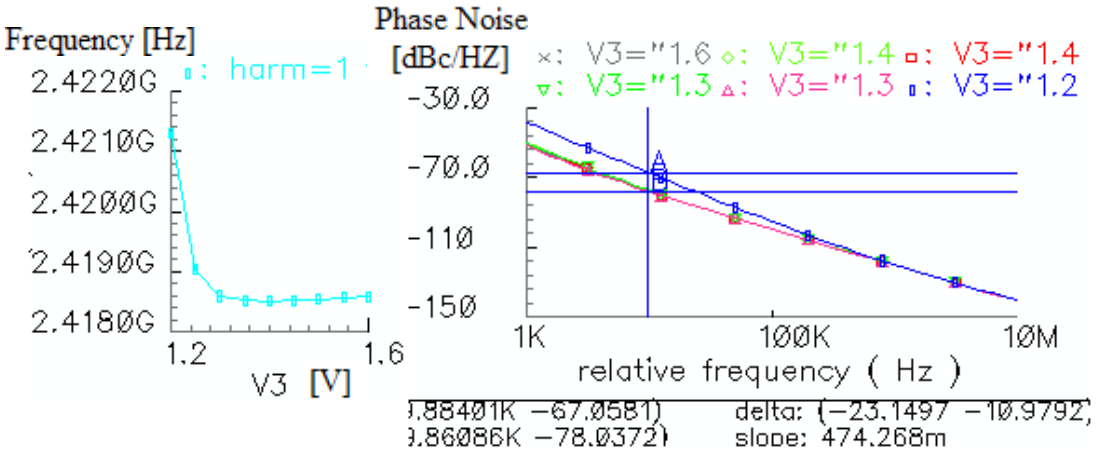


Figure 6.11: Effect of digital control voltage on phase noise performance

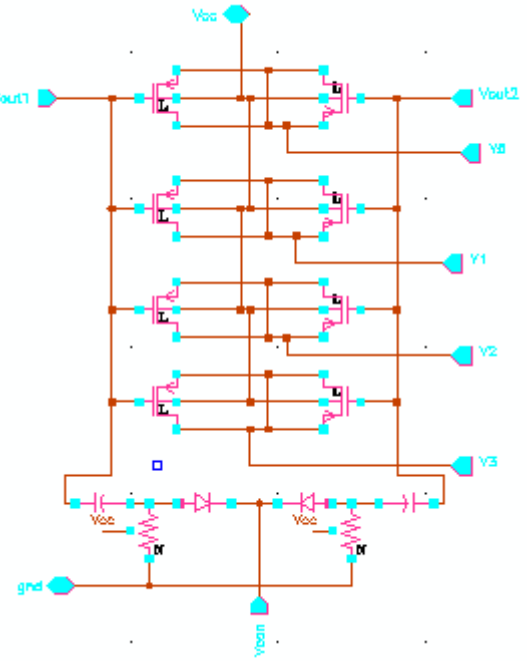


Figure 6.12: Fine and course tuning varactor schematics

After these consequences, two possible transistor types in varactor realization are simulated by increasing the bias current. It is shown that in the presence of a zero-V_{th} NMOS, for higher values than 1.5mA, the "0" state of a bit must be set to a value less than zero voltage or ground to obtain the minimum value of the capacitance. For this reason, PMOS low-V_{th} transistor is the only suitable transistor type in our design. The dimensions of MOSCAP realizing the least significant bit is chosen 17um in width and 400nm in length to satisfy the required tuning range. Also, a RF MIM capacitor is added to varactor circuitry because of the high gain of varactors.

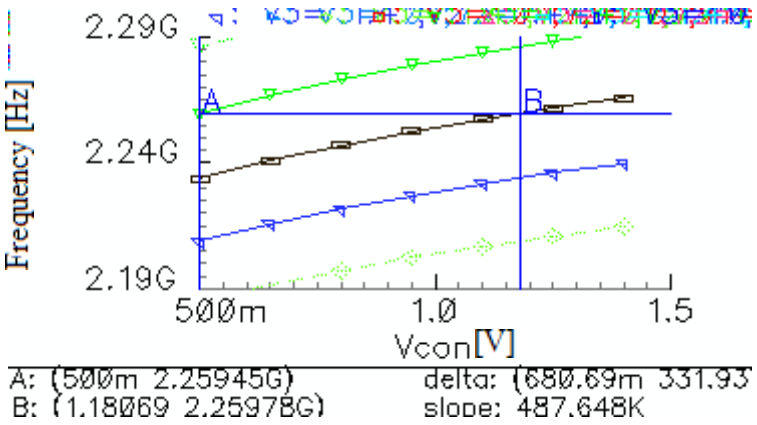


Figure 6.13: Fine tuning: frequency variation with respect to control voltage

The fine tuning of the tank is provided by a diode varactor. Since the consecutive lines on frequency graph must overlap at a sufficient percentage because of PVT variations, the varactor is adjusted to 350fF giving an overlap percent of 33. Additional to this, an RC filter is implemented between the diode and the output nodes. The overall structure is called “capacitor coupled varactor” in literature [29]. This structure filters low frequency components of the output waveforms so the direct FM resulted by the flicker noise of the switching transistors on this path is completely suppressed. Another advantage of this structure is the increased tuning range of the control voltage. It is proposed in the work that the control voltage should not exceed supply voltage except very low supplies. The minimum control voltage is set 0.5V because as the control voltage reduces, the nonlinearity increases; ascribing to more phase noise. The minimum quality factor of the varactor (at 0.5V) is approximately 62. The value of the capacitor is selected high enough (10pF) in order not to degrade the value of the diode varactor and also the resistor value is 40kΩ that does not load the tank since maximum parallel resistance at each branch is less than 350Ω.

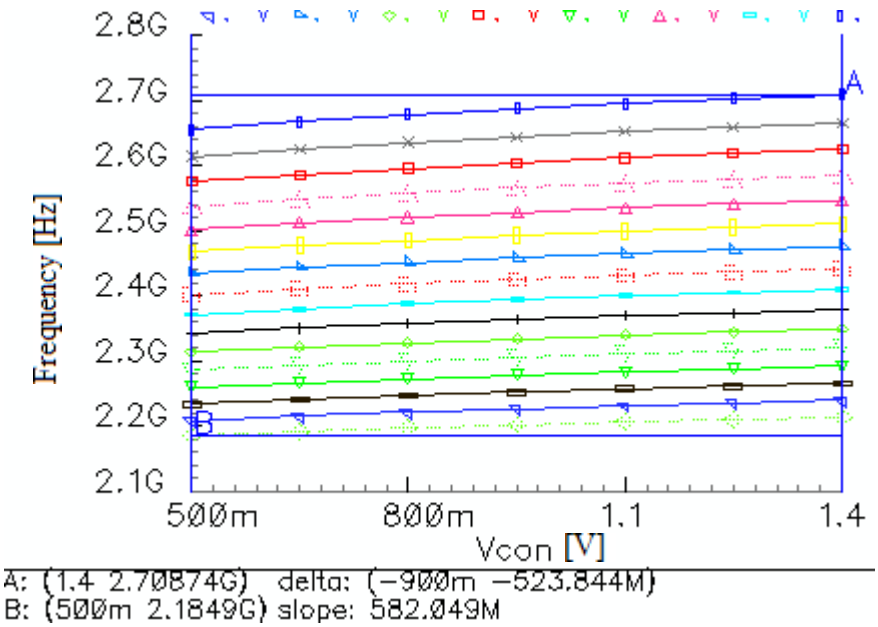


Figure 6.14: Coarse tuning: frequency variation with respect to digital control bits

Hence, the designed oscillator meets all requirements. After that, the bias current optimization is done by sweeping reference current value.

Table 6.7: Phase noise performances vs. bias current

Iref	Ibias	Phase Noise [dBc/Hz] @ 50 kHZ	Phase Noise [dBc/Hz] @ 3 MHZ
275u	1.10m	-87.0 -90.9	-128.3 -129.5
300u	1.20m	-88.1 -92.5	-128.6 -130.3
350u	1.39m	-89.1 -94.4	-128.8 -131.3
400u	1.59m	-89.7 -95.7	-129.0 -131.9
450u	1.79m	-90.0 -96.0	-129.0 -132.2
500u	1.98m	-90.3 -95.5	-129.1 -132.6
550u	2.18m	-89.8 -94.2	-129.1 -132.8
600u	2.37m	-86.1 -91.8	-129.2 -133.0

The phase noise improvement when the current increased to 1.4mA from 1.2mA is relatively higher than other current increments so the final value is determined as 1.4mA. The increased transconductance of the transistor is reduced to $2g_l$ by decreasing the transistor width; this also results a small rise in the linearity of the switching pair. Then, the dimension of the reference transistor in bias circuitry is recalculated and W/L=100um/1um is assigned. After all these modifications, the final simulation is done and the phase noise characteristics and the output waveforms are depicted in Fig 6.15 and Fig 6.16. After the addition of the 4-bits IMOS array, the phase noise at center frequency increases only 2dBc/Hz (Fig. 6.18).

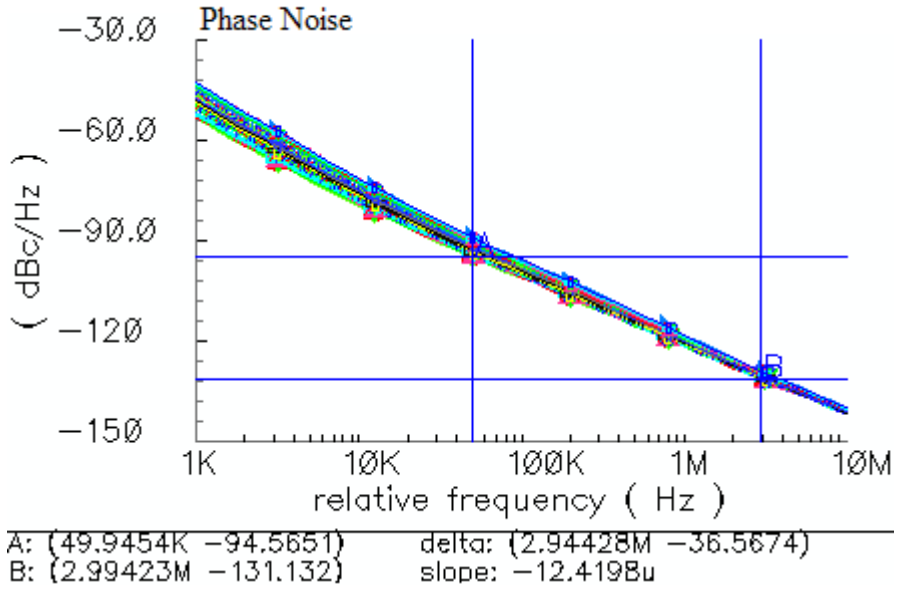


Figure 6.15: Phase noise spectrum of overall frequency tuning range

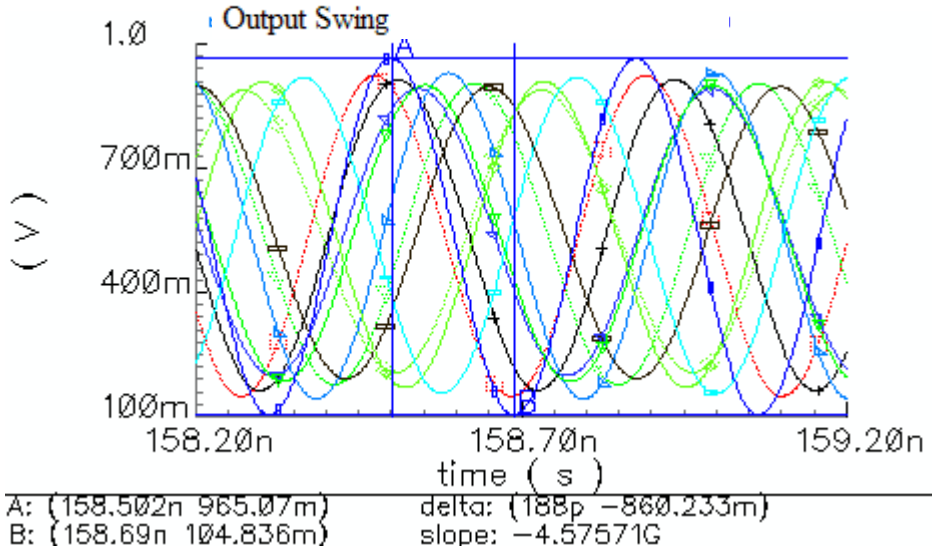


Figure 6.16: Output waveforms from “0000” to “1111” at 0.5V fine tuning voltage

Table 6.8: Phase noise degradation for the worst case

Condition	Phase Noise @ 50 kHz	Phase Noise @ 3 MHz
only ideal cap	-95.3 dBc/Hz	-130.9 dBc/Hz
V_{diode}=0.5V	-92.7 dBc/Hz	-130.1 dBc/Hz
V_{diode}=1.4V	-94.3 dBc/Hz	-130.5 dBc/Hz

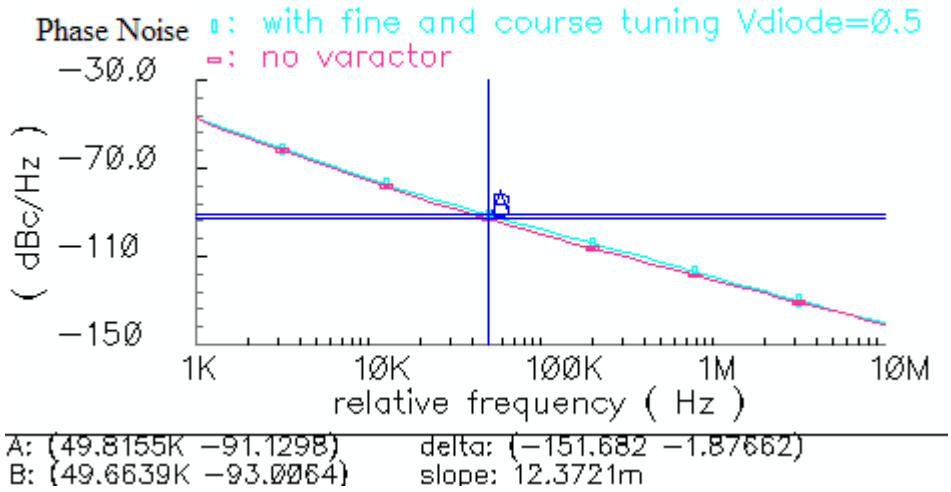


Figure 6.17: Phase noise degradation after the addition of 4bit IPMOS array and diode varactor at 2.45Ghz

6.3 NMOS LC VCO with Resistor Biasing

Firstly, the same VCO designed in the previous section is simulated after replacing the conventional NMOS switching pair transistors with their RF counterparts. This new transistor provided by the design kit have constant length (L=180nm) and width (W=5um). It is only possible to alter the number of fingers from 5 to 21. NF is selected as 5 satisfying the small signal loop gain of two. RF transistor is better modeled at high frequencies and its layout is ready to add including guard rings other protection techniques. For these reasons, after extracted view, the result will probably exhibit less variation in the presence of RF transistors. Therefore, in the following designs mostly these transistors are employed in the switching pair.

An alternative way to bias the oscillator is to employ a resistor instead. It has been shown that the bias noise is an important contributor to phase noise [5, 9]. Also, the upconversion of low frequency bias noise cannot be neglected due to AM-PM conversion [30]. However, it is possible to get rid of flicker bias noise with a resistor. The low thermal noise introduced by a resistance lower than 1,000 Ohms has nearly no influence in the oscillator's spectral purity [31].

The simulation results are depicted in Table 6.9. At low frequency offsets, the best phase noise improvement is only 2dBc/Hz and at 3MHz this reduces to 1.2dBc/Hz. These results reveal that the flicker noise upconversion mechanism is properly designed in the previous section, and it is not necessary to use a resistor in biasing for this low phase noise improvement.

Table 6.9 Comparison of top current source biased and resistor biased NMOS LC VCO

		NMOS			NMOS_RF			NMOS_RF res bias		
Phase Noise [dBc/Hz]	@50kHz	-89.1 -94.9			-88.6 -94.3			-90.6 -94.9		
	@3MHz	-129.0 -131.2			-128.3 -130.5			-129.5 -131.2		
Tuning Range[GHz]		2.19 – 2.71			2.19-2.72			2.19-2.72		
Power Consumption		1.4V*1.4mA								
Bias Circuitry [m]		W	L	ratio	W	L	ratio	W	L	res
		400u	1u	4	400u	1u	4	3.7u	5u	540Ω
Active Device [m]		Wn			Ln			gm		
		25u			180n			6.4mS		
Vamp [V]		bias	min	max	bias	min	max	bias	min	max
		0.64	0.34	0.44	0.64	0.34	0.44	0.64	0.37	0.46
Varactor	Course tuning(LSB)	W			L					
		17um			400nm					
	Fine tuning	NF=30 300fF-350fF								
	Cons.	607fF								
Digital Control		“0”= gnd			“1”=Vdd					
Tuning Voltage		0.5V – 1.4V								

6.4 Implementation of a Filtering Technique [28]

Firstly, as mentioned in subsection 3.4.1.3, only high frequency bias noise around second harmonic directly causes phase noise so the addition of a large shunt capacitor can suppress it by creating a low impedance path to V_{dd} at $2f_o$.

Secondly, in any balanced circuit, odd harmonics circulate in a differential path, while even harmonics flow in a common-mode path, through the resonator capacitance and the switching FETs to ground. In our case, second harmonic is dominant since the noise around it is downconverted to around oscillation frequency whereas other even harmonics are filtered by the resonator. Furthermore, while the switching transistors operate in triode region, the impedance at the source terminal of the switching transistors (in other words, common mode node) degrades abruptly and starts to load the LC tank so the quality factor of the resonator reduces. To overcome these, high impedance at the tail is required at $2f_o$. This can be accomplished by adding an inductor to source node, therefore, it resonates at $2f_o$ with the junction

capacitances of the NMOS pair and total parasitic capacitance of the inductor ($C_{p1,2}$+C_s in Fig. 4.4).

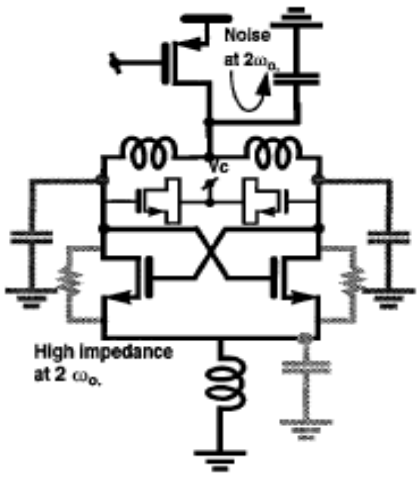


Figure 6.18: Implementation of filtering technique

A shunt capacitor is swept from 1pF to 30pF in PSS and phase noise analyses. The optimum value is found 8pF; however the phase noise is slightly reduced around 0.4dBc/Hz at 50kHz offset and there is no improvement at high offset frequencies. This can be related to the reduced cut-off frequency of the bias transistor. The f_t of a MOSFET is equal to g_m/C_{gs}. In the optimization of flicker noise in the bias transistor in two sections before, the transistor dimension was selected as 400um/1um so the this capacitance is quite high and leads to a value of 2.34pF in saturation and the transconductance of the bias transistor is 7mS with respect to DC analysis results in RF-Spectre so f_t is calculated as 2.9GHz after which the thermal noise of the bias transistor is filtered.

After that, an inductor is placed on the source node of the cross-coupled transistors. Its value is determined after sweeping in the phase noise analysis and selected 4.3nH. This shows that the total parasitic capacitance at source is around 240fF. The calculations in Matlab code show that the total parasitic capacitance of the inductor at 4.9GHz is estimated as 90fF and in DC analysis, RF-Spectre calculates the source junction capacitance of each transistor as 40fF when V_{gd}=0. Taking into account that in triode these capacitances will increase, the chosen value of the inductor is consistent with hand calculations. However, in spite of filtering the noise component from the tail device at twice the oscillation frequency, the inductor acts as a source of wide-band noise, which degrades the overall phase noise by less than 1 dB. The LC

filter is not effective because the time period of the switching pair in triode region is not significant due to low output swing.

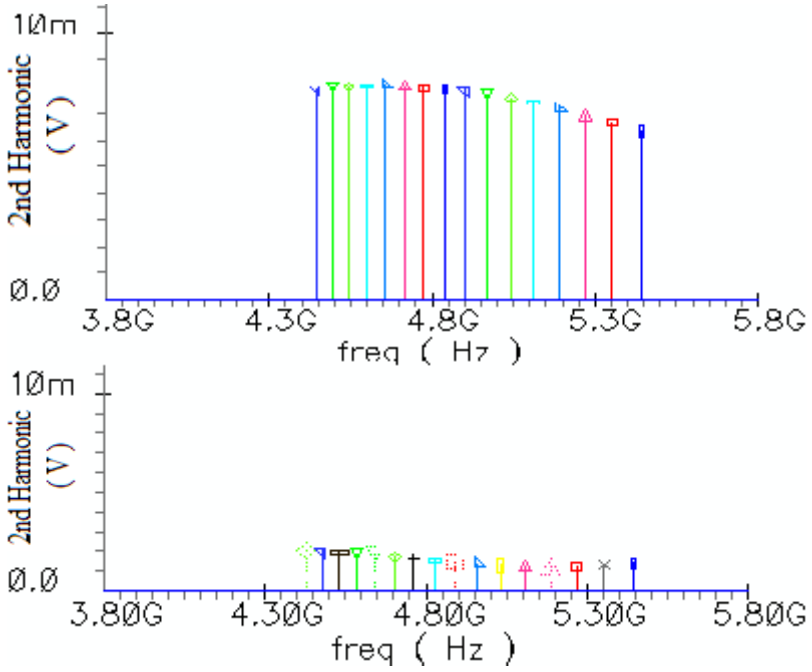


Figure 6.19: Suppression of second harmonic via noise filter

6.5 NMOS LC VCO with Resistive and Inductive Tail Biasing [32]

The overdrive voltage of the bias transistor is a prominent obstacle on low voltage design. To surmount this issue, the usage of a small resistor instead can be a solution if the current is also low. However, in this case, the transconductance of the switching pair reduces due to source degeneration so the start-up condition may not be met. On the other hand, as explained in the previous section, an inductor added in between the transistors and the bias resistor solves this problem. It prevents not only the degradation of the transconductance but also the loading of the resonator.

A supply voltage of 750mV is applied with a resistor of 65Ω to obtain a current of 1.4mA. The switching pair, the tank inductor and the constant capacitor are kept the same. The optimum value of filtering inductor, 2.5nH, is obtained with respect to the phase noise performance. The control voltage of the MOSCAPs which are used in course tuning topology must be greater than the supply voltage for the proper operation so the external voltages are set to 1.6 V.

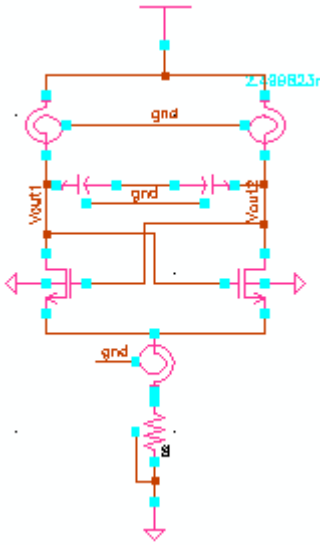


Figure 6.20: Schematics of an NMOS cross-coupled LC VCO with resistive and inductive Tail biasing

This oscillator has two main drawbacks. Firstly, the external voltage values greater than a supply voltage is an unwelcome situation in a PLL. Secondly, in the presence of a small resistor for biasing, the current strictly depends on the value of the resistor. In light of PVT variations, the performance of the circuit can be quite different in practice. For example, the DC bias current can shift at a considerable amount after manufacturing. Moreover, this oscillator is more tend to instantaneous variations on bias current; the phase noise can degrade due to bias current dependency of the oscillation frequency.

Table 6.10: Specifications of NMOS LC VCO with Res. and Ind. Tail Biasing

Phase Noise [dBc/Hz]	@50kHz	-86.7 -94.3		
	@3MHz	-131.0 -132.7		
Tuning Range[GHz]		2.17 – 2.70		
Power Consumption		0.75V*1.4mA		
Vamp [V]		bias	min	max
		0.75	0.40	0.53

It is possible to overcome the first case by designing a SCA varactor structure, however, the latter is a serious concern and it is not effective to go further on the improvements of this design in spite of the fact that a better phase noise can be achieved by proper selection of transistor dimensions.

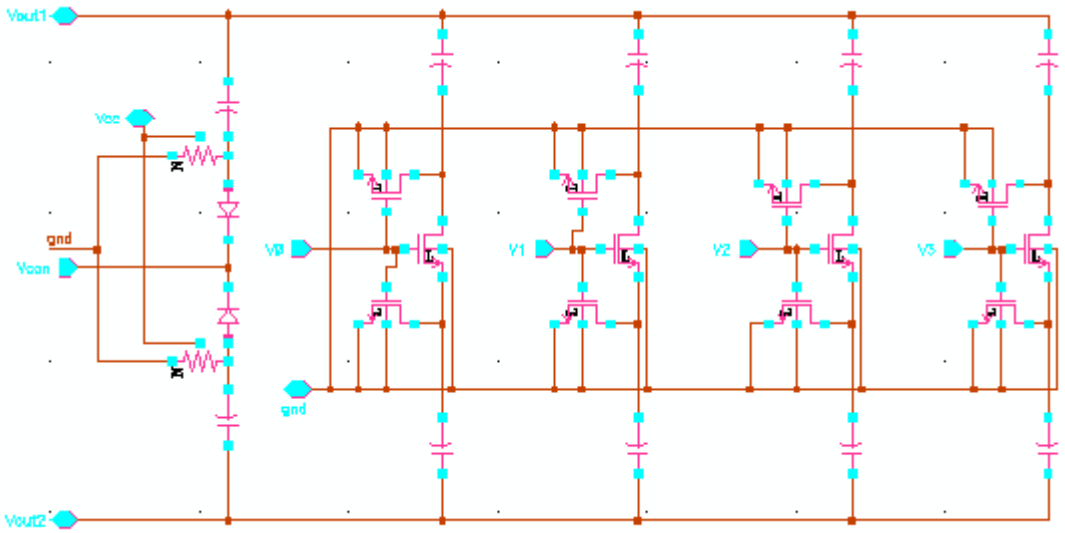


Figure 6.21: 4-bits differential SCA varactor with capacitor coupled diode varactor

6.6 A Self Biased NMOS LC VCO

For ultra low power applications, it is preferable to design a self-biasing oscillator so that voltage headroom on the bias transistor or on the bias resistor is eliminated. However, this topology needs more careful design because the transistors are biased at the supply voltage and the voltage swing increases compared to a top or bottom biased oscillator. The reason of that is the lack of self-limiting mechanism. For instance, in the presence of a tail current source, as the output voltage decreases below $V_{out,DC}$, V_{ds} of the bias transistor reduces and the bias transistor can even operate in triode region momentarily. Therefore, this phenomenon results in a limiting mechanism on the bias current and so that the output voltage. On the other hand, an increased amount of voltage amplitude causes the switching pair operate in triode region for a more time interval than those of other NMOS cross-coupled topologies.

In order to make a fair comparison with the previous designs, the current is kept close to 1.4mA. Since the transistor width and length are constant and the only variable parameter is the finger number (NF) of the RF transistor, the oscillator flows 1.45mA which is only achievable at 650mV and attains a small signal loop gain more than two. A new varactor topology is designed for course tuning in order to control the supply voltage for state “1”. This topology is called “binary weighted differential SCA”. Low threshold voltage transistors are used because of the low control voltage (0.65V). In order to check whether they are simulated properly, a standard NMOS

transistor version of this topology is realized and no difference is observed in the comparison of two phase noise spectrums. The width of the LSB switch is selected 50um to avoid R_{on} resistance loading the resonator and all the transistors are minimum length. The bias transistors are also binary weighted and the width of the transistors in the LSB branch is 1um. One drawback of this varactor structure is that when a low control voltage (<1V) is applied to the gate terminal, the on resistance is not high enough for the total capacitance of each branch to be equal to C_{MIMCAP} because as the R_{on} goes to infinity, this equality will be valid. However, this has no impact on the phase noise because during on state the AC signal on the drain and source nodes of the switches are zero since the differential signals cause these nodes to behave as virtual grounds. Therefore, no AM-PM conversion occurs.

Table 6.11: Phase noise degradation with respect to several control voltages for the worst case

Condition	Phase Noise @ 50kHz	Phase Noise @ 3MHz
only ideal cap	-83.9 dBc/Hz	-131.4 dBc/Hz
V_{dig}=0.6V, V_{diode}=0.5V	-81.8 dBc/Hz	-130.2 dBc/Hz
V_{dig}=0.6V, V_{diode}=1.4V	-81.9 dBc/Hz	-130.3 dBc/Hz
V_{dig}=1V, V_{diode}=0.5V	-81.9 dBc/Hz	-130.3 dBc/Hz
V_{dig}=1V, V_{diode}=1.4V	-82.1 dBc/Hz	-130.4 dBc/Hz
V_{dig}=1.4V, V_{diode}=0.5V	-82.0 dBc/Hz	-130.5 dBc/Hz
V_{dig}=1.4V, V_{diode}=1.4V	-82.3 dBc/Hz	-130.5 dBc/Hz

The designed circuit without an LC filter exhibits a poor performance at overall offsets. The main reason of that is the upconversion of the flicker noise in the switching pair. On phase noise spectrum, $1/f^3$ region is dominant up to several MHz. In order to reduce the flicker noise, the dimension of NMOS transistors must increase. However, the RF transistors have constant width and length, standard NMOS transistors are preferred. The supply voltage is reduced to 600mV. After that, proper dimensions are chosen satisfying a small-signal loop gain of at least two and the current value is also determined in order to keep the output voltage in current limited regime. Also, these different dimensions provide equal current. In the comparison the constant capacitor value is varied in order to keep the same operating frequency.

Table 6.12: Specifications of self-biased NMOS LC VCO

<table>
<tr><td colspan="2"></td><td colspan="3">Self biased</td><td colspan="3">with LC filter (4.3nH)</td></tr>
<tr><td rowspan="2">Phase Noise [dBc/Hz]</td><td>@50kHz</td><td colspan="3">-78.4 -82.5</td><td colspan="3">-84.1 -95.9</td></tr>
<tr><td>@3MHz</td><td colspan="3">-127.3 -130.3</td><td colspan="3">-131.2 -133.5</td></tr>
<tr><td colspan="2">Tuning Range[GHz]</td><td colspan="3">2.20-2.70</td><td colspan="3">2.20-2.71</td></tr>
<tr><td colspan="2">Power Consumption</td><td colspan="3">0.65V*1.45 mA</td><td colspan="3">0.65V*1.45 mA</td></tr>
<tr><td colspan="2" rowspan="2">Vamp [V]</td><td>bias</td><td>min</td><td>max</td><td>bias</td><td>min</td><td>max</td></tr>
<tr><td>0.65</td><td>0.48</td><td>0.60</td><td>0.65</td><td>0.48</td><td>0.60</td></tr>
<tr><td colspan="2" rowspan="2">Active Device</td><td colspan="2">Wn</td><td colspan="2">Ln</td><td colspan="2">gm</td></tr>
<tr><td colspan="2">25um</td><td colspan="2">180nm</td><td colspan="2">6.55mS</td></tr>
<tr><td rowspan="3">Varactor</td><td>Course SCA (LSB)</td><td>Wcap</td><td>Lcap</td><td>value</td><td colspan="3">Wsw</td></tr>
<tr><td>Fine</td><td>8.5um</td><td>8um</td><td>70fF</td><td colspan="3">50um</td></tr>
<tr><td>Cons.</td><td colspan="6">NF=30 (300fF-350fF)</td></tr>
<tr><td colspan="2">Digital Control</td><td colspan="3">“0”= gnd</td><td colspan="3">“1”=0.65V(Vdd)</td></tr>
<tr><td colspan="2">Fine Tuning Voltage</td><td colspan="6">0.5V – 1.4V</td></tr>
</table>

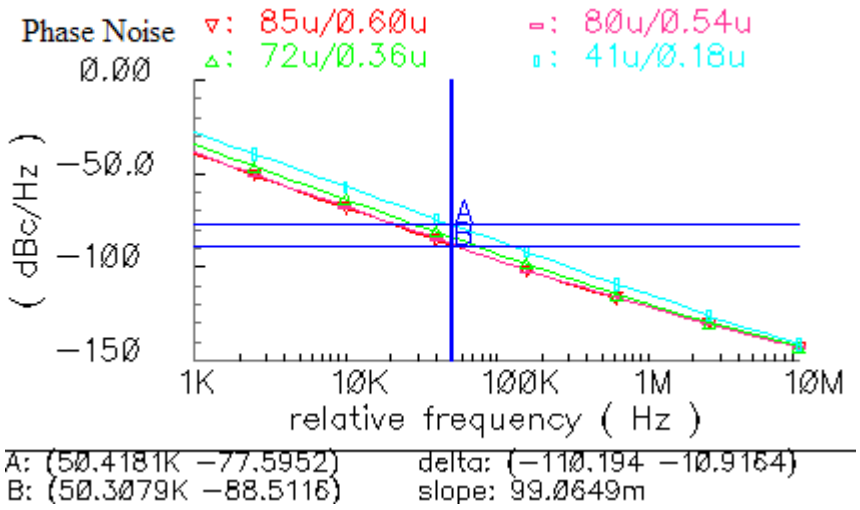


Figure 6.22: Phase noise spectrum for several transistor dimensions providing equal bias current at a fixed f_0

As shown in the above figure, the phase noise at 50kHz reduces more than 10dBc/Hz, however the increase in the dimensions has a limited effect since the increasing parasitic capacitances start to load the resonator. Also it is not possible to raise the dimensions much because of narrowing tuning range and lessening f_t. Consequently, considering these facts, optimum dimension is chosen not only satisfying start-up condition, frequency range and assuring current-limited regime

but also allowing a filtering inductor (min available 0.6nH) to resonate with common mode parasitic capacitance at $2f_o$.

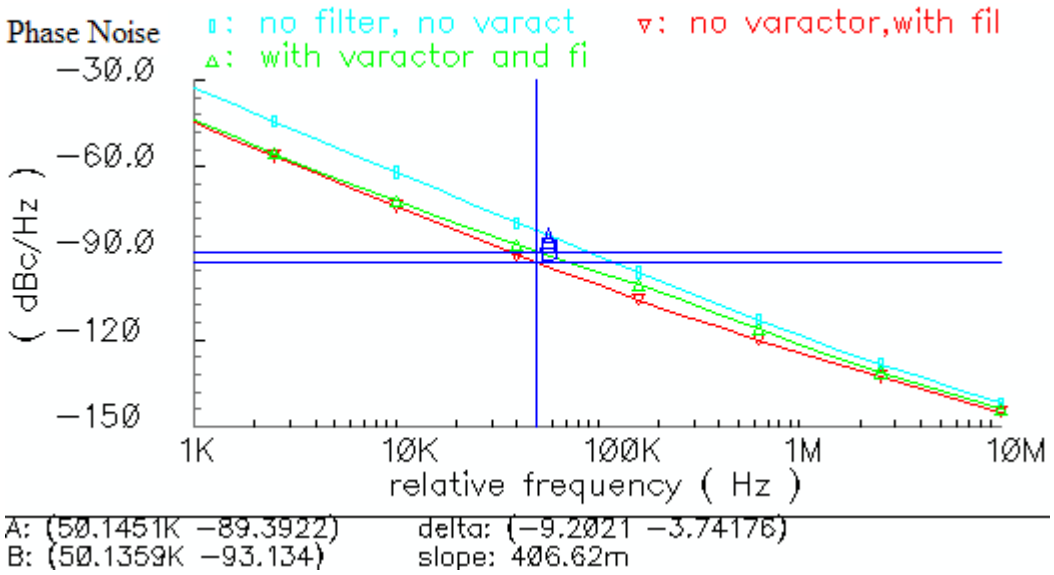


Figure 6.23: Effect of noise filter and 4 bits SCA varactor on phase noise at 2.4GHz

Table 6.13 shows the results for the optimized circuit design. Compared to the previous self-biasing design, the phase noise improves around 6dBc/Hz and 2dBc/HZ at 50kHz and 3MHz offsets, respectively. Furthermore, this oscillator with noise filter attains a better phase noise performance than the top biased RF NMOS cross-coupled LC VCO only at a very low power consumption of 900uW but occupies more area and is very sensitive to output variations.

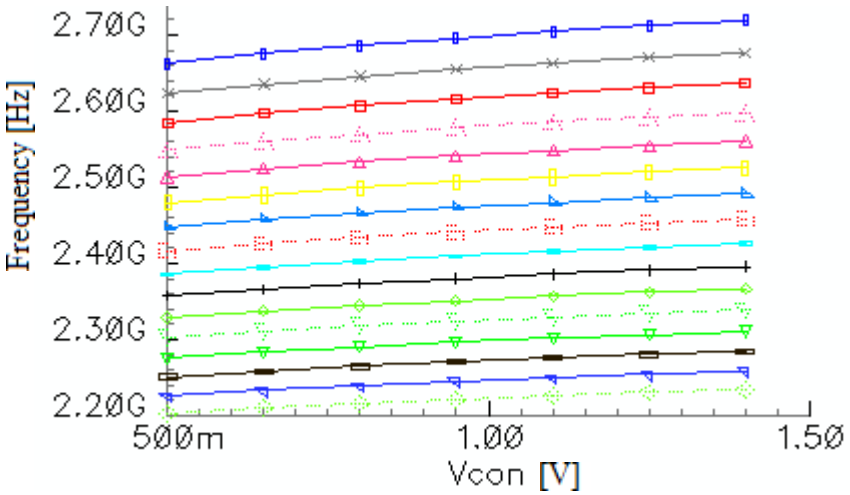


Figure 6.24: Frequency spectrum after the addition of 4 bits SCA varactor structure

Table 6.13: Specifications of self-biased NMOS LC VCO with noise optimized W/L

		Self biased			with LC filter (1.05nH)		
Phase Noise [dBc/Hz]	@50kHz	-84.3 -87.8			-88.9 -94.4		
	@3MHz	-129 -131.7			-132.7 -133.6		
Tuning Range[GHz]		2.20-2.70			2.20-2.68		
Power Consumption		0.6V*1.5 mA			0.6V*1.5 mA		
Vamp [V]		bias	min	max	bias	min	max
		0.6	0.53	0.59	0.6	0.53	0.59
Active Device		Wn		Ln		gm	
		88um		570nm		7.25mS	
Varactor	Course SCA (LSB)	Wcap	Lcap	value	Wsw		
		8.5um	8um	70fF	50um		
	Fine	NF=30 (300fF-350fF)					
	Cons.	---					
Digital Control		"0"= gnd		"1"=0.6V(Vdd)			
Fine Tuning Voltage		0.5V – 1.4V					

6.7 Implementation of Bias Level Shifting Technique [33]

To get over the issue of loaded Q-factor degradation because of the operation of the switching pair mostly in triode region during on-state in a self biased NMOS cross-coupled oscillator, the presented technique in [33] can be applied. The main goal of the technique is to reduce the time interval in which MOSFETs operate in triode region. This provides the average Q factor to degrade less. This condition is accomplished in two parts. Firstly, the DC voltage on the gate is separated from the drain terminal with a capacitor and is shifted down via an external bias voltage. Secondly, the output swing is decreased at gate terminal through capacitive dividers. Therefore, two advantages are attained with the implementation of this technique; less noise source contributed to phase noise and small degradation of loaded Q-factor during the on-state of MOS transistors [33]. On the other hand, the main drawback of this topology is the tougher start-up condition due to the use of capacitive divider and also this circuit achieves higher output swing than that of self-biasing topology.

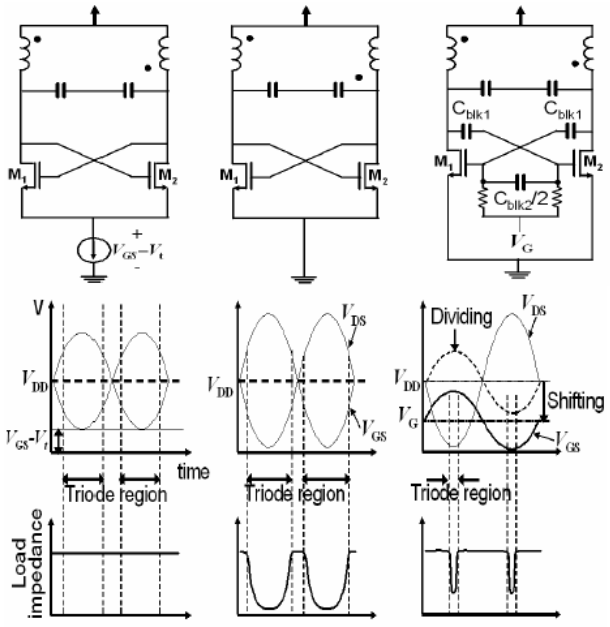


Figure 6.25: Waveforms and load impedances (*Rload*) of LC VCO (a) with current source, (b) without current source, and (c) using gate voltage dividing and bias level shifting techniques.

The bias transistor is kept a close value to 1.4mA to make the design comparable with others. The main bottleneck is the capacitive divider ratio because low current limits the achievable transconductance of a transistor; therefore it is not possible to reduce the ratio so much in order to meet start-up condition. Firstly, this topology is implemented with RF NMOS transistors. The ratio value is selected as 0.78 so that a small signal of two is attained by increasing the finger number. The supply voltage is set to 1V and the transistors are biased at 0.6V. In the course tuning implementation, 4-bits differential switched capacitor array with MIM capacitors are utilized.

The bias level shifting technique suffers from high output swing in our design. The idea behind the proposed technique does not work because the high output swing at the gate loads the resonator and degrades effectively the quality factor. This is also proven by the results after the addition of the inductance at the common mode node.

The phase noise significantly reduces and reaches the highest achieved value at 3MHz offset among all oscillator circuits designed up to this section.

Table 6.14: Specifications of NMOS LC VCO with bias level shifting

		Bias Level Shifting			with noise filter		
Phase Noise [dBc/Hz]	@50kHz	-74.4 -79.6			-86.4 -93.8		
	@3MHz	-123.9 -128.9			-133.1 -136.4		
Tuning Range[GHz]		2.19-2.70			2.19 – 2.71		
Power Consumption		1V*1.53 mA			1V*1.53 mA		
Active Device (RF NMOS)		W	L	gm	W	L	gm
		35um	180nm	8.2mS	35um	180nm	8.2mS
Vamp [V]		bias	min	max	bias	min	max
		1	0.87	0.97	1	0.84	0.95
Varactor	Course SCA (LSB)	Wcap	Lcap	Wsw	Wcap	Lcap	Wsw
		8.5um	8um	50um	8.5um	8um	50um
	Fine	300fF-350fF			300fF-350fF		
	Cons.	C1=2.51pF C2=610fF			C1=2.51pF C2=610fF		
Digital Control		“0”= gnd	“1”=1V(Vdd)		“0”= gnd	“1”=1V(Vdd)	
Fine Tuning Voltage		0.5V – 1.4V			0.5V – 1.4V		

In order to reduce the effect of switching pair flicker noise, a similar design method is implemented to this topology that the dimension of standard NMOS transistors is increased to 68um/0.38um. The current is chosen as to be 1.44mA that provides sufficient loop gain and keep the operation very close to the voltage-limited regime.

After that optimization, a significant phase noise improvement around 7dBc/Hz is achieved at 50kHz offset. Again, the degradation of the quality factor because of the long time period of operation in triode region is observed. The noise filter works significantly to reduce this effect on phase noise. The improvement at low offsets reaches up to 14dBc/Hz.

Table 6.15: Specifications of NMOS LC VCO with bias level shifting after noise optimized W/L

		Bias Level Shifted			With LC filter L=1.9nH		
Phase Noise [dBc/Hz]	@50kHz	-81.3 -86.2			-86.7 -100.5		
	@3MHz	-125.1 -129.5			-130.7 - 138.1		
Tuning Range[GHz]		2.20-2.71			2.20-2.71		
Power Consumption		1V* 1.44mA			1V*1.44mA		
Active Device (NMOS)		Wn	Ln	gm	Wn	Ln	gm
		68um	380nm	8.2mS	68um	380nm	8.2mS
Vamp [V]		bias	min	max	bias	min	max
		1	0.9	0.98	1	0.87	0.98
Varactor	Course SCA (LSB)	Wcap	Lcap	Wsw	Wcap	Lcap	Wsw
		8.5um	8um	50um	8.5um	8um	50um
	Fine	300fF-350fF			300fF-350fF		
	Cons.	C1=1.81pF C2=400fF			C1=1.81pF C2=400fF		
Digital Control		"0"= gnd	"1"=1V(Vdd)		"0"= gnd	"1"=1V(Vdd)	
Fine Tuning Voltage		0.5V – 1.4V			0.5V – 1.4V		

6.8 Differential Colpitts Implementation

The Colpitts configuration features superior phase noise because noise current from the active devices is injected into the tank during minima of the tank voltage when the impulse sensitivity is low [27]. For this reason, in this section three variations of differential Colpitts oscillator explained in 2.3.4 are aimed to design. To make a fair comparison, the bias current is kept at 1.4mA. The first oscillator is basically a combination of two single-ended Colpitts structure (Fig. 2.15) so it suffers from severe start-up condition. To get over this matter, the ratio of capacitive divider is selected as 1/3 although the capacitor C_2 must be chosen to be four times C_1 for near optimum operation [3]. Even in this situation, the start-up condition could not be met because each transistor flow only a current of 700uA whereas the necessary transconductance $2\cdot(1/N)\cdot g_L$ is around 20mS at the highest transconductance loss. Secondly, the current shifting Colpitts structure [6] which reduces the required large signal transconductance is designed with equal divider ratio, but again the start-up condition could not be met since it needs a small signal transconductance value of around 12mS.

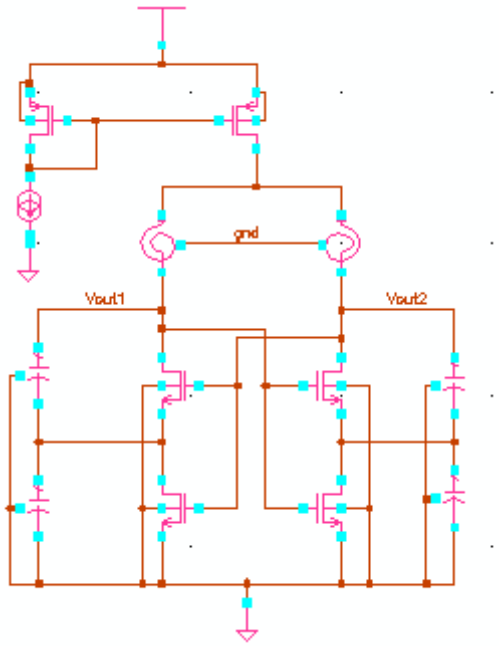


Figure 6.26: Circuit schematics of Gm boosted differential Colpitts VCO

The latest circuit is the G_m boosted differential Colpitts oscillator [21]. This structure enhances the large signal transconductance by a factor of $(2+C_2/C_1)$ which relaxes the start-up condition significantly. For a capacitive divider ratio of N=1/3, the necessary small signal transconductance is around 5mS which is even less than a conventional NMOS cross-coupled topology. The bias circuitry is kept the same and the sizes of the bias and reference transistor are preserved. The lower transistors have a dimension of 25u/0.18u whereas that of the switching pair is 35u/0.18u which is obtained with respect to phase noise performance. The small-signal transconductance is 8mS.

To see the effect of the capacitive divider ratio, two more simulations are run with N=1/4 and N=1/5. Since the small-signal transconductance is around 8mS, the small signal loop gain is more than two even for the lowest divider ratio. The transistor dimensions are kept the same and the suitable values of MIM capacitors are selected to meet the frequency tuning range. The coarse tuning of the oscillator is provided by the first structure as shown in Fig. 6.13. Among different N values, the best phase noise performance at low offsets is achieved when N=1/5 whereas three circuits exhibit close performance at high offsets. The NMOS cross-coupled oscillator designed in section 6.3 have the same devices except switching transistors.

Comparing NMOS cross-coupled design with Gm boosted Colpitts oscillator for N=1/5, Colpitts exhibits worse performance at all offsets.

Table 6.16: Specifications of Gm Boosted Colpitts VCO for several capacitive divider ratio values

Gm Boosted Colpitts		N=1/3	N=1/4	N=1/5
Phase Noise [dBc/Hz]	@50kHz	-87.3 -90.0	-87.8 -91.1	-88.1 -91.7
	@3MHz	-129.1 -131.7	-128.8 -131.7	-128.7 -131.6
Tuning Range[GHz]		2.20– 2.70	2.20– 2.70	2.20-2.70
Power Consumption		1.4V*1.4mA		
Bias Circuitry		W	L	Ratio
		400um	1um	4
Active Device		Wn	Ln	gm
		40um	180nm	8mS
Vamp [V]		bias	min	max
		0.62	0.35	0.44
Varactor	Course tuning	W	L	
		16um	400nm	
	Fine tuning	NF=30 300fF-350fF		
	Cons.	C1=0.79pF C2=1.58pF	C1=0.71pF C2=2.12pF	C1=0.67pF C2=2.66pF
Digital Control		“0”= gnd	“1”=Vdd	
Tuning Voltage		0.5V – 1.4V		

6.9 Self-biased Gm Boosted Differential Colpitts VCO design

To reduce the power consumption, a self biased version of the Gm boosted Colpitts topology is designed. In this case, the bottom transistors can be used as biasing transistors and the start-up condition is met by altering the dimensions of the switching pair but this also affects the value of the bias current. The size of the switching pair is reduced to 25um/0.18um and the bottom transistors is kept the same so that the current around 1.4mA which gives the opportunity to make a fair comparison with other designs. The voltage supply is chosen to be 0.75V. The 4- bit differential SCA composed of the low-V_{th} PMOS transistor as the switch is implemented

Table 6.17: Specifications of self-biased Gm Boosted Colpitts VCO for N=1/5

Gm Boosted Colpitts N=1/5		Self-biased		
Phase Noise [dBc/Hz]	@50kHz	-84.5 -89.3		
	@3MHz	-131.0 -132.6		
Tuning Range[GHz]		2.20 – 2.70		
Power Consumption		0.75*1.4mA		
Active Device (NMOS)		Wn	Ln	gm
		25um	180nm	8 mS
Vamp [V]		bias	min	max
		0.62	0.40	0.61
Varactor	Course SCA (LSB)	Wcap	Lcap	Wsw
		8.5um	8um	50um
	Fine	300fF-350fF		
	Cons.	C1=0.5pF C2=2pF		
Digital Control		"0"= gnd	"1"=0.75V(Vdd)	
Fine Tuning Voltage		0.5V – 1.4V		

The phase noise degrades at low offset frequencies. However, the removal of the bias circuitry must contribute to less close in phase noise due to elimination of bias transistor flicker noise upconversion. This result is similar to the result obtained in the NMOS cross-coupled topology. However, in the cross-coupled topology the close-in phase noise reduces as the size of the switching pair increases whereas in differential Colpitts topology, the close-in phase noise degrades as the size of the switching pair increases. This can be related to the AM-PM conversion mechanism on the switching pair because the linearity of these transistors is increased and the phase noise reduces.

6.10 Buffer Design

A buffer is designed for PMOS biased NMOS cross-coupled topology for 50 Ω load termination. The DC component of the buffer output is isolated by a 40pF capacitor. The buffer is composed of two-stages due to the VCO output bias voltage value that is around 620mV. Low threshold transistors are employed in order to keep the buffer voltage at the same value of that of the VCO. It delivers -10dBm output swing to the load.

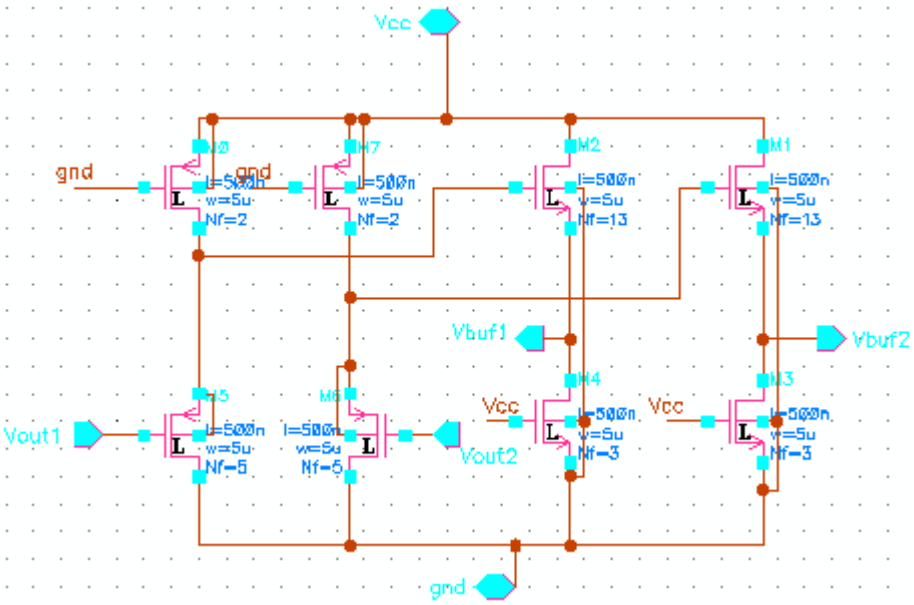


Figure 6.27: Schematic of buffer

6.11 Layout

The layout of the NMOS cross-coupled pair with PMOS bias circuitry is drawn in order to investigate the physical effects on the VCO design. The main important issue in a differential circuit is the symmetry between two halves of the circuit. In a differential oscillator, any asymmetry will generate an imbalance in the tank causing the frequency to change. Moreover, this will also affect the phase noise mismatch between the output waveforms. Therefore, the modules are placed with respect to the axis of symmetry.

Since only an asymmetric spiral inductor is supplied by the UMC library, two inductors are implemented in the layout. This causes to occupy a substantial amount of area and has a significant impact on the overall layout area. One of the drawbacks of the large area inductors is the long metal wires between the tank and the other devices. The resistance of the metal wires will reduce the quality factor of the tank. Hence, the metal 6 is chosen due to its low resistivity and the wires are kept as wide as possible.

The quality factor of the MOS varactor is determined by the gate resistance. To reduce it, the gate of the fingered transistors is connected from both sides. Also, the total length of each gate including the length of the connection between poly lines for two transistors in the each MOSCAP pair is kept the same. All the MOSFETS in fine

tuning structure has a length of 400nm whereas the widths are 1um and 8um for the LSB and MSB implementation, respectively. Furthermore, the AC current on the tank is Q times higher than and each metal type has a different per um. The DC and AC electromigration rules of metals, via and contacts are taken into account in the layout of the tank.

In the fine tuning structure, the MIMCAPs are protected with a p-type ring. Each high resistive n-well resistor is realized by combining two parallel resistors. Two dummy resistors are placed around each parallel resistor. They are also surrounded by guard rings in an n-well. The RF MIMCAPs are added for the realization of constant capacitors. These capacitors are ready to place with its guard rings and shields.

The bias circuitry is separated into two equal parts. Each cell is divided into sufficient fingers in order to carry the dc current with respect to the metal widths. The shorted dummy transistors are also added to short edges of the structures. In between two parts the MOS varactor structure is implemented.

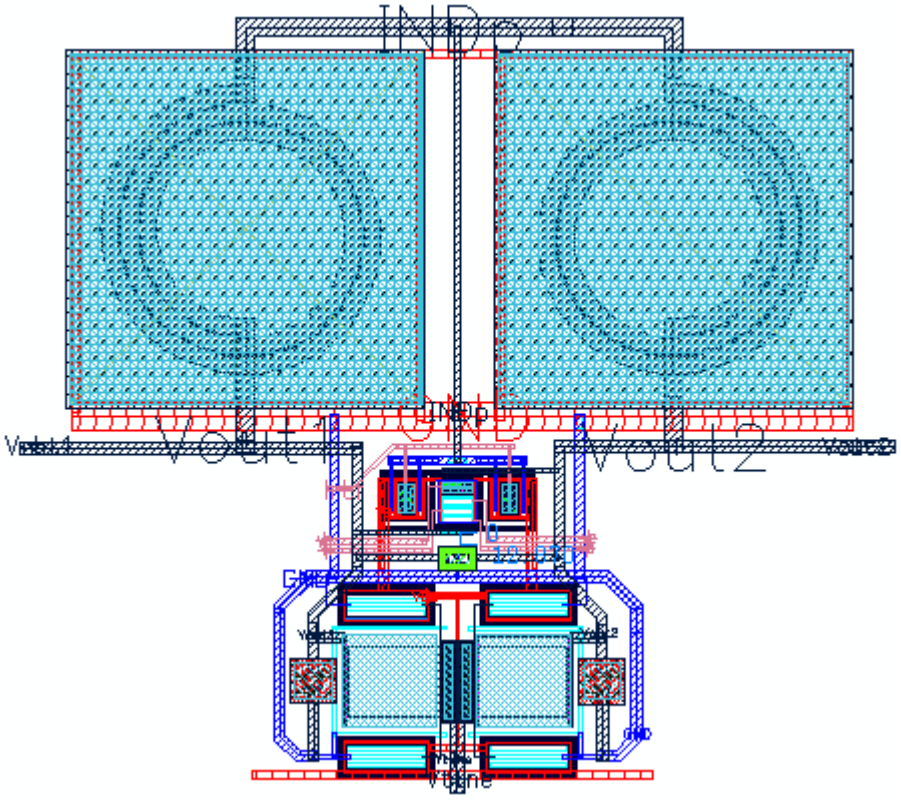


Figure 6.28: Layout of VCO

The switching pair is composed of two RF transistors. For better matching, they are connected in the same guard ring and protection pads. Their source terminals are overlapped and the connections from metal 6 to via 2 are removed since the ground wire is metal 2 in the overall layout. The connections of cross-coupling of the transistors are provided in the guard ring with only metal 6.

After post-layout simulation, the parasitic capacitances shift the frequency 200MHz down, but this is compensated by reducing the value of the constant capacitor. The phase noise is increased 4dBc/Hz, the main reason of that the reduction in the quality factor of the tank; mainly of the IMOS varactor structure. To verify that, a post-layout simulation with externally added coarse tuning structure is run and the difference in the phase noise is around 3dBc/Hz. The settling time of the output waveform is around 58ns and 17ns for the worst and best cases, respectively.

7. CONCLUSIONS

In this work, several LC oscillators were designed to meet the specifications of Bluetooth standard in UMC 0.18u technology at low power consumption. All the LC VCOs consume a power less than 2mA. The frequency control was provided by 4 digital bits for coarse tuning and a DC voltage between 0.5V and 1.4V for fine tuning. The digital control voltages were set to ground and supply voltage in all circuits. The AM-PM conversion was reduced due to proper design of varactor structure. The first varactor structure employing IMOS circuitry only degrades the phase noise around 2.5dBc/Hz whereas the differential SCA varactor degrades around 2dBc/Hz at low offset. At high offset the phase noise degradation reduces to 0.9dBc/Hz and 1.2dBc/Hz for two structures, respectively.

The first oscillator, PMOS biased NMOS cross-coupled oscillator attained the required the phase noise specification with a 5dBc/Hz phase noise margin for the worst case. The oscillator has a FOM (figure of merit) of -185.1 at 50kHz and-185.6 at 3MHz for a power consumption of less than 2mW.

In addition to this oscillator, lower power LC cross-coupled oscillators presented in several papers were designed. After the simulations of these circuits, it was observed that the flicker noise of the switching transistors has a significant impact on the phase noise for self biased oscillators, their dimension must be optimized. Furthermore, an inductor must be connected to the common mode ground to filter the second harmonic and to avoid loading of the resonator while operating in triode region. Consequently, low power solutions generally need an extra inductor, in other words, low power solutions attain the phase noise specification at a cost of larger area. The best phase noise performance achieved in the bias level shifting NMOS LC VCO with noise filter. The best FOM value is -191.3 at 50kHz and -193.2 at 3MHz. These values are significant and superior to the most of the oscillator designs presented in the literature. However, this oscillator has an output swing of close to 2V, therefore it is not suitable for most applications and also the phase noise spectrum at low offset varies around 13dBc/Hz.

Taking the popularity of the Colpitts oscillators into account, a differential Gm boosted Colpitts oscillator is also designed with the same power consumption. However its phase noise performance is slightly worse than the first designed oscillator.

All in all, several LC VCOs were simulated by maintaining the same amount of current so this study can also be described as a comparative study for low power applications which do not require stringent phase noise specification.

In the future work, the VCO can be implemented into a PLL structure and its performance measurements can be done. To reduce the area of the layout, a center tapped inductor can be designed and MIMCAPS can be replaced by MOS capacitors. Higher Q inductor models in different technologies or bondwire inductors can be employed.

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APPENDIXES

A. Inductor Q and Parameter Calculator

```
%%%%%% Inductance Q and Parameter Calculator %%%%%%
clear all

u=1e-6;
G=1e9;

%%%%% Cadence Input Parameters %%%%%
f=2.45*G;
D=161.06*u;
N=2.5;
W=19*u;

%%%% Internal Calculations %%%%


%%%%% Equivalent Network (Distributed Parameters) %%%%%
Rs=p_rs*(1+drs_l_rf);
Ls=p_ls*(1+dls_l_rf);
Cs=p_cp*(1+dcp_l_rf) * ( 2/S_um);
Cox1=p_cox*(1+dcox_l_rf);
Cox2=p_cox*(1+dcox_l_rf);
Rsub1=p_rsub1;
Rsub2=p_rsub2;
Csub1=p_csub1;
Csub2=p_csub2;



%%%%% Equivalent Network (of Narrowband Model) %%%%%

w=2*pi*f;
Rp1=(1+(w*Rsub1*(Csub1+Cox1))^2)/(w^2*Rsub1*(Cox1)^2);
Rp2=(1+(w*Rsub2*(Csub2+Cox2))^2)/(w^2*Rsub2*(Cox2)^2);
Cp1=(Cox1+w^2*Rsub1^2*(Csub1+Cox1)*Csub1*Cox1)/(1+((w*Rsub1)*(Csub1+
Cox1))^2);
Cp2=(Cox2+w^2*Rsub2^2*(Csub2+Cox2)*Csub2*Cox2)/(1+((w*Rsub2)*(Csub2+
Cox2))^2);

%%%%% Grounded Inductance Values %%%%%

%%% Grounded from right side (gr_r) %%%
Cp_gr_r=Cp1;
Ls_gr_r=Ls;
Rs_gr_r=Rs;
Cs_gr_r=Cs;
```

```
gl_gr_r=Rs/(Rs^2+(w*Ls_gr_r)^2)+1/(Rp1);
Q_gr_r=1/(gl_gr_r*w*Ls_gr_r);

Csr_gr_r=Cp_gr_r+Cs_gr_r;  %% self resonant cap
Lsr_gr_r=Ls;
fsr_gr_r=1/(2*pi*sqrt(Csr_gr_r*Lsr_gr_r));

%%% Grounded from left side (gr_l) %%%
Cp_gr_l=Cp2;
Ls_gr_l=Ls;
Rs_gr_l=Rs;
Cs_gr_l=Cs;

gl_gr_l=Rs/(Rs^2+(w*Ls_gr_l)^2)+1/(Rp2);
Q_gr_l=1/(gl_gr_l*w*Ls_gr_l);

Csr_gr_l=Cp_gr_l+Cs_gr_l; %% self resonant cap
Lsr_gr_l=Ls;
fsr_gr_l=1/(2*pi*sqrt(Csr_gr_l*Lsr_gr_l));

%%% Differential Inductance Values %%%

Cp_diff=Cp1*Cp2/(Cp1+Cp2);
Ls_diff=Ls;
Rs_diff=Rs;
Cs_diff=Cs;

gl_diff=Rs/(Rs^2+(w*Ls_diff)^2)+1/(Rp1+Rp2);
Q_diff=1/(gl_diff*w*Ls_diff);

Csr_diff=Cp_diff+Cs_diff; %% self resonant cap
Lsr_diff=Ls;
fsr_diff=1/(2*pi*sqrt(Csr_diff*Lsr_diff));
```

B. Layout Details

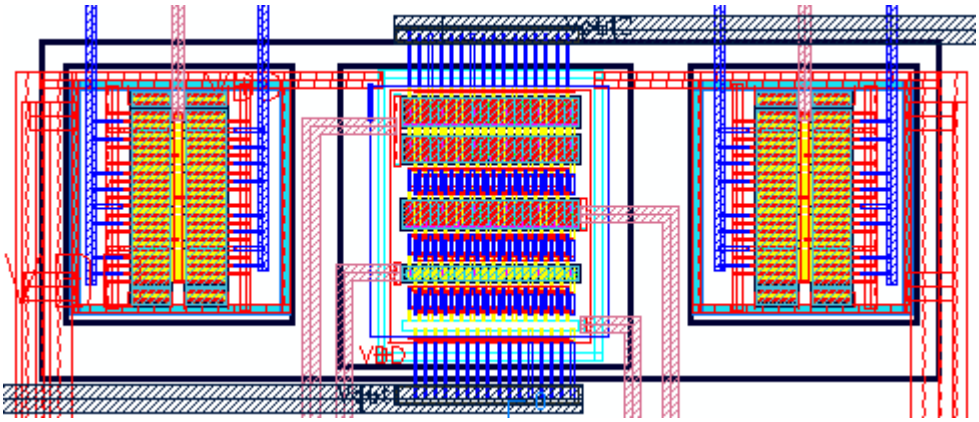

Figure A.1: Layout of SCA varactor and bias circuitry

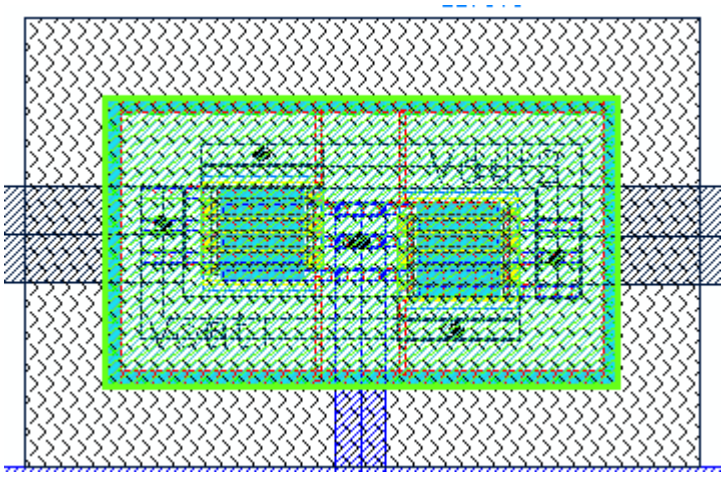

Figure A.2: Layout of switching transistors

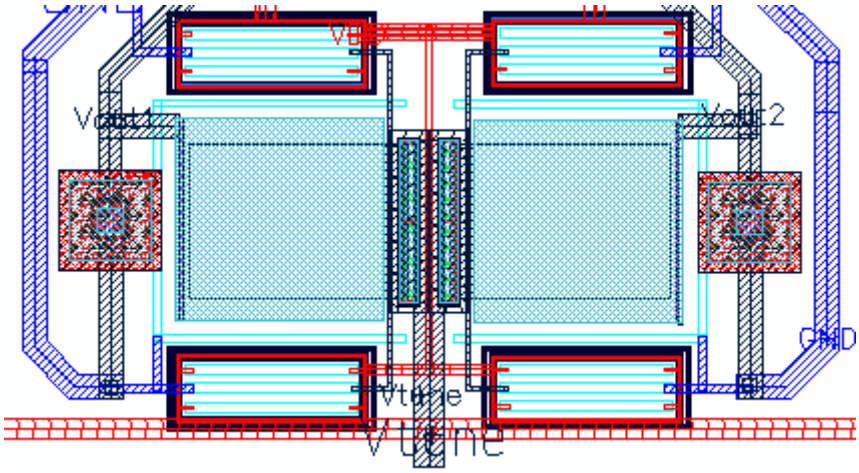

Figure A.3: Layout of capacitor coupled diode varactor

RESUME

Volkan ORHAN was born in Istanbul in 1983. In 2001, he was enrolled with the programme of Electronics Engineering at Istanbul Technical University (ITU). During his undergraduate study, he completed his first internship in the hardware section of R&D department of traffic management system of ISBAK A.S. He was an intern in AGH University of Science and Technology where he studied on the physical characteristics of SOI MOSFETs in Krakow. In the final project, he designed a high efficiency class-D audio amplifier under the supervisory of Prof. Melih PAZARCI. After receiving his B.Sc. degree in 2005, he continued the master programme in the same section. During his thesis term, he was accepted as an exchange student by EPFL (Swiss Federal Institute of Technology Lausanne) for the whole academic year.
His research interests are analog and RF IC design.