İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

CLOCK AND DATA RECOVERY USING BANG-BANG PLL's

M.Sc. Thesis by

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Department : **Electronics and Communications Engineering**

Programme: **Electronics Engineering**

JUNE 2008

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Date of submission : 5 May 2008

Date of defence examination: 9 June 2008

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JUNE 2008

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

İKİ KONUMLU FKÇ'ler ile SAAT ve DATA İŞARETLERİNİN YENİDEN ÇIKARIMI

YÜKSEK LİSANS TEZİ

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Tezin Enstitüye Verildiği Tarih : 5 Mayıs 2008
Tezin Savunulduğu Tarih : 9 Haziran 2008

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HAZİRAN 2008

ACKNOWLEDGEMENT

I would like to thank my supervisor Prof. Dr. Ali Toker for his support and guidance during this thesis.

TUBITAK supported me financially during my Master of Science education. I really appreciate their help.

I am also grateful to my colleagues in Maxim Istanbul Design Center, with whom I discussed and learned many things about clock and data recovery circuits.

This thesis is dedicated to my family. I would like to thank them for their endless support and love.

June, 2008 **Çağlar YILMAZER**

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ABBREVIATIONS

CDR	: Clock and Data Recovery
FKÇ	: Faz Kilitlemeli Çevrim
VCO	: Voltage Controlled Oscillator
CCO	: Current Controlled Oscillator
PD	: Phase Detector
PLL	: Phase Locked Loop
FLL	: Frequency Locked Loop
ADC	: Analog to Digital Converter
DAC	: Digital to Analog Converter
SERDES	: Serializer and Deserializer
V2I	: Voltage to current converter
CML	: Current Mode Logic
FF	: Flip-flop

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İKİ KONUMLU FKÇ'ler ile SAAT ve DATA İŞARETLERİNİN YENİDEN ÇIKARIMI

ÖZET

Bu çalışmada, saat ve data işaretlerinin yeniden çıkarımında kullanılan iki konumlu faz kititlemeli çevrimlerden bahsedilmiştir. Sistem seviyesinde hızlı simülasyonlar yapabilmek amacıyla çevrim elemanlarının davranışsal modelleri geliştirilmiştir. İki konumlu kontrol sistemlerinin el ile analizinin oldukça zor olmasından dolayı modelleme zorunlu hale gelmektedir. Ayrıca gerçeklenen elemanların idealsizliklerinden kaynaklanan davranışlar da olabilidiğince modellenmeye çalışılmıştır. Söz konusu faz kilitlemeli çevrimlerin sistem seviyesinde sağlaması gereken özelliklerin kabaca hesaplanması ve datadaki değişim sıklığının bu özellikleri nasıl etkilediği anlatılmıştır. Çevrim elemanlarının tranzistör seviyesinde nasıl gerçeklendiklerinden bahsedilmiştir. Çok kullanılan bir ring osilatör yapısı olan simetrik yüklü osilatör (Maneatis yük) çevrimde etkili bir şekilde kullanabilmek amacıyla modifiye edilmiştir. Osilatörün üretim ve sıcaklık değişimlerini tolere edebilmesi için kazancının yüksek olması gerekir. Bu da sistemin harici gürültü kaynaklarına (besleme, taban gürültüsü gibi) olan duyarlılığını oldukça arttırmaktadır. Bu nedenle osilatörü otomatik olarak kalibre eden bir teknik geliştirilmiştir. Değişik faz kilitlemeli çevrimlere uygulanabilen teknik için osilatörün akım kontollü olması gerekmektedir. Frekans kitlenmesi gerçekleştikten sonra osilatörün akımı bir analog-sayısal çevirici ile örneklenmekte ve asıl sistem bu nokta etrafında daha dar bir bölgede çalışmaktadır. Ayrıca, sıcaklıktan kaynaklanabilecek değişimler de analog-sayısal dönüştürücünün refererans akımı üzerinden kompanze edilmektedir. Son olarak, tasarlanan sistemin simülasyon sonuçları verilmiştir. 0.18um CMOS teknolojisinde tasarlanan devre 5Gb/s data hızlarında çalışabilmektedir.

CLOCK AND DATA RECOVERY USING BANG-BANG PLL's

SUMMARY

In this work, bang-bang PLL structures, which are extensively used in clock and data recovery systems, are investigated. Behavioral models of loop elements are created to do faster simulations in system level. This step is mandatory in bang-bang systems, which are hard to analyze with simple calculations. Some non-idealities of real circuit elements are inserted to these models. System level design issues of bang-bang PLL's are discussed and the effect of data transition density to system specifications is mentioned. Transistor level implementations of loop elements are described. A popular delay cell with symmetric loads (Maneatis cell) is modified to be used effectively in a bang-bang loop. Gain of the VCO seems very large after initial design, which is required to cover the operating frequency range over process and temperature corners. Large gain makes the system prone to external noise sources such as noise from power supply, substrate etc. Therefore, an automatic calibration method is developed to reduce the VCO gain. This technique can be applied to any current controlled oscillators in various phase locked loops. After frequency lock is achieved, current of the oscillator is sampled by a current mode ADC and a narrower range is generated around that point. Additionally, frequency variation due to temperature is compensated through the specifically designed reference current of ADC. Finally, simulation results of CDR and calibration circuits are given. CDR is designed in 0.18um CMOS technology and can operate at 5Gb/s data rate.

1. INTRODUCTION

In most of the communication standards clock is not transmitted through a second link. This is sometimes due to the impossibility like in fiber communications or due to time skew and cost issues like in a SERDES (serializer/deserializer) design. A clock and data recovery circuit should extract the clock information from data and optimally sample it (e.g. in the middle of the eye diagram) for maximum jitter tolerance.

Among Clock and Data Recovery (CDR) structures bang-bang topologies have gained importance during the last years. It has some important advantages. A bang-bang CDR can automatically center its clock to the eye diagram of data signal, which is important for maximum jitter tolerance. In a given technology, it can work at frequencies where a working flip-flop can be designed [1]. This is due to the fact that it only generates one bit long UP or DOWN pulses indicating the clock is early or late. It is also easily adaptive to half rate clocks. This can relax the Voltage Controlled Oscillator (VCO) speed requirements but we need the quadrature phases of the VCO in this case.

It has also some critical issues which should be addressed carefully in the design phase. Due to the fact that its phase detector is non-linear, design requires many iterations with time domain behavioral models. These models should include many non-idealities. Bang-bang loop creates large hunting (or quantization) jitter. If loop delay is too large, jitter generation may increase. Large loop delay also decreases the stability factor [1]. Metastability in the phase detector latches may also contribute to jitter generation [2, 3]. Tracking bandwidth of the latches (latch hysteresis) may cause pattern dependent jitter [2].

A bang-bang CDR loop consists of integral and proportional paths [1]. Integral path keeps the VCO at data frequency whereas the proportional path dominantly adjusts the phase of the clock. Proportional path modulates the VCO frequency in small amounts around the center frequency. This path should be fast enough to reduce the inherent jitter generation of CDR. In fact, a VCO should respond to an UP or DOWN pulse in one bit time ideally. Additionally, frequency jumps should be well controlled over process and temperature corners because it largely determines the loop specifications. A method to obtain well controlled bang-bang frequency steps is

proposed in [4] for a bipolar ring VCO. Bang-bang frequency steps are generated by modulating the main current of the oscillator. A similar technique is used in this thesis but it is applied to a CMOS ring oscillator. Modulation speed is optimized for CML type input signals.

Voltage controlled oscillators should have sufficient gain to cover the desired frequency band over process and temperature variations. Required gain increases due to lower supply voltages and higher operating frequencies. This makes VCO more susceptible to noise coming from loop filter, power supply etc. Some techniques are proposed in [5-7]. In all these techniques, VCO gain is reduced by dividing the desired frequency range into overlapping sub ranges. Proper sub-range is found during initial lock by searching all the ranges. Range searching algorithms may result in long locking times or more complex circuits. Additionally in these approaches, if VCO locks close to the limits of a range, a re-calibration need may arise due to changes in temperature. If this should be avoided, ranges have to be wider, which results in a large oscillator gain.

To overcome the limitations mentioned above, a new calibration method is developed to reduce the VCO gain in CDR systems but it can be applied to other phase locked loops as well. After the frequency locked loop completes the frequency acquisition, current of the oscillator is sampled by a current mode Analog to Digital Converter (ADC). Then, a narrower range is generated around the operating point, which prevents the VCO to be calibrated close to the range limits. This provides robust calibration to process variations. Additionally, frequency variation due to temperature is compensated through the specifically designed reference current of ADC.

Organization of the thesis is as follows. First section includes the introduction part and a general review of CDR loops. Linear and bang-bang phase detectors are described. Bang-bang loops are presented in system level. Section II presents the system level design issues of bang-bang loops. In Section III, behavioral modeling of CDR's is described. Some useful behavioral elements are constructed to be used in transistor level simulations. Design of loop components is discussed in Section IV. Automatic frequency calibration method is described in Section V. Simulation results of the entire system are also presented in this section. Finally, Section VI gives the conclusion and future work directions.

1.1 CDR Phase Detectors

There are two basic data formats: NRZ (non return to zero) and RZ (return to zero). NRZ is almost universally used due to relatively lower data bandwidth required. As

depicted in Figure 1.1, data frequency (assuming 10101010… pattern) is half of the clock frequency. This causes classical mixer type phase detectors fail in recovering the clock because multiplying two different frequencies in time domain results a signal with a zero average.

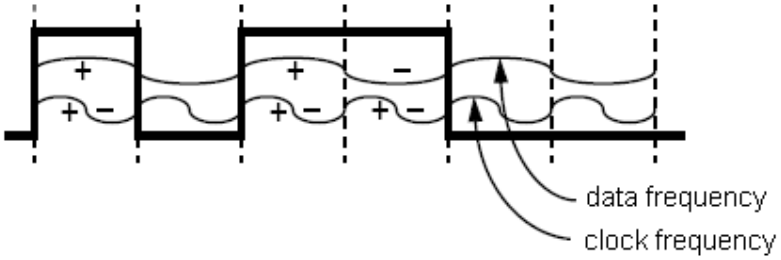

Figure 1.1: NRZ signal

Basically phase detector in a CDR should provide edge detection (both edges for NRZ data) and produce a signal indicating clock is early or late. Phase detectors (PD) used in CDRs can be grouped into two main categories:

- Linear (Continuous) phase detectors: These PDs generate a non-zero DC component linearly proportional with the time difference of clock sampling edge and optimum sampling point, Figure 1.2.
- Bang-bang (Binary) phase detectors: These types are also called binary or early-late phase detectors. They generate one bit UP or DOWN signal to indicate whether clock is early or late, Figure 1.2.

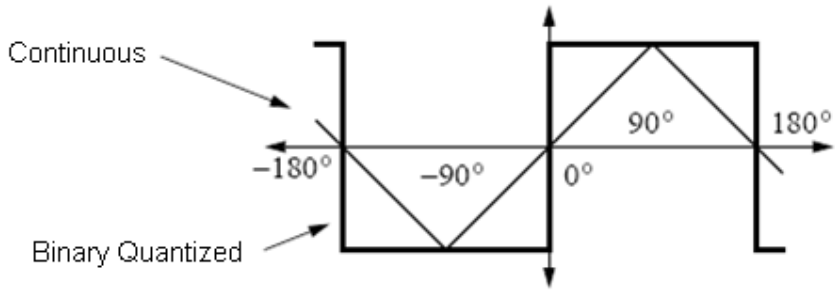

Figure 1.2: Phase vs. output average of two types of phase detectors

1.1.1 Linear Phase Detectors

First inventor of this type of PD is Hogge [8]. It is instructive to start with its basic but problematic implementation [9]. The circuit on the left in Figure 1.3 is an edge-detector circuit. If we replace the delay element with a flip-flop (FF), we can obtain the synchronous version of the edge detector. If clock rising edge is far from data transition point a proportional signal is generated at the output. This circuit provides

both edge detection and a signal proportional with the phase difference. Falling edge of CK signal samples the data.

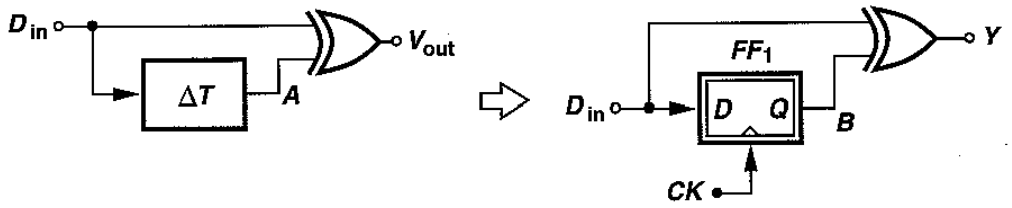

Figure 1.3: Simple linear phase detector

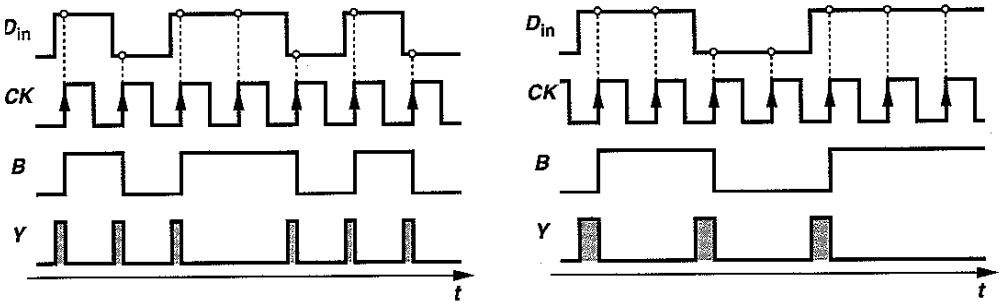

Figure 1.4: Waveforms for the PD above for different transition densities

The problem of the circuit above is that DC component of PD output is dependent on transition density. As depicted in Figure 1.4, although phase difference is two times higher in the second figure, output average is same due to lower transition density. In order to solve this pattern dependency problem reference pulses are added to the output signal. These are pulses generated at each transition and have a constant width. Final phase detector circuit is depicted in Figure 1.5. Y signal is the same as in the circuit above. X is the reference signal having constant pulse-width (Tck/2). A is the half clock period delayed version of B. A xor B output provides reference pulses in each transition. Integration of difference of Y and X pulses drives the loop towards lock. Rising edge of the clock samples the data in this implementation. In locked condition, the area of Y pulses is equal to the area of X pulses.

If we consider CK-to-Q (Tck2q) delays of FFs, Y pulse is actually Tck2q wider than needed. X reference pulse width is still equal to half of the clock period because B and A signals are delayed by the same amount at rising and falling edges. Under zero phase error condition (e.g. when CK samples the data at the middle point), difference of Y and X pulses is not zero in average due to clock-to-output delay. If we think of the closed loop response, CK deviates from ideal sampling point by Tck2q in steady state behaviour. This reduces the jitter tolerance especially if bit times are comparable with Tck2q. To reduce this effect, a delay is added between

D_{IN} and 1st XOR input. This delay should match with CK-to-Q delay of the flip-flops used in the circuit. This is a disadvantage of this phase detector since matching may not be perfect due to device mismatches. Another critical issue is that a real charge pump should follow this PD to achieve infinite loop gain. This charge pump should operate comfortably with pulses half a bit period wide to avoid dead zone problems. This issue can limit the maximum reliable speed of the linear CDR.

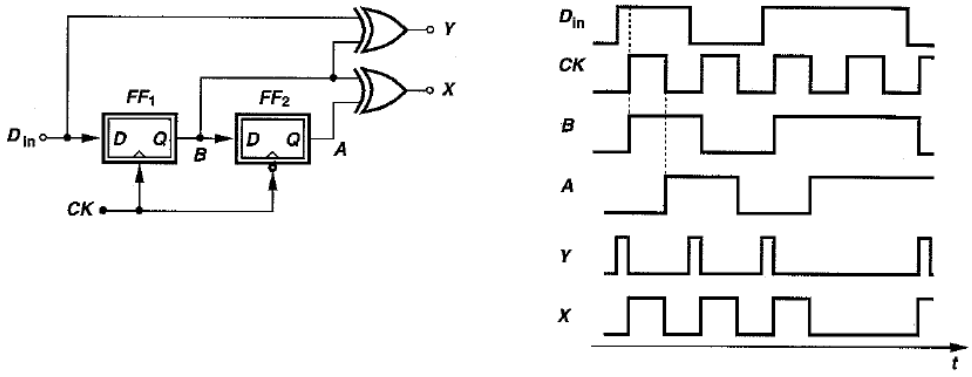

Figure 1.5: Linear (Hogge) phase detector

1.1.2 Bang-bang phase detector

This type of phase detector was invented by Alexander [10]. It produces a positive or negative pulse (UP or DOWN) which has one bit time duration. As seen in Figure 1.6, if we sample data at three points by consecutive clock edges, we can obtain the information if clock is early or late. When there is no data edge, no UP or DOWN pulses should be generated to prevent phase drifts during consecutive bits.

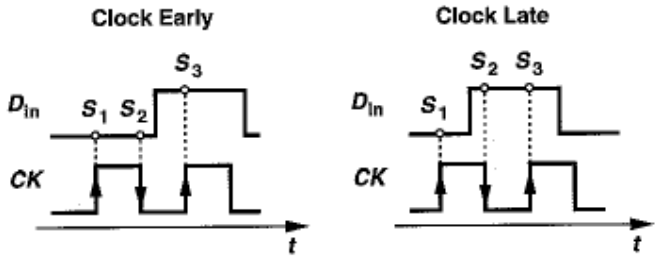

Figure 1.6: Clock position determination

Bang-bang PD can be implemented as shown in Figure 1.7 [9]. The sign of the transition sample (sampled by falling edge of clock, Q4) is compared with the previous (Q2) and the following bit (Q1). If it is different from the previous bit, this means that clock is late and an UP pulse is generated. If transition sample is different from the following bit, this means that clock is early and a DOWN pulse is generated. If all samples are the same, this means there is no data edge and UP,

DOWN signals become zero. If transition sample is different from both previous and the following bits, this means clock frequency is too low. This case is usually neglected in CDR design but UP and DOWN both become one in this case and the loop filter is not updated in a typical Current Mode Logic (CML) type charge pump. Truth table for the bang-bang PD is given in Table 1.1.

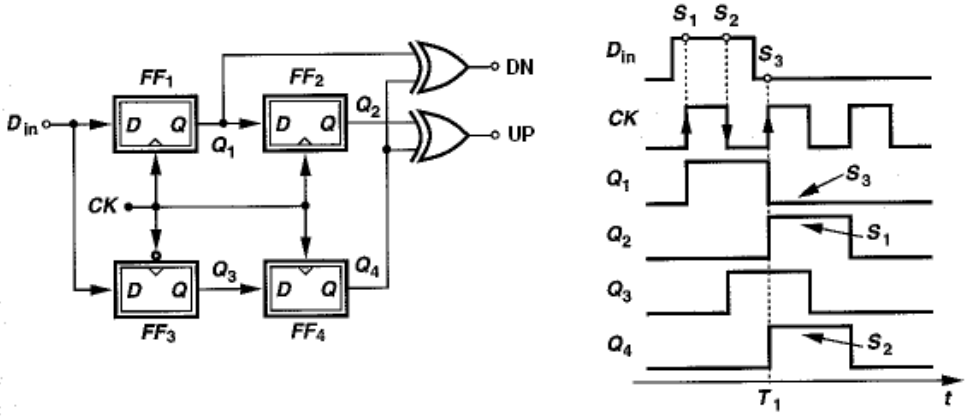

Figure 1.7: Bang-bang phase detector

Table 1.1: Truth table for the bang-bang PD

Case	S1	S2	S3	UP	DOWN	Meaning
0	0	0	0	0	0	Hold
1	0	0	1	0	1	Early
2	0	1	0	1	1	Hold
3	0	1	1	1	0	Late
4	1	0	0	1	0	Late
5	1	0	1	1	1	Hold
6	1	1	0	0	1	Early
7	1	1	1	0	0	Hold

An important advantage of bang-bang PD is that a conventional charge pump is not really needed because the PD has inherently a large gain at the transition point. This gain depends on the metastability region of the flip-flops. In metastability region flip-flop outputs cannot reach to full logical levels from the initially tracked voltage [2]. Therefore, special care should be taken in latch design since it directly effects the

jitter performance of the CDR. This behavior can be simulated by sweeping the phase of D and CK inputs of the flip-flop in small steps.

It is also possible to implement this PD with a half rate clock which has quadrature phases. This relaxes the VCO speed requirements in a given technology. Many half-rate phase detectors are proposed in the literature [2, 11-12]. The PD proposed in [11] does not have a hold mode: it suffers from large phase drift during consecutive bits. Whereas the PD given in [12] has less delay than the one proposed in [2] and this feature makes it attractive to reduce the inherent jitter generation of the CDR. Effect of minimizing loop delay on jitter generation and loop stability will be discussed later.

As depicted in Figure 1.9, quadrature phases (0^o and 90^o) of the clock sample the data. If rising edge of the CKI and CKQ samples different data, it means UP. If CKI falling edge and CKQ rising edge are different, it means DOWN (CKI and CKQ are 0^o and 90^o phases of the clock respectively).

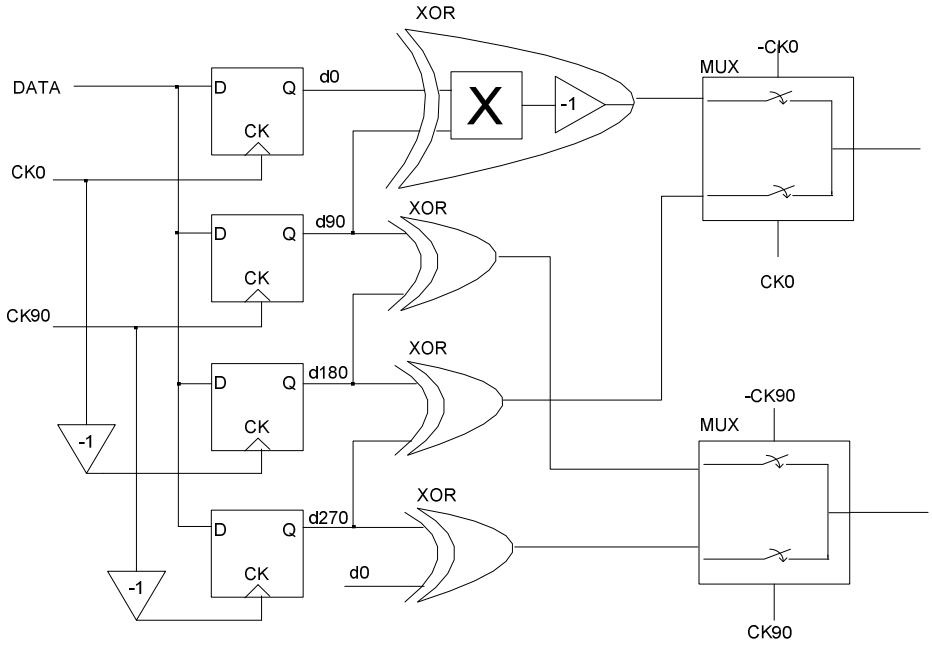

Figure 1.8: Phase detector single ended view proposed in [12]

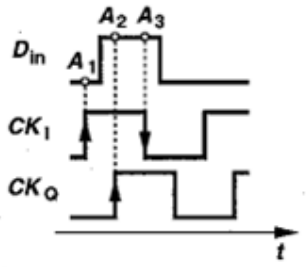

Figure 1.9: Quadrature phases of the clock sample the data in a half rate CDR design

1.2 CDR Loops

Having introduced the phase detectors, we can construct a CDR loop. Linear CDRs, which use linear (Hogge) phase detector, can be designed like classical PLLs. Their stability and jitter bandwidth can be analyzed using classical linear PLL equations. However, bang-bang loops are difficult to analyze using linear equations due to large non-linearity in the phase detector. Simplified equations, which were derived by Walker in [1], can help during the design but using time domain behavioral models is mandatory. A bang-bang loop can be constructed in two types as shown in Figure 1.10 and Figure 1.11. First one uses a conventional R-C loop filter whereas the second one uses a separate proportional path. In the second approach, phase detector output directly modulates the VCO around its center frequency. Actually, filter resistor R and separate proportional path do the same thing: They form a path proportional with the phase difference. Phase detector reacts to a phase difference and produces UP or DOWN pulses according to the sign of the phase error. These pulses move the VCO frequency in small amounts around the center frequency, which continues until the phase difference gets zero. In fact, phase detector continuously generates UP or DOWN pulses even in the locked condition but their average is zero. Proportional path is generally called “bang-bang branch” and charge pump with capacitor constitute the “integral branch”. Bang-bang branch responds to phase steps and slow integral branch provides the loop to remain in center frequency. When bang-bang loop responds to a phase step, integral loop also reacts. CDR is designed such that phase change due to the bang-bang branch dominates over the phase change due to the integral path. This is also required for stability, which will be discussed later in detail.

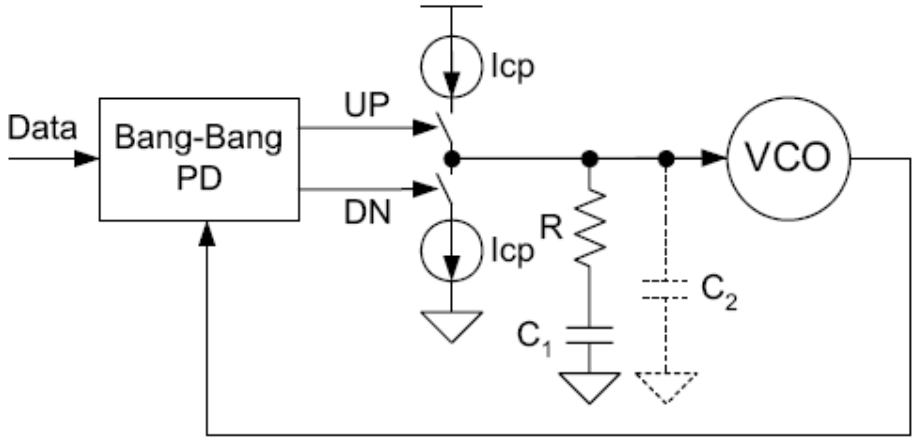

Figure 1.10: Bang-Bang Loop with R-C filter

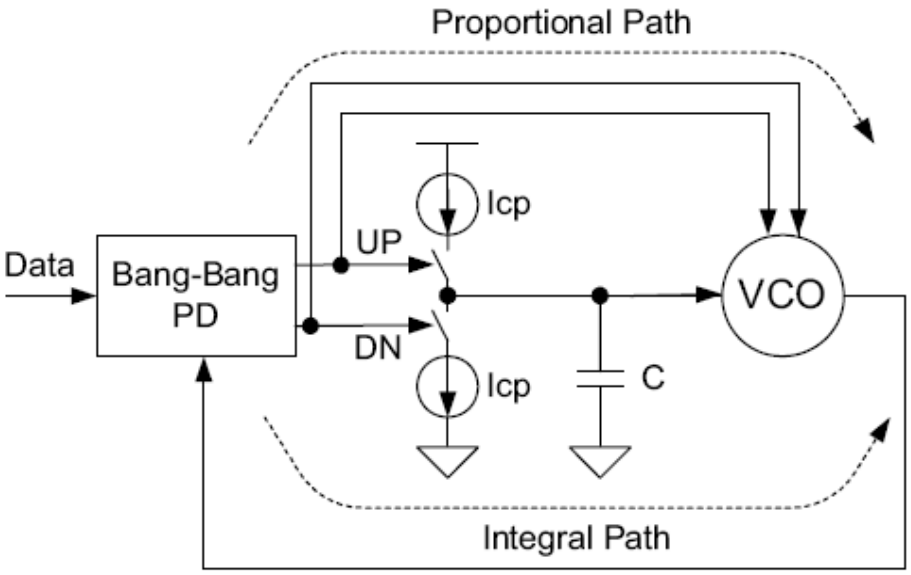

Figure 1.11: Bang-bang loop with separate proportional path which directly modulates the VCO

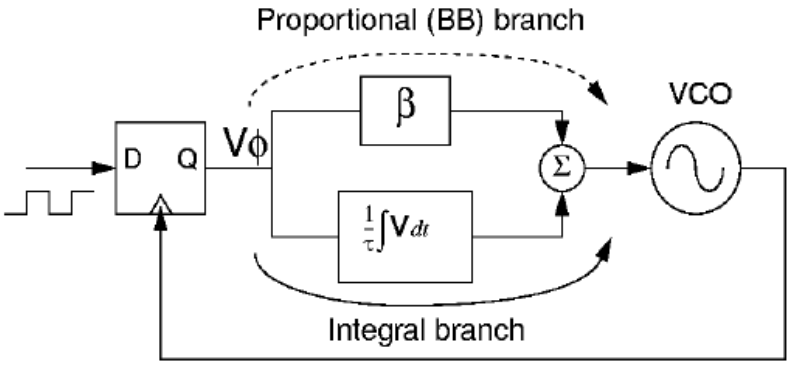

Figure 1.12- Another view of the bang-bang loop with separate proportional path

Bang-bang branch should have a high bandwidth for less jitter generation and better stability [1]. CDR loop with a conventional R-C filter cannot provide this feature because of C2 capacitance, which cannot be made too small. Therefore, R*C2 limits the bandwidth of the proportional path. Due to this fact, “separate proportional branch” method is usually employed in the bang-bang loop design. Design details of this kind of loops such as stability, jitter bandwidth and jitter generation will be presented in next section.

2. BANG-BANG PLL SYSTEM LEVEL ISSUES

A clock and data recovery circuit should meet some specs. These include stability, jitter tolerance and jitter generation. There are three independent system level design parameters: Bang-bang frequency step (F_{bang}), loop capacitor (C) and charge pump current (I). Jitter generation and jitter tolerance strongly depend on the bang-bang frequency step. Stability depends on all these parameters.

2.1 Stability

In fact, bang-bang PLLs do not converge to a final state. Frequency and phase of the output clock dither in the locked condition. According to [1] and [13], if the phase change due to the bang-bang path is higher than the phase change due to the integral loop in one bit time, system is stable.

Bang-bang path creates up and down frequency steps. If a VCO runs F_{bang} faster than its existing frequency for t_{bit} length, phase change can be calculated by integrating the frequency change for t_{bit} length.

$$\Delta\theta_{bang} = 2\pi F_{bang} t_{bit} \tag{2.1}$$

If an UP or DOWN pulse is received by the integral path, charge pump injects a positive or negative current to the loop capacitor. Control voltage of the VCO linearly rises to $Vc+I*t_{bit}/C$, where Vc is the initial control voltage, I is the charge pump current and C is the loop capacitor value. This frequency change should be integrated over t_{bit} update period to find the phase change due to the integral loop.

$$\begin{aligned} \Delta\theta_{\mathrm{int}\,eg} &= \frac{2\pi\Delta V \cdot t_{bit} \cdot K_{vco}}{2} \\ &= \frac{2\pi I \cdot {t_{bit}}^2 K_{vco}}{2C} \end{aligned} \tag{2.2}$$

K_{vco} is the VCO gain in Hz/V. Stability factor for a bang-bang loop is defined as the proportion of $\Delta\Phi_{bang}$ to $\Delta\Phi_{integ}$ by Walker [1]:

$$\xi = \frac{\Delta\theta_{bang}}{\Delta\theta_{\text{int}eg}} = \frac{2F_{bang}C}{I \cdot K_{v\text{co}} \cdot \text{t}_{bit}} \quad \textbf{(2.3)}$$

Stability factor, ξ, should be higher than 1 for the loop to remain stable.

In order to derive the equation above, assume that there is a finite phase difference but zero frequency error between data and clock, f_e=0, θ_e=θ. An UP or DN pulse is produced at the first transition to decrease the phase error; in the expense of frequency error. This frequency error causes phase accumulation until another transition arrives. The data transition density (D_T) can also be brought in the picture by noting that the phase accumulation due to the frequency error grows for lower D_T.

After the first data transition, the phase error decreases by $\theta_1=\Delta\theta$ ($\Delta\theta=\Delta\theta_{bang}$) and the frequency error increases to $\Delta\omega=I*t_{bit}/C$. After the next transition, the total phase error change is

$$\theta_2 = \theta_1 + \Delta\theta + \frac{1}{D_T}\Delta\omega T \quad \textbf{(2.4)}$$

The frequency error at this point increases to 2Δω. After the third transition the total phase error change is

$$\theta_3 = \theta_2 + \Delta\theta + \frac{1}{D_T}2\Delta\omega T \quad \textbf{(2.5)}$$

We can write the total phase change after n data transitions as:

$$\theta_n = \frac{1}{D_T}\sum_{k=1}^{n-1} k\Delta\omega T + \sum_{k=1}^{n}\Delta\theta \quad \textbf{(2.6)}$$

$$\theta_n = \frac{1}{D_T}\frac{n(n-1)}{2}\Delta\omega T + n\Delta\theta \quad \textbf{(2.7)}$$

When θ_n= θ, the phase error goes to zero, and the frequency error increases to nΔω. For the frequency error to diminish, n more steps are needed, and after n steps phase error becomes:

$$\theta^I = \frac{-1}{D_T}\frac{n(n+1)}{2}\Delta\omega T + n\Delta\theta \quad \textbf{(2.8)}$$

Assume that θ^I is negative, which means that loop will converge with some negative phase peaking. Now if $|\theta^I|<\theta$, which means that phase error envelope is reducing

during the lock operation, Figure 2.1, then the CDR loop is stable. $|\theta^{I}|$-θ must be less than zero:

$$\frac{1}{D_T} n\Delta\omega T - 2n\Delta\theta < 0 \qquad \textbf{(2.9)}$$

Hence, the stability factor and the stability criterion are defined as follows:

$$\xi = \frac{2D_T\Delta\theta}{\Delta\omega T} > 1 \qquad \textbf{(2.10)}$$

This equation, which is extracted in [13], is similar to the Walker's formula and D_T was inserted to the equation in this thesis.

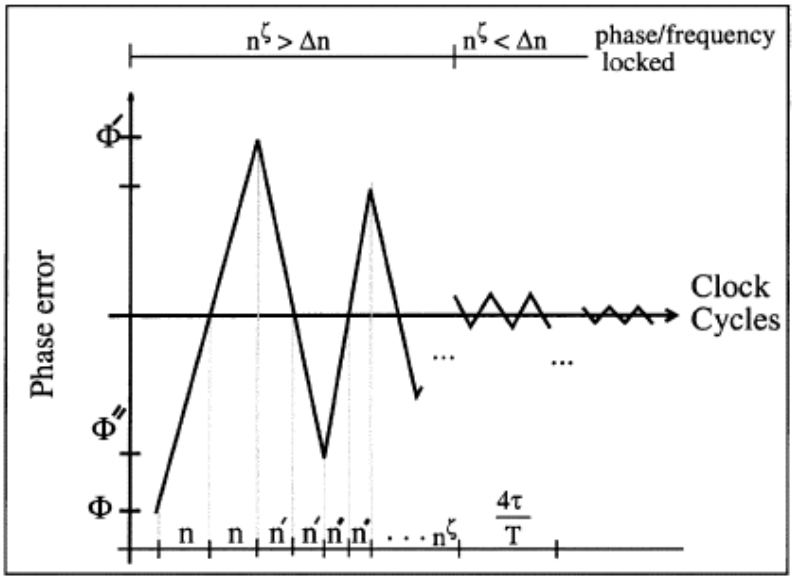

Figure 2.1: Phase error stabilization

CDR stability requires the phase change by the proportional branch to dominate the phase change by the integral branch. Figure 2.2 shows the phase stabilization process where C1 is the first clock with an initial phase error, θ. C2 is the clock after n data transitions. Its frequency is lower than the nominal frequency, but the phase error is 0 at t_0. After n more transitions the frequency offset between the nominal clock and C3 crosses zero at some point with a finite phase error, θ^{I}. This situation is similar to the initial state, if $|\theta^{I}|<\theta$ the loop converges.

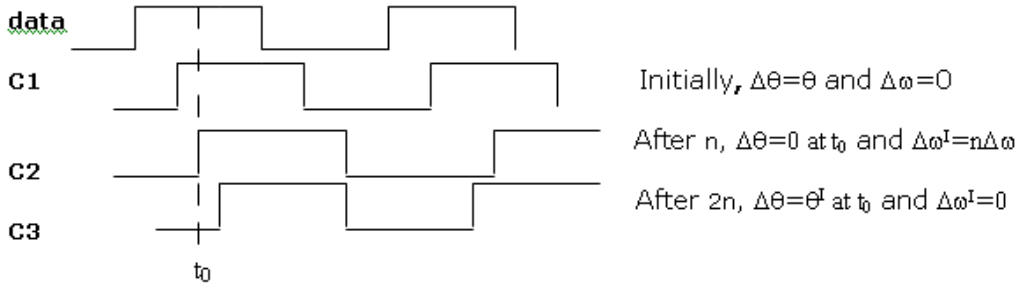

Figure 2.2: Data and clock signals during phase error stabilization for low damped loop

In some applications such as SONET, phase error peaking is critical because CDR circuits are repeated over long distances. If there is a peaking in one CDR characteristic, it accumulates through multiple CDRs. ξ is generally made greater than 1000 in these systems. If only one CDR will recover the data then peaking accumulation is not a concern. ξ is not made much larger than 100 in these systems because large ξ can slow down the response to frequency noise at the input. Additionally, transmitter clock frequency is modulated in some systems to reduce the EMI (Electromagnetic Interference) so large ξ is not preferred. Sometimes large VCO ranges cause large K_{vco} and this prevents to obtain a large stability factor without using off-chip capacitors.

2.2 Jitter Transfer

Bang-bang CDR loops have a jitter transfer function which changes with the input jitter amplitude. When input jitter is slow CDR closely tracks the input jitter. When the jitter frequency is too fast, loop generates UP signal for half cycle of the jitter period and DOWN signal for the other half cycle. This means CDR loop slews when the input jitter is large and at high frequencies (This is also called slope overload in [1]).

Figure 2.3 shows the extreme case that CDR is slewing due to the fast changing input jitter, [14]. VCO frequency is alternating between two points, $\omega_{center} \pm \omega_{bang}$. VCO output phase is the integration of its frequency so phase of the output clock is like a triangular wave. Peak value of the output phase can be calculated integrating the VCO frequency for $T_\Phi/4$ where T_Φ is the period of the input jitter.

$$\phi_{out,p} = \frac{\omega_{bang} T_\phi}{4} \tag{2.11}$$

Jitter transfer can be written as

$$\left|\frac{\phi_{out,p}}{\phi_{in,p}}\right| = \frac{\pi\omega_{bang}}{2\phi_{in,p}\omega_{\phi}} \tag{2.12}$$

where ω_Φ is equal to $2\pi/T_\Phi$. This equation is valid when the CDR loop slews. It depends on the input jitter amplitude because of slewing.

Bandwidth of the loop can be found approximately by extrapolating linear and slewing regimes, Figure 2.4 [14]:

$$\omega_{-3dB} = \frac{\pi\omega_{bang}}{2\phi_{m}} \tag{2.13}$$

Φ_m is the jitter amplitude value, $\Phi_{in}=\Phi_m\cos(\omega_\Phi t)$. Bandwidth is proportional with the bang-bang amount and is inversely proportional with the jitter amplitude, Figure 2.4. Transition density is ignored in [14]. If the phase detector is tri-stated when there is no data transition then VCO frequency does not stay at a constant frequency. It returns to the center in the absence of data transitions. Therefore, the above bandwidth formula should be multiplied by data transition density value for tri-state phase detectors.

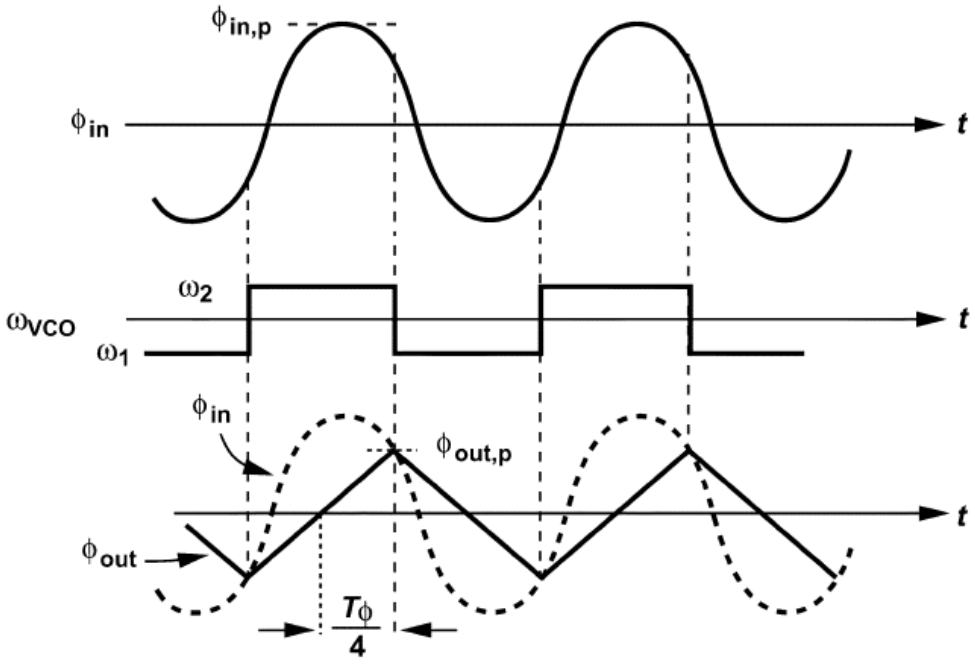

Figure 2.3: CDR slews for fast changing input jitter

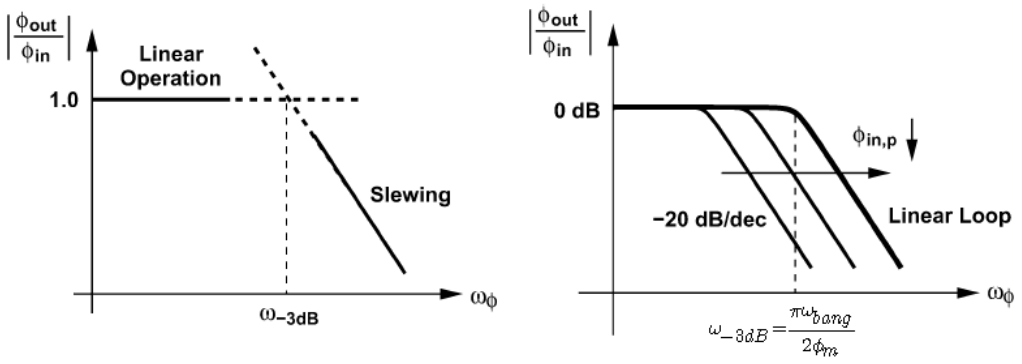

Figure 2.4: Calculation of jitter bandwidth and transfer function for different jitter amplitudes [14]

2.3 Jitter Tolerance

Jitter tolerance is defined as the maximum input jitter that a CDR loop can tolerate without increasing the bit error rate at a given jitter frequency [14]. This spec is generally given as a jitter mask, Figure 2.5. Sinusoidal jitter is added to the transmitter clock and the max jitter amplitude that meets the BER spec is recorded for a frequency. Frequency of the jitter is swept and points are interpolated. If the test results are above the mask, CDR meets the jitter tolerance specification.

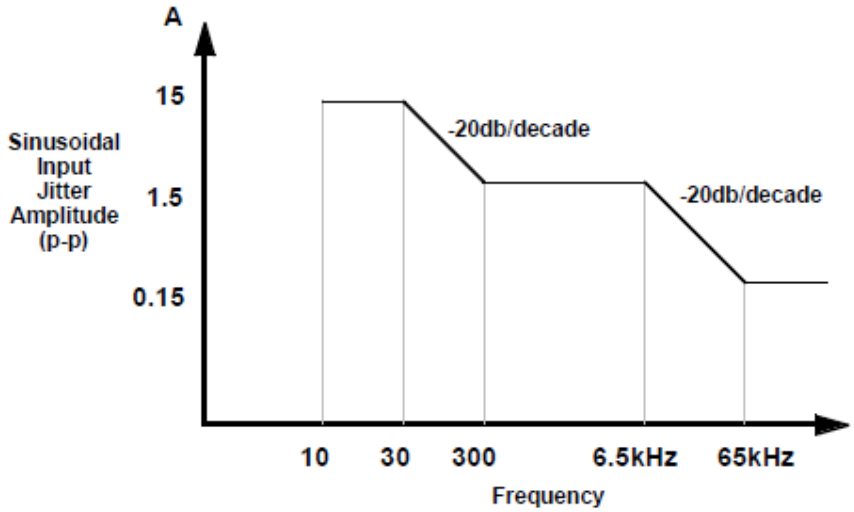

Figure 2.5: SONET OC-3 Category II Jitter Mask

At low frequencies CDR can track the large amplitude jitters. When frequency increases, CDR enters slewing regime and a difference occurs between the input and output phases, Figure 2.6. If the maximum difference, $\Delta\Phi_{max}$, is 0.5UI (half of the bit time), BER rises rapidly (sampling clock approaches the data edges). In a real implementation maximum tolerable difference can be less than 0.5UI because

of the jitter generated by the CDR loop, phase mismatches between the quadrature VCO phases and pulse width distortion in the data. In [14] G_{JT}, which shows the maximum jitter amplitude that CDR can tolerate, is calculated assuming $\Delta\Phi_{max}$ is 0.5UI:

$$G_{JT} = \pi\sqrt{1 + \frac{{\omega_{bang}}^2}{4{\omega_\phi}^2}} \tag{2.14}$$

G_{JT} falls at a rate of 20db/dec and approaches π at high frequencies (π=0.5UI). A corner frequency can be calculated by equating G_{JT} to π√2:

$$\omega_1 = \frac{\omega_{bang}}{2} \tag{2.15}$$

Typical jitter tolerance characteristic of a bang-bang loop is depicted in Figure 2.7. ω_1 was already calculated. It should be multiplied by data transition density value for tri-state phase detectors like the bandwidth. ω_2 occurs due to the voltage change in the loop capacitor during slewing [14]. Its value is not critical.

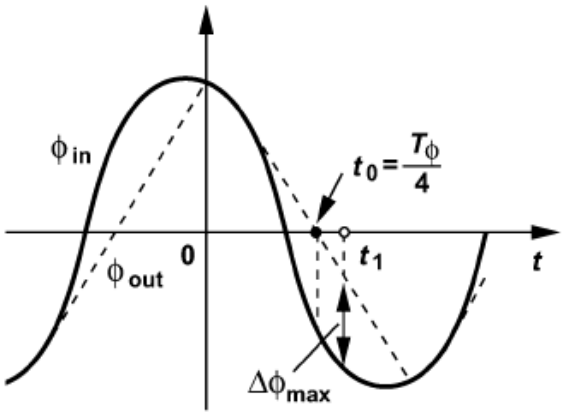

Figure 2.6: Slewing of a bang-bang CDR circuit during jitter tolerance test

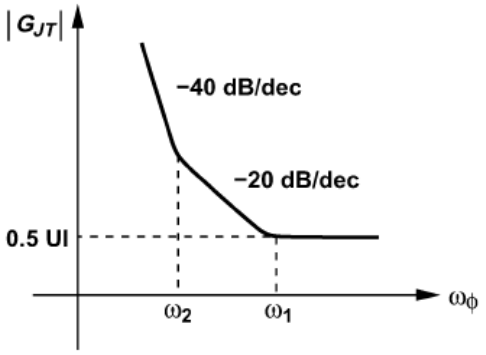

Figure 2.7: Jitter tolerance of a bang-bang CDR circuit

2.4 Jitter Generation and Loop Optimization

Bang-bang CDR loop can only produce UP or DOWN pulses so output phase will dither even if there is no jitter at the input and VCO is noiseless. This jitter is called hunting jitter. For one UP pulse VCO phase deviates:

$$\Delta\theta_{bang} = 2\pi F_{bang} t_{bit} \tag{2.16}$$

Large bang-bang amount, F_{bang}, causes large hunting jitter. Additionally, delays around the loop increase the phase error correction time and this causes larger hunting jitter. Therefore keeping the loop delay short is important for little jitter generation.

Large F_{bang} increases the jitter but jitter tolerance is directly proportional with F_{bang} only. Therefore minimum F_{bang}, which still satisfies the jitter tolerance spec, should be chosen, [2]. In [3], jitter bandwidth and jitter generation trade-off is shown graphically, Figure 2.8. To satisfy the jitter tolerance spec, bang amount should be higher than ΔF_{bb1} while it should be less than ΔF_{bb2} to meet the jitter generation spec. A bang amount between these points can be chosen to cover the process and temperature variations.

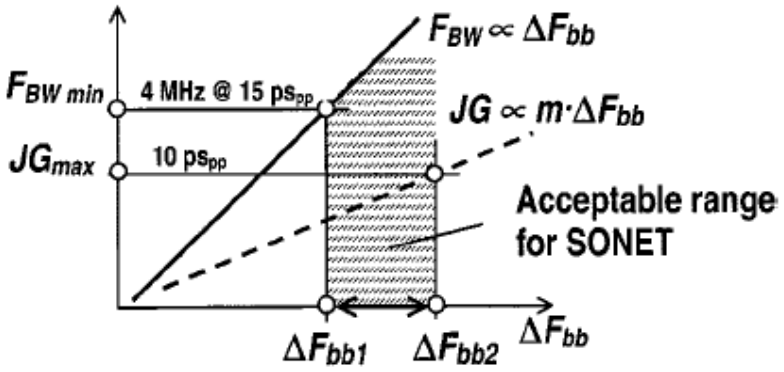

Figure 2.8: Jitter generation and jitter bandwidth trade-off

After choosing the bang-bang frequency step, we should determine the charge pump current and loop filter capacitor values. Stability factor was already calculated as

$$\xi = \frac{\Delta\theta_{bang}}{\Delta\theta_{\mathrm{int}\,eg}} = \frac{2D_T \cdot F_{bang} \cdot C}{I \cdot K_{v\mathrm{co}} \cdot \mathrm{t}_{bit}} \tag{2.17}$$

K_{VCO} depends on the VCO structure and the desired frequency range. It cannot be designed flexibly. If charge pump current is kept low, loop filter capacitor value can be decreased for the same stability factor. Minimum value of the charge pump current is limited with the leakage current values at its output.

3. CDR BEHAVIORAL MODELING

Clock and data recovery circuit was modeled in Spectre in order to run the system level simulations fast enough. We can insert a non-ideality to the model to see its effect on top level without simulating the circuit in transistor level. It is also useful for testing the performance of an individual loop component. For instance, a behavioral block can be replaced with its transistor level realization to see its contribution to output jitter. There are three major blocks in a CDR loop: Phase detector, VCO and charge pump.

Phase detector was modeled as depicted in Figure 3.1. Flip-flops were taken from Cadence behavioral library. They sample the data input at the clock threshold crossing time (e.g. at 0V). If the sampled value is greater than the given threshold it produces logic high and vice versa. -1V corresponds to logical low while 1V corresponds to logical high. XOR was modeled with a multiplier and an inverter. When one input is -1, output is equal to the other input. When one input is 1, output is equal to the inverted version of the other input. Multiplexer was implemented with two switches, which are controlled by complementary signals. Phase detector schematic view in Cadence is also depicted in Figure 3.2.

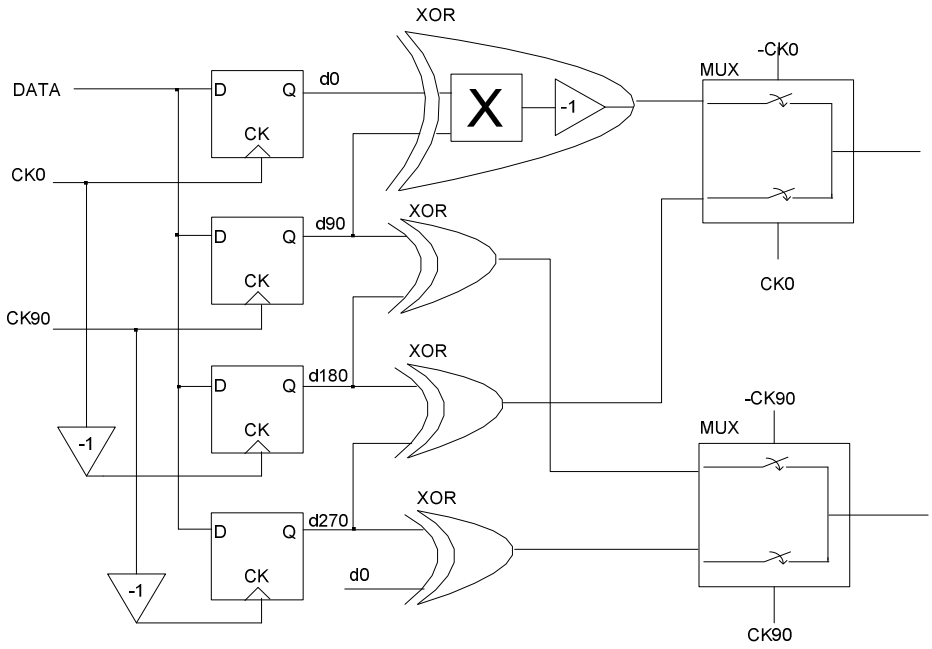

Figure 3.1: Phase detector model

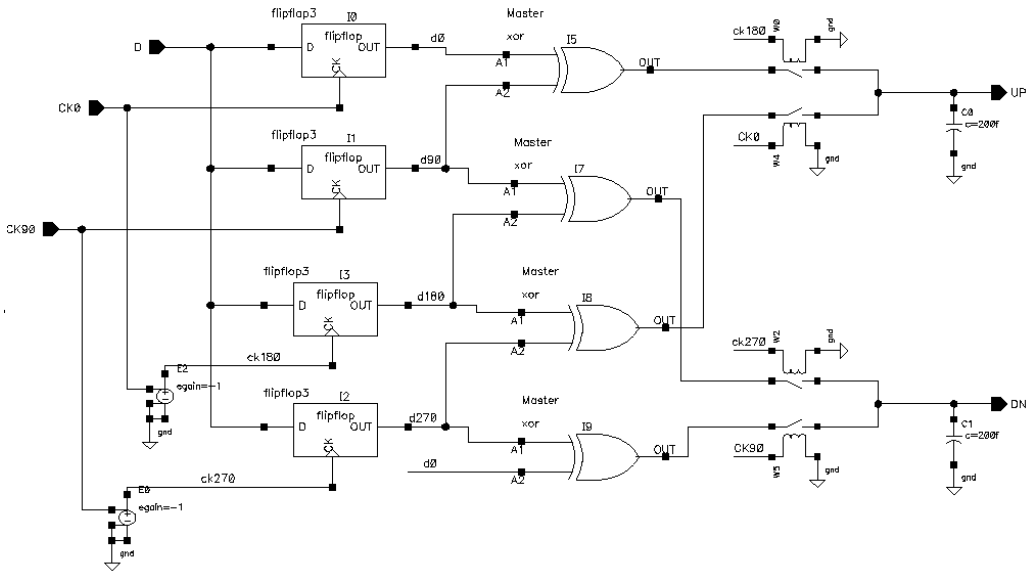

Figure 3.2: Phase detector schematic view in Cadence

VCO was modeled as shown in Figure 3.3. An oscillator core is available in Cadence behavioral library. K_{vco} and center frequency parameters can be entered for this block. It generates a clock signal which has a frequency $Vc*K_{vco}$. Our oscillator will have two control inputs: bang-bang and integral. Integral path keeps the frequency at data rate while bang-bang portion creates UP or DOWN frequency steps to adjust the phase of the clock. If UP=1 and DN=-1, positive frequency step is generated. If UP=-1 and DN=1, negative frequency step is generated. If UP and DN are equal frequency remains the same. To provide this, UP-DN voltage is applied to a transconductance stage which sources 1A when differential input crosses 0.1V and sinks 1A when differential input crosses -0.1V. This produces F_{bang}/K_{vco} voltage at transconductor output and Fstep frequency jumps at VCO output after being multiplied by K_{vco}. A low pass filter is cascaded to model the limited bandwidth of the bang-bang port of a real VCO. Then filter output is summed with the integral control voltage. Finally summing block output is applied to the control voltage of the behavioral VCO instance. It generates a sinusoidal signal. VCO output is differentiated to obtain quadrature VCO outputs. Two high gain amplifiers limit the sinusoidal VCO output and hence generate square wave signals. VCO model schematic view in Cadence is shown in Figure 3.4. Low pass filters and a few high value resistors (to prevent the convergence errors) are added to the models.

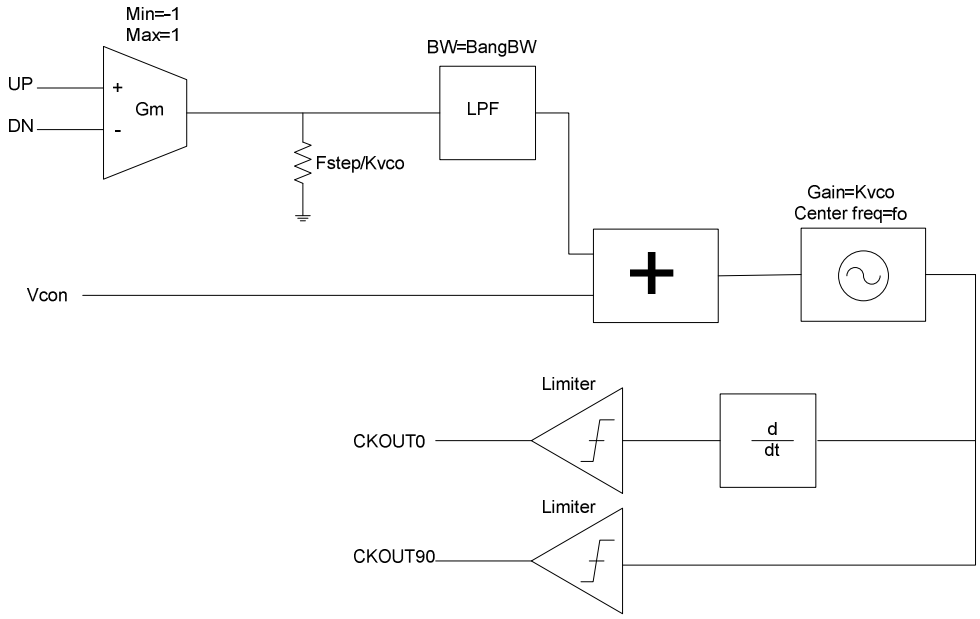

Figure 3.3: VCO behavioral model

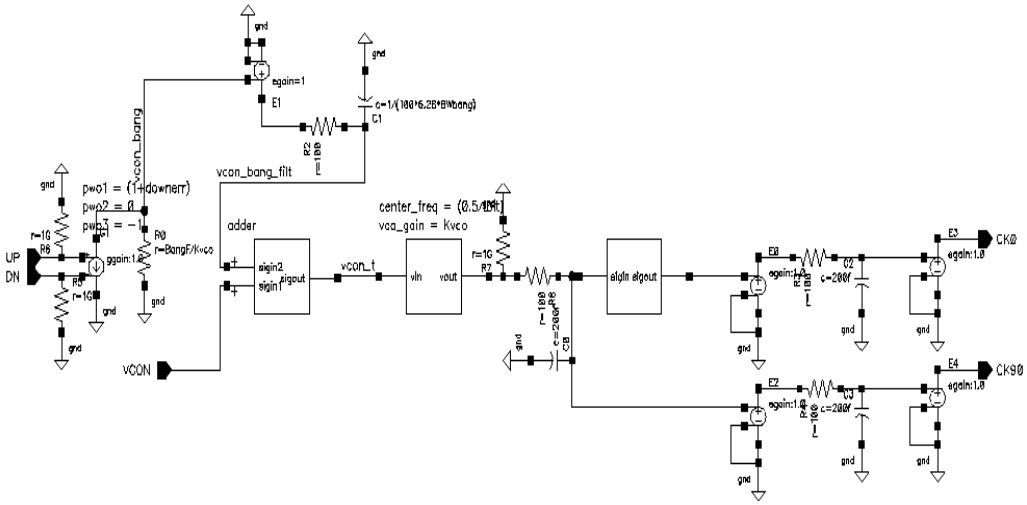

Figure 3.4: VCO model schematic view in Cadence

A charge pump can be modeled with a transconductor which sources current to loop capacitor when UP>DN and sinks current from loop capacitor when UP<DN. Complete loop model is depicted in Figure 3.5. Delay elements are also added to model the delay of the VCO buffer.

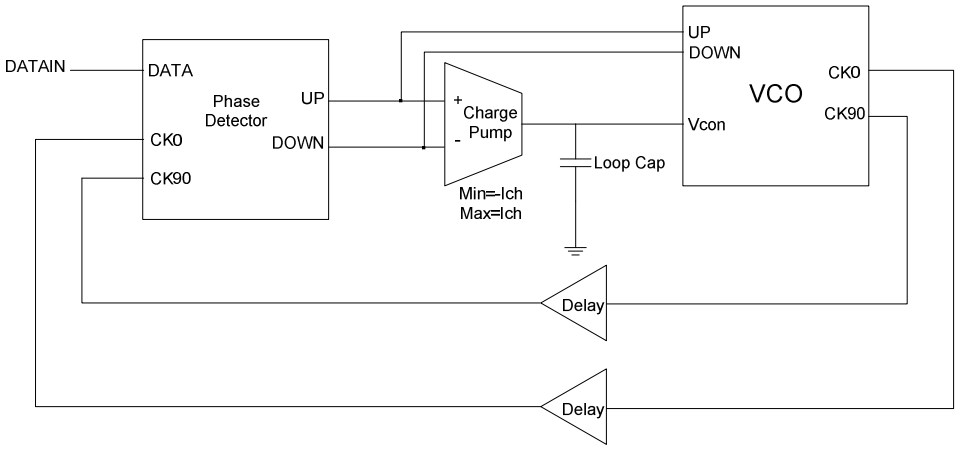

Figure 3.5: CDR model

3.1 Simulations

Simulations were run to test the implemented CDR model with a 5Gbs random data signal. Figure 3.6 shows the case when the VCO output is lagging the data signal. Transition sampling clock coincides with the data edges in the phase locked condition. As depicted in Figure 3.6, data sampling clock rising edge (cursor A) samples a different value than the transition sampling clock (cursor B), which causes phase detector to produce UP signal. Figure 3.7 shows the case when the VCO leads the data signal so phase detector outputs DOWN signal until transition sampling clock coincides with the data edges. Eye diagrams of data and clock signals after phase lock is achieved are depicted in Figure 3.8. Data sampling clock samples the data in the middle of the bit with a flip-flop having a zero setup time. Bang-bang frequency step is 10MHz in these simulations which means frequency is increased or decreased with an UP or DN signal by 10MHz instantaneously. This parameter plays a key role in determining the loop performance. If it increases loop corrects the phase steps much faster which means loop bandwidth gets higher. However, increasing the bang step increases the jitter which is inherently generated by the CDR loop in the locked condition. Figure 3.9 shows the clock eye diagrams for 3 different bang-bang frequency steps: 5, 10 and 15Mhz. Jitter increases almost linearly with the bang steps.

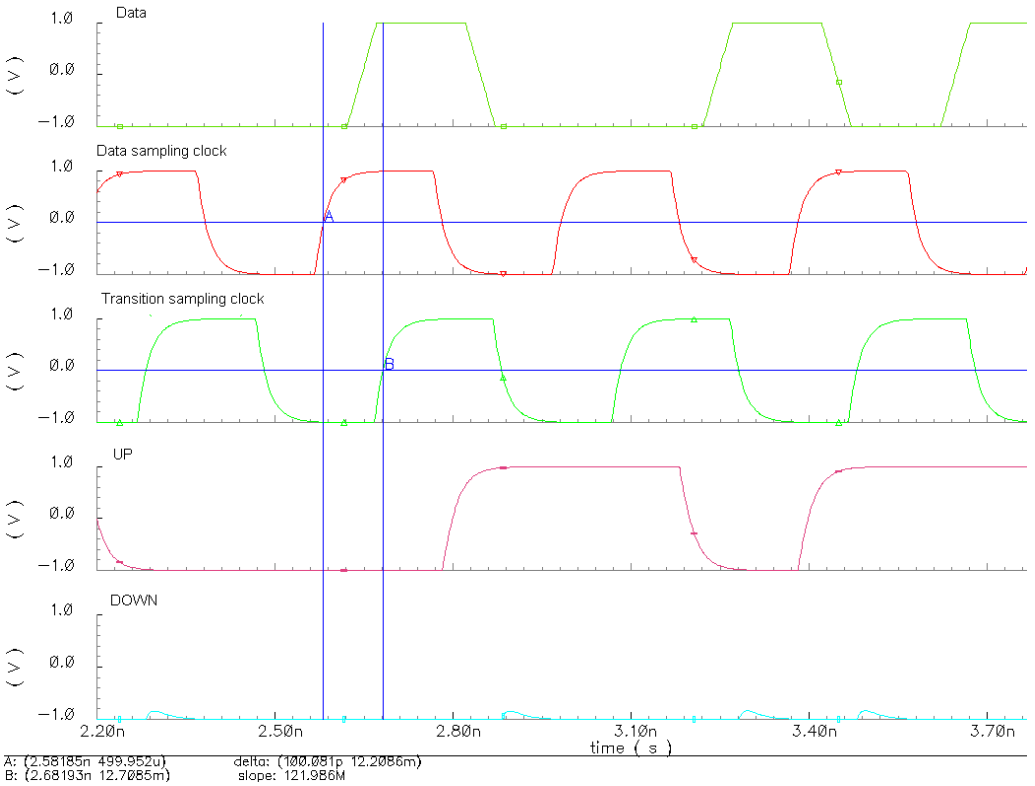

Figure 3.6: UP generation

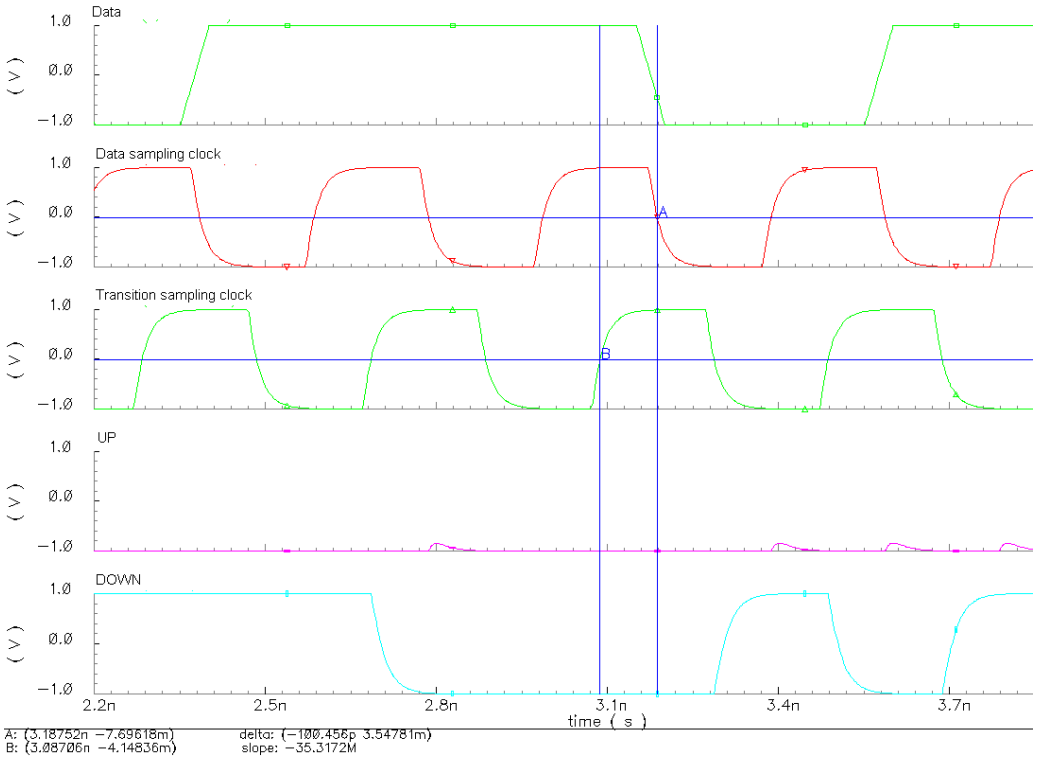

Figure 3.7: DN generation

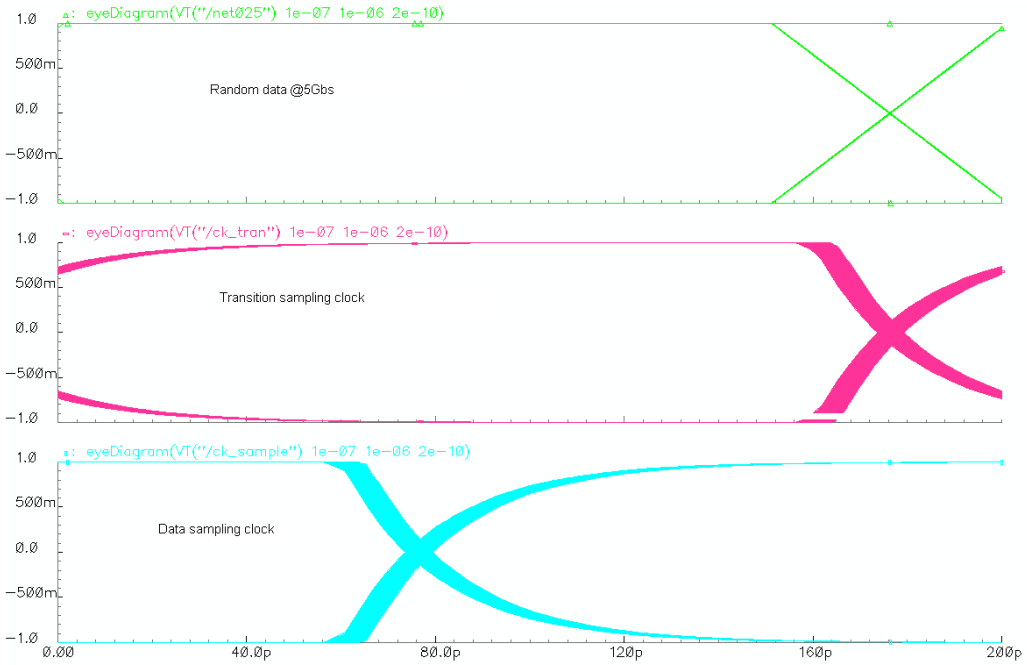

Figure 3.8: Eye diagrams of data and quadrature phase clocks

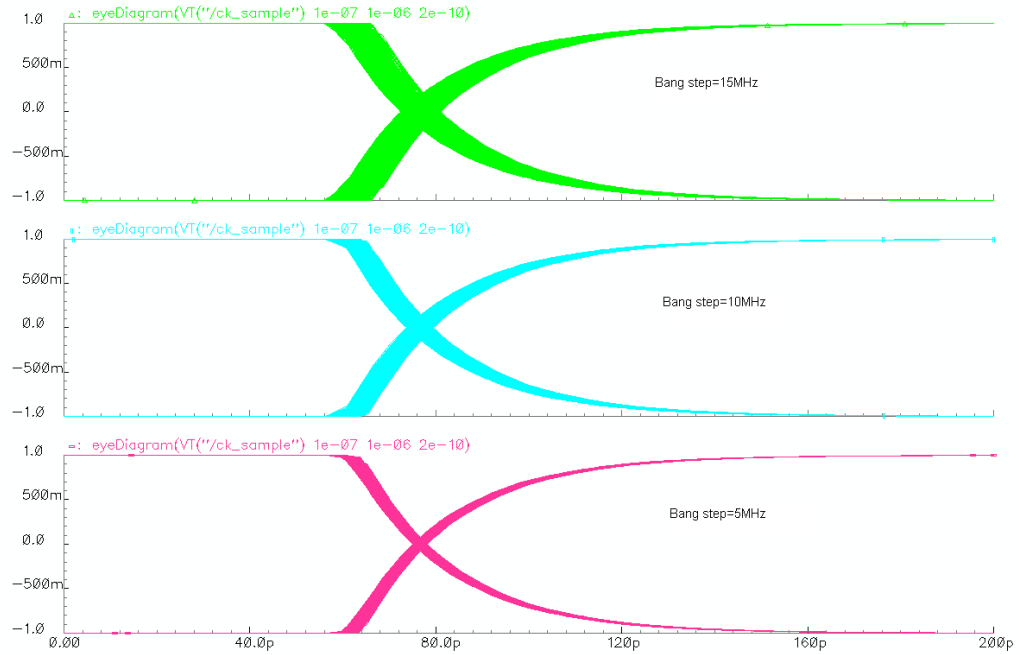

Figure 3.9: Eye diagrams for different bang-bang frequency steps

3.1.1 PRBS Circuit

7-bits and 15-bits ideal PRBS circuits were designed to test the different cases with the same data pattern. Schematic of 7-bits PRBS circuit is shown in Figure 3.10. Last two bits are XNOR'ed and applied to the input of first flip-flop. If all FF outputs get high, PRBS circuit is stuck. Therefore, FF outputs are set to zero initially. Maximum run length is 7 bits for this PRBS circuit. Flip-flops were taken from Cadence library and their initial values are set with the capacitors at the output.

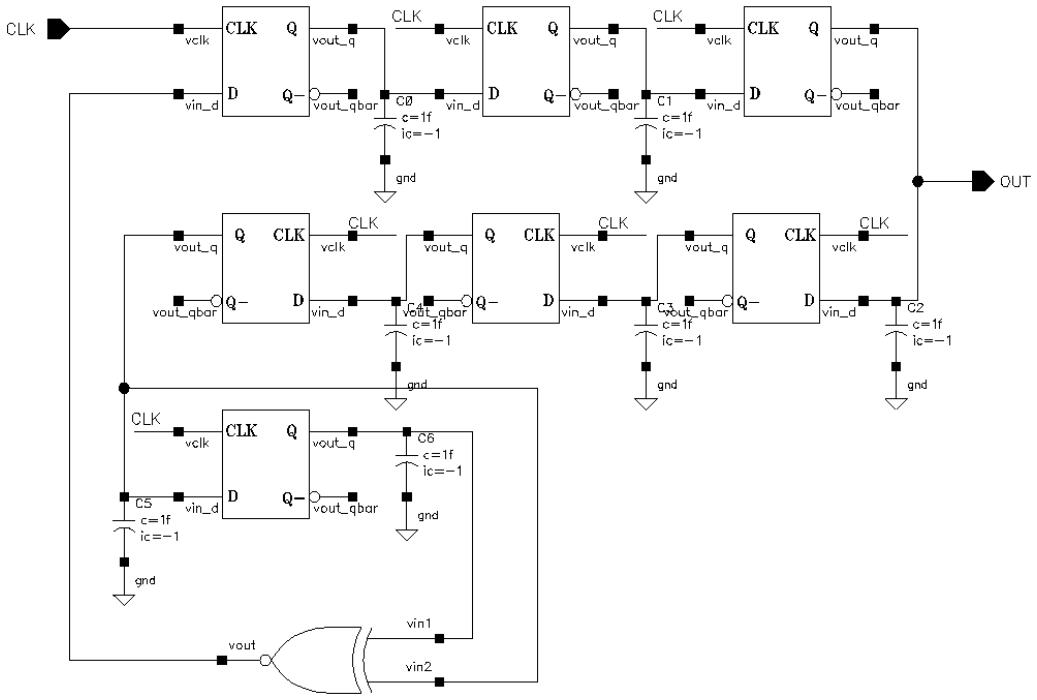

Figure 3.10: 7 bit PRBS circuit

3.1.2 Jitter Measuring Circuit

Eye diagrams are useful for observing the long term jitter but we cannot measure the jitter for a specific time looking at the eye diagram. To measure the jitter over time the transmitter clock edges are compared with the recovered clock. This is done with a circuit and the output voltage of this circuit gives the jitter, Figure 3.11. If we charge a capacitor with a current equal to the value of the capacitor, capacitor voltage gets equal to the time value. When transmitter clock rises and recovered clock rises and falls, time values at these transition points are sampled. Then difference of these time values are taken and it is sampled with a delayed version of the transmitter clock. In Figure 3.11, rising and falling edges of the recovered clock are compared with only the rising edges of the transmitter clock since this is a half rate architecture.

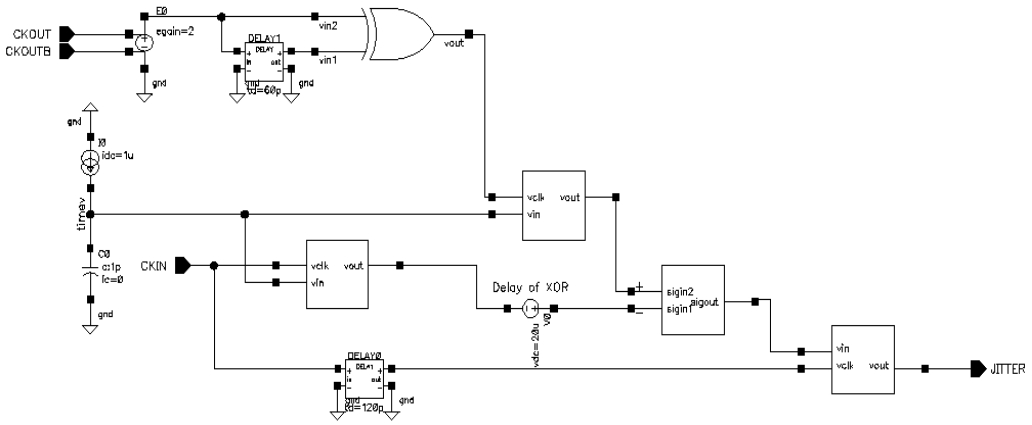

Figure 3.11: Jitter measuring circuit

Bang port bandwidth of the VCO and delays in the loop cause hunting jitter to increase. In Figure 3.12 and Figure 3.13, simulation results for different bang port bandwidths and loop delays are depicted.

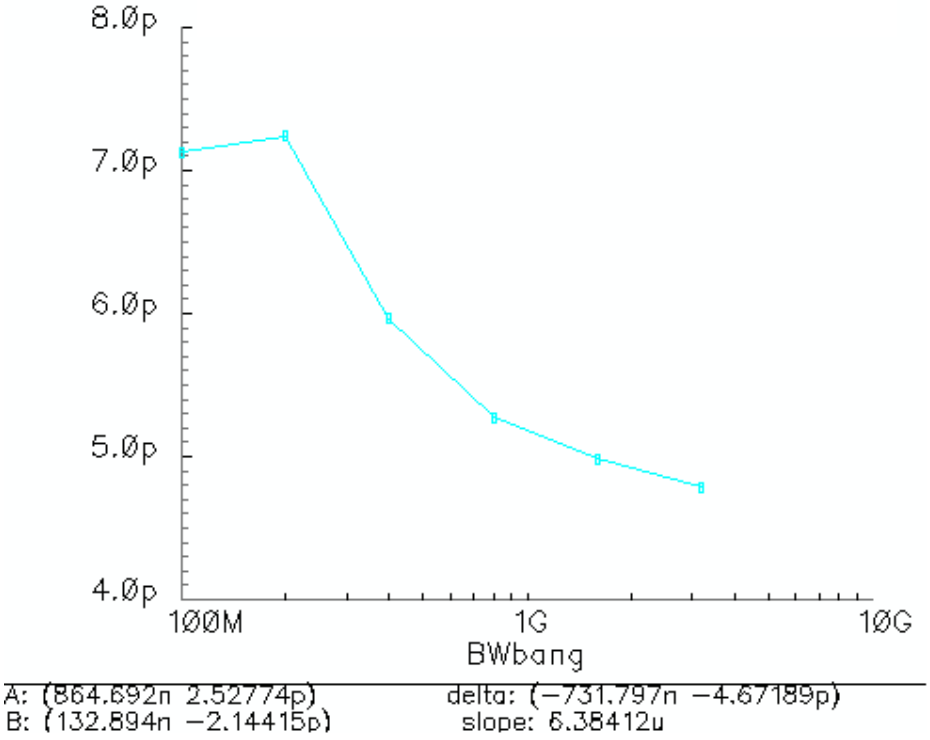

Figure 3.12: VCO bang-bang port bandwidth and hunting jitter relation

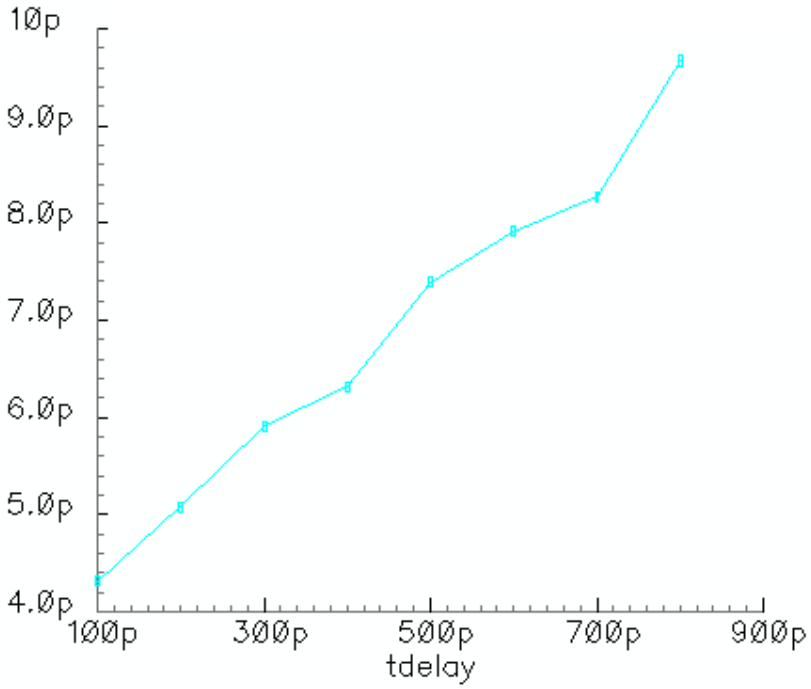

Figure 3.13: Loop delay and hunting jitter relation

4. DESIGN OF LOOP COMPONENTS

4.1 Phase Detector

Half-rate phase detector proposed in [12] was implemented due to its symmetric structure and low latency features. Its block diagram is shown in Figure 4.1. Although, signals are shown single-ended in this figure, circuit implementation is fully differential. PD consists of flip-flop, XOR and MUX gates. These logical elements are designed with CML type logic.

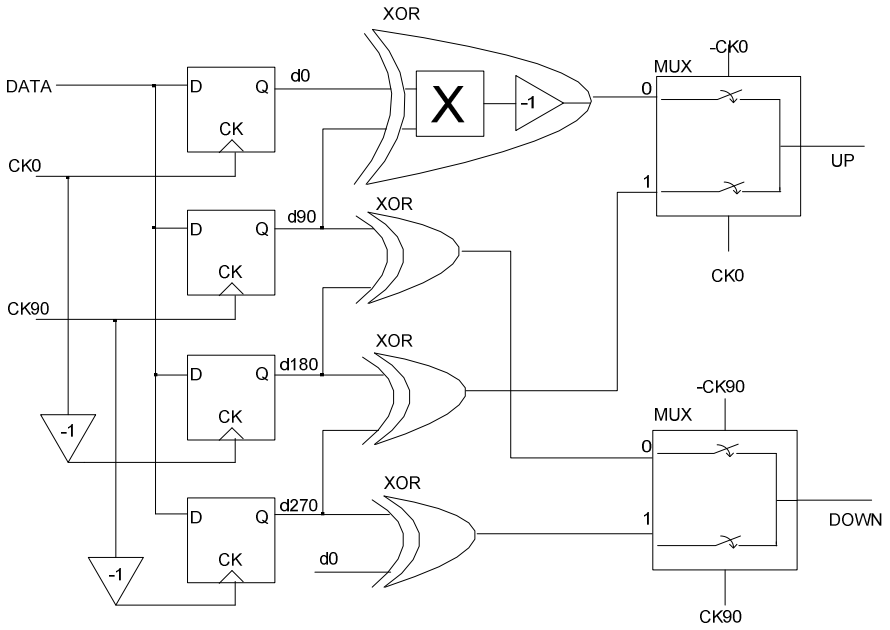

Figure 4.1: Half-rate phase detector structure

Flip-flop consists of master and slave latches as shown in Figure 4.2. When CK is low, master latch tracks the data signal (transparent phase) whereas slave latch keeps the last input latched by the master. When CK goes high, the master latches the data and the slave gets transparent. Therefore, flip-flop samples the data with the rising edge of clock. Major features of a flip-flop such as set-up time, metastability and hysteresis are determined by master latch whereas the slave latch affects the time delay from clock input to output.

CML type latch circuit is depicted in Figure 4.3. When CLK is high, latch tracks (or amplifies) the input. When CLK is low, bias current is fully steered to cross-coupled

devices, which form a positive feedback loop. This loop amplifies the tracked voltage and produces a full level logical signal at the latch output. Metastability and hysteresis of master latch increase the jitter generation of a bang-bang CDR [3]. Metastability occurs when data edges get close to the clock sampling edge. Therefore, flip-flops, which sample the data with the transition sampling clock (CK90), suffer from metastability. Tracked output voltage gets small and so positive feedback cannot produce a full-level logical signal in the desired time. Minimum time required to latch an initial voltage V_0 can be approximately given by [2]

$$T_{latch} = \frac{R_L C_L}{g_m R_L - 1} \ln\left(\frac{V_{full}}{V_0}\right) \quad \textbf{(4.1)}$$

g_m is the transconductance of cross-coupled devices and V_{full} is the final logical value. gm cannot be increased too much because larger gm reduces the bandwidth of the latch in tracking mode. Low bandwidth of the latch increases the pattern dependent jitter (hysteresis) [2]. This tradeoff is overcome by sizing the master latch larger than the slave, which reduces the output loading of master by slave [2].

This method (reverse scaling) is also used in this project, where master latch is made two times larger than the slave, Figure 4.2. Tail currents of master and slave latches are 900uA and 450uA respectively. Output swing amplitude is chosen 600mV. This is the maximum voltage that differential pair still operates in saturation when current is fully steered in one direction. Differential pair overdrive voltage should be around 300mV (when inputs are balanced) to fully steer the differential pair current when differential input is high or low (Amplitude is 600mV). Higher overdrive voltages reduce the maximum operating frequency of the latch.

XOR schematic is shown in Figure 4.4. This is a Gilbert cell, which multiplies the two inputs. Let us label the two inputs of XOR with IN1 and IN2. Basically, an XOR gate inverts IN2 when IN1 is high and buffers IN2 when IN1 is low. The circuit in Figure 4.4 implements this function differentially. When IN1 is high (IN1>IN1B), gain from IN2 to the output is negative whereas the gain is positive when IN1 is low. Tail current of XOR circuit is 300uA and the output swing is 600mV.

MUX schematic is shown in Figure 4.5. When SEL is high (SEL>SELB), the differential pair on the left is ON and the right is OFF, which means IN1 input is selected . When SEL is low (SEL<SELB), IN2 input is selected. Tail current of MUX circuit is 300uA and the output swing is 600mV.

Phase detector simulation results are depicted in Figure 4.6 and Figure 4.7. CK0 and CK90 are data and transition sampling clocks respectively. When CK90 makes a transition later than data edge, phase detector produces UP signal. When CK90

makes a transition earlier than data edge, PD produces DOWN signal. A and B cursors show the zero crossing points of CK90 and data respectively.

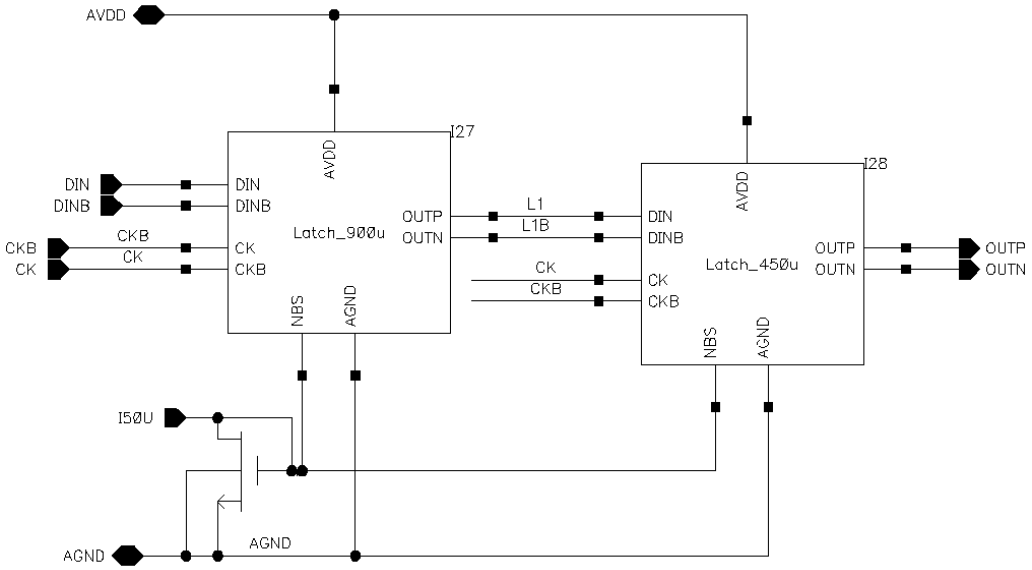

Figure 4.2: Flip-flop schematic

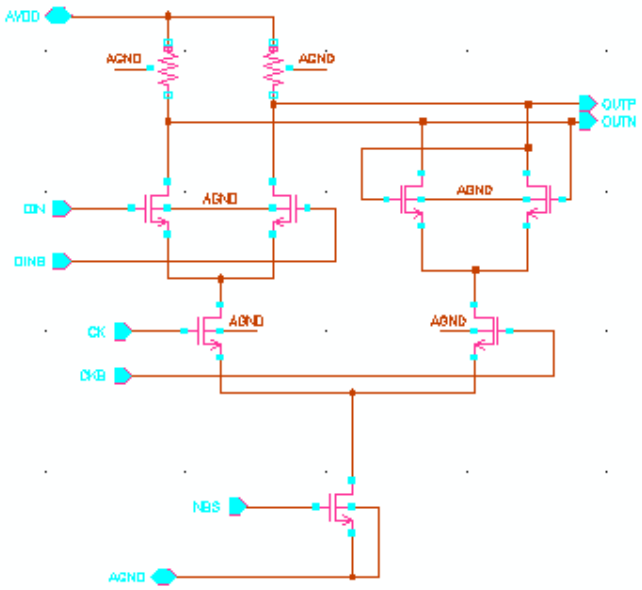

Figure 4.3: CML type latch circuit

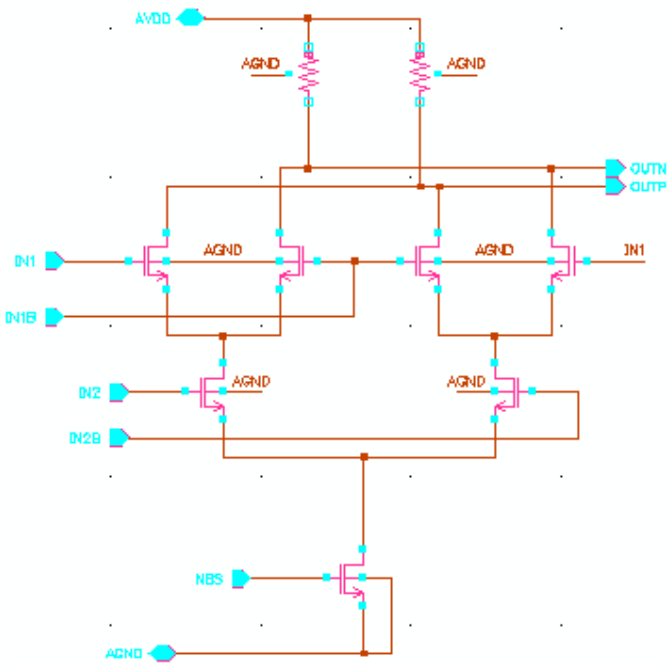

Figure 4.4: CML type XOR circuit

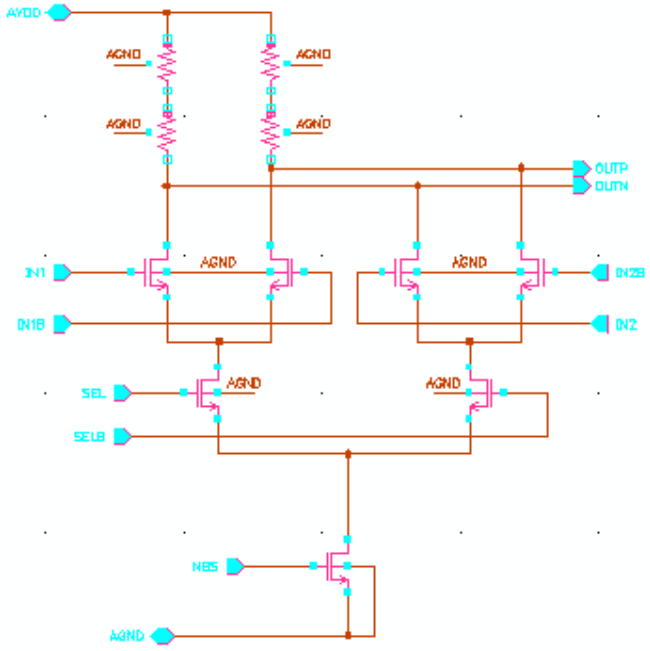

Figure 4.5: CML type MUX circuit

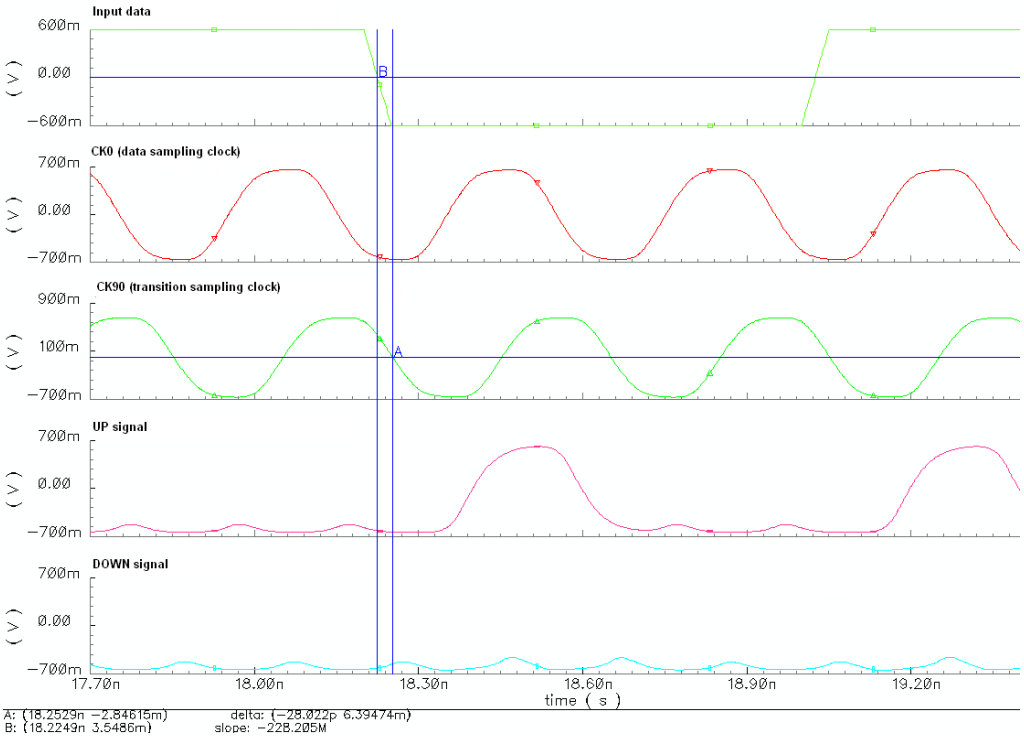

Figure 4.6: Phase detector generating UP signal

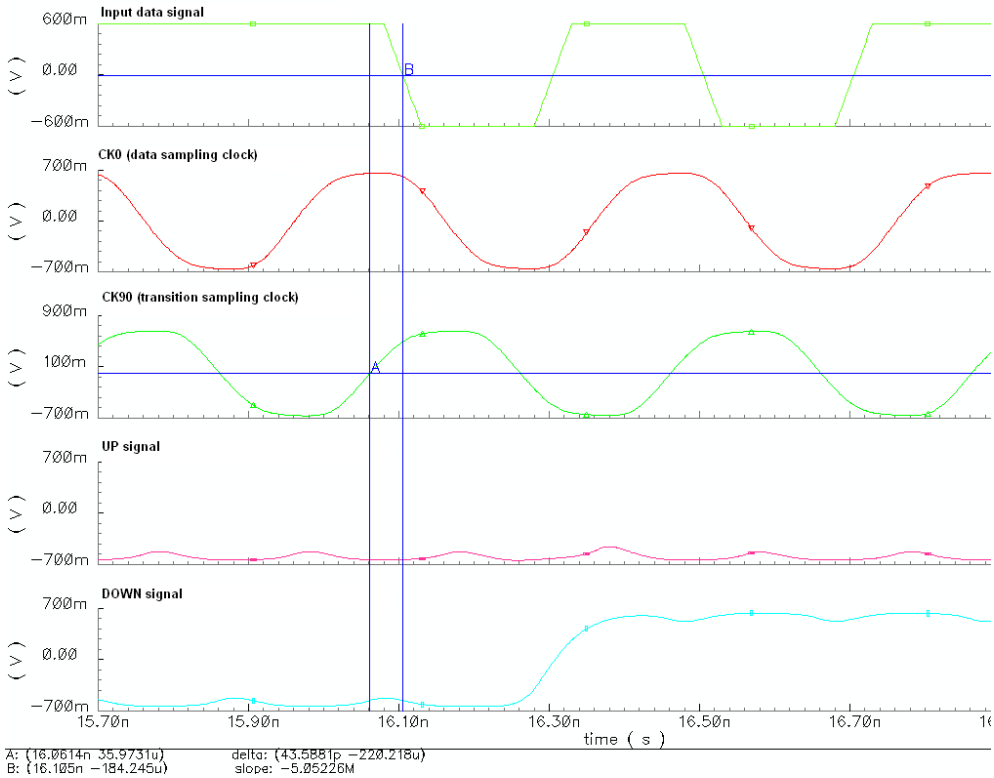

Figure 4.7: Phase detector generating DOWN signal

4.2 Charge Pump

Charge pump is a current steering differential circuit, which is depicted in Figure 4.8. MNBS1 and MNBS2 are NMOS current sources whereas MP1 and MP2 are PMOS current sources. All these sources have the same current, Ibs, in saturation region. When UP is high and DOWN is low, MN1 and MN3 are OFF so a current equal to Ibs is sourced to output. When UP is low and DOWN is high, MN1 and MN3 are both ON so a current equal to Ibs is sunk from output. This circuit has two differential outputs but only one output is used. Unused output is driven to the same voltage as the output in use via a voltage follower OPAMP. This method prevents the drain voltages of MNBS1 and MNBS2 to deviate too much when UP or DOWN signals steer the tail current in either directions. If unused output is left floating, it can go to some voltage which puts the differential pair transistors into triode region. Then drain voltages of NMOS current sources experience significant voltage changes, which causes additive displacement currents at the output. OPAMP of the voltage follower is a single stage with active loads, Figure 4.9.

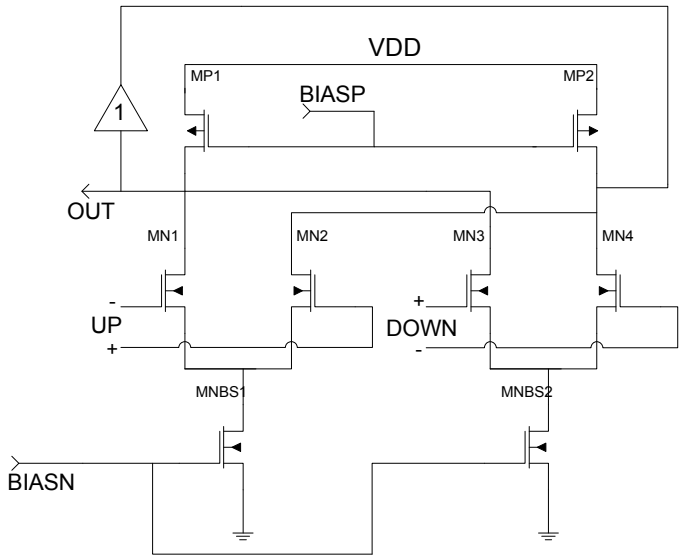

Figure 4.8: CDR charge pump circuit

Output current of the charge pump is visualized in Figure 4.10, where UP and DOWN pulses are sent at 10ns in two different simulations. In another simulation output voltage of the charge pump is swept in DC analysis for UP and DOWN cases. Its result is shown in Figure 4.11: It seems like charge pump circuit can reliably operate for control voltages between 0.8 and 1.45V. For large output voltages PMOS current source enters triode region and for low voltages differential pair transistors leave the saturation region.

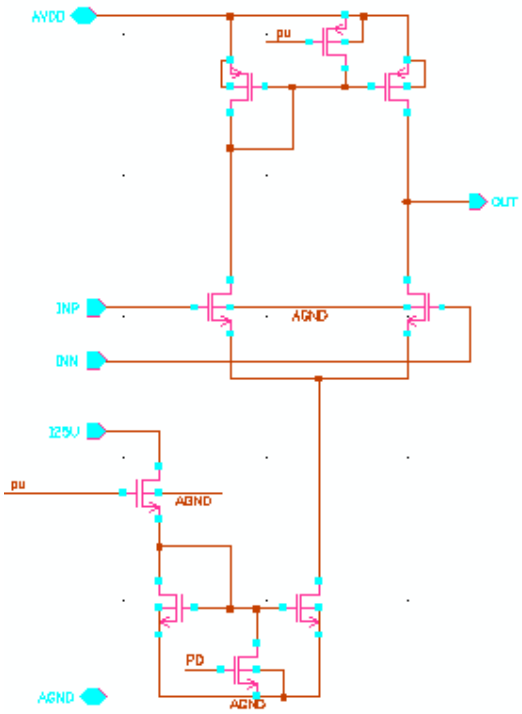

Figure 4.9: OPAMP circuit used in the voltage follower of charge pump

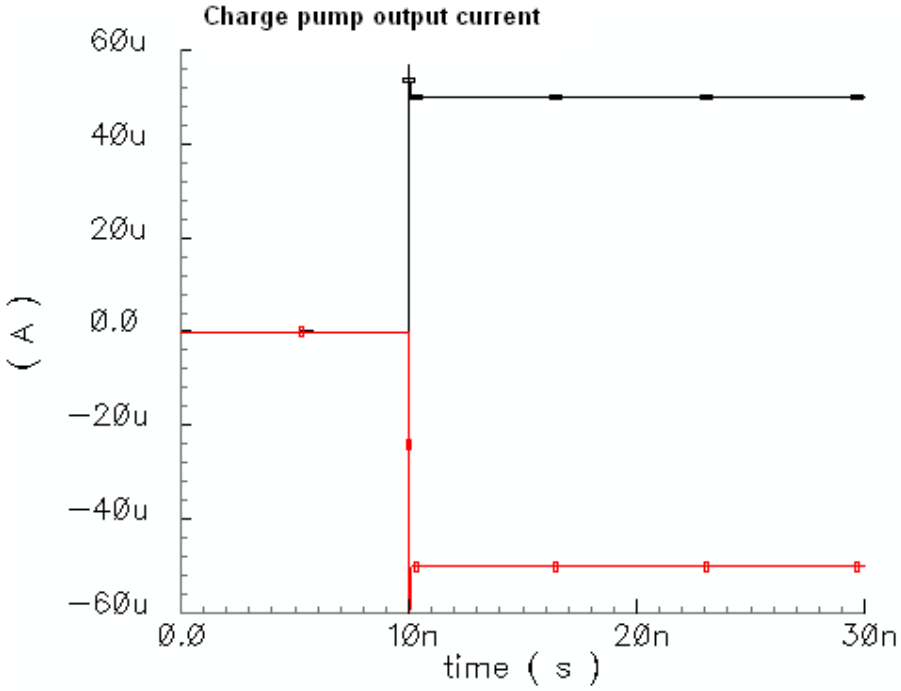

Figure 4.10: Charge pump output current transient behavior

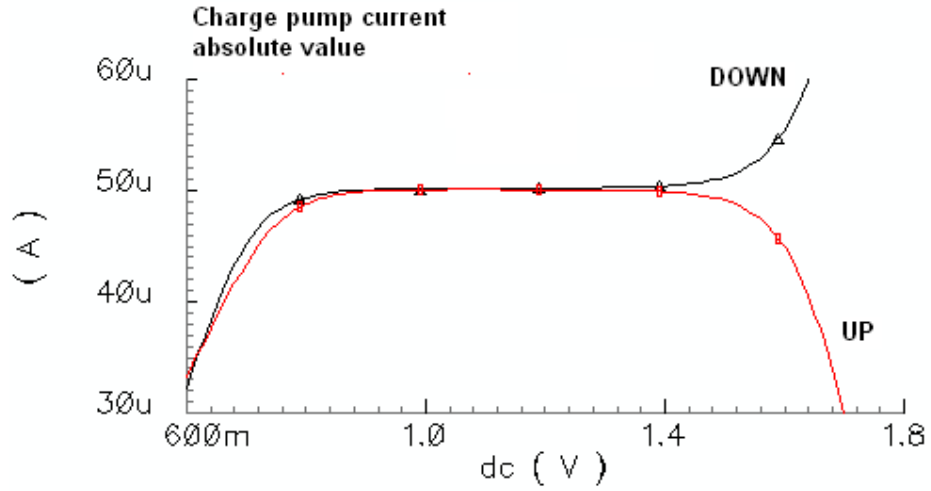

Figure 4.11: Charge pump output current variation when output voltage is swept

4.3 VCO

Differential ring-type oscillators are usually preferred to LC oscillators in mixed-signal applications due to their less area. Additionally, on-chip inductors are sensitive to the capacitively coupled substrate noise and magnetically coupled noise from noisy supply bondwires [15]. Nonetheless, LC structures become mandatory when a ring oscillator design cannot meet the speed and phase noise specifications.

In a PLL loop, phase noise components, which are at lower frequencies than the PLL bandwidth, are attenuated by the loop. Beyond the PLL bandwidth, phase noise of the loop is almost equal to the phase noise of the VCO. Jitter is more meaningful in some applications such as clock and data recovery circuits. Integration of the PLL phase noise gives the long term jitter. High loop bandwidth gives less phase noise area and hence less jitter. This calculated jitter number is an rms value. It should be multiplied by a factor according to the desired bit error rate (BER). This factor is equal to 14 for less than 10^{-12} BER. This discussion reveals that a loop can be designed with a very low jitter by employing a high bandwidth although noisy ring oscillators are used in the design.

Differential delay cells are usually preferred due to their better substrate and supply noise suppression. A general representation of a differential delay cell is shown in Figure 4.12. Loads should be controllable to tune the VCO frequency. A PMOS operating in the triode region can serve as a load element. However, there is an important point for supply noise suppression: loads should be symmetrical about the mid-point of the voltage swing. If the instantaneous resistance of the differential load elements is not equal when the complementary outputs are swinging, noise at Vcc will be coupled to complementary outputs with unequal amounts. Unequal noise

components at differential outputs will change the zero crossing time of the next stage and hence cause jitter. Therefore, loads should be symmetrical about the mid-point of the voltage swing to increase the dynamic supply noise suppression.

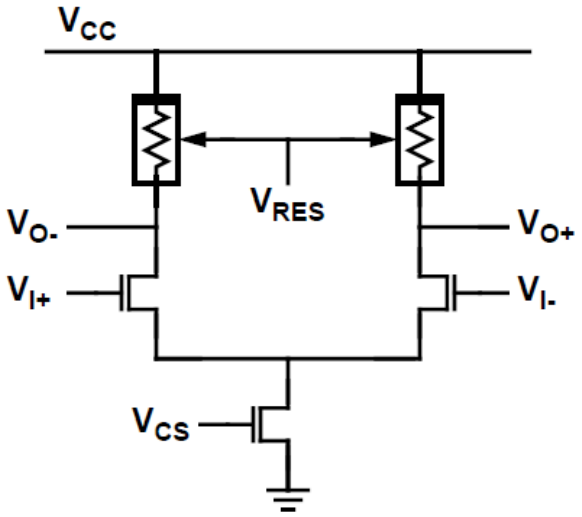

Figure 4.12: A general view of a differential delay cell [16]

A symmetric load element is proposed in [16] realized with MOS transistors and is shown in Figure 4.13. A symmetric load element consists of a diode connected and another same size PMOS device in shunt. Control voltage is applied to the gate of the PMOS device. I-V characteristics of the symmetrical load for two different control voltages are depicted in Figure 4.14. I-V curves are symmetric around the half of the control voltage which means that output should swing between Vcc and Vcc-Vctrl to utilize the load symmetry feature. Voltage swings are defined with the current bias transistor of the delay cell. When current is fully steered to one side, node voltage of the corresponding output should be equal to Vdd-Vctrl. One way is to employ a feedforward method, Figure 4.15. A feedback circuit adjusts the gate voltage of the NMOS device (replica of the bias transistor) such that the voltage drop across the replica of the symmetric load is equal to Vcc-Vctrl. Opamp output also drives the bias transistors in delay cells, which means that symmetric loads are biased at the symmetry point.

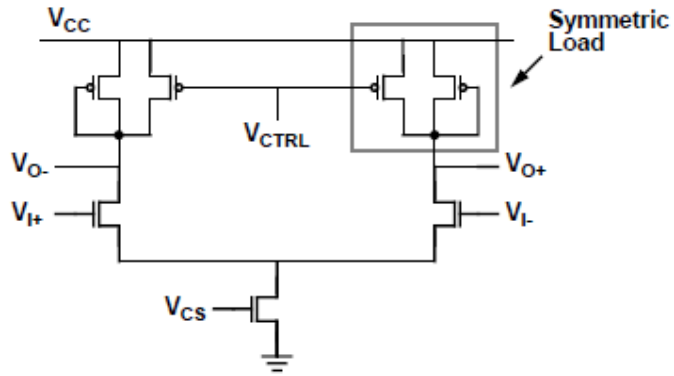

Figure 4.13: Symmetric load MOS realization [16]

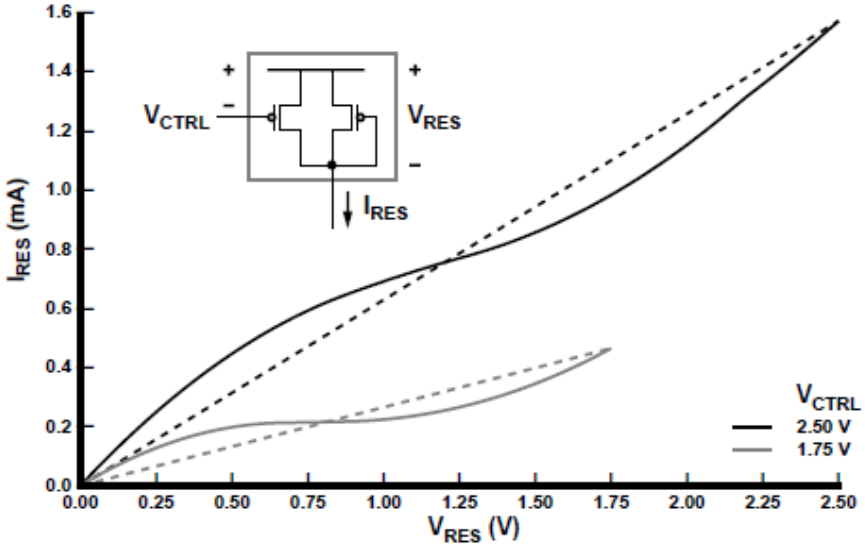

Figure 4.14: I-V characteristics of the symmetric load [16]

Other way of biasing the symmetric loads is shown in Figure 4.16, [17]. A diode connected device (MP7), which is equally sized with the other load devices, is biased with the half of the tail current. Drain voltage of the diode connected device forms the control voltage of the symmetric loads. Outputs still swing from VDD to VDD-Vctrl where Vctrl is equal to VDD-V_{SG7}. When tail current is completely steered to MN1, current is equally shared between MP5 and MP3 because saturation current of MP5 is equal to half of the tail current. Since same currents flow through two equally sized diode connected device, MP3 and MP7, lower swing limit is equal to Vctrl as desired for symmetric operation. This biasing scheme is more appropriate for bang-bang modulation as explained later in this document.

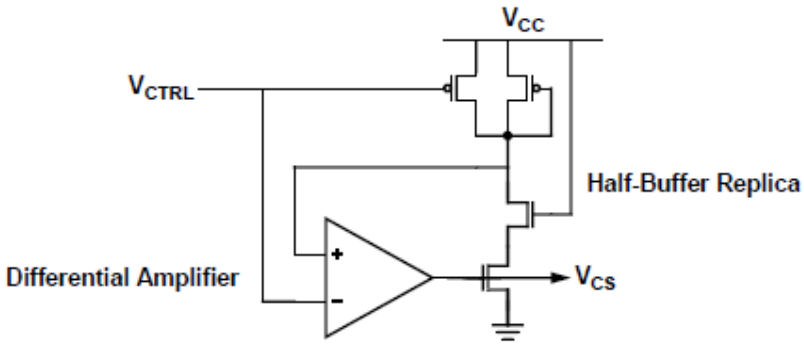

Figure 4.15: Replica and control circuits for obtaining the appropriate bias voltage of the NMOS bias transistor [16]

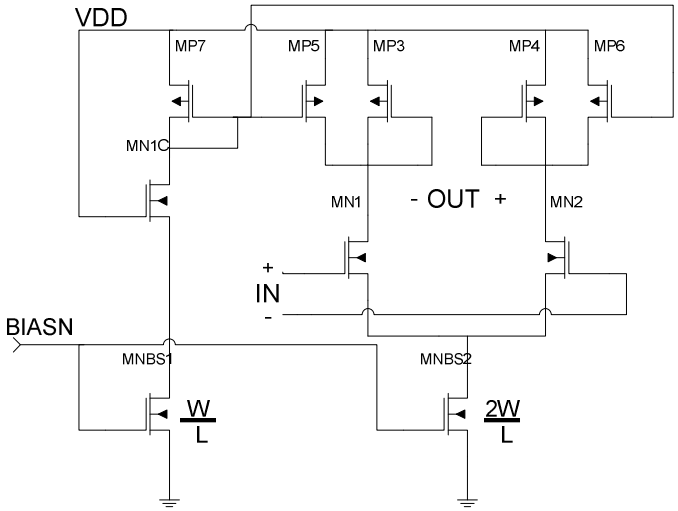

Figure 4.16: Another biasing structure for the symmetric loads

BIASN voltage is supplied with a diode connected device as shown in Figure 4.17. Control voltage of the VCO is converted to current with MNVCON device. This current, Iosc, is mirrored with MP1 and MP2 devices and applied to the diode connected device MNBS, which biases all the delay cells. Iosc current also flows through MP7 device in Figure 4.16 and hence control voltage of the delay cell is generated. This control voltage is proportional with the square root of the Iosc. Resistance of the symmetric load is proportional with the control voltage which means that VCO frequency is proportional with the square root of the Iosc. Iosc is proportional with the square of the VCON voltage so VCO frequency is proportional linearly with VCON if we neglect the short channel effects. This provides a fairly constant Kvco over the desired frequency range.

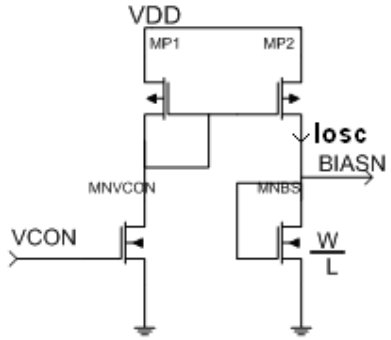

Figure 4.17: Bias block of the VCO

With the delay cell in Figure 4.16 and bias block in Figure 4.17, we can design a ring VCO. However, we also need UP and DOWN inputs to jump the frequency up and down in small amounts. VCO should respond to these UP and DOWN signals as quick as possible since it affects the jitter generation of the CDR loop. Since, VCO frequency is proportional with Iosc as shown in Figure 4.17, we can modulate the frequency up or down by adding or subtracting a small amount current. If this small current is made proportional with the Iosc, which can be done very accurately in an IC process, VCO frequency jumps can be controlled in a reliable manner. This method is used in [4] for a bipolar VCO and it gives constant frequency steps across process corners. Another method is proposed in [18] for bang-bang controlling but it suffers from large deviation of the bang-bang steps across process corners and for different bit rates.

We can modulate the Iosc by modulating the current of MP1. This current is mirrored with MP2, MNBS in Figure 4.16 and forms the control voltage of the delay cell after converted to voltage by MP7 in Figure 4.17. This long signal path can limit the bandwidth of the bang-bang modulation. Especially, loading at BIASN node in Figure 4.16 limits the bandwidth because of large bias devices. Therefore, it is better to modulate the cells individually. In fact, for a 4-stage ring VCO, which is required to generate quadrature phases, we can modulate only two delay cells. This modulation can be done by directly modulating the control voltage of two delay cells. Since these bang-bang steps are very small (for instance, 0.5% of the center frequency), control voltage change is also small. This means that we do not disturb the symmetrical behavior of the loads too much.

In a high speed CDR circuit, UP and DOWN signals are generally CML type signals which means that they can drive NMOS input pairs. Therefore, the delay cell, which will be modulated by UP and DOWN signals, are designed as depicted in Figure 4.18. UP and DOWN differential signals drive two differential pairs and outputs of the differential pair are connected to MP7 according to the following explanation. When UP=low and DOWN=low, MN8 is OFF and MN11 carries k*Iosc current, there

is also a fixed Iosc current so total current of MP7 is (1+k)Iosc. This is the quiescent situation: no UP or DOWN. We choose the bias current of the differential amplifier as 2(1+k)Iosc, which is required for symmetric load operation. We do not modulate the bias of differential pair since it will cause extra delays in bang-bang modulation. When UP=high and DOWN=low, MN8 and MN11 both carry k*Iosc current, which means that current of MP7 is (1+2k)Iosc. This causes a negative voltage jump at the control voltage and a positive step in VCO frequency. When UP=low and DOWN=high, MN8 and MN11 both carry a zero current and current of MP7 is Iosc. This causes a positive voltage jump at the control voltage and a negative step in VCO frequency. The case where UP=DOWN=high is identical to the case where UP=DOWN=low. VCO frequency is tri-stated in these cases. Added or subtracted current to MP7 is k*Iosc and its fixed current is (1+k)Iosc. Therefore, control voltage change of the delay cell is proportional with k/(1+k) which is equal to k if k<<1 is considered. k is controlled with the device ratios so its value does not change with manufacturing variations. This modulation scheme provides wide modulation bandwidth since BW is only defined by gm7 and total device capacitances at the control voltage node.

Overall VCO block diagram is shown in

Figure 4.19. DELAY_BANG, DELAY and VCO_BIAS blocks are already depicted in Figure 4.18, Figure 4.16 and Figure 4.17 respectively. BUFFER blocks are needed to isolate the VCO and also to drive the routing and the loading capacitances. An active inductor loaded NMOS amplifier is used to increase the buffer bandwidth and to minimize the buffer delay. NMOS loads are biased with a voltage higher than Vdd to decrease the DC voltage headroom consumed by the NMOS load devices [19]. An initially estimated 60fF loading capacitance is connected to the output. 16ps delay is measured between buffer input and output.

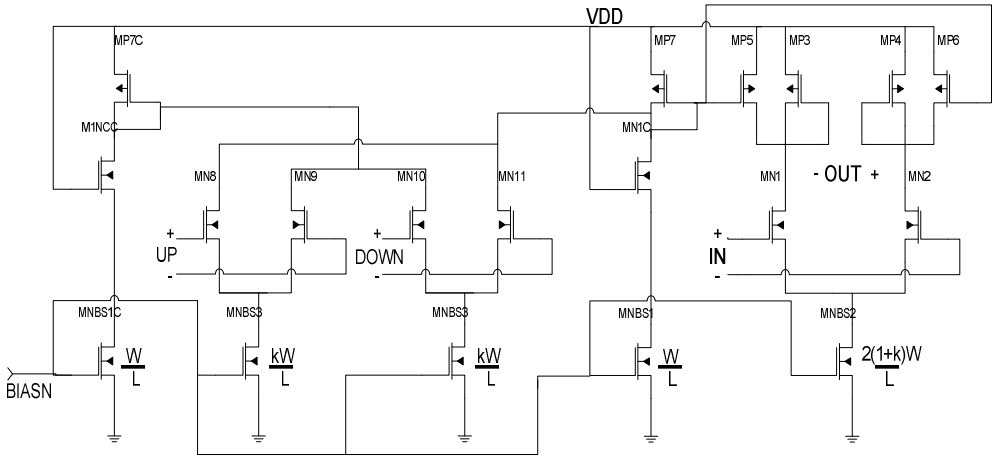

Figure 4.18: VCO delay cell modulated by UP and DOWN signals

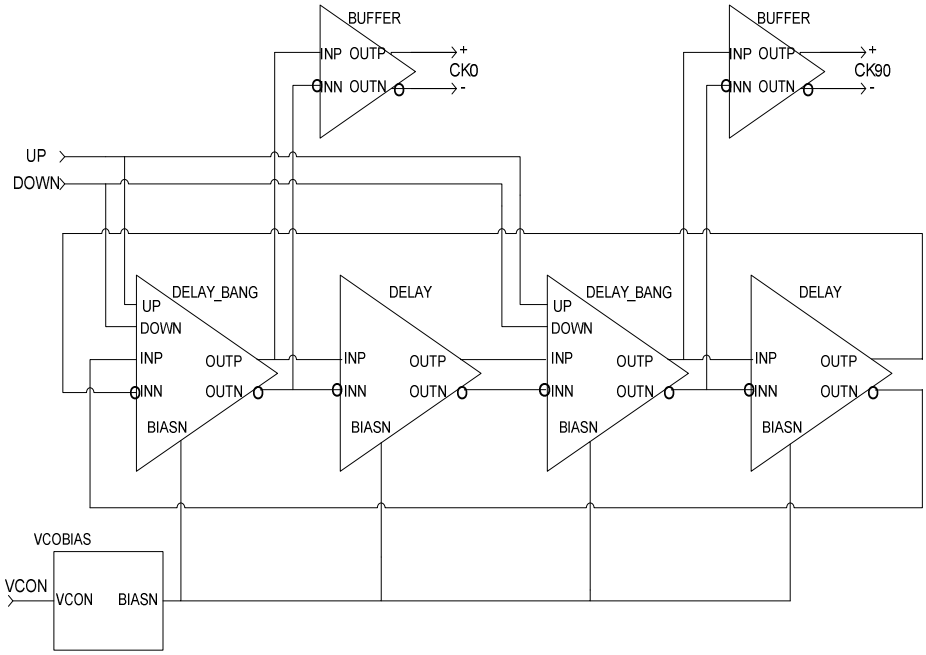

Figure 4.19: Overall VCO block diagram

The proposed VCO structure was designed and simulated in Cadence environment. It can oscillate at 2.5Ghz for VCON=1V, which is needed to recover the 5Gbs data with a half rate architecture. Its voltage-frequency characteristic is shown in Figure 4.21. VCO gain is around 4.4GHz/V for control voltages around 1V. VCO ring and buffer differential outputs are shown in Figure 4.22. Buffer delay is around 15ps when buffer is connected to the phase detector.

VCO output frequency is modulated by UP and DOWN signals as shown in Figure 4.23. VCO responds to these signals in one period, 400ps. Another important point is that UP and DOWN frequency steps should be symmetrical. According to transient simulations, UP and DOWN frequency steps are 5.093 and 5.081 MHz respectively.

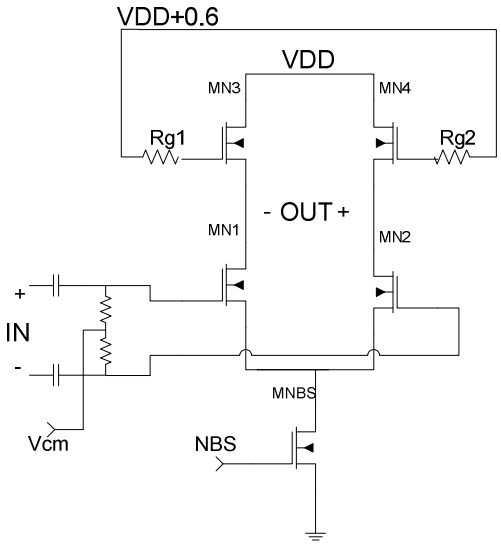

Figure 4.20: VCO buffer with active inductor loads

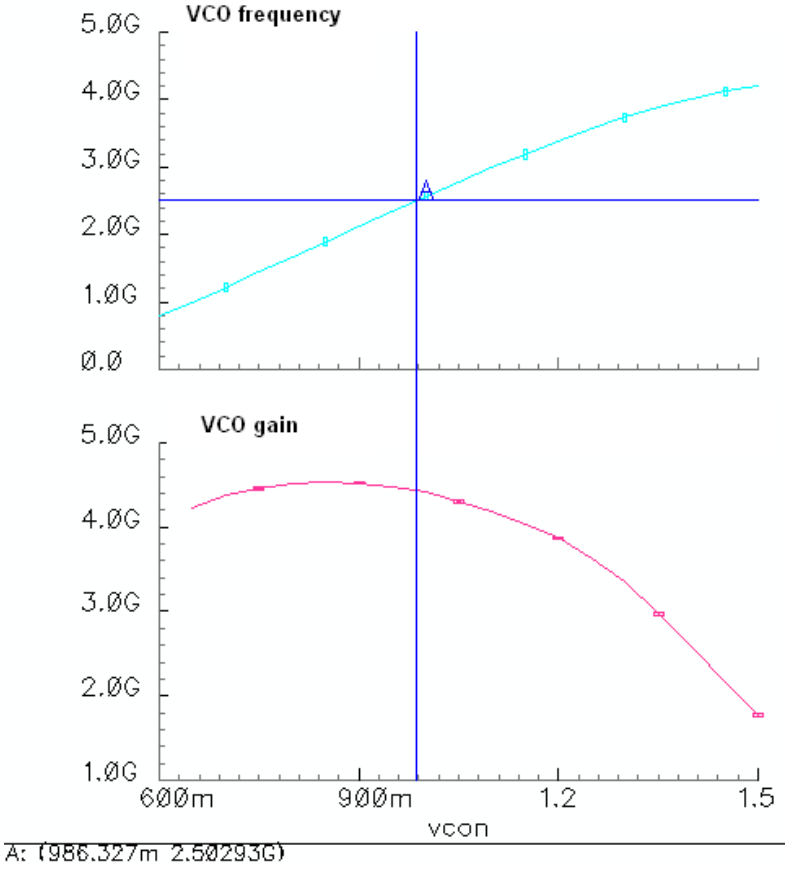

Figure 4.21: VCO frequency and gain vs. control voltage

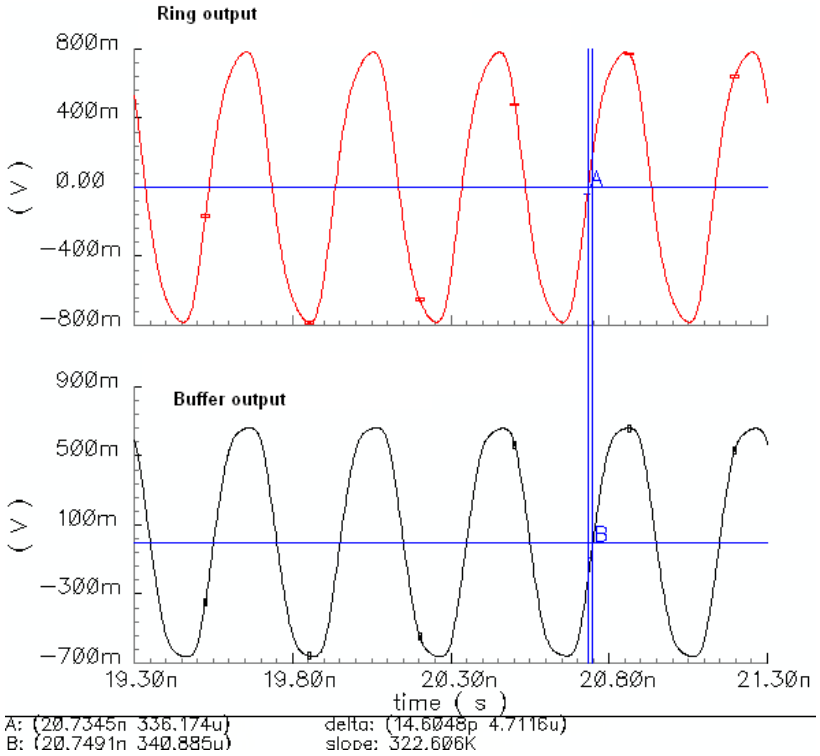

Figure 4.22: VCO ring and buffer outputs

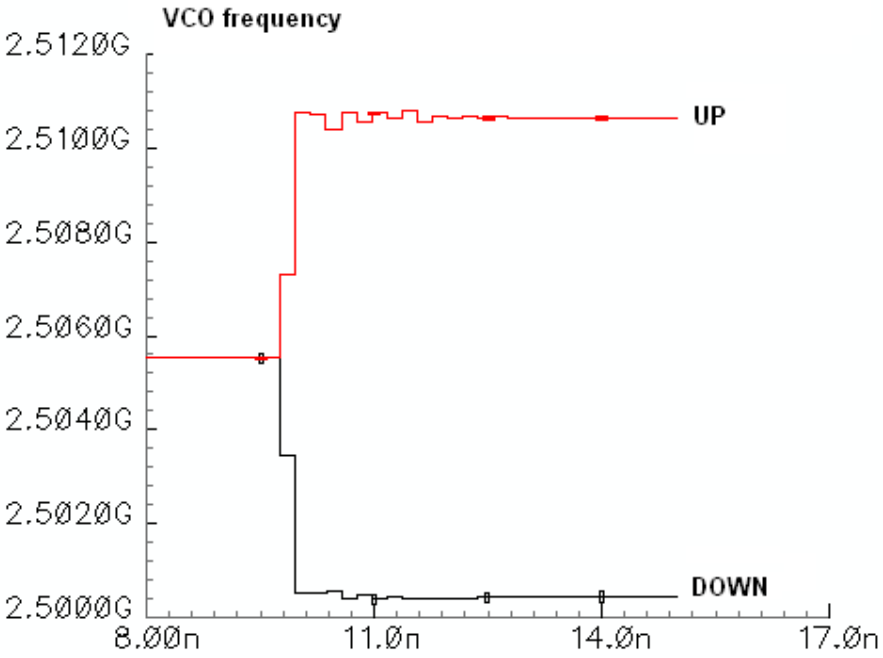

Figure 4.23: UP and DOWN response of the VCO

5. CDR AUTOMATIC FREQUENCY CALIBRATION

Voltage controlled oscillators should have sufficient gain to cover the desired frequency band over process and temperature variations. Required gain increases due to lower supply voltages and higher operating frequencies. This makes VCO more susceptible to noise coming from loop filter, power supply etc. Some techniques are proposed in [5-7]. In all these techniques, VCO gain is reduced dividing the desired frequency range into overlapping sub ranges as shown in Figure 5.1. Proper sub-range is found during initial lock by searching all the ranges. Range searching algorithms may result in long locking times or more complex circuits. Additionally in these approaches, if VCO locks close to the limits of a range, a re-calibration need may arise due to temperature change. If this should be avoided, ranges have to be wider, which results in a large oscillator gain.

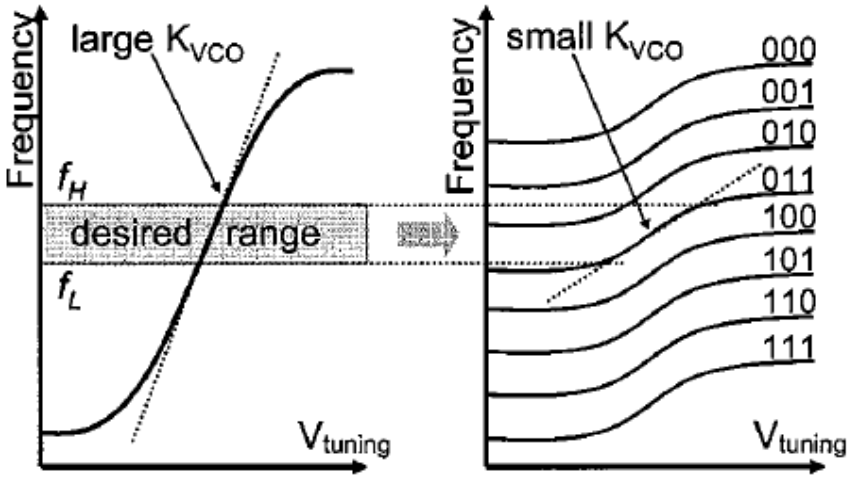

Figure 5.1: VCO wide tuning range is divided into overlapping subranges to reduce gain [5]

A method for calibrating the current-controlled ring oscillators is proposed in this section, which tries to overcome the limitations mentioned above. It was designed for a CDR system but idea can be applied to other phase locked loops as well.

5.1 Proposed Calibration Method

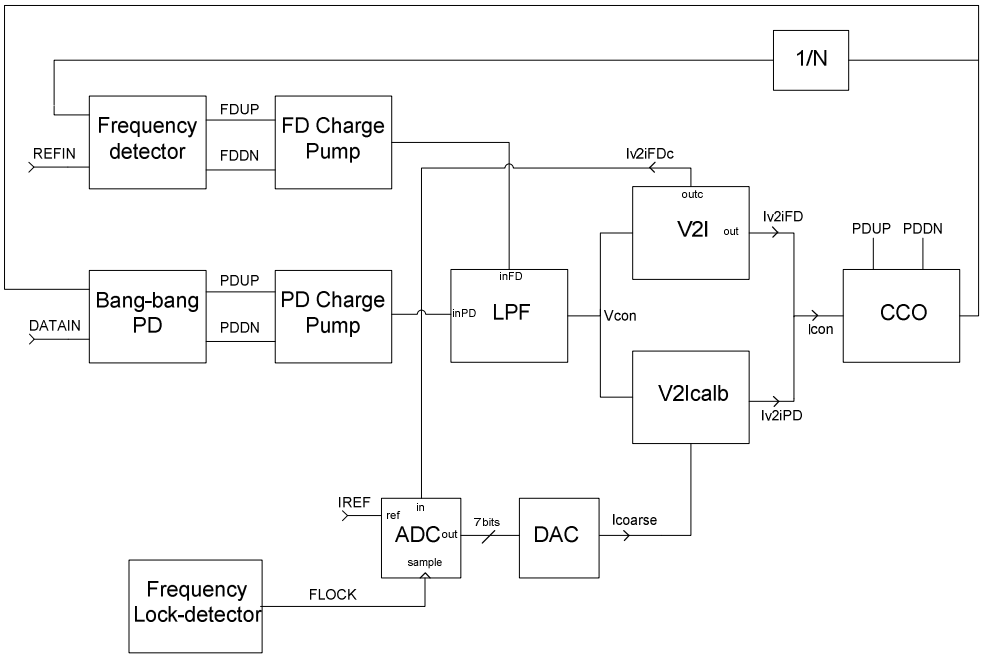

Figure 5.2: Proposed CDR VCO auto-calibration architecture

Block diagram of the proposed architecture is shown in Figure 5.2. A frequency acquisition aid is generally needed in CDRs due to the low pull-in range of CDR phase detectors. This can be done in many ways; we assume here that there is a proportional frequency source coming to the IC. This signal is called REFIN in the figure. During the frequency acquisition, frequency detector, which is a classical phase/frequency detector with two resettable flip-flops and a reset path as depicted in Figure 5.3, pulls the VCO to the target frequency. Main oscillator is a current controlled ring oscillator, CCO. There are two voltage-to-current converters (V2I) between the loop filter and the CCO. First one is a wide range V2I to cover the desired frequency band over process and temperature variations. It is only used in the frequency acquisition process. After frequency lock is achieved, lock detector triggers a current mode ADC. ADC samples the replica current of the wide-range V2I and following DAC converts the digital code to analog current again.

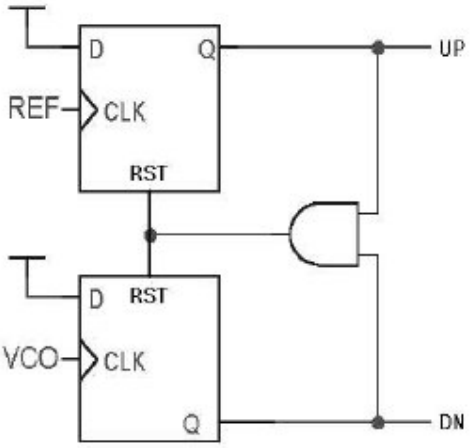

Figure 5.3: Classical phase frequency detector

VCO oscillates close to the target frequency if DAC output is applied to the CCO. This current is called coarse current, I_{coarse}. Calibrated V2I injects I_{coarse} in the middle of its voltage-current characteristics, Figure 5.7. Its current can go up to $(1+K)I_{coarse}$ and fall to $(1-K)I_{coarse}$ when control voltage is varied. K should be chosen as low as possible to reduce the VCO gain. Oscillator frequency variation with temperature puts a lower bound for K. Therefore, reference current of ADC and DAC is designed in such a way that it compensates the frequency variation of the oscillator with temperature. Compensation is simply done with a current source, which has around 400ppm/^{0}C temperature coefficient.

After VCO is calibrated, wide-range V2I is turned off and calibrated V2I is turned on. To start the clock and data recovery, bang-bang phase detector and proceeding charge pump are powered up and additionally loop filter resistor is shorted through a transmission gate, Figure 5.4. Transmission gate is realized with zero-Vt NMOS and nominal PMOS devices in parallel.

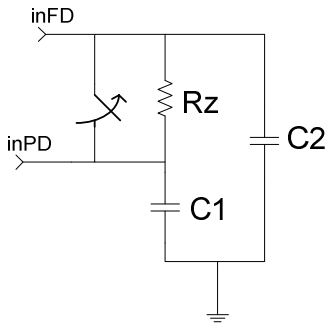

Figure 5.4: Loop filter

Flow chart of the calibration algorithm is shown in Figure 5.5. It is quite simple as compared to other published calibration methods. Iterative range finding algorithms are not needed, which reduces calibration time considerably. Actually, VCO operating frequency range is not divided into sub-ranges here; range is generated during calibration. Because VCO operates in the middle of the calibrated range, re-calibration possibility decreases. That possibility is further reduced with temperature compensation of the oscillator.

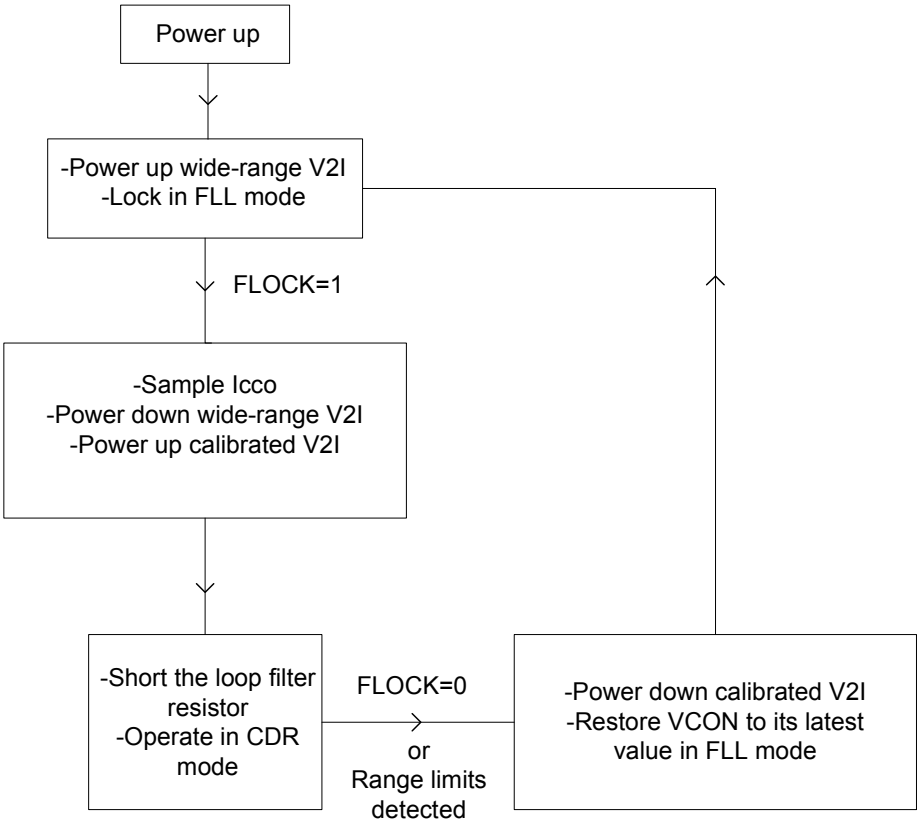

Figure 5.5: Flow chart of the calibration algorithm

5.2 V2I Design

This section describes the design of voltage-to-current converters. CCO structure was already described in previous chapter. Key component for the VCO is V2I block, which is depicted in Figure 5.6. Wide-range V2I and calibrated one are both shown in this figure. PU_{wide} and PU_{calib} are the two switches that power up (or down) wide-range and calibrated V2Is respectively. Wide-range V2I is implemented with MNVCON transconductance element and MP1, MP3 current mirrors. MP1, MP2 and MP3 are matched so same current injected to the CCO flows through MP2. When frequency lock is detected, a current-mode ADC samples the current of MP2. Proceeding DAC circuit again converts the digital value to analog current, which is

called I_{coarse}. DAC also outputs $K \cdot I_{coarse}$, which is mirrored by MN4 and MN5 from MN3. MN4 and MN5 are sized as half of MN3. Therefore, differential amplifier built with MN1-5 and MP6-7 can output a current between $\pm K \cdot I_{coarse}$. Differential amplifier output current is called I_{fine}. I_{coarse} and I_{fine} are summed and applied to the oscillator through MP4 and MP5 current mirrors. Source degeneration is utilized to widen the input range of the differential amplifier, which helps to reduce the oscillator gain.

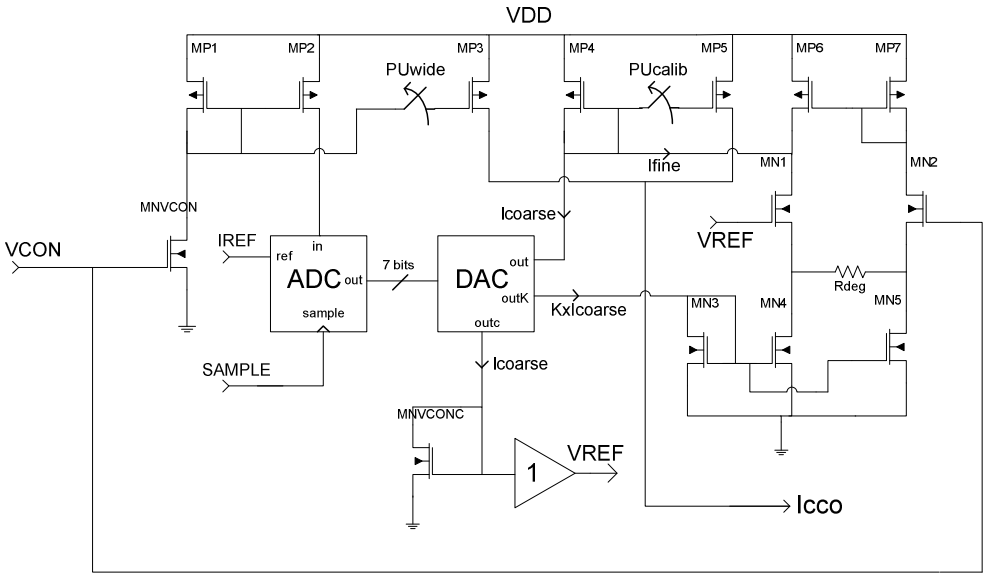

Figure 5.6: Voltage-to-current converters with ADC and DAC blocks

After CCO current is sampled, PUwide switch is open and PUcalib switch is closed. Now VCO operates in a narrower range, which means that oscillator gain is reduced. Voltage-current characteristics of wide-range and calibrated V2Is are depicted in Figure 5.7.

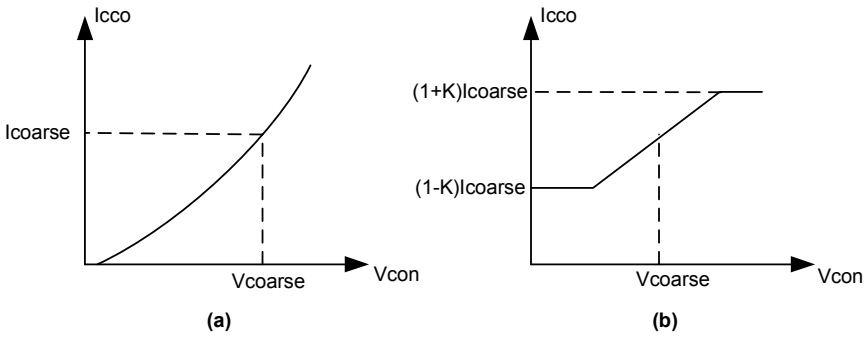

Figure 5.7: Voltage vs. current characteristics of (a) Wide range V2I (b) Calibrated V2I

VREF constant voltage of the differential amplifier is generated with I_{coarse} and a diode-connected transistor, which has the same size of MNVCON. Then, VREF voltage is almost equal to the stabilized control voltage value after frequency lock is achieved. Therefore, loop continues to operate around latest VCON voltage when switched to CDR mode. VREF can also be a constant voltage but then loop cap should be forced to that voltage in the beginning of data recovery mode. This means we also keep record of the latest control voltage. This information is valuable when a need arises to switch to frequency locked loop (FLL) again. Loop cap is forced to VREF before FLL starts operation, which shortens the re-lock time considerably.

5.3 ADC and DAC Design

Simplified schematic of ADC and DAC circuits are depicted in Figure 5.8. 7 bits resolution seems enough for this application. Nominal reference current of ADC is 25uA, which means that ADC can digitize any current between 0-3175uA. In typical conditions, VCO needs around 2.5mA to operate at 2.5GHz frequency, which means that there may be 1% error between sampled CCO current and DAC output due to the quantization error.

Successive approximation method is used for conversion. Every single bit, n, controls a current source, which sinks $2^n \cdot I_{ref}$ current. It is easy to compare the input current and ADC output: They are just shorted. If input current is higher, output is high. If the input current is lower, output is low. After SAMPLE gets high, logic section sets D6 high with the rising edge of external low-frequency oscillator clock. This makes the 7th current source on while the others are off, which means that ADC output current is $2^6 \cdot I_{ref}$. If input current is higher than $2^6 \cdot I_{ref}$, D6 remains high. If it is lower, D6 is set to zero. Same procedures are applied for other bits. Total conversion time is $7 \cdot T_{clkDAC}$, where T_{clkDAC} is the period of the ADC oscillator. 5MHz oscillator was used in this project, which corresponds to total 1.4us conversion time. In the actual implementation of ADC, cascode current sources were used to improve the accuracy as depicted in Figure 5.9.

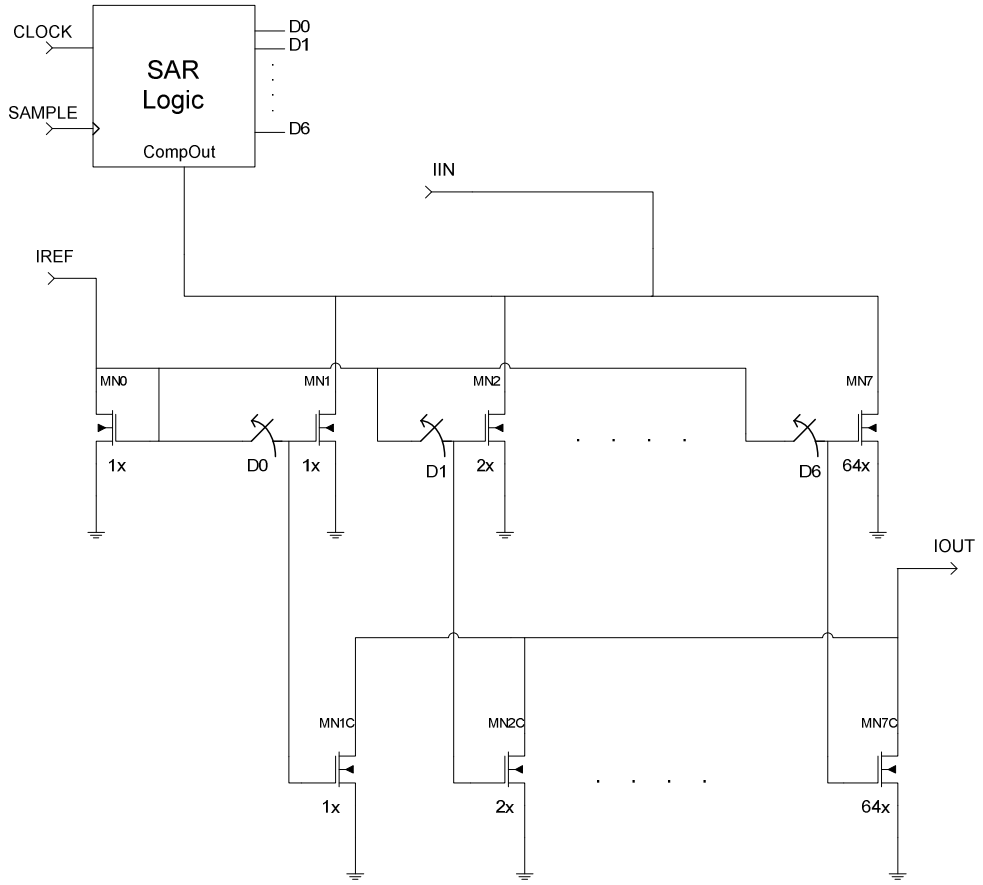

Figure 5.8: Simplified schematic of current mode ADC and DAC

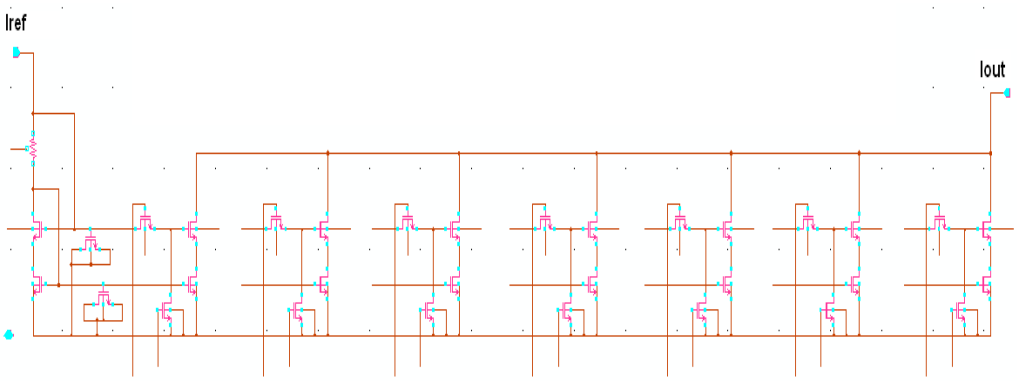

Figure 5.9: Actual implementation of reference current sources

DAC consists of replicas of the weighted current sources of ADC. DAC and ADC current sources are connected to the same bias voltage. DAC additionally outputs $K \cdot I_{coarse}$ and another I_{coarse} currents, which are generated with a second replica branch and PMOS current mirrors. K is adjusted by the mirroring ratio.

Logic section is designed with behavioral models as shown in Figure 5.10 due to the lack of logical library in UMC 0.18 design kit. These behavioral elements can be replaced with their transistor level implementations quite easily. After SAMPLE gets high, logic section sets MSB (7^{th} bit) high with the rising edge of external low-frequency oscillator clock, CLKADC. If ADC comparator output goes low, MSB is set to low. Otherwise, it remains high. This process is repeated until LSB.

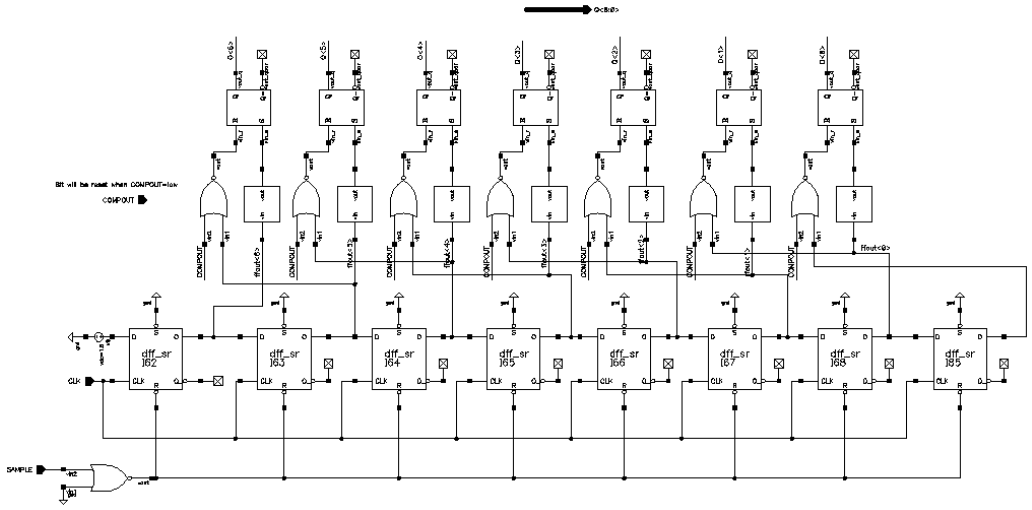

Figure 5.10: Logic part of ADC

5.3.1 Reference Current Design of ADC

ADC reference current is designed to compensate the oscillator frequency change with temperature. As shown in Figure 5.11, a temperature independent current source causes the oscillator frequency to change 6.8% around 2.5GHz when temperature is swept from -20 to 105 ^{0}C. When a current source with around 400ppm/^{0}C temperature coefficient is used, frequency variation gets 2.8% as depicted in Figure 5.12. Current source with specific temperature coefficient is obtained by summing Vbg/R and PTAT currents with different weights. Vbg is the bandgap voltage, which has negligible temperature dependence. Circuit schematic is depicted in Figure 5.13. This helps us to decrease the K value and hence oscillator gain. Three process corners: typical, fast and weak were simulated and the variation numbers given above belong to the worst-case corners. Change of the reference current with temperature is visualized in Figure 5.14.

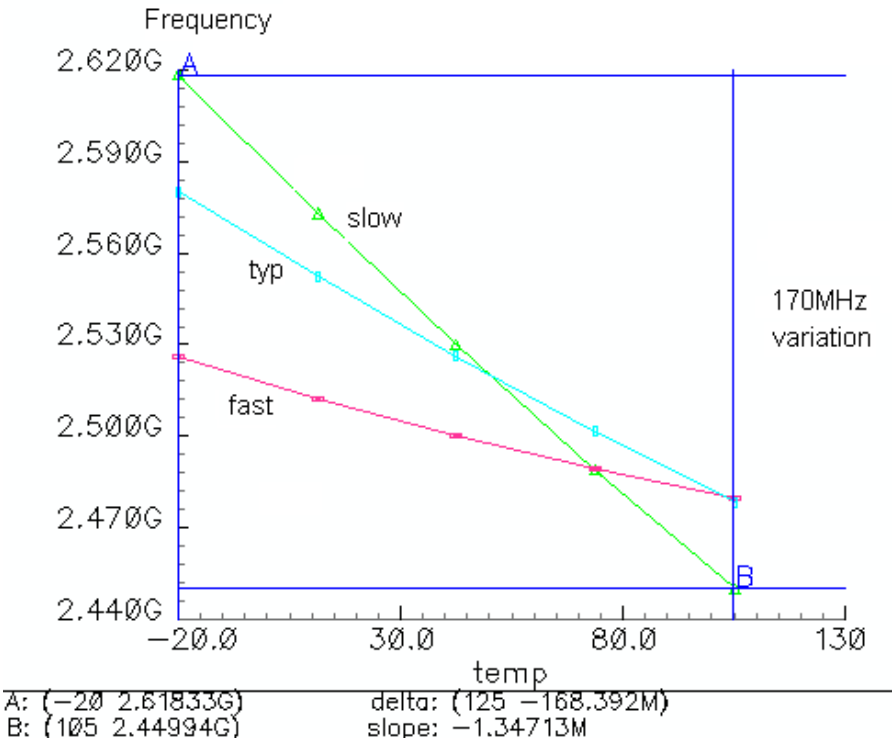

Figure 5.11: CCO frequency variation over temperature with 0 ppm/^{0}C current source

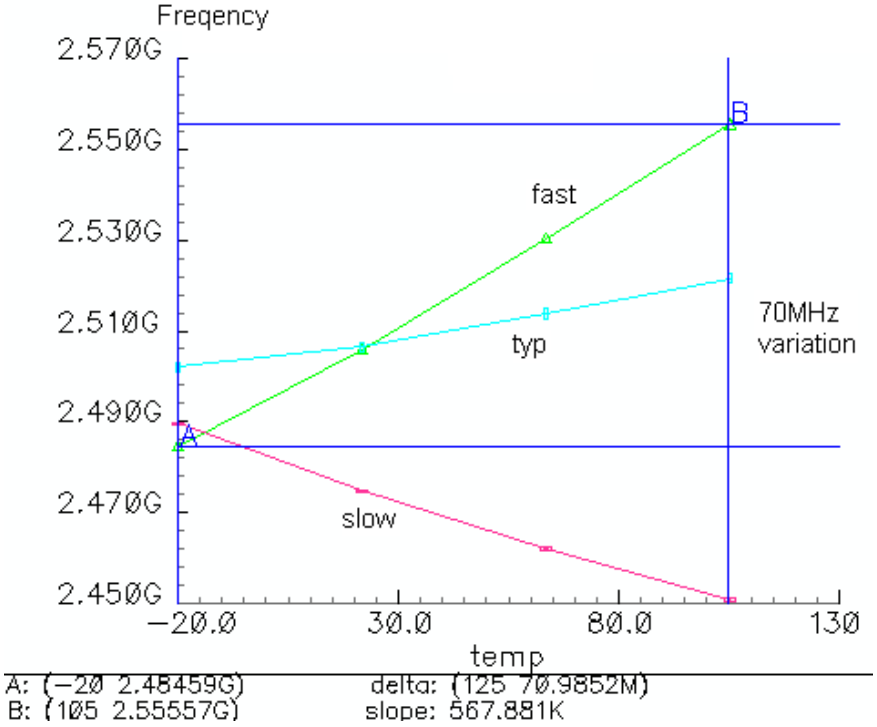

Figure 5.12: CCO frequency variation over temperature with 400 ppm/^{0}C current source

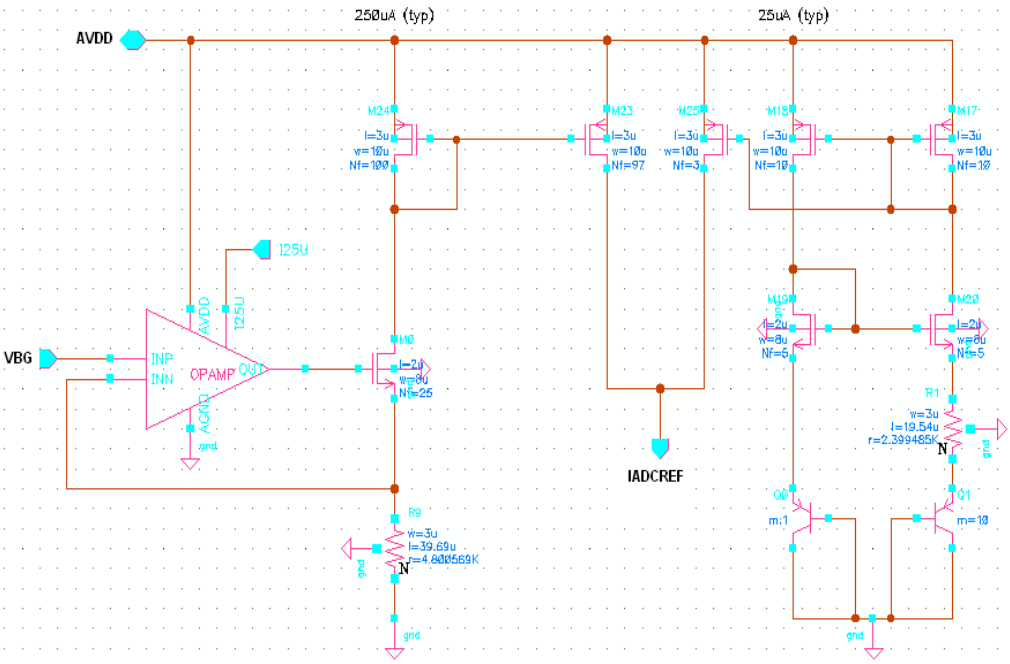

Figure 5.13: Schematic of ADC reference current source

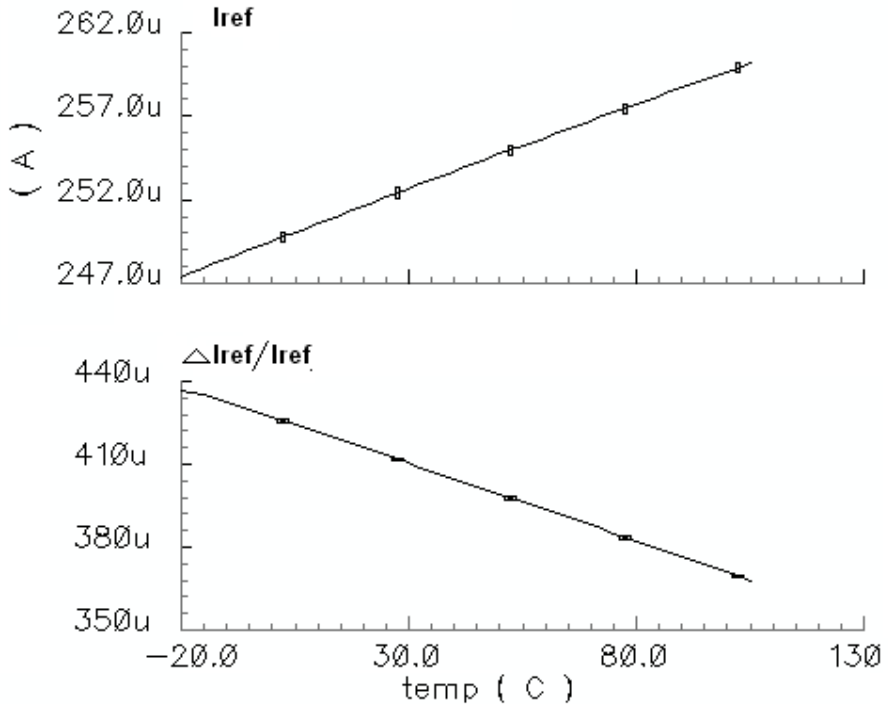

Figure 5.14: Reference current change over temperature

5.4 Simulation Results

5.4.1 V2I, ADC and DAC Simulation Results

Figure 5.15 shows wide-range and calibrated V2I currents. Sampled value of wide-range V2I constitute the center current of calibrated V2I as mentioned before. Difference between two currents is less than 1%. Decimally coded digital output of ADC is shown Figure 5.16 during the sampling process.

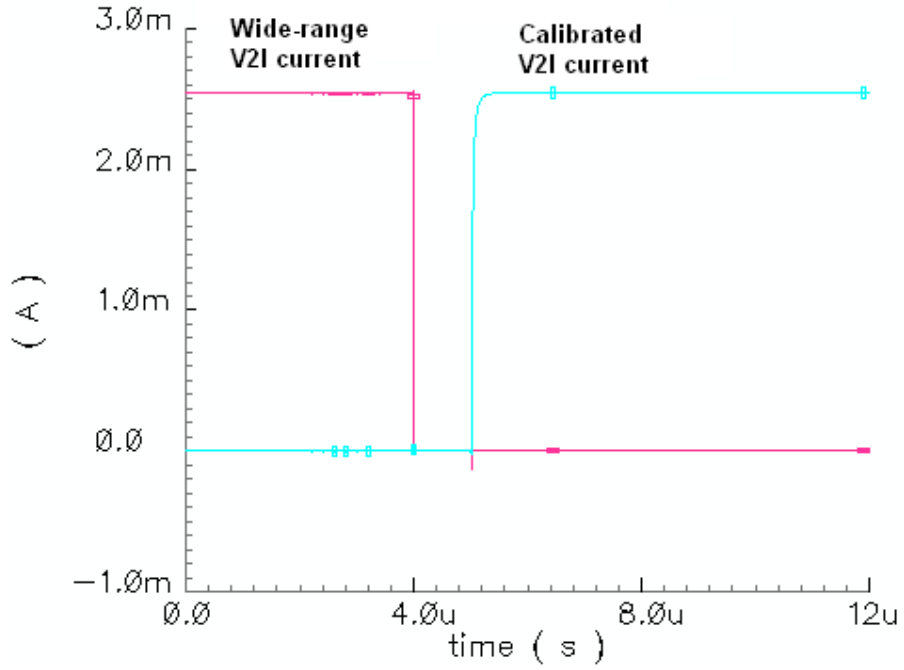

Figure 5.15: Wide range V2I current and DAC outputs after sampling operation

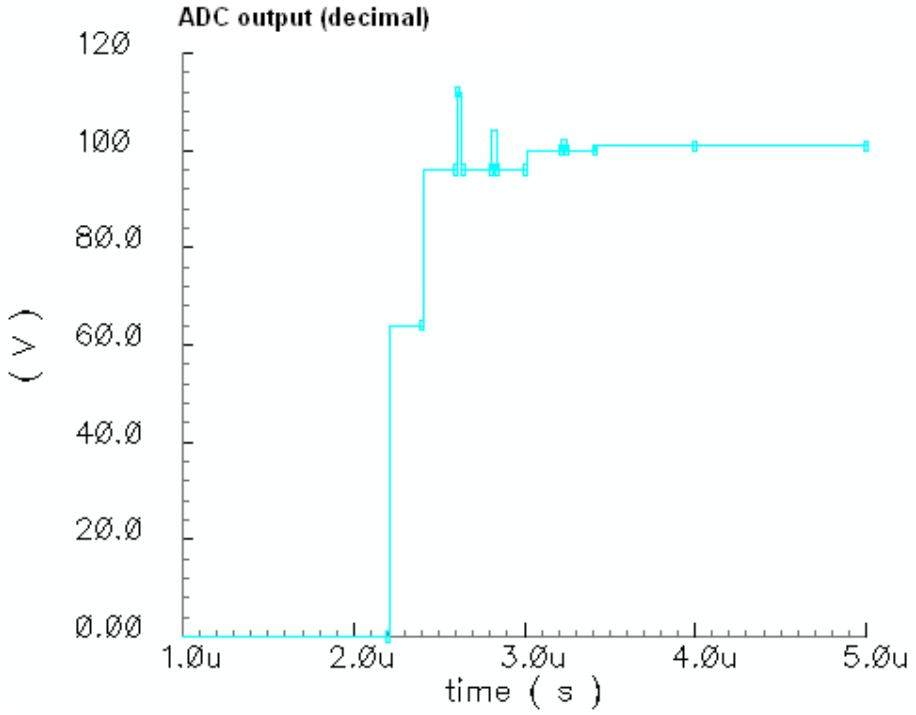

Figure 5.16: ADC decimal output during the sampling process

5.4.2 Top-Level Simulation Results

Operating temperature range for this circuit is from -20 ^{0}C to 105 ^{0}C. Our target is to prevent any re-calibration need due to marginal temperature changes. Therefore, oscillator was calibrated at -20 ^{0}C and its voltage-frequency characteristic was checked at 105 ^{0}C for typical, weak and fast corners. Simulation results are visualized in Figure 5.17, Figure 5.18 and Figure 5.19 for typical, weak and fast corners respectively. When VCO is calibrated at -20 ^{0}C, center frequency, 2.5 GHz, is in the middle of the voltage-frequency characteristics. When temperature goes to 105 ^{0}C, VCO still can operate at 2.5GHz with some margin to range limits in weak and fast corners. If temperature range is narrower or re-calibration is acceptable, K value of V2I can be decreased. K is chosen 0.05 for this project, which gives 330 MHz/V oscillator gain after calibration in typical conditions. Calibrated gain varies between 230 and 410 MHz/V over process and temperature corners mainly due to the change of V2I differential amplifier input range. Gain is 4.4 GHz/V (typical) in frequency locked loop mode to cover the center frequency over process and temperature corners.

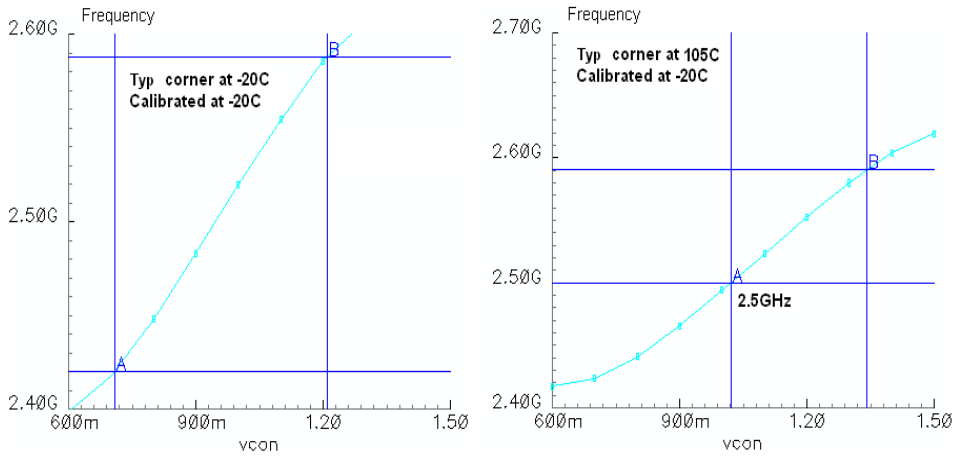

Figure 5.17: VCO voltage-frequency characteristics for typical corner at -20 ^{0}C and 105 ^{0}C when it is calibrated at -20 ^{0}C

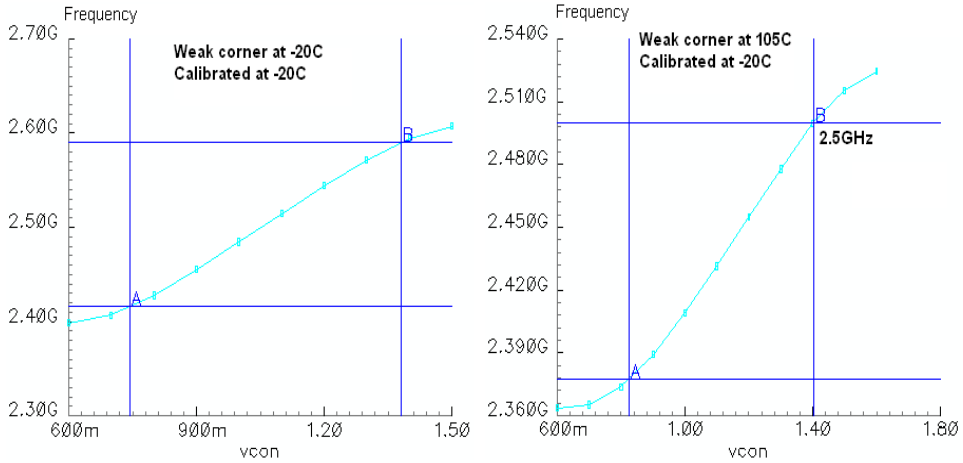

Figure 5.18: VCO voltage-frequency characteristics for weak corner at -20 ^{0}C and 105 ^{0}C when it is calibrated at -20 ^{0}C

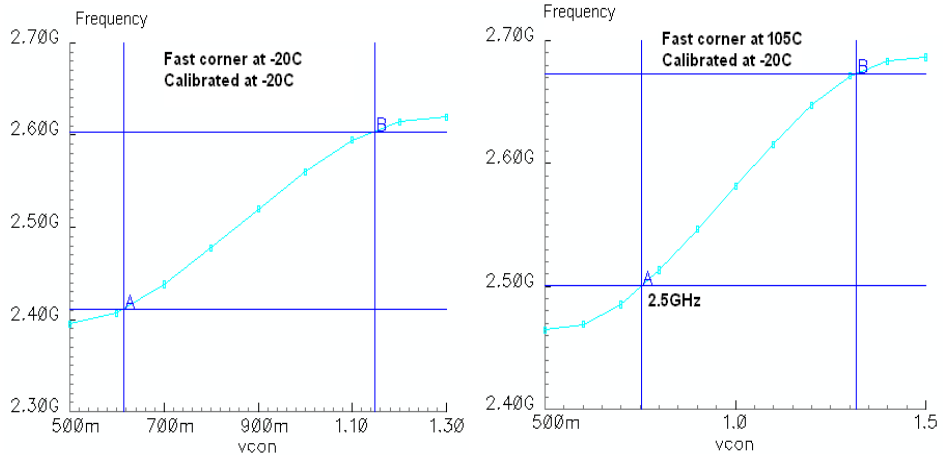

Figure 5.19: VCO voltage-frequency characteristics for fast corner at -20 ^{0}C and 105 ^{0}C when it is calibrated at -20 ^{0}C

Entire system was simulated with the parameters summarized in Table 5.1. System specifications for these parameters are given in Table 5.2. Input data is generated with an ideal 15 bit PRBS circuit. VCO output frequency plot is visualized in Figure 5.20. Sampling process starts at 3.5us and is finished in 1.7us. At 5.5us, frequency locked loop is stopped. It takes a few hundreds of nanoseconds for DAC output to stabilize so CDR loop is powered up at 6us. Bang-bang PD corrects the frequency error and starts to recover the data and clock.

Table 5.1: System parameters

Loop cap (C1)	200pF	VCO wide-range gain	4.4G/V
Loop ripple cap (C2)	5pF	VCO calibrated gain	330M/V
FLL charge pump current	10uA	Bang-bang loop CP current	50uA
FLL N division ratio	32	Bang-bang frequency step	5MHz
Loop filter res.	6k		

Table 5.2: System specifications

FLL bandwidth	1.75MHz	CDR jitter tolerance corner frequency	2.5MHz
FLL phase margin	70^0	CDR stability factor	300
		CDR p-p jitter generation	3.7ps

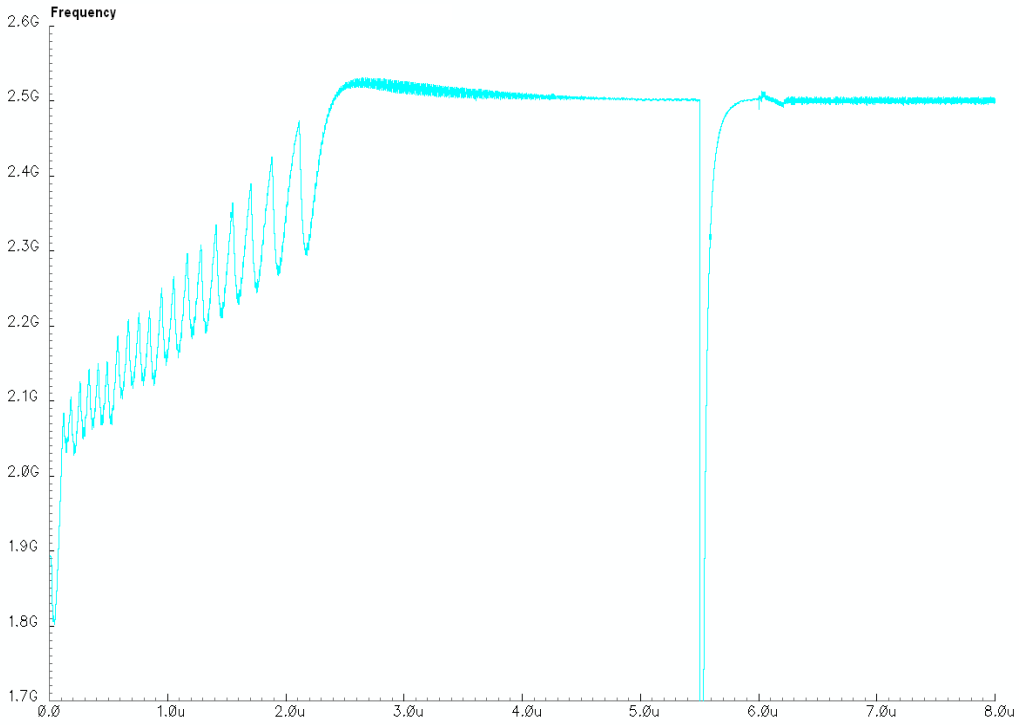

Figure 5.20: VCO output frequency during transition from FLL to CDR mode

Eye diagrams of input data and quadrature clock phases are shown in Figure 5.21. CK0 samples the data while CK90 samples data transitions. Jitter plots are depicted in Figure 5.22 and Figure 5.23. Jitter is defined as the time difference between sampling clock and the middle of data signal. Peak-to-peak value of hunting jitter is 3.7ps in CDR mode.

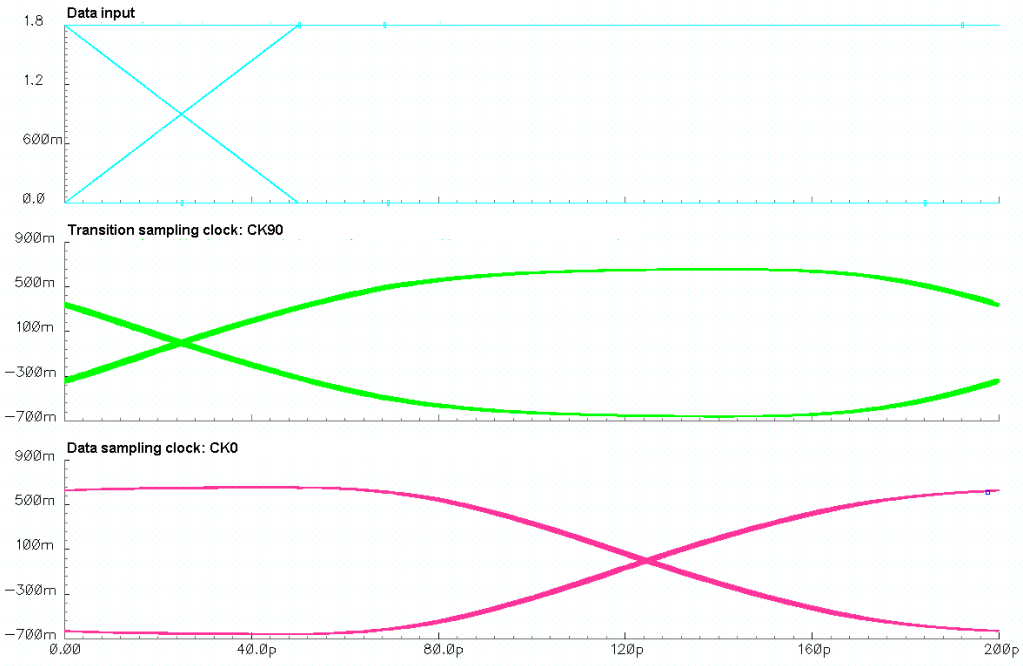

Figure 5.21: Eye diagrams for data and quadrature clocks after CDR locks to random data

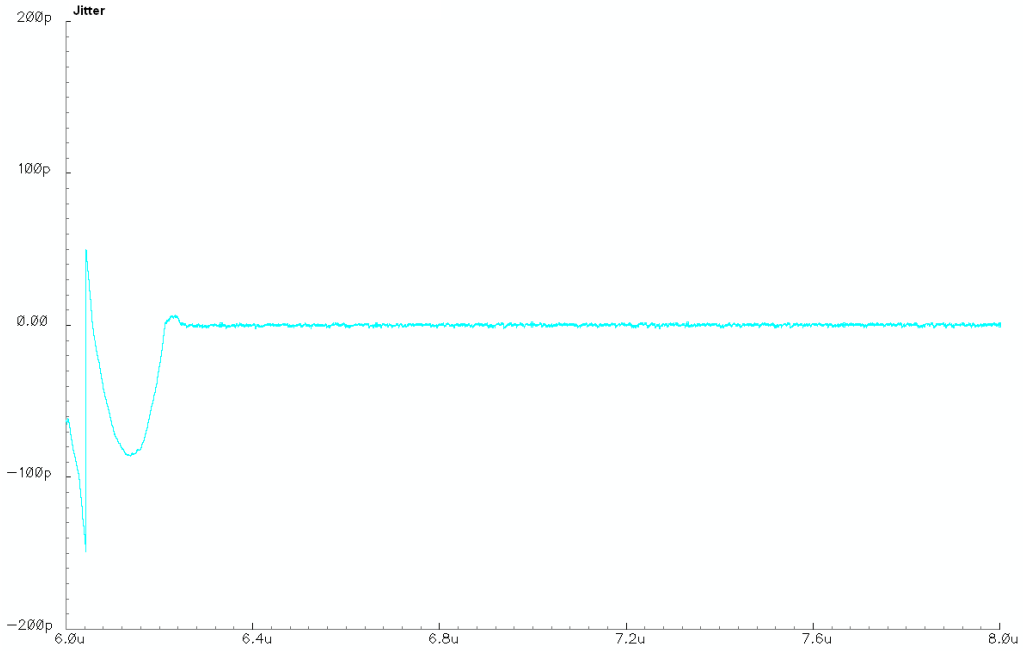

Figure 5.22: Jitter between data and sampling clock

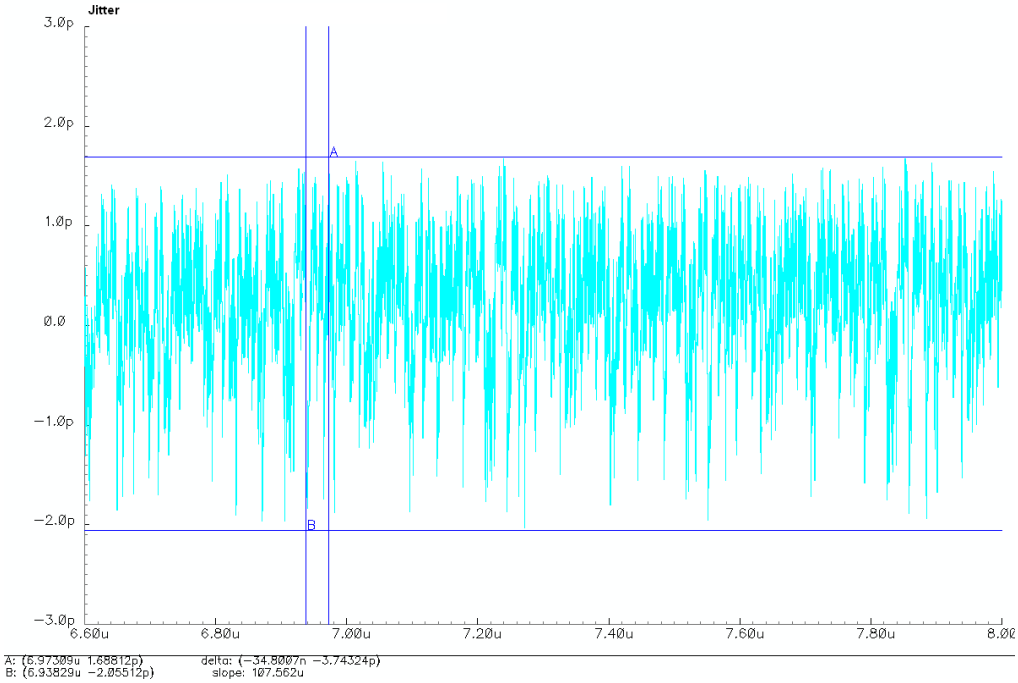

Figure 5.23: Jitter between data and sampling clock (ZOOMED version)

6. CONCLUSION

Bang-bang type clock and data recovery circuits were investigated in this study. Behavioral modeling, system level design issues and transistor level implementations of loop elements were described.

An alternative method for VCO calibration is proposed and implemented in 0.18u CMOS technology. Circuits were designed and simulated in Cadence design environment. Corner simulations indicate that VCO is successfully calibrated after frequency lock so that re-calibration is not needed even temperature varies marginally. No range searching algorithms are needed, which reduces the design complexity and initial lock time.

Future work is to fabricate the circuits and to test the functionality and performance in real silicon. Additionally, digitally extracting the center current of the current controlled oscillators can provide good controllability over the VCO frequency characteristics.

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BIOGRAPHY

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