行政院國家科學委員會專題研究計畫　期中進度報告

子計畫三:寬頻光都會與接取網路之強健系統與智慧網路設計(1/3)

計畫類別： 整合型計畫
計畫編號： NSC94-2213-E-032-005-
執行期間： 94 年 08 月 01 日至 95 年 07 月 31 日
執行單位： 淡江大學電機工程學系

計畫主持人： 李揚漢

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☑期中進度報告

寬頻光都會與接取網路之關鍵技術－
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中　華　民　國　九十五　年　五　月 二十　日

行政院國家科學委員會專題研究計畫成果報告

寬頻光都會與接取網路之關鍵技術－

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一、　中文摘要

在光網路中，雷射的輸出波長容易受到溫度變化、元件老化與電流漂移等因素而造成輸出波長的不穩定，針對此問題我們提出利用 PID controller 加入雷射等效模型迴路中並且提出其演算法，經過理論分析與數值分析後，可得到雷射輸出波長的動態誤差可以控制到零，而穩態誤差也可以控制在不錯的範圍內。另一方面，我們除了討論 PID 對雷射輸出波長穩定度的探討，另一方面也針對在可調式雷射(DBR)中利用三個電極的電流來調整出不同的 ITU Channel，在同一個 ITU Channel 中可由許多組不同的電流組合來產生，但是在考慮跳換 ITU Channel 時哪一組電流組合能夠有最好的效能(Chirping 與 Switching Time)是我們所討論的重點，同時也評估與挑選好壞電流組合的方法。

關鍵詞：光纖通信，波長穩定，半導體雷射，PID 控制器， 分散式布拉格反射雷射二極體，線性調頻。

Abstract

In the optical network, laser model easily influenced by temperature changes, device aging and current drift to effect wavelength instability. In the other hand, how faster to get the wavelength stability when change the wavelength in different channel that is very importance. We use theoretical analysis for PID controller to control the stable error to be equal to zero and to control the dynamic error to can accept range. PID controller has two advantages that are easily to implement and integrated.

In the other hand, DBR (Distributed Bragg Reflector) laser, it uses and adjusts driving currents in the tri-electrode to provide various ITU channels. It can have many different current combinations to generate the ITU channels. But when we take system performance into consideration, such as the chirp and transient time status when we switch channels between ITU channels, certain current combinations will generate better system performance than the others.

We will develop the principle of how to select current combinations to get better system performance and also discuss the method to evaluate their system performance when various

current combinations are considered.

Keywords: optical communication; wavelength stabilizer; semiconductor lasers; proportional integral derivative (PID) controller; DBR (Distributed Bragg Reflector) laser, Chirping.

二、 研究目的

在半導體雷射(Semiconductor lasers)中，輸出的波長穩定度會受到溫度(Temperature)、電流漂移(Current drift)，元件老化(Aging)等影響。在光通訊系統中,為了避免 adjacent channel 與 signal drop-out 之間產生 interference / crosstalk 所以需要一個精準的波長穩定(Wavelength Stability)控制來控制雷射的輸出波長。而在大多的系統中所使用的波長穩定(Wavelength Stability)控制器通常都很昂貴、架構複雜與通用性不高（not flexible）**[1]**。另外也有比較容易的控制 WS 的方法，此方法是利用普通的溫度控制器來解決問題，但此方法不能解決變動的 bias current 與 device aging 所造成波長不穩定的影響。所以近年來的發展廣泛的使用 Synchronized etalon filters 或經由電子電路鎖住 birefringent Fabry-Perot interferometer 的共振與 Bragg Wavelength 的 fiber grating coupled to a Fabry-Perot**[2-4]**，這些方法均使用 error signal 來控制 laser turning 並提供令人滿意的 WS，但是這些方法不適用於光通訊系統通道(Channel)數量大時，因為控制器整體的複雜度會隨著 Channel 個數成倍數的長。所以在**[5]**中，提出 Photodetector (VT-WSPD) 的架構，利用偵測雷射輸出波長所受到溫度變化、元件老化與電流漂移的影響所造成的波長漂移量，利用外部電壓微調經由回授網路來減少外部溫度或元件老化所造成的波長不穩定的影響，在這方法中需要一個非常準確的電壓源提供給 Photodetector 使用，我們依據[5]中的架構提出在雷射等效模型的控制迴路中加入有效的 PID controller 並且分析其演算法，此方法可以改善環境溫度變化、元件老化與電流漂移的問題,得到更穩定的 WS。

在另一方面，由於光纖具有頻寬大、損耗小等優點，所以為了在未來能提供更快的頻寬與更有彈性的服務，利用光纖作為傳輸介質網路將為必要的選擇，同時為了能使光纖傳送資料更有效率與增加通道容量，使用了波長分段多工(Wavelength-division multiplexing, WDM)的技術，根據不同的需求又可以分為 DWDM 與 CWDM[6][7]，這些運用技術都需要很多的通道，這些通道分別由雷射來產生，所以根據不同的規格所需要的雷射也不同，但是可以知道的是我們需要一個穩定的可調式雷射[8]。因為在 DWDM 系統中，有超過一百個以上的通道在傳輸，每個波長間隔會小於 50GHz，所以我們需要一個精準的雷射來提供可調的波長。在 DBR 雷射中最常見的是利用三個電極來控制輸出的波長，可利用不同的電極所加入的電流來調整輸出的波長[9-14]，但是同一個 ITU-Band 有好幾組的電流組合可以調整到所需的範圍，而實際的應用上只能挑出一組能夠使用的電流，但是有這麼多組的電流組合要如何挑選一個最合適的電流是很值得討論的問題。

三、 研究方法

1. PID 控制器設計

(1). 系統描述

雷射等效模型是使用**[5]**中所提出的架構如**圖 1** 所示，在此架構中考慮了外部溫度的效應與元件熱效應的等效模型，在[5]中也提出一個 *Photodetector*(VT-WSPD)的架構並利用外部電壓(V)的微調來控制輸入波長(λ)與輸出電流(I)之間的關係經由回授迴路進而減少雷射輸出波長的影響，在此架構需要一個穩定的外部電壓源提供給 Photodetector，在這我們在迴路中

加入 PID 控制器的分析來增進整體的波長穩定性

(2). 系統之穩態與暫態分析

在設計 PID 控制器前，我們需要先將圖 1 轉換為所圖 2 以方便分析 PID 控制器，接著我們要將圖 2 中 Temperature、Thermal stage 與 Laser model 對於輸出波長的影響的轉移函數先求出，我們將對於輸出波長影響分為兩大部份第一部份為暫態分析，為室溫隨時間的變化(△T)對於輸出波長(△λ)的影響的轉移函數，如下所示:

$$\pounds\left[\Delta\lambda\big|_{\sin usoidal}\right]=[a]\ \pounds[\Delta\lambda]$$

where

$$a=\frac{b\times k(s)\times m_p A\times G_1(s)\times m_{laser}+m_{laser}}{1-k(s)\times m_p A\times G_1(s)\times m_{laser}\times(m^*_{PD}+\Delta_{MPD})}$$

由於△T是隨著時間變化所以此項轉移函數可得到當T變化時對於輸出△λ的影響。

第二部份為穩態分析，其中包括 Photodetector(PD)、Thermal stage(TS)、Room Temperature 對於雷射輸出波長的影響其轉移函數，如下所示:

$$\pounds\left[\Delta\lambda\big|_{offset}\right]=[b]\pounds[a+cv+dv^2+bT^*]$$

$$+[\frac{G_1(s)\times m_{laser}}{1-loop\_gain}]\pounds[\ell_p]$$

$$+[c][G_2(s)\times\pounds[q_\ell]+\pounds[T^*]]$$

where

$$b=\frac{k(s)\times m_P A\times G_1(s)\times m_{laser}}{1-loop\_gain}$$

$$c=\frac{m_{laser}}{1-loop\_gain}$$

最後我們將穩態與暫態對於△λ的總效應之轉移函數列出，如下所示:

$$\pounds[\Delta\lambda]=\pounds\left[\Delta\lambda\big|_{\sin usoidal}\right]+\pounds\left[\Delta\lambda\big|_{offset}\right]$$

(3). PID 控制器的演算法

我們要分析所需要的 PID 控制器，首先利用參數λ_0，m_pA，m_{laser}，m_{PD}，b，$(a+cV+dV^2)$，T^*，A_T 與 w^*

來設計一個一階回路轉移函數 $G_1(s)=\frac{1}{s-p}$ 與

一個 PID 控制器 $K(s)=\frac{K_1(s)}{s}=\frac{as^2+a_1s+a_0}{s}$

接著根據所設計的 PID 控制器，我們得到波長的漂移量如下所示:

$$\Delta\lambda\ \big|_{offset}=\frac{a+cV+dV^2+bT^*}{m_{PD}}+\lambda_0$$

$$\Delta\lambda\ \big|_{\sin usoidal}=0$$

由上面的結果可得到，此雷射等效模型加入 PID 控制器後可將溫度隨時間變化對於輸出波長的影響減少至 0，並且得到 Photodetector(PD)、Thermal stage(TS) 與 Room Temperature 對於輸出△λ的 offset 的影響。

2. DBR 雷射電流最佳組合分析

所選用的是常見的三個電極 DBR Laser，只使用單一邊光柵區與共振腔的縱模(Longitudinal Modes)與增益頻譜(Gain)的加乘效果，其中三個電極分別為 Phase 區、Grating 區、Active 區。在實際的應用上我們會將 Ia(Active)固定，利用 Ig(Grating)與 Ip(Phase)的調整的方式來對應出標準波長通道，在同一個標準波長通道中可由許多不同的電流組合所產生，通常在實驗或模擬中我們可以利用電

流掃描的方式來找出所需要的 ITU-Band 與電流組合，如圖 3 所示，這是當 Ia 固定在 40mA 時 Ig 由 3mA 變化至 15mA 且 Ip 由 0mA 變化至 10mA。

(1).系統模擬方塊圖

將雷射參數設定好後還需要建立所需要的模擬方塊圖，在模擬方塊圖方面分為兩個部份，第一個部份為Sweep的量測，如圖4所示(其中之DBR元件由右至左分別為Active區、Phase區以及Grating區。)、第二部份各種電流組合Chirping與Switching Time的量測，如圖5所示。Sweep 量測試用來找出所有可能的電流組合，並將所有的組合紀錄用來做分析用，Chirp 與 Switching Time 的量測用來觀察各種電流組合，所造成的 Chirp 與 Switching Time 的大小。

(2).模擬的方法

a. 模擬參數設定(Simulation Parameter Setup)

Active 區所提供的電流 Ia 固定為 40mA、Grating 區所提供的電流 Ig 由 2mA 變化至 15mA 每次變化 0.2mA、Phase 區所提供的電流 Ip 由 0mA 變化至 15mA 每次變化 0.2mA，所設定的 ITU-Band 在 1544.53nm、1543.73nm、1542.94nm 與 1542.14nm 四個 Channe1。

b. Sweep 模擬(找出對映至 ITU Band 的所有電流組合)

我們需先找出符合 ITU-Band 的所有電流組合，將 Active 區之電流設為固定的 40mA 之後，將 Grating 區以及 Phase 區的電流設定在範圍內使用 Sweep、電流遞增之方式(當 Ig 的電流每增加 0.2mA，Ip 的電流由 0mA 變化至 15mA 每次變化 0.2mA)，找出符合 ITU-Band 的電流組合，並從中挑選出較合適的電流組合(合適的定義為，產生 ITU-Band 均在平坦的區域並非跳動的瞬間所取樣到的值)。

如表 3 為挑選出符合 ITU-Band 的電流組合，為了分析容易我們只挑選符合 ITU-Band 的其中五組電流組合，用來做 Chirp 與 Switching Timee 的量測。

c. Chirping 與 Switching Time 的模擬

(模擬 ITU Band 的所有電流組合所產生的 Chirp 與 Switching Time)

Chirp 與 Switching Time 的量測是利用不同的 Channel 的跳動與不同的 Ip 與 Ig 組合所做的模擬，我們是利用一個非理想的方波(rising time and falling time)來產生 Ig 與 Ip 跳動之輸入訊號，利用這訊號來使 DBR Laser 在不同的兩個 ITU Band 跳動。我們將 CH1←→CH2、CH1←→CH3、CH1←→CH4、CH2←→CH3、CH2←→CH4 與 CH3←→CH4 各種組合都測出來，並利用量測出來的數值做分析與探討。

四、結果與討論

1. PID 控制器方面

在這我們要用數值分析的方式來分析 PID controller 加入我們的系統後的效能。因為系統加入 PID 控制器後，$\Delta\lambda\big|_{\sin usoidal}$ 項可以有效的控制到零，所以我們只針對 $\Delta\lambda\big|_{offset}=\frac{a+cV+dV^2+bT^*}{m_{PD}}+\lambda_0$ 來分析，我們分兩個部份來討論，首先先討論 PD 中的所提供的外部電壓源不穩定時所造成的雷射輸出波長不穩定，並且分析有加 PID controller 與沒有加 PID controller 之雷射輸出波長變化量如表 1 所示，我們可以看到沒有加入 PID 控制器時，當提供給 PD 之外部電壓源有 5%的變異量時 $\Delta\lambda\big|_{offset}$ 爲 $0.00255nm$ 已經不符合 Spec. 的要求($\Delta\lambda=0.02nm$)，當加入 PID 控制器後，

當提供給 PD 之外部電壓源有 5%的變異量時 $\Delta\lambda\mid_{offset}$ 爲 $0.0047nm$ ，當提供給 PD 之外部電壓源有 10%的變異量時 $\Delta\lambda\mid_{offset}$ 爲 $0.0069nm$ 皆能符何 Spec.的要求並且提供更可靠的輸出波長。

第二部份當元件老化所造成輸出波長的影響，如表 2 所示，當 PD 的元件參數(m_{PD})受到元老化造成有 Δm_{PD} 的變化時，我們將 PID 控制器加入後在 $\Delta\lambda = 0.0103nm$ 的 Spec.下，我們可以忍受元件的元件最大變異量為 0.0013 %.

最後根據上面兩部分的分析我們可以得到當雷射等效模型加入 PID 控制器後在電壓漂移所造成的波長的影響可以增進 76.5 %的效益另外對於元件老化對於波長的影響可以增進 48.5 %的效益。

2. DBR 雷射電流最佳組合方面

我們將所量測到的結果整理後，如圖 6 所示，橫軸為 initial channel 分別為 Channel 1~Channel 4，Final Channel 也分別為 Channel 1~Channel 4，每個 Channel 內再分為五小格，分別為 A~F，分別將表三中 ITU-Band 的電流組合由低排到高，並且填入顏色當 Switching Time 越短時顏色越淺，反之越深。由圖 6 我們可以整理出第一個結果由低的 Channel 跳到高的 Channel(長波長跳到短波長)不同組的電流所造成的 Switching time 只會有些微的差距，當由高的 Channel 跳到低的 Channel(短波長跳到長波長)時不同組的電流所造成的 Switching time 就會有很大的差距，所以當我們要挑選電流時首要的考量反而是考慮高的 Channel 跳到低的 Channel(短波長跳到長波長)時的情況，並且挑選兩組 Channel 間 Ig 與 Ip 差值較小的組合。另一個模擬結果如圖 7 所示，是以 Channel 1 跳到 Channel 3 為說明由兩組電流之 Ip 差值大小，可以看出當不同組之電流組合所造成的 Chirping。當 Channel 1 與 Channel 3 之 Ip 電流差值很大時相對的所造成的 Chirping 也會很大，與 Ip 差值大小成正比，所以當考量 Chirping 大小時我們在許多的電流組合中會挑選 Ip 差值較小的組合。

由以上的分析可以得知若要選擇 Switching time 較小的組合則挑選由短波長跳到長波長時與兩個 Channel 差距較小的 Ip 與 Ig 來決定，若要選擇 Chirping 較小時是由兩個 Channel 之 Ip 差距較小的組合決定，因為每個 Laser 的特性均不同所以我們只列出經驗法則來協助使用著在挑選電流組合時能更有依據。

五、計畫自評

(共發表 Paper 4 篇、Conference 2 篇)

(a) PID 控制器的分析與模擬 (已完成之具體成果 1)

在本計畫中，第一年用於加強波長穩定的設計我們利用 PID 控制器來完成，我們提出理論分析與結果模擬，並且藉由快速穩定的波長來設計更多通道的 DWDM 與 optical switch，並且希望能在第二年開始進行硬體的實現。

(b) DBR 雷射電劉最加組合之分析(已完成之具體成果 3)

本計畫之第一年的研究重點是加強波長穩定的設計，所以我們又提出在不同的 Channel 之間跳動時，搭配不同的組合能找出使雷射輸出波長最穩定的解，在第二年可以搭配，所設計的 PID 控制器來得到更穩定的雷射輸出，提供細統使用。

(c) 智慧型相異質碼多工傳輸系統之設計(已完成之具體成果 2)

利用二種不同相異質數碼彼此不會互相干擾的特性，以相異質數碼(Different Prime Code)相結合的方式，以不影響原有使用者及原有資料為前提下，在原有光纖傳輸系統中，動態加入另外的使用者或其他種類資料，改善質數碼系統容量不足的缺點，進而提昇解碼容量，達成多工目的。提供第二年光網路系統之 MAC 設計時另一種架構，能使網路的使用更有效率。

六、 已完成之具體成果：

1. **Yang-Han Lee**, Yung-Shan Chou, Ming-Hsueh Chuang, Chun-Liang Yang, and Hsien-Wei Tseng "PID Controller for Stabilizing Laser Wavelength," Journal of Optical Communications. **(Accepted on April 4, 2006) (EI, Engineering)**
2. **Yang-Han Lee**, Yih-Guang Jan, Hsien-Wei Tseng, and Ming-Hsueh Chuang, "Performance Analysis and Architecture Design for a Smartly Generated Prime Code Multiplexing System," Journal of Optical Communications. **(Accepted on April 4, 2006) (EI, Engineering)**
3. **Yang-Han Lee**, Chun-Liang Yang, Ming-Hsueh Chuang, Hsien-Wei Tseng,Yung-Shan Chou, Hen-Wai Tsao, and San-Liang Lee, "Analysis and Selection of Optimum Driving Current Combinations for Tunable Wavelength Laser," *Microwave and Optical Technology Letters* Volume 48, number 7, July 2006.**(SCI, EI, Engineering)**
4. **Yang-Han Lee**, Yih-Guang Jan, Hsien-Wei Tseng, Ming-Hsueh Chuang, Chiung-Hsuan Peng, Wei-Tsong Lee, and Chih-Tsung Chen, "A Novel Architecture for High Speed Viterbi Decoder," *Tamkang Journal of Science and Engineering* . **(Accepted on January 16, 2006) (EI, Engineering)**
5. Liang-Lin Jau, **Yang-Han Lee**, Yin-Guang Jan, Ming-Hsueh Chuang, Hsien-Wei Tseng, Min-Ju Wen, Chiung-Hsuan Peng, and San-Liang Lee, "The Design And Simulation of Optical Synchronous Code Division Multiplexing System with Balanced Encoder," *11th International Conference on Fuzzy Theory and Technology (FTT 2006) in conjunction with 9th Joint Conference on Information Sciences (JCIS 2006)*, Kaohsiung, Taiwan, R.O.C., October 8-11, 2006. (Submitted on April 15, 2006)
6. **李揚漢**, 楊淳良, 莊明學, 周永山, 曾憲威, 彭瓊萱, 溫敏如 "DBR 雷射波長之驅動電流組合最佳化分析," *台灣光電科技研討會 (OPT 2005)*, December 9-10, 2005.

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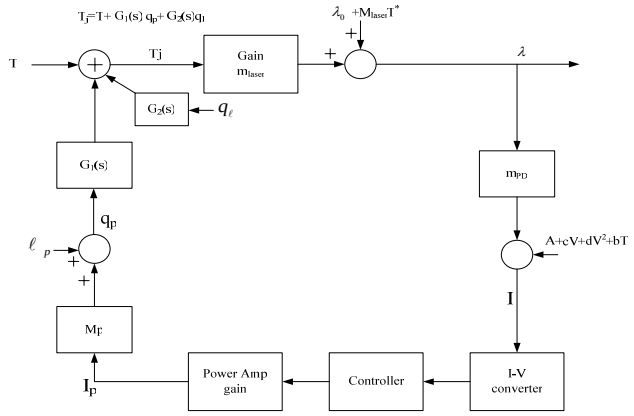

圖 1. 雷射模組的方塊圖。

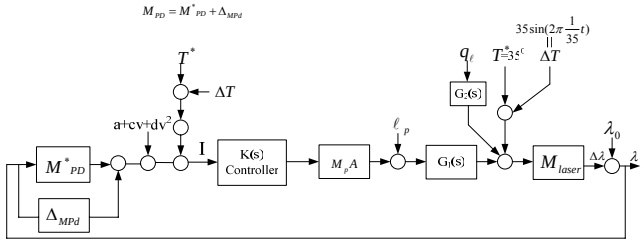

圖 2. 用於PID控制器分析之雷射模組方塊圖。

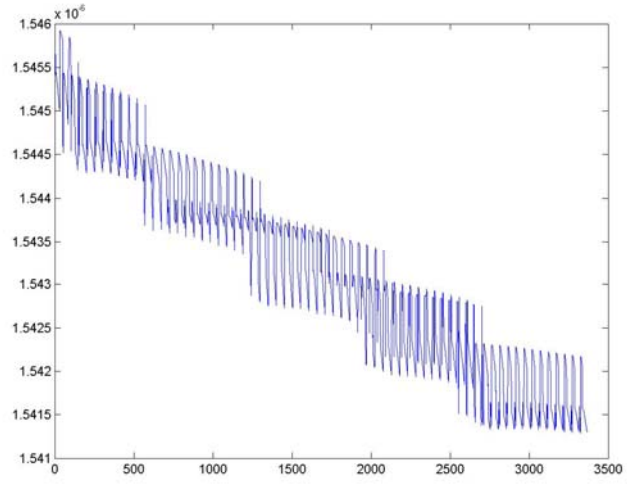

圖 3. Ia 固定為 40mA、Ig 由 2mA 變化至 15mA 每次變化 0.2mA、Ip 由 0mA 變化至 15mA 變化 0.2mA，所觀察到之雷射輸出波形。

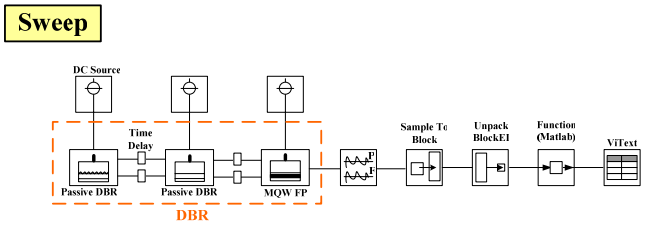

圖 4. Sweep 模擬方塊圖。

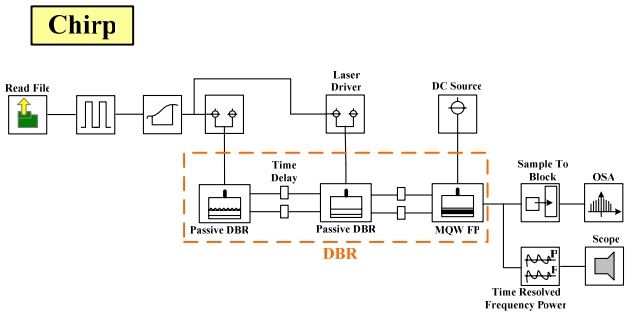

圖 5. Chirping 與 Transient time 模擬方塊圖。

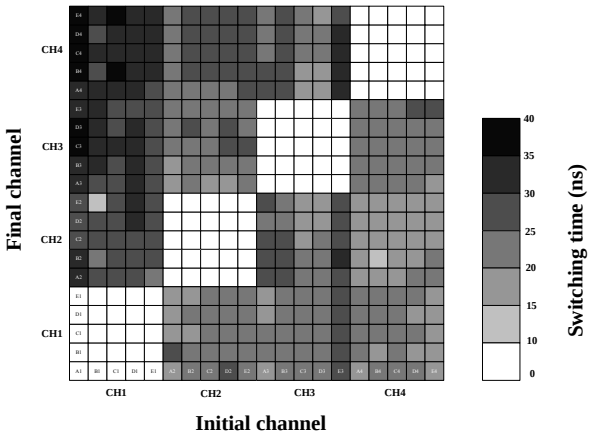

圖 6. Channel 1~Channel 4 之不同電流組所造成之 Switching time。

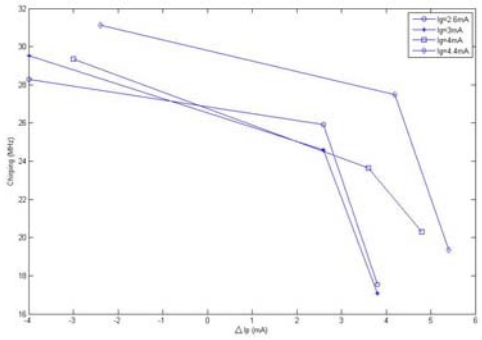

圖 7. 不同的電流組合由 Channel 1 跳到 Channel 3 所產生之 Chirping 的大小。

表 1. 在 V=-4.9359550 mV 與 λ_0=1548.44nm 時，當 V 有 1%～10% 之變化量時，觀察有加與沒加 PID controller 之 $\Delta\lambda\,|_{offset}$ 變化量。

$V\ (mV)$	$\frac{\Delta V}{V}$ %	$\Delta\lambda\,\|_{offset}\ (nm)$ with PID controller	$\Delta\lambda\,\|_{offset}\ (nm)$ without PID controller
-4.93595	0	0	0
-4.98531	1	0.0008	0.0042
-5.23458	5	0.0047	0.0247
-5.42955	10	0.0069	0.0424

表 2. 在 V=-4.9359550 mV 與 λ_0=1548.44nm 時，當元件老化變異量(Δm_{PD})有 0.0005%～0.0013 % 之變化量時，觀察加入 PID 控制器後之 $\Delta\lambda\,|_{offset}$ 變化量。

Δm_{PD}	$\frac{\Delta m_{PD}}{m_{PD}}$ (%)	$\Delta\lambda\,\|_{offset}\ (nm)$ with PID controller	$\Delta\lambda\,\|_{offset}\ (nm)$ without PID controller
2.043×10^{-3}	0.0005	0.00205	0.0057
4.058×10^{-3}	0.001	0.00065	0.0148
5.275×10^{-3}	0.00 13	0.0103	0.021

表 3.　DBR Laser 符合 ITU-Band 之電流組合。

符合 ITU Band@1544.53nm 之電流組合				符合 ITU Band@1543.73nm 之電流組合			
組別	Ig(mA)	Ip(mA)	Wavelength(nm)	組別	Ig(mA)	Ip(mA)	Wavelength(nm)
A1	2.6	6.2	1544.5352437	A2	5	9.6	1543.7344188
B1	3	6.2	1544.5366977	B2	6	8.8	1543.7363370
C1	4	5.2	1544.5355090	C2	7	7	1543.7348757
D1	4.4	4.6	1544.5333676	D2	7.2	5.6	1543.7365426
E1	4.8	3.6	1544.5362242	E2	7.2	6.2	1543.7364454
符合 ITU Band@1542.94nm 之電流組合				符合 ITU Band@1542.14nm 之電流組合			
組別	Ip(mA)	Ip(mA)	Wavelength(nm)	組別	Ip(mA)	Ip(mA)	Wavelength(nm)
A3	8.2	3	1542.9453116	A4	11	5.4	1542.1445951
B3	9.8	2.2	1542.9452452	B4	13	4.4	1542.1455595
C3	9.8	8.8	1542.9460317	C4	13.6	4	1542.1446068
D3	9.8	10	1542.9461867	D4	14.6	3.2	1542.1437565
E3	11	1.2	1542.9458734	E4	14.8	3	1542.1430111

PID Controller for Stabilizing Laser Wavelength

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Summary

In optical network, laser output is easily influenced by temperature changes, device aging and current drift to affect its wavelength stability. In this paper, we propose by implementing PID controller in laser equivalent model loop and develop its algorithm with theoretical and numerical analysis to control wavelength of the laser output so that its dynamic error can be controlled almost to zero and its dynamic error can also be controlled in satisfying limit.

Key words: optical communication; wavelength stabilizer; semiconductor lasers; proportional integral derivative (PID) controller

1. Introduction

In semiconductor lasers their wavelength stability will be varied due to temperature changes, current drifts and device aging. In optical communication system it needs precise wavelength stability (WS) control to reduce or eliminate interference or cross talk between the adjacent channel and signal dropout. The WS controller used in most systems is expensive with complicate architecture and low flexibility [1]. Of course it has some measures to control the WS by using the commonly used temperature controller but these methods cannot solve the wavelength unstable problem due to the varying bias current and device aging. In recent years in the development of WS control it widely use the Synchronized Etalon Filters or by implementing electronic circuits to lock the resonance of birefringent Fabry-Perot Interferometer and to control the Bragg Wavelength of fiber grating coupled to a Fabry-Perot [2-4]. They use error signal in these methods to control laser tuning and it provides satisfactory wavelength stability. But it is not suitable for use in WDM system when it has large number of channels since its complexities are exponentially growing with the number of channels. In [5] Colace et al proposed the Photo-detector (VT-WSPD) architecture that is based on the wavelength drift detected due to outside temperature and device aging by fine- tune the outside voltage through feedback network to reduce the wavelength drift effect. But in this method it needs a very accurate voltage source to supply the voltage to Photo-detector. In order to solve this problem we propose to include a

robust controller in the laser equivalent model and analyze its algorithm. This method can improve temperature environment, device aging and current drifting problems to get more stable wavelength stability.

The structure of the paper is as follows. In Section II, we will make some transformation of the laser model to transform it into the necessary architecture suitable for analysis of PID controller. It also illustrates the formulas and parameters used in the model. In Section III some mathematical analysis is performed to analyze the transient and stable states of the output wavelength and develop its transfer function. In Section IV we will design and make mathematical analysis of the PID controller that is designed based on the transfer function and parameters developed in Section III. In Section V we will make numerical analysis and performance comparison for the designed architecture. We will then draw a conclusion in Section VI.

2. System Description

The laser equivalent model we use in this paper has the same architecture as proposed in [5] as shown in Fig. 1. In this architecture the outside temperature effect and the device heat effect have been considered in the model. Meanwhile we also propose a new photo-detector (VT-WSPD) architecture and by using fine tune of the outside voltage (V) to control the relation between the

input wavelength (λ) and output current (I) and then via the feedback loop to reduce its effect on the *wavelength* of the laser output .In this paper we include the analysis of PID controller to improve the whole system wavelength stability. We will give some simple explanations and mathematical relations and related parameters to be used in the paper:

Laser source—The output wavelength of the semiconductor laser can be approximately expressed by the following linear relations:

$$\lambda_{laser} = \lambda_0 + m_{laser} T_J \tag{1}$$

Where T_J is the junction temperature, λ_0 is the wavelength at $0°C$ and m_{laser} is the temperature coefficient.

Photodetector—VT-WSPD has been explained in detail in [5] and it can be approximately by the following relation:

$$I(\lambda, T, V) = m_{PD}\lambda_{laser} + a + bT^* + cV + dV^2 \tag{2}$$

The current I versus wavelength λ_{laser} for a given voltage V and temperature T can be realized, parameters m_{pd}, a, b, c have been listed in [5].

Thermal stage—It contains two heat sources (laser and Peltier cell), mounting hardware and the heat sink at the thermal stage. The thermal stage can be stated by the following coupled equations [5].

$$q_p = l_p + m_p I_p \tag{3}$$

$$T_J = T + G_1(s)q_p + G_2(s)q_l \tag{4}$$

Where I_p is the supplied current for the heater, the constant l_p and m_p are specified by the cell manufacturer, T_J is the laser-junction temperature, T is the room temperature, q_p and q_l are heater and laser heat flows, respectively, with $G_1(s)$ and $G_2(s)$ as their appropriate transfer functions.

3. System Steady State and Transient Analysis

Before design PID controller we need transfer Fig. 1 into Fig. 2 to make it easy to analyze the PID controller. We then develop the transfer functions of the effect of temperature, thermal stage and laser model on the output wavelength. We classify the effect on output wavelength into two parts. The first part is the transient analysis it is the transfer function of the effect of the time varying room temperature (ΔT) on the output wavelength ($\Delta\lambda$) it has the following relation:

$$£\left[\Delta\lambda\big|_{\sin usoidal}\right]=\left[\frac{b\times k(s)\times m_p A\times G_1(s)\times m_{laser}+m_{laser}}{1-k(s)\times m_p A\times G_1(s)\times m_{laser}\times(m^*_{PD}+\Delta_{MPD})}\right]£\left[\Delta T\right] \tag{5}$$

In (5), ΔT varies with time therefore this transfer function will generate the effect on output $\Delta\lambda$ when T varies.

The second part is the steady state analysis. It includes the transfer functions of the effects of photo-detector (PD), thermal stage (TS) and room temperature on the output wavelength as

shown in the following:

$$£\left[\Delta\lambda\big|_{offset}\right]=\left[\frac{k(s)\times m_P A\times G_1(s)\times m_{laser}}{1-loop\_gain}\right]£[\text{a+cv+dv}^2+\text{b}T^*]$$
$$+\left[\frac{G_1(s)\times m_{laser}}{1-loop\_gain}\right]£[\ell_p]$$
$$+\left[\frac{m_{laser}}{1-loop\_gain}\right][G_2(s)\times £[q_\ell]+£[T^*]] \quad (6)$$

In (6) it gives the effects of photo-detector, thermal stage and room temperature on the offset of the output $\Delta\lambda$.

Finally the total effect of steady state and transient state on the $\Delta\lambda$ has the following transfer function.

$$£\left[\Delta\lambda\right]=£\left[\Delta\lambda\big|_{\text{sin}usoidal}\right]+£\left[\Delta\lambda\big|_{offset}\right] \quad (7)$$

After having these relating transfer functions we will in the following section to use these transfer functions to design PID controller.

4. Algorithm for PID Controller

In this section, we will analyze the required function of PID controller, we first use parameters λ_0 , m_pA, m_{laser}, m_{PD}, b, $(a+cV+dV^2)$, T^*, A_T and w^* (note: $\Delta T = A_T \sin(w^*t)$) to design the first –order loop transfer function $G_1(s)=\frac{1}{s-p}$ and PID controller $K(s)=\frac{K_1(s)}{s}=\frac{as^2+a_1s+a_0}{s}$ to achieve the following goals:

(1) Closed-loop stability, i.e., all the roots of $s-K_1(s)G_1(s)m=0$ lie in the left half complex

plane (LHP), where $m = (m_p A) \times m_{laser} \times m_{PD}$.

(2) $\Delta\lambda \mid_{offset}$ is as small as possible.

$\Delta\lambda \mid_{\sin usoidal} = 0$, i.e., $\left| K_1(jw^*) G_1(jw^*)(m_p A)b + jw^* \right| = 0$.

(3) Good transient response (settling time, overshoot, etc).

Then we assume $\left| \frac{m_{laser} \times m_{PD}}{b} \right| << 1$ and select appropriate parameters p and to satisfy the following two restricted conditions:

(i) $p < 0$; $a > \frac{-1}{(m_p A)b}$;

(ii) $p > 0$; $a < \frac{1}{(m_p A) \times m_{laser} \times m_{PD}}$.

Let $G_1(s) = \frac{1}{s - p}$ and $K(s) = \frac{as^2 + a_1 s + a_0}{s}$ with the parameters a_1 and a_0 defined by the following formulae

$$a_1 = \frac{p}{(m_p A)b} \tag{8}$$

$$a_0 = \left[a + \frac{1}{(m_p A)b} \right] (w^*)^2 \tag{9}$$

After getting first-order loop transfer function $G_1(s) = \frac{1}{s - p}$ and parameters p, a, a_1 and a_0 for the PID controller $K(s) = \frac{K_1(s)}{s} = \frac{as^2 + a_1 s + a_0}{s}$ we need execute the following verifications :

(1) Check closed-loop stability, i.e., compute the roots of $(1-am)s^2+(-p-a_1m)s+(-a_0m)=0$.

(2) Compute $\Delta\lambda\,|_{offset}$ (according to £[$\Delta\lambda$]).

(3) Compute $\Delta\lambda\,|_{\sin usoidal}$ (according to £[$\Delta\lambda$]).

(4) Compute the overall time response of $\Delta\lambda$.

After these verifications it completes the analysis of PID controller and gets its required relating parameters. Then the wavelength drift has the following amount:

$$\Delta\lambda\,|_{offset}=\frac{a+cV+dV^2+bT^*}{m_{PD}}+\lambda_0 \tag{10}$$

$$\Delta\lambda\,|_{\sin usoidal}=0 \tag{11}$$

From above results we can conclude that when we include PID controller in the laser equivalent model it will reduce the effect of temperature variation with time on the output wavelength to zero and meanwhile it will provide the effect of photo-detector, thermal stage and room temperature on the offset of output $\Delta\lambda$. In the following section we will make comparison and analysis of system performance with respect to these items.

5. Performance Analysis

We will apply numerical analysis method to analyze the system performance when the PID controller in included in the system. When PID controller is included in the system, we can effectively control the term $\Delta\lambda \mid_{\sin usoidal}$ to zero so we need only analyze the term $\Delta\lambda \mid_{offset} = \frac{a + cV + dV^2 + bT^*}{m_{PD}} + \lambda_0$, it can be separated into two terms. First we consider the wavelength variation of the laser output due to unstable outside supply voltage in PID controller. We also analyze the wavelength variation amount of the laser output with and without PID controller implemented in the system as shown in Table 1. It shows that without PID controller and when the output supply voltage varies 5% the offset of $\Delta\lambda$ is 0.0255 *nm* it is beyond the specification requirement of $\Delta\lambda = 0.02nm$ while with PID controller included the offset of $\Delta\lambda$ is 0.0047 *nm* when the outside voltage variation is 5% and it is 0.0069 nm when it has 10% varies. They all meet the specification requirement and provide more stable wavelength of the output laser. The device aging on the output wavelength has the effect as shown in Table 2. When the device parameter m_{PD} of PID controller changes Δm_{PD} and when the PID controller is included with the requirement of $\Delta\lambda = 0.0103\,nm$ the device tolerable variation is 0.0013 %.

From above two parts analysis it shows that when the PID controller is included in the laser equivalent model the system performance has improved about 76.5 % from reducing due effect of voltage drift on the output wavelength while the system performance has improvement of 48.5 %

by reducing the effect due to device aging.

6. Conclusion

In this paper we analyzed the steady and transient states of the wavelength stability of the output laser due to the effects of temperature, current drift and device aging. We also proposed an algorithm to design the PID controller from analysis results. The result of $\Delta\lambda \mid_{\sin usoidal} = 0$ and $\Delta\lambda \mid_{offset} = \frac{a + cV + dV^2 + bT^*}{m_{PD}} + \lambda_0$ have been derived. Finally we made numerical comparison and analysis of the effects of unstable outside supply voltage and device aging on laser wavelength with and without including PID controller in the system. From analysis and simulation it concluded that through the PID controller the system performance has about 76.5 % improvement in the control of unstable outside supply voltage and the tolerable range has improved about 48.5 % from reducing the effect of device aging. In has the advantage of simple and easy in the implementation of PID controller and it will have wide and practical applications in the future optical communications.

7. Acknowledgement

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005, and the funding from Tamkang Unversity for the University-Department joint research project.

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Table 1 With and without PID controller the variation of $\Delta\lambda\,|_{offset}$ when outside supply voltage varies 1% ~ 10% from its nominal value (V=-4.9359550 *mV*, λ_0=1548.4483 *nm)*

$V\ (mV)$	$\frac{\Delta V}{V}\%$	$\frac{a+cV+dV^2+bT^*}{m_{PD}}\ (nm)$	$\lambda_0\,(nm)$	$\Delta\lambda\,\|_{offset}\,(nm)$ with PID controller	$\Delta\lambda\,\|_{offset}\,(nm)$ without PID controller
-4.9359550	0	-1548.4483	1548.4483	0	0
-4.9853145	1	-1548.4433	1548.4441	0.0008	0.0042
-5.2345802	5	-1548.4181	1548.4228	0.0047	0.0247
-5.4295505	10	-1548.3994	1548.4059	0.0069	0.0424

Table 2 With and without controller when the device aging included in the system the variation of $\Delta\lambda\,|_{offset}$ has 0.0005% ~ 0.0013 % variation (V=-4.9359550 *mV*, λ_0=1548.4483*nm*)

Δm_{PD}	$\frac{\Delta m_{PD}}{m_{PD}}(\%)$	$\frac{a+cV+dV^2+bT^*}{m_{PD}{}^*+\Delta m_{PD}}\ (\mu m)$	$\lambda_0\,(\mu m)$	$\Delta\lambda\,\|_{offset}\,(nm)$ with PID controller	$\Delta\lambda\,\|_{offset}\,(nm)$ without PID controller
2.043×10^{-3}	0.0005	-1548.4406	1548.4426	0.00205	0.0057
4.058×10^{-3}	0.001	-1548.4328	1548.4335	0.00065	0.0148
5.275×10^{-3}	0.00 13	-1548.4283	1548.4293	0.0103	0.021

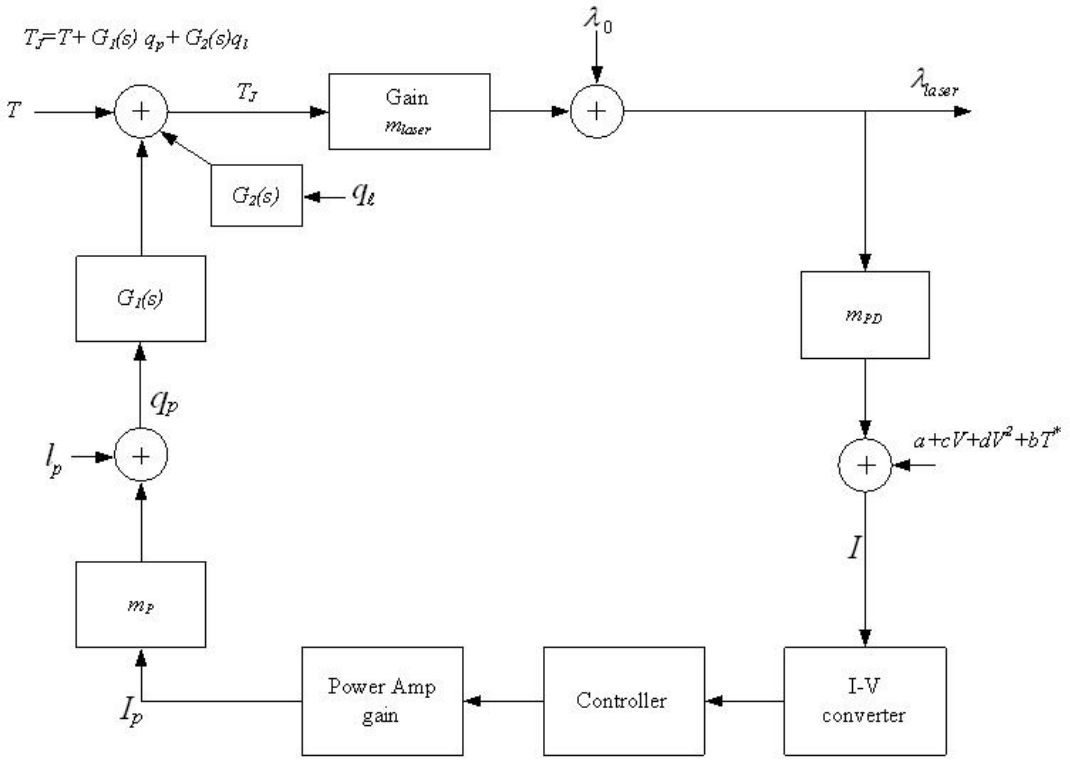

Figure 1 The block diagram for laser model

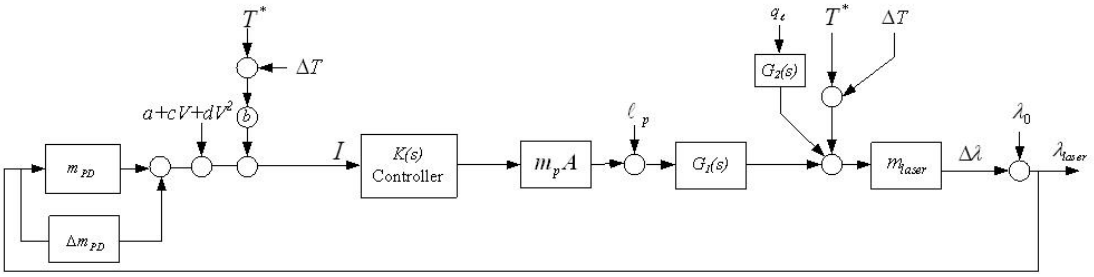

Figure 2 The block diagram for laser model using for PID controller analysis

Performance Analysis and Architecture Design for a Smartly Generated Prime Code Multiplexing System

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Summary

In this paper we present a method to combine different prime codes by using the characteristic that two different prime codes do not interfere with each other. In the code combination it bears the prerequisite that the inserted code should not interfere with the existing users and their transmitting information it then dynamically inserts different kind of information in the existing system to solve the system inadequate capacity problem. By this codes combination it improves the system decoding capacity to achieve the objective of multiple accesses.

Key words: prime code; multiple access; decoding capacity; dynamic; CDMA; optic fiber

1. Introduction

It has been widely discussed in recent years of the techniques used in traditional optic fiber code division multiplexing system [1-3]. It adopts the modified prime codes in its decoding algorithm. It has only P sets of decoding capacity in Asynchronous Code Division Multiple Access (ACDMA) and it has P^2 sets of decoding capacity in Synchronous Code Division Multiple Access (SCDMA). In SCDMA system when the data is spread by prime code the synchronous decoder of every chip can identify more prime codes. For example in P_7 code the ACDMA decoder can identify only 7 codes (P_7 =7) while it can decode 49 codes in SCDMS decoder ($P_7{}^2$ = 49). If we transmit data with the speed of 10G/s it is equivalent with a chip rate of 490 G/sec by spreading with P_7 codes. It is a challenging work to achieve the synchronization in the transmission with high data rate.

By searching literatures and patents it is found that some authors used Digital Wavelength Division Multiplex Optical Transducers to improve decoder performance. Others used Variable Length Code (VLC) to improve decoder performance. In [6] the authors used optic fiber design to provide synchronization so as to improve the system performance. Although some papers [7-10] discussed the use of coder/decoder in the optical code division multiplexing system it is just a few papers discussed the decoder applications in the optic fiber communication system. It

has few papers discussed how to apply the CDMA technique to the wireless communication system. In this paper we will use different prime code system [11-14] to improve the system capacity.

We propose the architectures of Different Prime Code Multiplexer and Different Prime Code Demultiplexer and develop the optimal design of the different prime code multiplexer and system applications to improve the system capacity by inserting smaller prime code signals (P_S) into and co-existing with the larger prime code system (P_L).

2. The Concept of a Smartly Generated Prime Code Multiplexing System

In the Smartly Generated Prime Code Division Multiple Access System it combines P_L and P_S two different prime codes. Suppose in the original system it has N P_7 users, $user_1$, $user_2$ …. and user $_{NP7,}$ they use different P_L codes as their spreading codes at the transmission site and at the receiver they use their corresponding de-spreading codes to decode the transmitting signals. The Monitor Center at the multiplexer will monitor the optic fiber system and search in this system how the P_L codes are used and to decide is it possible to insert certain P_s codes. The Monitor Center will execute the Optimal Design Algorithm from the existing P_L codes to execute certain operations and report its decision to the Multiplexing Control Center that some spaces are available for transmitting information with P_S prime codes. With the ability to insert other spaces

for information transmission it can use P_3 prime codes to transmit other kind of information to achieve the multiple access purpose and consequently the whole system capacity has been increased.

In the optic fiber communication network, the user group originally uses P_L codes as their transmission spreading codes. That is in the information transmission they use corresponding P_L prime codes at the transmitting and receiving sites. After adding multiplexer it will allow users to use different P_S prime codes to transmit different information so that it will simultaneously transmit $P_L + P_S$ prime codes information in this optic fiber communication network. Because we use two different kinds of prime codes with the characteristic that they will not interfere with each other it will not generate any problem for users who do not have de-multiplexer installed they are still able to decode their information by using their corresponding P_L codes. The whole system concept is as shown in Fig. 1. In the concept figure we assume that it has five users in the whole communication network in which two users, user 2 and user 4, have installed different prime codes multiplexers so that they can transmit different kind of information to achieve the multimedia transmission function. Other users without installing the multiplexer will only be able to decode their corresponding prime code information.

2.1 Optimal Prime Code Insert Model

By observing the Sum of seven selected P_7 codes we are looking for a method to insert the

different prime codes and developing an effective decoding process, we have the following observations:

1) In order to insert a P_3 prime code in the system that originally consists entirely of only P_7 codes, it must have a '0' in the sum of P_7 prime codes. On the other hand while their sum comprises of a '0' it does not guarantee that a P_3 prime code can be inserted. Therefore as shown in Figs. 2(A) and 2(B) we can increase the search speed by searching only those locations where the different prime codes might be inserted.

2) As shown in Fig. 2 (C), while inserting a P_3 prime code into the original system if the position for the P_3 code equals 1 and its corresponding position for the Sum of the P_7 primes codes is 0 or larger than 2 then the P_3 prime code can be inserted. On the other hand, if the position for P_3 code equals 1 and its corresponding position for the Sum of the P_7 primes codes is 1 then the P_3 code cannot be inserted. Therefore the decoding time can be reduced to enhance the whole system performance and the speed of inserting different prime codes is increased.

3. Functional Processes in Multiplexing System

When a user in the communication network uses digital data (such as voice) to trigger a laser diode in the primary transmitter/receiver it passes through the delay line logic with proper amount of delay and is encoded as a prime code P_L with a prime index of L. This prime code is

then coupled to the optic fiber. At the receiver after passing through the corresponding delay line logic and the photo detector, a threshold of a proper position is determined through the Chip Synchronization signal that is synchronized with the transmitted signal. If the detected threshold equals the threshold the data is decoded as 1 and if it is less than the threshold then the data is decoded as 0.

As shown in Fig. 3 in the different prime code multiplexing system a secondary transmitter/receiver is added. That is in the original system a smart different prime code multiplexer is added. This multiplexer automatically detects the state of usage in the transmission channel. When they are only a fewer users, it automatically enters into the multiplexing state to allow different kinds of data to transmit simultaneously in the channel. The users can then achieve the objective of multimedia transmissions. For example when the main system is transmitting voice, the multiplexer may simultaneously transmit video images while the channels are not busy. In Fig. 3, the thick solid line, the thin solid line and the dash line respectively represent the optical signal, the electric signal and the control clock.

We use the combination of P_7 and P_3 prime codes as an example to illustrate the system operation. From the consideration of integrating system compatible capacity we propose an optimal design algorithm for the generation of different prime codes system. The system flow chart is shown in Fig. 4.

1) The nominal P_7 prime code system.

2) The Monitor Center based on the combinations of P_7 prime codes used by the current user group to decide is it possible to insert different prime code in the system (the P_3 prime code system)

3) If the different prime codes cannot be inserted then it continuously uses the original P_7 codes.

4) If it is possible to insert different prime codes then by implementing the optimization algorithm to determine which P_3 different code can be inserted. This new P_3 code is then inserted into the original P_7 prime code system through the multiplexer and the system enters into the different prime codes multiplexing state. Then the system can transmit different kinds of information to achieve the multiple access state.

5) Use the corresponding decoder and determine the threshold level to detect it is a signal

6) After all used prime codes are detected as genuine signals and other prime codes not used are not signals then this combination is a correct combination otherwise it is a fail combination.

7) Complete the whole system design

4. The Architecture of Smart Multiplexing System

Based on the aforementioned model of optimal insertion algorithm, we develop the hardware architecture for a smart different prime codes multiplexer as shown in Fig. 5. The solid

line denotes the optical signal and the thin black line represents the transmission medium of the electrical signal. The original data in the optic fiber is coupled to the Optical Decoder Array (ODA) to decode the current users who are occupying the channel. It is then inputted into the Channel Occupied Sensor (COSR). After observing for a period of time it can determine which P_L codes have been used. It then uses the Slot Occupied Sensor (SOSR) to determine which time slots have been occupied. It bases on previous detection result the Overload Decision Device (ODD) will decide whether there are too many users existing in the channel. If the transmission channel is busy the multiplexer will automatically terminate the multiple access state and enter into the state of only P_L prime code can be transmitted. If the channel is not busy it means that it is permitted to enter into the different prime codes multiple access state. It then bases on the information in the Insert Process Unit (IPU) to realize the optimal inserting method by a simple logic structure. It finally utilizes the synchronization between the Insert Control Unit (ICU) and the IPU to determine the location to insert P_S different prime code. Other inserted data are re-coupled into the optic fiber via the coding laser of the IPU. In decoding similar method is used to detect the position and the type of prime code. It then uses the Different Prime Code Decoder (DPCD) to decode the corresponding prime code to complete the whole multiple access process.

5. Performance analysis of Multiplexing System

By implementing the hardware architecture for our designed multiplexing system, we first try to find the threshold value (P_L User) because as mentioned above if P_L User is set too high then the system will be too busy and the number of locations we can insert for the different prime codes are also limited. We use simulations to find the possible best threshold value and with the value found we then identify which prime code group can be inserted in those locations. The information relating to the locations and the prime code group can be inserted will directly affect our architecture design.

In our simulation we use P_7 as the large prime code system and P_3 are the smaller prime codes. We know that the maximum number of users can be used in the system is 7 User. We then use random number generator to determine how many and which users are existing in the optic fiber system and from these to determine how many P_3 prime codes can be inserted in the system. The simulation results are shown in Fig. 6. As shown in the figure it appears that when the users in the system are more than 7 Users it would be able to achieve the objective of multiple access. The parameter can be setting up by user's demand. In Table 1 it shows that with the 7 Users determined it lists how many P_3 prime code users can be inserted. These are important parameters in our hardware architecture design.

6. Conclusion

From simulation results we found that when more users exist in the network the busier the network will be. It is because the search times to find an available location to insert different prime codes is an important factor needs considered be and the possible number of different prime codes can be inserted are reduced correspondingly. From our evaluation when the threshold value for the network users is ser at 4 Users it will not give too much burden to the system because when the system works in this range 4 users it can insert and complex the different codes into the optic fiber network without any problem. It also will not incur any data processing speed too slow problem either. This code division multiple system implemented by different prime codes increases the system transmission capacity. Coupled with hardware architecture of different prime code multiplexer and complete operation few chart it expects that this different prime codes system has widely practical applications in optic fiber system.

7. Acknowledgement

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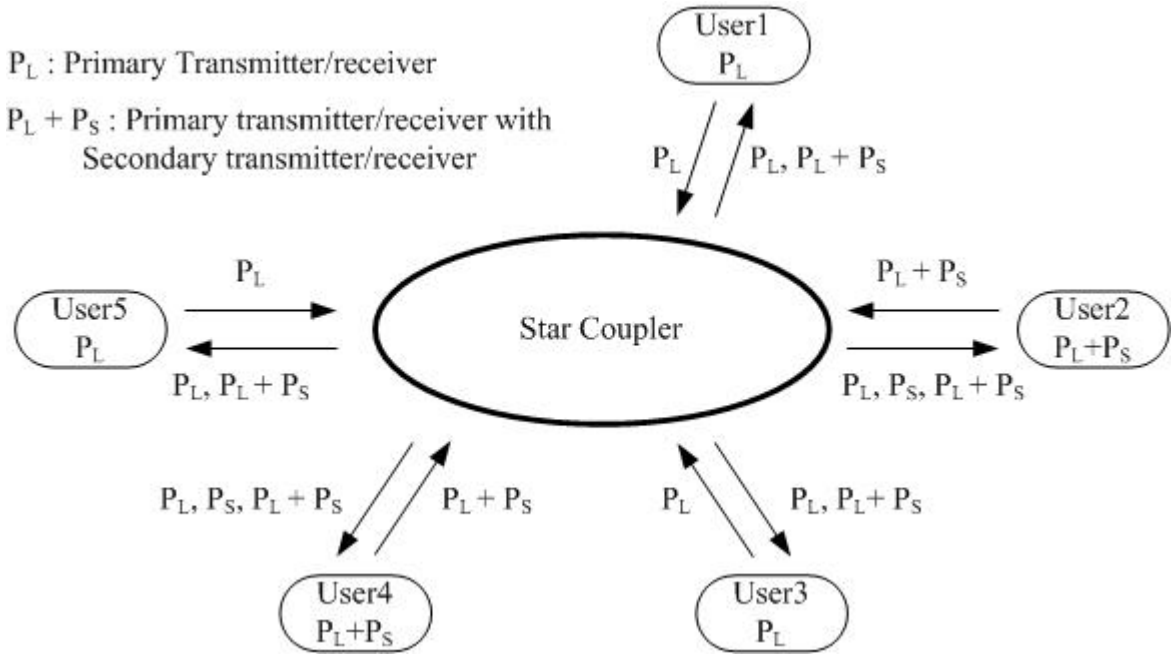

Figure 1. Smartly Generated Prime Code division multiple access system

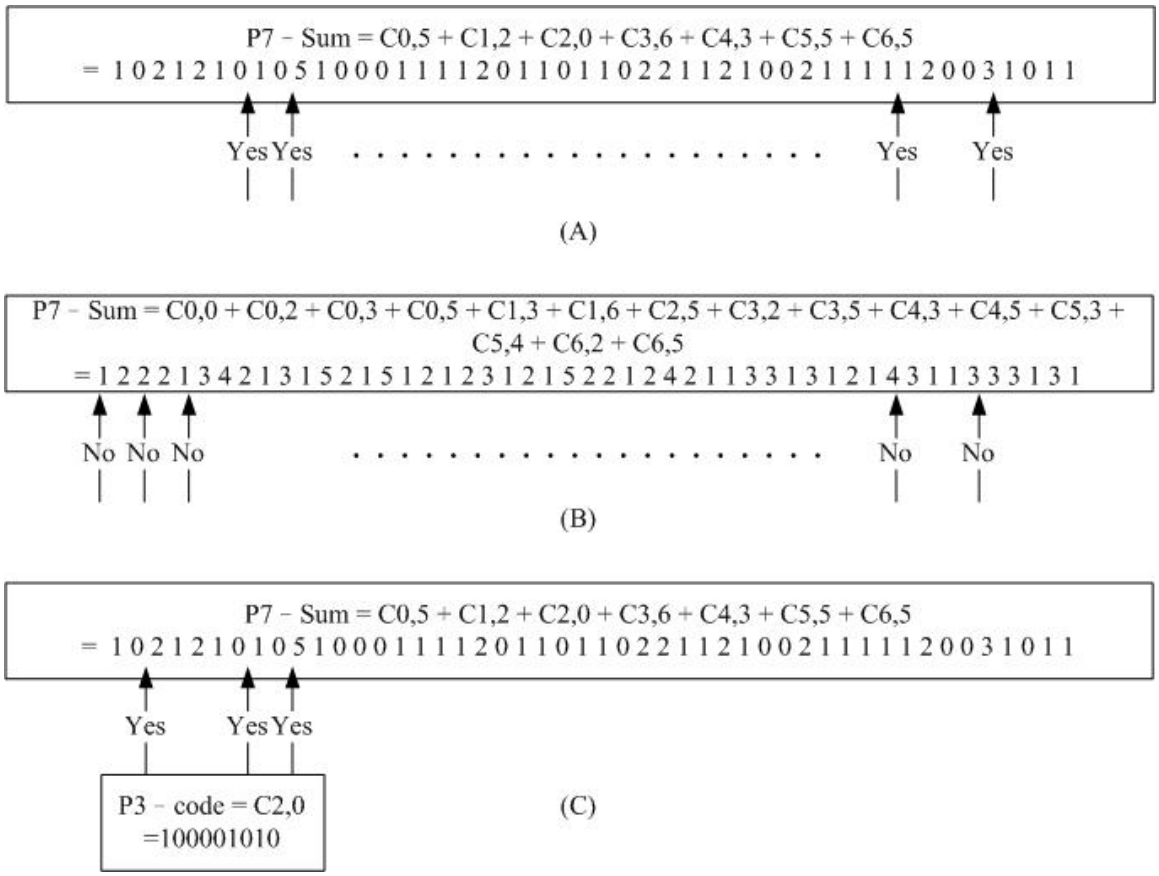

Figure 2. Optimal Smartly Generated Prime Code Insert Model

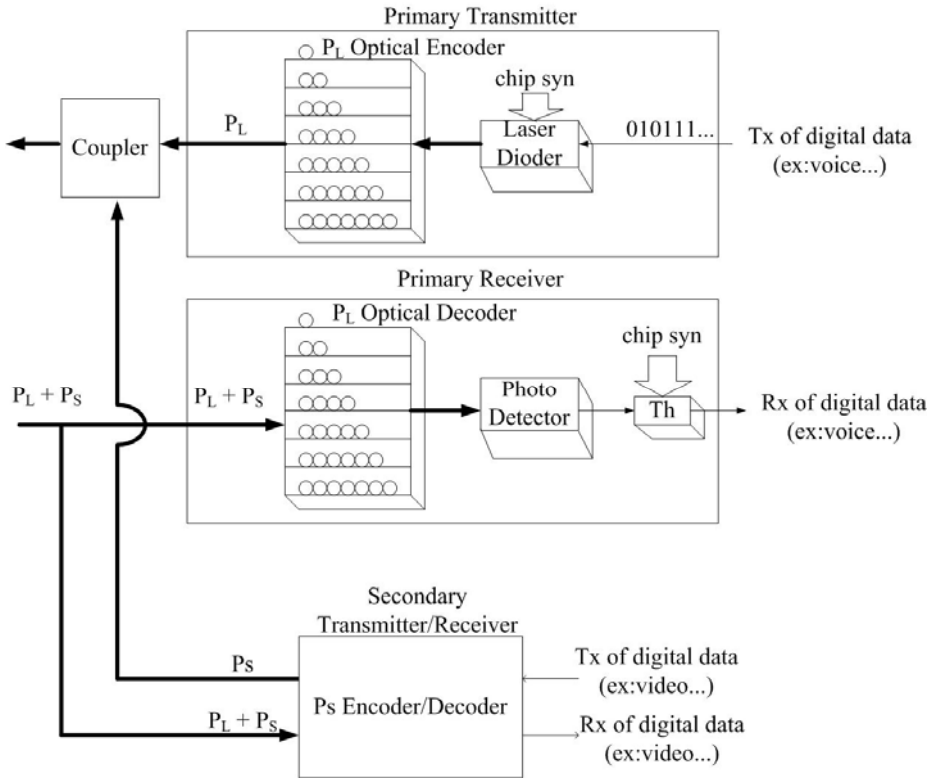

Figure 3. Smartly Generated Prime Code Multiplexing System Architecture

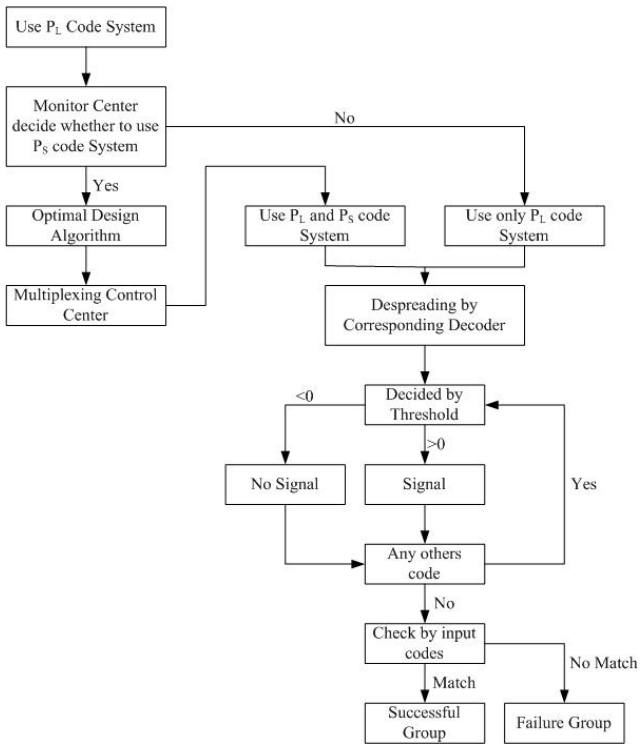

Figure 4. Multiplexing System Flow Chart

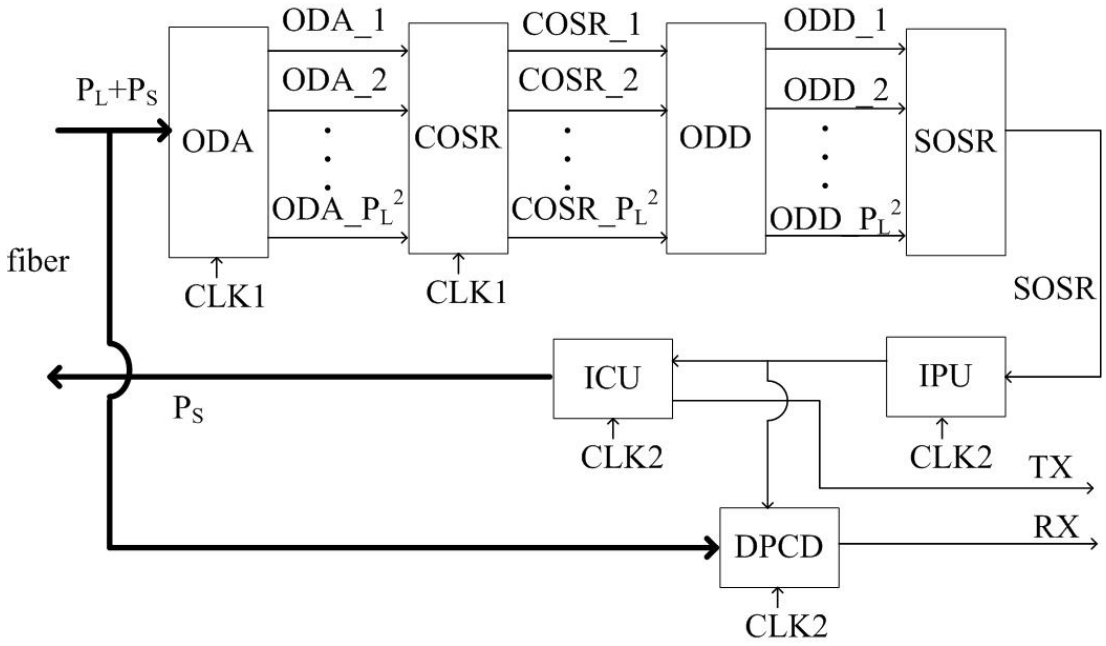

Figure 5. P_S Encoder/Decoder hardware architecture

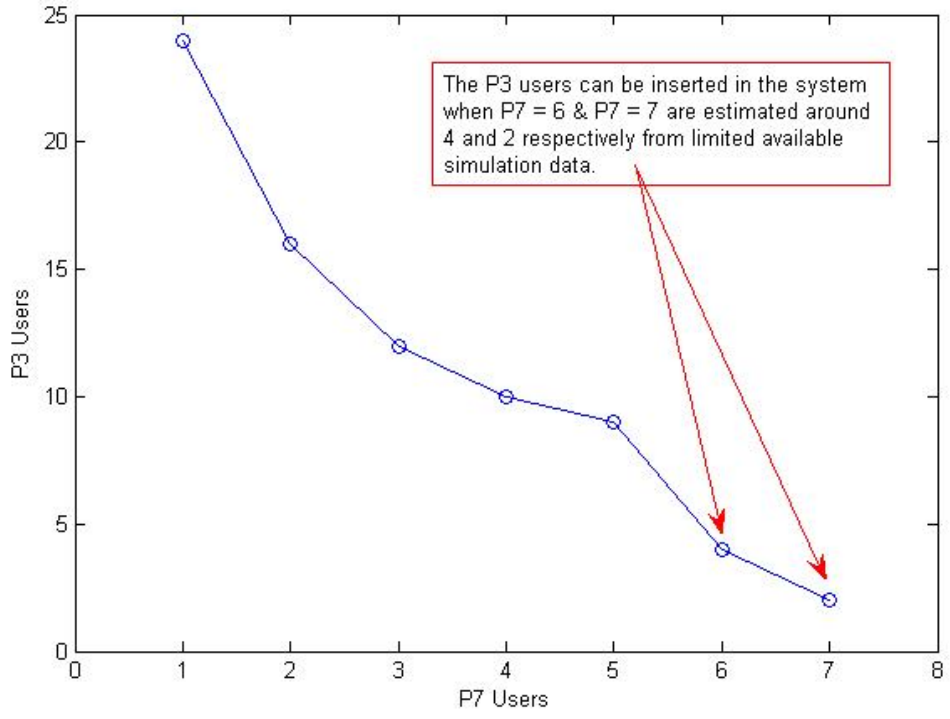

Figure 6. Different P_3 prime codes can be inserted in the P_7 system

Table 1. Different P_3 prime codes can be inserted in the P_7 system

P7 Users	P3(0,0)	P3(0,1)	P3(0,2)	P3(1,0)	P3(1,1)	P3(1,2)	P3(2,0)	P3(2,1)	P3(2,2)	Average	Note
1	25	25	25	25	24	24	24	24	24	24	
2	17	17	17	16	16	16	16	16	16	16	
3	12	12	12	12	12	12	12	12	12	12	
4	10	10	10	10	10	10	10	10	10	10	
5	9	9	9	9	9	9	9	9	9	9	
6	4	4	4	4	4	4	4	4	4	4	(*)
7	2	2	2	2	2	2	2	2	2	2	(*)

(*) The P_3 users can be inserted in the system when $P_7 = 6$ & $P_7 = 7$ are estimated around 4 and 2 respectively from limited available simulation data.

only the amplitude spectrum to demodulate the cavity parameters. The experimental results were found to agree well with the synthesized ones from the demodulated parameter at or near the centre wavelengths of FBG 1 and FBG 2; however, the experimental results deviate from the synthesized ones when the wavelength is outside the centre wavelengths of FBG 1 and FBG 2. This behaviour is believed to be due to the nonuniformity of the FBGs' parameters along their length.

ACKNOWLEDGMENTS

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ANALYSIS AND SELECTION OF OPTIMUM DRIVING CURRENT COMBINATIONS FOR TUNABLE WAVELENGTH LASER

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ABSTRACT: *In a distributed Bragg reflector (DBR) laser, driving currents in the tri-electrode are adjusted to generate various channels in the ITU-Band. Many driving-current combinations can generate the same ITU channel. But when we take system performance into consideration, such as the chirping and the switching time when we switch DBR lasers between ITU channels, certain current combinations will generate better system performance than the others. In this paper, we develop the principle of how to select current combinations in order to obtain better system performance and also discuss the method of how to evaluate the system performance when different current combinations are selected.* © 2006 Wiley Periodicals, Inc. Microwave Opt Technol Lett 48: 1417–1423, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21643

Key words: *tunable diode laser; distributed Bragg reflector (DBR); laser; chirping*

1. INTRODUCTION

With the rapid development of information transmission and various applications of Internet networks, the demand for information bandwidth has enormously increased. The advantages of wide bandwidth and low signal attention make optic fiber the sole choice of transmission medium to provide fast and wide bandwidth and reliable service. Meanwhile, in order to efficiently transmit information and increase the channel capacity in optic-fiber transmission, we use the technique of wavelength-division multiplexing (WDM). It can be further divided according to various requirements into two categories: DWDM and CWDM [1, 2]. No matter which technique is selected, many channels are always needed for information transmission. Lasers are used to generate these channels; therefore, when we have different specification requirements, we need various laser sources. But we all realize that a reliable and tunable laser is necessary [3]. Specifically, a DWDM system uses more than 100 channels to transmit information and the separation between channels is less than 50 GHz; a precise laser source is needed in order to generate tunable wavelength.

DBR lasers usually employ a tri-electrode to control output wavelength. Or, more precisely, they use currents generated from different electrodes to control the output wavelength [4–10]. In one ITU band, there are many current combination sets that can be adjusted to the defined channel band. But in practical applications, we can select and implement only one set of current combinations; thus, the question arises: how do we select the most proper set of current combinations among many possible available sets?

In this paper, we find the combinations between the corresponding current and wavelength in tri-electrode DBR laser with output laser frequency falling in the specified channel band. Also, through simulation we discuss the stability issue of the output DBR laser when it is generated from different current combinations. Finally, we propose certain rules in the selection of current combinations for future system implementation. This paper is organized as follows. In section 2 we discuss the problems it may

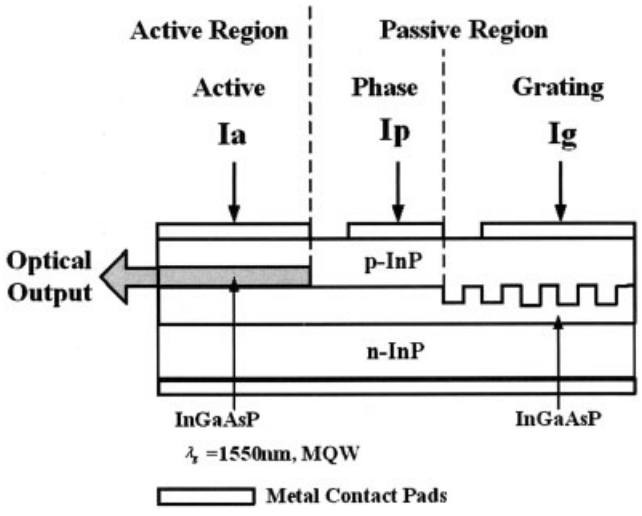

Figure 1 Basic architecture of the DBR laser: from right to left: the grating zone, the phase zone, and the active zone. The grating zone is used to select the source wavelength, the phase zone is to fine tune the laser wavelength, and the active zone is to provide laser power gain

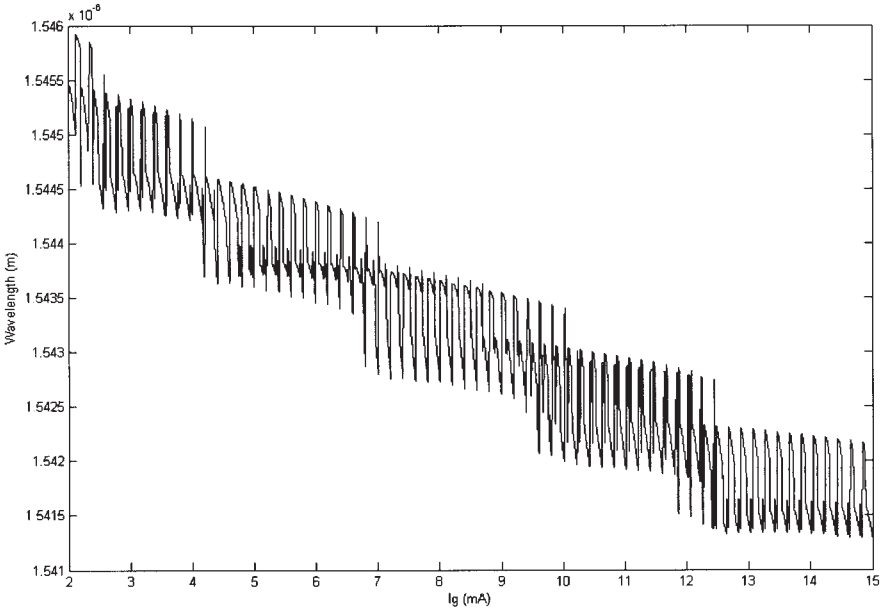

Figure 2 I_a is fixed at 40 mA, I_g varies from 2 to 15 mA in step sizes of 0.2 mA, I_p varies from 0 to 15 mA in step sizes of 0.2 mA

encounter when we implement the DBR laser. Section 3 introduces some basic specifications of DBR laser which will be used as certain parameters in the simulation. In section 4 we discuss thesimulation method and procedures for simulating chirping and switching time. We analyze the simulation results and propose the empirical rules for the selection of current combinations in section 5. The conclusion is drawn in section 6.

2. PROBLEMS IDENTIFICATION FOR DBR LASER

Figure 1 shows a typical tri-electrode DBR laser, which uses only one side of the light grating zone, the longitudinal modes in the resonant cavity, and the multiplication effect of the spectral gain. The three electrodes are the phase zone, the grating zone, and the active zone. This kind of laser has the characteristics of being easy to operate, simple in architecture, and simple to fabricate compared with other kinds of DBR lasers. However, its tunable wavelength range is rather limited and is suitable for local area network applications.

The tri-electrode DBR laser uses the biased driving currents I_p, I_a, and I_g from the phase, grating, and active zones, respectively, to adjust its output laser wavelength. The range of the laser bandwidth can be adjusted has the following relationship:

$$\frac{\Delta\lambda_m}{\lambda_m} = \frac{\Delta\bar{n}_a L_a + \Delta\bar{n}_p L_p + \Delta\bar{n}_{DBR} L_{eff}}{\bar{n}_a L_a + \bar{n}_p L_p + \bar{n}_{DBR} L_{eff}}, \quad (1)$$

where λ_m is the laser operating central frequency, $\Delta\lambda_m$ is the range the laser bandwidth can be adjusted, $\bar{n}_a$, $\bar{n}_p$, and $\bar{n}_{DBR}$ are the affected index due to the injection of current or voltage, and L_a, L_p, and L_{DBR} are the lengths in the laser three working zones. Therefore, we can use currents in different zones to control the output wavelength.

The active zone is driven by the I_a current to adjust the output laser power, the I_g current provides the current in the grating zone to adjust a wide range of laser wavelength, while the I_p current in the phase zone is used to fine tune the output wavelength. Various combinations of these three driving currents can be used to adjust the output laser wavelength to provide channels with specifications meet the International Telecommunication Union (ITU-T) G692 requirements. In the practical implementation we will adjust currents I_g and I_p, while keeping I_a fixed, so as to generate a channel with standard wavelength. Many possible combinations of these three driving currents may be used to generate a channel with the same wavelength. In the laboratory measurement or in the simulation test, we can use the current-sweeping method to find appropriate combinations among driving currents to generate channels in the ITU-Band, as shown in Figure 2. To obtain the result, we keep the I_a current at 40 mA, and vary the I_g current from 3 to 15 mA and the I_p current between 0 to 10 mA. It is quite an effort to find the proper current-combination sets for generating a laser source in the ITU band. Furthermore, for any channel in ITU band, sometimes it can be generated from more than one current-combination sets. In conventional implementation there is no standard rule or specification of how to select a current-combination set from many possible sets to attain the best system performance. In the following sections, we discuss and solve this problem based on analysis and simulation of the DBR laser system.

3. SIMULATIONS STRUCTURE FOR DBR LASER SYSTEM

In this section we introduce all relevant laser parameters and present the functional blocks for system simulation test using VPI simulation platform. First, we choose the tri-electrode DBR laser

TABLE 1 Basic Physical Parameters of DBR Laser

Parameters\Section	Grating Section	Phase Section	Active Section
Laser chip length	175E-6 m	50E-6 m	320E-6 m
Active region width	1E-6 m	1.5E-6 m	1E-6 m
Active region thickness	0.25E-6 m	0.25E-6 m	0.2E-6 m
Group effective index	4.3	4.3	4.3
Left-facet reflectivity	1.2E-12	0.001	0.001
Right-facet reflectivity	1.2E-12	0.022	0.022
Nominal wavelength	1.550E-6 m	1.550E-6 m	1.550E-6 m

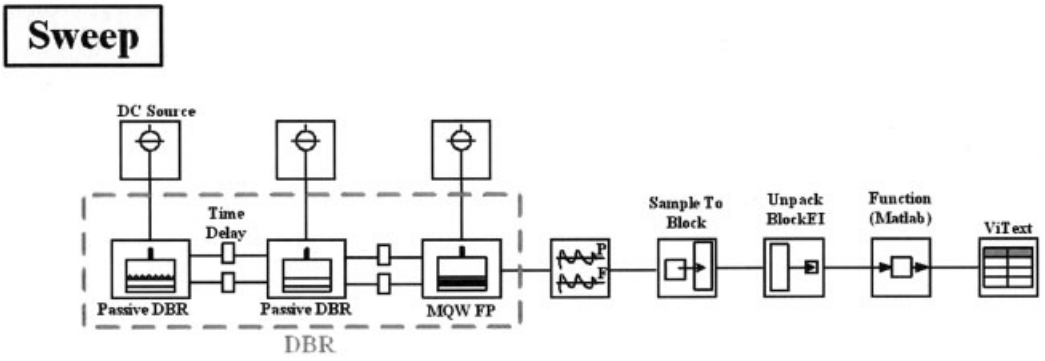

Figure 3 Simulation: functional block diagram for sweeping channels

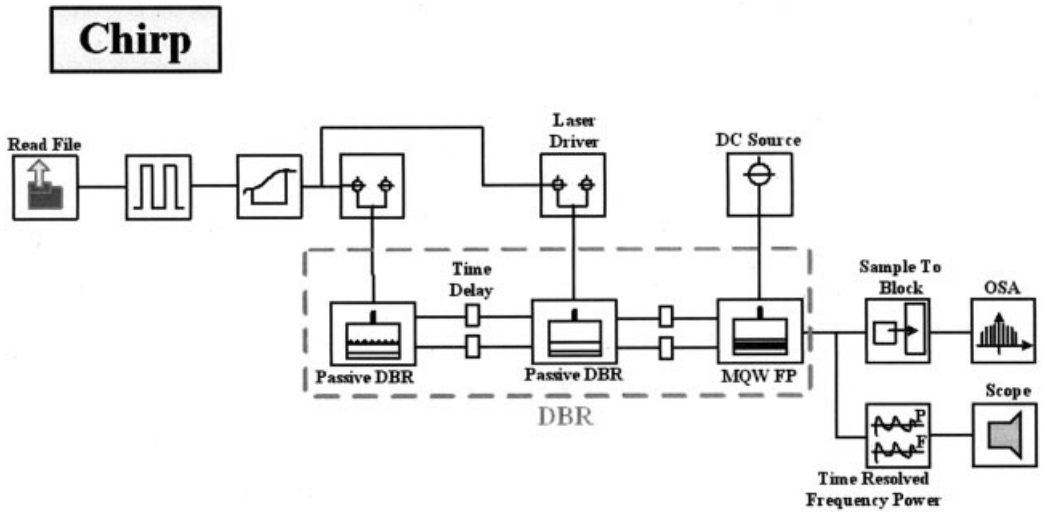

Figure 4 Simulation: functional block diagram for chirping and switching time

to have working wavelength $\lambda_m = 1550$ nm. The total laser length is $L_a + L_p + L_{DBR} = 545$ μm, the tri-electrode has length $L_p = 50$ μm in the phase zone, $L_{DBR} = 175$ μm in the grating zone, and $L_a = 320$ μm in the active zone. The active region in the tri-electrode has width 50 μm in the Phase zone, 175 μm in the grating zone, and 320 μm in the active zone. Other relevant parameters are listed in Table 1.

After the basic laser parameters are set, the next step is to build the simulation functional blocks, divided into two parts. The first part of the functional blocks is the current-sweeping measurement, as shown in Figure 3. In the figure, the components of the DBR laser from right to left are the active zone, the phase zone, and the grating zone. The second part of the functional blocks involves the measurements of chirping and switching time, as shown in Figure 4.

The current-sweeping measurement has the task to find and record all possible current combinations and then analyze these records. The chirping and switching time measurements are done to find the effect or magnitude of the chirping and switching times from all considered current combinations.

4. SIMULATION METHOD

In this section, we determine all possible I_g and I_p current combinations in order to generate output laser in the defined ITU band. From these current combinations, we also measure their corresponding chirping and switching time when the currents are swept across two different channel bands. From these measurements, we select certain current-combination sets and analyze their performance. The simulation of the current-sweeping part is introduced first, and then the simulation of chirping and switching time in the sequel is discussed.

4.1. Set Up of Simulation Parameters

Before the simulation, we need to consider and set up the required driving-current range of the tri-electrode. The current provided from the active zone, I_a, is kept at 40 mA; the current provided from the grating zone, I_g, is varied from 2 to 15 mA within step sizes of 0.2 mA; and the current provided from the phase zone, I_p,

TABLE 2 Set Up of the Simulation Parameters For Generating DBR Laser

ITU Band	CH1	1544.53 nm	CH2	1543.73 nm
	CH3	1542.94 nm	CH4	1542.14 nm
I_a	40 mA (fixed)			
I_g	2–15 mA (0.2-mA steps)			
I_p	0–10 mA (0.2-mA steps)			
Purpose	From the conditions specified above for I_a, I_g, and I_p and by using the sweeping method, find four channels in the ITU band and also analyze its chirping effect			

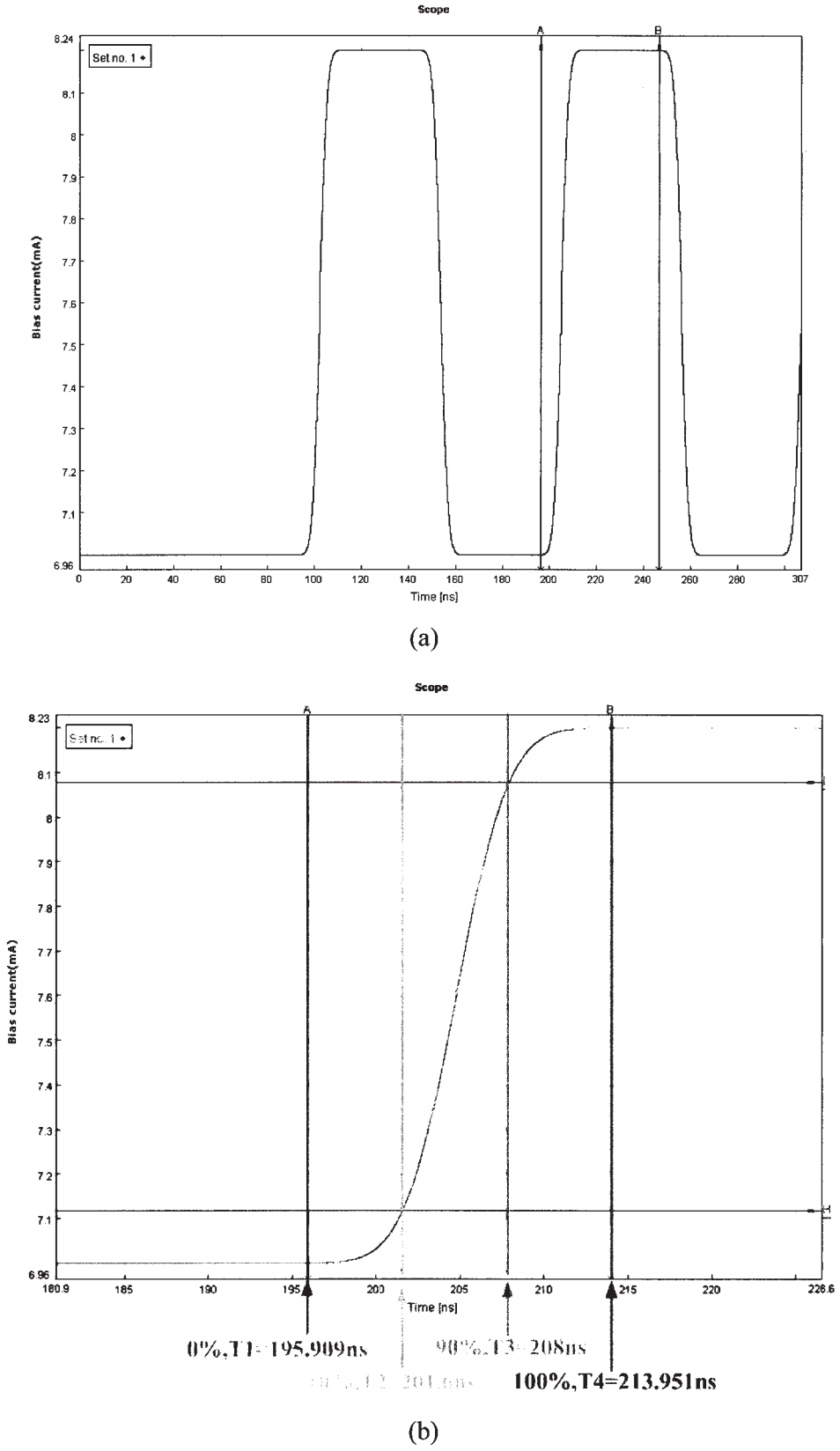

Figure 5 Input laser signals for measuring (a) chirping and (b) switching time

is varied from 0 to 15 mA and, also in step sizes of 0.2 mA. Four ITU band channels are selected and their wavelengths are set at 1544.63, 1543.73, 1542,94, and 1542.14 nm. The currents are swept in the ranges as discussed above and their corresponding chirping and switching-time values are measured.

4.2. Currents Sweeping

All possible current combinations, which will generate lasers in the considered ITU band, are searched and selected. The parameters of the current sweepings are specified in Table 2. The current in the active zone is set at 40 mA, and the sweeping currents are in-

TABLE 3 Current Combinations in DBR Laser to Generate Lasers in ITU-Band

Current Combinations for ITU Band at 1544.53 nm				Current Combinations for ITU Band at 1543.73 nm			
Set	I_g [mA]	I_p [mA]	Wavelength [nm]	Set	I_g [mA]	I_p [mA]	Wavelength [nm]
A1	2.6	6.2	1544.5352437	A2	5	9.6	1543.7344188
B1	3	6.2	1544.5366977	B2	6	8.8	1543.7363370
C1	4	5.2	1544.5355090	C2	7	7	1543.7348757
D1	4.4	4.6	1544.5333676	D2	7.2	5.6	1543.7365426
E1	4.8	3.6	1544.5362242	E2	7.2	6.2	1543.7364454

Current Combinations for ITU-Band at 1542.94 nm				Current Combinations for ITU-Band at 1542.14 nm			
Set	I_p [mA]	I_p [mA]	Wavelength [nm]	Set	I_p [mA]	I_p [mA]	Wavelength [nm]
A3	8.2	3	1542.9453116	A4	11	5.4	1542.1445951
B3	9.8	2.2	1542.9452452	B4	13	4.4	1542.1455595
C3	9.8	8.8	1542.9460317	C4	13.6	4	1542.1446068
D3	9.8	10	1542.9461867	D4	14.6	3.2	1542.1437565
E3	11	1.2	1542.9458734	E4	14.8	3	1542.1430111

creased in step sizes of 0.2 mA in the grating and phase zones, as specified in the previous section. We search all current combinations so as to have their output lasers generated in the ITU band. From these current combinations, we then select certain proper combination sets. We define the proper current-combination sets are those sets which will generate a smooth and settled flat channel in the ITU band and not those with generated laser output signals that exhibit the chirping effect when the currents are swept across different channels. The current combinations which generate the output lasers in the ITU-Band are shown in Table 3. For ease of illustration, we select only five typical current combinations to measure their chirping effect and switching time.

4.3. Simulation of Chirping and Switching Time

The simulation is the measure of chirping and switching time when we vary different combinations of the I_a and I_g currents to sweep across channels. As shown in Figure 5, we use nonideal pulse signals, with suitable rising and falling time constants, to generate the I_g and I_p signals. The sweeping of these currents generates DBR lasers in the different channels. The simulation for the chirping measurement is shown in Figure 6. The magnitude of chirping is defined as the unsettled situation when we switch from one channel to another channel. The simulation for the switching-time measurement is shown in Figure 7. The switching time is defined as the time duration from the time instant when the input current rises to 10% of its final value or the time instant when the input current falls to 90% of its final value until the time when it switches to another channel with its wavelength settled below 0.01 μm. We use these two definitions to measure the chirping and switching time when lasers switching between two channels. We take measurements between channels 1 and 2, channels 1 and 3, channels 1 and 4, channels 2 and 3, channels 2 and 4, and channels 3 and 4. We then analyze and discuss these measurement results.

5. SIMULATION RESULTS

The measurement results are shown in Figure 8. The x-axis is the initial channel from channel 1 to channel 4, and the final channel is also from channel 1 to channel 4. We then divide each channel into five grids, namely, A, B, C, D, and E. The lower to higher current combinations for the ITU band in Table 3 are then filled into the grids (they are also shaded by different colors). Shorter switching time channels will be shaded by lighter colors and vice versa. From Figure 8 we obtain the first conclusion that when the lasers are switched from the lower channel (high wavelength) to the higher channel (short wavelength), the switching time for different current combinations will have only minor differences. However, a big difference in the switching time occurs from different current combinations when the lasers are switched from the higher channel to the lower channel. Therefore, in selecting current combinations, the first thing we need to consider is the

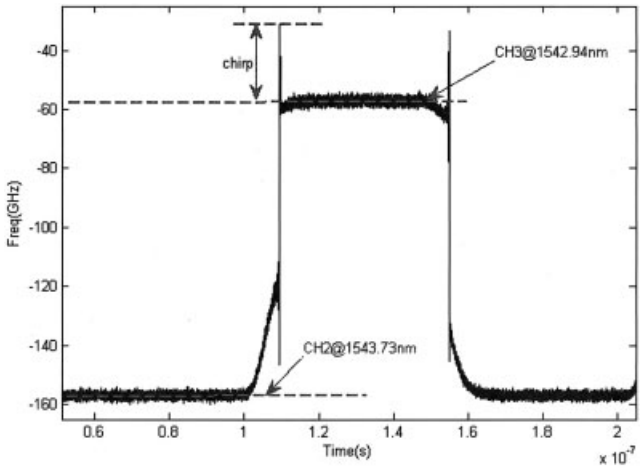

Figure 6 Method for measuring chirping

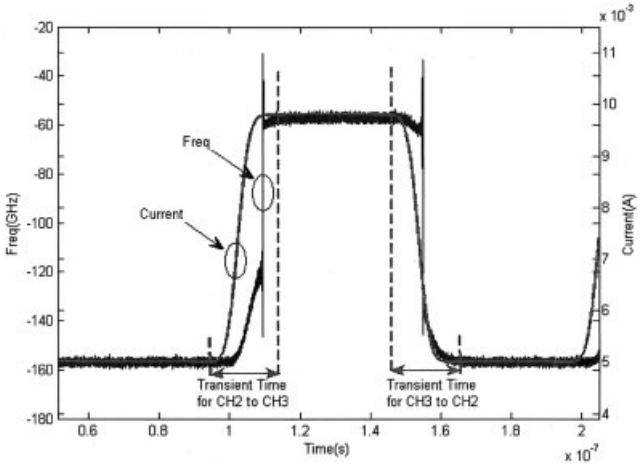

Figure 7 Method for measuring switching time

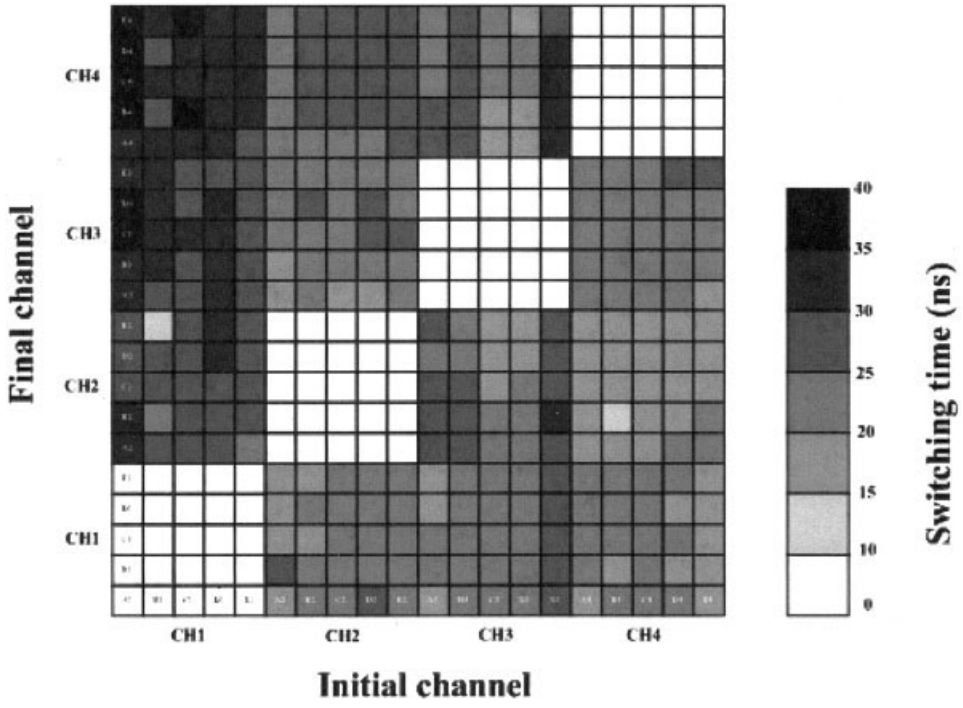

Figure 8 Switching time due to different current combinations in channels 1 through 4

situation when the lasers are switched from the higher channel (lower wavelength) to the lower channel (higher wavelength), and also we need to select the combinations which have smaller differences in the I_g and I_p currents between channels. Another simulation result, as shown in Figure 9, is the result of the chirping effect due to the I_p current differences in channels 1 and 3 when we use lasers switched from channel 1 to channel 3 as an illustrating example. We conclude that when the driving currents I_p in channels 1 and 3 have a significant difference, a big chirping effect will be generated. Its chirping effect is actually proportional to the I_p current differences in the two channels considered. Therefore, in considering the chirping effect, we select the current combinations which have lower I_p differences. From the above simulation and analysis results, we conclude that when we consider the switching-time effect, we select the switching from the shorter-wavelength channel to the longer-wavelength channel, and also select the current-combination set which has smaller differences in the I_p and I_g currents between the two channels considered. While considering the chirping effect, we need to select the current-combination set which has a smaller I_p difference between the two channels.

These are the empirical rules we derived from our simulation results and analysis. We hope they will help to provide engineers with some foundations when they select current combinations.

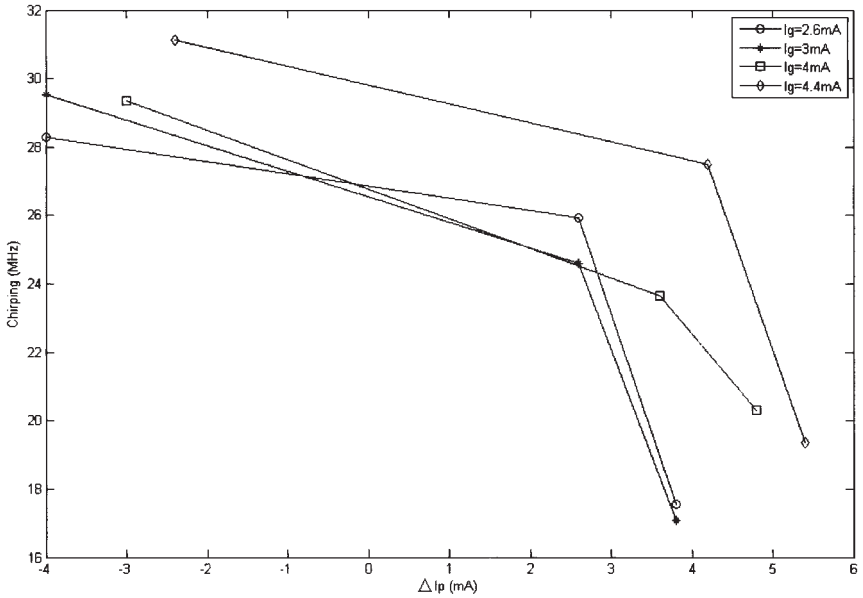

Figure 9 Chirping due to different current combinations between channels 1 and 3

6. CONCLUSION

In this paper, we have proposed empirical rules in the selection of current-combination sets for DBR lasers. DBR laser can have different driving-current combinations to generate laser sources in the ITU band. This then leads to the problem of how to select proper current-combination sets so as to expose certain proper characteristics. The characteristics we considered in this paper are the switching time and the chirping effect when a laser is switched from one channel to another channel in the ITU band. From the simulation results, we derived the empirical rules, which are based on the minimization of the switching-time and chirping effects when a laser is switched from one channel to another channel, in the selection of proper current-combination sets. These empirical rules can be exploited by engineers when they make decisions in the selection of laser sources in addition to considering those basic parameters relating to the laser's physical characteristics.

ACKNOWLEDGMENTS

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SCALABLE DISTRIBUTED-CAPACITANCE MODEL FOR SILICON ON-CHIP SPIRAL INDUCTORS

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ABSTRACT: *We present physics-based modeling for silicon on-chip spiral inductors, taking into account the coupling capacitance between metal spirals. The coupling capacitance C_p is calculated using a distributed-capacitance model based on finite-element analysis. As demonstrated for a series of inductors with the number of turns ranging from 2.5 to 6.5 fabricated in a 0.18-μm CMOS technology, the current model provides simulation results for the quality factor Q, the S-parameter, and the self-resonance frequency f_{SR} that are in good agreement with the measurements without any fitting parameters.* © 2006 Wiley Periodicals, Inc. Microwave Opt Technol Lett 48: 1423–1427, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21642

Key words: *on-chip inductor; physical mode; distributed-capacitance model*

1. INTRODUCTION

Due to the potential RFIC applications such as low-noise amplifiers and oscillators, silicon-based on-chip spiral inductors have been widely utilized in state-of-the-art CMOS foundry processes, and their characteristics have been intensively investigated [1–4]. Among various modeling methodologies for spiral inductors, the equivalent-circuit model using frequency-independent RLC elements to represent the electrical performance has a great benefit compared with electro-magnetic (EM) numerical simulation [5, 6], since a lumped equivalent-circuit model dramatically reduces computation time and supports rapid optimization in circuit simulations.

Equivalent-circuit models for the most frequently adopted single-π equivalent circuit [5, 7, 8] have been established for a long time, and the model parameters can be formulated in a simple analytical form [7]. To include various high-order parasitic effects, a ladder structure and a transformer-loop structure have been proposed within the framework of the single-π model [9, 10]. And a more complicated double-π structure has also been developed recently [11].

The capacitance in the spiral segment of an equivalent circuit includes the overlap capacitance between the spirals and the underpass metal lines C_o, and the capacitive coupling between the spirals C_p. In the conventional model [7], only the overlap capacitance has been considered. As the spacing between metal spirals becomes smaller, the contribution from the coupling capacitance becomes substantial and has to be considered. C_p has been analyzed recently using a distributed capacitance model (DCM) [12]. However, this model suffers from a major deficiency, that is, it is not scalable. The derived formulations exhibit nonphysical results with a decreasing C_p as the number of turns of the metal spirals (and hence the total area of capacitors) increases for a series of inductors with a similar geometry.

The purpose of this paper is to develop a fully scalable model for the coupling capacitance between metal spirals C_p, as well as

A Novel Architecture for High-Speed Viterbi Decoder

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Abstract

In this paper we present a high- speed and low- complexity Viterbi decoder architecture. The Add-Compare-Select Unit (ACSU) is an indispensable unit in the Viterbi decoder. The processing speed in the conventional architecture of Viterbi decoder is limited due to the large amounts of calculations executed in the ACSU. Meanwhile in the hardware implementation of the ACSU it also encounters a great extent of wires connecting complexities. We propose to create the Cyclic-Shift Register Unit (CSRU) and the Pseudo-Correlator Unit (PCU) in the ACSU so that ultimately it not only reduces its hardware connecting complexities in the unit but also improves the overall processing speed in the Viterbi decoder. We make analysis and comparison in the hardware complexities and processing speed between our proposed and conventional architectures in the Viterbi decoder.

Key words: Viterbi Decoder, Add-Compare-Select Unit (ACSU), Cyclic-Shift Register Unit (CSRU), Pseudo-Correlator Unit (PCU).

1. Introduction

It exists many decoding algorithms in the decoding of Convolutional codes, the Viterbi decoding algorithm is currently the most popularly used algorithm which was proposed by Viterbi in 1967 [1]. It uses the Maximum Likelihood Decoding (MLD) concept. Omura [2] proved later that the Viterbi decoding algorithm is equivalently trying to find the minimum path in the weighted graph problems, i.e. it is the solution for the dynamic programming problems. Finally Forney [3, 4] identified that Viterbi decoding algorithm is the Maximum Likelihood Decoding algorithm for Convolutional codes. Forney [5] is also the first person to demonstrate that the Viterbi decoding algorithm possess the maximum prediction capability from its received signals when signals are transmitted through a finite bandwidth channel and suffering any inter-symbol interference.

Although Viterbi algorithm is the best decoding algorithm for Convolutional code its complexity increases in exponential form versus the increases in the decoding Trellis states as 2^M, where M is the memory order [6]. When M becomes large it becomes difficult in the hardware realization and also generates the complexity in the circuits wiring so that many computation- reducing proposals have been proposed to reduce the complexity in the execution of Viterbi algorithm. It usually consists of four

modules in the Viterbi decoder, as shown in Figure 1. The computation complexity usually happens in the ACSU block therefore a lot of literatures were proposed to conquer the problem existing in the execution of this block [7-10]. In other literatures [11-15] the authors have other considerations in the realization of Viterbi decoders. In [11] Kamuf et al. presented the architecture of simplifying the BM (Branch Metric) and the ACSU block. It has the result in 1/2 Convolutonal code of saving an adder in each ACSU however it still has the wires connecting complexities problem. Gang et al. [12] proposed an adaptive Viterbi decoding architecture to simplify the operation of the ‘Compare’ unit in the ACSU. They also proposed an LUT (Look-Up Table) concept to reduce the hardware complexities. The wiring complexities in the revised architecture have not been reduced. Zhu and Benaissa [13] discussed multi-level pipeline architecture for the ACSU to lift the Viterbi decoding speed to a higher level and this architecture can also be realized in FPGA. The structure of ACSU is different from our proposed architecture and it is a different design philosophy for the ACSU. Traber [14] proposed the idea of path-metric buffering to realize ACSU so that its occupied area is reduced, the wiring reliability is improved and also the power consumption is optimized. However their processing speed is slowed. In [15] Inkyu and Sonntag presented the concept of doubling the number of Trellis states and then transformed the traditional serial operations of ACSU into parallel structure to

improve the processing speed. Their main consideration is how to increase the decoder processing speed even resulting the increase of the complexities of ACS. In order to reduce the computation time and to simplify the wiring complexity in the ACSU block we create the Cyclic-Shift Register Unit (CSRU) and the Pseudo-Correlator Unit (PCU) to replace the Branch Metric Generation Unit (BMU), the ACSU and the FBU. It results in not only reducing the hardware complexities but also increasing the decoder processing speed. This paper is organized in the following sections. In Section 2 we will illustrate the complexity problem by considering a simple (2, 1, 2) Convolutional code and then investigate the hardware design of Viterbi decoder. In Section 3 we discuss the wiring complexity in Viterbi decoder. It then in Section 4 explains in detail the structures of CSRU and PCU and the design of the decoding algorithm for this (2,1,2) Convolutional code. In Section 5 we will analyze and compare the timing sequences between our proposed and the conventional architectures. Then we draw conclusions in Section 6.

2. Example of (2,1,2) Convolutional Code with Radix-2 and Radix-4 Structure

In this section, we present a simple example to demonstrate the Convolutional code and the design principle of Viterbi decoding algorithm. As shown in Figure 2 is a

(2,1,2) Convolutional code where the designation (n, k, M) denotes the number of output bits n, the number of input bits k and the number of shift registers M used in the Convolutional code. This (2, 1, 2) Convolutional code is generated by the generator polynomial $G(x) = (x^2 + x + 1, x^2 + 1)$. By observing Figure 2, in this (2,1,2) Convolutional code, it consists of a two-stage shift register and three mod-2 adders that convert a single input bit into two output bits.

From the Convolutional code as shown in Figure 2 it generates an associated state diagram. The state diagram depicts the relation between an input data and an output data. The transfer relation from one input state to an output state depends on the current input data and its current state. Besides by using state diagram to represent Convolutional code it can also be represented by using Trellis diagram. In the Trellis diagram the positions of all input and output states are fixed. We can demonstrate the Trellis structure by observing the (2, 1, 2) Convolutional code when time evolves. In this Trellis diagram, with (0, 0) as the initial state, it rearranges by showing all its possible states in the vertical axis as input information changes and time proceeds with time shown in the horizontal axis.

After discussing the Trellis diagram we will briefly explain the Viterbi decoding algorithm. As shown in Figure 1 it consists of four basic building blocks in Viterbi

decoder namely, the Branch Metric Generation Unit (BMU), the Add-Compare-Select Unit (ACSU), the FeedBack Unit (FBU) and the Survivor Memory Management Unit (SMU). When the BMU receives new information it calculates its associated branch distance. The ACSU constantly updates the minimum branch distance of each state after executing the addition, comparison and selection operations. The FBU is used to store every updated shortest path and to detect possible overflow. The SMU records all decision results generated from the ACSU and it also feedbacks remaining survival path to find the possible decoding bit. After introducing the Convolutional code and the Viterbi decoder we will be in the following to analyze the connection complexity of this (2, 1, 2) Convolutional code. We will then propose a new architecture to minimize its connection complexity as much as possible.

3. Complexity Analysis for Viterbi decoder

As shown in Figure 1 the ACSU and FBU recursively use the same Trellis structure to attain the task of reducing the hardware size but however increase the hardware complexity. We will first analyze in this section the hardware complexity when we use ACSU and FBU blocks in the conventional Viterbi decoder. The connection diagram between ACSU and FBU is shown in Figure 3 in which the previous state and its branch distance are input to the ACSU and the ACSU, after operations, will output the Hamming distance and the survival path of the next state

S_n(t+1). The information of the survival path will be transmitted to SMU and the Hamming distance of state S_n (t+1) will feedback to the input port of ACSU, S_n(t). From these described operations in SMU, FBU and ACSU we can estimate the hardware complexity of this Trellis structure. As shown in Figure 3 the state information of S_0 (t+1) is feedback to S_0 (t) and S_1 (t) and the information of S_2 (t+1) will also be feedback to S_0 (t) and S_1 (t) we then have the wiring cross connection problem. It concludes that in this (2, 1,2) Convolutional encoder it counts to generate six cross connection points. We define the number of cross connection points as the "connection factor". We will use this number as a comparison measure to examine the complexities of various Viterbi decoders. The connection factor for the configuration of Figure 3 is:

$$Connection \quad Factor = \frac{(1+(2^M-1))2^M}{2} n_M \qquad (1)$$

where M is the number of shift registers used in the Convolutional encoder, n_M is the number of bits used to express each state. From this relation it shows that the connection factor grows increasingly with the number of shift registers M in an exponential form, 2^{2M-1}. The relation between n_M and the number of shift registers M is shown in Figure 4. It concludes that the hardware complexity becomes worse when M increases and becomes large.

4. High- Speed and Low Complexity Design for Viterbi Decoder

In conventional architecture of Viterbi decoder as discussed in the previous section it uses the feedback connections between ACSU and FBU to achieve the goal of hardware reuse. Although it attains the task of saving hardware counts it increases the system complexities. And also it slows down the decoder processing spend due to this system complexity increase. In order to solve this processing speed slowing effect we propose a new architecture that it replaces the design of ACSU and FBU in the conventional decoder. It first uses Radix- 4 instead of usually implemented Radix -2 to realize the one-stage Trellis diagram in the (2, 1, 2) Convolutional code in the conventional architecture. By using this translation it simplifies some of the hardware complexity. In part (a)-(d) of Figure 5 it shows the resulting branch codes for the four states (S_0, S_1, S_2, S_3) in Radix-4 architecture when time evolves from t to t + 1 in the Trellis diagram.

In the following we will illustrate the new architecture of each functional block:

(1) Pseudo-Correlator Unit (PCU)

PCU has the structure as shown in Figure 6. It replaces BMU and ACSU blocks in the conventional architecture to reduce not only its complexities but also to improve decoder processing speed. It consists of six parts in the PCU block:

a. Serial-In-Parallel-Out (SIPO) shift register:

In Radix-4 architecture it needs to process four bits simultaneously we therefore convert the data received at Viterbi decoder from serial format to parallel format and then temporarily store these four output bits into the shift register.

b. Branch Code Generator (BCG):

When the branch codes corresponding to the four states (S_0, S_1, S_2, S_3), as shown in Figure 5, are stored in the lookup table they are also been forwarded to XOR and Adder for them to calculate their corresponding Hamming distances. At any time instant the total number of data received and the amount of registers used in each of the four branch codes has the following relation:

$$Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-4$$

, $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-3$

, $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-2$ and $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-1$, respectively.

where Rem is the Survival data, L is the total received data bits and M is the number of registers used in the Convolutional code.

After proper rearrangements of the branch codes generated at any time instant it

has the results shown in Table 1.

c. Feedback- Compare Unit (FBCU):

After comparing the calculated results at two consecutive times in the Adder block it outputs the one with smaller distance. And after finishing the comparisons of all four states it will output both the Previously Minimum Hamming Distance State (PMHS) and the Survival Data. The PMHS outputs the branch code with its associated minimum Hamming distance while the Survival Data records the survival path and outputs this information to Survival Path Memory (SMU).

The basic operating principle of FBCU is illustrated in the following.

For demonstration we take the state PCSU0, shown in Figure 8, as a starting point then this unit is executed in the following three steps:

Step 1: The result of adding the Hamming distance of Branch 0000 ($Branch_{0000}$) with S_0 is forwarded to FBCU. It has only one branch at the present time. We store the calculated result in MHS-Reg and record the branch number 00. It has four wires connecting to this state. We then give each branch wire a symbol such as 00, 01, 10 and 11 to identify the Survival path associated with each wire.

Step 2: Compare the result of adding the Hamming distance of Branch 1011 and S_1 with the content in MHS-Reg which contains the result calculated from Step 1. After the comparison it stores in MHS-Reg the smaller Hamming distance and also it records its associated Branch number. It repeats the above-stated operations until it finishes the adding of the Hamming distances of Branch 0111 (Branch $_{0111}$) and S_3. It outputs the minimum Hamming distance, PMHS (Previous Minimum Hamming Distance State), from last four comparisons and stores to SMU the Survival Data of the state which has the minimum Hamming distance.

Step 3: Feedback the PMHS information through CSRU to the state PCSU0.It then repeats the execution of Steps 1 and 2.

d. Exclusive-OR (XOR):

It calculates the Hamming distance between the data output from SIPO shift register and the branch code generated from branch code generator. It uses XOR unit for this Hamming distance calculation, i.e. its output is one when both data are the same otherwise it generates a zero output.

e. Adder:

The Adder does the summing operation by adding the Hamming distance

calculated in XOR and the Hamming distance generated from previous stage. The minimum Hamming distance generated in the previous stage, CMHS (Current Minimum Hamming Distance State), will be forwarded to CSRU and after it has been feedback from CSRU this CMHS will be added with the resulting Hamming distance of the current state. The summation result will be transmitted to FBCU for further operation.

f. Minimum Hamming Distance State Register (MHS-Reg):

The calculated result in FBCU is temporarily stored in this register and it then feedbacks this data with the next coming data to FBCU. Due to this register can compare only two branch codes at any time we need to store the previously obtained comparison result for FBCU when it executes the comparing task in the next stage.

(2) Cyclic-Shift Register Unit (CSRU):

The CSRU has the structure as shown in Figure 7. It utilizes a 4-bit shift register to form a loop-like structure. After reading the final PMHS information, which is calculated from PCU, it starts the shift and rotation actions it then outputs the shifted result, which to be used in next state execution, to PCU. In Figure 8 it shows the operation of each state branch code after combining CPU and CRSU. Since it

calculates only one branch code at any time instant it needs four time instants to complete the calculations of four branch codes. It is because of the use of CSRU it reduces tremendously the system connection complexities.

5. Timing Analysis for the Tradition and Novel Viterbi Decoders

We analyze and compare in two different cases the latency time in the Viterbi decoding for the conventional and our proposed architectures. One case is the total execution time in which we calculate in average the system overall latency time and the other is the maximum possible execution speed in the hardware realization of the architecture. In the following table is a list of delay times of basic building devices used in BMU, ACSU and FBU. These delays are extracted from the specifications of UMS 0.18um fabrication process.

Device	Delay Time
OR	0.139ns
AND	0.107ns
NOT	0.023ns
HA	0.140ns
FA	0.732ns
4-bit Comparator	0.166ns
2→1 Mux	0.167ns
XOR	0.199ns
D-latch	0.328ns

First we will analyze the overall system latency time in the conventional architecture. We use the (2, 1, 2) Viterbi decoder as an illustrating example. The

conventional architecture has the structure shown in Figure 9. The input data is transmitted through BMU, ACSU and FBU. This is the most critical path which limits the processing speed in Viterbi decoding and has the latency time $T_{Tradition\_latency}$. It is good enough only to analyze this path. In BMU its only function is to calculate the Hamming distance between the received data and the branch code. It consists of a Half Adder (HA) and a Not Gate. We denote T_{BMU} as the time required for the data to pass through this longest path. In ACSU it consists of three units, namely, the adding unit, the comparing unit and the selecting unit. When it receives the Hamming distance information transmitted from BMU it will be added with the Hamming distance calculated from previous stage. It then outputs the resulting smaller distance from comparing these two distances between two relevant states. It needs a full adder to execute the adding operation. We include in our latency time for the adding operation the time required in the comparing and selecting operations. The processing time for this unit is denoted as T_{ACSU}. It then passes through the FBU to repeatedly processing the Trellis diagrams. The total time spent in the shift registers is T_{FBU}. We then have the system overall latency time for the conventional architecture:

$$T_{Tradition\_latency} = T_{BMU} + T_{ACSU} + T_{FBU}$$

$$T_{BMU} = T_{HA} + T_{NOT} = 0.140\text{ns} + 0.023\text{ns} = 0.163\text{ns}$$

$$T_{ACSU} = T_{4bitAdder} + T_{4-bitcomparator} + T_{2-1Mux}$$

= 4×0.732ns+0.166ns+0.167ns

=3.261ns

$T_{FBU} = T_{D-latch}$ =0.328ns

$T_{Tradition\_latence}$ =0.163ns+3.261ns+0.328ns

=3.752ns

Then we analyze the possible maximum possible speed in the hardware realization of the conventional architecture. In the conventional architecture the element which limits or restricts the operation speed is the feedback path in the ACSU and the FBU. It has the longest latency time of T_{ACSU} . Consequently we have:

$$T_{Tradition\_\min} = T_{ACSU} = 3.261\text{ns}$$

In processing speed analysis for our proposed architecture it can be analyzed from Figure 10. When data is received it will first pass through a serial-to-parallel converter it will have a parallel output whenever 4 bits are input. This parallel output will be forwarded with the code generated from the Branch Code Generator to the XOR block to generate the branch code. The time required to complete this operation and the time required to add with the Hamming distance generated from the previous stage is defined as T_{XOR} + $T_{4\text{-}bit\ Adder}$. After this Hamming distance additions for all four states they are sent to the comparator to make decision to determine which state has the minimum distance. The time required to make this comparison is denoted as T_{FBCU}. The time required to feedback the data from CSRU is T_{CSRU}. The average system

latency time in the Viterbi decoding in our proposed architecture then has the following calculations:

$$T_{Novel\_latence} = \frac{Iteration \quad number}{Radix \quad n}(T_{XOR} + T_{4bitAdder} + T_{FBCU} + T_{CSRU})$$

$$T_{FBCU} = T_{4bitcomparator} + T_{2-1Mux} = 0.166\text{ns}+0.167\text{ns}=0.333\text{ns}$$

$$T_{CSRU} = T_{D-latch} = 0.328\text{ns}$$

$$T_{Novel\_latencye} = \frac{4}{4}(0.199\text{ns}+4*0.732\text{ns}+0.333\text{ns}+0.328\text{ns})=3.788\text{ns}$$

The possible maximum speed in our novel architecture is limited by $T_{Novel\_\min}$. Every time when it processes the CSRU block it also needs to complete the operations of the path, XOR→4bit Adder→FBCU→MHS-Reg. The longest delay block in this path is the 4-bit Adder therefore the delay $T_{Novel\_\min}$ is determined by the 4- bit Adder or the maximum speed in our proposed architecture is limited by the 4-bit Adder as:

$$T_{Novel\_\min} = T_{4bitAdder} = 2.928\text{ns}$$

From above analysis we come to the conclusion that the overall system latency delay in our proposed architecture is almost the same as the conventional one but its maximum processing speed will be faster than the conventional one with latency time of 2.928 ns in our proposed architecture versus the 3.261 ns in the conventional architecture.

6. Conclusion

In order to reduce the complexity in ACSU architecture and also to improve the processing speed in the conventional architecture of Viterbi decoding we proposed in this paper to use PCU to replace BMU and ACSU to provide higher decoding speed and to use CSRU to reduce the complexities in ACSU and FBU realizations. We derived timing equations to find the average system latency delay time and the maximum possible system processing time in the conventional and our proposed novel architectures. It concluded that in average they have almost the same system latency time in both architectures however the maximum speed available in our proposed architecture is almost 11%, 2.928 ns vs. 3.261 ns, higher than the conventional one.

Acknowledgement

The authors would like to thank the National Science Council, R.O.C. for the financial support under Contract NSC 94-2745-E-032-001-URD, NSC 94-2745-E-032-004–URD, NSC 94- 2213-E-032-005, and Tamkang University for the funding support from the University-Department joint research project.

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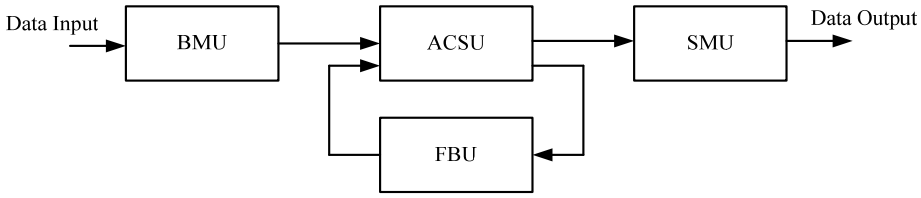

Figure 1. Fundamental blocks for Viterbi decoder

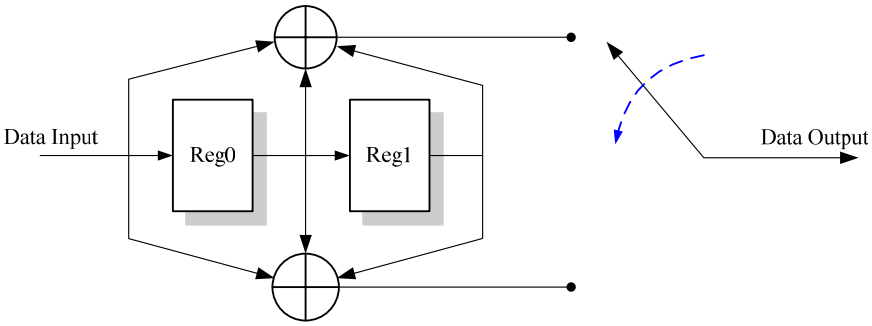

Figure 2. Structure of (2,1,2) Convolutional encoder

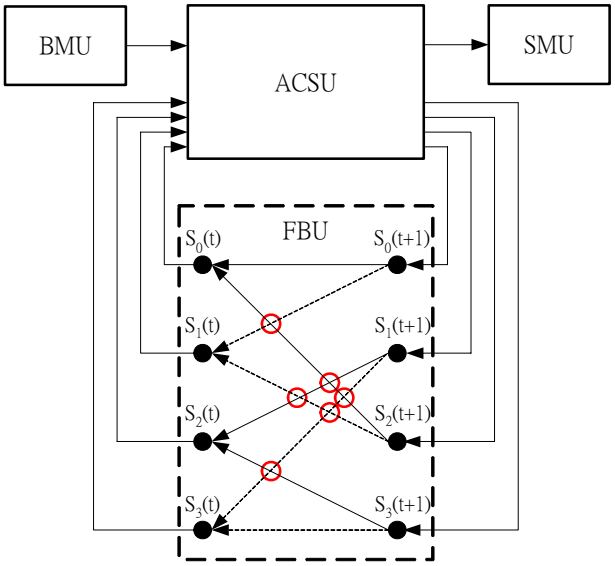

Figure 3.Wirings of ACSU and FBU (The complexity spot is shown in the dotted box)

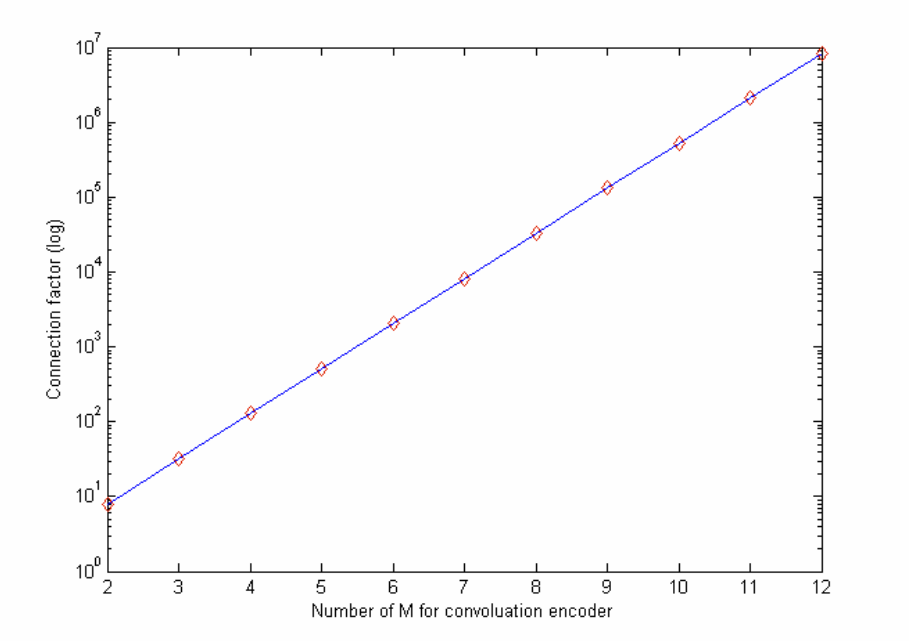

Figure 4. Relation between shift registers used M and the wiring complexities

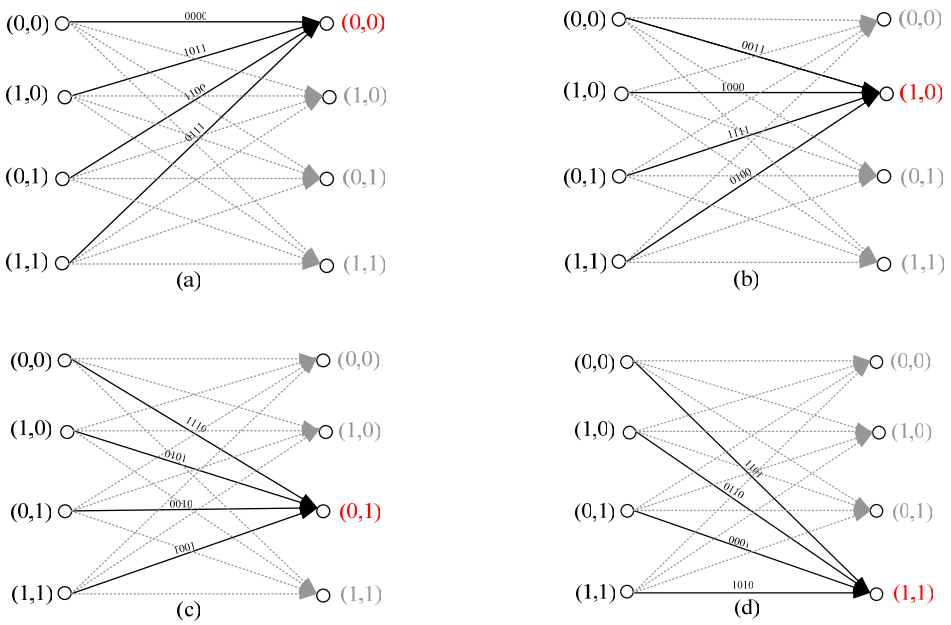

Figure 5. Trellis diagram in Radix-4 operation

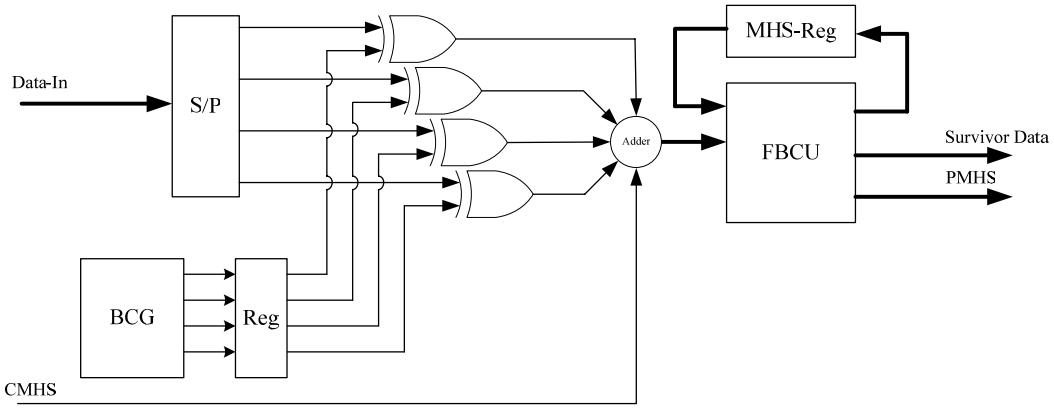

Figure. 6. Pseudo-Correlator Unit (PCU)

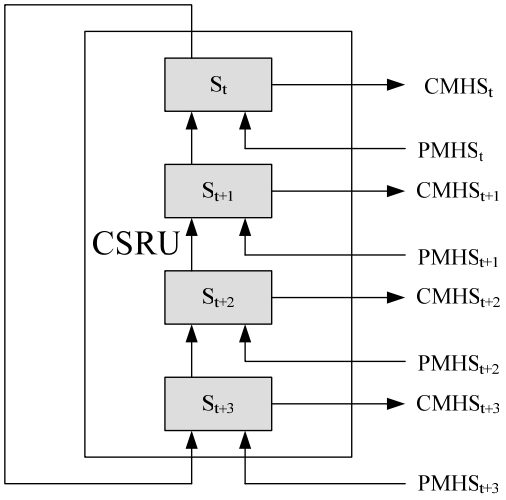

Figure 7. Cyclic-Shift Register Unit (CSRU)

(a)

(b)

(c)

(d)

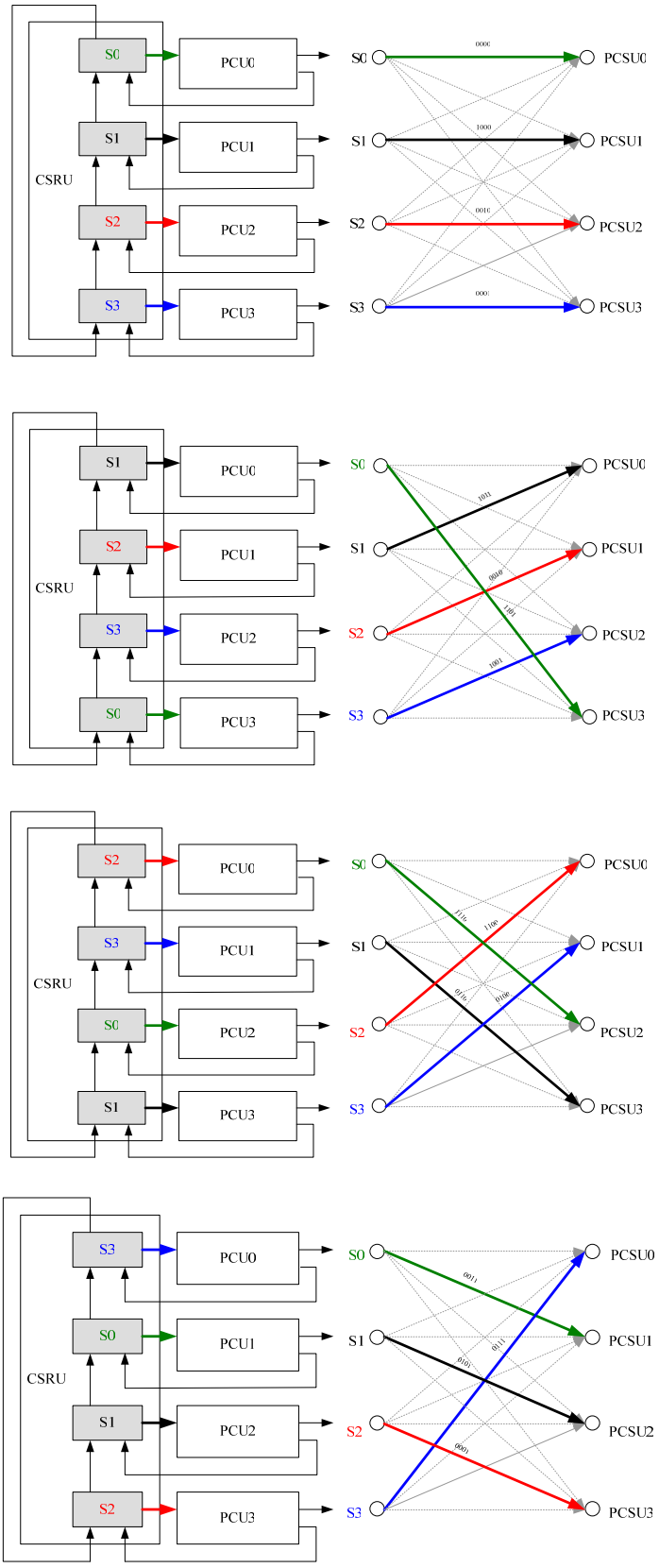

Figure 8. (a)-(d) Examples of executions between states in CSRU and PCU at a time instant

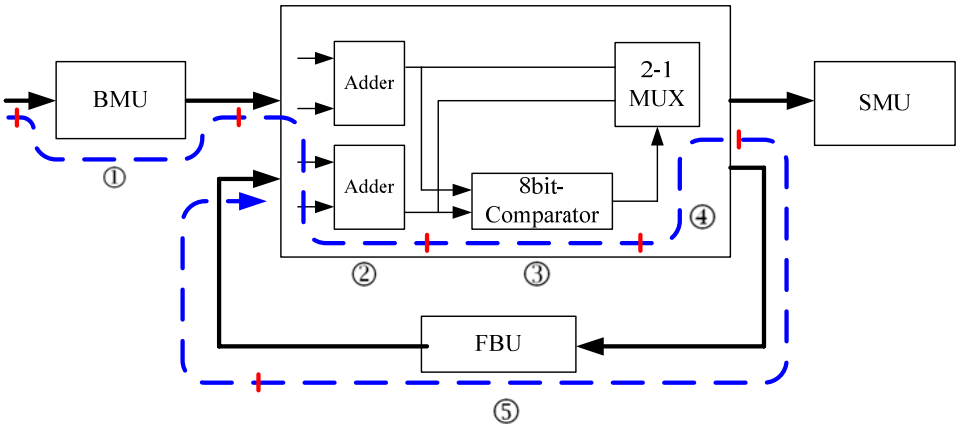

Figure 9. Timing analysis for conventional Viterbi decoder

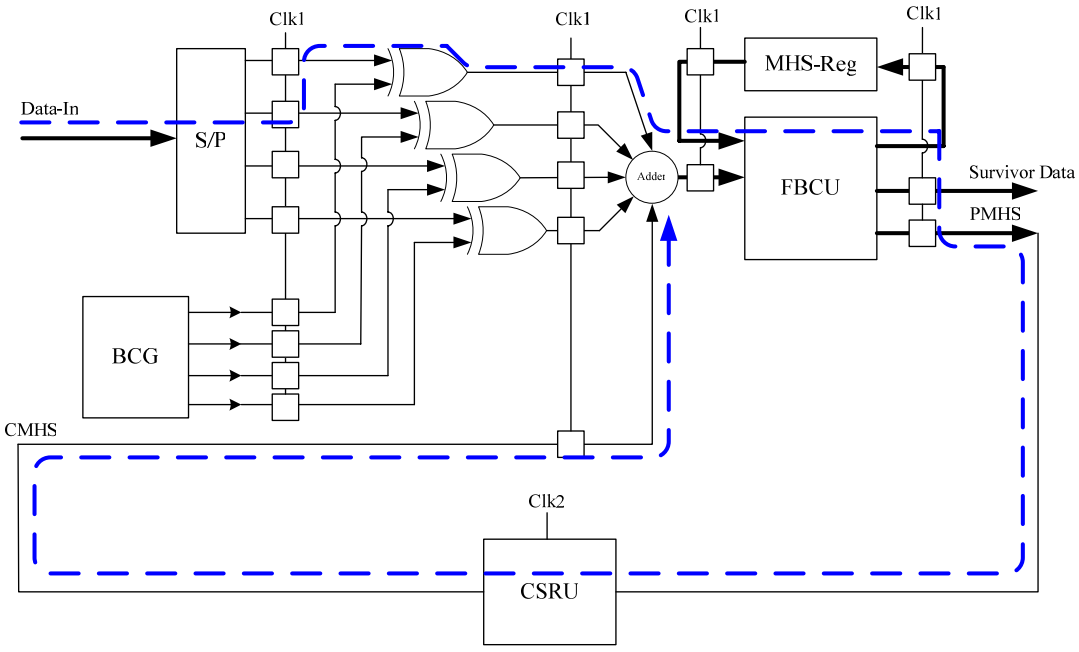

Figure 10. Timing analysis for high speed Viterbi decoder

Table 1. Branch generator for PCU at a time instant

Time Unit	Branch code	
t = 0, 4, …, $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-4$	PCU 0	0000
	PCU 1	0011
	PCU 2	1110
	PCU 3	1101
t = 1, 5, …, $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-3$	PCU 0	1011
	PCU 1	1000
	PCU 2	0101
	PCU 3	0110
t = 2, 6, …, $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-2$	PCU 0	1100
	PCU 1	1111
	PCU 2	0010
	PCU 3	0001
t = 3, 7, …, $Rem[\frac{2(L+M)}{4}]+\frac{2(L+M)}{4}-1$	PCU 0	0111
	PCU 1	0100
	PCU 2	1001
	PCU 3	1010

The Design And Simulation of Optical Synchronous Code Division Multiplexing System with Balanced Encoder

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Abstract

In this paper we propose to use the balanced encoder instead of the conventional on-off keying technique in the design of synchronous optical CDMA system. Due to the use of the balanced encoder in the system architecture the user interference suffered is estimated from every frame instead of the conventional estimation by using every bit, the resulting estimated interference is kept constant for one frame. In addition, due to the simplification in the receiver architecture the receiver processing spend is not restricted by its associated electrical signal processing speed so that it not only effectively speeds the whole system processing spend it also greatly simplifies the system complexity. The VPItransmissionMaker simulation package is used to set up a eight users optical code division multiplexing system to verify the effectiveness of the system designed.

Keywords: optical code-division multiple access, on-off keying, multi-user interference.

1. Introduction

The code-division multiple accessing (CDMA) was originally investigated in radio frequency (RF) communication systems. In fiber optic communication systems, the bandwidth of the optic fiber is much wider than that of the electronic data. To exploit the huge bandwidth of the optic fiber, the optical code-division multiple access (OCDMA) system, which has been proposed and widely discussed since mid-1980s [1][2], is a viable alternative for the broadband communication networks [3][4]. In non-coherent OCDMA systems, which are much simpler than the coherent systems, the nonnegative nature of optical signal has restricted the spreading codes to be pseudo-orthogonal unipolar sequences [1][2][5][6]. Under this restriction some asynchronous OCDMA networks are designed where the users have independent clocks, and others are designed for synchronous networks. Although the synchronous OCDMA networks need more complex structure to reach their synchronization [7], they have much larger spreading code size, which is defined as the number of available codes, and they can also accommodate more users simultaneously [8][9].

Since the cross-correlations of the unipolar codes are non-negative, the multi-user interference (MUI) increases with the increasing number of simultaneous users. Hence, most of the OCDMA systems use the on-off-keying (OOK) scheme in the transmitters to reduce the MUI; that is, only the bit 1 in binary bit is encoded by a signature code sequence. In the receiver, there have also been many schemes proposed and analyzed to reduce the error probability resulting from the MUI. For examples, optical hard-limiters were utilized in [10][11], error control codes were applied in [12][13], receivers with interference estimators were proposed in [9][11], etc. In this paper we will design a receiver to enable it to eliminate the interference effect from its estimated interference value by utilizing the balancing encoding to generate a constant interference level in a frame so that it can effectively reduce the error probability

2. Analysis of Design Principle

The OCDMA system considered in this paper is a star network with a central star coupler. Every node in the system is assumed synchronized to a common clock, which can be broadcasted through a beacon from a control node. The packets in the system are transmitted through synchronous frames, and also the number of simultaneous users in a frame is constant.

2.1. Balanced Encoder

The basic encoding principle of the balanced encoder is shown in Figure 1. Every information bit, no matter it is 0 or 1, will output a spreading code and every code is spreading into many chips, then we perform the encoding by using different prime code, as illustrated in Table 1, is an example to generate 12 sets of spreading codes for prime number 3 or p = 3. Due to the use of balanced codes we then divide these 12

sets of spreading codes into eight groups of users and split them into four groups. It has two mutually interference –free users in each group, they use the same set of spreading code when the data bit is 0. As shown in Figure 2 is the architecture of the balanced encoder, it generates a code with different prime in the lower branch when the data bit b = 1 and it generates in the upper branch another set of code from the same group code with different prime when the data bit b = 0. Consequently no matter the bit transmitted is 0 or 1 it will generate an output code with constant weight and consequently from this characteristic it will also generate a constant interference to other channels.

2.2. Decoder

The decoder has the basic structure as shown in Figure 3. The received optical signal passes through different optical delay lines to perform the correlating decoding step for each user. It then passes through the APD photo detector to perform the optic-electrical conversion. In order to estimate the mutual interference among users it inserts many 0 bits before inserting the information bit in the frame design.

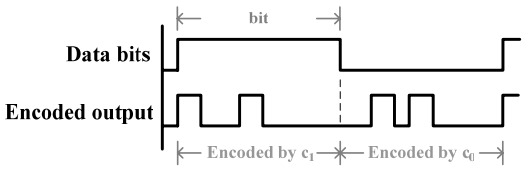


Fig. 1: Principle of balanced encoder

Table 1: Spreading codes combinations for different prime, p = 3

Group	Code sequences
0	100 100 100
	010 010 010
	001 001 001
1	100 010 001
	010 001 100
	001 100 010
2	100 001 010
	010 100 001
	001 010 100
3	111 000 000
	000 111 000
	000 000 111

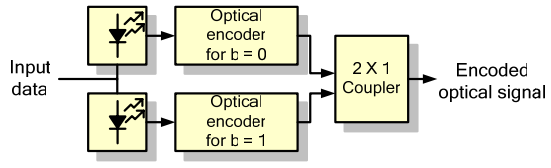


Fig. 2: Functional block diagram using balanced codes as the spreading codes

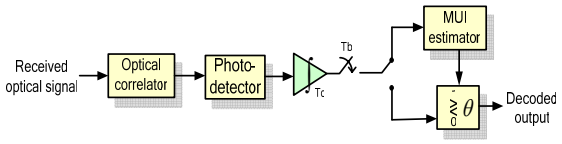


Fig. 3: Transceiver implemented with balanced encoder

Consequently in the receiver design we will switch to Multi-user interference (MUI) system to perform the estimation process before beginning the data transmission in every time frame and then to estimate how many users are in the system, through the entry in Table 2, and then determine the signal threshold level so as to make it as the basis in the signal detection.

2.3. Frame Format

In OCDMA system, we should define each user's frame format to reach the multiple accessing mechanism. For example as shown in Figure 4 is the frame formats for four users when they transmit frames at different time instants. Simply, each frame consists of three fields. In the first field is the preamble field it consists of all zero bits to estimate the MUI amount and also by using these zero bits to attain the synchronization task. The second filed is the data field. In this field the first bit is 1 to declare the beginning of the data field. The last field is the pad field. In order to maintain constant MUI in the system we need to pad 0 bits till all users finish their data transmission.

Table 2: Estimated users' mutual interferences

Number of user	Number of interference	APD output current (A)	Threshold current (A)
1 or 2	0	0.46×10^{-4}	0.23×10^{-4}
3	1	0.83×10^{-4}	0.645×10^{-4}
4	2	1.3×10^{-4}	1.065×10^{-4}
5	3	1.88×10^{-4}	1.59×10^{-4}
6	4	2.56×10^{-4}	2.22×10^{-4}
7	5	3.34×10^{-4}	2.95×10^{-4}
8	6	4.23×10^{-4}	3.785×10^{-4}

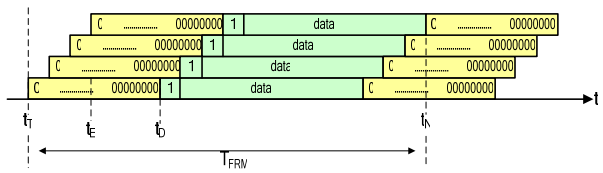


Fig. 4: Frame format

3. System Architecture

In this paper we use two sets of software packages to verify and simulate the design of this OCDMA transceiver. The first part is the optical signal processing part. We use VPItransmissionMaker software to set up our transmitter and receiver parts. It then stores the data received. It then uses the Matlab software to read the output file and do the decoding operation to extract the original data.

3.1. Transmitter Architecture

The simplified transmitter architecture is shown in Figure 5. We use 0.5A current to drive the single mode laser, the laser has wavelength of 1552.52 nm. It then uses amplitude modulation to process the external modulation in which the electrical signal is modulated by the input data signal in the transmission and then these signals are separated to use as the spreading codes. These signals then pass through the optical delay lines to insuring proper delays for using as the spreading codes for all users. And finally these signals are multiplexed and transmitted.

3.2. Receiver Architecture

The simplified receiver architecture is shown in Figure 6. The main function of the receiver terminal is to simulate the optical correlation function, as depicted and shown in Figure 3 of the system architecture. Through the concept of optical correlation we can use proper optical delay lines to separate users with different demodulation formats from the received signal. It then operates the optic-electrical signal conversion. The APD photo detector used in this paper has thermal noise 10^{-13} ($\frac{A}{\sqrt{Hz}}$).

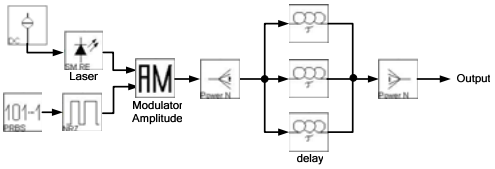


Fig. 5: Basic architecture of OCDMA transceiver system

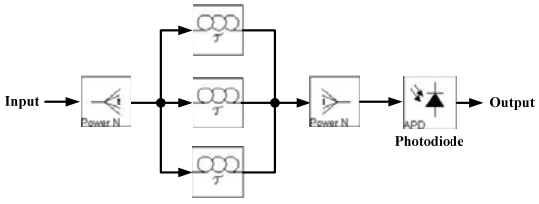


Fig. 6: Basic architecture of OCDMA receiver sub-system

3.3. OCDMA Transceiver Architecture

As shown in Figure 7 is the simplified complete transceiver system by combining eight sets of users transceivers. Every transceiver in the system is modularized. At different time instant each user enters into the transceiver system, performs the optical modulation, and then it passes through the optical coupler and all signal are combined and transmitted. In the receiver, in order to perform the estimation of the MUI interferences among users, it performs separate demodulation methods for 0 and 1 data bits. Through Matlab program we will find the average interference from the 0 data bits and then use this average interference to set the current threshold level for the detection of data bit 1. Through this detection scheme the original data sequence are consequently determined.

4. Simulation results

In the simulation test we will use and let eight users to transmit their data at different time instants and then pick one of the user's outputs to discuss its performance. In Figure 8(a)(b) it shows the estimation of the MUI interferences among users. In the front part the interferences are monotonically increasing since users are continuously sending their data and it then shows a part with ten equal interferences time segments. From these ten signals we can find their average value and determine that it has eight users are in transmitting data. Then using the entry data in Table 2 we can find the proper current threshold for the receiver in its detection operation. In this particular case we can set the current threshold at 0.3785 mA and extract the data samples at every time instants. It shows that the detected data are exactly the same as the transmitted data.

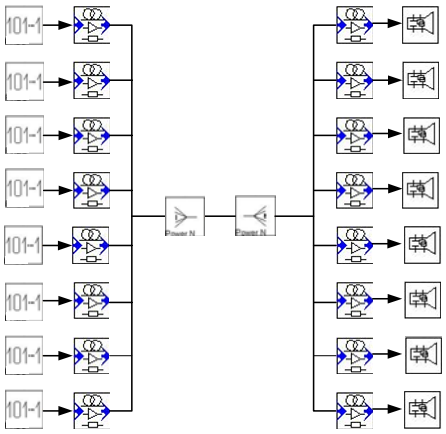
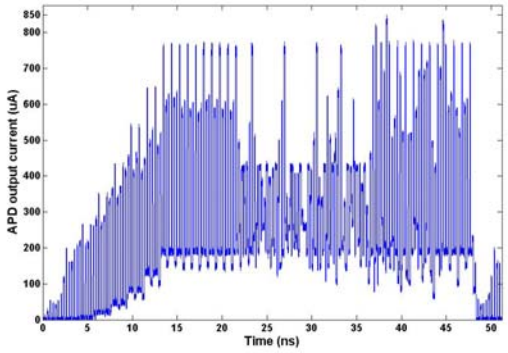
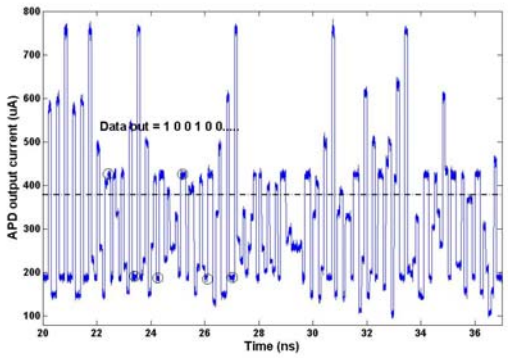


Fig. 7: Basic architecture of OCDMA transmitter sub-system



(a)



(b)

Fig. 8 Receiving data at the OCDMA receiving terminal

5. Conclusions

In this paper we used simulations to verify the design of synchronous optical CDMA system by utilizing the balanced encoding. We also set up the frame format that meet the system requirement. The system error probability is reduced due to the use of the balanced codes to estimate the MUI interferences among users. The estimated mutual interference is kept constant in each time frame. By this design it greatly reduce the complexity in the conventional receiver design so to avoid the restriction in the system design that is limited by the electrical signal processing speed. In the future consideration we will try to realize our proposed designed system into the hardware implementation.

6. Acknowledgements

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DBR 雷射波長之驅動電流組合最佳化分析

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摘要 ---在本論文中，我們利用可調式雷射(DBR Laser)三個電極的電流調整出對應 ITU 波長的通道輸出，由於每一個 ITU 波長的輸出擁有許多不同的電流組合，所以此篇論文著重在分析當切換至不同 ITU 波長的通道時，哪一組電流組合能夠提供最好的效能(低的啁啾與短的切換時間)。

關鍵詞: *可調式雷射二極體 (Tunable laser)、分散式布拉格反射雷射二極體 DBR (Distributed Bragg Reflector laser)、啁啾(Chirp)*

前言

隨著資訊的蓬勃發展以及網路應用的急速成長，對於資料傳輸及訊號所需要的頻寬要求也越來越高。因為傳輸介質光纖具有大頻寬與低損耗等優點，因此能提供更高的傳輸容量與更彈性的服務。利用光纖作為傳輸網路介質將成為必要的選擇，同時為了能增加光纖傳送資料的效率及通道容量，分波多工(Wavelength-division multiplexing, WDM)[1][2]等技術也相繼而生。由於在 DWDM 系統中，有超過一百個以上波長間隔小於 50GHz 的通道在傳輸，所以我們需要精確且穩定的可調式雷射[3]來提供備用所需的波長或應用於波長路由網路中。

DBR 雷射中最常見的即是利用三個電極控制輸出的波長，我們可以分別在不同的電極上，調整加入電流的組合來產生我們所需要的波長[4-10]，但由於同一 ITU (International Telecommunication Union)波長可以由好幾組的電流組合產生，所以要如何從多組電流中挑選出一個最適合的電流，將是很值得討論的問題。

DBR 雷射之動作原理

在此篇論文中，我們選用常見的三個電極之 DBR 雷射(如圖 1 所示)，並使其工作在 1550nm 的波長；三個電極分別為主動區、光柵區及相位區。此雷射架構簡單、操作容易，且製程較其他種類的 DBR 雷射簡單，缺點是可調動的波長範圍有限，適合在區域網路(LAN)中使用。

三個電極的 DBR 雷射，利用主動區、光柵區及相位區分別供應的偏壓電流 Ia、Ig、Ip 來調整輸出的波長，Ia 提供主動區調整雷射輸出波長功率的大小，Ig 提供光柵區大範圍調整雷射輸出的波長，Ip 則提供相位區微調雷射輸出的波長。因此，搭配不同的 Ia、Ig 及 Ip 電流，我們可以調整出我們所需要且符合 ITU 標準波長的通道。

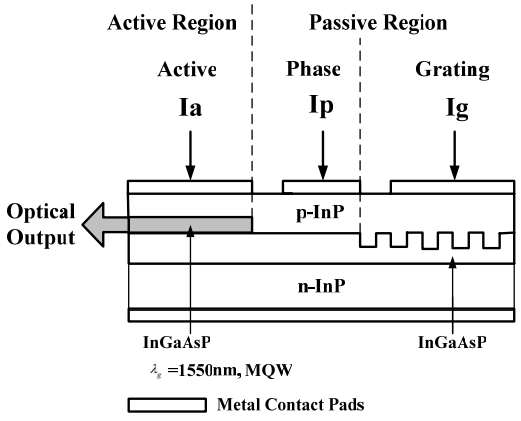

圖 1. DBR 雷射基本架構

模擬程序

此小節中，我們要找出相對應於 ITU 波長之 Ig 與 Ip 的所有電流組合以及切換電流組合使輸出在兩個不同的 ITU 波長間切換時，觀察所造成的啁啾與轉換時間，進而使用這些數據來分析啁啾的大小以及切換的時間。接下來我們針對掃描模擬、啁啾與切換時間做詳細的介紹。

(a). 模擬參數設定

我們在模擬前先設定 DBR 雷射內部之相關物理參數，並設定雷射三個電極所需要之電流範圍，其中主動區所提供的電流 Ia 固定為 40mA，光柵區所提供的電流 Ig 由 2mA 變化至 15mA，每次變化 0.2mA，相位區所提供的電流 Ip 由 0mA 變化至 15mA，每次變化 0.2mA，所設定的 ITU 波長在 1544.53nm、1543.73nm、1542.94nm 以及 1542.14nm 四個通道。我們將針對上述所設定的範圍內掃描出啁啾與切換時間的數值。

(b). 掃描模擬(找出對應至 ITU 波長之所有電流組合)

上述之掃描參數設定後，我們將主動區之電流設定為固定的 40mA，且設定光柵區及相位區的電流於範圍內，使用掃描之電流遞增方式(當 Ig 電流每增加 0.2mA，Ip 的電流由 0mA 變化至 15mA，每次變化 0.2mA)，找出符合 ITU 波長的電流組合，掃描出之波形如圖 2。挑選出符合 ITU 波長的電流組合後，為了便於分析只選擇五組符合 ITU 波長的電流組合，用來做啁啾與切換時間的量測。

(c). 啁啾與切換時間的模擬(模擬 ITU 波長所有電流組合所產生的啁啾與切換時間)

我們利用不同的 Ig 與 Ip 之電流組合，在相異的通道間轉換，模擬量測其啁啾與切換時間；我們使用一個非理想的方波(具有 rising time 和 falling time)來產生 Ig 與 Ip 跳動之輸入訊號，並利用此訊號使得 DBR 雷射在不同的兩個 ITU 波長間切換。圖 3 為啁啾的量測方式，我們定義啁啾的大小為：前一個通道跳至另一通道時所造成不穩定之現象。圖 4 為切換時間的量測方法，我們定義切換時間的大小為：當輸入電流的上升時間輸出變化 10%(或下降時間變化 90%)時開始，計算到切換至另一個波長穩定在 $\Delta\lambda \leqq 0.01$nm 時為止，藉由此方式來量測啁啾與暫態時間。我們將通道 1←→通道 2、通道 1←→通道 3、通道 1←→通道 4、通道 2←→通道 3、通道 2←→通道 4 及通道 3←→通道 4 各種組合都測出來，並利用量測出來的數值做分析與探討。

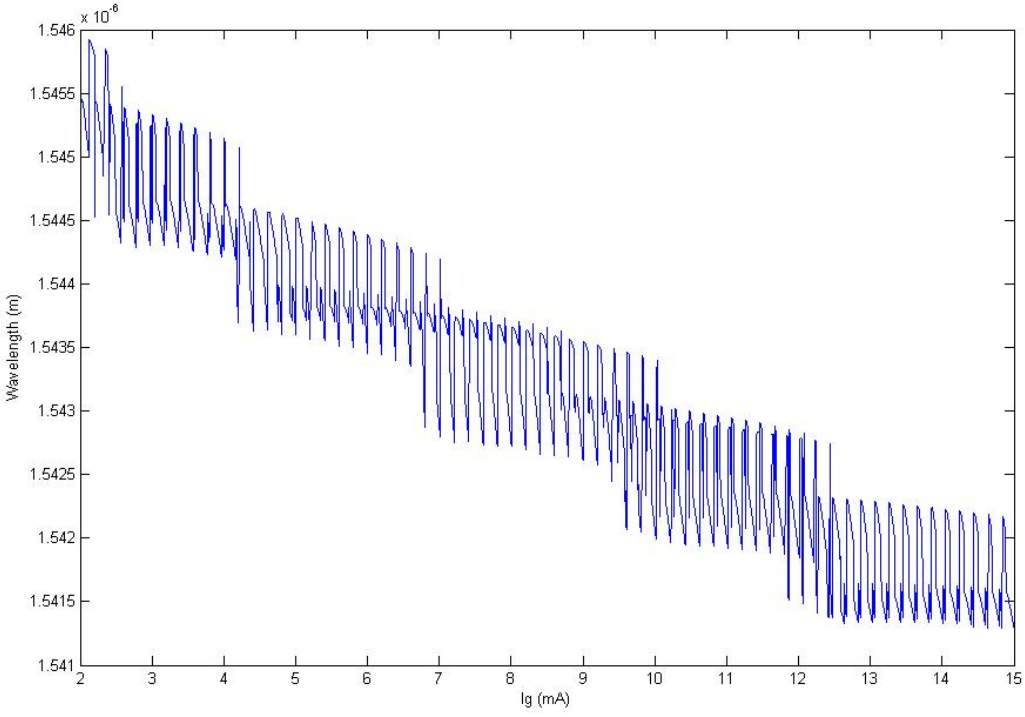

圖 2. Ia 固定為 40mA、Ig 電流每增加 0.2mA，Ip 的電流由 0mA 變化至 15mA，每次變化 0.2mA，所觀察到之雷射輸出波形

模擬結果與分析

我們將所量測到的結果整理後得知，當低通道跳到高通道(長波長跳到短波長)時，不同組的電流所造成的切換時間只會有些微的差距，而高通道跳到低通道(短波長跳到長波長)時，不同組的電流所造成的切換時間就會有很大的差距，所以當我們要挑選電流時，首要的考量是考慮高通道跳到低通道(短波長跳到長波長)時的情況，並且挑選兩組通道間 Ig 與 Ip 差值較小的組合。另一個模擬結果則是以通道 1 跳到通道 3 來說明；當通道 1 與通道 3 之 Ip 電流差值很大時，所造成的啁啾也會很大，其啁啾與 Ip 差值的大小成正比，所以當考量啁啾大小時，我們在許多的電流組合中會挑選 Ip 差值較小的組合。

由以上的分析可以得知，若要選擇切換時間較小的組合，則挑選在短波長跳到長波長下且兩個通道間差距較小的 Ip 與 Ig 來決定，若要選擇啁啾較小時，是挑選由兩個通道之 Ip 差距較小的組合決定，因為每顆雷射的特性均不同，所以我們只列出經驗法則來協助使用者在挑選電流組合時能更有依據。

結論

在本篇論文中，我們提供了一個挑選 DBR 電流組合的經驗法則。由於在 DBR 雷射中，我們可藉由不同之驅動電流組合使得雷射工作在相同的 ITU 波長上，所以在這篇論文中，利用不同電流組合在切換時間的時間長短與啁啾的大小上整理出經驗法則，供使用者在使用 DBR 雷射時能有更多的依據以便挑選最好的電流組合。

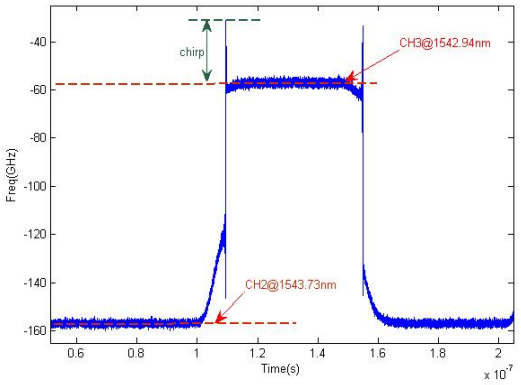

圖 3.啁啾之量測方法

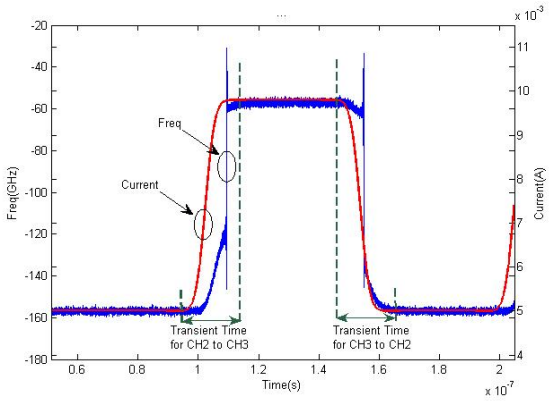

圖 4. 切換時間之量測方法

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