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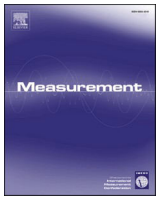

Processing techniques for metrological improvement of low-cost smart meter hardware solution for IEC 61000-4-7 Class I harmonics measurements

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ABSTRACT

The work investigates the feasibility of harmonic analysis implementation on smart meter microcontroller devices, according to IEC 61000-4-30 Class A and IEC 61000-4-7 Class I requirements. The final aim was to evaluate to what extent Class I harmonic analysis can be integrated into existing low-cost hardware platforms for smart metering, which normally have limited hardware features, especially concerning the ADC and the possibility of varying the sampling frequency with high resolution, according to the power system signal frequency. An extended experimental characterization is carried out on a case study device, aimed at analyzing its performances in terms of both measurement accuracy and computational burden. To increase metrological ADC behavior and decrease computational costs, sampling strategies and optimized interpolation algorithm have been implemented and tested verifying the feasibility of harmonic analysis implementation on smart meter microcontroller devices, according to IEC 61000-4-30 Class A and IEC 61000-4-7 Class I requirements.

1. Introduction

With the growing harmonic pollution in power systems and the need to maintain suitable power quality (PQ) levels, distribution network operators and electricity users, producers and prosumers have become more and more interested in embedding the measurement of harmonic distortion in electricity metering systems [1–5], so to obtain the possibility of a capillary monitoring of the network, without increasing unreasonably the costs for instrumentation. Furthermore, the development of smart grids and the integration renewable energy sources and even electric vehicles have fostered the development of distributed measurement technologies and new smart metering solutions for PQ measurements. The attention has been focused not only on measurement devices accuracy but also on their synchronization and communication capabilities, as well as on the possibility of using low-cost hardware equipment (instead of expensive instrumentation typically used for PQ analysis) [6–14].

As regards the metrics implementation, several studies have been carried in recent years to investigate different solutions for PQ monitoring and harmonics assessment, with the aim to develop suitable solutions, capable to cope with standards requirements for instrumentation for power supply systems and equipment connected thereto [15–20]. More specifically, main reference standards are IEC 61000-4-30 [21] and IEC 61000-4-7 [22], which deal with power quality measurement methods and harmonics and interharmonics measurements and instrumentation, respectively. These standards define two classes of instruments, with different metrological features, namely class A and class S in IEC 61000-4-30, corresponding to class I and class II in IEC 61000-4-7, respectively. Class A/I instruments are conceived for contractual applications, billing purposes, verification of

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compliance with standards, etc.; class S/II instruments are meant to be used for statistical applications, instead. In this framework, the solutions proposed in literature deal with the measurement of several typical PQ parameters, mainly including total harmonic distortion for harmonic pollution assessment; in few cases harmonic analysis is implemented, with class S/II features, unless more expensive equipment, rather than low-cost platforms, are used.

In more detail solutions based on microprocessor boards or Field Programmable Gate Array (FPGA) architectures have been proposed in literature for large scale monitoring of PQ, since they have been recognized to allow the implementation of powerful measurement algorithms on low-cost hardware with reconfigurable firmware. For example, in [23] a FPGA-based measurement instrument for harmonic and interharmonic monitoring in compliance with [21], despite the absence of a sampling frequency synchronization system. In [24] PQ measurements are implemented on a low-cost power quality measurement system based on a Texas Instruments DSP processor, with a particular focus on spectral analysis by means of FFT or DFT. In [25] a low-cost smart Web sensor has been designed and implemented to acquire, process and transmit data over an 802.3 network. In [26] a low-cost power quality parameters monitor is proposed, based on PIC16F877A, as an alternative to power quality analyzers; it includes the measurement of some parameters, like RMS voltage and current, powers (active, reactive, apparent) and power factor, etc.; as regards harmonics, only THD measurements are included in the meter. In [27] the use of a harmonic analysis algorithm is validated on a microcontroller board, to perform measurements on non-stationary signals, by means of CZT algorithm; it allows improving the spectral resolution in a limited bandwidth of interest of few hundreds of Hertz, even with short observation windows; such algorithm would be not feasible for the whole Class I frequency range (i.e. up to 50th harmonic), because it would entail an high computational cost, as the one of the DFT algorithm. A more expensive solution was presented in [28], where compressive sampling was proposed and tested on a 16 bit data acquisition system built with a DAQ NI 9215 and a voltage transducer LEM CV 1000, for measuring the amplitude of harmonic and interharmonic disturbances. In such papers aggregated parameters for harmonic distortion are mostly addressed, such as THD, while the issues related to the measurement of single harmonic components and the compliance with Class A/I requirements is not fully covered and investigated; in some cases specific harmonic ranges of harmonics up to 25th are considered, while the Class I requirements cover the range up to 50th order. Moreover, while accuracy requirements are somewhat analyzed for proposed low-cost solutions, few reference is made to the computational costs and the required measurement time. As regards this, a more challenging topic for developing low-cost power quality meters is the integration of accurate PQ metrics in commercial low-cost platforms for obtaining the compliance with the class A/I requirements, in terms of both measurement accuracy and time. Existing power quality analyzers available on the market allow fulfilling both such requirements, but they are expensive so their use is not feasible for large scale adoption and capillary power quality and harmonics monitoring purposes. The investigation of the feasibility of Class A/I efficient and accurate harmonics measurement with low-cost devices is the goal of this paper, instead.

As regards harmonics measurements, according to [21] and [22], the observation window Tw must be 10 or 12 cycles of the fundamental frequency for 50 Hz or 60 Hz power systems, respectively, i.e. 200 ms, with a maximum synchronization error of 0.03 % of Tw. For class A/I instruments, measurements must be performed without gaps between two consecutive windows, (for class S/II gaps are permitted instead). To synchronize the sampling, a preliminary estimation of the power frequency is required, to set the sampling parameters, i.e. sampling frequency f_s and number of acquired samples N. By increasing f_s it is possible to collect more samples and, by consequence, to have a more precise reconstruction of the sampled signal. On the other hand, for low-cost devices, the processing of a high number of samples can be not feasible within the specified time for a gapless operation, depending on the device memory and computational capabilities. Moreover, some low-cost platforms use a fixed sampling frequency or they provide just the possibility to choose the sampling frequency among some predefined values derived from the internal reference clock.

For harmonic analysis, in [22] DFT algorithm is considered, without any windowing, except for Hanning weighting, which is allowed only in case of synchronization loss. To efficiently perform the analysis, reference is made to the use of FFT, which allows reducing the computational cost of the spectral analysis algorithm [29–31]. However this requires processing a number of samples equal to a power of two, posing further constraints on sampling frequency. To avoid this issue, when the suitable sampling frequency is not available, a possible solution is to implement a time-domain interpolation to obtain the desired number of points for FFT calculation, whatever the sampling parameters are. In previous works [32,33], the authors investigated the issues related to the spectral analysis implementation on a low-cost device, showing the feasibility of using time-domain interpolation to improve the spectral analysis accuracy and efficiency. It was shown that the use of a proper interpolation algorithm allows reconstructing the sampled signal with suitable approximation, depending on the sampling frequency used for collecting the samples data and the order of the interpolation function. However while class S/II accuracy requirements can be feasible without the need of high sampling frequencies, class A/I features can be challenging.

Moreover, as mentioned above, current measurement instruments for PQ analysis available on market are not usable in distributed measurement systems as they have high costs. On the other hand, existing smart meters are already part of a well-defined distributed measurement system for medium and low voltage (MV and LV) networks and their exploitation for PQ measurements, other than those already implemented for billing purposes, can be foreseen. However, existing low-cost hardware platforms for smart metering can have limited hardware features, especially concerning limited computational capability and ADC features, in terms of effective number of bits and the possibility of varying the sampling frequency with high resolution, according to the power system signal frequency. These scientific and technological issues have led the authors to seek solutions based on smart meter microcontroller devices, in order to investigate the feasibility of harmonic analysis implementation, according to IEC 61000-4-30 Class A and IEC 61000-4-7 Class I requirements. In this way, thanks to the diffusion of smart meters, it would be possible to perform distributed PQ harmonic analysis without excessively increasing costs, integrating the proposed novel approach into the existing smart meters. Thus, in this paper is an extended experimental characterization is presented, which was carried out on a case study device, able to implement different sampling and processing techniques, as proposed in this paper. The study was aimed at analyzing the device performances in terms of both measurement accuracy and computational burden. Different solutions were implemented and tested, concerning both signal processing algorithms and sampling strategies for data acquisition, aimed at improving the metrological characteristics of low-cost hardware. As regards the metrics implementation, a time-domain interpolation algorithm is proposed, based on Farrow filter. It is a valid alternative to Lagrange polynomial interpolation, thanks to its lower computational cost; moreover it allows optimizing the computational burden for harmonic analysis, whatever the values of sampling frequency and number of samples are. The proposed algorithm has been implemented on the case study microcontroller board and several experimental tests have been carried out by using the on-board ADC for signal acquisition. Different sampling strategies have been tested, to identify a suitable solution for both data acquisition and processing, capable to comply with Standards requirements.

The paper is structured as follows. In section II the issues related to the efficient and high accuracy spectral analysis implementation on low-cost devices are discussed. In section III the basics of the proposed

Farrow interpolation algorithm are recalled. In Section IV the preliminary validation of the algorithm is presented, which was carried out on a PC based IDE environment; the spectral analysis results are compared with those obtained with Lagrange polynomial interpolation and the IEC 61000-4-7 Class I accuracy requirements. In Section V the implementation on the microcontroller device is presented and the results of the experimental characterization are discussed, showing the feasibility of the proposed solution.

2. Feasibility analysis of efficient and high-accuracy spectral analysis on low-cost devices

As mentioned in the introduction, Standards IEC 61000-4-30 and IEC 61000-4-7 provide strict requirements in terms of both sampling synchronization and observation window. Specifically, the observation window *Tw* must be 10/12 cycles for 50/60 Hz power system frequency, respectively, i.e. 200 ms, with a maximum synchronization error of 0.03 % of Tw, i.e. 60 μs. For Class A/I instruments, harmonics measurements must be performed without gaps between two consecutive windows. This means that the spectral analysis (and subsequent grouping and smoothing operations [22]) must be completed within 200 ms, to avoid missing samples from an observation window to the subsequent one. Gaps are allowed for class S/II instruments, instead (with a minimum of three measurements within the aggregation time of 3 s, i.e. 150/180 cycles, and at least one measurement every second, i.e. 50/60 cycles). For harmonic analysis, the reference algorithm is the discrete Fourier transform (DFT) or its faster version, i.e. the Fast Fourier transform (FFT).

To efficiently execute the FFT algorithm, a number of samples equal to a power of two should be acquired. This poses strict constraints in terms of sampling frequency for data acquisition in a real case implementation, when the requirements on observation window synchronization are considered. For example, to synchronously sample a 50 Hz signal in the observation window of 200 ms and to acquire 2048 points, a sampling rate of 10,240 samples/s would be required. In real devices, especially commercial low-cost ones, sampling frequency is fixed or it can be chosen among discrete values derived from the microcontroller reference clock; thus the optimal sampling frequency value could be not available. Moreover, in real cases signal frequency is not exactly known and it may slightly differ from the rated value, thus an uncertainty occurs on the proper number of samples to be acquired to have synchronous sampling for a given sampling frequency. To remove such constraints, DFT algorithm could be used, which does not pose any limitation about sampling frequency and the number of samples to be acquired in the desired observation window. The only limitation is related to the minimum sampling frequency for fulfilling the requirement on the maximum synchronization error. Specifically, considering the aforesaid limit of 60 μs for $Tw = 200$ ms observation window and a rounding error of 0.5 samples between Tw and its nearest integer multiple of the sampling time, the minimum sampling frequency to have a synchronization error not higher than 0.03 % is 8.334 kHz (i.e. the sampling time should be not higher than 120 μs). With this sampling frequency, 1667 samples would be acquired for the DFT analysis, in the observation window $Tw = 200$ ms. The higher the sampling frequency, the higher the number of samples for the same observation window. However, due to its high computational cost [$O(N^2)$ instead of $O(NlogN)$ for the efficient FFT], the DFT execution time could not allow achieving Class A requirements, in terms of processing time vs. gapless signal acquisition and analysis, unless very high-performance systems are used.

In more detail, a comparison of computational cost (number of operations) required by DFT and FFT algorithms is reported in Table 1 and Fig. 1, for different number of samples (powers of two). The required processing times for DFT analysis are reported in Table 2.; they were experimentally measured by implementing the DFT algorithm on the device used in this paper as case study (NUCLEO STM32F767ZI by STMicroelectronics, see section IV) and by measuring the processing time with a digital oscilloscope Tektronix MSO54 5-BW-350 (as made for the tests presented in section V). In detail, the measurements were carried out by acquiring a signal at an output pin of the NUCLEO board; the pin signal was changed from low to high level at the beginning of the DFT processing task and it was changed back to low level at the end of the task. The test reported in Fig. 2 refers to the processing of 1667 samples (acquired over the observation window of 200 ms). The required processing time for DFT is much higher than 200 ms, thus the algorithm is not feasible for the implementation on the case study device. On the other hand, FFT calculation requires a much lower number of operations, thus the required time for processing is expected to be significantly lower than the one needed for DFT. Experimental measurements of processing times in the case of FFT calculation are presented and discussed in section V.

Table 1
Computational costs of spectral analysis algorithms (DFT vs. FFT).

Number of points N	Computational cost for DFT (N*N)	Computational cost for FFT (N*log(N))
4	16	2
8	64	7
16	256	19
32	1024	48
64	4096	116
128	16,384	270
256	65,536	617
512	262,144	1387
1024	1,048,576	3083
2048	4,194,304	6782
4096	16,777,216	14,796

It should be noted that, when the sampling frequency cannot be adapted to the signal frequency (to directly acquire a number of samples equal to a power of two, for the efficient FFT calculation), techniques like zero padding (ZP) or time-domain interpolation (TDI) can be used to obtain the desired number of points for the FFT analysis. In this case, the computational cost of such techniques must be added to the total processing burden.

As regards ZP, it consists in adding zeros to the sequence of acquired samples, in order to reach the desired numbers of points for the efficient FFT calculation. Obviously, this operation does not add a significant processing time and it is faster than any TDI algorithm. However, in the viewpoint of a Class A/I instrument, ZP has important drawbacks.

The first ZP limitation is that it always leads to an increase of the number of points for FFT analysis. For example, for the sampling frequencies tested in the following, i.e. 16 kHz, 24 kHz and 32 kHz, 3200, 4800 and 6400 samples are acquired in the observation window of 200 ms, respectively. By adding zeros, the nearest upper number of points for FFT can be reached, i.e. 4096 for the 16 kHz case, 8192 for the others. On the contrary, by using a TDI, also 2048 points could be obtained, which can be more feasible in terms of computational cost. The second and most critical aspect of ZP technique is that it leads to a loss of synchronization of zero-padded signal with respect to the required observation window length. In fact, zeros are added to the acquired a number of samples corresponding to a synchronous observation window *Tw*. In this way the nearest upper power-of-two number of points is obtained; however these points do not correspond to the desired integer number of cycles anymore. This causes scallop loss errors on harmonics measurement, which may not allow fulfilling the accuracy requirements for Class A/I instruments. Generally speaking, filtering or windowing could be used to reduce such errors. However, this would be in contrast with the IEC 61000-4-7 requirements; in fact, according to the Standard, the window width must be synchronized and no windowing should be used (Hanning weighting is allowed in the case of loss of synchronization; however the loss of synchronization must be indicated and the harmonics measurements must be "flagged" and not be used for the purpose of determining compliance with standard limits). On the

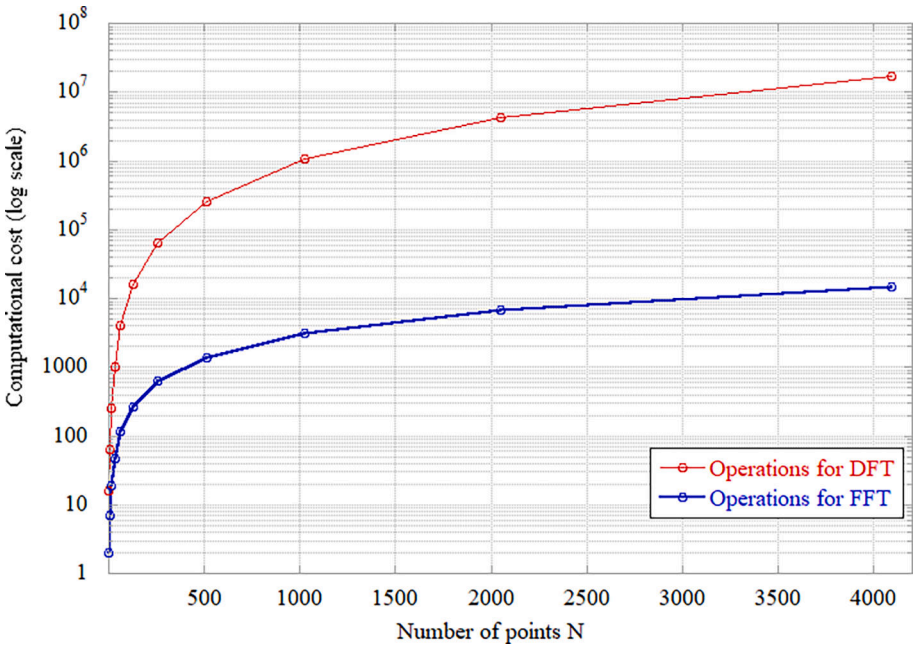


Fig. 1. Computational cost of spectral analysis (number of operations, DFT vs. FFT).

Table 2
DFT Processing time.

Number of points N	Measured DFT processing time (s)
128	0,12
256	0,49
512	1,96
1024	7,85
1667	20,8
2048	31,4

contrary, by using a TDI algorithm, the observation window length does not change, thus the synchronous sampling is maintained (according to IEC 61000-4-7 requirement) and no scallop loss errors are introduced.

To evaluate the impact of errors due to ZP, tests have been carried with different sampling frequencies, according to the tests of section IV, i.e. 16 kHz, 24 kHz and 32 kHz and 3200, 4800 and 6400 samples, respectively. A test signal with harmonics up to 50th was used as reference (i.e. the same signal used for the tests of section IV and V). The errors on harmonics measurement with the ZP technique were evaluated and compared with those obtained with the TDI described in section III. Some results are reported in Fig. 3; as can be seen, by using ZP scallop loss are clearly visible and the errors on harmonics measurements are significantly higher than those obtained with the TDI algorithm.

Thus, according to the aforesaid analysis, in this paper a proper TDI algorithm has been developed and implemented on the case study device, as described in the following section. As regards the additional computational burden introduced by TDI, in section V it will be shown that the overall processing time (interpolation + FFT) remains much lower than the one required for DFT and in certain conditions it can be feasible for gapless analysis, even considering the additional time needed for the interpolation. The analysis of both accuracy and processing times for FFT analysis (with TDI) are presented and discussed in section V.

3. Time-domain interpolation algorithm. The Farrow filter

As previously mentioned, a possible solution is to apply a TDI interpolation algorithm and to perform an efficient FFT calculation, whatever f_s is [15,29]. In this case attention should be paid to the interpolation algorithm, as the use of a low-order function could be not suitable for correctly reconstructing the signal. In fact, interpolation algorithms act by approximating the part of signal between consecutive samples using a given function (linear, polynomial, sinusoidal, ecc). The signal reconstruction accuracy and computational burden depend on the sampling frequency f_s and the type and order of chosen interpolation algorithm. In detail, the accuracy increases with the order of the approximation function and the number of samples N in the given observation window Tw. The increase of sampling frequency also determines an increase of memory requirements to store the acquired data. As regards the computational burden, the number of operations needed to implement the algorithm increases with both the order of the interpolation function and the number of samples required for spectral analysis; this causes also an increase of the time employed to execute the operations [30,34]. In this scenario, a suitable tradeoff should be reached between the available number of samples for the interpolation and the use of a lower order function for the reconstruction of the signal. In detail, for a given number of samples, the reconstruction accuracy increases with the interpolation function order; for example, Fig. 4 shows an example of comparison between two interpolation functions with the same number of interpolated points. On the other hand, for a given interpolation function, the reconstruction accuracy increases with the number of acquired samples. Thus the use of low order interpolation function (even linear) can be feasible only with a significant number of points in the given time window [32]. In the perspective of a Class I gapless harmonic analysis, the interpolation algorithm execution time must be added to the time needed for the spectral analysis and any other operation to be performed within the 200 ms observation window; this may lead to a high computational cost of the whole processing algorithm (including both the interpolation and the spectral analysis), which can cause problems in meeting the standard requirements.

In this work the study has been focused on the use of interpolation algorithm based on the Farrow filter, typically used as Fractional-delay digital filter (FD-DF) [35,36]. FD-DFs can be implemented either as finite-duration impulse response (FIR) or infinite-duration impulse response (IIR). FIR-based FD-DFs are commonly implemented using the Farrow structure, which enables both variable signal delay and high-speed online tuning [37,38]. In general, FD-DFs are used to adjust the

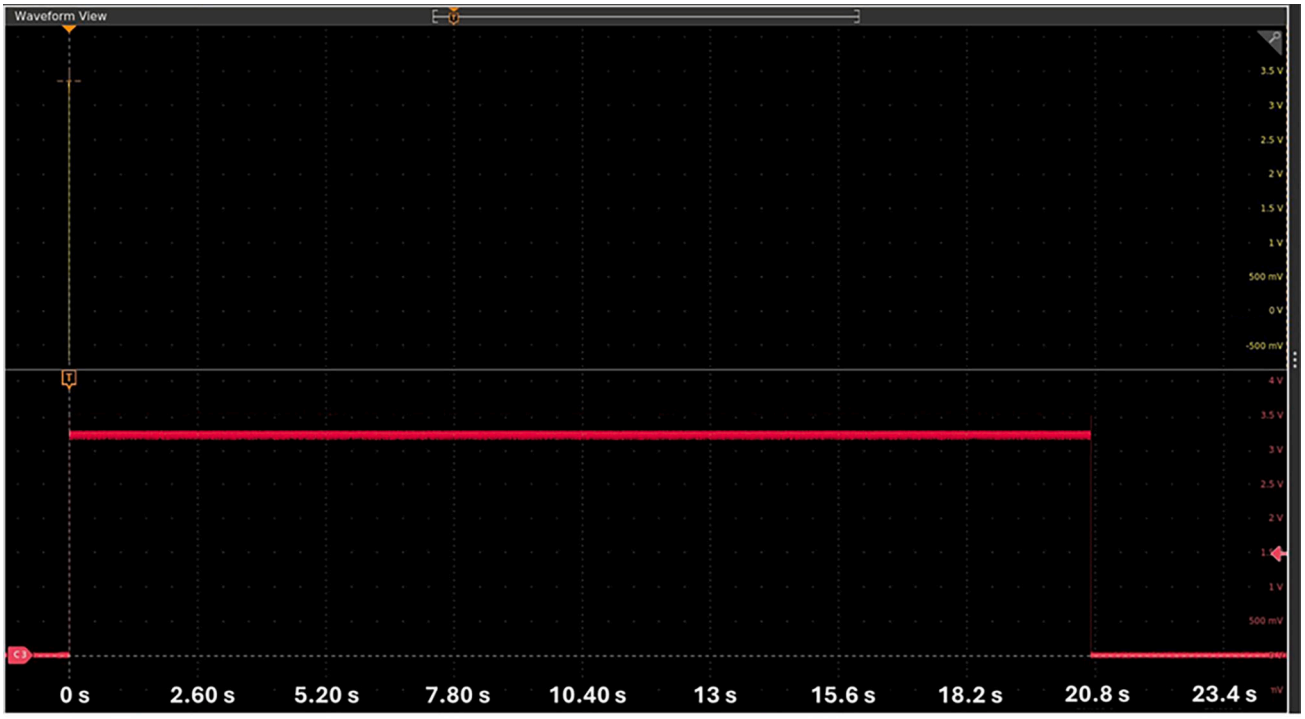


Fig. 2. Measured processing time for DFT calculation (1667 samples).

delay of a signal by a non-integer amount. This can be useful in various applications such as audio processing, communication systems, and control systems. The choice between FIR and IIR filters for implementing FD-DFs depends on various factors such as the desired accuracy, computational complexity, stability, and phase response.

In detail, for a giver function $f(x)$ in the x variable, the N order interpolator polynomial of Lagrange $L(x)$ is defined starting from $n+1$ samples $(a_0,\ a_1,\ a_2,\ \cdots a_n)$ and the related values $[f(a_0),\ f(a_1),\ f(a_2)\cdots f(a_n)]$, as:

$$\boldsymbol{L(x)} = \sum_{i=0}^{n} \boldsymbol{f(a_i)} \bullet \prod_{j=0 j\neq i}^{n} \frac{\boldsymbol{x}-\boldsymbol{a_j}}{\boldsymbol{a_i}-\boldsymbol{a_j}} \tag{1}$$

This implies that for each value of x all the coefficients of the interpolating polynomial must be recalculated.

Farrow interpolator can be seen as a particular case of Lagrange interpolator.

It can be implemented in different h order functions and it uses the same coefficients calculation to generate a function that tries to approximate the original signal every $h+1$ points. In Lagrange, every time a new point is considered, the entire polynomial must be recalculated, as reported in Eq. (1). For Farrow implementation, it is assumed that the samples are equidistant, which is a reasonable assumption if a fixed sampling frequency is considered. Whit this assumption, the calculation time is significantly reduced even with higher order functions, because it is not necessary calculate the series of products and ratios of the term $\prod_{j=0 j\neq i}^{n} \frac{x-a_j}{a_i-a_j}$.

In detail, in continuous time domain, a h order function can be express as:

$$f(t) = k_h t^h + k_{h-1} t^{h-1} + \cdots + k_1 t + k_0 \tag{2}$$

with k_i = constant, for $i = h, h-1, h-2 \cdots 0$.

In discrete time domain, according to Farrow hypothesis, a distance between two consecutive samples equal to T_s is considered, so the samples n and $n+1$ are placed at the time $n \bullet T_S$ and $(n+1) \bullet T_s$, respectively. The observation window T_w is equal to the total number of samples N multiplied by Ts. The value of the signal at the time $n \bullet T_s$ is the value of the sample n and it can be calculated only with n = integer.

The mathematical procedure of interpolate to increase or reduce the number of samples from N to the number of interpolated points P is equivalent to change T_S keeping constant T_w, so to have:

$$N \bullet T_s = P \bullet T_{snew} \tag{3}$$

The ratio of T_{snew}/T_s is called interpolation ratio and it is a constant.

To calculate the placement of a new point p, it is assumed that the time pT_{snew} can be expressed as:

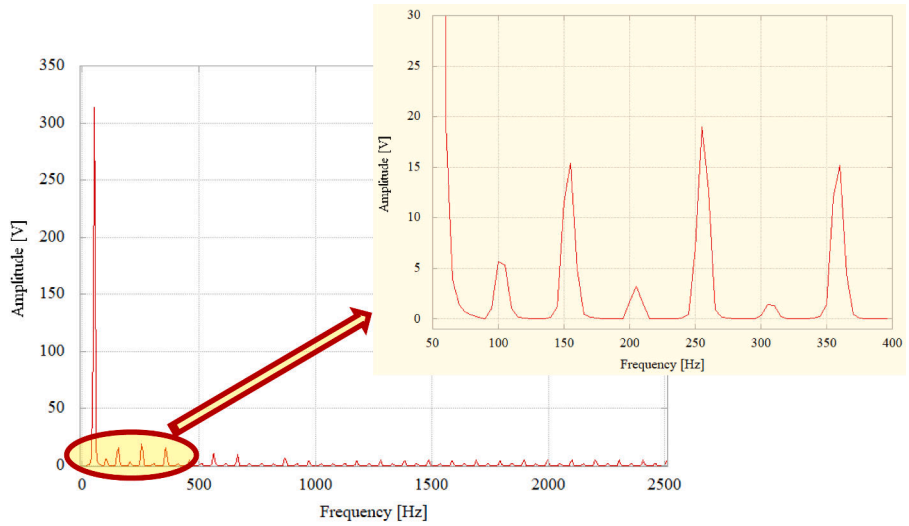
$$pT_{snew} = (n+\mu) \bullet T_S \tag{4}$$

In (4) p is the index of each point after interpolation ($p = 0,1,2 \ldots P$) and μ is a value between 0 and 1; n is the closest integer value that fulfils the relationship $pT_{snew} \geq nTs$; thus, n is the acquired sample which is immediately preceding the point p to be interpolated and it is taken as reference for the interpolation (see Fig. 5).

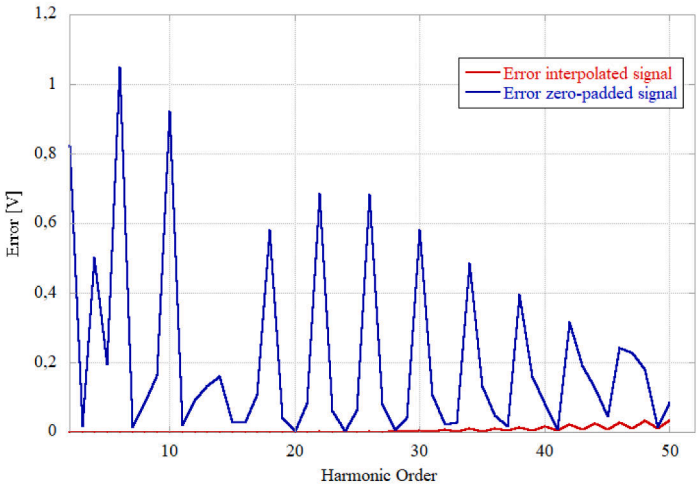
Starting from these considerations, it is possible to express the value of the interpolating h-order function z at every time $(p \bullet T_{snew})$, within the observation window, just changing the coefficients K and μ, as follows:

$$z(nT_S + \mu Ts) \approx K_h (nT_S + \mu Ts)^h + K_{h-1}(nT_S + \mu Ts)^{h-1} + \cdots + K_1 (nT_S + \mu Ts) + K_0 \tag{5}$$

For example, for a third order function, the variables are the four coefficients K_3, K_2, K_1 and K_0. They can be calculated by using the known values of the function of 4 consecutive acquired samples placed at $(n-1)T_s$, nT_s, $(n+1)T_s$ and $(n+2)T_s$. Under the hypothesis that T_S is constant, the four coefficients can be expressed with the only dependence of the parameter μ and the values of the four acquired samples. With few mathematical passages, it is possible to express the interpolating function in the only variable μ:



(a)



(b)

Fig. 3. FFT analysis with ZP. (a) Obtained spectrum; (b) harmonics measurement errors and comparison with TDI technique.

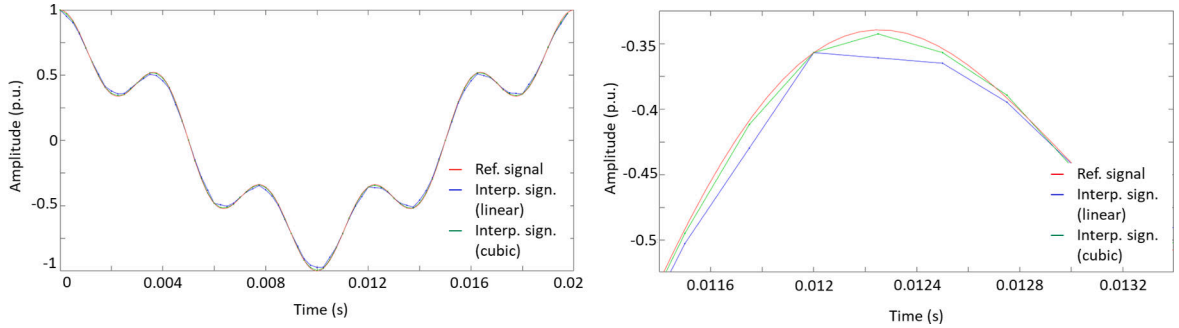


Fig. 4. Comparison between different interpolation functions (linear and cubic). Example with a non-sinusoidal signal (fundamental 50 Hz component and 5th harmonic). On the left: one signal period (0–0.02 s); on the right: zoom between 0.0116 s and 0.0132 s.

$$\begin{aligned} \boldsymbol{z}(\boldsymbol{n}\bullet\boldsymbol{Ts}+\boldsymbol{\mu}\bullet\boldsymbol{Ts}) = &\left(\frac{\boldsymbol{\mu}^3}{6}-\frac{\boldsymbol{\mu}}{6}\right)\boldsymbol{z}((\boldsymbol{n}+2)\boldsymbol{Ts})+\left(-\frac{\boldsymbol{\mu}^3}{2}+\frac{\boldsymbol{\mu}^2}{2}+\boldsymbol{\mu}\right)\boldsymbol{z}((\boldsymbol{n}+1)\boldsymbol{Ts}) \\ &++\left(\frac{\boldsymbol{\mu}^3}{2}-\boldsymbol{\mu}^2-\frac{\boldsymbol{\mu}}{2}+1\right)\boldsymbol{z}((\boldsymbol{n})\boldsymbol{Ts}) \\ &+\left(-\frac{\boldsymbol{\mu}^3}{6}+\frac{\boldsymbol{\mu}^2}{2}-\frac{\boldsymbol{\mu}}{3}\right)\boldsymbol{z}((\boldsymbol{n}-1)\boldsymbol{Ts}) \end{aligned} \tag{6}$$

In this way, for each interpolated point, only μ must be calculated, and not the h+1 coefficients as for the h-order Lagrange polynomial. This allows decreasing the number of operations needed for the interpolation and the time required for the algorithm execution.

To reduce the calculation, in coding programming it is possible to rewrite the expression (6) using matrix and vectors, because the coefficients of μ^h are constant. This can be made for every Farrow function

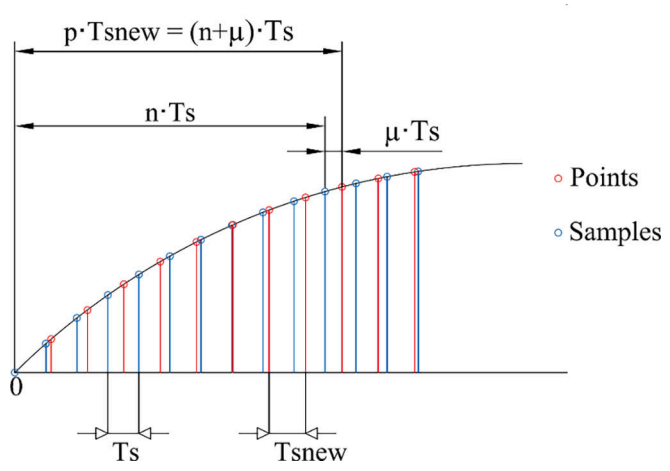


Fig. 5. Scheme of Farrow interpolation.

order. For example, for the third order function, it is possible to define the vector (column) μ^* as:

$$\mu^* = [\mu^3; \mu^2; \mu; 1]$$

The matrix C can be defined as:

i	c_3[i]	c_2[i]	c_1[i]	c_0[i]
−2	1/6	0	−1/6	0
−1	−1/2	1/2	1	0
0	1/2	−1	−1/2	1
1	−1/6	1/2	−1/3	0

Thus, it is possible to express equation (6) as follows:

$$\boldsymbol{z}(\boldsymbol{n} \bullet \boldsymbol{Ts} + \boldsymbol{\mu} \bullet \boldsymbol{Ts}) = \boldsymbol{H}[-2]\boldsymbol{z}((\boldsymbol{n}+2)\boldsymbol{Ts}) + \boldsymbol{H}[-1]\boldsymbol{z}((\boldsymbol{n}+1)\boldsymbol{Ts}) + \boldsymbol{H}[0]\boldsymbol{z}((\boldsymbol{n})\boldsymbol{Ts}) + \boldsymbol{H}[+1]\boldsymbol{z}((\boldsymbol{n}-1)\boldsymbol{Ts}) \quad (7)$$

i.e.

$$z(n \bullet Ts + \mu \bullet Ts) = \sum_{i=-2}^{1} H[i] z((n-i)T_S) \quad (8)$$

where

$$H[i] = \sum_{l=0}^{3} C[i]\mu^l \quad (9)$$

By substituting (8) and (9) in (7):

$$z(n \bullet Ts + \mu \bullet Ts) = \sum_{i=-2}^{1} \sum_{l=0}^{3} C[i]\mu^l z((n-i)T_S); \quad (10)$$

$$z(n \bullet Ts + \mu \bullet Ts) = \sum_{l=0}^{3} \mu^l \sum_{i=-2}^{1} C[i] z((n-i)T_S) \quad (11)$$

The term $\sum_{i=-2}^{1} C[i]z((n-i)T_S)$ is defined as $Y(l)$; thus, the aforesaid expression becomes:

$$z(n \bullet Ts + \mu \bullet Ts) = \sum_{l=0}^{3} Y(l) \bullet \mu^l \quad (12)$$

The extended form is:

$$z(n \bullet Ts + \mu \bullet Ts) = Y(3)\mu^3 + Y(2)\mu^2 + Y(1)\mu + Y(0) \quad (13)$$

For a better implementation, it can be rewritten as:

$$z(n \bullet Ts + \mu \bullet Ts) = [(Y(3)\mu + Y(2))\mu + Y(1)]\mu + Y(0) \quad (14)$$

In comparison with Lagrange implementation, the main simplification of this method is that $Y(l)$ is evaluated just by multiplying the matrix C constants by the acquired samples at $(n-1)T_s$, nT_s, $(n+1)T_s$ and $(n+2)T_s$. By calculating μ for every new point p starting from the interpolation ratio, the implementation of the interpolation algorithm is very easy, even with a third order function.

As a numerical example of μ calculation, let us consider the case of Tw = 0.2 s and a sampling frequency of $f_s = 24$ kHz; the sampling time is $T_s = 1/24000 = 41.667 \bullet 10^{-6}$ s and the number of acquired samples is $N = f_s \bullet Tw = 4800$. The desired number of points for FFT, after interpolation is $P = 4096$ (i.e. P is lower than N); this corresponds to a new equivalent sampling frequency of $f_{snew} = 4096/0.2 = 20480$ kHz and $Ts_{new} = 1/f_{snew} = 48.828 \bullet 10^{-6}$ s.

Let us consider the interpolation of the point of index $p = 9$. The point is placed at the time $p \bullet Ts_{new} = \frac{9}{20480} = 439.45\,10^{-6}$ s;

The first step is to find the index of the acquired sample strictly before the point p;

$$pT_{snew} \geq nTs;$$

$$n = \frac{p \bullet Ts_{new}}{Ts} = \frac{9 \bullet 24000}{20480} = 10.546;$$

$$n_{integer} = 10$$

Starting from this, it is possible to calculate μ as follows:

$$pT_{snew} = (n+\mu) \bullet T_S;$$

$$\mu = \frac{p \bullet Ts_{new}}{Ts} - n_{integer} = \frac{9 \bullet 24000}{20480} - 10 = 0.546.$$

The same procedure can be applied when P is higher than N.

For example, let us consider the case of a different sampling frequency, i.e. fs = 16 kHz, which corresponds to a sampling time of $T_s = 1/16000 = 62.5 \bullet 10^{-6}$ s, and a number of acquired samples $N = f_s \bullet Tw = 3200$, for the same $Tw = 200$ ms. As for the previous example, $P = 4096$, f_{snew}= 20480 kHz, $Ts_{new} = 1/f_{snew} = 48.828 \bullet 10^{-6}$ s, $p = 9$ and $p \bullet Ts_{new} = \frac{9}{20480} = 439.45\,10^{-6}$ s.

By repeating the process described above, the μ calculation for the interpolation of p is obtained as follows:

$$pT_{snew} \geq nTs;$$

$$n = \frac{p \bullet Ts_{new}}{Ts} = \frac{9 \bullet 16000}{20480} = 7.031;$$

$$n_{integer} = 7$$

$$pT_{snew} = (n+\mu) \bullet T_S;$$

$$\mu = \frac{p \bullet Ts_{new}}{Ts} - n_{integer} = \frac{9 \bullet 16000}{20480} - 7 = 0.031.$$

It is worth noting that the interpolation allows maintaining the synchronous sampling condition, since the observation window length is not modified, according to equation (3), i.e. $N \bullet T_s = P \bullet T_{snew}$.

In this viewpoint, the advantage of using the proposed Farrow time domain interpolation is that, for a given observation window Tw, it allows optimizing the computational burden of harmonic analysis, whatever the values of sampling frequency f_s and number of acquired samples are. In detail, as previously mentioned, for IEC 61000-4-7 Class I harmonics measurements, the first requirement is to synchronize the observation window length to 10/12 cycles of the 50/60 Hz fundamental power system frequency f. In real operating conditions, if small frequency variations occur, the observation window ($Tw = 10/f$) shall change too, to ensure the sampling synchronization (i.e. 200 ms for f = 50 Hz, 199.8 ms for f = 50.05 Hz, etc.). This condition can be achieved by keeping constant the number N of acquired samples and by varying

the sampling frequency *fs*, or vice versa (or even by varying both parameters, keeping constant their ratio $Tw = 10 / f = N/f_s$). In the first case, when the sampling frequency can be adjusted (even finely, as in high-quality PQ meters), for a given value of *N*, the sampling synchronization can be obtained by varying f_s, as a function of *f* (for example, if $N = 4096$, $f_s = 20.48$ kHz for $f = 50$ Hz, or $f_s = 20.50$ kHz for $f = 50.05$ Hz, etc.). However in many low-cost platforms for typical smart metering purposes, sampling frequency can be fixed or not so finely adjustable; thus the variations of fundamental frequency may lead to a loss of synchronization, unless the number of samples *N* is changed (in previous examples, if $f_s = 24$ kHz, $N = 4800$ for $f = 50$ *Hz*, or $N = 4795$ for $f = 50.05$ *Hz*, etc.; equally, if $f_s = 20.48$ kHz and $f = 50.05$ *Hz*, $N = 4092$). This means that in real cases *N* can be different from a power of two, depending on the sampling frequency available for the used device and/or the actual power system frequency.

To solve the issue, in the solution herein presented, Farrow interpolation is used to obtain the desired power-of-two number of interpolated points (for efficient FFT calculation) in a synchronous observation window, whatever the power system frequency, sampling frequency and number of acquired samples are. In the following, tests are referred to the most restrictive case of fixed sampling frequency. In more detail, different fixed sampling frequencies were tested. For each considered case, the observation window is synchronized by means of a zero-crossing technique (thus, if the fundamental frequency varies, the number of acquired samples will vary accordingly). Farrow interpolation is then applied to obtain the power-of-two number of interpolated points for FFT calculation (which will correspond to the new equivalent sampling frequency, f_{snew} for the sequence of interpolated samples).

4. Algorithms implementation and preliminary validation

To evaluate the errors in the approximation of the signal due to interpolation, more specifically the differences between Lagrange and Farrow algorithms (first, second and third order), and the impact of such errors on spectral analysis accuracy, a simulation study was carried out by using the approach schematized in Fig. 6.

Both Lagrange (linear, quadratic and cubic) and Farrow (first, second and third order) interpolation algorithms were written in C language using a PC-based IDE. The algorithms were firstly implemented in floating-point 32-bit coding. A Virtual Instrument (VI, in LabVIEW environment) was built for the generation of the reference test signal, i.e. a 50 Hz and 230 Vrms signal with harmonics up to 50th order. Sampling parameters (i.e. sampling frequency f_s and number of samples *N*) were set to simulate the acquisition of *N* samples in a time window of $Tw = 200$ ms (i.e. 10 cycles of the 50 Hz fundamental frequency) with different sampling frequencies, i.e.f_s = 16, 24, and 32 kHz, and N = 3200-4800-6400 samples, respectively. The samples were then processed by the interpolation algorithms to obtain a number of points *N'* after interpolation equal to a power of two for the spectral analysis implementation via FFT algorithm ($N' = 2048$ or 4096 points were considered in the study). The errors introduced by the interpolation algorithm were estimated by comparing the results of the spectral analysis with the harmonic components amplitudes of the simulated reference test signal.

As regards the test signal, the IEC 61000-4-30 and IEC 61000-4-7 report limits on the accuracy of harmonics measurement up to the 50th order harmonic, but they do not give any information about the signal waveform, in terms of single harmonics amplitudes or overall harmonic distortion level; thus, the signal used for the simulations was built in accordance with the standard EN 50160 "Voltage characteristics of electricity supplied by public distribution systems", which provides amplitudes limits for harmonics up to the 25th [39]. For higher order harmonics, amplitudes were set to values similar to those of EN 50160, i.e. 0.5 % and 1.5 % of the fundamental for even and odd harmonics, respectively [32,33]. The test signal harmonics amplitudes are summarized in Table 3. The waveform of the test voltage signal is shown in Fig. 7.

The VI assessed if the IEC 61000-4-7 error limits were fulfilled or not. In detail, class I instrumentation requirements were taken into account; for such instruments, the error limits for harmonic measurement are:

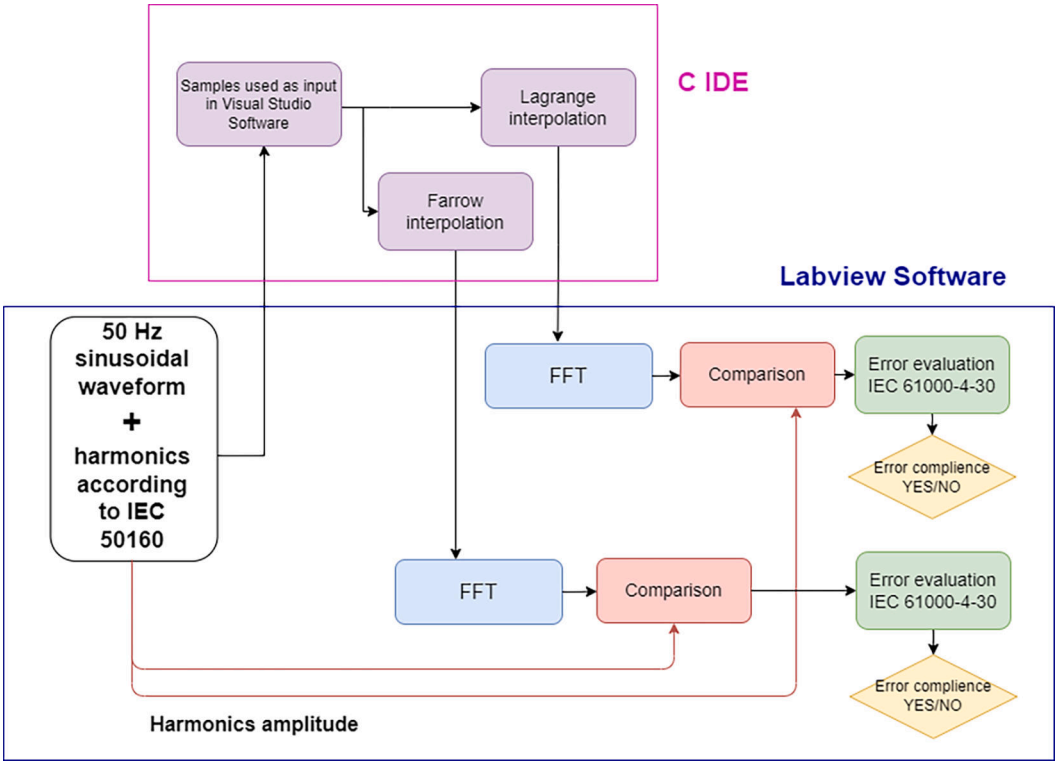


Fig. 6. Block diagram of the test system for error comparison.

Table 3
Test signal. Harmonics amplitudes (in percentage of fundamental).

Even order harmonics		Odd order harmonics			
Order *h*	Relative amplitude *uh*	Order *h* (multiple of three, up to 21st)	Relative amplitude *uh*	Order *h* (other, up to 49th)	Relative amplitude *uh*
2	2,00 %	3	5,00 %	5	6,00 %
4	1,00 %	9	1,50 %	7	5,00 %
6 ÷ 50	0,50 %	15, 21	0,50 %	11	3,50 %
				13	3,00 %
				17	2,00 %
				19 ÷ 49	1,50 %

uh is the amplitude of the h-order harmonic (percentage of fundamental component).

- $e \leq 5\ \%\ Um$, for $Um \geq 1\ \%\ Unom$,
- $e \leq 0.05\ \%\ Unom$, for $Um < 1\ \%\ Unom$,

where *Um* is the measured amplitude of each harmonic component and *Unom* is the rated voltage.

The simulated cases and obtained results of compliance with the standard limits are summarized in Table 4.

Some detailed results of comparison between Lagrange and Farrow algorithms are reported in Fig. 8, Fig. 9 and Fig. 10.

The results of Fig. 8 refer to the case n.1, ($f_s = 16$ kHz, linear interpolation, 2048 points); it can be seen that errors with Farrow and Lagrange first order algorithms are almost the same; small differences are due to rounding errors in calculations; the first order linear interpolation is not feasible with $f_s = 16$ kHz. Similar results were obtained with interpolation to 4096 points (case n. 4). On the other hand, simulations results with linear interpolation and higher sampling frequencies (cases n. 2–3 and n. 5–6) showed errors within the standard limits; for example the results for the case n. 2 are shown in Fig. 9. For higher order interpolation functions error limits were met for all considered sampling frequencies, instead; for example, results of case n. 13 are reported in Fig. 10.

According to these results and in the perspective of implementing the algorithm on a commercial microcontroller board and performing experimental tests with all sampling frequencies considered in simulations (see next section), the third order Farrow function was chosen for the implementation, as it offered the best tradeoff between accuracy and computational cost. In fact the third order Farrow function has a lower computational cost compared to the Lagrange function, while maintaining the same level of accuracy. Additionally, it can be used for all sampling frequencies, so ensuring proper signal reconstruction, with both 2048 and 4096 points, and compliance with the standards limits.

To further investigate the feasibility of implementation on a commercial microcontroller board (without requiring any coding conversion), a comparison between fixed-point and floating-point coding was performed. Fixed-point and floating-point functions were implemented and compared in the same test conditions of previous simulations. In all cases close results were obtained for the FFT analysis and the harmonics amplitudes errors, with fixed-point errors slightly higher than floating-point ones (as expected). As an example, the results Case n. 13 test are reported in Fig. 11. These results confirmed the feasibility of fixed-point coding, which was used for the implementation on the case study microcontroller board (see next section).

5. Data acquisition and harmonic analysis. Microcontroller device characterization

To validate the simulation results and to assess the feasibility of developing a cost-effective device for harmonic analysis, the metrics for interpolation and FFT analysis were implemented on a commercial low-cost microcontroller board. The chosen board for the case study is the NUCLEO STM32F767ZI, by STMicroelectronics; it is equipped with a 12-bit ADC, a 0–3.3 V input range, and a maximum CPU frequency of 216 MHz. An experimental characterization was made to investigate the feasibility of using such device for the implementation of harmonic analysis according to IEC 61000-4-7 Class I instrument requirements.

The final aim of the study was to evaluate to what extent Class I harmonic analysis can be integrated into existing low-cost hardware platforms for smart metering, which normally have limited hardware features, especially concerning the ADC (in terms of effective number of bits or the possibility of varying the sampling frequency with high resolution, according to the power system signal frequency). In this viewpoint, the NUCLEO board was chosen as case study device since it has typical hardware features of low-cost platforms, with low performance in terms of ADC accuracy features, but suitable computational and memory capabilities, as well as the possibility to change the sampling frequency, according to the solutions investigated in the study.

In more detail, the performance of commercial smart metering platforms and the issues related to the integration of power quality and harmonics measurements on such devices were analyzed in earlier work. Some limitations of such platforms were highlighted, even supported by experimental tests on different case study platforms (for example the STCOMET smart meter device used in [2]). It was shown that the main issue for low-cost commercial platforms is related to the available sampling frequency options. In fact, sampling frequency can be adjusted (even finely) in high-quality PQ instrumentation, according to the actual power system frequency. On the contrary many smart metering

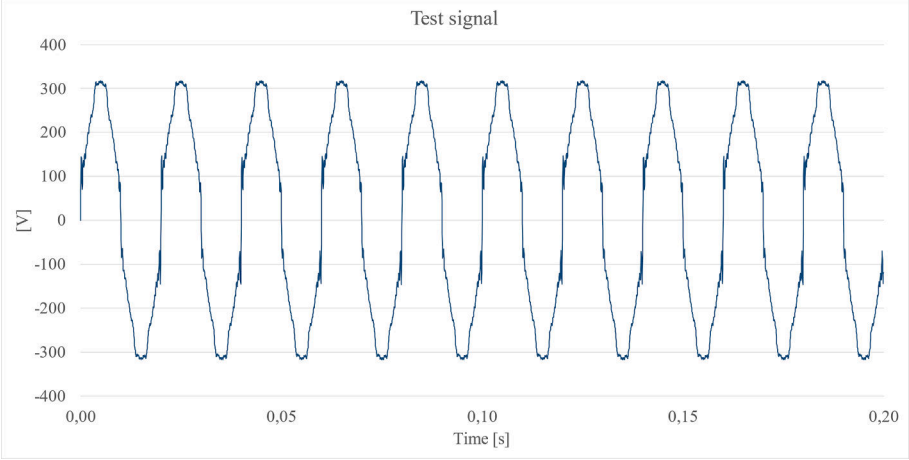


Fig. 7. Test signal waveform.

Table 4
Simulated cases for interpolation algorithms test and compliance with the standard limits.

Case	Interp. Algorithms	Number of pointsafter interpolation	SamplingFrequency [kHz]	Standard complience
n.1	Lagrange 1st order	2048	16	Not verified
	Farrow 1st order			Not verified
n.2	Lagrange 1st order		24	Verified
	Farrow 1st order			Verified
n.3	Lagrange 1st order		32	Verified
	Lagrange 1st order			Verified
n.4	Lagrange 1st order	4096	16	Not verified
	Farrow 1st order			Not verified
n.5	Lagrange 1st order		24	Verified
	Farrow 1st order			Verified
n.6	Lagrange 1st order		32	Verified
	Lagrange 1st order			Verified
n.7	Lagrange 2nd order	2048	16	Verified
	Farrow 2nd order			Verified
n.8	Lagrange 2nd order		24	Verified
	Farrow 2nd order			Verified
n.9	Lagrange 2nd order		32	Verified
	Farrow 2nd order			Verified
n.10	Lagrange 2nd order	4096	16	Verified
	Farrow 2nd order			Verified
n.11	Lagrange 2nd order		24	Verified
	Farrow 2nd order			Verified
n.12	Lagrange 2nd order		32	Verified
	Farrow 2nd order			Verified
n.13	Lagrange 3rd order	2048	16	Verified
	Farrow 3rd order			Verified
n.14	Lagrange 3rd order		24	Verified
	Farrow 3rd order			Verified
n.15	Lagrange 3rd order		32	Verified
	Farrow 3rd order			Verified
n.16	Lagrange 3rd order	4096	16	Verified
	Farrow 3rd order			Verified
n.17	Lagrange 3rd order		24	Verified
	Farrow 3rd order			Verified
n.18	Lagrange 3rd order		32	Verified
	Farrow 3rd order			Verified

platforms have a fixed sampling frequency, which can be also lower than the minimum required for Class I constraints on sampling synchronization. In this case, as shown in [2], even if high-quality ADCs are used (24-bit sigma-delta), Class I cannot be reached because of the synchronization error. If higher sampling frequencies can be available, namely from 10 kHz on (considering possible power system frequency variations), Class I feasibility can be investigated, instead. In [32,33] preliminary studies were made on measurement accuracy and repeatability, with both high-quality data acquisition hardware and with devices with limited ADCs features. As shown in the following, the implementation of efficient FFT calculation can be done thanks to the time domain interpolation; if the Class I requirements are not reached, the combination with suitable sampling strategies can be used, compatibly with the available sampling frequency options. In this viewpoint, the STMicroelectronics NUCLEO board was chosen as test platform, as it is equipped with 12-bit ADCs, with limited metrological features (if compared with those of the smart metering platforms previously mentioned). On the other hand, it can allow a wide range of sampling frequencies, and it has enough memory and computational capabilities to achieve a suitable processing time, also in the perspective of Class I gapless implementation (where the overall processing time should be lower than 200 ms).

When hardware solutions with fixed sampling frequency are considered, a possible approach to cope with this constraint could be to choose or design the device to have a suitable sampling frequency, i.e. an integer multiple of the rated 50/60 Hz frequency value, that would allow acquiring a power-of-two number of samples in a synchronous observation window of 10 periods, for effective FFT calculation. However, as mentioned in section III, small variations of frequency normally occur in power systems. This means that, after adjusting the system to have the desired sampling frequency and number of samples, the power system frequency variations would lead to asynchronous sampling (if sampling parameters are kept constant) or to the acquisition of a number of points not equal to a power of 2 (if the number of samples is changed to synchronize the observation window). For example, for 50 Hz power system frequency, 2048 samples can be acquired in $Tw = 200$ ms, with sampling frequency of 10240 Hz. If a variation of signal frequency of 0.1 Hz occurs, the observation window length should be $T'w = 10/f' = 10/50.1 = 199.6$ ms. If the sampling frequency remains constant, the number of samples to be acquired to match the observation window synchronization should be $N' = f_s \bullet T'w \approx 2044$.

Another aspect to consider, even more relevant in the case of low-cost devices (including the board herein used for tests), is the low stability of the ADC sampling frequency. It may cause a variation of the number of samples to be acquired to keep the observation window synchronized with power system frequency. To investigate the impact of such kind of phenomenon, some experimental tests have been carried on the case study NUCLEO board. A sampling frequency value was set and a 50 Hz signal was acquired in subsequent observation windows of 10 cycles of the signal ($Tw = 200$ ms); the actual sampling frequency was measured for each test. Some results are reported in Table 5. They refer to the case of the aforesaid sampling frequency set to $fs = 10240$ Hz; as can be seen, the actual sampling frequency showed small fluctuations, leading to consequent variation of the number of acquired samples in the given observation window.

With the use of an interpolation algorithm, as the Farrow one presented in the previous section, both the aforesaid problems can be solved, since the power-of two number of samples and the observation window synchronization can be obtained, whatever actual sampling frequency and number of acquired samples are.

6. Experimental setup for harmonics measurements

The experimental setup is depicted in Fig. 12. A calibrator (Fluke 5720A or Fluke 6100A, for tests with sinusoidal and distorted signals, respectively) and a reference voltage divider (Precision Ratio Transformer TEGAM PRT73) were used for generating the test signal. A

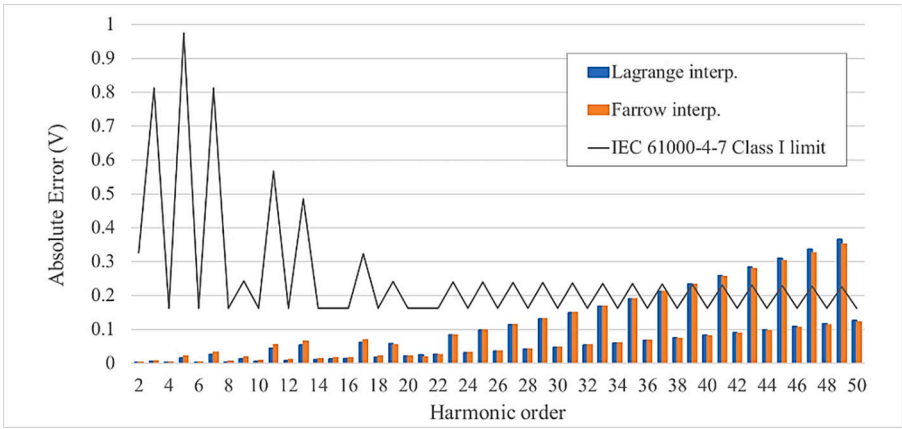


Fig. 8. Comparison between Lagrange and Farrow algorithms. Case n.1: f_s = 16 kHz, linear interpolation, 2048 points.

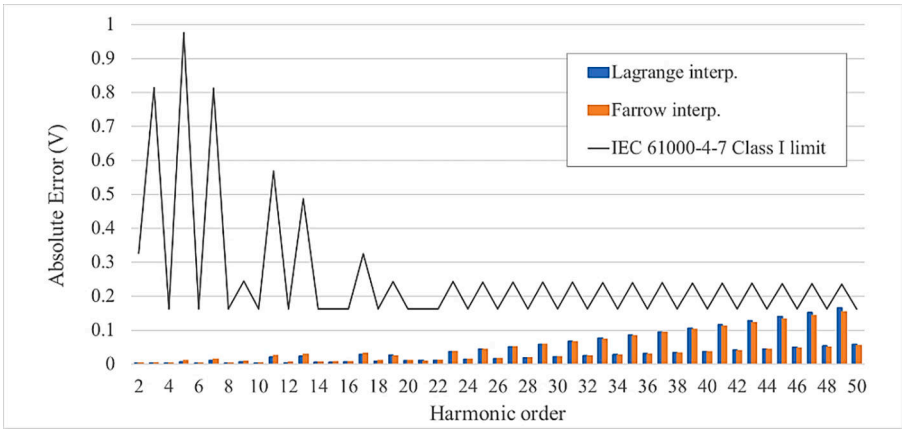


Fig. 9. Comparison between Lagrange and Farrow algorithms. Case n.2: f_s = 24 kHz, linear interpolation, 2048 points.

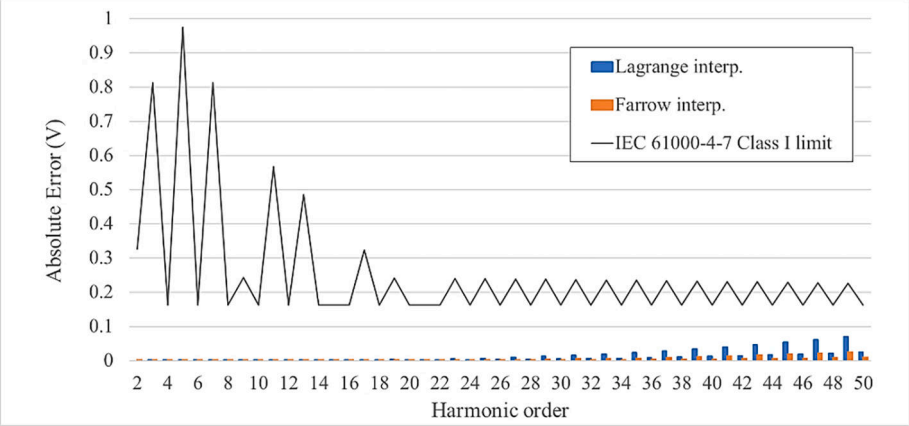


Fig. 10. Comparison between Lagrange and Farrow algorithms. Case n.13: f_s = 32 kHz, third-order interpolation, 2048 points.

Tektronix AFG31152 signal generator was used to generate a continuous component, which was necessary to adapt the signal to the ADC's input range of 0–3.3 V. To exploit the full dynamic range of the NUCLEO board ADC, the power calibrators and the voltage divider were set to have a 3.3 Vpp signal at the output of the voltage divider. This signal was added to a 1.65 V DC component generated by the Tektronix AFG31152, by means of an op-amp adder circuit; a low-noise op-amp AD797 was used for this purpose. The op-amp circuit provided also for a decoupling between the signal generator and the calibrator, so to avoid over-currents circulation (above the allowable limits for power calibrator output currents). A second-order active filter was also added at op-amp output, to reduce out-of-band noise (from 2.5 kHz on) and prevent aliasing.

The observation window *Tw* for data acquisition was set to 10 cycles of the 50 Hz test signal, according to IEC 61000-4-30 requirements. After acquiring and storing the data on the on-board memory of the NUCLEO device, the acquired samples were processed by means of Farrow third-order interpolation and the FFT algorithms, so to obtain the harmonics

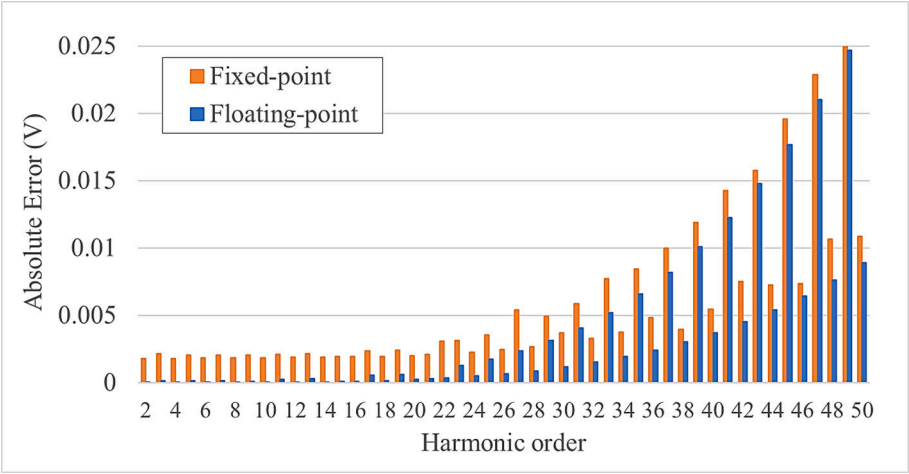


Fig. 11. Comparison between fixed-point and floating-point implementation. Farrow algorithm (third order). Case n. 13: f_s = 32 kHz, third-order interpolation, 2048 points.

Table 5
Experimental measurement of sampling frequency fluctuations in subsequent observation windows (Tw = 200 ms).

Test	Set fs [Hz]	Expected number of acquired samples	Measured fs [Hz]	Actual number of acquired samples
1	10,240	2048	10245.5	2049
2			10250.0	2050
3			10245.1	2049
4			10253.7	2051
5			10236.6	2047
6			10243.4	2049
7			10235.1	2047
8			10230.3	2046
9			10242.9	2049
10			10224.8	2045

amplitudes measurements. To meet the requirement on the coherent sampling (maximum synchronization error of 0.03 %), sampling synchronization was obtained by means of a zero-crossing algorithm implemented on the microcontroller board. In fact, preliminary signal acquisition tests showed a low stability of the internal clock of the microcontroller board, which resulted in an inaccurate setting of the sampling frequency and number of samples to be acquired in the observation window. To correct such behavior, more than 10 signal cycles (about 11 cycles) were acquired; the zero-crossing algorithm provided for synchronizing the *Tw* window to the desired length of 10 cycles, and for removing the unneeded samples before starting the signal processing (interpolation and FFT).

Sinusoidal tests were carried out to perform a preliminary characterization of the measurement setup (the microcontroller device and the signal conditioning). Tests with sinusoidal waveforms were carried out and the acquired signal was analyzed to evaluate four parameters: ENOB (effective number of bits), SiNAD (signal to noise and distortion ratio), SFDR (spurious free dynamic range), and THD (total harmonic distortion). A picture of the test bench for the tests with sinusoidal signals and the Fluke 5720A calibrator is shown in Fig. 13. The test bench for the tests with distorted signals and the Fluke 6100A calibrator is shown in Fig. 14, instead. The generation of the voltage signal has been done with a FLUKE 6100A calibrator; harmonics amplitudes, were the same of the test waveform used for the preliminary algorithm validation tests (i.e. harmonics up to 50th, with amplitudes, expressed in percentage of the fundamental, equal to Table 3. values).

To compare the microcontroller board performances with those of a

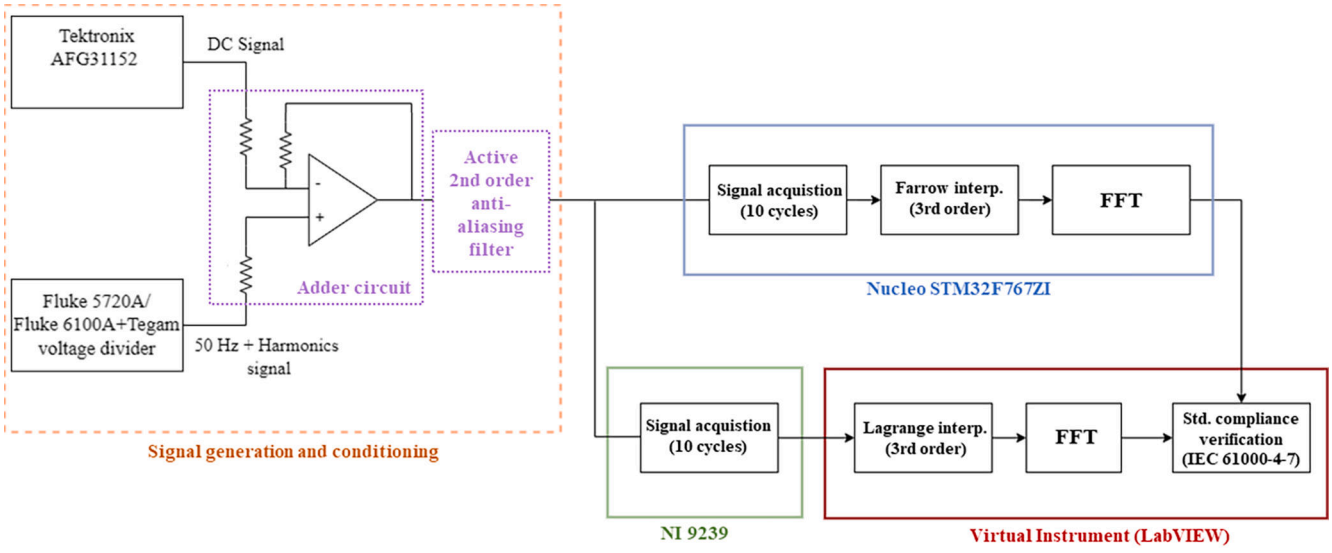


Fig. 12. Experimental setup scheme.

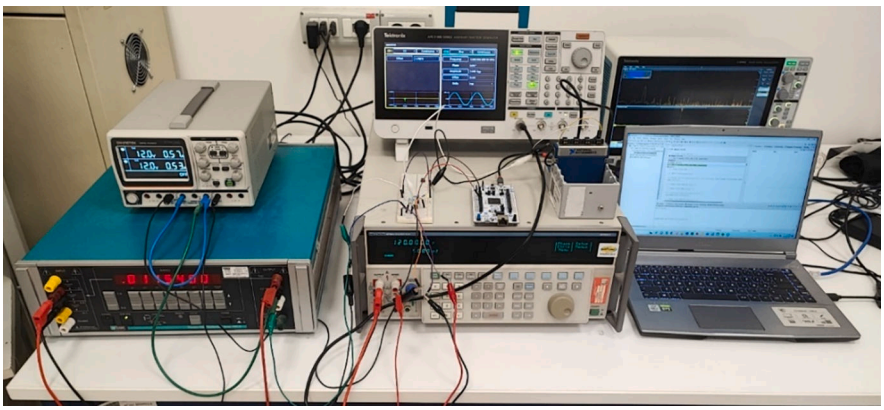


Fig. 13. Experimental setup – Sinusoidal tests (with Fluke 5720 calibrator).

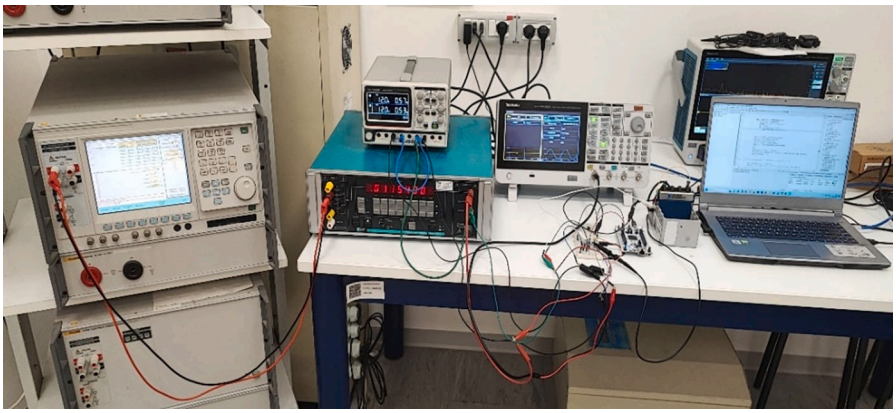


Fig. 14. Experimental setup –Tests with harmonics (with Fluke 6100A calibrator).

more accurate system, the errors on the harmonics measurements were compared with those obtained with a reference PC-based instrument, built with a NI 9239 data acquisition board (24-bit ADC, −10/+10 V input range) and a virtual instrument in LabVIEW environment, implementing both the interpolation (Lagrange cubic function) and the FFT analysis, with the same number of points of the microcontroller measurements (2048 or 4096, depending on the test conditions). For both the NUCLEO board and the NI 9239 PC-based instrument, the errors were compared with the IEC 61000-4-7 Class I limits.

Moreover a digital oscilloscope (Tektronix MSO54 5-BW-350) was used to measure the time employed by the NUCLEO board to process the acquired samples and to obtain the harmonic analysis results, so to investigate the feasibility of a gapless data acquisition and analysis, according to IEC 61000-4-30 Class A requirements. The measurements were carried out by acquiring a signal at three output pins of the NUCLEO board (one for each signal processing stage, i.e. preprocessing – if any –, interpolation and FFT). Each pin signal was changed from low to high level at the beginning of the related processing task and it was changed back to low level at the end of the task.

Three sequences of tests were carried out, to investigate the microcontroller device performances with different sampling and processing conditions. The detailed test cases are reported in Table 6. The first series of tests (test condition (1), test cases n. 19–24) were carried out in the same operating conditions of the preliminary tests for algorithms validation (sampling frequenciesf_s = 16–24-32 kHz, number of acquired samples N = 3200–4800-6400, third-order Farrow interpolation to 2048/4096 points; see previous section, test cases n. 13–18). These tests allowed to evaluate the performances of the whole measurement system, and to compare the results with those of the preliminary validation, so to analyze the impact of the data acquisition stage on the overall measurement accuracy. As shown in the following sections, the experimental tests showed unfeasible results, even with third-order interpolation algorithm, due to the low resolution of data acquisition. Further tests were carried out the feasibility of using different solutions for samples acquisition and preprocessing, aimed at improving the device

Table 6
Summary of experimental tests conditions.

Test condition	Test case	Sampling and pre-processing	Points after interpolation (Farrow, 3rd order)
1	19–24	Sampling frequency of 16-24-32 kHz; zero-crossing synchronization for coherent sampling; no pre-processing	2048 / 4096
2	25–57	Oversampling at different sampling frequencies; zero-crossing synchronization for coherent sampling; digital filter and decimation (equivalent sampling frequencies of 16-24-32 kHz after decimation)	
3	58–75	Oversampling at different sampling frequencies; zero-crossing synchronization for coherent sampling; moving average (equivalent sampling frequencies of 16-24-32 kHz after average)	

performances. In detail, the second and third series of tests were carried out by employing oversampling techniques; in detail for the second series of tests, after acquiring the samples (with a given oversampling factor), a pre-processing with digital filtering and decimation is applied to obtain the new sequence of samples, with an equivalent sampling frequency off$_s$ = 16, 24, or 32 kHz, to be further processed with Farrow interpolation and FFT algorithms. The third series of tests were carried out by applying a moving average pre-processing, instead. In both cases, tests were made with different sampling frequencies (and number of acquired samples, being the observation window Tw = 200 ms); filtering/decimation or moving average were set to obtain equivalent sampling frequencies of 16, 24, or 32 kHz at the end of the pre-processing stage.

For all test cases, measurements were caried out with both sinusoidal and distorted test waveforms. In the sinusoidal case the measurements were carried out to characterize the microcontroller acquisition system. In tests with harmonics, the measurements performed with both the NUCLEO board were compared with the NI9239 PC-based instrument and the Class A/I accuracy limits of the IEC 61000-4-7 standard. For each test, 1000 trials were repeated and errors (minimum, maximum and mean values) and 95th percentile intervals were evaluated.

6.1. Test condition (1): Results with sampling frequencies 16-24-32 kHz

The first series of tests was carried out with a basic setup; data were acquired with sampling frequencies of 16, 24, and 32 kHz) and no preprocessing was made before interpolation (with Farrow third order algorithm) and FFT analysis. To compensate for clock oscillations, if any, the observation window of 10 cycles was synchronized by means of a zero-crossing algorithm.

The results of the characterization tests with sinusoidal signals are summarized in Table 7. In comparison with the nominal specifications of the NUCLEO board ADC (12 bit), the characterization results showed a severe loss of resolution of data acquisition chain, due to both signal conditioning and data acquisition stages. The results of spectral analysis tests with harmonics are summarized in Table 8. In comparison with the preliminary tests results of Section IV, the tests with non-sinusoidal signals showed higher errors on harmonic amplitudes measurement, and no compliance with the IEC 61000-4-7 Class I limits with any sampling frequency. As an example, the results of errors and 95th percentile intervals on measured harmonics amplitudes are reported in Figs. 15, 16 and 17, for the test cases n. 19, 20 and 21, respectively. The plots of signal processing times (interpolation and FFT algorithms) measured with the oscilloscope are reported in Fig. 18 and Fig. 19, for the test cases n. 21 and n. 24, respectively. The processing time is feasible (about 21 ms and 42 ms, in the case of interpolation and FFT calculation with 2048 and 4096 samples, respectively). The same results would be obtained for the cases with lower sampling frequencies, since the interpolation algorithm and the FFT calculation only depend on the number of interpolated samples (2048 or 4096). The additional time needed for zero-crossing task was around 12 ms for highest sampling frequency of 32 kHz (which is the worst case among the considered sampling frequencies, due to the highest number of acquired samples in the observation window); even considering this further time, the results are promising for a gapless harmonic analysis; moreover, in the perspective of a real-time implementation, the zero crossing could be optimized to be executed during the sampling task. However the sampling frequency should be increased to match the accuracy requirements or different techniques should be used to improve the measurement accuracy (see next sections).

Table 8
Test condition (1) – Experimental results with harmonics – compliance with the standard limits.

Test case	*fs* [kHz]	N. of points after interpolation	Standard compliance on accuracy	Processing time
n.19	16	2048	Not verified	< 200 ms
n.20	24		Not verified	< 200 ms
n.21	32		Not verified	< 200 ms
n.22	16	4096	Not verified	< 200 ms
n.23	24		Not verified	< 200 ms
n.24	32		Not verified	< 200 ms

6.2. Test condition (2): Results with oversampling, digital filtering and decimation

The second series of tests were carried out by implementing an oversampling technique for data acquisition. Sampling frequencies were set to integer multiple values of 16, 24 and 32 kHz; after the zero-crossing task, further pre-processing of sampled data with digital filter and decimation was implemented, so to obtain equivalent sampling frequencies (and number of samples) equal to the values of the first series of tests, i.e.f_{s_eq} = 16–24-32 kHz (and N_{eq} = 3200–4800-6400 samples).

As known, this technique allows reducing the quantization noise in the frequency range of interest, so to obtain an improvement of resolution (see Fig. 20). In fact, the quantization noise amount depends on the acquisition system features and it is distributed all over the frequency range up to the Nyquist frequency; thus, the higher the sampling frequency, the lower the noise level; after filtering some noise is removed and with decimation the samples are reduced to obtain the desired equivalent sampling frequency and number of samples to be further processed [40,41]. From a theoretical viewpoint, with the respect to the sole ADC quantization error, to improve the resolution of n bits, an oversampling factor $k = 2^{2n}$ is needed. For example, with respect to an equivalent sampling frequency of 16 kHz, an improvement of 1, 2, or 3 bits of resolution require an oversampling factor of 4, 16, or 64 (i.e. sampling frequency of 64 kHz, 256 kHz or 1024 kHz), respectively.

The results of the characterization tests with sinusoidal signals are summarized in Table 9. The results show an improvement of the measured parameters, even if the results are worse than those theoretically expected, because of the presence of additional noise due to the signal conditioning stage.

The results of spectral analysis tests with harmonics are summarized in Table 10. In almost all cases the results of the tests with equivalent sampling frequency (after decimation) f_{s_eq} = 16 kHz are not in compliance with the IEC 61000-4-7 Class I limits. On the other hand,

Table 7
Test condition (1) – Characterization with sinusoidal signals.

Test case	*fs* [kHz]	N. of points after interpolation	SINAD [dB]	ENOB [bit]	THD [dB]	SFDR [dB]	Measured amplitude [V]
n.19	16	2048	43.87	7.0	−63.29	55.69	1.584
n.20	24		44.17	7.0	−65.05	62.21	1.584
n.21	32		45.14	7.2	−63.91	64.78	1.584
n.22	16	4096	45.02	7.2	−65.82	64.44	1.586
n.23	24		45.07	7.2	−64.91	65.29	1.584
n.24	32		44.88	7.1	−66.08	68.86	1.584

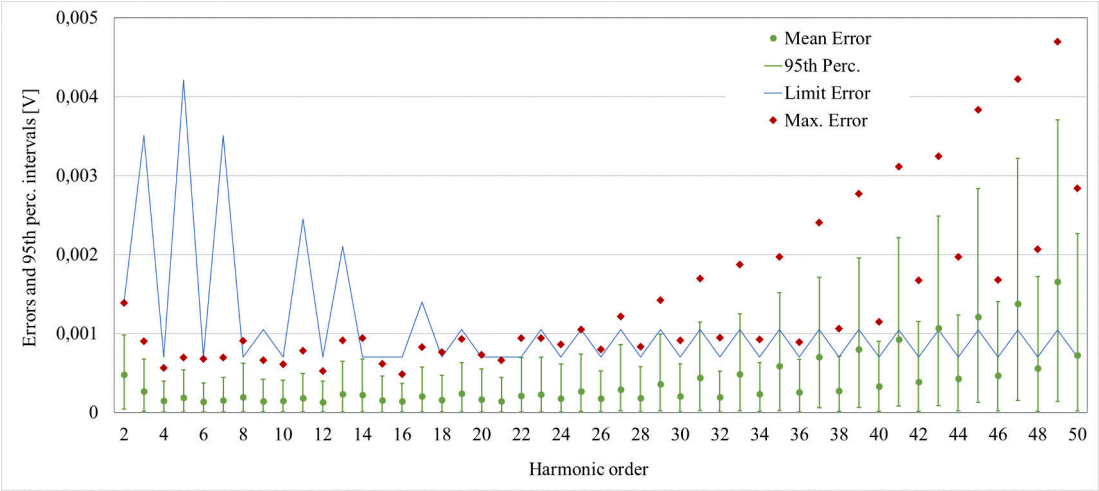


Fig. 15. Test condition (1), test case 19 (fs 16 kHz, 2048 points after interpolation). Errors and 95th percentile intervals of harmonic amplitudes measurements.

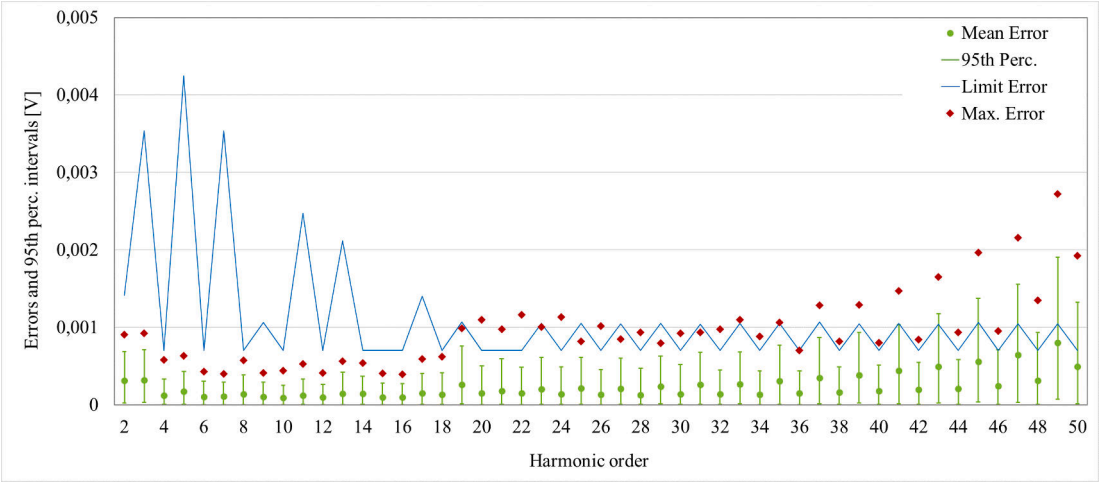


Fig. 16. Test condition (1), test case 20 (fs 24 kHz, 2048 points after interpolation). Errors and 95th percentile intervals of harmonic amplitudes measurements.

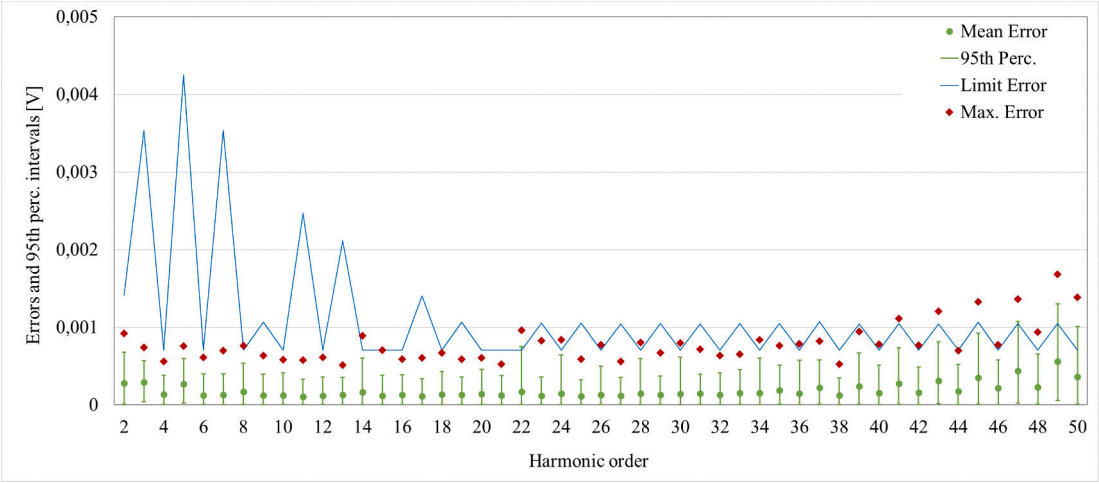


Fig. 17. Test condition (1), test case 21 (fs 32 kHz, 2048 points after interpolation). Errors and 95th percentile intervals of harmonic amplitudes measurements.

results with higher equivalent sampling frequency (after decimation), i. e. $f_{s\_eq} = 24$ kHz and, even more, $f_{s\_eq} = 32$ kHz are in compliance with the IEC 61000-4-7 Class I limits. As an example, the results of errors and 95th percentile intervals on measured harmonics amplitudes are reported in Fig. 21, for the test case n. 27. For the same test case, the plots of signal processing time (preprocessing – zero crossing, filtering and

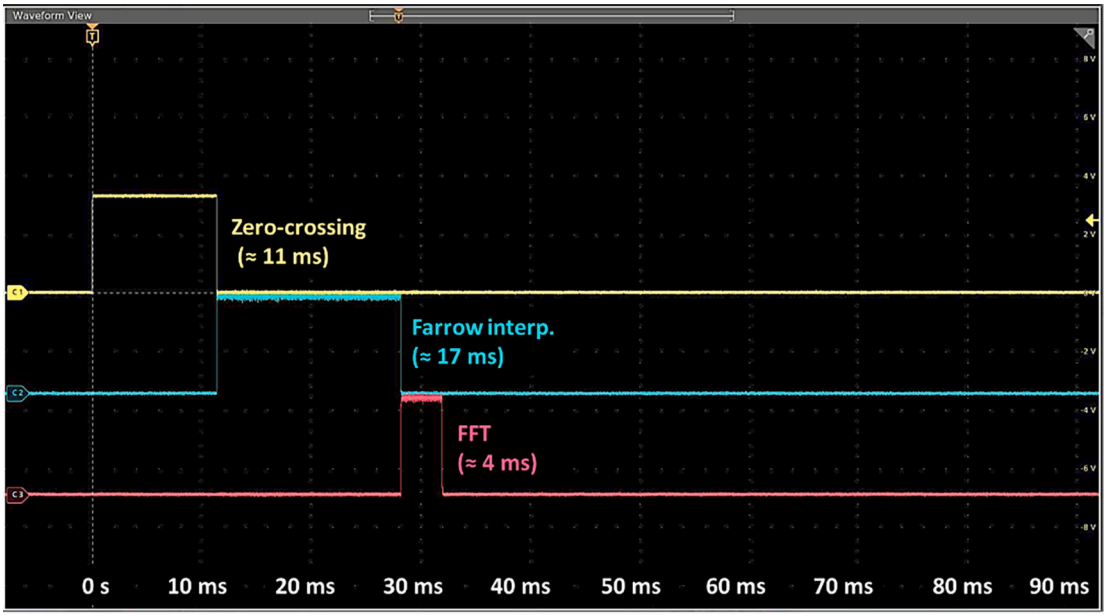


Fig. 18. Test condition (1), test case 21 (f_s = 32 kHz, 2048 points after interpolation). Measured times for signal processing.

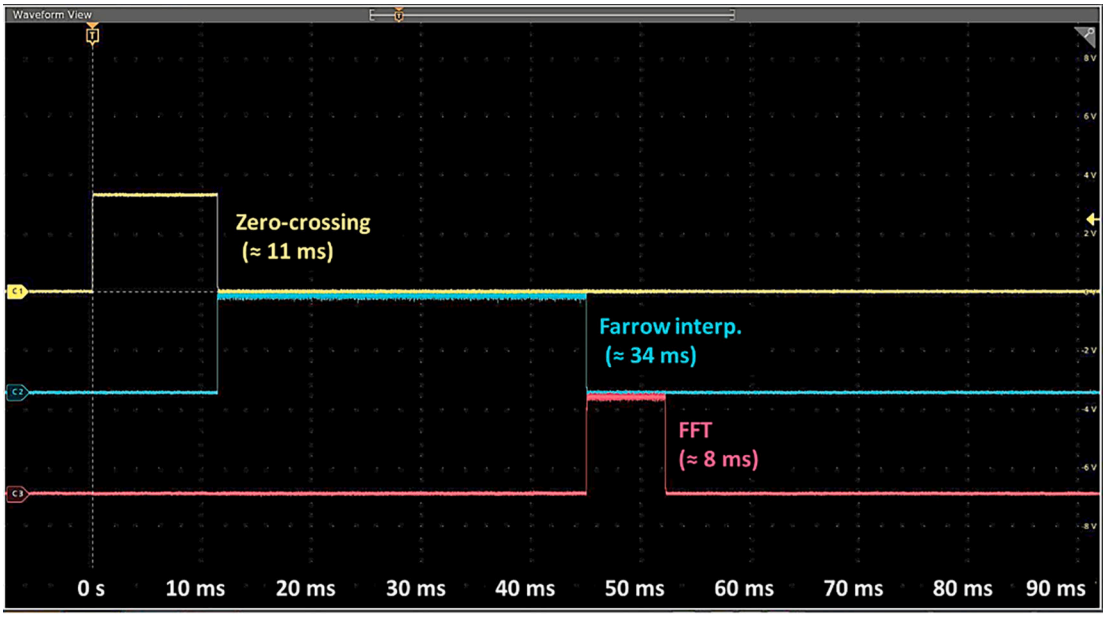


Fig. 19. Test condition (1), test case 24 (f_s = 32 kHz, 4096 points after interpolation). Measured times for signal processing.

decimation –, interpolation and FFT algorithms) measured with the oscilloscope are reported in Fig. 22. Filtering and decimation stage required an additional computation time of about 116 ms, which is predominant if compared with the time needed for executing both interpolation and FFT algorithms. The total time required for filtering, interpolation and FFT tasks was lower than 200 ms. However, if also zero-crossing is considered, the total processing time exceeds the limit of 200 ms. Similar results were found for tests with sampling frequencies up to 480 kHz; on the contrary, for higher sampling frequencies the aforesaid computational time was higher than 200 ms, thus it was not feasible for Class A gapless implementation, even considering the possibility of zero-crossing synchronization during the signal acquisition. Moreover, if compared with the previous test condition, the zero-crossing task required more time (about 100 ms in the best case of lowest oversampling frequencies), due to the higher number of acquired samples.

6.3. Test condition (3): Results with oversampling and moving average

The third series of tests was carried out by implementing a different oversampling technique. For each equivalent sampling frequency value (f_{s_eq} = 16, 24, 32 kHz), three NUCLEO board sampling frequencies were used, equal to 10 times, 20 times and 30 times f_{s_eq} and the average value was calculated over 10, 20 or 30 acquired samples, respectively. A schematic example of the implemented moving average technique (average over 10 samples) is showed in Fig. 23. This procedure allowed reducing the signal noise, with a lower computational cost, if compared with the previous case of filtering and decimation. As for the tests of previous section, after the moving average a new sequence of "average samples" was obtained, with equivalent sampling parameters equal to

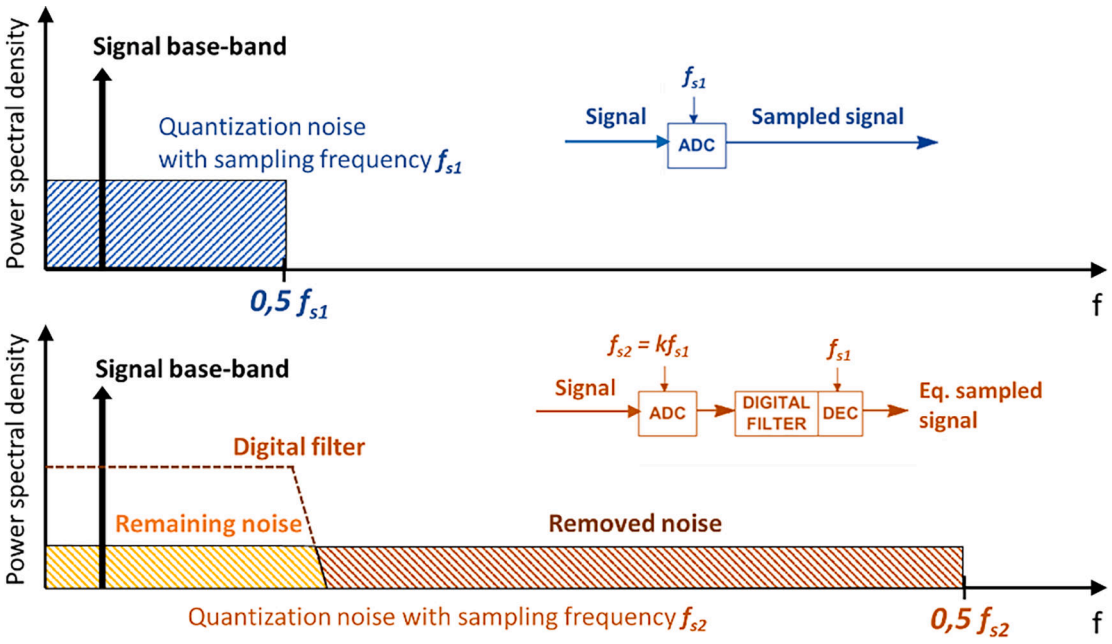


Fig. 20. Oversampling and digital filtering principle – quantization noise reduction.

Table 9
Test condition (2) – Characterization with sinusoidal signals.

Test case	*fs* [kHz]	*fs_eq* after decimation [kHz]	N. of points after interpolation	SINAD [dB]	ENOB [bit]	THD [dB]	SFDR [dB]	Meas. amplitude [V]
25	288	16	2048	49,32	7,9	−63,43	62,50	1,578
26		24		49,47	7,9	−63,19	65,22	1,578
27		32		53,12	8,5	−63,33	62,15	1,578
28		16	4096	51,50	8,3	−64,57	77,52	1,578
29		24		51,44	8,2	−64,55	68,46	1,578
30		32		51,89	9,3	−64,35	73,55	1,578
31	384	16	2048	48,45	7,8	−63,40	55,97	1,577
32		24		52,22	8,4	−62,76	59,48	1,577
33		32		50,39	8,1	−63,06	61,69	1,577
34		16	4096	53,93	8,7	−62,43	64,47	1,577
35		24		55,15	8,9	−62,92	78,55	1,577
36		32		55,63	8,9	−62,76	47,79	1,577
37	480	16	2048	49,19	7,9	−61,61	56,18	1,575
38		24		50,76	8,1	−62,25	59,38	1,575
39		32		51,32	8,2	−64,17	68,48	1,575
40		16	4096	48,15	7,7	−61,71	76,44	1,578
41		24		55,90	9.0	−62,19	68,65	1,575
42		32		49,33	7,9	−63,37	72,49	1,575
43	672	16	2048	49,90	7,5	−59,92	55,92	1,573
44		24		51,62	8,3	−59,72	65,59	1,573
45		32		48,20	7,7	−60,25	71,38	1,573
46		16	4096	54,68	8,8	−59,38	69,62	1,573
47		24		51,43	8,2	−60,24	74,63	1,573
48		32		54,89	8,8	−60,37	68,75	1,573
49	768	16	2048	48,86	7,8	−58,80	56,18	1,572
50		24		47,52	7,6	−57,40	59,57	1,572
51		32		51,57	8,3	−58,230	61,55	1,572
52		16	4096	52,77	8,5	−57,71	70,20	1,572
53		24		52,61	8,4	−57,75	78,40	1,572
54		32		54,34	8,7	−58,27	66,21	1,572
55	960	16	2048	47,52	7,6	−53,82	56,00	1,570
56		24		49,64	7,9	−53,83	74,94	1,570
57		32		47,75	7,6	−54,48	71,30	1,570

the values of the first series of tests, i.e.f_{s_eq} = 16–24-32 kHz and N_{eq} = 3200–4800-6400 samples. Then Farrow interpolation (to 2048 or 4096 points) and FFT were carried out to obtain the harmonics measurements.

The results of the characterization tests with sinusoidal signals are summarized in Table 11. In comparison with the first case (without oversampling), an improvement of the measured parameters was obtained, confirming the feasibility of moving average in reducing the signal noise and the compatibility with the results obtained by means of digital filtering and decimation.

The results of spectral analysis tests with harmonics are summarized

Table 10
Test condition (2) – Experimental results with harmonics – compliance with the standard limits (accuracy and processing time).

Case	*Fs* [kHz]	Equivalent *fs* after decimation [kHz]	N. of points after interpolation	Standard compliance on accuracy	Processing time(zero-crossing included)	Processing time(zero-crossing excluded)
n.25	288	16	2048	Not verified	> 200 ms	< 200 ms
n.26		24		Verified	> 200 ms	< 200 ms
n.27		32		Verified	> 200 ms	< 200 ms
n.28		16	4096	Not verified	> 200 ms	< 200 ms
n.29		24		Verified	> 200 ms	< 200 ms
n.30		32		Verified	> 200 ms	< 200 ms
n.31	384	16	2048	Not verified	> 200 ms	< 200 ms
n.32		24		Verified	> 200 ms	< 200 ms
n.33		32		Verified	> 200 ms	< 200 ms
n.34		16	4096	Not verified	> 200 ms	< 200 ms
n.35		24		Verified	> 200 ms	< 200 ms
n.36		32		Verified	> 200 ms	< 200 ms
n.37	480	16	2048	Not verified	> 200 ms	< 200 ms
n.38		24		Verified	> 200 ms	< 200 ms
n.39		32		Verified	> 200 ms	< 200 ms
n.40		16	4096	Not verified	> 200 ms	< 200 ms
n.41		24		Verified	> 200 ms	< 200 ms
n.42		32		Verified	> 200 ms	< 200 ms
n.43	672	16	2048	Not verified	> 200 ms	> 200 ms
n.44		24		Verified	> 200 ms	> 200 ms
n.45		32		Verified	> 200 ms	> 200 ms
n.46		16	4096	Not verified	> 200 ms	> 200 ms
n.47		24		Verified	> 200 ms	> 200 ms
n.48		32		Verified	> 200 ms	> 200 ms
n.49	768	16	2048	Not verified	> 200 ms	> 200 ms
n.50		24		Verified	> 200 ms	> 200 ms
n.51		32		Verified	> 200 ms	> 200 ms
n.52		16	4096	Not verified	> 200 ms	> 200 ms
n.53		24		Verified	> 200 ms	> 200 ms
n.54		32		Verified	> 200 ms	> 200 ms
n.55	960	16	2048	Not verified	> 200 ms	> 200 ms
n.56		24		Verified	> 200 ms	> 200 ms
n.57		32		Verified	> 200 ms	> 200 ms

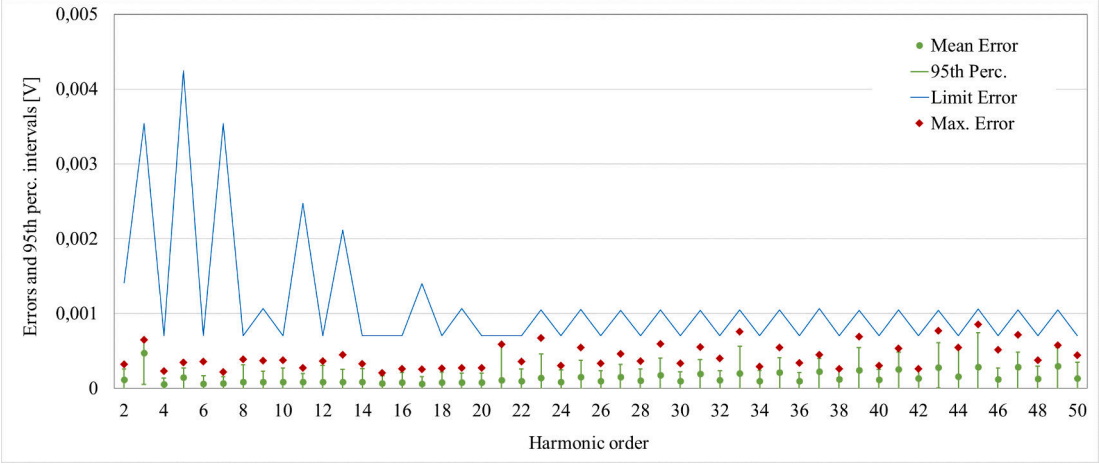


Fig. 21. Test condition (2), test case 27 (f_s = 288 kHz, f_{s_eq} = 32 kHz, 2048 points after interpolation). Errors and 95th percentile intervals of harmonic amplitudes measurements.

in Table 12. As for the previous case, the results of the tests with f_{s_eq} = 16 kHz (after average) were not in compliance with the IEC 61000–4-7 Class I limits for accuracy. On the other hand, results with higher equivalent sampling frequencies (after decimation), i.e. f_{s_eq} = 24 kHz and f_{s_eq} = 32 kHz fullfil the IEC 61000–4-7 Class I limits. As an example, the results of errors and 95th percentile intervals on measured harmonics amplitudes are reported in Fig. 24, for the test case n. 70. For the same test case, the plots of signal processing times (preprocessing – zero crossing and average –, interpolation and FFT algorithms) measured with the oscilloscope are reported in Fig. 25. As expected, the moving average computational time was significantly lower than the filtering (about 8 ms, vs. 116 ms for the case of Fig. 22), thus increasing the feasibility of gapless implementation [42]. The same results were obtained for all the other test cases, where the required time for average (excluding zero crossing) was comparable with that of interpolation and FFT computations. Considering also the zero-crossing task, the overall computational time was lower than 200 ms for tests with sampling frequencies lower than 480 kHz.

7. Conclusion

The work has investigated the feasibility of harmonic analysis

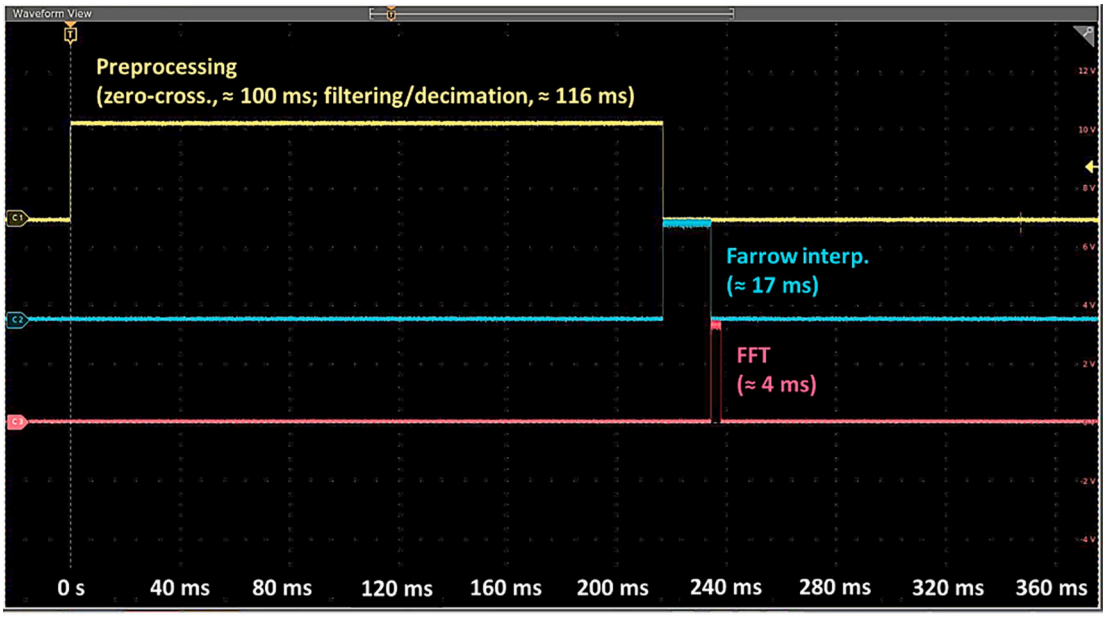


Fig. 22. Test condition (2), test case 27 (f_s = 288 kHz, f_{s_eq} = 32 kHz, 2048 points after interpolation). Measured times for signal processing.

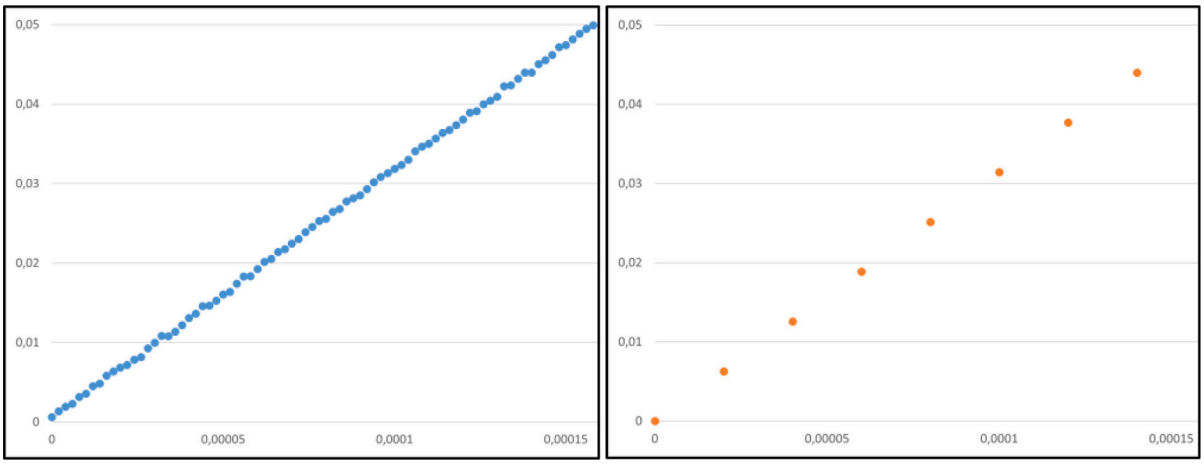


Fig. 23. Moving average technique. Example over 10 samples.

implementation on smart meter microcontroller devices, according to IEC 61000-4-30 Class A and IEC 61000-4-7 Class I requirements. An extended experimental characterization has been carried out on a case study device, aimed at analyzing its performances in terms of both measurement accuracy and computational burden. Different solutions have been tested, concerning sampling strategies, data acquisition and signal processing algorithms, in order to increase metrological ADC behavior and decrease computational cost.

As regards the spectral analysis, a focus has been made on time-domain interpolation algorithms for FFT efficient calculation. In detail, Farrow interpolation algorithm is proposed as valid alternative to Lagrange polynomial interpolation, thanks to its lower computational cost. The obtained results show the feasibility of the proposed algorithm. Moreover, the adoption of a time-domain interpolation technique allows gaining more flexibility in terms of sampling frequency and number of acquired samples and reaching a suitable tradeoff between accuracy requirements for spectral analysis, device memory, processing capabilities and computational burden.

The proposed algorithm has been implemented on the case study microcontroller board and several experimental tests have been carried out by using the on-board ADC for signal acquisition. Different sampling strategies have been tested, to identify a suitable solution for both data acquisition and processing, capable to comply with Standards requirements. The results of the experimental tests have shown that the metrological performances of the low-cost solution can be improved by implementing efficient sampling and processing strategies; in detail, the best results, in terms of both measurement accuracy and processing time, have been obtained by implementing an oversampling technique with a moving average for noise reduction. The obtained results demonstrate the feasibility of the spectral analysis implementation, with respect to both IEC 61000-4-7 class I accuracy and timing requirements.

CRediT authorship contribution statement

Giovanni Artale: Writing – review & editing, Validation, Supervision, Funding acquisition, Conceptualization. **Antonio Cataliotti:** Writing – review & editing, Validation, Supervision, Funding acquisition, Conceptualization. **Lionel Cimaz:** Validation, Supervision, Software, Methodology. **Valentina Cosentino:** Writing – review & editing, Validation, Supervision, Investigation, Funding acquisition, Conceptualization. **Dario Di Cara:** Writing – review & editing, Methodology, Investigation, Conceptualization. **Vito Ditta:** Writing – original draft,

Table 11
Test condition (3) – characterization with sinusoidal signals.

Test case	f_s [kHz]	Samples for average	N. of points after interpolation	f_{s_eq} after average [kHz]	SINAD [dB]	ENOB [bit]	THD [dB]	SFDR [dB]	Meas. amplitude [V]
58	160	10	2048	16	46.11	7.5	−65.84	69.99	1.583
59	320	20			48.07	7.8	−64.64	63.21	1.581
60	480	30			47.31	7.6	−63.11	65.65	1.578
61	160	10	4096		53.42	8.6	−66.61	98.55	1.583
62	320	20			55.54	8.9	−63.81	66.50	1.581
63	480	30			50.45	8.1	−62.00	71.43	1.579
64	240	10	2048	24	49.88	8.0	−66.17	63.77	1.581
65	480	20			46.99	7.5	−62.23	64.99	1.580
66	720	30			51.17	8.2	−60.37	65.77	1.577
67	240	10	4096		53.73	8.6	−63.67	72.69	1.581
68	480	20			56.34	9.1	−62.13	70.75	1.578
69	720	30			51.24	8.2	−60.51	72.88	1.576
70	320	10	2048	32	50.64	8.1	−65.28	67.96	1.581
71	640	20			50.74	8.1	−59.48	67.03	1.577
72	960	30			49.42	7.9	−59.90	64.13	1.573
73	320	10	4096		56.92	9.2	−65.14	70.59	1.581
74	640	20			53.47	8.6	−61.94	69.90	1.577
75	960	30			52.43	8.4	−60.41	73.55	1.579

Table 12
Test condition (3) – experimental results with harmonics – compliance with the standard limits (accuracy and processing time).

Case	fs [kHz]	Points for the mean value	fs equivalent after mean value [kHz]	N. of points after interpolation	Standard compliance on accuracy	Processing time(zero-crossing included)	Processing time(zero-crossing excluded)
n.58	160	10	16	2048	Not verified	< 200 ms	< 200 ms
n.59	320	20			Not verified	< 200 ms	< 200 ms
n.60	480	30			Not verified	< 200 ms	< 200 ms
n.61	160	10		4096	Not verified	< 200 ms	< 200 ms
n.62	320	20			Not verified	< 200 ms	< 200 ms
n.63	480	30			Not verified	< 200 ms	< 200 ms
n.64	240	10	24	2048	Verified	< 200 ms	< 200 ms
n.65	480	20			Verified	> 200 ms	< 200 ms
n.66	720	30			Verified	> 200 ms	< 200 ms
n.67	240	10		4096	Verified	< 200 ms	< 200 ms
n.68	480	20			Verified	> 200 ms	< 200 ms
n.69	720	30			Verified	> 200 ms	< 200 ms
n.70	320	10	32	2048	Verified	< 200 ms	< 200 ms
n.71	640	20			Verified	> 200 ms	< 200 ms
n.72	960	30			Verified	> 200 ms	< 200 ms
n.73	320	10		4096	Verified	< 200 ms	< 200 ms
n.74	640	20			Verified	> 200 ms	< 200 ms
n.75	960	30			Verified	> 200 ms	< 200 ms

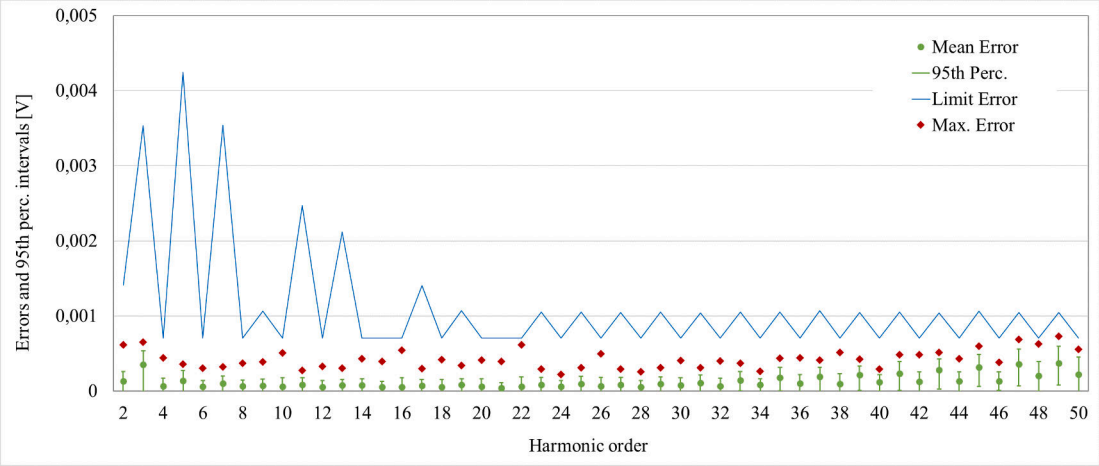


Fig. 24. Test condition (3), test case 70 (fs = 320 kHz, fs_eq = 32 kHz, 2048 points after interpolation). Errors and 95th percentile intervals of harmonic amplitudes measurements.

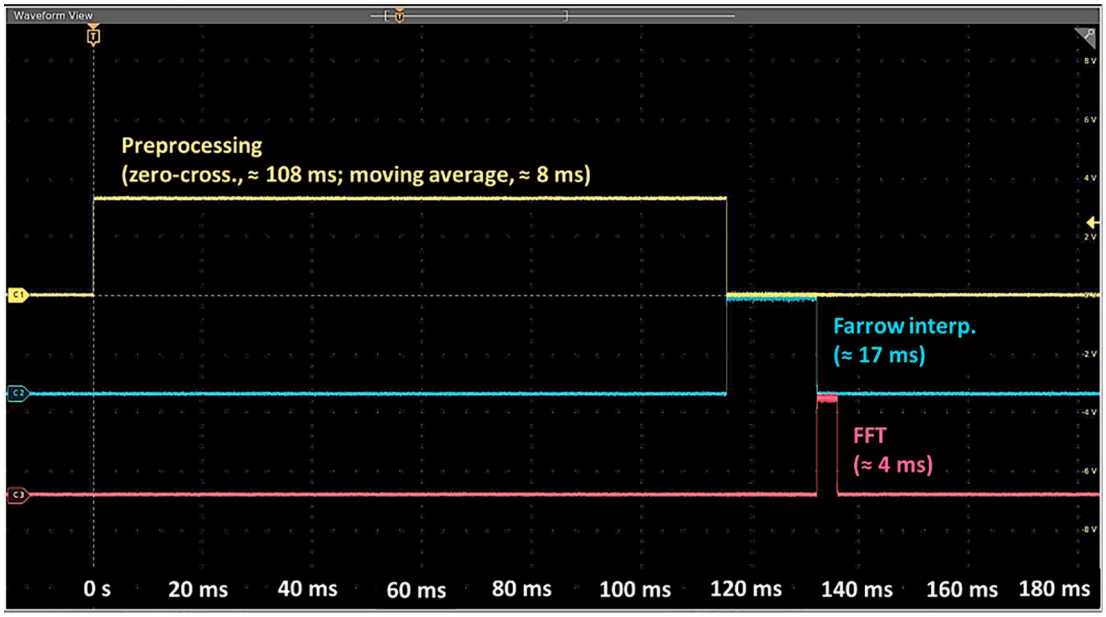


Fig. 25. Test condition (3), test case 70 (f_s = 320 kHz, f_{s_eq} = 32 kHz, 2048 points after interpolation). Measured times for signal processing.

Software, Methodology, Investigation, Formal analysis, Data curation. **Nunzio Dipaola:** Writing – review & editing, Validation, Supervision, Funding acquisition, Conceptualization. **Salvatore Guaiana:** Software, Methodology, Investigation, Data curation. **Nicola Panzavecchia:** Software, Methodology, Investigation, Data curation. **Marilena Sambataro:** Validation, Supervision, Funding acquisition, Conceptualization. **Giovanni Tinè:** Writing – review & editing, Validation, Supervision, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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