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Characteristics of Vertical Transistors on a GaN Substrate Fabricated via Na-Flux Method and Enlargement of the Substrate Surpassing 6 Inches

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The Na-flux method is expected to be a key GaN growth technique for obtaining ideal bulk GaN crystals. Herein, the structural quality of the latest GaN crystals grown using the Na-flux method and, for the first time, the characteristics of a vertical transistor fabricated on a GaN substrate grown using this method are discussed. Vertical transistors exhibit normally off operation with a gate voltage threshold exceeding 2 V and a maximum drain current of 3.3 A during the on-state operation. Additionally, it demonstrates a breakdown voltage exceeding 600 V and a low leakage current during off-state operation. It is also described that the variation in the on-resistance can be minimized using GaN substrates with minimal off-angle variations. This is crucial for achieving the large-current chips required for future demonstration of actual devices. In addition, the reverse *I–V* characteristics of the parasitic p–n junction diode (PND) structures indicate a reduction in the number of devices with a significant leakage current compared to commercially available GaN substrates. Finally, a circular GaN substrate with a diameter of 161 mm, surpassing 6 inches, grown using the Na-flux method is demonstrated, making it the largest GaN substrate aside from those produced through the tiling technique.

1. Introduction

In recent years, as society demands carbon neutrality, gallium nitride (GaN)-based semiconductor devices, along with silicon carbide (SiC) devices, have attracted attention as energy-saving devices that contribute to carbon neutrality because of their ability to reduce power loss during high power conversion.[1] The dominant platform for developing commercial GaN power electronic devices is based on lateral AlGaN/GaN structures grown on large, low-cost silicon substrates.[2] Lateral GaN devices can utilize high-mobility two-dimensional electron gas (2DEG), thereby effectively reducing the on-state resistance. However, those lateral GaN devices exhibit low threshold voltages owing to the use of 2DEG and have certain limitations in the breakdown voltage and output power of the switching systems because of the lateral device configuration. Therefore, vertical GaN transistors fabricated on bulk GaN substrates are expected to overcome the limitations of lateral devices.[3–6]

However, commercially available GaN substrates are expensive and exhibit low crystalline quality because of their high threading dislocation densities (TDDs) of $\approx 10^6$ cm^{-2} and large off-angle variations due to the bowing of the crystal plane. These threading dislocations (TDs) are thought to generate a leakage current, particularly in vertical structures,[7] and some types of TDs have been reported to contribute to the increased

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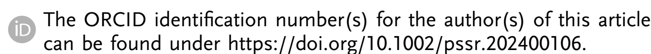
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leakage current in Schottky barrier diodes and p–n junction diodes (PNDs).[8,9] Recently, TDs with screw components have been found to act as significant leakage pathways in response to excitation during continuous forward current stress trials in GaN PNDs.[10] To reduce these TDDs, several techniques for promoting the fusion and annihilation reactions of TDs, such as thick film growth through hardness control,[11] epitaxial lateral overgrowth (ELO)-based growth,[12–14] and maskless three-dimensional (3D) growth,[15] have been proposed in the hydride vapor phase epitaxy (HVPE) method, resulting in reported reductions of TDD on the order of 10^4–10^5 cm^{-2}. Regarding crystal bowing, it has been reported that crystals with a lattice curvature radius of ≈50 m are obtained by maskless 3D growth, and the off-angle variation is suppressed to within 0.05° in a 2 inch plane.[15] Repeated 3D growth has also yielded crystals with a lattice curvature radius of 215 m. The off-angle variation estimated from the radius is reported to be less than 0.01°.

With the oxide vapor phase epitaxy (OVPE) method,[16] the basic ammonothermal method,[17,18] and the acidic ammonothermal method,[19] growth of GaN crystals with a dislocation density of the order of 10^4–10^5 cm^{-2} has also been reported. In the ammonothermal method, GaN crystals with minimal bowing are obtained, and the off-angle variation was reported to be within 0.03° in a 60 × 60 mm area.[19]

To realize low-cost GaN substrates, large-diameter and thick GaN ingots such as silicon ingots are necessary. Currently, 4 inch diameter GaN substrates fabricated by HVPE are commercially available, and it has been reported that 6 inch GaN crystals can be obtained using HVPE,[11] while 7 inch GaN substrates can be obtained by tiling 2 inch GaN substrates.[20] For thick film growth, thicknesses greater than 5 mm have also been reported using the HVPE method.[11,21] The simultaneous growth of large quantities of GaN crystals achieved using the ammonothermal method is also beneficial for reducing fabrication costs.

Among these methods, the Na-flux method has also attracted attention as a means of obtaining large-diameter, low-dislocation, and low-curvature GaN crystals. In a recent Na-flux method, a substrate featuring numerous dots of GaN crystals selectively grown on sapphire, known as a multi-point seed (MPS) substrate, was used as the seed. This is known as the MPS technique.[22] In this technique, hexagonal pyramidal GaN crystals grown from individual point seeds (PS) coalesce to obtain a single crystal. In principle, the diameter of the grown crystals is determined by the diameter of the MPS substrate, making it relatively easy to achieve large-diameter crystals. In contrast, {10-11} and {10-12} plane growth, which easily incorporates oxygen impurities, was reported to become dominant, and both the blackening of crystals and the expansion of lattice constants were observed.[23] Therefore, we developed a flux-film-coated (FFC) technique to promote the lateral growth and coalescence of GaN crystals by pulling the substrate up from the melt and using the residual melt between the crystals.[24] The development history of the Na-flux method is summarized in our previous paper.[25] By using this technique, we succeed in obtaining highly transparent crystals larger than 3 inches.[26] We previously reported that the typical TDD and lattice curvature radius of GaN substrates grown by the Na-flux method are on the order of 10^4–10^5 cm^{-2} and ≈30 m, respectively.[24,26] In this article, we report on the quality of the latest GaN crystals obtained by combining the MPS and FFC techniques in the Na-flux method.

As mentioned earlier, most reports related to the Na-flux method have dealt with the crystal quality; few have characterized GaN devices. While the current–voltage (I–V) characteristics of PNDs fabricated on GaN substrates grown using the Na-flux method have been reported,[3,7] there have been no reports on vertical transistors on GaN substrates. Therefore, in this article, we report, for the first time, the characteristics of a vertical transistor with the structure proposed by Shibata et al.[5] fabricated on a GaN substrate grown using the Na-flux method.

Finally, we report on efforts to further increase the diameter of GaN substrates using the Na-flux method. It has been reported that a hexagonal GaN crystal with a diagonal length of 96 mm and an inscribed circle diameter of φ78 mm was obtained from a 4 inch diameter MPS substrate by grown using the FFC growth techniques described earlier.[26] Recently, we fabricated an 8 inch diameter MPS substrate and succeeded in growing hexagonal GaN crystals with a diagonal length of just under 8 inches on the new MPS substrate. We also successfully hollowed out circular GaN wafers with a diameter of 161 mm, over 6 inches, which is the largest GaN substrate aside from those produced through the tiling technique.

2. GaN Crystal Growth by Na-Flux Method

The MPS-GaN substrate was produced through the selective growth of dot-shaped and 5 μm thick *c*-plane GaN crystals, called point seeds, grown by metal organic vapor phase epitaxy (MOVPE) on a 3 inch diameter (0001) sapphire substrate. The point seeds were arranged in a triangular grid so that the coalescence direction of the grown crystals corresponded to the a-direction of the GaN. Crystal growth was performed using the FFC technique to promote the coalescence of GaN crystals grown from point seeds and form a *c*-plane across the surface. Although details of the conditions have been reported previously,[24] the growth conditions have been further optimized in the present study to reduce the lattice curvature and dislocation density.

Figure 1a shows photographs of the as-grown GaN crystal, which separated naturally from the MPS-GaN substrate after immersion in cold ethanol and water to dissolve the residual flux. Thus, it seems that the crystal separated during the cooling process after growth owing to the thermal stress originating from the difference in the coefficients of thermal expansion between sapphire and GaN. The diameter of the grown crystal was almost 3 inches, and the surface appeared mirror-like because it was composed of a flat *c*-plane. In contrast, the crystal appeared to be colored due to the initial growth layer composed of {10-11} growth sectors, showing a black color caused by the incorporation of high-density oxygen impurities.[23,24] Therefore, after these sectors were eliminated by back grinding and a chemical mechanical polishing (CMP) process carried out on both the surface and backside, only the *c*-plane sector at the latter growth layer remained in the GaN wafer, which appeared highly transparent, as shown in Figure 1b. The diameter of the wafer was set to φ60 mm so that a 2 inch GaN wafer could be obtained even if the diameter became smaller in the subsequent process of HVPE growth.

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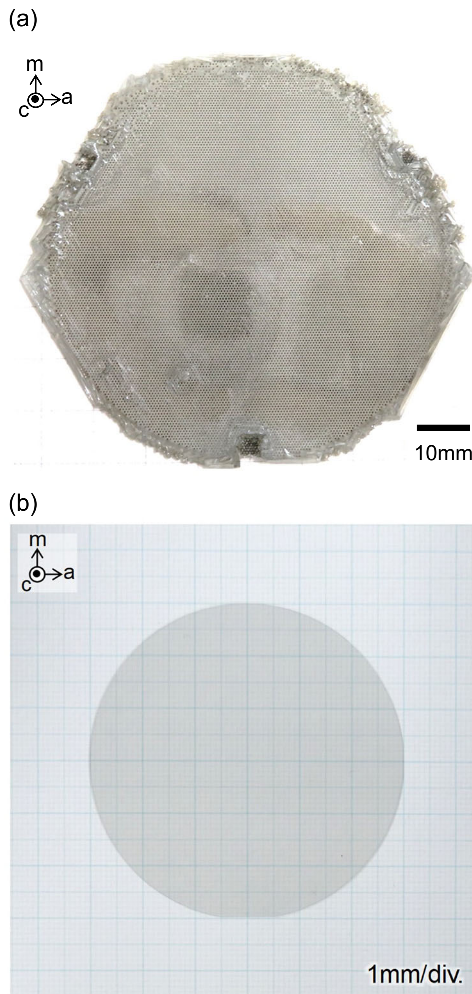

Figure 1. a) Photograph of the freestanding GaN crystal grown on MPS-GaN substrate and b) the GaN wafer after the initial growth layer was eliminated by back grinding and a chemical mechanical polishing (CMP) process carried out on both surface and backside.

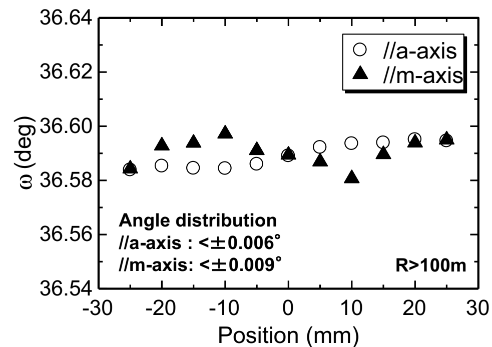

Figure 2. Dependence of peak top angle of GaN 0004 ω-scan XRCs on measurement position.

The lattice curvature radius of the GaN wafer was measured from a shift in the peak top angle of GaN 0004 ω-scan X-ray rocking curve (XRC) profiles. Taking 11 points in 5 mm steps (50 mm range), measurements were performed along the incident X-ray directions parallel to the a-axis (//a-axis) and m-axis (//m-axis). Maximum shift based on center peak angle, i.e., angle distribution, were less than ±0.006° for //a-axis and ±0.009° for //m-axis, as shown in **Figure 2**. The lattice curvature radius calculated from the peak shifts was greater than 100 m in both directions.

The TDD and behavior of the individual threading dislocations in the wafers were measured using multi-photon excitation photoluminescence (MPPL), in which an in-plane image at each focal depth is obtained by varying the focal depth.[27] Since the TDD was estimated to be high around the coalescence region of the GaN crystals, we focused on the regions where a single GaN crystal was surrounded by six GaN crystals grown from point seeds, as illustrated in **Figure 3**a. MPPL images were captured at two depths: above and below the depth at which the crystals completely coalesced and the surface was completely composed of the *c*-plane, as illustrated in the schematic drawing of the cross section in Figure 3b. Figure 3c shows a 750 µm square MPPL image at the deeper level obtained by 3 × 3 mapping of 250-µm-square MPPL images, Figure 3d shows that at the shallow level (surface side) obtained by 3 × 3 mapping of 250-µm-square MPPL images in which TDD values were described, while Figure 3e shows the magnified image of one of the 250 µm square MPPL images. As shown in Figure 3a and c, voids are present at deeper levels in the region surrounded by the three GaN crystals and located at both ends of the coalescence boundary of the GaN crystals. We previously reported that a high density of TDs exceeding 10^6 cm^{-2} appears at the region above voids, whereas the TDD decreases to the order of 10^5 cm^{-2} during thick growth, resulting in an overall in-plane dislocation density ranging from 10^4 to 10^5 cm^{-2} order.[26] In contrast, with the optimized growth conditions used in the present study, TDD was successfully reduced to the order of 10^3 to 10^4 cm^{-2} even above the region on voids, as shown in Figure 3d. The crystals showed a slight distribution of the TDD, with the TDD being relatively high above the voids formed by the coalescence of the three GaN crystals. Details of the optimized conditions will be reported in future research. Since there remain areas with TDD of the order of 10^5 cm^{-2} in some regions on the voids in the crystal plane, we are investigating ways to improve uniformity so that the TDD becomes of the order of 10^3 to 10^4 cm^{-2} over the entire crystal.

3. Characteristics of Vertical Transistors on a Na-Flux-Based HVPE-GaN Substrate

In this section, we describe the characteristics of the vertical transistors fabricated on GaN substrates obtained by HVPE growth on GaN crystals fabricated using the Na-flux method as seed crystals, which are referred to as Na-flux-based HVPE-GaN substrates. In the Na-flux method, GaN crystals are undoped and the substrate exhibits high electrical resistance due to the low carrier concentration of about 2×10^{16} – 3×10^{16} cm^{-3}. In addition, it is difficult to form ohmic electrodes on the rear side of the GaN substrate. Therefore, we fabricated a GaN substrate with a carrier concentration of about 2×10^{18} – 3×10^{18} cm^{-3} by Si-doped HVPE growth on the seed crystal

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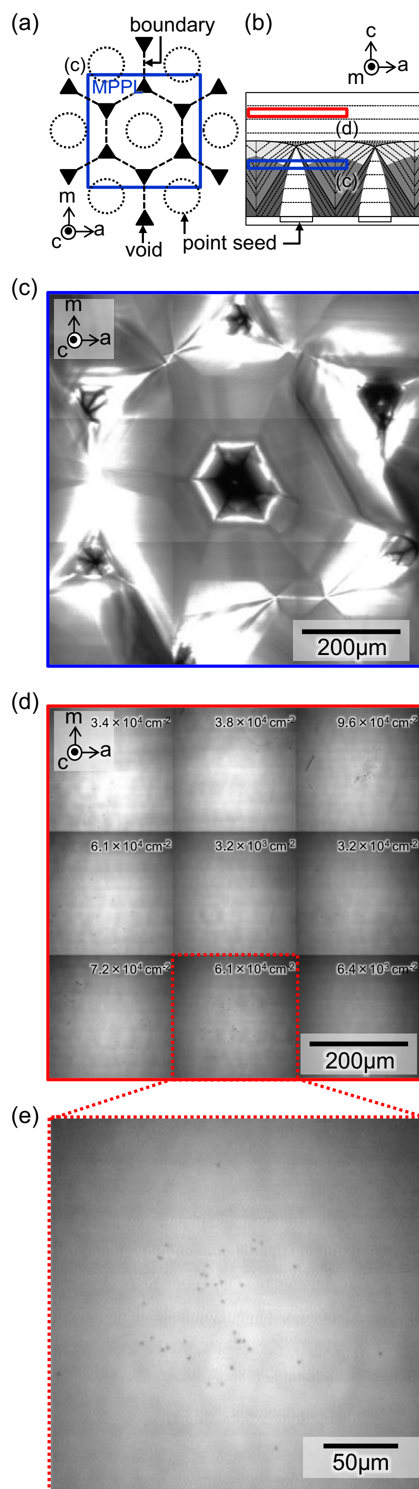

Figure 3. Schematic drawings of a) the region for MPPL observation, where a single GaN crystal is surrounded by six GaN crystals grown from point seeds, and b) the cross section showing observation areas at two depths. c) The 750 μm square MPPL image at the deeper level obtained by 3 × 3 mapping of 250 μm square MPPL images, d) shows that at the shallow level (surface side) obtained by 3 × 3 mapping of 250 μm square MPPL images in which TDD values were described, and e) shows the magnified image of one of the 250 μm square MPPL images.

grown by the Na-flux method. While the Na-flux method can grow GaN crystals with large diameter, low lattice curvature, and low TDD, the growth rate is slow at about 20 $\mu m\,h^{-1}$, which is insufficient for thick GaN growth. Therefore, to facilitate mass production and thereby reduce costs, we are working on achieving high-speed and thick growth using HVPE.[20,23]

Figure 4a shows a photograph of a 2 inch GaN wafer obtained by removing the seed crystal grown using the Na-flux method on the back surface after the HVPE growth and the polishing of the front and back surfaces. Figure 4b shows a photograph of the GaN wafer after the vertical transistors were formed. In this study, vertical transistors were fabricated on two types of commercially available HVPE-GaN substrates with different dislocation densities, in addition to a Na-flux-based HVPE-GaN substrate, and their characteristics were compared. **Table 1** lists the TDD, off-angle in the a-axis direction at the center position, and the maximum and minimum in-plane off-angle variations for these GaN substrates. The off-angle in the m-axis direction at the center position was set at ≈0°. The off-angle variation is related to the lattice curvature of the GaN substrate,[15,20] and the variation in the Na-flux-based HVPE-GaN substrate used for the vertical transistors was smaller than that of commercially available HVPE-GaN substrates.

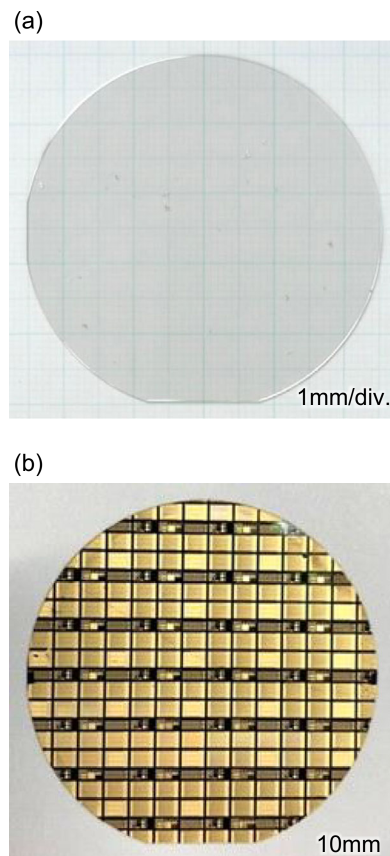

Figure 4. a) Photograph of the 2 inch GaN wafer obtained by removing the seed crystal grown by the Na-flux method on the back surface after the HVPE growth and polishing the front and back surfaces, referred to as Na-flux-based HVPE-GaN substrate, and b) the GaN wafer after vertical transistors were formed.

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Table 1. TDD and off-angle values of GaN substrates.

Substrate	TDD [cm^{-2}]	Off-angle in the a-axis direction [°]		
		Min	Center	Max
Commercially available HVPE-GaN substrate	$2 \times 10^6 - 3 \times 10^6$	0.21	0.40	0.57
Commercially available low TDD HVPE-GaN substrate	$5 \times 10^5 - 6 \times 10^5$	–	–	–
Na-flux-grown GaN base HVPE-GaN substrate	$1 \times 10^5 - 4 \times 10^5$	0.33	0.41	0.50

Figure 5a shows the cross-sectional structure of a vertical GaN-based transistor on a GaN substrate. The transistor features epitaxially re-grown p-GaN gate/AlGaN/GaN triple layers formed over the V-grooves at the surface of p-GaN well (0.3 μm, Mg: 3×10^{19} cm^{-3})/n-GaN drift layers (7 μm, carrier concentration: 1.3×10^{16} cm^{-3}). The use of triple layers at the side wall of the V-grooves enables the lifting of the potential of the 2DEG channel at the AlGaN/GaN heterojunction, as indicated by the red dashed line, making it easy to achieve normally off characteristics, which is important for power devices. Other structural features have been described in previous research.[5] The wafer-calibrated device area was 0.27 mm^2 and cathodes were formed on top of the mesas dug into the p-GaN well. Mesa etching was performed into the n-GaN drift layers. On the other hand, this transistor had a parasitic vertical PND structure between the source and drain electrodes in the area enclosed by the blue dashed line in Figure 5b. The wafer-calibrated device area was 0.9 mm^2 and the source electrodes were formed on top of the mesas dug into the p-GaN layers. Mesa etching was performed into the n-GaN drift layers. The larger the leakage current of this vertical PND, the larger is the leakage during the off state of the vertical transistor. Therefore, we evaluated the reverse *I–V* characteristics of PNDs formed simultaneously with a vertical GaN transistor on the Na-flux-based HVPE-GaN substrate and compared them with those of commercially available low-TDD HVPE-GaN substrates. Because the PNDs were fabricated on the same wafer as the vertical GaN transistor, the crystal growth and device process history, including dry etching, were the same as those of the transistor.

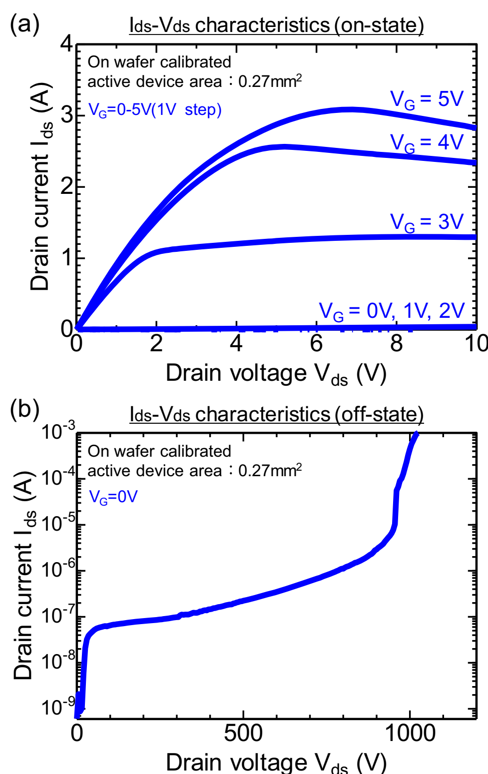

Figure 6. a) On-state and b) off-state drain–source current (I_{ds}) – drain–source voltage (V_{ds}) characteristics of a vertical transistor fabricated on the Na-flux-based HVPE-GaN substrate.

Figure 6a and b show the on- and off-state drain–source current (I_{ds}) – drain–source voltage (V_{ds}) characteristics, respectively, of a vertical transistor fabricated on the Na-flux-based HVPE-GaN substrate. A normally off operation with a gate-voltage threshold over 2 V and a maximum drain current of 3.3 A (current density: 1.2 kA cm^{-2}) was confirmed from the on-state characteristics, indicating the successful creation of

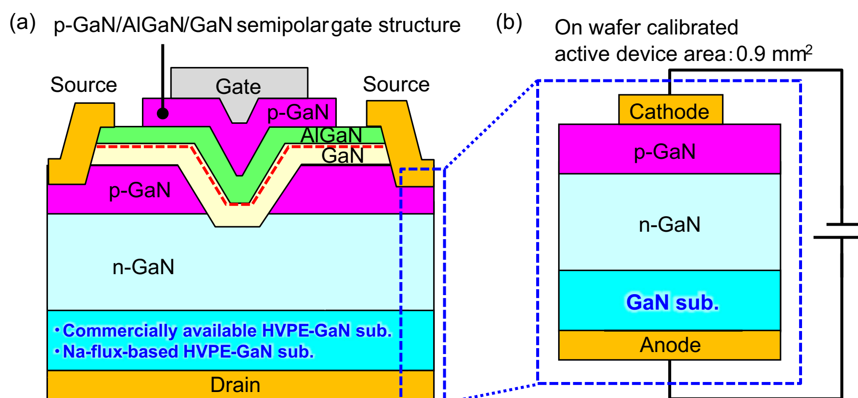

Figure 5. a) Cross-sectional structure of a vertical GaN based transistor on GaN substrates and b) parasitic vertical PND structure between the source and drain electrodes in the transistor.

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the first vertical GaN transistor operation on a GaN substrate produced through the Na-flux method. While the transistor was driven in the ampere class during the on-state operation, a breakdown voltage of over 600 V was confirmed from the off-state characteristics, and a low leakage current was realized. The breakdown voltage is considered to exhibit the voltage defined by the drift layer thickness of 7 μm and does not differ between a Na-flux-based HVPE-GaN substrate and a commercially available HVPE-GaN substrate.

Figure 7a shows the effective carrier densities in the drift layer of a vertical transistor on a Na-flux-based HVPE-GaN substrate and a commercially available HVPE-GaN substrate, which were estimated from the capacitance–voltage (C–V) measurements of the parasitic PND structures at 19 points in the plane. The variation of effective carrier density was $1.15 \times 10^{16} - 1.53 \times 10^{16}$ cm^{-3} for the Na-flux-based HVPE-GaN substrate, which was suppressed compared to $8.83 \times 10^{15} - 1.55 \times 10^{16}$ cm^{-3} for the commercially available HVPE-GaN substrate. This was attributed to the smaller in-plane off-angle variation of the Na-flux-based HVPE-GaN substrate, as shown in Table 1. The concentration of carbon unintentionally incorporated into the drift layer depends on the substrate off-angle, as previously reported,[28–30] and the incorporated carbon affects the effective carrier density because it activates as an acceptor. When the in-plane off-angle variation of the substrate is small, the variation in the incorporated carbon concentration is also small, resulting in a reduction in the variation in the effective carrier density, as described earlier.

Figure 7b shows the on-resistance values of the vertical transistors measured at 17 in-plane points. The on-resistance variation was 1.01–1.19 Ω for the Na-flux-based HVPE-GaN substrate, while that was 1.17–1.86 Ω for the commercially available HVPE-GaN substrate. The on-resistance variation was confirmed to be reduced by suppressing the variation in the effective carrier density. Suppressing variations in device characteristics is extremely important for obtaining large-current chips required for future applications in actual devices. Thus, the advantages of using GaN substrates with large lattice curvature radius and small off-angle variations were confirmed.

Figure 8a shows a photograph of the Na-flux-based HVPE-GaN substrate with a lattice curvature radius as large as 57 m (after freestanding the HVPE layer), which was recently obtained

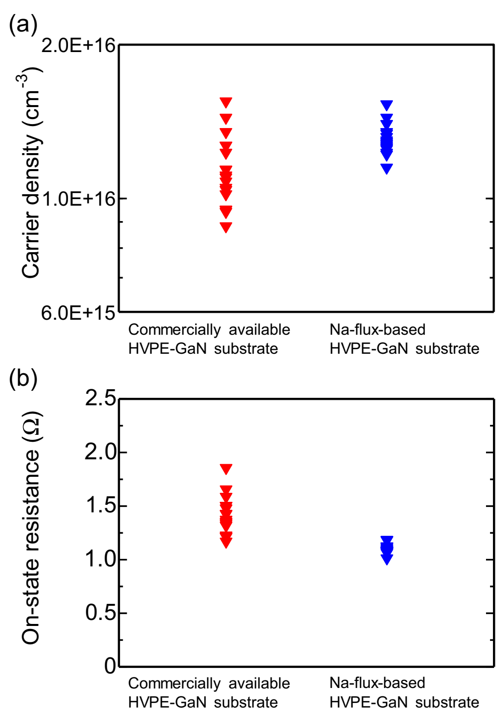

Figure 7. a) Effective carrier densities in the drift layer and b) the on-resistance values of vertical transistors fabricated on Na-flux-based HVPE-GaN substrate and commercially available HVPE-GaN substrate.

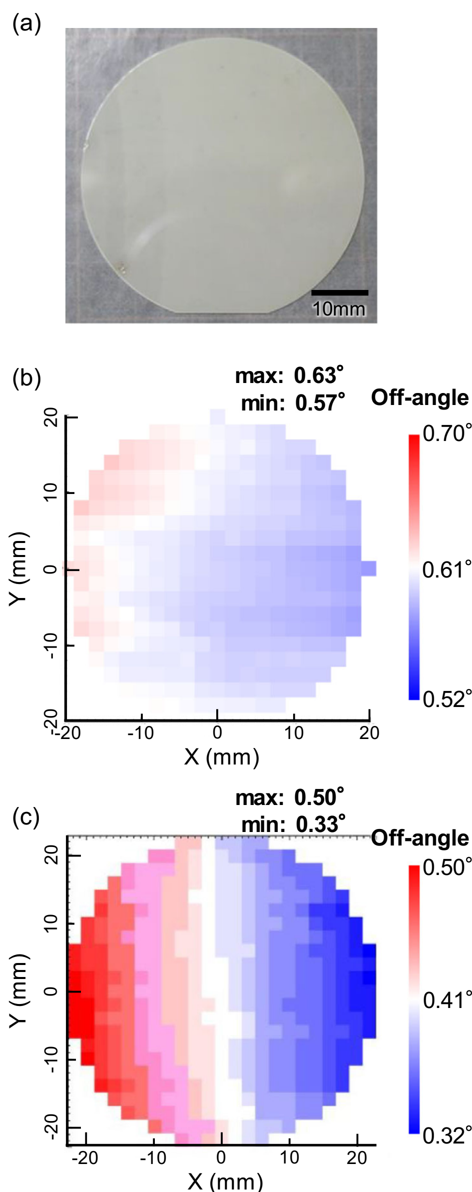

Figure 8. a) Photograph of a newly obtained Na-flux-based HVPE-GaN substrate with a lattice curvature radius as large as 57 m and b) the off-angle variation of the substrate with c) that of Na-flux-based HVPE-GaN substrate on which the vertical transistor was fabricated in this study for comparison.

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through HVPE growth with optimized conditions on a seed crystal having an even larger lattice curvature radius grown by the Na-flux method. The off-angle variation of the substrate was evaluated by X-ray diffraction (XRD) measurements. The center off-angle measured was 0.60° and the off-angle variation was within ±0.03°, as shown in Figure 8b, which was further reduced compared to the off-angle variation within ±0.09° of the Na-flux-based HVPE-GaN substrate on which the vertical transistor was fabricated, as shown in Figure 8c. It is expected that the fabrication of vertical transistors on GaN substrates with smaller off-angle variations will further reduce on-resistance variation in the future.

Figure 9a and b show the reverse *I*–*V* characteristics measured in 18 PNDs with the structure illustrated in Figure 5b, on the Na-flux-based HVPE-GaN substrate and the commercially available low-dislocation GaN substrate, respectively. The jumps observed in some curves may be due to breakdowns in the electrodes formed on the pits. Whether the formation of these pits is due to the epitaxial growth conditions or substrate defects is currently under investigation. The number of PNDs with a large leakage current was suppressed in the Na-flux-based HVPE-GaN substrate compared to that in the commercially available low-dislocation GaN substrate. In the criterion where PNDs available without problems must meet the characteristics of leakage current less than 1 μA at an applied voltage of 600 V and a breakdown voltage higher than 800 V (indicated by the blue curves in Figure 9a and red curves in Figure 9b), a significant improvement was confirmed. The yield of the Na-flux-based HVPE-GaN substrate was 72% (13/18), compared 33% (6/18) for the commercially available low-dislocation GaN substrate. In contrast, when evaluating the reverse *I*–*V* characteristics of simple PNDs fabricated on commercially available HVPE GaN substrates that were not exposed to the fabrication process of vertical transistors, the estimated yield was ≈80%. Thus, the reason for the low yield of parasitic PNDs on commercially available low-dislocation GaN substrates is assumed to be the generation of new defects during the vertical transistor fabrication process (i.e., dry etching and regrowth). In contrast, the yield was maintained for the Na-flux-based HVPE-GaN substrate. Few defects in the substrate would create new defects during the fabrication process of vertical transistors, leading to a high yield. The origin of PND leakage after the fabrication process history of vertical transistors is currently under investigation.

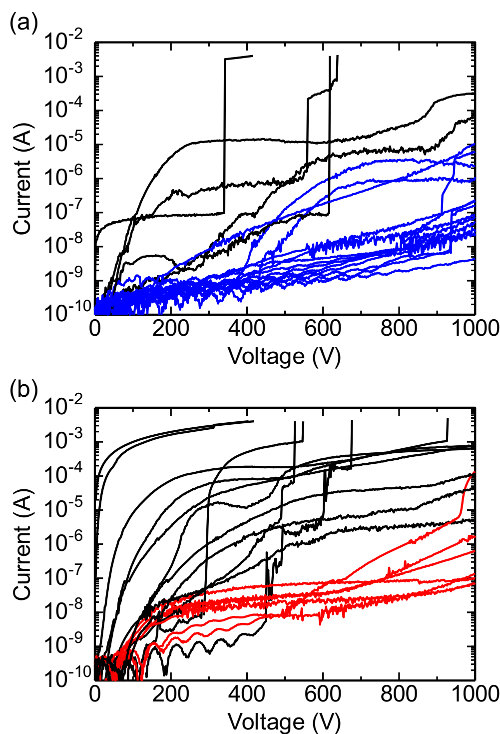

Figure 9. Reverse *I*–*V* characteristics measured in 18 PNDs on a) the Na-flux-based HVPE-GaN substrate and b) the commercially available low-TDD GaN substrate. The *I*–*V* characteristics indicated by the blue curves in Figure 9a and red curves in Figure 9b meet leakage current less than 1 μA at an applied voltage of 600 V and a breakdown voltage higher than 800 V.

4. Enlargement of GaN Wafer Diameter by Na-Flux Method

As mentioned earlier, low-dislocation and low-lattice-curvature GaN wafers have been successfully produced using the MPS and FFC techniques. On the other hand, to increase the diameter of the GaN wafer further, a larger-diameter MPS substrate is required. Since a φ3-inch MPS substrate was used to obtain φ60 mm GaN crystals, a φ8 inch MPS substrate was needed to obtain a GaN wafer larger than φ6 inches. Therefore, we attempted the selective growth of point seeds by MOCVD on a φ8 inch sapphire substrate. The growth of uniform point seeds in the plane became more difficult with larger diameters; however, by optimizing the MOCVD growth conditions, we successfully obtained a φ8 inch diameter MPS substrate with no lack of point seeds. **Figure 10** shows a photograph of the φ8 inch MPS substrate with φ3 and φ6 inch substrates. In the φ8 inch substrate, numerous point seeds with diameters of several hundred microns are arranged within a hexagonal region spanning ≈8 inches diagonally.

Next, the apparatus for the FFC technique was introduced into a large reactor to grow a GaN crystal on the aforementioned 8 inch MPS substrate using the Na-flux method. After crystal growth with the MPS substrate and the FFC technique was completed, the grown GaN crystal spontaneously separated from the sapphire substrate during the cooling process, and a freestanding hexagonal GaN crystal with an 8 inch diagonal length was successfully obtained. The thickness of the grown crystal was ranged from ≈1.3 to 1.7 mm. With the current setup, it is possible to achieve a thickness of 5 mm or more. In previous growth experiments, we have confirmed that the TDD is maintained or slightly reduced with increasing a thickness at a constant growth rate, so that we expect the TDD not to increase in the above thickness range. However, the growth rate is slow at ≈10 μm h^{-1}. For mass production of GaN substrates, we are currently considering the use of GaN crystals fabricated by the Na-flux method as seed crystals and growing thicker films by HVPE, OVPE, or ammonothermal methods. As shown in **Figure 11**a, a circular GaN wafer was hollowed out from the crystal with a core drill, and a φ161 mm GaN wafer was successfully obtained without cracks. As seen

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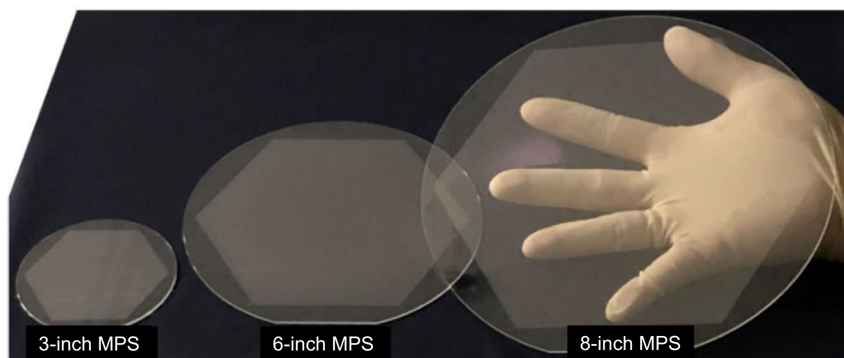

Figure 10. The φ8 inch MPS substrate shown with φ3 inch and φ6 inch MPS substrates.

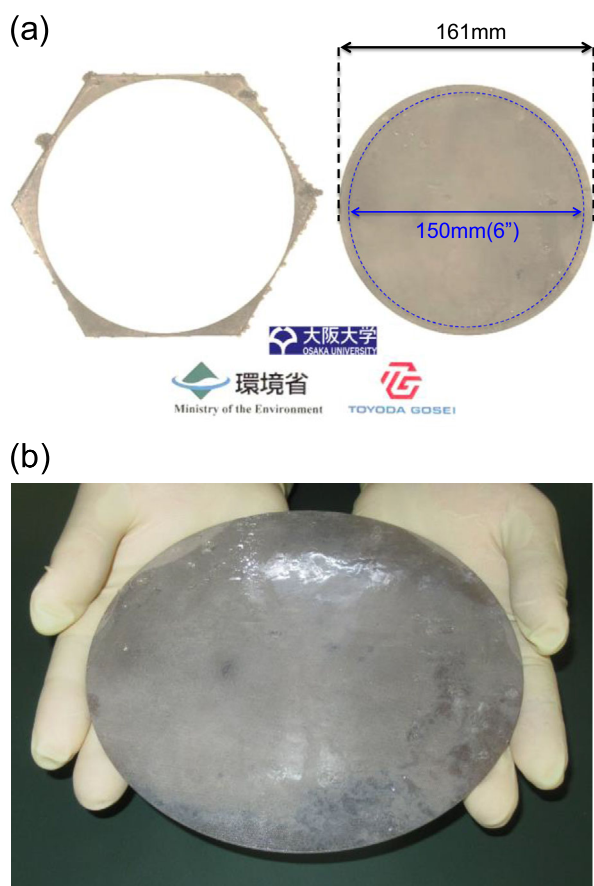

Figure 11. Photographs of a) a φ161 mm GaN wafer hollowed from a hexagonal GaN crystal with an 8 inch diagonal length, and b) the same wafer taken from a different angle.

from the as-grown surface of the GaN wafer in Figure 11b, the crystal surface is flat and mirror-like, indicating that complete *c*-plane growth by the FFC technique and sapphire separation through the MPS substrate can be realized without problems, even on large-diameter substrates. Currently, we are attempting to produce MPS substrates larger than φ10 inches to obtain GaN wafers larger than φ8 inches.

5. Summary

In this article, the structural quality of the latest GaN crystals grown using the Na-flux method and the characteristics of a vertical transistor fabricated on a GaN substrate grown using the Na-flux method were described. In the latest GaN crystal grown with the optimized condition, the area with low TDD on the order of 10^3 to 10^4 cm^{-2} existed even above the region including coalescence boundaries of several GaN crystals, while TDD was usually on the order of 10^4 to 10^5 cm^{-2} in crystals grown with a conventional condition. The lattice curvature radius of the latest GaN crystal was greater than 100 m. The vertical transistor produced on the Na-flux-based HVPE-GaN substrate exhibited normally off operation with a gate-voltage threshold of over 2 V and a maximum drain current of 3.3 A during the on-state operation, indicating the achievement of the first vertical GaN transistor operation on a GaN substrate produced through the Na-flux method. A breakdown voltage of over 600 V was confirmed based on the off-state characteristics, and a low leakage current was realized. We also found that the on-resistance variation could be reduced by suppressing the effective carrier density variation using a GaN substrate with small off-angle variations. In addition, the reverse *I–V* characteristics of the parasitic PND structures exhibited suppression of the number of devices with a large leakage current compared to the commercially available GaN substrate. These results indicate the importance of low bowing and TDD in GaN crystals. Finally, we demonstrated a circular GaN substrate with 161 mm diameter, surpassing 6 inches, grown by the Na-flux method, which is the largest GaN substrate except for those made through the tiling technique.

We believe that the Na-flux method provides GaN substrates with a low TDD, small off-angle variation, and large diameter, which are essential for the practical application of vertical GaN transistors. Currently, we are attempting to grow GaN wafers larger than φ8 inches.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

6 inch, GaN, hydride vapor phase epitaxy, Na flux, on-resistance, p–n junction diode, vertical transistor

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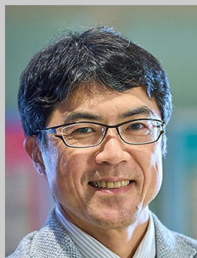

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