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FlashCam: a novel Cherenkov telescope camera with continuous signal digitization

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ABSTRACT: The Cherenkov Telescope Array (CTA) will be the next generation ground-based observatory for cosmic gamma rays. The FlashCam camera for its mid-size telescope introduces a new concept, with a modest sampling rate of 250 MS/s, that enables a continuous digitization as well as event buffering and trigger processing using the same front-end FPGAs. The high performance Ethernet-based readout provides a dead-time free operation for event rates up to 30 kHz corresponding to a data rate of 2.0 GByte/s sent to the camera server. We present the camera design and the current status of the project.

KEYWORDS: Trigger concepts and systems (hardware and software); Front-end electronics for detector readout; Data acquisition concepts; Gamma telescopes

Contents

I	Introduction
2	Concept of FlashCam
	2.1 The photon-detector module
	2.2 The readout system
3	The camera trigger
	3.1 Trigger class simulations
	3.2 Trigger class implementation
4	Performance of FlashCam
5	Summary

1 Introduction

Very high energy (VHE) cosmic gamma rays are messengers from galactic and extragalactic objects like supernova remnants, active galactic nuclei, pulsar wind nebulae and others allowing the examination of those objects within the highest energies of the electromagnetic spectrum. The observation of such VHE gamma rays is possible either with space-borne satellites like FERMI [1] or with ground-based observatories like the current Imaging Atmospheric Cherenkov Telescopes (IACTs) MAGIC [2], H.E.S.S. [3], and VERITAS [4]. The IAC technique exploits the atmosphere as calorimeter where the primary gamma ray undergoes pair production resulting in an electromagnetic shower. An IAC telescope may map, with a tessellated mirror, the morphology of the faint ($\mathcal{O}(100)$ photons/m² for 1 TeV gamma ray) and short (few ns) Cherenkov light pulse produced by the secondary particles of the shower into a pixelated camera. The analyzed picture allows the reconstruction of the direction and of the energy of the primary gamma ray.

The Cherenkov Telescope Array (CTA [5]) will be the next generation ground-based Cherenkov observatory for VHE gamma rays. The project aims to improve on sensitivity by a factor of ten compared to current experiments and to extend the accessible energy coverage well below 100 GeV and above 100 TeV. The array, divided into a northern and southern subarray, with about 50 and 120 individual telescopes, will host single and dual mirror telescopes with dish diameters from 4 m up to 23 m. The large number of telescopes and the weak signal signature call for cost effective and very sensitive telescope cameras.

FlashCam, a joint project of several groups from four European countries, is a novel modular camera design best suited for the 12 m mid-size single-dish telescope (MST) of CTA. It is designed such that the photon-detector plane can be adapted to provide different number of pixels (from 900 up to 2304 pixels arranged in a hexagon), different pixel pitch or different sensor types (e.g. Si

1

2 2 4

4 4 6

7

7



Figure 1. Schematic illustration of the basic concept of FlashCam. The photon-detector plane is separated from the readout and both blocks can be multiplied to form cameras with varying number of pixels.

photodetectors or photomultiplier tubes) without modifying the readout electronics. However, the mechanics may have to be adapted accordingly.

2 Concept of FlashCam

Many lessons learned from other Cherenkov telescope and high energy particle experiments, as well as new ideas, have been incorporated into the concept of FlashCam. The three basic ideas are: a continuous and dead-time-free digitization of the sensors' signals to allow the implementation of the trigger algorithms on the digital side, the separation of the readout electronics and the sensor plane with transmission of the analogue sensor signals via off-the-shelf category 6 (CAT6) cables, and implementation of highest modularity wherever possible to introduce highest flexibility and maintainability. Figure 1 gives an overview of the concept showing the photon-detector modules on the left side and the Field Programmable Gate Arrays (FPGA) based readout electronics on the right side.

2.1 The photon-detector module

Figure 2 shows a photon-detector plane (PDP) module equipped with twelve photomultiplier tubes (PMT). The hexagonal shape of the PDP (figure 3) is formed by rotating the modules by 120° and 240° naturally leading to three sectors as indicated by the dashed lines. Each sector with its corresponding readout electronics forms a kind of self-contained unit. Digitized and preprocessed pixel data of each sector (see section 3.2) are exchanged with the other sectors within the readout electronics to allow a seamless trigger.



Figure 2. Rear-side view of a PDP module equipped with 12 PMTs. The Royer high voltage generators are implemented on the small piggyback PCB. The three RJ45 connectors are used to transmit the analogue signals of the 12 pixels to the readout electronics. Power and slow control (CAN-bus) is provided via the DSUB-9 connector.



Figure 3. 144 pixel mini-camera with 12 PDP modules seen from the rear. The power distribution and the CAN-bus is daisy-chained by a ribbon cable (later on replaced by a multicore cable with larger cross section). The dashed yellow lines indicate the boarder of the three sectors formed by the rotating of the PDP modules.

The functions of the PDP module are divided into three parts, each being implemented on a separate board. The control part (figure 2 rear PCB) hosts a microcontroller and the Controller Area Network (CAN) bus interface for slow control. The analogue part (front PCB including the detectors) comprises the high voltage (HV) regulation and distribution for the PMTs, preamplifiers, current and voltage measurement circuits. The third part, the HV generation realized on a small piggyback, hosts two custom developed Royer type HV generators for -500 V and -1.5 kV. The interface to the readout electronics is realized with three RJ45 connectors for the differential transmission of the analogue signals of four pixels per connector. All required voltages are generated on-board with high efficiency DC-DC converters supplied by 24 V. The total power consumption of a single PDP module is 2.3 W. The low power consumption allows a passive cooling of the modules by simple convection inside the camera housing (consumption of 147 modules for a 1764 pixel camera is about 450 W distributed over an area of about 4 m²).

The PMTs deliver signals which cover the large amplitude range of 1 photoelectron (pe) up to several 1000 pe, with the latter being more rare. The upper limit has been set by the CTA collaboration at 3000 pe, thereby covering most relevant physics cases. The preamplifier used on the PDP module, a current feedback operational amplifier (AD8001), is operated in its linear transfer regime to cover amplitudes up to several 100 pe (threshold is adjustable over the gain and the supply voltage) and in a saturation regime for the higher amplitudes. During saturation of the amplifier, the PMT pulses are 'transformed' into square-like pulses with areas proportional to the input pulse amplitudes. Integrating the resulting signals and unfolding them allows to have a single signal path for the large amplitude range, reducing components, costs and power consumption. Unfolding of the signal may be done inside the readout FPGAs or offline (currently implemented).

2.2 The readout system

The readout of the PDP modules is realized with general purpose FPGA (Xilinx Spartan-6) motherboards selectively equipped with functional daughter boards (ADC-, trigger-, or master-triggerboards) and installed in mini-crates, half 19" crates. Such a mini-crate, equipped with eight motherboards, can digitize the signals of up to 192 pixels (16 PDP modules). A ninth motherboard is equipped with a trigger daughter board for preprocessing of the digitized signals coming from the mini-crate ADC modules and from the neighboring mini-crates. Four such mini-crates per PDP sector, twelve in total are foreseen.

Each ADC daughter board is equipped with twelve 250 MS/s 12 bit ADCs to serve a single PDP module. The signals are digitized continuously and sent to the motherboard FPGA (see also figure 1). There, the data are stored in ring buffers allowing to send pre and post trigger data to the camera server whilst new data are stored in parallel ring buffers. The currently implemented ring buffers have a depth of up to 8000 samples, which corresponds to $32 \,\mu$ s per pixel. A high-performance raw Ethernet protocol is implemented to handle the large amount of data sent over commercial Ethernet switches from each motherboard to the distant camera server. The camera server, located for instance in a counting house, performs post-processing (e.g. event-building) of the data and makes the data available to the storage system (disk or tape). Data transfer rates of 3.8 GByte/s have successfully been measured using a cluster of computer nodes emulating the readout electronics. The camera server can process more than 2 GByte/s with post-processing of the data (event-building), which results in an upper camera trigger rate of about 30 kHz. A final event rate of about 16 kHz, which can be stored to disk with full event information, is possible after event selection by e.g. using an array-wide trigger scheme.

3 The camera trigger

The Cherenkov light pool induced by a gamma ray may extend at ground level over areas much larger ($\gg 400$ times larger) than the mirror area of the telescope. Hence, an IACT will 'see' the Cherenkov light as long as the telescope is located within the illuminated area, the telescope's detection area. A figure of merit of an IACT is thus the effective (detection) area, which is defined for given energy intervals and convolves the detection area with the efficiency of the telescope to detect an event. The major included efficiencies are those of the mirrors, the photo-detectors, the readout electronics and the trigger classes. The latter can be compared and optimized by calculating the corresponding effective areas.

3.1 Trigger class simulations

FlashCam has the advantage of the trigger evaluation being implemented on the digital side, hence having access to the full digitized signal form. This allows the implementation of a large variety of trigger classes and the exchanging of classes or adjusting of parameters during observation. Simulations have shown that one of the most efficient and homogeneous trigger classes would be a sum trigger. The amplitude of a number M of unique pixels are summed up. The resulting amplitude is clipped and the resolution is reduced to e.g. 4 or 8 bits. Subsequently, a number N of such patches are summed up and compared to a threshold to generate a possible trigger event. Figure 4



Figure 4. Performance of different clipped sum trigger configurations. The figure shows the achievable effective detection area of a mid-size telescope for a wide range of VHE gamma-ray energies. Best performance for the effective area is achieved with the P3-4 closely followed by the P3-7 configuration. The digital majority trigger performs worst of all tested trigger configurations.



Figure 5. Spatial trigger homogeneity over the full camera detector area for different clipped sum trigger configurations. Δ_{eff} describes the area between the two trigger efficiency curves of the trigger roll-off between equal inner (red) and outer (blue) areas of the basis shape (e.g. P3) for each patch. The P3-7 performs best for low energy events.

shows a trigger simulation with a variety of numbers for M and N with the resulting sensitivity. A digital majority trigger class has also been evaluated for comparison. Figure 5 shows the trigger homogeneity over the whole camera for different patch configurations. The best combined result is achieved with a P3-7 trigger, clipped sum of three unique pixels in patches and sum of



Figure 6. Trigger data transfer scheme shown in detail for one of the three camera sectors with 64 PDP modules (largest possible camera with 2304 pixels). The trigger data transfer to the camera server is not shown.

seven patches. The simulated results have yet to be confirmed with measurements but this has been postponed due to the difficult task of setting up a proper setup.

3.2 Trigger class implementation

The trigger condition evaluation is performed at four places: on the ADC card,¹ on the trigger card, on the master trigger card, and finally on the camera server. The first operation performed on the ADC card is a sum of a number of unique *M* pixels with a subsequent clipping and reduction of the bandwidth to ≤ 8 bit to reduce the amount of data. The clipped sums are sent each clock cycle (4 ns) to all twelve trigger cards over mini-crate backplanes and via CAT5/6 cables to allow a seamless and homogeneous trigger decision (figure 6). The camera trigger can be generated on each trigger card individually by, for instance, summing up for each individual patch its adjacent patches and setting a threshold to the sum. The resulting trigger signals are sent to a master trigger

¹The notation *card* refers to the combination of an FPGA motherboard with a specific daughter board.



Figure 7. Measured charge resolution of a single pixel compared to the CTA requirements. The square dots denote the amplitude determination with the pulse amplitude while the round dots denote the amplitude determination with the pulse area.

card, which initiates the readout of the ring buffers and the sending of the data to the camera server. A synchronous signal transmission over all paths is achieved by phase locking of the individual clocks to a distributed clock from the master trigger card to each trigger card and from there to each board over the crate backplane.

4 Performance of FlashCam

The performance of FlashCam has mainly been verified with the 144-pixel setup shown in figure 3 and a single mini-crate with six ADC cards and one trigger card. Besides functionality checks, many parameters for operation as a Cherenkov camera have been verified. For example, the time and amplitude resolution of single pixels under different environmental conditions as temperature changes and different amounts of night sky background (NSB: light pollution from sources like stars, artificial lights etc.). Figure 7 shows a typical measurement of the amplitude resolution for two representative pixels under nominal NSB conditions. The achievable amplitude resolution fulfills the specified CTA requirement and goal. The reconstruction of the pulse amplitude for the linear and the saturation regime of the preamplifier was done with the readout FPGA and verified offline. For the linear regime, a simple max-search algorithm is used, whereas an integrator in combination with a calibration factor is used for the non-linear regime.

5 Summary

The Cherenkov Telescope Array (CTA) [5] will be the next generation array of Imaging Atmospheric Cherenkov Telescopes (IACTs), and is the successor to the current generation of IACTs, which includes MAGIC [2], H.E.S.S. [3], and VERITAS [4]. These telescopes are used to detect gamma rays in the range of tens of GeV to tens of TeV, emitted from exotic astrophysical sources such as quasars, supernovae and their remnants, gamma-ray bursts, and dark matter annihilations. When these gamma rays enter the Earth's upper atmosphere, they create an electromagnetic shower comprising many highly-energetic charged particles. Those particles traveling faster than light in the atmosphere produce Cherenkov photons that travel in a cone to the ground. The IACTs can detect these Cherenkov photons and reconstruct the electromagnetic shower by imaging it with multiple telescopes. The reconstructed shower can then be used to determine the direction and energy of the initial gamma ray. The goal of CTA is to build improved and larger versions of the current IACTs, based upon the lessons learned and exploiting new technologies. CTA is approaching the final R&D stage and first telescope prototypes already exist.

FlashCam [6] is a novel camera design for the mid-size telescope of CTA incorporating a fully digital data and trigger pathway. Its aim is to improve in performance compared to current generation IACT cameras while reducing costs per channel. The key point is a 250 MS/s readout system, permitting a continuous digitization with data buffering and real-time processing in FPGAs. Trigger algorithms are implemented in the same FPGAs and use the full digitized information. This concept introduces flexibility in optimizing signal processing and trigger efficiency without the need of changing hardware. The Ethernet-based readout system sends the data of the 1764 camera pixels to a camera server using standard Ethernet switches and a tailor-made raw Ethernet protocol. Data rates of up to 2.0 GB/s corresponding to about 30 kHz trigger rate have already successfully been transmitted. Photon detectors, currently photomultipliers, high voltage generators and preamplifiers are embedded in discrete 12-pixel modules detached from the readout system. The analogue data are transmitted from the modules via CAT5/6 cables to the readout system. Detaching the two parts permits a simple change of detector types and pixel spacing.

The FlashCam concept has been studied extensively and has entered the prototyping phase. First results with a 144 pixel prototype show a significantly better performance than required for CTA. The first camera housing prototype has been assembled and is currently being equipped with the cooling and safety system. The first fully equipped FlashCam is foreseen for mid 2015.

Acknowledgments

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