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A switch for epitaxial graphene electronics: Utilizing the silicon carbide substrate as transistor channel

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Due to the lack of graphene transistors with large on/off ratio, we propose a concept employing both epitaxial graphene and its underlying substrate silicon carbide (SiC) as electronic materials. We demonstrate a simple, robust, and scalable transistor, in which graphene serves as electrodes and SiC as a semiconducting channel. The common interface has to be chosen such that it provides favorable charge injection. The insulator and gate functionality is realized by an ionic liquid gate for convenience but could be taken over by a solid gate stack. On/off ratios exceeding 44000 at room temperature are found. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3695157]

Graphene has the potential for outstanding electronic applications. In particular, it has high charge carrier mobilities[1,2] and extremely high current stability.[3,4] High-frequency transistors and circuits have been demonstrated with amplifier functionality.[5] However, a reliable switch with large on/off ratio is still not realized. Previous experiments on transistors with graphene as active channel show only on/off ratios of the order of 10 due to the absence of an energy gap in graphene's band structure.[6–9] Various concepts have been proposed, typically in operation regimes remote from practical requirements.[10]

To our opinion, epitaxial graphene grown on silicon carbide (SiC) is the ideal material for graphene microelectronics, because it provides a high-quality, wafer scale, CMOS processing compatible system, and as we will see the ability to implement an efficient switch by employing the underlying SiC substrate. However, the SiC/graphene interface can be prepared with different properties. In order to couple both materials electronically, a special choice is mandatory. We opted for monolayer graphene (MLG) material on n-type SiC (0001).[5,11] This well-defined epitaxial interface determines the properties of the graphene layer (electron density $n \approx 10^{13}\,\mathrm{cm}^{-2}$, room temperature mobility $\mu \approx 800$–$1200\ \mathrm{cm}^2/\mathrm{Vs}$)[2] and provides the favorable charge injection between graphene and SiC.[12] Earlier experiments on this material have revealed that the graphene layer is lying on top of a buffer layer of carbon, which is not conducting.[13,14] The SiC material underneath is partially terminated by bonds to the buffer layer, partially by dangling bonds, which provide Fermi level pinning to the graphene layer.[12,15] Note that a manipulation of this interface, e.g., hydrogen intercalation,[16] leads to a drastically increased injection barrier and inhibits vertical current flow.

In contrast to pure graphene electronics,[5,8,17] we make use of the advantages of both layers of the compound system: we design current paths in the graphene layer as well as in the wide-bandgap semiconductor SiC. We focus on the hexagonal polytype 6 H (bandgap $E_g = 3.06\,\mathrm{eV}$).

Two different SiC wafers A and B were used. Wafer A is semi-insulating, on-axis 6 H-SiC(0001) with vanadium (V) doping of $[\mathrm{V}] \approx (1-2) \times 10^{17}\,\mathrm{cm}^{-3}$. Surface polishing damage was reduced by a hydrogen etch step.[11] Nitrogen (N) implantation was carried out at room temperature through a masked oxide layer using a box profile with a mean concentration of $[\mathrm{N}] = 4 \times 10^{17}\,\mathrm{cm}^{-3}$ up to a depth of 50 nm below the oxide layer. After oxide removal, graphene was grown in a vertical cold-wall reactor under 900 mbar of argon pressure at 1700 °C resulting in ≈1.3 monolayers (characterized by core level photo electron spectroscopy (XPS)).

Wafer B is an n-type 6H-SiC wafer 3.5° off the (0001) direction. A 3.0 μm thick heavily aluminum (Al) p-doped ($[\mathrm{Al}] = 2 \times 10^{18}\,\mathrm{cm}^{-3}$) and a 2.9 μm thick low n-doped ($[\mathrm{N}] = 1 \times 10^{15}\,\mathrm{cm}^{-3}$) epitaxial layer were deposited by chemical vapour deposition (CVD). Subsequent to hydrogen etching (consuming 400 nm of SiC), graphene was grown. To achieve the same graphene coverage as on wafer A, the growth temperature was reduced to 1650 °C. Mesa structures were fabricated by reactive ion etching to avoid conductive edge paths between the epilayers and to open a window to the p-doped layer, which was contacted by ohmic nickel (Ni) contacts.

On both wafers, graphene was patterned by electron beam lithography and subsequent oxygen plasma etch followed by a hydrogen fluoride dip. Metal contacts (5 nm titanium and 50 nm gold) were deposited by electron beam evaporation. The gate was realized using a small droplet of the ionic liquid (IL) 1-ethyl-3-methylimidazolium tris(pentafluoroethyl)trifluorophosphate (EMIM FAP) with a diameter of ≈500 μm and a dipped-in tungsten tip. The electrical characterization used relatively long delay times between the distinct data points (10–60 s) in order to allow the IL to relax to stable configurations.

Fig. 1 shows the basic device concept: the essential feature is that graphene is partially removed, such that two graphene electrodes are defined (source and drain). When a current is passed from source to drain, the only available path is through the semiconductor. However, for the semi-insulating wafers frequently used for epitaxial graphene

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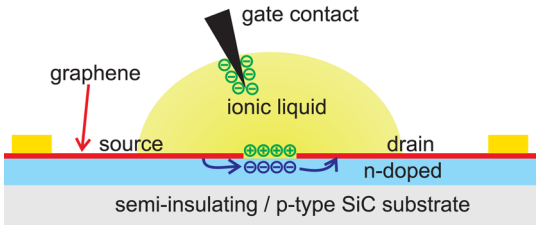

FIG. 1. (Color online) Scheme of the device showing two separated graphene electrodes on top of the n-doped SiC. The current is guided through the semiconducting layer, which is vertically confined by an underlying semi-insulating or a p-doped layer. The IL droplet serves as gate electrode.

investigations, the resistance is at least in the TΩ-regime.[4] In devices fabricated on wafer A, a current pathway is offered in the N implanted layer. The n-doping has two favorable consequences: First, the injection barrier between graphene and SiC is relatively low.[12] Second, free charge carriers are created in the n-type region, which can be accumulated or depleted by an electrostatic gate, typically using a solid gate stack. We, however, opted here for a liquid gate using a droplet of IL. This replacement allows a convenient test of the concept. It brings along extremely high gate efficiency and virtually no damage to the surface[18] (drawbacks of using ILs will be discussed below). When a positive gate voltage V_{TG} is applied to the gate contact, an electrical double layer forms at the interface, which induces electrons in the semiconducting channel. Fig. 2(a) displays the gate effect on the source-drain current I_D measured on a device with channel width $W = 200\,\mu$m and channel length $L = 5\,\mu$m. A current I_D of 660 nA ($V_{SD} = 0.1$ V) is flowing when $V_{TG} = 2$ V is applied. At negative gate voltages, the current is suppressed as charge carriers are displaced from the channel. An on/off ratio of 36 is resulting within the electrochemical stability range of the IL. The leakage current through the IL remains below 10 nA and is, therefore, negligible (see Fig. 2(a) lower part).

Note the simplicity of the fabrication of this first and essential test device: lithography alignment is uncritical; the only requirement is the removal of graphene to form a transistor channel in the n-type semiconductor. Further, the graphene quality (monolayer/multilayer, with voids or other imperfections) is not essential for basic device operation, as long as the interface is epitaxially defined. It is obvious that a proper design of the semiconductor and its doping opens wide space for engineering.

Consequently, an improved setup was built using wafer B with a layered p-n junction. The upper low-doped n-type layer was partly used as the source for graphene growth. The result is a graphene layer with an underlying high-mobility n-type SiC ($\mu = 350$ cm^2/Vs at room temperature obtained from Hall-effect data (not shown)). The conductive channel layer is vertically confined by the space charge regions of the p-n junction at the bottom side and by the gate stack at the top side. This setup further allows tuning the thickness of the conductive layer *in operandi* by applying a parametric backgate voltage V_{BG} to the p-type layer. As a further improvement, the channel width to length ratio has been increased by a factor of 250 to $W/L = 10\,000\,\mu$m/1 μm using a meander-like geometry. A specific graphene/SiC contact resistance of $\rho_C \approx 0.06\ \Omega\ \text{cm}^2$ has been determined by circular transfer length method (C-TLM). Although this value is higher than

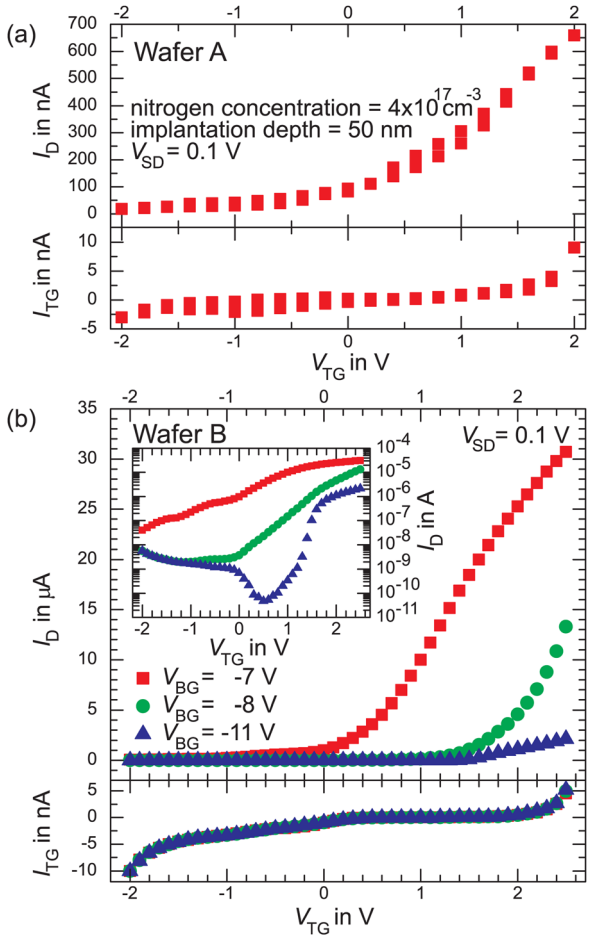

FIG. 2. (Color online) Transfer characteristics (upper panel) and leakage currents (lower panel) for sample A (a) and sample B (b). The device operation of wafer B can be tuned using a parametric backgate voltage V_{BG}. Both normally on (red squares) and normally off (blue triangles) operations are possible. The inset shows the same data in logarithmic scale.

for metal ohmic contacts to SiC,[19] the graphene/SiC contact is perfectly ohmic despite the very low doping concentration of the SiC epilayer.

Fig. 2(b) displays the transfer characteristic of the improved device. We first discuss the data observed with a backgate voltage of $V_{BG} = -11$ V, which corresponds to the normally off operation. The minimum current flow is $I_D = 4.8 \times 10^{-11}$ A, whereas at $V_{TG} = 2.5$ V a current of $I_D = 2.1 \times 10^{-6}$ A is measured. This corresponds to an on/off ratio of 4.4×10^4, which is many orders of magnitude better than for previous graphene transistors that rely on graphene as active channel, and is well in the range of many technological applications. The limitations of the on/off ratio are given by the stability range of the IL not by the graphene/SiC part. This can be seen both in the off- and on-states: The unexpected upturn of I_D at negative V_{TG} results from the leakage current through the IL. On the other hand, we see no saturation at positive V_{TG} (cf. linear transfer characteristic, Fig. 2(b)). These observations suggest that an optimized gate stack will allow even better device performance.

When choosing more positive backgate voltages the channel is opened and at $V_{BG} = -7$ V, the device is in the normally on mode. The data in Fig. 2(b) (red squares) show the device performance when sweeping the topgate: the

current level at zero topgate voltage equals 10^{-6} A and can be switched off to 4×10^{-8} A by applying $V_{TG} = -2$ V. Again, the current range is rather limited by the stability of the gate than by the graphene/SiC part of the device. For positive topgate voltage, the current can substantially be increased beyond 3×10^{-5} A. It should be stressed that the backgate is convenient for fundamental experiments but is not required for the device operation. When doping and thickness of the n-type epilayer are well balanced, both operation modes can be implemented without external control voltage.

The observed field effect of the top gate may origin from two mechanisms: (i) a gate effect that modifies the number of free charge carriers in the channel or (ii) a gate effect on the graphene monolayer, which affects the charge injection from graphene to SiC. The precedent observation of Fermi level pinning[12] may already exclude mechanism (ii), but we carried out further control experiments to disentangle the two mechanisms. In particular, *I-V* measurements of a single graphene/SiC interface (Fig. 3(a)) showed a rather small gate effect ($\Delta I_D (V_{TG})/I_D \approx 0.1$) of the charge injection (Fig. 3(b)). Moreover, when protecting the graphene source/drain electrodes of a transistor device with PMMA from immediate contact to the IL no qualitative change of the overall gate behavior has been observed. Hence, the large gate effect is indeed caused by a field-effect transistor mechanism. This implies that the same effect is expected when more graphene layers are added, up to graphitic material, which would reduce the serial resistance of the electrodes. The charge injection into the channel is thereby unaffected: it depends on the epitaxial interface between the SiC and the first graphene layer.

The ionic liquid device provides several drawbacks: First, the source-drain voltage V_{SD} is limited by the electrochemical stability window of the IL, and consequently, the high-voltage capabilities of the transistor cannot be tested. Second, the frequency of operation is limited by the slow rearrangement of the IL; hence, no speed-of-operation of the graphene/SiC part can be derived from our experiments. Third, the voltage scale is not fully reproducible: due to our simplified setup without reference electrode, the applied voltage V_{TG} drops partially at the tip/IL interface and partially at the IL/SiC interface.

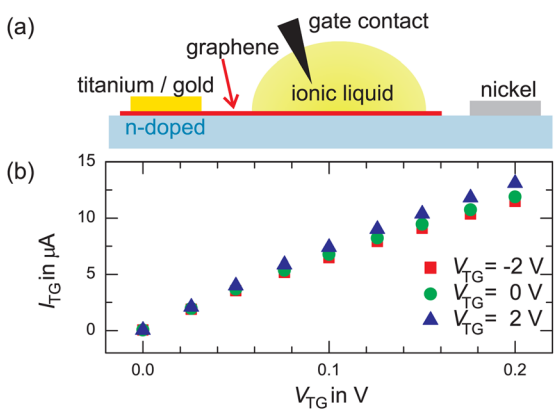

FIG. 3. (Color online) (a) Sketch of a control experiment to explore the influence of the gate on the injection barrier between graphene and SiC. Current flows through a gated graphene electrode to the substrate contacted with an ohmic nickel contact. (b) *I-V* measurements at different gate voltages show only little difference.

Although we took care to establish the predominant fraction of voltage drop at the channel interface, the ratio depends on the different interfaces and is, therefore, a source of variations from experiment to experiment.

For a technological application, a solid gate stack is mandatory. Given the successful proof of principle and the known strength of the materials graphene and SiC, we anticipate that such a device will operate at high temperatures, high voltages, and high frequencies, also under harsh chemical and radiative conditions.

Altogether, we propose a switch with large on/off ratio for epitaxial graphene electronics. The fabrication effort is small. The device is robust and scalable. The concept of employing both the graphene layers, but also the underlying SiC semiconductor for guiding the current through an electrical circuit overcomes obvious problems related to graphene-only electronics. When fitted with a solid gate stack, this transistor concept may be combined with graphene-only circuits[5,17] or with state-of-the-art SiC power electronics[20] side-by-side on the same chip.

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