**Title** X-IFU CryoAC technology demonstration plan

| | | | | |
|---|---|---|---|---|
| Prepared by : | C. Macculi, A. Argan, G. Torrioli | | Date : | 27/07/2020 |
| Inputs by : | F. Gatti, L. Ferrari Barusso, M. Rigano, G. Minervini, M. D'Andrea | | Date : | 27/07/2020 |
| Agreed by : | D. Brienza | | Date : | 27/07/2020 |
| Approved by: | A. Argan | | Date : | 27/07/2020 |
| Authorised by: | L. Piro | | Date : | 27/07/2020 |

## DISTRIBUTION LIST

X-IFU consortium
ESA

## DOCUMENT CHANGE RECORD

| Issue | Date | Changed Section | Description of Change |
|---|---|---|---|
| | | | |
| Issue 1 | 14/01/2020 | | First Issue. |
| Issue 2 | 27/07/2021 | 2 | Figure 3 updated (thermometer readout in charge of the FAB) |
| Issue 2 | 27/07/2021 | 3 | Section updated |
| Issue 2 | 27/07/2021 | 5.1 | Section updated |
| Issue 2 | 27/07/2021 | 5.1.2 | New section “Structural Model 0 (SM0)” added |
| Issue 2 | 27/07/2021 | 5.1.3 | Section updated |
| Issue 2 | 27/07/2021 | 5.1.6 | Old section “Demonstration Model 2 (DM2 - TBC)” deleted since no more applicable. |
| Issue 2 | 27/07/2021 | 7.2.2 | Section updated |
| Issue 2 | 27/07/2021 | 7.2.3 | Section updated with Inphotec contribution |
| Issue 2 | 27/07/2021 | 8 | Figure 8 updated |

## Abbreviations and acronyms

| Item | Meaning |
|---|---|
| AIT | Assembly Integration and Test |
| ASI | Agenzia Spaziale Italiana |
| ASW | Application Software |
| BB | BreadBoard |
| CADM | Configuration and Data Management |
| CNR | Consiglio Nazionale delle Ricerche |
| CPO | Central Project Office |
| CryoAC | Cryogenic Anticoincidence |
| FA | Funding Agency |
| FEE | Front End Electronics |
| FPA | Focal Plane Assembly |
| GSE | Ground Segment |
| ICU | Instrument Control Unit |
| INAF | Istituto Nazionale di Astrofisica |
| LPO | Local Project Office |
| MP | Management Plan |
| OBS | Organization Breakdown Structure |
| PA | Product Assurance |
| PBS | Product Breakdown Structure |
| PS | Project Scientist |
| SM | System Manager |

| | |
|---|---|
| UniGE | University of Genova |
| UniPA | University of Palermo |
| WBEE | Warm Back End Electronics |
| WBS | Work Breakdown Structure |
| WE | Warm Electronics |
| X-IFU | X-ray Integral Field Unit |

## Applicable Documents

| [AD#] | Doc. Reference | Issue | Title |
|---|---|---|---|
| [AD1] | SRON-XIFU-SP-2018-028 | 1.0 | FM CryoAC requirement specifications |
| [AD2] | XIFU-INAF-SYS-PL-0001 | 1 | X-IFU Italian Management Plan |
| [AD3] | XIFU-CNRF-CRA-DS-0001 | 1 | X-IFU CryoAC definition document |

## Reference Documents

| [RD#] | Doc. Reference | Issue | Title |
|---|---|---|---|
| [RD1] | XIFU-PL-MAN-296-CNES | 3 | X-IFU Critical Items Demonstration Plan |
| [RD2] | XIFU-INAF-CRA-DS-0002 | 1.0 | X-IFU CryoAC definition document |
| [RD3] | XIFU-INAF-CRA-DS-0001 | 1 | FPA CryoAC Design Concept |
| [RD4] | XIFU-INAF-CRA-TR-0001 | 1 | CyroAC DM test report |
| [RD5] | X-IFU Performance Working Group, 07th October 2020 | | First joint test of CryoAC and TES array DMs in the SRON 40pixB setup |
| [RD6] | Applied Surface Science 197-198 (2002) 169-174 | | Large area PLD of nanometer-multilayers |
| [RD7] | ATH-RP-CGS-001_iss2 | | CRYOAC TRADE-OFF ANALYSIS REPORT |
| [RD8] | ATH-RP-CGS-002 | | CRYOAC SM ANALYSIS REPORT |

# Table Of Contents

# 1 INTRODUCTION

## 1.1 Objectives of the technology demonstration plan

The main purpose of the present plan is to provide a clear path to demonstrate the CryoAC TRL5 by the mission Adoption.

The reference statement from which we have derived our present CryoAC Technology Demonstration Plan comes from the "X-IFU Critical Items Demonstration Plan" document (see [RD1]). It reports:

"The Technology should not be developed to the detriment of the Design. The confusion between Technology demonstration and Design has for consequence to go into Technology demonstration by sacrifying the design with negative impacts:

- Poor requirements
- Poor level of trade-offs
- Poor understanding of d*esign drivers"*

Hence, after having identified the main critical items an effort has been performed in trying to separate, as much as possible, the CryoAC technology from the CryoAC design.
The identified items are:

- Chip (it is the etched Si wafer having on-board the TES network, Nb wiring, and heaters)
- CFEE (this is mainly constituted by the SQUID pcb)
- Mechanics (this is the metallic supporting frame to host the chip)
- Cold Assembly (this is the union of the above items)

This document is structured as follows. We will show:

- in § 2 a brief overview of the CryoAC detector
- in § 3 a brief report about the CryoAC concept validation
- in § 4, for each above identified item, the separation between technology and design
- in § 5 the CryoAC model philosophy
- in § 6 the list of the technological processes
- in § 6 the critical technologies or processes that are the main driver to get TRL5
- in § 8 the planning

Then the Conclusion.

# 2 CRYOAC OVERVIEW

The baselined detector is divided into 4 independent pixels, each one made of silicon having an area of 1.23 $cm^2$, and a thickness of 0.5 mm (TBC). Each pixel is sensed by a network of ~ 120 (TBC) Ir/Au TES connected in parallel (see Fig. 1). The CryoAC is placed below and very close to the TES-arrays, at a distance < 1 mm, to maximize the geometric particles rejection efficiency. The active part, as sum of the 4 independent pixels, covers a full area of 4.91 $cm^2$, larger than the arrays (2.3 $cm^2$). Each pixel is connected to a gold-plated Si rim by 4 Si beams realizing the pixel thermal conductance. Each pixel-absorber will also have deposited on board Pt heaters (see also Fig. 3) to increase its temperature, if necessary, to decrease bias currents thus limiting magnetic coupling effects to the TES array (expected ~ 10 mA order due to the TES network high critical current).

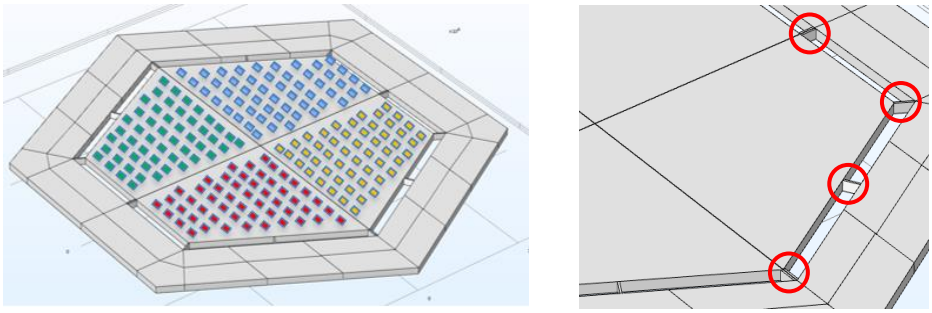

**Fig. 1 - CryoAC baseline configuration: 4 independent pixels. It is shown only the "concept": 4 independent TES networks, each network deposited on a separate trapezoidal absorber. On the right, the 4 silicon beams connecting each of the 4 absorber to the silicon rim are shown.**

This configuration offers important advantages. Being the pixel technology similar to the TES array, integration, interface and SQUID readout issues can be substantially accommodated by using the same technology solutions.

At cold, the mechanics that will support the chip to integrate the chip inside the FPA is at present made of OFHC Cu, gold plated. The chip will be glued at 3 different points onto 3 different "leaf-springs", and the PCB will be screwed on other 3 different points at the bulk of the mechanics. A sketch of the cold assembly is shown in Fig. 2.

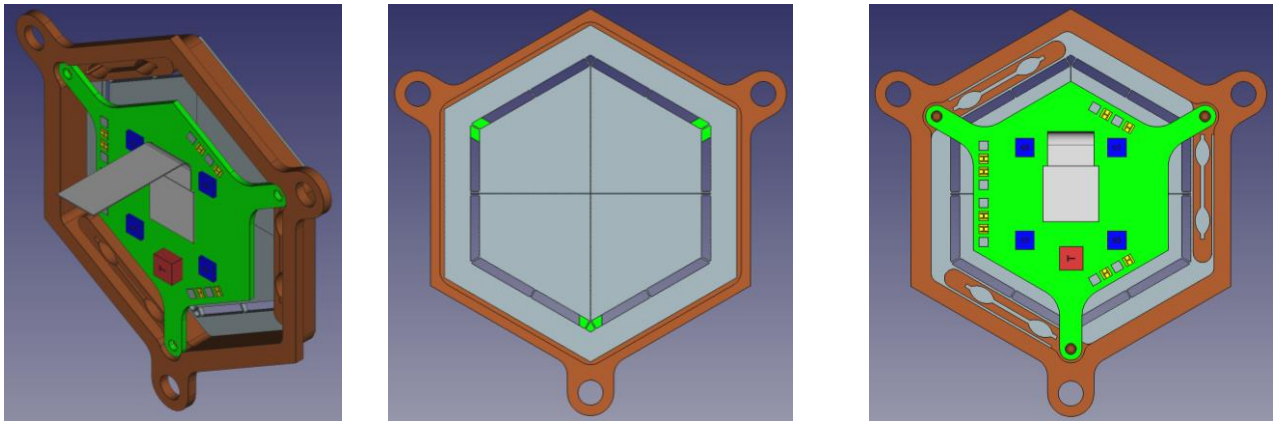

**Fig. 2 - The CryoAC cold assembly: it is shown the chip (it is grey and glued on 3 points onto the leafspring), the CFEE (green), and the mechanics (brown).**

As for the electronics (see Fig. 3), the CryoAC detector will be read out by standard FLL technique based on SQUID, one for each of the 4 pixels in which the detector is divided into, plus only one thermometer to monitor the thermal bath (readout system in charge of the FAB). We plan to adopt the same SQUID technology selected for the TES array, but having requirements tailored to the CryoAC needs. To be compliant with the failure management philosophy we have adopted as baseline an independent FLL chain for each "pixel + SQUID" (4 independent FLL for 4 pixels) that will be served by a so-called Quadrant service electronic section inserted in the CryoAC Warm Front End Electronics (WFEE). The Warm Back End Electronics (WBEE) will manage the WFEE, digitize its analogic output, apply quality grades and time stamps to the pulses, implement triggers identification, and organize the telemetry packet.

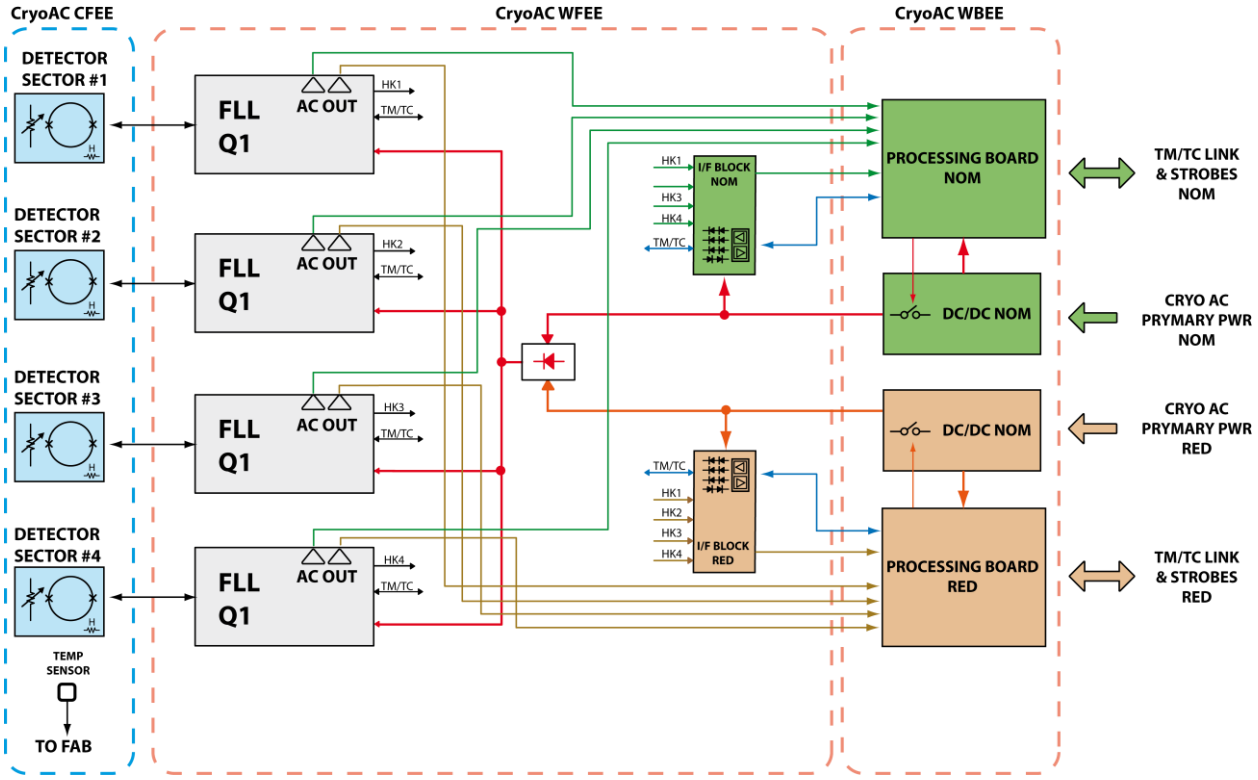


**Fig. 3 - The CryoAC Electronics: Cold Front End (CFEE) composed by the 4 SQUID to sense the current from the 4 pixels, Warm Front End divided in 4 Quadrant, each one providing bias to TES and SQUID single pixel and producing the analogic scientific signal (AC OUT) and the FLL HouseKeepings. On the right the Warm Back End divided in Nominal and Redundant boards, each one processing and digitizing the signal from the WFEE, and packeting the data to be sent to the Instrument Control Unit.**

The baseline foresees that the veto operation will be performed on ground.

More information about the detector definition and related concept design can be found in [RD2], [RD3] and REFs. therein.

## 3 CRYOAC CONCEPT VALIDATION

The concept just reported has been validated in the context of the DM activity where a single pixel detector has been developed by taking into account the following requirements:

- operation at 50 mK (this is the reference "$T_0$" thermal bath inside the X-IFU FPA)
- low energy threshold at 20 keV (it is linked to the required residual particle background)
- absorber area of 1 $cm^2$ (the baseline foresees 4 pixels having ~ 1.23 $cm^2$ area each)
- suspended absorber (the baseline foresees 4 suspended silicon pixels)

Further, it has been allocated at the CryoAC detector as "whole" a power dissipation at cold of 40 nW (CBE) inside the FPA. Thus, also this parameter has been probed during the DM testing activity to verify the compatibility inside the FPA thermal environment.
The magnetic mutual-compatibility with the TES array is part of the DM joint programm which foresees a dedicated campaign.

The DM detector is representative of the baseline configuration, it is a first assessment of the most critical technologies involved and it is the model used to acquire a full knowledge of the physics ruling the detector performance.

In Fig. 4 are reported some pictures and results of the “DM CryoAC” compliant with the above requirements.

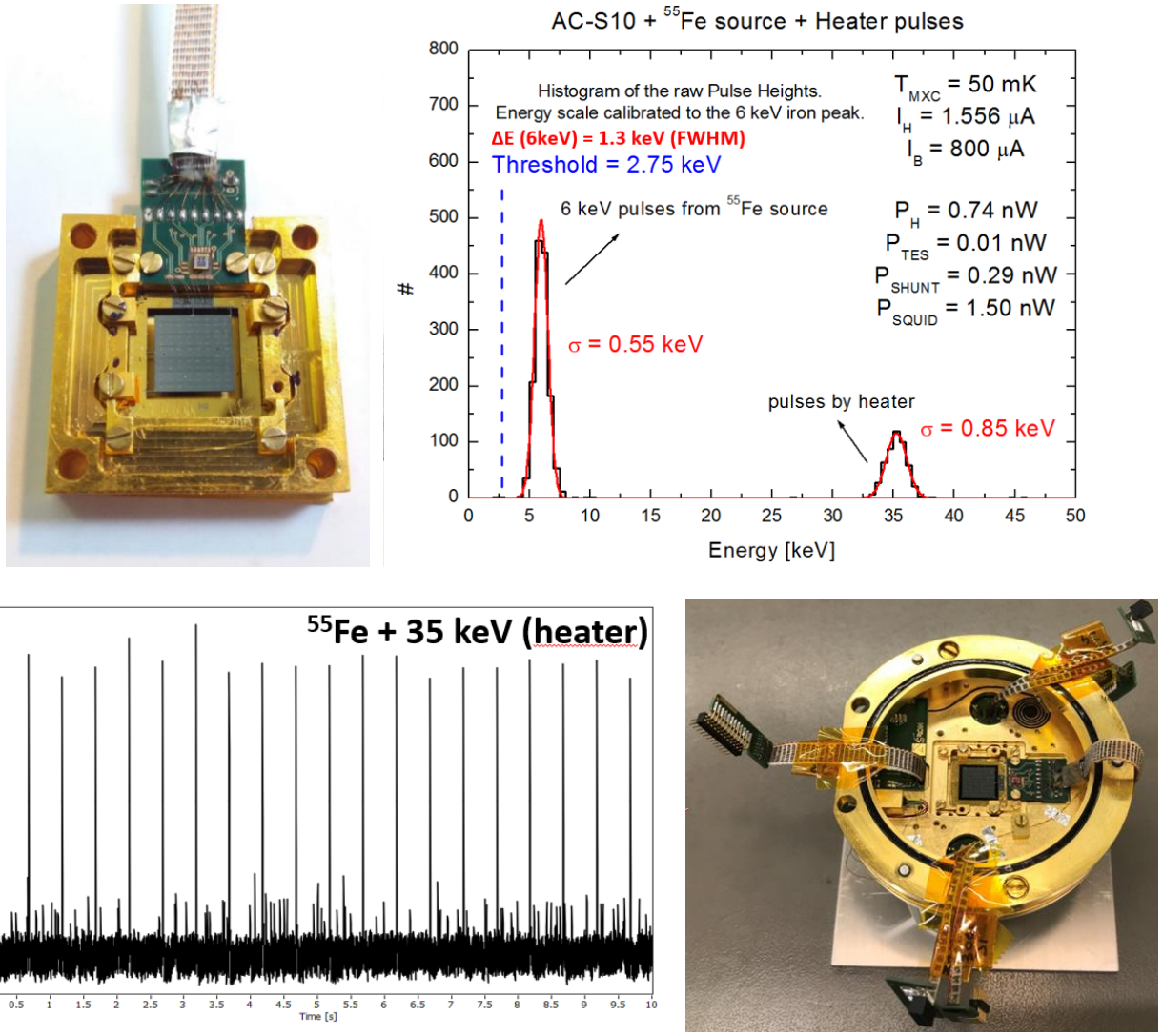


**Fig. 4 - Top left DM: CryoAC in INAF holder. Top right: Energy spectrum from 55Fe, and 35 keV pulses injected by the heater. Bottom left Raw data stream. Bottom right fit-checking in the 40 PxIB flange at SRON (credits SRON).**

See [RD4] for more details.
The DM CryoAC has been integrated in the 40PxIB setup at SRON for the integrated chipset test campaign carried out on mid 2019 – mid 2020.
Just as highlight we report in Fig. 5 an example of the anticoincidence operation performed by the DM CryoAC and the expected typical Landau distribution whose peak is due to the MIP (Minimum Ionizing Particle). See [RD5] for more details.

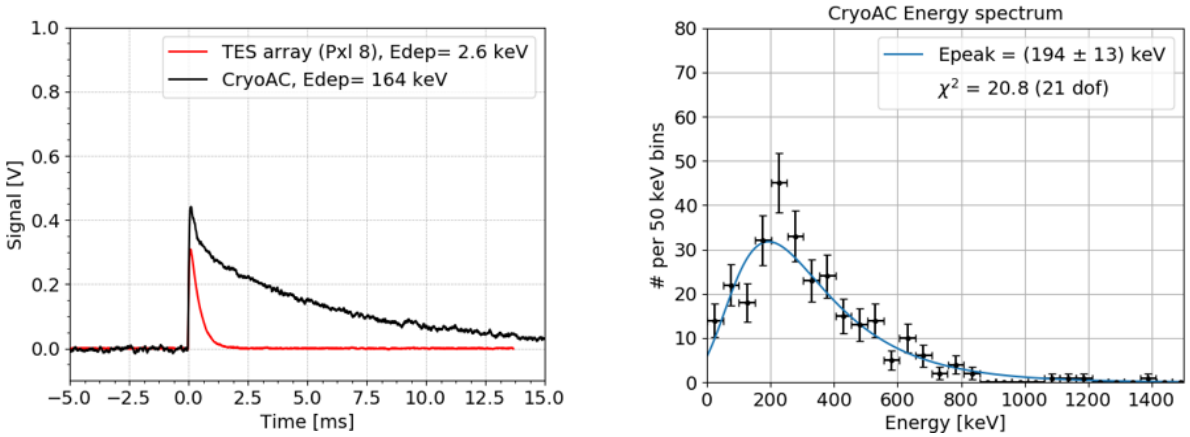


**Fig. 5 - Left - Anticoincidence demonstration of a cosmic muon hitting the TES array. - Right - Distribution of the deposited energy on the CryoAC by muons.**

# 4 TECHNOLOGY VS DESIGN

Following the objective already presented in Introduction, in Table 1 below we show how we separate the technology processes from the design development. This Table represents our main reference for the TRL5 demonstration plan.

| Item | Technology | Design |
|---|---|---|
| Chip | 1. TES network full scale manufacturing processes<br>2. TES network performance (Rn, Tc, Rp) in relevant environment<br>3. Silicon DRIE full scale manufacturing process<br>4. Silicon DRIE mechanical performance in relevant environment | 1. Trade-off related to the thermal model<br>2. Trade-off monolithic vs segmented<br>3. Detector shape optimization<br>4. Rim size<br>5. TES array + FPA I/Fs<br>6. Mass, Volume, Power |
| CFEE | SQUID performance (gain, noise, dissipation, Rs) | 1. PCB Size, volume, mass<br>2. PCB Layout, schematics |
| Mechanics | None | Architecture, Mass, Thermal, Volume |
| Cold Assembly | None | Architecture, Mass, Thermal, Volume, Power |

**Table 1 - Technology vs Design separation: the main items are identified.**

For each item, we have highlighted the main parameters affected by each technological process. We remark that the technology demonstration can be also sensitive to detector full scale area.
In order to deal with unavoidable contact between Technology and Design, we assume to solve the overlap by transferring the optimization to the design process, while the technologies are validated only considering configuration not containing all the details. For example, the detector shape or Si beams size optimization are not a technological process validation but a design issue.

# 5 CRYOAC MODEL PHILOSOPHY

## 5.1 Expected Models

In the next section we are going to provide the main information related to the main expected models to support the Instrument Phase B development of technologies and design.
Such expected models are:

1. Demonstration Model 1 (DM1, cold section)
2. Structural Model 0 (SM0, cold section chip)
3. Structural Model 1 (SM1, cold section assembly)
4. Trade-off models (for thermal and athermal models validation, cold section)
5. Technology validation models (cold section)
6. Mechanical test structures (cold section)
7. Proto-EM (cold section)
8. WE BB (warm section)
9. Structural Model 2 (SM2, cold section)
10. EM Cold Assembly

In the following sections, for each model we are going to identify the Layout, the Objective, and the Number of samples.

#### 5.1.1 Demonstration Model 1 (DM1)

The DM1 is focused to the critical technologies and to the detector design.
Layout:

- single pixel
- suspended absorber
- square geometry
- mechanical bracket (SRON design)
- pcb SQUID prototype
- cold interconnection by loom soldered on one side and terminated by a SRON-like pcb connector on the opposite side

Objective:

- detector concept demonstration
- first assessment of the technologies affecting the CryoAC cold stage development
- compatibilty test with the DM TES array

Number of samples: 1

The DM1 has been already developed and tested with results compliant with the DM CryoAC requirements. It has been also delivered to SRON in April 2019. Integration at chipset level are on-going.

#### 5.1.2 Structural Model 0 (SM0)

The SM0 is focused to the verification of the compliant geometry and micromachining with the foreseen mechanical environment.
Layout:

- chip hexagonal geometry
- segmented and monolithic
- mechanical constraints representative of the final configuration

Objective:

- first assessment of the chip design
- first assessment of the micromachinnings

- first assessement of the chip elastic proprieties (eigen frequencies, displacement, modes, robustness)
- first comparison with the FEM model analyses [RD7] [RD8]
- first mechanical qualification of the chip stand alone in relevant environment (sine and random vibration)
- first assessment of the chip glueing procedure vs curing temperature

Number of Samples: 10

#### 5.1.3 Structural Model 1 (SM1)

The SM1 is focused to the detector design.
Layout:

- chip hexagonal geometry
- final chip layout (segmented or monolithic)
- mechanical bracket derived from the DM design, not representative of the external I/Fs to FPA

Objective:

- consolidation of chip layout (pads)
- first assessment of the mechanics
- first assessement of the pcb + cold interconnection
- first assesment of the assembly
- FEM model
- development and first mechanical qualification of the assembly in relevant environment (cooling down, sine, quasi-static and random vibration)

Number of Samples: 3

#### 5.1.4 Trade-off models (for thermal and athermal models validation)

Such models are focused on the detector design.
Layout:

- 1 DM-like as shape (1 cm^2 supsended absorber, 96 TES in parallel connected)
- 1 single pixel with special TES layout

Objective:

- the DM-like is used for thermal validation
- the single pixel is used for the athermal model validation
- experimental data from these models are crucial to support the closure of the trade-off studies

Number of Samples: 2

#### 5.1.5 Technology validation models

Such models are focused only on the technology development.

Layout:

- DM-like detector shape (# 4)

- Specific test structures (# 10)
- full scale detector shape (# 6)

Objective:
- validation of the manufacturing procedures
- TRL-5 demonstration of the most critical technologies

Number of Samples: 20

#### 5.1.6 Mechanical test structures

Such test structures are focused only on the design definition.

Layout: Si beams having size representative of the EM, characterized by 3 different orientations wrt the Si main lattice axes

Objective: modellig of the Si beams into the FEM model taking into account 4 different mechanical stress applied (bending, shearing, compression, torsion)

Number of Samples: 10*3*4 = 120

#### 5.1.7 Proto-EM

This model is focused on both the technology and the design development.

Layout:
- hexagonal geometry
- monolithic or segmented configuration (as selected from the trade-off study)
- SM1 mechanical bracket
- SM1 CFEE made of pcb mechanical shape + cold interconnection
- 1 or 2 operative readout chain

Objective:
- validation of the mechanical design towards the EM development
- technology demonstration of the CFEE
- completion of the TRL5 demonstration path with all the critical technolgies operating simoultaneously
- mechanical verification in representative environment (TBC)

Number of Samples: 1

#### 5.1.8 WE BB

This model is focused on the WE design development.

Layout:
- WFEE representative layout and partially populated
- WBEE main functions implemented in not representative layout

Objective:

- First assessment of the WE EM design
- First end-to-end CryoAC test based on Proto-EM + WE BB

Number of Samples: 1

#### 5.1.9 Structural Model 2 (SM2)

This model is focused on the EM design development.

Layout:

- Revision of the SM1 mechanics based on test feedbacks
- FPA representative i/f
- hexagonal chip, monolithic or segmented configuration (as selected from the trade-off study)
- Proto-EM CFEE + cold interconnection

Objective:

- mechanical validation towards the EM design
- vibrations at FPA chipset level

Number of Samples: 3

#### 5.1.10 EM Cold Assembly

This model is focused on the EM cold part development.

Layout:

- SM2 mechanics
- FPA representative i/f
- hexagonal chip, monolithic or segmented configuration (as selected from the trade-off study)
- Proto-EM CFEE + cold interconnection
- 4 operative readout chain (TBC)

Objective:

- validation of the CryoAC cold stage design in representative environment
- test and qualification at FPA level

Number of Samples: 3 (nominal, backup, and reference model)

## 6 LIST OF TECHNOLOGICAL PROCESSES

The CryoAC chip is the product of the following processes shown in Fig. 6.

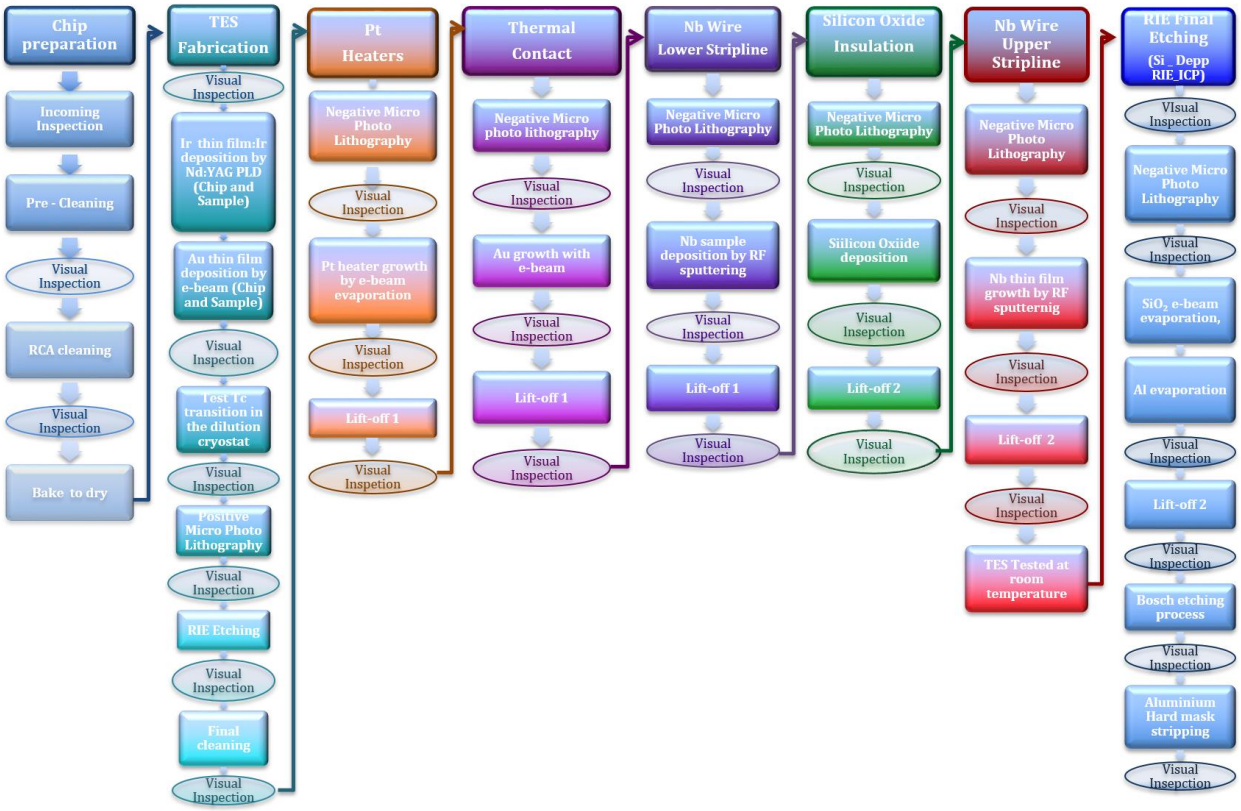


**Fig. 6 - CryoAC DM Chip Manufacturing Process Flow.**

After each main process a visual inspection is performed not only to verify the result of such a process, but also to verify the cleanness to avoid contaminants, as particles for example, that could negatively affect the following process.
Inside the present plan we will focus only on the cleanliness aspects potentially impacting on the performance of the most critical technologies.
Each process is carried out by following the related procedure shown in Table 2.

| Process | Procedure |
|---|---|
| Negative Micro Photo Lithography | XIFU-UNGE-CRA-PR-0001 |
| Positive Micro Photo Lithography | XIFU-UNGE-CRA-PR-0002 |
| RIE Etching for TES Fabrication | XIFU-UNGE-CRA-PR-0003 |
| E-beam Deposition | XIFU-UNGE-CRA-PR-0004 |
| Nb thin film deposition | XIFU-UNGE-CRA-PR-0005 |
| Incoming Inspection | XIFU-UNGE-CRA-PR-0006 |
| Pre - Cleaning | XIFU-UNGE-CRA-PR-0007 |
| Visual inspection at sight and under a microscope | XIFU-UNGE-CRA-PR-0008 |
| RCA clean | XIFU-UNGE-CRA-PR-0009 |
| Bake | XIFU-UNGE-CRA-PR-0010 |
| Ir thin film deposition | XIFU-UNGE-CRA-PR-0011 |
| Final cleaning | XIFU-UNGE-CRA-PR-0012 |
| Lift off 1 | XIFU-UNGE-CRA-PR-0013 |
| Lift off 2 | XIFU-UNGE-CRA-PR-0014 |
| Al evaporation | XIFU-UNGE-CRA-PR-0015 |
| Bosch process | XIFU-UNGE-CRA-PR-0016 |
| Aluminium hard mask stripping | XIFU-UNGE-CRA-PR-0017 |

**Table 2 - Process Procedures according to the chip manufacturing process flow.**

To conclude this section, the Declared Material and Process lists are configured as follows:

- DML: XIFU-UNGE-CRA-LI-0001_X-IFU CryoAC Declared Material List
- DPL: XIFU-UNGE-CRA-LI-0002_X-IFU CryoAC Declared Process List

# 7 CRITICAL TECHNOLOGIES/PROCESSES TO GET THE TRL5

## 7.1 INTRODUCTION

The most critical processes to be probed are:

1. Ir/Au deposition
2. TES patterning in RIE
3. Nb wiring deposition
4. Silicon Deep-RIE

The TRL5 demonstration, is based on the following assumption:

1. we consider “Ir/Au deposition + TES pattering in RIE” as not independent processes since the validation is got by verifying the compliance of Tc, Rn, and ΔTc with the related target values. Those values depend on the patterning process as well from the Ir/Au deposition .
2. Nb wiring is an indpendent process wrt the TES fabrication since the superconductive circuit can validated as stand alone process by terminating with dummy TES film with known resistance .
3. the Si DRIE is independent from all the other processes, and can be validated as standalone process

The process flow to arrive at the TRL5 demonstration is structured as follows:

1. Single process validation, i.e., all the above processes has not to operate simultaneously to get validation. At this stage the most critical technologies 1-3 are validated separately and, when necessary, on a full scale chip area (i.e., EM).
2. Final TRL5 demonstration. At this stage the most critical technologies are validated in a h/w where they operate simultaneously.

## 7.2 SINGLE PROCESS VALIDATION

### 7.2.1 Ir/Au bilayer deposition + TES pattering in RIE

**Heritage**

Iridium is superconducting metal which bulk critical temperature of Tc=112mK. We have selected Iridium for the CryoAC’s TESs because of the excellent mechanical, thermal and chemical stability. The Tc of thin films of 120-160 nm are higher than the bulk one, therefore we grow typically 50-80 nm, of gold to adjust the final Tc to 100 mK about. Once the film has been produced this is positively lithographed and etched in RIE argon plasma.

The fabrications of iridium films last back to the middle of ’90 when we have developed the Pulsed Laser Deposition (PLD) with infrared NdYAG laser method for film growth. The method has the advantage to achieve excellent adhesion onto silicon at room temperature instead of heating the silicon substrate at T > 450 °C. This avoids cross contamination in particular from magnetic species

(iron, chromium, …) that suppress the superconductivity of iridium if present at level of 10-10 ppm. PLD film growth has two main drawbacks: limited thickness uniformity due to narrow angular emission and possible presence of droplets sub and micron sized. After more than 20 years of development both issues have been solved in many industrial and laboratory applications. Uniformity at 1% over 6" wafers has been already demonstrated (see for example [RD6]) and vacuum stage for substrate movements are available. Similar considerations apply to droplets elimination: laser scanning, cross beams and velocity filter can efficiently reduce the droplets density to negligible values These two upgrades has been planned in order to enlarge the uniformity area at the size of SM and EM and

**Current status**

Our PLD system is very well suited for Ir film growth being in Ultra High Vacuum (pressure: $10^{-10}$-$10^{-9}$ mbar) and fully dedicated only to this metal in order to minimize the risk of cross-contamination. The system and the processes have been specialized for +/- 5% uniformity over 10 mm size, that is sufficient for the DM CryoAC, because the Tc varies weekly with the film thickness at value greater than 120 nm. The PLD production system need to be upgraded with commercial automatic rastering stages for samples and laser beam (for example see https://www.surface-tec.com) in order to the meet the uniformity requirements for the larger area of the Structural and Engineering models hexagonal shape. We have produced 19 samples with the DM Ir/Au TES configuration with 2 failures (not working sample) and 2 out of specifications (working sample). The main issue to be addressed is the Tc/Rn reproducibility with narrower band of acceptance and good uniformity over 30 mm size.

**Roadmap towards TRL5**

**Layout 1:** TES shaped like long strip with resistance per square equivalent to single DM's TES.
N. of samples: 10
Pre-conditions: pre-cleaning and RCA cleaning, existing PLD system.
Success criteria: t(Ir) (absolute thickness with optical profilmeter), Tc, Rn. Yield.
t(Ir) = 150 nm + t(Au)=50 nm +/- 5%
Tc = 100 mK +/- 5% TBC
Rn = calculated as total resistance of series of square in the long strip +/- 10% (TBC)
0 1mK<DTc<2mK

**Layout 2:** array of TES with shape like DM over the area with the size of Structural and Engineering models
N samples: 3
Pre-conditions: pre-cleaning and RCA cleaning, upgraded PLD system for large uniformity area.
Success criteria: t (absolute thickness with optical profilometer), $\Delta$t/tcenter (uniformity (tmax - tmin)/tcenter), Tc, $\Delta$Tc, Rn. All samples within the criteria. Yield.

t(Ir) = 150nm +/- 5% (TBC)
Tc = 100 mK +/- 5% (TBC)
Rn = +/- 10% equivalent to total resistance for the number of squares in series(TBC)
0.5 mK < $\Delta$Tc < 1 mK

### 7.2.2 Nb wiring

Niobium films are produced for connecting the TESs on the CryoAC to the external circuitry and SQUID current to voltage amplifier. Niobium is produced by Radio Frequency Magnetron Sputtering (RFMS) in Ultra High Vacuum (base pressure 1-3 x $10^{-8}$ mbar). RFMS is the main method for producing Nb film of good quality and transition temperature Tc from 6 to 8 K about.

The film is produced with negative lithographic process, in which the sample, covered with developed PMMA, cleaned with oxygen plasma, is inserted in the chamber for the deposition in Ar plasma of RFMS. The fabrication of the connecting striplines require 3 consecutive processes of negative lithography: in the first one, the bottom Nb strip (about 300 nm thick), is grown onto the silicon, in the second one a $Si_xO_{2-x}$ insulating layer (about 400 nm thick) is deposited and, in the third one, the top Nb strip (about 700 nm) complete the connections. We were unable to observe the critical current of the Nb striplines under operation till ~ 10 mA, which is typically used to perform I-V curve having the DM CryoAC at Tb = 50 mK.

**Current status**

We have produced 25 full wired samples, with 14 failures due to singular defects in the connection (part of the film pulled away), shortcut due to breakdown by static charges, metal bad adhesion or not reproducibility of Tc in only Iridium TES samples. Sample belonging to this class of failures show unexpected and suddenly low resistance at room temperature after handling and shipping. We have observed that shortcutting the striplines with temporary bonded wires, prevent this failure.
A critical issue that has been under investigation for longtime is the presence of a low current induced superconducting to normal transition of some part of the connections that give rise to tents of mOhm series parasitic resistance (Rp(I)). We have observed unambiguously that this resistance is located on the active area of the DM CryoAC and the size of the critical current is attributable to very small cross section conducting path in Nb.We have performed a structural study at FIB-SEM after in which we have found breaks in Nb/ $Si_xO_{2-x}$/Si or Nb/Ir-Au at the covering steps wiring/wiring crossing and wiring/TES that are compatible with the expected cross-section reduction. The cause has been attributed to stress release during film growing in presence of steep edge. The fab process has been analyzed and adjusted in order to increase the sloping at the edges, testing several methods and adjusting the film thicknesses consequently. Presently there is the indication that the issue seems resolved, having obtained first few samples with small or negligible parasitic resistance.
Last issue that causes shortcut are pinhole in the stripline. Even if the surface cleaning has been substantially improved residual metal droplets sticked to the surface can cause pinhole in the stripline. Most of them are surely produced by the PLD and therefore the expected upgrade with a speed selector should prevent the formation. Others are deposited in the RIE chamber because of low temperature process. The upgrading of RIE, which is under way, should allow re-deposition free processes.

**Roadmap towards TRL5**

Layout: single pixel DM-like with new process for sloped edges of insulating $Si_xO_{2-x}$ film, dummy TES,
N samples: 3
Pre-conditions: pre-cleaning, RCA cleaning, new process for sloped edges of insulating $Si_xO_{2-x}$ film
Success criteria: single Nb transition, null Rp, no shortcut due to pin-hole.

No full scale area validation.

### 7.2.3 Si DRIE (Inphotech)

**Heritage**

We have developed our Deep Reactive Ion Etching (DRIE) process for a full etching through the wafer starting from the Oxford Plasma Technology primitive recipe for PlasmaPro 100 Cobra ICP at our premise in Inphotec. The basic process is a Bosch with high density plasma with ICP (our plasma pressure is 30-50 mTorr) with a two steps cycle:

1) Deposition step, to create a passivation layer
2) Breakthrough step, to remove the passivation on the bottom, preserving it on the sidewalls.

3) Etch Step isotropic etch removing material more on the non-passivated regions

High-Rate 3-steps Bosch used to produce sample SM0 test structures consists in seven stages plus a landing stage, cycles numbers: 905, temperature 5°C, using SF6 and C4F8 gases. The suitability of silicon oxide mask 2.5 μm thick was demonstrated.

**Current status**

Sidewall verticality:
The whole chip thickness (535 μm) was etched obtaining a profile with a slope, for Sample SM-0 test structures, ϴsem = 91°.

Sidewalls textures:
Current process target: hi, vi ≤ 2.5 μm.

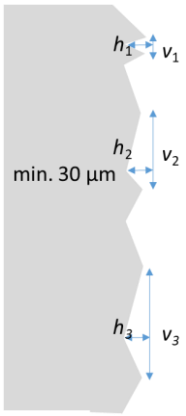


**Fig. 7 - Sketch of the sidewall cross section of DRIE process at Inphotec.**

Top and bottom sizes:
Current result for Sample SM-0 test structures require adjustments. In the latest experiments major notching was avoided.

Erosions, stains and particles on unprocessed surfaces:
Current results for SM-0 test structures shows some residuals due to the immobilization/detachment chips procedures. Cleaning procedure must be improved and finalized.

As backup facilities a plasma lab 100 plus is available in Genova, already used with success for the fabrication of the SM-0 and DM models, giving us a good average verticality of the sidewalls, Θ = +/-1° with an average aspect ratio of the sidewall not greater than 5μm/525μm.
At these facilities we have manufactured the 10 SM-0 samples undergone to the vibration tests.

**Roadmap towards TRL5**
Layout: hexagonal shape only silicon (segmented or monolithic as selected by the trade-off study)
N samples: 3
Pre-conditions: pre-cleaning, RCA cleaning, Inphotec Bosh recipe
Success criteria: measurement of average aspect ratio, scallop size, roughness, absence of grass, absence of notches and footing.

### 7.3 FINAL TRL5 DEMONSTRATION

The final TRL5 demonstration will be carried out by using the Proto-EM model.

## 8 PLANNING

In Fig. 8 the schedule of the CryoAC development activities foreseen until the delivery of the EM CryoAC cold stage.
Highlighted in orange the tasks associated to the demonstration of the technologies at single process level, and at assembly level.

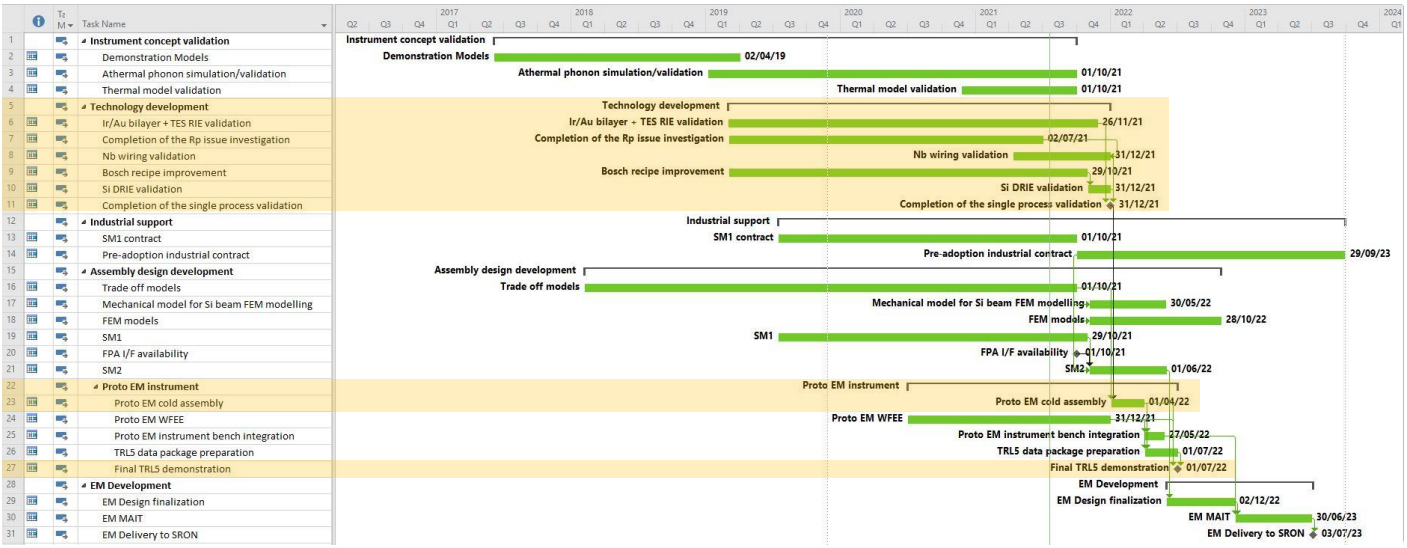


**Fig. 8 - Planning**

## 9 CONCLUSION

Following the CNES address, we have divided the items related to the technology demonstration with respect to the items related to the development of the design.
This approach allows to mitigate the potential impact on the schedule due to the coupling between technology and design development.
This Technology Demonstration Plan will be part of the CryoAC Development Plan which will include also the justification of the models here reported and used for the development of the design.