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Large-scale sub-5-nm vertical transistors by van der Waals integration

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Vertical field effect transistor (VFET), in which the semiconductor is sandwiched between source/drain electrodes and the channel length is simply determined by the semiconductor thickness, has demonstrated promising potential for short channel devices. However, despite extensive efforts over the past decade, scalable methods to fabricate ultra-short channel VFETs remain challenging. Here, we demonstrate a layer-by-layer transfer process of large-scale indium gallium zinc oxide (IGZO) semiconductor arrays and metal electrodes, and realize large-scale VFETs with ultra-short channel length and high device performance. Within this process, the oxide semiconductor could be pre-deposited on a sacrificial wafer, and then physically released and sandwiched between metals, maintaining the intrinsic properties of ultra-scaled vertical channel. Based on this lamination process, we realize 2 inch-scale VFETs with channel length down to 4 nm, on-current over 800 A/cm^2, and highest on-off ratio up to 2×10^5, which is over two orders of magnitude higher compared to control samples without laminating process. Our study not only represents the optimization of VFETs performance and scalability at the same time, but also offers a method of transfer large-scale oxide arrays, providing interesting implication for ultra-thin vertical devices.

Vertical field effect transistors (VFETs), where the semiconductor channel is sandwiched between source and drain electrodes, have demonstrated promising potential for ultra-scaled transistors, wearable electronics, photoelectric devices and high-density devices[1–5]. Within the vertical geometry, the top metal and bottom graphene electrodes are integrated at two sides of the semiconductor channel with a sandwich structure. Here, the bottom electrode is graphene and is essential due to its low density of states and weak electrostatics screening, where the gate electrical field could effectively penetrate and modulate the vertical carrier transport efficiency[5,6]. Based on this unique device structure, the channel length of VFET is simply determined by the semiconductor thickness and thus can be scaled down to sub-5 nm regime[3,7,8]. This is in great contrast to conventional planar transistors, where the source and drain electrodes are laterally patterned on two ends of the semiconductor channel[9–11], and the device channel length is largely limited by the resolution of fabrication processes (e.g., ultra-violet lithography, implantation), yielding a longer channel length > 10 nm (ref. 7).

However, despite extensive efforts over the past decade, the absence of a scalable method to fabricate short channel VFETs remains a critical challenge. Previous approaches to realizing VFETs were often limited by the trade-offs between device scalability and its channel length[5]. For example, two-dimensional (2D) semiconductors (such as MoS_2, WSe_2) have been widely used as the channel materials for VFETs,

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because they can be easily stacked on top of the bottom graphene electrode with atomic clean van der Waals (vdW) interfaces[12–14]. Therefore, these proof-of-concept devices have demonstrated high device performance with current density over 1000 A/cm^2, short channel length down to 1 nm (as determined by 2D layer thickness), on-off ratio over 10^3, and ultra-scaled vertical pitch size of 20 nm[3,7,15,16]. However, the synthesis of large-scale 2D channel remains challenging[17], particularly for VFETs that need multilayer channel with desired thickness (rather than monolayer channel used in planar devices), limiting the scalability of 2D based VFETs for practical application. To improve scalability, organic semiconductors and oxide thin films have been used as the channel materials of VFETs, owing to their wafer-scale processing capability with well-controlled thickness[18–21]. However, applying these scalable materials often lead to inferior device performance and larger channel length. For example, organic VFET shows a much lower current density <5 A/cm^2, which could be largely attributed to the longer channel length and low carrier mobility in vertical direction[19]. On the other hand, oxide semiconductors did exhibit improved carrier mobility, however, the deposition of high-quality oxide films usually involves high energy process or chemical reaction (such as sputtering or chemical vapor deposition), which could easily damage the bottom graphene electrode[22,23]. Hence, current oxide VFET typically involves a more complicated top-gate structure (inverted structure) at the sacrifice of channel length, output current and gate dielectric performance[5,24,25]. Therefore, up to date, the simultaneous achievement of large-scale VFETs and ultra-short channel remains challenging, greatly limiting its practical application and further development.

Here, we demonstrate a layer-by-layer transfer process of large-scale oxide semiconductor arrays and metal electrodes, and realize large-scale VFETs with ultra-short channel length and high device performance. Within this process, indium gallium zinc oxide (IGZO) layer could be pre-deposited on a sacrificial wafer via high-energy magnetron sputtering, and then physically released and transferred on top of the graphene, avoiding conventional fabrication-induced damages to bottom graphene electrode. In the meantime, vdW metal integration approach is also applied as the top electrode, maintaining the intrinsic properties of ultra-scaled vertical channel and reducing its vertical leakage current. Together, we realize 2 inch-scale IGZO VFETs with channel length down to 4 nm, on-current over 800 A/cm^2, and on-off ratio up to 2×10^5, representing the optimization of VFET performance and scalability at the same time. Detailed thickness-dependent measurements are further conducted, confirming the optimized performance are originated from the ultra-clean vdW interfaces within both top and bottom metal-semiconductor contacts. Our study not only optimizes the VFET performance and scalability at the same time, but also provides a large-scale layer-by-layer transfer process of oxide semiconductors, which could provide interesting implication for construct other ultra-thin vertical devices that are previously limited by fabrication difficulties.

Results

Fabrication processes of large-scale oxide VFETs

Figure 1a-f schematically shows the device structure and fabrication processes of large-scale IGZO VFETs, and the corresponding optical images are also included. To fabricate the devices, thin layer polymethyl methacrylate (PMMA, ~200 nm thickness) and polyvinyl alcohol (PVA, ~9 nm thickness) are first spin-coated on a SiO_2 wafer as a bilayer buffer. Next, IGZO films are directly sputtered on top of the polymer buffers via radio-frequency sputtering in large-scale (Fig. 1c), and the thickness of oxide film could be well controlled through the sputtering time and speed, as detailed in Supplementary Fig. 1 and “Methods” section. Furthermore, the IGZO film (with underlayer PVA buffer layer) could be mechanically peeled-off from the sacrificial substrate using a designed polydimethylsiloxane (PDMS) stamp (Fig. 1d), and the exposed bottom PVA layer could be dry-etched through gentle nitrogen plasma treatment (60 W, 90 seconds), as schematics illustrated in Fig. 1e and Supplementary Fig. 2. The mechanical-peeling and dry-etching processes here are important to avoid solution-induced strains during wet-etching process[26,27], and is essential to ensure an ultra-thin and uniform oxide semiconductor layer in large-scale without any cracks and residues, as shown in the control sample in Supplementary Fig. 3. Finally, the released IGZO film could be laminated onto graphene monolayer arrays using optical microscopy with customized designed transfer platform and alignment process is detailed in “Methods” section, leading to the formation of graphene/IGZO bottom contact in large scale (Fig. 1f and Supplementary Fig. 4).

We note the PMMA/PVA bilayer buffer is essential here for transferring ultra-thin IGZO layer with large-scale uniformity, due to following reasons[26]. First, PVA layer is spin-coated with ultra-thin thickness (< 10 nm), hence could be easily dry-etched using gentle plasma treatment. Second, the thin PVA layer still demonstrate atomic flat surface (~0.36 nm roughness), which is essential to deposit ultra-thin and flat IGZO layer. For other polymer buffer layers such as polyimide (PI) or polypropylene carbonate (PPC), achieving sub-10 nm thickness with atomic flat surface is challenging. Third, strain is unavoidable during transfer process during the bending of the holding substrate, especially for large-scale transfer of IGZO film with brittle lattice. Using 9 nm thin PVA layer here, the applied strain during the dry-transfer process could also be minimized since strain is proportional to the substrate thickness, leading to uniform and large-scale oxide layer without any cracks. Finally, although PVA shows desired properties for transferring IGZO film, it exhibits strong adhesion force with the SiO_2 substrate (after IGZO sputtering), and cannot be mechanically peeled-off, leading to the failure of IGZO film transfer (Supplementary Fig. 5). To overcome this challenge, we deposited another PMMA layer prior to PVA to realize a PMMA/PVA bilayer buffer, where the top PVA layer demonstrates low adhesion force with bottom PMMA layer and can be easily mechanically peeled-off (with IGZO films) from the sacrificial PMMA/SiO_2 substrate.

Furthermore, the yield of IGZO transfer process is important for scalable vdW integration and further construction of VFETs. To calculate device yield, we have batch-fabricated 9216 graphene/IGZO devices (64 × 144 arrays) and examine the IGZO transfer rate through optical images. Among all devices, 8842 patterned IGZO films are successfully transferred (Figs. 1g–i), representing a high process yield ~96%. We note the failed devices largely originated from devices loss during the IGZO patterning process, due to the relatively weak adhesion between IGZO and PVA buffer layer (compared with the strong interaction force between IGZO and conventional SiO_2 substrate), as shown in Supplementary Fig. 6. In the meantime, we also note the air bubbles, wrinkles and IGZO cracks are not observed across the whole wafer, indicating the high uniformity and reliability of our oxide transfer process.

Fabrication and switching mechanism study of VFETs

To further highlight the importance of the IGZO transfer process. We have also fabricated control samples by directly sputtering IGZO channels on graphene bottom electrode, and examined the graphene quality through both optical and electrical measurement. As shown in Fig. 2a, the intrinsic graphene (before IGZO sputtering) exhibits G and 2D peaks at 1583 cm^{-1} and 2697 cm^{-1}, respectively, consistent with previous literature and indicating its monolayer nature[28]. After directly sputtering IGZO on top, the graphene 2D peak disappears, while the defects D peak emerges and dominates the whole spectrum (Fig. 2a), suggesting the monolayer graphene lattice is largely destroyed during the IGZO sputtering process[29,30]. The sputtering induced damages can be further verified through electrical measurement of graphene.

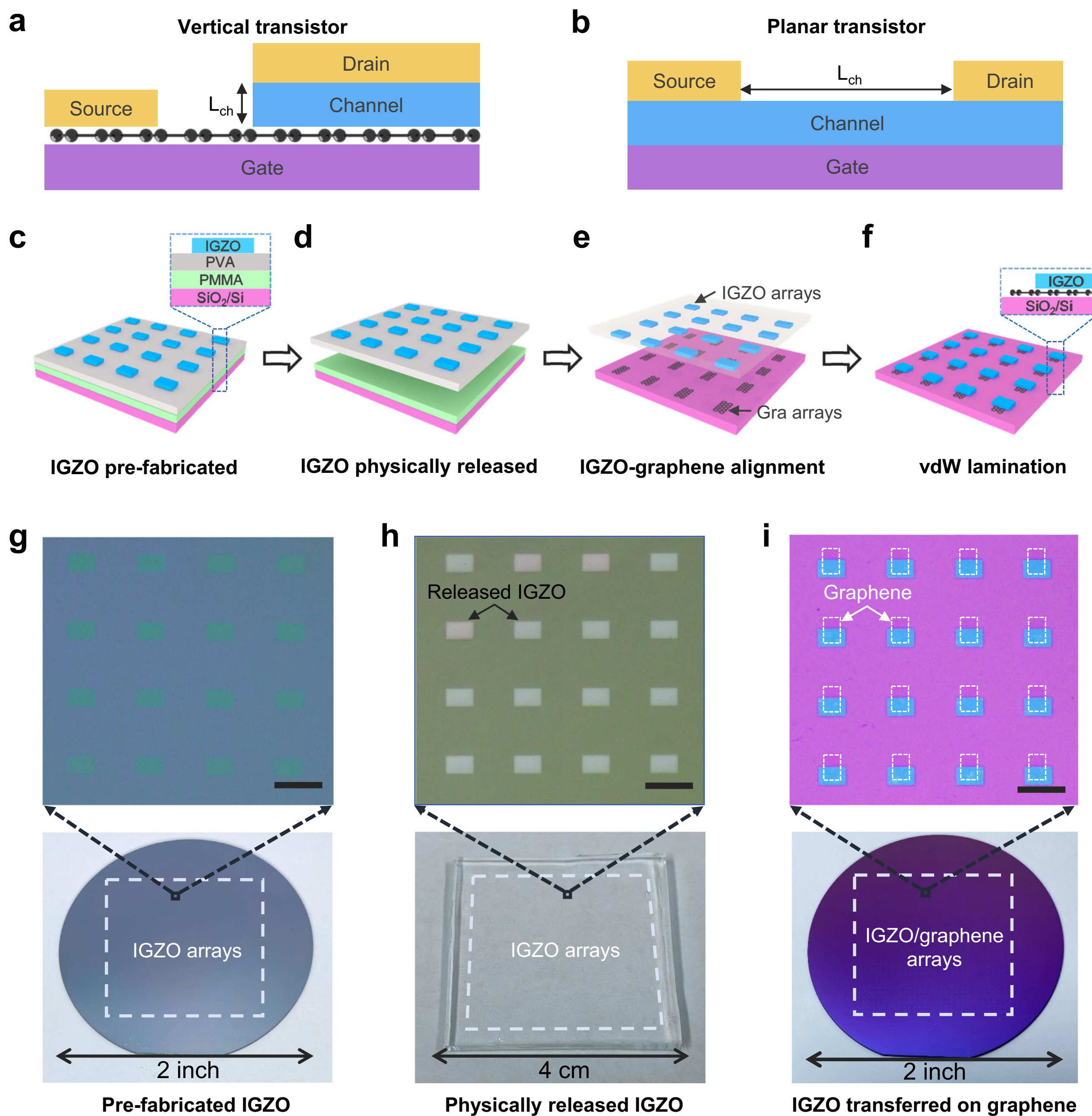

Fig. 1 | Device structure and fabrication processes. a, b Schematical illustration of a graphene-based vertical field effect transistor (FET) (**a**) and conventional planar FET (**b**). **c**–**f**, Schematical fabrication processes of the vdW indium gallium zinc oxide (IGZO)/graphene arrays, including four steps: (**c**) pre-fabrication of IGZO arrays, (**d**) physical peeling of IGZO through polymer encapsulation, (**e**) alignment of IGZO with graphene under optical microscope, (**f**) van der Waals (vdW) lamination of IGZO arrays on the graphene arrays. **g**–**i** The corresponding optical images and the photos of the large-scale lamination processes for pre-fabricated IGZO (**g**), physically released IGZO (**h**), as well as IGZO transferred on graphene (**i**). The scale bar is 50 µm. L_{ch}, channel length.

As shown in Fig. 2b, the intrinsic graphene exhibits clear bipolar transfer behavior with a low sheet resistance of ~500 Ω sq^{-1}; while after sputtering IGZO on top, graphene device is totally open circuit with only noise signal measured (< 10^{-13} A). This behavior is in great contrast to our vdW integrated IGZO/graphene junction. As shown in Fig. 2c, the 2D and G peaks of graphene remain unchanged before and after transferring IGZO on top, indicating the graphene lattice is well retained during the IGZO integration process. In the meantime, the graphene transistor also exhibits identical transfer curve after IGZO integration (Supplementary Fig. 7), suggesting the IGZO vdW integration won't alter its electrical properties.

With the ability to construct large-scale IGZO/graphene bottom contacts, we could further build up large-scale VFETs by depositing Ti/Au or Ag/Au metal (20/30 nm thick) on IGZO as the top electrode. As shown in Figs. 2d–f, 9000 IGZO VFETs are realized across a 2-inch wafer, exhibiting a well retained sandwich structure. We note the lateral device footprint could be further reduced using cross-bar structure, as demonstrated in Supplementary Fig. 8.

Electrical measurements of IGZO VFETs are further conducted at room temperature within a vacuum probe-station. For all electrical measurements, the bottom graphene contact is always grounded as source electrode, the top Ti/Au metal is biased as drain, back-gate voltage is applied on the highly doped silicon, and the gate dielectric is 300 nm thick SiO_2, as labeled in the schematic in Fig. 2g. In general, a negative gate voltage p-dopes graphene, leading to large Schottky barrier with n-type IGZO channel, and the device is at off-state with a

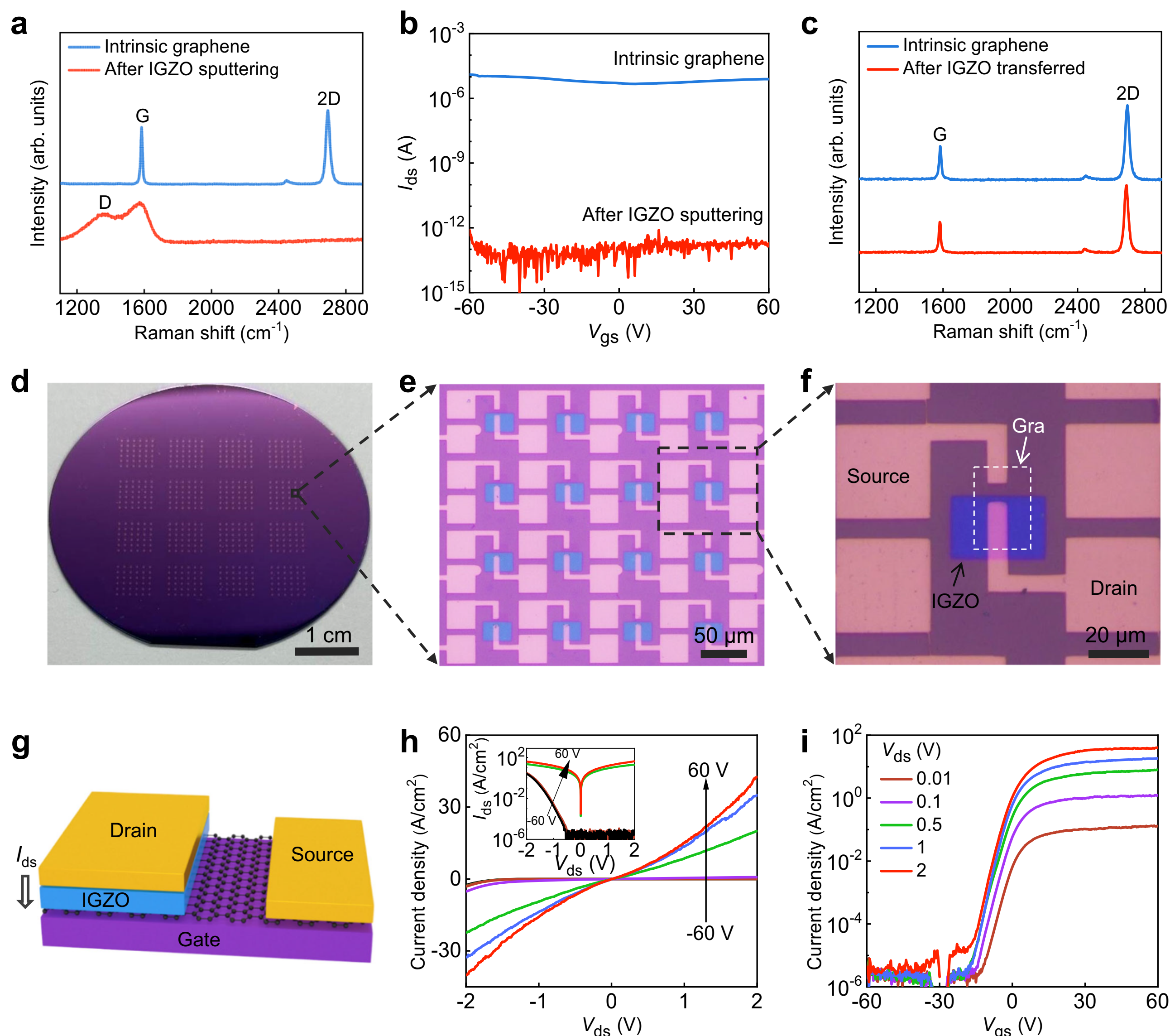

Fig. 2 | Characterization of vdW IGZO vertical transistors. Raman spectra (**a**) and I_{ds}-V_{gs} transfer curves (**b**) of intrinsic graphene as well as the graphene device after directly sputtering IGZO film on top. After directly IGZO sputtering, the graphene 2D peak disappears and the transistor lost electrical conductivity, indicating the high-energy sputtering process is not compatible with graphene lattice. **c** Raman spectra of intrinsic graphene and graphene after transferring IGZO film, where the unchanged Raman signal suggest the transfer process won't impact the intrinsic properties of monolayer graphene. **d**–**f** Photo picture and zoomed-in optical images of large scale IGZO-VFETs. The white dashed box and blue rectangles are graphene and IGZO, respectively. **g** Schematic of the device structure and the current transport of a standard IGZO VFET. **h**, **i** I_{ds}-V_{ds} output curve (**h**) and I_{ds}-V_{gs} transfer curve (**i**) of a typical IGZO-VFET with channel length of 50 nm. The inset is corresponding log plot of I_{ds}-V_{ds} output curve. The current is normalized by the overlap area between top contact and bottom contact. I_{ds}, drain-source current; V_{gs}, gate-source voltage; V_{ds}, drain-source voltage.

clear rectifier behavior, as shown in Fig. 2h (black line). On the other hand, a positive gate voltage reduces the IGZO/graphene Schottky barrier, leading to much-enhanced carrier transport efficiency and a more linear output curve, and the device is at on-state[5]. The I_{ds}-V_{gs} transfer characteristics of VFET (Fig. 2i) show clearly that the current density increases with increasing positive gate potential, demonstrating that the electrons are the majority charge carriers. We need to note the switch of VFET is realized by changing the Schottky barrier height between graphene and channel material, hence the conventional pinch-off effect and I_{ds}-V_{ds} current saturation could not occur. This device working mechanism is consistent with previous VFETs using graphene electrode[7,21]. Despite the absence of output saturation, VFET structures could still be used in various circuit applications such as wearable electronics, logic circuits, photoelectric device and high-density transistors[2,3,14,16].

To further reduce the power consumption, we have fabricated additional IGZO VFET with thinner high-κ dielectric (10 nm thick Al_2O_3 *vs.* 300 nm thick SiO_2 previously), as shown in Supplementary Fig. 9. We note that the device shows low gate voltage range down to 2 V and small gate leakage current $<10^{-12}$ A, indicating that thinner high-κ dielectric could greatly reduce the device overall power consumption. Furthermore, to analyze the driving capability of the short channel VFET, we have normalized measured current by the overlapping area of the top metal electrode and the bottom graphene[3]. As shown in Figs. 2h, i, the highest on-state current density is 42 A/cm^2 for devices with 50 nm channel length (50 nm thick IGZO), which is over one order of magnitude higher compared to organic-based VFETs with similar thickness[18,19], and could be largely attributed to the better conductivity of oxide semiconductors and higher carrier mobility within vertical direction.

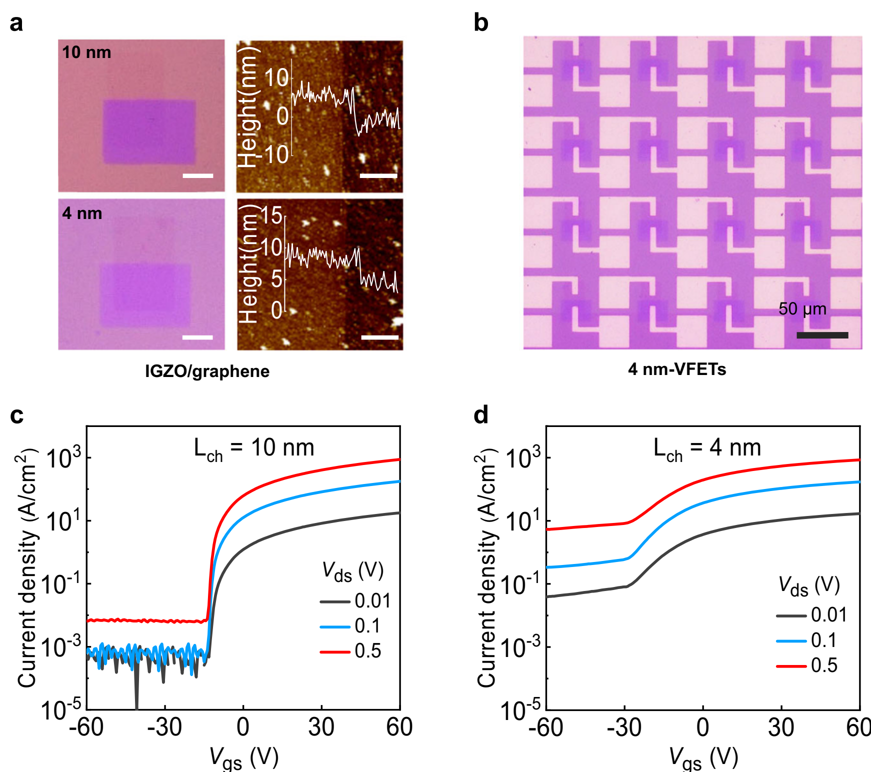

Fig. 3 | Electrical characteristics of IGZO-VFETs with different channel length. **a** Optical and corresponding AFM images of IGZO/graphene with various IGZO thickness, the scale bar for optical images is 10 μm, for AFM images is 3 μm. **b** Optical image of VFETs with channel lengths of 4 nm. **c**, **d**, I_{ds}-V_{gs} transfer curves of VFETs with channel length of 10 nm (**c**) and 4 nm (**d**).

Channel length dependent electrical properties

To further improve the device on-state current, we have fabricated IGZO VFETs with shorter channel length, by vdW integrating thinner IGZO films of 10 nm and 4 nm thick, as shown in Figs. 3a, b and Supplementary Fig. 10. In general, n-type I_{ds}-V_{gs} transfer characteristics is consistently observed for all devices with different channel length, indicating the n-type Schottky junction is well retained even at 4 nm channel length, as shown in Figs. 3c, d. Within a 10 nm channel length, the average on-state current is 840 A/cm^2 and the highest on-state current could reach 979 A/cm^2, which is comparable to non-scalable 2D-based VFETs with similar channel length[2,3,8,12,13,15]. With further reducing the channel length to 4 nm, the average on-state current gradually saturated with similar current density of 820 A/cm^2, as shown in Fig. 3d and Supplementary Fig. 11. Such current saturation behavior has also been observed in ultra-scaled planar transistors, and could be largely attributed to dominated contact resistance rather than the channel resistance[31]. On the other hand, although current density is not improving at sub-10 nm channel length, further channel length scaling of VFETs could still be important because it increases 'out-of-plane' integration density, where vertical transistors can be integrated by stacking different devices layer-by-layer in the vertical direction, as predicted by International Roadmap for Devices and Systems (IRDS)[32]. This is similar with scaling of conventional planar silicon transistor, where the primary motivation is increasing 'in-plane' device density, since the performance improvement of a single device is gradually saturated below 20 nm physical channel length[33]. Take one step further, planarization is also important if multiple devices are stacked in vertical direction, and the planarization layer thickness is also important for VFET scaling. Currently, the optimized total device thickness would be ~20 nm based on 4 nm channel length and 7 nm hybrid contact in our previous studies[16,26] (as schematically illustrated in Supplementary Fig. 12), hence developing a planarization layer with similar thickness would be an interesting topic for further investigation.

Besides on-state current density, on-off ratio is another important device parameter related to VFETs. As shown in Fig. 3c, VFET with 10 nm channel length shows highest on-off ratio of ~10^5, much higher than the VFETs with 2D channels[3,8,12,13], and could be largely attributed to the larger band gap of oxide semiconductor (e.g., ~3.3 eV for IGZO, ref. 34) With decreasing the channel length, the on-off ratio of the VFETs decreases, eventually reaching ~10^2 for devices with 4 nm channel length (Fig. 3d). As shown in Figs. 3c, d and Supplementary Fig. 11, the decreased on-off ratio is directly related to the increased off-state current, and could be largely attributed to two reasons. First, with decreasing channel thickness, the potential of the entire channel becomes more and more dominated by the electric field of top metal electrode, which could reduce the graphene-IGZO Schottky barrier height, resulting in the increase of field emission carrier transport (rather than pure thermionic carrier in thicker device)[7]. As the channel length is reduced to sub-10 nm regime, direct quantum tunneling current starts to emerge between the top drain and bottom graphene source, which will gradually dominate the carrier transport[35]. Second, the high energy drain deposition processes usually lead to considerable interface damage and reduce the effective channel thickness. Such highly disordered interface can lead to leakage current paths occurring underneath the top metal contact region that cannot be controlled by a gate voltage, leading to reduce on-off ratio and eventually device failure by short circuit between source and drain, as observed in 2D based VFETs (refs. 3,7).

All van der Waals VFETs using metal transfer technique

To further improve the on-off ratio of the 4 nm VFETs, large-scale vdW metal integration technique is applied, where the device structure remains unchanged and the only difference is the integration of top metal electrode. Within vdW metal integration, large-scale metal

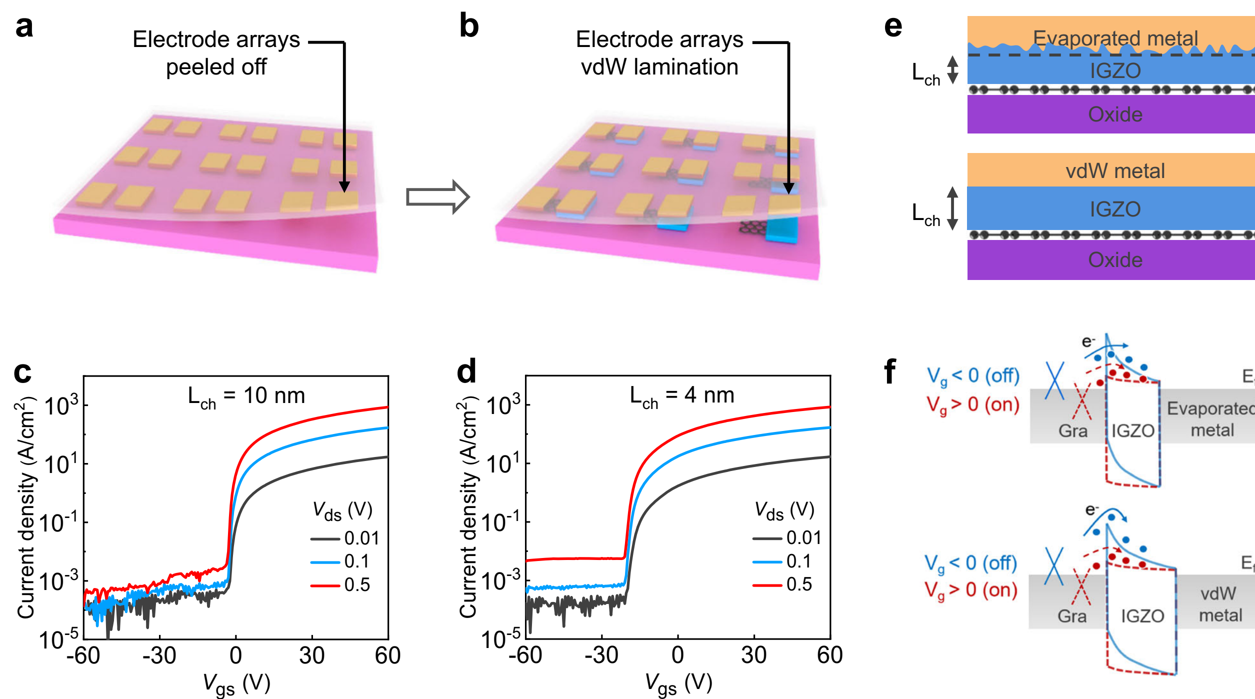

Fig. 4 | All vdW IGZO-VFETs with top metal lamination. a, b Schematical fabrication processes of all vdW IGZO-VFETs by vdW laminating the top contact metal, including two steps: (**a**) physical peeling of pre-fabricated metal arrays, (**b**) vdW lamination of metal arrays on the IGZO/graphene arrays. **c, d,** I_{ds}-V_{gs} transfer curves of all vdW VFETs with channel length of 10 nm (**c**) and 4 nm (**d**). **e** Device schematics of all vdW VFETs by laminating the top metal, exhibiting an atomic sharp top contact interfaces and is essential for ultimate channel length scaling. **f** Corresponding band diagrams for VFETs with conventional evaporated top electrode and vdW top electrode. The blue and red arrows represent the carriers cross the barrier at on-state and off-state, respectively. E_f, Fermi level.

electrode (Ag/Au, 20/30 nm thick) is pre-fabricated on a silicon sacrificial wafer, and then physically released and laminated on the surface IGZO as top contact (detailed in our previous work[36]), as shown in Fig. 4a-b and Supplementary Fig. 13. By applying vdW metal integration, both IGZO semiconducting channel and the top metallic drain are layer-by-layer transferred with weak vdW interactions in between, thus could maintain the intrinsic properties of ultra-thin IGZO channel within the sandwiched structures.

Figure 4c, d shows the I_{ds}-V_{gs} transfer characteristics of the resulting all vdW IGZO-VFETs with channel length of 10 nm and 4 nm, respectively. The on-off ratio of sub-10 nm vdW device could reach over 10^6, which is over one order of magnitude higher than the control device which using thermally deposited drain electrode (Fig. 4c). By further scaling the channel length to 4 nm, high on-off ratio of 2×10^5 is realized, two orders of magnitude higher compared with the deposited device with same channel length (Fig. 4d). The on-off ratio improvement of vdW devices is a direct result of overcoming two previous limitations. First, the intrinsic thickness of IGZO channel is largely retained by using vdW metal electrode (Figs. 4e, f), and the direct tunneling current and deposition induced metal atom diffusion can be minimized. Second, vdW metal-IGZO interface with minimized surface states could greatly reduce the fermi-level pinning effect[7,36]. As a result, the gate electrical field could efficiently modulate the carrier concentration of IGZO, leading to higher on-off ratio. In addition, the on-state current density of 10 and 4 nm-VFTEs with vdW metal electrodes are ~870 A/cm^2 and ~840 A/cm^2 (Supplementary Fig. 14), respectively, indicating the ohmic contact between IGZO and vdW top drain electrode.

Discussion

In summary, we developed a mechanical peeling method of large-scale IGZO with high processing yield, leading to the realization of all-vdW VFETs through a layer-by-layer lamination process. Based on this structure, we demonstrated large-scale IGZO VFETs with channel length down to 4 nm, on-current over 800 A/cm^2, and on-off ratio up to 2×10^5, overcoming the trade-off limitation between VFET performance and scalability. In the future, our VFET could be suitable for thin-film-transistor (TFT) for display applications. To reduce the cost in large-area fabrication, planar oxide TFT technologies usually adopt lower resolution lithography, with the resulting devices typically exhibiting low delivering current. With the design of VFETs, the ultra-short oxide channel transistors (< 10 nm) are created by using low resolution lithography to afford a delivering current greatly exceeding that of planar TFTs. Our study not only optimizes the VFET performance and scalability at the same time, but also provides a large-scale layer-by-layer transfer process of oxide semiconductors, which could provide interesting implication for construct other ultra-thin vertical devices that are previously limited by fabrication difficulties.

Methods

Material synthesis and device fabrication process

For preparation of sacrifice substrate, PMMA (495 A8, purchased from Kayaku Advanced Materials) is spin-coated (speed 4000 rpm) on SiO_2 substrate first, followed by baking at 150 °C for 5 mins. Subsequently, PVA (1 wt%) is spin-coated on top the PMMA layer (speed 6000 rpm), and followed by baking at 120 °C for 1 min.

To fabricate IGZO arrays, patterned IGZO (20 × 30 μm for each flake) arrays with different thickness is deposited on the PVA sacrifice layer via radio-frequency sputtering and the patterning process is assisted by either e-beam lithography or stencil lithography. The atom ratios of In to Ga to Zn to O for the pellet target are 1:1:1:4. The reaction pressure during sputtering is 0.7 Pa, the power is 100 W, the temperature is 300 K and the Ar is selected as shielding gas with gas flow of 15 sccm. After deposition, the IGZO array is encapsulated by a PMMA (495 A8) layer. Post annealing is used for 10 nm and 4 nm VFETs (200 °C for 10 min) to avoid the reduced film quality of ultra-thin IGZO.

The graphene was grown by chemical vapor deposition (CVD) on copper foil at 1050 °C with methane as carbon source. After growth, the graphene was transferred onto SiO_2 substrate and patterned into 20 × 30 μm strips by oxygen plasma etching with 100 W power.

Layer-by-layer alignment transfer process

The transfer process is achieved using optical microscopy with a customized designed transfer platform. To better clarify the alignment accuracy, we have schematically illustrated the layer-by-layer alignment processes. As shown in supplementary Fig. 15, the top layer is first picked up by a PDMS stamp, and aligned with the bottom layer under optical microscope. At this stage, the top layer and bottom layers are not physically contacted. By moving their relative positions using x-y stage, all alignment markers on both layers can be accurately fitted with each other, suggesting all component within top circuits are well aligned with the bottom contact. Finally, the top layer is gradually pushed towards bottom target layer using a motor-controlled manipulator in *z*-axis, leading to the contact of the top layer with bottom layer.

The alignment resolution between different layer is ~0.5 μm in our lab system, and is mainly limited by optical microscope resolution[37]. We note our alignment process essentially mimics the alignment between photo-masks and wafers within photo-lithography process, and the alignment resolution could be pushed to sub-micron scale by learning from the mature photo-lithography system.

Material characterization and electrical measurement

Atomic force microscopy (Dimension Icon made by Bruker) is applied to investigate thickness as well as surface roughness of the IGZO. Raman measurements of the IGZO/graphene heterostructures are performed via a confocal Raman imaging system (Renishaw in Via-Reflex Raman Microscope), where 532 nm laser with 1800 lines mm^{-1} grating is used. Optical images are acquired by optical microscopy (Olympus, BX53M). All electrical characteristic measurements are characterized in a Lakeshore PS-100 cryogenic probe station at room temperature in vacuum, using Agilent B1500 source measurement unit.

Data availability

Relevant data supporting the key findings of this study are available within the article and the Supplementary Information file. All raw data generated during the current study are available from the corresponding authors upon request.

References

1. Liu, Y. et al. Maximizing the current output in self-aligned graphene-InAs-metal vertical transistors. *ACS Nano* **13**, 847–854 (2019).
2. Georgiou, T. et al. Vertical field-effect transistor based on graphene-WS_2 heterostructures for flexible and transparent electronics. *Nat. Nanotechnol.* **8**, 100–103 (2013).
3. Yu, W. J. et al. Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters. *Nat. Mater.* **12**, 246–252 (2013).
4. Britnell, L. et al. Field-effect tunneling transistor based on vertical graphene heterostructures. *Science* **335**, 947–950 (2012).
5. Liu, L. et al. Graphene-based vertical thin film transistors. *Sci. China Inf. Sci.* **63**, 201401 (2020).
6. Liu, Y. et al. High-current-density vertical-tunneling transistors from graphene/highly doped silicon heterostructures. *Adv. Mater.* **28**, 4120–4125 (2016).
7. Liu, L. et al. Transferred van der Waals metal electrodes for sub-1-nm MoS_2 vertical transistors. *Nat. Electron.* **4**, 342–347 (2021).
8. Moriya, R. et al. Large current modulation in exfoliated-graphene/MoS_2/metal vertical heterostructures. *Appl. Phys. Lett.* **105**, 083119 (2014).
9. Chau, R. et al. Integrated nanoelectronics for the future. *Nat. Mater.* **6**, 810–812 (2007).
10. Cao, W. et al. 2D semiconductor FETs-projections and design for sub-10 nm VLSI. *IEEE Trans. Electron. Dev.* **62**, 3459–3469 (2015).
11. Franklin, A. D. et al. Sub-10 nm carbon nanotube transistor. *Nano Lett.* **12**, 758–762 (2012).
12. Kang, J. et al. Probing out-of-plane charge transport in black phosphorus with graphene-contacted vertical field-effect transistors. *Nano Lett.* **16**, 2580–2585 (2016).
13. Choi, Y. et al. Low-voltage complementary electronics from ion-gel-gated vertical van der Waals heterostructures. *Adv. Mater.* **28**, 3742–3748 (2016).
14. Yu, W. et al. Highly efficient gate-tunable photocurrent generation in vertical heterostructures of layered materials. *Nat. Nanotech.* **8**, 952–958 (2013).
15. Ma, L. et al. Realizing on/off ratios over 10^4 for Sub-2 nm vertical transistors. *Nano Lett.* **23**, 8303–8309 (2023).
16. Xiao, Z. et al. High-density vertical transistors with pitch size down to 20 nm. *Adv. Sci.* 2302760 (2023).
17. Phuong, V. P. et al. 2D heterostructures for ubiquitous electronics and optoelectronics: principles, opportunities, and challenges. *Chem. Rev.* **122**, 6514–6613 (2022).
18. Hlaing, H. et al. Low-voltage organic electronics based on a gate-tunable injection barrier in vertical graphene-organic semiconductor heterostructures. *Nano Lett.* **15**, 69–74 (2015).
19. Liu, Y. et al. High-performance organic vertical thin film transistor using graphene as a tunable contact. *ACS Nano* **9**, 11102–11108 (2015).
20. Heo, J. et al. Graphene and thin-film semiconductor heterojunction transistors integrated on wafer scale for low-power electronics. *Nano Lett.* **13**, 5967–5971 (2013).
21. Liu, Y. et al. Highly flexible electronics from scalable vertical thin film transistors. *Nano Lett.* **14**, 1413–1418 (2014).
22. Liu, Y. et al. Van der Waals integration before and beyond two-dimensional materials. *Nature* **567**, 323–333 (2018).
23. Wang, L. et al. A general one-step plug-and-probe approach to top-gated transistors for rapidly probing delicate electronic materials. *Nat. Nanotechnol.* **17**, 1206–1213 (2022).
24. Farmer, D. et al. Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors. *Nano Lett.* **9**, 4474–4478 (2009).
25. English, C. et al. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).
26. Lu, Z. et al. Wafer-scale high-κ dielectrics for two-dimensional circuits via van der Waals integration. *Nat. Commun.* **14**, 2340 (2023).
27. Schranghamer, T. F. et al. Review and comparison of layer transfer methods for two-dimensional materials for emerging applications. *Chem. Soc. Rev.* **50**, 11032–11054 (2021).
28. Zandiatashbar, A. et al. Effect of defects on the intrinsic strength hand stiffness of graphene. *Nat. Commun.* **5**, 3186 (2014).
29. Eckmann, A. et al. Probing the nature of defects in graphene by Raman spectroscopy. *Nano Lett.* **12**, 3925–3930 (2012).
30. Beams, R. et al. Raman characterization of defects and dopants in graphene. *J. Phys.: Condens. Matter* **27**, 083002 (2015).
31. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
32. More Moore table. (page 20, Table MM14) International Roadmap for Devices and Systems IRDS 2022 More Moore (ieee.org) https://irds.ieee.org/images/files/pdf/2022/2022IRDS_MM.pdf (2022).
33. Cao, W. et al. The future transistors. *Nature* **620**, 501–515 (2023).
34. Shi, J. et al. Wide bandgap oxide semiconductors: from materials physics to optoelectronic devices. *Adv. Mater.* **33**, 2006230 (2021).

35. Ma, L. et al. Complementary tunneling behaviors in van der Waals vertical heterostructures. *Phys. Rev. Appl.* **17**, L061004 (2022).
36. Liu, Y. et al. Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. *Nature* **557**, 696–700 (2018).
37. Lu, D. et al. Monolithic three-dimensional tier-by-tier integration via van der Waals lamination. *Nature* **630**, 340–345 (2024).

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Author contributions

Y.L. conceived the research. Y.L. and X.Y. designed the experiments. X.Y. lead the sample fabrication and electrical characterization. R.H. and Lei L. lead the IGZO deposition. Zheyi L., Y.C., Liting L., D.L., L.M., Q.T., L.K., Z.X., S.L., S.D., Zhiwei L., X.L., Yunxin L., and Y.W. contributed to the optical and electrical measurements. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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